RAM Interface

- Provides access to 1 Gbit of onboard DDR2 RAM.
- Requires modified clocking
  - Design will operate at 37.5 MHz
- Interface consists of IP Core and Wrapper.
  - Provides 8-bit data interface
  - 26-bit addressing
- Single-Step Write Operation
  - Write `data_in` to `address`
- Two-Step Read Operation
  - Request data from `address`
  - Wait for ready
  - Get data & acknowledge

Installing

- Copy 'ram_interface_wrapper.v' to your project root
- Extract the contents of IPCore.zip to the `ipcore_dir` folder in your project root.
  - If it does not exist, create it.
- Add to ISE Project
  - From ISE, select 'Project->Add Source' (NOT copy)
  - Select `ram_interface_wrapper.v` and `ipcore_dir/ram_interface.xise`

Using the RAM Interface

- General
  - reset: [input] synchronous reset
  - clk: [input] 100MHz clock
  - clkout: [output] 37.5 MHz System Clock
  - sys_clk: [input] 37.5 MHz System Clock (Yes, you have to route this yourself)
  - rdy: [output] '1' signals that the interface is ready for use.
- Writing
  - Single-operation write
  - When `write_enable` goes high, the value of `data_in` is written to loc `address`
- Reading
  - Two-operation write
  - When `read_request` goes high, the system queues a READ from loc `address`
  - When read is ready, `rd_data_pres` goes high, & data is available at `data_out`
  - When reading data, acknowledge with a `1` on `read_ack`