

Welcome to ACE Engineering Academy - online live class

Subject: **Computer Organization and Architecture**

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### **Subject**

Computer organization & Architecture

### **Chapters (Topics)**

- I. Computer Arithmetic ✓
- II. Memory Organization
- III. Secondary Memories
- IV. Basic processor organization and Design
- V. Pipeline organization
- VI. Control unit Design
- VII. IO Organization

## Chapter 2 Memory Organization

- Introduction ✓
- Memory Basics ✓
- Memory Classification ✓
- Memory Size Expansion ✓
- Primary Memory
- Secondary Memory ✓
- ROM and its design ✓
- **RAM and its design** ✓
- Memory Hierarchy ✓
- Cache Memory
- Mapping Techniques
- Different misses occurred in cache
- Different block replacement techniques
- Tag directory design
- Associative Memory

Q. A 4-way set-associative cache memory unit with a capacity of 16 KB is built using a block size of 8 words. The word length is 32 bits. The size of the physical address space is 4 GB. The number of bits for the TAG field is 20.

$$N = 4$$

C M S I Z E  
= 16 KB  
Main  
mem.  
Capacity  
= 4 GB

$$\begin{aligned} & \text{2}^{14} \text{B}, CA = 14 \\ & \text{2}^3 \text{B}, PA = 32 \\ & (PA - CA) + \log_2 4 \\ & 18 + 2 = 20 \end{aligned}$$

Q. Let the Cache and main memory be divided into equisized blocks  
partitions having 16 words. If cache has 256 blocks & main memory has 4096 blocks and Cache is 4-way set associative the number of Tag bits is

- (a) 5
- (b) 6
- (c) 7
- (d) 9

$$\log_2 \frac{MB}{S} = \log_2 \frac{2^{12}}{2^6} = 6$$

$$MB = 4096 = 2^{12}$$

$$N = 4$$

$$S = \frac{CL}{N} = \frac{2^8}{4} = 2^6$$

Q. The width of the physical address on a machine is 40 bits. The width of the tag field in a 512 KB 8-way set associative cache is 24 bits.

$$PA = 40, \quad N = 8, \quad CMW = 512K = 2^{19}$$

$$CA = 19 \quad (40 - 19) + \log_2 8 = 24.$$

Q. The size of the physical address space of a processor is  $2^P$  bytes.

The word length is  $2^W$  bytes. The capacity of cache memory is  $2^N$  bytes. The size of each cache block is  $2^M$  words. For a K-way set-associative cache memory, the length (in number of bits) of the tag fields is

- (a)  $P - N - \log_2 K$
- (b)  $P - N + \log_2 K$
- (c)  $P - N - M - W - \log_2 K$
- (d)  $P - N - M - W + \log_2 K$

$$\begin{aligned} MMW &= 2^P, CMW = 2^N \\ PA = P, CA = N &\quad (\text{PA-CA}) \\ P - N + \log_2 K &\quad + \log N \end{aligned}$$

M, m } are  
C, m } expressed  
in same  
units - Bytes.

Q. The main memory of a computer has  $2^{cm}$  blocks while the cache has  $2^c$  blocks. If the cache uses the set associative mapping scheme with 2 blocks per set, then block 'k' of the main memory maps to the set:

- (a)  $(k \bmod m)$  of the cache
- (b)  $(k \bmod c)$  of the cache
- (c)  $(k \bmod 2^c)$  of the cache
- (d)  $(k \bmod 2^{cm})$  of the cache

$$\begin{aligned} MB &= 2^{cm} \\ CL &= 2^c \\ N &= 2 \\ K \bmod C &= \frac{S}{N} \\ S &= \frac{2^c}{2} \\ S &= C \end{aligned}$$

Q. A CPU has 32-bit memory address and a 256 KB Cache memory. The Cache is organized as a 4-way set associative Cache with Cache block size of 16 bytes.

$$N = 4$$

$$PA = 32$$

$$CMW = 2$$

$$CA = 18$$

What is the size (in bits) of the tag field per Cache block?

- (a) 16 bits
- (b) 9 bits
- (c) 19 bits
- (d) 12 bits

$$(32 - 18) + \log_2 4 \\ = 16$$

Q. A computer has a 256 K Byte, 4-way set associative, write

back data cache with block size of 32 Bytes. The processor sends 32 bit addresses to the cache controller. Each cache tag directory entry contains, in addition to address tag, 2 valid bits, 1 modified bit and 1 replacement bit.

The number of bits in the tag field of an address is

- (a) 11
- (b) 14
- (c) 16
- (d) 27

$$PA = 32$$

$$CA = 18$$

$$N = 4$$

$$14 + \log_2 4 \\ = 16$$



Ex) A direct mapped Cache is having 256 blocks and physical memory is having 4096 blocks. Tag field size for each Cache line is 4 bits.

1Q) Tag field size for each Cache line is 4 bits.

2Q) Total Tag directory size is 1024 bits.

1Q)  $C_L = 256 = 2^8$ ,  $MB = 4096 = 2^{12}$   
 $\text{Tag field size} = (PA - CA) = \log_2 \frac{MB}{CL} = \log_2 \frac{2^{12}}{2^8} = 4 \text{ bits}$

$$2Q) T * CL = u * 256 = 1024$$

Tag field size in Direct mapped Cache Memory =  $(PA - CA)$

$$MB = 4096 = 2^{12}$$

$$CL = 256 = 2^8$$

$$BW = 2^x$$

$$MMW = MB \times BW = 2^{12+x}$$

$$= 2^{12} * 2^x = 2^{12+x}$$

$$(PA = 12 + x) \checkmark$$

$$CMW = CL * BW = 2^8 * 2^x = 2^{8+x}$$

$$(CA = 8 + x)$$

$$\text{Tag field size} = 12 + x - 8 - x = 4$$

(Ex)

A Direct mapped cache size is 4 K Bytes with block size of 512 Bytes.  
CPU generates 20 bit physical Address



1) Tag field size of each Cache line is 8 bits

2) Total tag directory is 64 bits

$$\begin{aligned} \text{BW} &= 2 \\ \text{CM Size} &= 4 \text{K} \times 8 = 2^{12} \times 8 \\ \text{CMW} &= 2^{\frac{12}{2}} = 2^6 \\ \text{CA} &= 12 \\ \text{el} &= \frac{\text{CMW}}{\text{BW}} = \frac{2^6}{2^9} = \frac{1}{2} = 8 \end{aligned}$$

(2)  $T \times CL = 8 \times 8 = 64 \text{ bits}$

$$\begin{aligned} PA &= 20 \\ \text{Tag Size} &= PA - CA \\ &= 8 \text{ bit} \end{aligned}$$

3) In a System, Main Memory has 64 blocks  
and Cache memory has 4 blocks. CPU  
block request order is MB<sub>3</sub>, MB<sub>12</sub>, MB<sub>31</sub>, MB<sub>20</sub>  
MB<sub>2</sub>, MB<sub>15</sub>, MB<sub>3</sub>, MB<sub>8</sub>, ~~MB<sub>28</sub>~~ and MB<sub>2</sub>



After completion of these requests, which  
main memory blocks are available in Cache memory?

$$K \bmod CL, \quad K \bmod 4$$
$$K \text{ range} = (0 \text{ to } 63)$$

CL=4      Order

MB  
 ③ 12 31, 20 2, 15,  
 ④ 8 28, 2

Finally MB<sub>2</sub>, MB<sub>3</sub>  
 and MB<sub>28</sub> are  
 available in  
 Cache

Kmod4

12 9 8 28	CL0
	CL1
2 hit	CL2
31 15, 3	CL3



→ when CPU requires a main memory  
 block number/word in 2nd time and that  
 word/block is not available in cache then  
 it is known as Conflict miss





### Block Set Associative mapping

Set = Group of blocks, let one set has ' $N$ ' blocks, it is known as ' $N$ ' way Set Associative mapping and in this ' $N$ ' way Set Associative mapping technique, any M.M. block is having ' $N$ ' no. of unique Cache block Address while Mapping, that reduces Conflict misses and improves hit rate.

Mapping Expression is  $K \bmod S$

$$S = \text{no. of Sets in Cache}, \quad S = \frac{CL}{N}$$

$N = \text{Associativity}$

Ex :- let  $CL = 64$ ,  $N = 4$   
 $(C_{lo} \text{ to } C_{l63})$

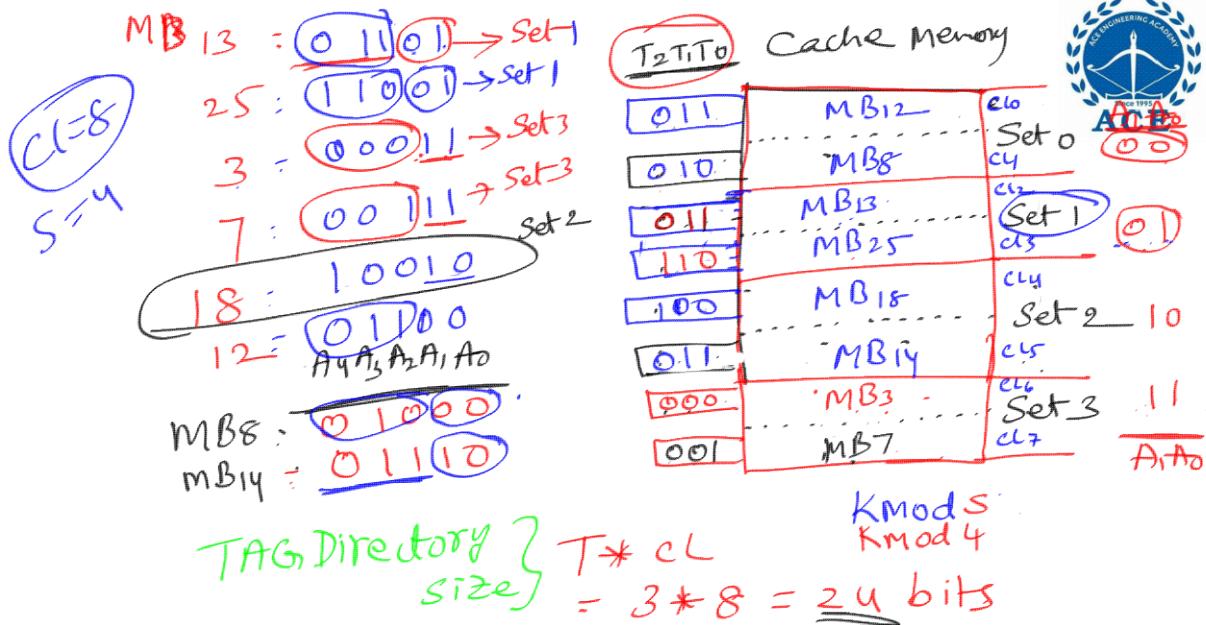
$$\left. \begin{array}{l} S = \frac{64}{4} = 16 \\ (S_0 \text{ to } S_{15}) \end{array} \right|$$

In 'N' way block set Associative mapped cache; each set has 'N' Cache lines i.e. any MM block can have N no of mapping Cache line Address Chances.

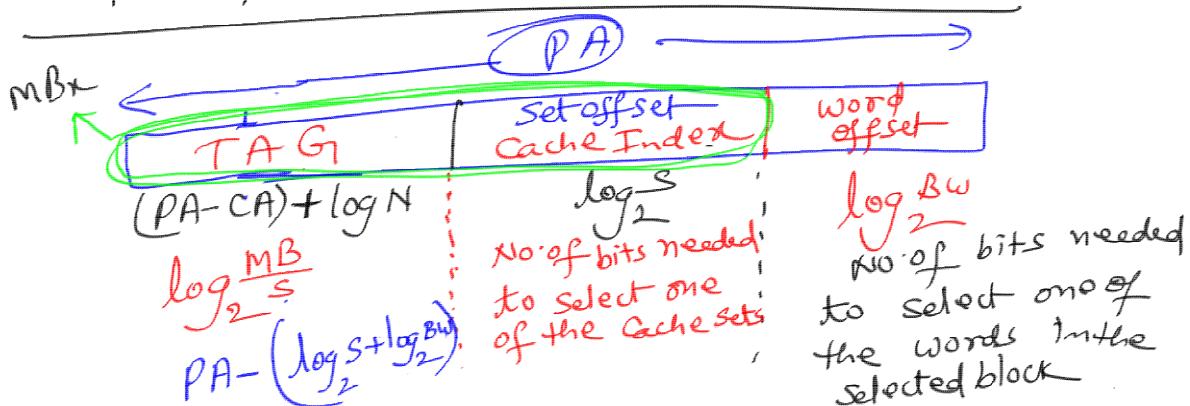


Tag Directory Size =  $T * CL$  only  
 because each Cache line requires one Separate Tag information.

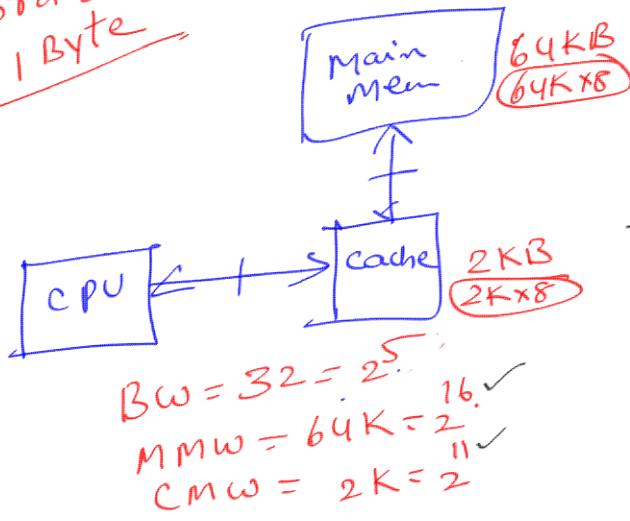
(Ex) Let  $MB = 32$ ,  $CL = 8$  ( $CL_0$  to  $CL_7$ )  
 $MB = 2^5$  ( $MB_0$  to  $MB_{31}$ )  
 and Associativity is 2 ( $N=2$ ).  
 The CPU request order is  $MB_{13}, MB_{25}, MB_3, MB_7, MB_{18}$  and  $MB_{12}$ . After completion of these requests, which blocks are available in Cache :  
 $N=2$ ,  $S = \frac{CL}{N} = \frac{8}{2} = 4$  ( $S_0$  to  $S_3$ )  
 Mapping expression is  $K \bmod S$   $K \bmod 4$ .



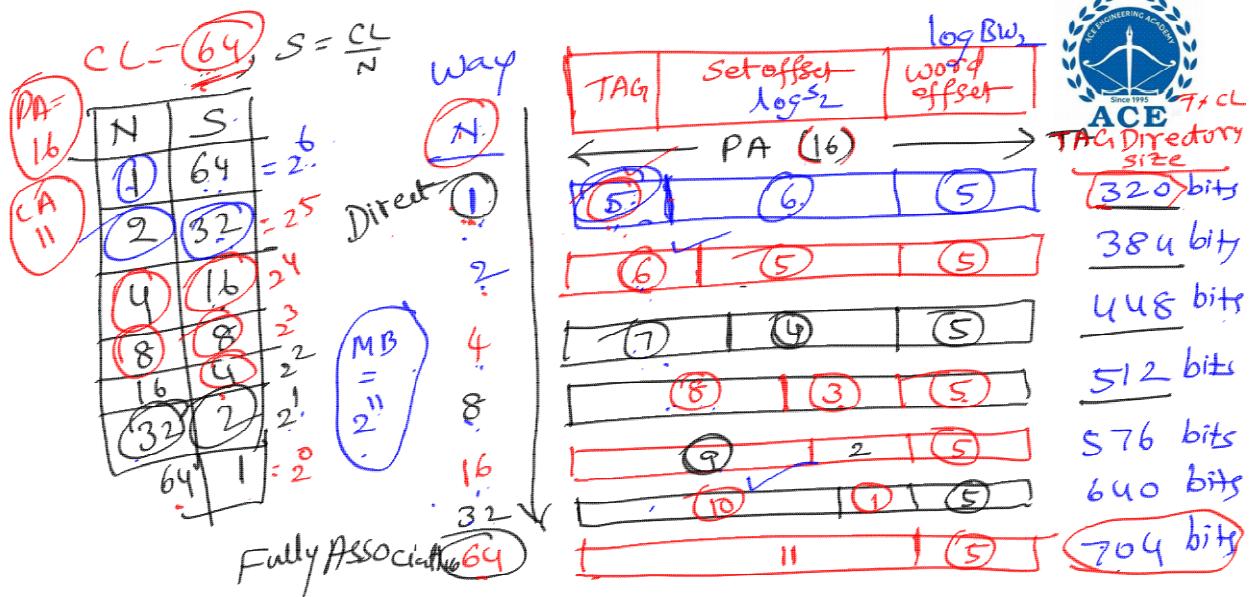
physical Address format for Block  
 N-way Set associative mapped Cache



Word size =  
1 byte



$PA = 16 \text{ bits}$   
 $CA = 11 \text{ bits}$   
 $MB = \frac{MMW}{BW} = \frac{2^{11}}{2^5} = 2^{11-5} = 2^6 = 64$   
 $MB_0 \text{ to } MB_{2047}$ ,  
 $CL = \frac{CMW}{BW} = \frac{2^6}{2^5} = 2^6 = 64$ , CL<sub>0</sub> to CL<sub>63</sub>



→ In  $N$  way block set Associative mapped cache; Tag field size

$$= (PA - CA) + \log_2 N$$

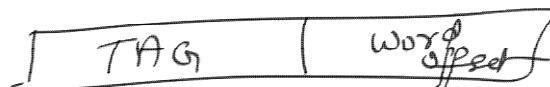
$$\log_2 \frac{MB}{S}$$



$N = 1$ , one set has only one cache line = Direct mapped Cache.



$N = CL = 64$ , it is known as Fully Associative mapped cache; it does not require Set offset field (Index field)





- Tag Directory size is directly proportional to 'N'
- Direct mapped cache requires smallest Tag directory
- Fully Associative mapped cache requires largest Tag directory.

while finding Tag field size with  $(PA - CA) + \log_2 N$  expression in 'N-way block set Associative mapped Cache ; it is ensure that the Main memory capacity and Cache memory capacity are mentioned in same units i.e. both memories should be expressed in either bytes or words.

2022  
GATE

Q) Consider a system with 2 KB Direct mapped Cache with block size of 64 Bytes.



During the execution of a program, four data words

(MSQ)

P, Q, R and S are accessed in order 10 times  
ie. (PQRS PQRS PQRS....) Hence there are 40  
accesses to data cache in total. Assume that  
data cache is initially empty. The address of the  
words are P = (A248)<sub>16</sub>, Q = (C28A)<sub>16</sub>, R = (CA8A)<sub>16</sub>  
and S = (A262)<sub>16</sub>. For execution of the program  
which of the following statement(s) is/are True  
with reference to the Data Cache.

TRUE

a) Every access to 'S' is a Hit

TRUE b) Once 'P' is brought in to Cache,  
it is never evicted.

False c) At the end of the execution, only R and S  
reside in the Cache.

TRUE d) Every access to R evicts Q from the  
Cache

a, b and c are correct



$$CMW = 2K = 2^11, CA = 11, BW = 2^6$$

$PA = 16 \text{ bit}$ , Direct mapped, Tag size = 5 bits.

$$P = (A248)_{16}$$

$$Q = (C28A)_{16}$$

$$R = (CA8A)_{16}$$

$$S = (A262)_{16}$$

$$CL = \frac{2^{11}}{2^6} = 2^5 = 32$$

CL 0 to CL 31

$$P = \begin{array}{c|ccccc|c} & & & & & & \\ & 1 & 0 & 1 & 0 & 0 & 1 & 0 & 0 & 1 & 0 & 0 & 0 \\ \hline MB & & & & & & CL_9 & & & & & & word \\ & 1 & 0 & 1 & 0 & 0 & 0 & 1 & 0 & 0 & 1 & & \\ & 8 & & & & & & 8 & & & & & \\ & 128 & & & & & & 128 & & & & & \\ & 512 & & & & & & 512 & & & & & \end{array} = MB_{649}$$



$$Q = C28A$$

$$\begin{array}{c|ccccc|c} & & & & & & \\ & 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 0 & 1 & 0 & 0 \\ \hline MB & & & & & & CL_{10} & & & & & & \\ & 1 & 1 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & 0 & 0 & 0 \\ \hline & 512 & & 256 & & & 512 & & 256 & & & & \\ & 128 & & 128 & & & 128 & & 128 & & & & \\ & 256 & & 256 & & & 256 & & 256 & & & & \end{array}$$

$$MB \rightarrow CL_{10}$$

$$R = CA8A$$

$$\begin{array}{c|ccccc|c} & & & & & & \\ & 1 & 1 & 0 & 0 & 1 & 0 & 1 & 0 & 0 & 1 & 0 & 0 \\ \hline MB & & & & & & CL_{10} & & & & & & \\ & 1 & 1 & 0 & 0 & 1 & 0 & 0 & 1 & 0 & 0 & 1 & 0 \\ \hline & 512 & & 256 & & & 512 & & 256 & & & & \\ & 128 & & 128 & & & 128 & & 128 & & & & \\ & 256 & & 256 & & & 256 & & 256 & & & & \end{array}$$

$$MB_{810}$$

$$S = A262$$

$$\begin{array}{c|ccccc|c} & & & & & & \\ & 1 & 0 & 1 & 0 & 0 & 1 & 0 & 0 & 0 & 1 & 0 & 0 \\ \hline MB & & & & & & CL_9 & & & & & & \\ & 1 & 0 & 1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 1 & 0 \\ \hline & 512 & & 256 & & & 512 & & 256 & & & & \\ & 128 & & 128 & & & 128 & & 128 & & & & \\ & 256 & & 256 & & & 256 & & 256 & & & & \end{array}$$

$$MB = 649$$



P: MB649; CL9

Q: MB778, CL10.

R: MB810; CL10

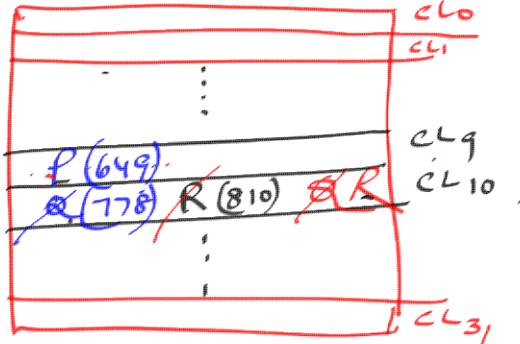
S: MB649, CL9

$$B = 2^6 = 64$$

S = Hit

Same block.

If CPU brings MB649 for P automatically 'S' is available



2nd Time

P = Hit

R is Replaced with Q

Q is Replaced with R

S = Hit

Repeated

10 times.

At End of execution, P, R and 'S' are available in cache

