

Welcome to ACE Engineering Academy - online live class

Subject: **Computer Organization and Architecture**

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Subject

Computer organization & Architecture

Chapters (Topics)

I. Computer Arithmetic ✓

II. Memory Organization

III. Secondary Memories

IV. Basic processor organization and Design

V. Pipeline organization

VI. Control unit Design

VII. IO Organization

Chapter 2 Memory Organization

- Introduction ✓
- Memory Basics ✓
- Memory Classification
- Memory Size Expansion ✓
- Primary Memory
- Secondary Memory
- ROM and its design
- RAM and its design
- Memory Hierarchy
- Cache Memory
- Mapping Techniques
- Different misses occurred in cache
- Different block replacement techniques
- Tag directory design
- Associative Memory

Q. It is desired to have a 64×8 memory. The memory IC's available is of 16×4 size. The number of ICs required

- (a) 8
- (b) 4
- (c) 6
- (d) 2

$$\frac{64 \times 8}{16 \times 4} = 8$$

These 8 chips are connected in
Four Rows with 2 columns.

Q) No. of 32Kx1 bit chips needed
to implement 256K Bytes memory
is 64



$$\begin{array}{r} 8 \quad 8 \\ \hline \cancel{256K \times 8 \text{ bits}} \\ \hline \cancel{32K \times 1 \text{ bit}} \\ \hline \text{64.} \end{array}$$

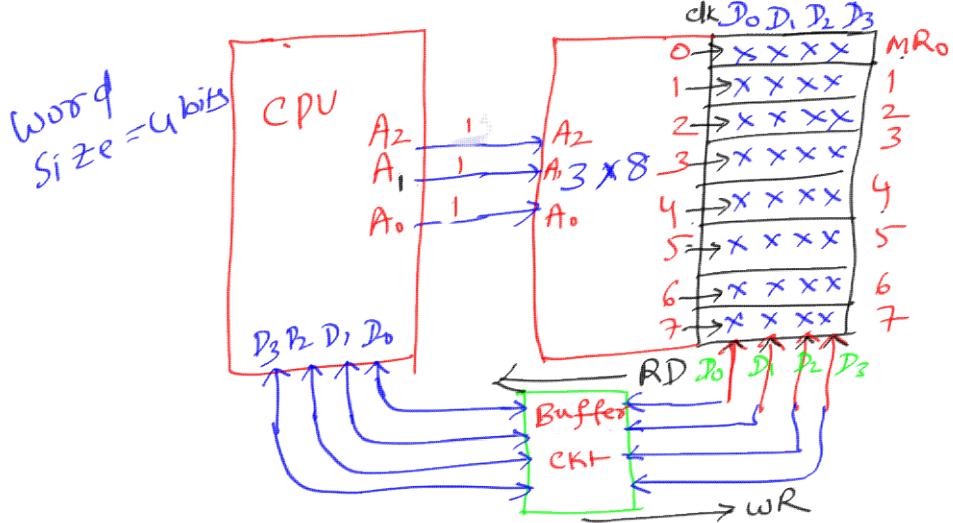
Addressing of 8x8 memory chip



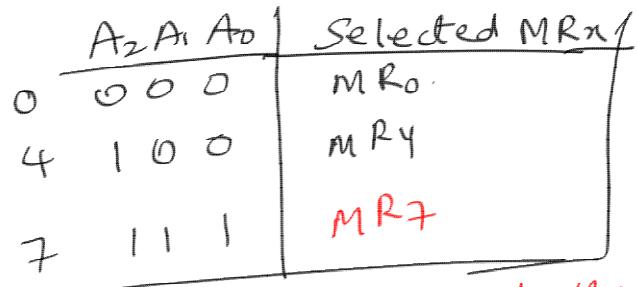
No. of Regs = $8 = 2^3$, 3 Address bits
($A_2 A_1 A_0$)

No. of bits in each Register = $4 = \frac{\text{Word size}}{4}$

Hence, to address this chip, CPU
requires 3 Address lines ($A_2 A_1 A_0$) and
4 data lines ($D_3 D_2 D_1 D_0$)



Buffer
CKT
is
used
to
define
READ
WRITE
operations



→ Address Bus of the CPU is directly connected to the input of the Decoder.

→ Data Bus is used to perform RD/WR operation with the Selected Mem. Reg.



Q) Size of the Decoder required
to fabricate in $512K \times 16$ bit

memory chip is

$$\begin{array}{c|c} & 512K \times 16 \text{ bit} \\ \hline a & 16 \times 2^{16} \\ b & 18 \times 2^{18} \\ \cancel{c} & 19 \times 2^{19} \\ d & 17 \times 2^{17} \end{array}$$

$\cancel{(2)} \times 2^{16} \text{ bit}$

$$19 \times 2^{19}$$

Memory size Expansion.



- (i) How to increase the no. of words.
- (ii) How to increase the word size



Process of Increasing the No. of words in memory space

- Find the no. of words in Target Memory and Basic chip
- Find the no. of Address bits required for Target Memory and Basic Memory chip
- Compute the free Address lines.
- Connect the Free Address lines for the input of External Decoder known as chip select Decoder

(Ex) Implement 4K x 8 bit memory with 1K x 8 bit chips



Solution:-

$$\text{Target size} = \frac{4K \times 8 \text{ bit}}{1K \times 8 \text{ bit}} = \frac{12}{2} \times 8$$

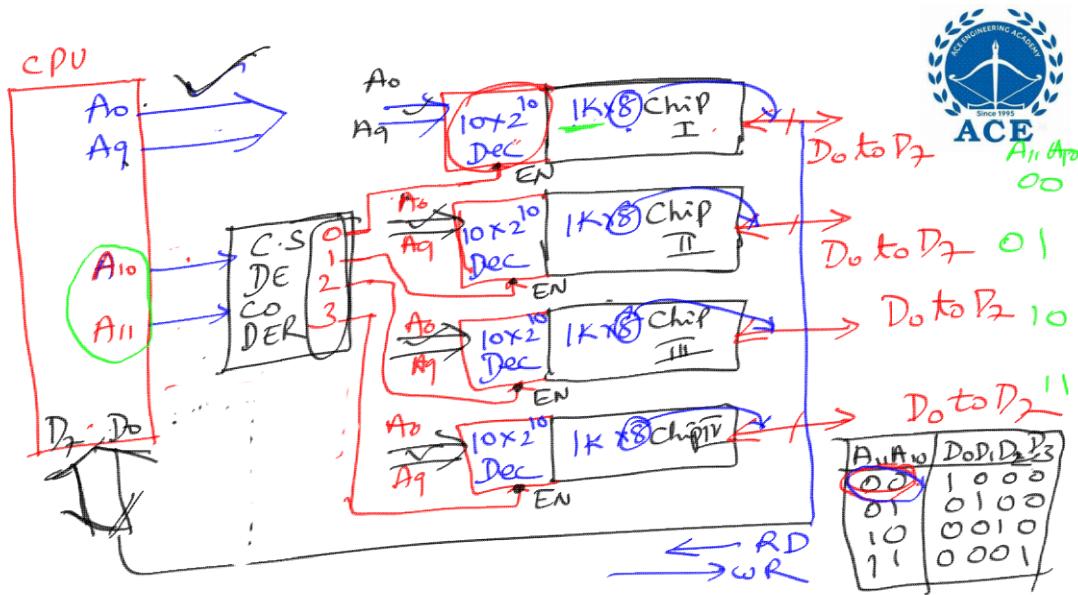
$$\text{Basic size} = \frac{12}{2} \times 8$$

$$\text{free address lines} = 12 - 10 = 2 \text{ bits.}$$

$$\text{No. of Basic chips needed} = \frac{\text{Target size}}{\text{Basic size}}$$

$$= \frac{4 \cancel{4K \times 8}}{\cancel{1K \times 8}} = 4 \times 1 = 4 \text{ chips}$$

These 4 chips are arranged in Four Rows with Single Columns.



- C.S. Decoder is used to select one of the four chips.
- In the selected chip, the internally fabricated Memory Address Decoder is used to select one of the available memory registers.



Address Range of the each chip

Since CPU is having 12 Address lines

Starting word Address: 000000000000_2

Ending word Address: 111111111111_2

$(000H \text{ to } FFFH}$ } 4 chips

Address Range
chip I chip II chip III chip IV

	$A_{11} A_{10}$	$A_9 A_8$	$A_7 A_6 A_5 A_4$	$A_3 A_2 A_1 A_0$	Range
Chip I	0 0	0 0	0 0 0 0	0 0 0 0	$000H$ to $3FFH$
Chip II	0 0	1 1	1 1 1 1	1 1 1 1	$400H$ to $7FFH$
Chip III	0 1	0 0	0 0 0 0	0 0 0 0	$800H$ to $BFFH$
Chip IV	1 0	0 0	0 0 0 0	0 0 0 0	$C00H$ to $FFFH$



(Ex) For implementing $256K \times 16$ bit memory with $16K \times 16$ bit chips.

18) Total no of chips required is $\frac{16}{16}$

29) Internal Memory Address Decoder size is 16×2^4

38) No. of free Address lines is 4

48) Size of C.S. Decoder is 4×2^4 4×16

$$\begin{aligned}
 & \text{(A}_0 \text{ to A}_7\text{)} \text{ Target Size} = \underline{\underline{256K \times 16 \text{ bits}}} \\
 & \text{(A}_8 \text{ to A}_{11}\text{)} \text{ Basic Size} = \underline{\underline{16K \times 16 \text{ bits}}} \\
 & \text{No. of chips required} = \frac{\text{Target Size}}{\text{Basic Size}} = \frac{256K \times 16}{16K \times 16} = \frac{16 \times 16}{16 \times 16} = 16 \quad \text{R.C} \\
 & 16K \times 16 = \underline{\underline{\frac{14}{2} \times 16}} \\
 & 256K \times 16 \text{ bit} \\
 & = \underline{\underline{\frac{18}{2} \times 16 \text{ bit}}} \quad 14 \times 2^4
 \end{aligned}$$



process of Increasing the word size
in the given memory space

→ In this C-S Decoder is not needed because all the chips are needed to enable always for providing the Target word size

(Ex)

Implement $1K \times 8$ bit memory
with $1K \times 4$ bit chips

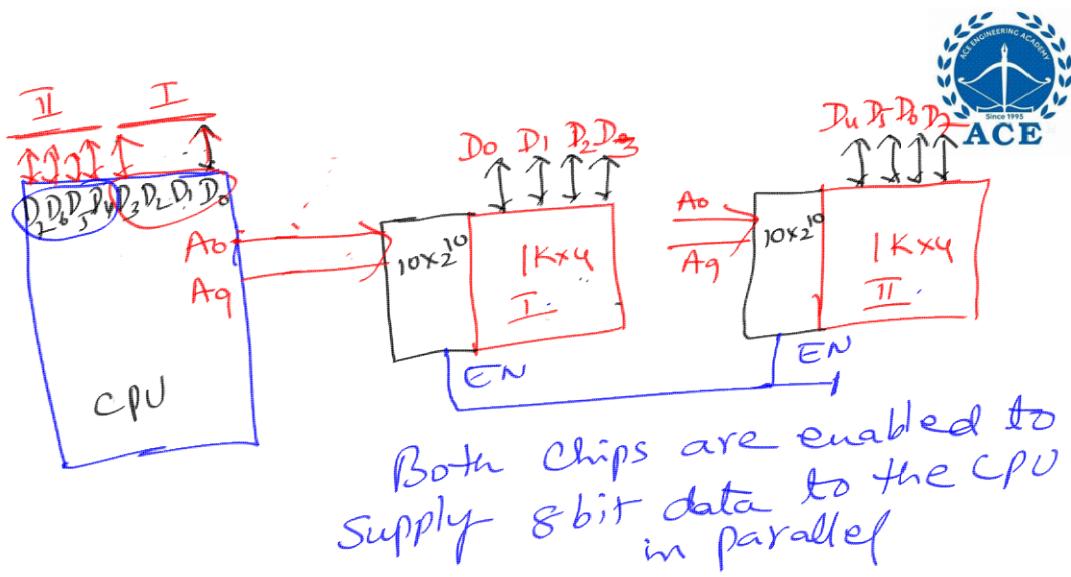
$$\text{Target size} = 1K \times 8 = 2^{10} \times 8 \text{ bit}$$

$$\text{Basic size} = 1K \times 4 = 2^{10} \times 4 \text{ bits}$$

No Free Address lines: No CS Decoder

$$\text{No of chips required} = \frac{1K \times 8}{1K \times 4} = 1 \times 2 = 2 \text{ RxC chips}$$

Arrange these 2 chips in single Row
with 2 columns.



- 1 (Q) No. of $2K \times 8$ bit chips needed to implement $2K \times 24$ bit Memory
 is (3) $\frac{2K \times 24}{2K \times 8} = 3$ (3)
- 2 (Q) Size of C.S. Decoder needed for the above is not needed



Memory classification

- In Digital Computer; different memories are used for different functions
- Smallest Cache Memory is used for storing the current executing program and largest secondary Memory is used for storing the Back-up files.

Byte Addressable memory:-

One memory Register is used to store only one byte -



Word Addressable memory:- One

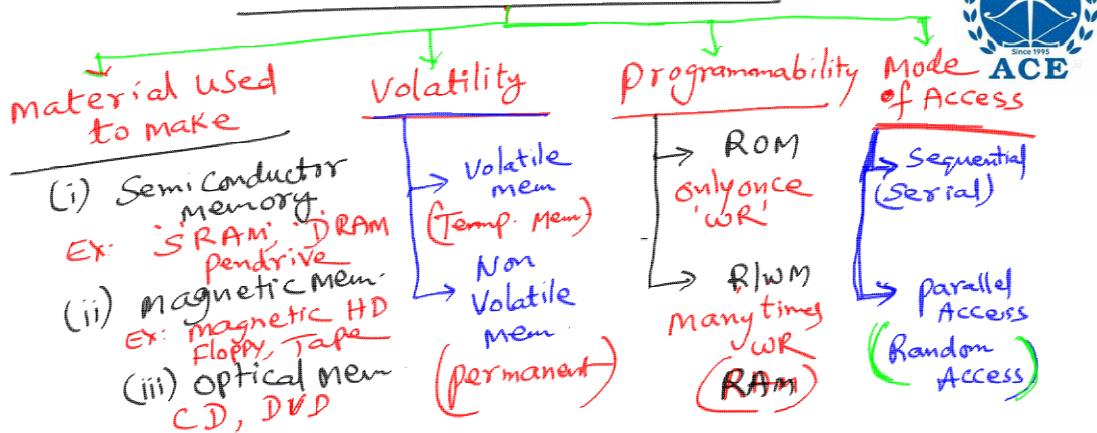
memory Register is used to store one word.



System Configuration

I5 processor	: Name of the CPU
3 GHz	= fck
100 MB	= Cache Memory RAM
8 GB	= Main Memory RAM
1 TB	= Hard disk
DVD writer	= optical Memory

Memory classification

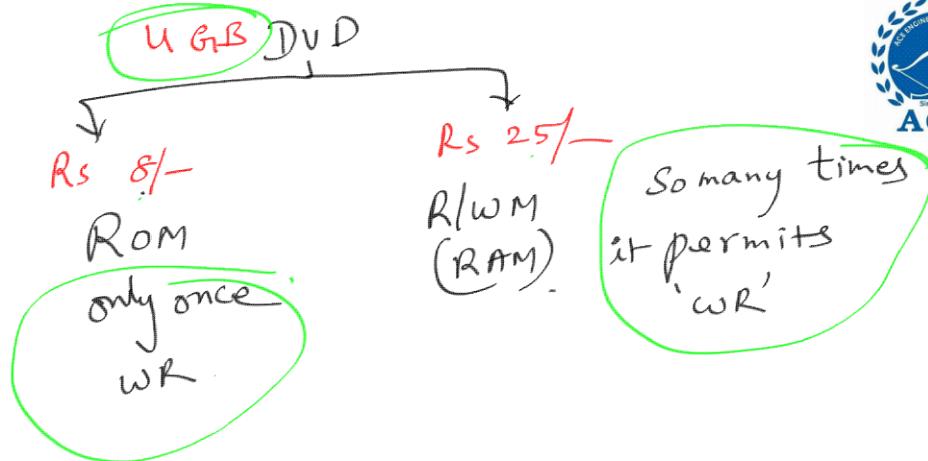




- In Serial Access Memory, the access time is different from word to word.
- In Random Access Memory, the access time is same for all words

→ All ROMs are belonging to Non-Volatile category

<u>Electronic Rom</u>	<u>Magnetic Rom</u>	<u>optical Rom</u>
ROM PROM	Nowadays No. Such type of design	CD } R DVD } O M.



→ All magnetic and optical RAMs are designed with Non Volatile technology



Floppy = RAM ?
magnetic HD = RAM
25Rs CD, DVD = RAM
Tape : RAM } R/W Mem (RAM)

→ All Electronic RAMS are Volatile
Memories.
Ex:- static RAM (Cache mem)
Dynamic RAM (main mem)



100%
Correct

Pendrive: Electronic
RAM ✗
Non Volatile



Pendrive designed with ROM
technology

Electronic ROMs are designed with 2 techniques.



Permanent Rom

ROM } once
PROM } programming
programmable Rom

Semi permanent Rom.

Can be programmed
for Limited
no. of times
(i) EEPROM
(ii) EEPROM
(iii) Flash memory

→ Process of writing information in ROM is known as programming



→ ROM is programmed by the designer only

→ PROM is programmed by designer or user



SNo.	Parameter	EPROM	EEPROM	Flash Memory
1	No. of times can be reprogrammed	1 K times	<u>10 K times</u>	<u>1 Lac times</u>
2	UV Signals for erasing	Required	No	No
3	Application	familiar till 2000 year	Familiar (mem. card)	Familiar (pendrive)

→ EEPROM permits only Bytelevel erasing
but Flash mem. permits Both Bytelevel and Chiplevel erasing



EPROM: Erasable and Programmable ROM

EEPROM: Electrically erasable and programmable ROM