

Welcome to ACE Engineering Academy - online live class

Subject: **Computer Organization and Architecture**

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### **Subject**

Computer organization & Architecture

### **Chapters (Topics)**

- I. Computer Arithmetic ✓
- II. Memory Organization
- III. Secondary Memories
- IV. Basic processor organization and Design
- V. Pipeline organization
- VI. Control unit Design
- VII. IO Organization

## Chapter 2 Memory Organization

- Introduction ✓
- Memory Basics ✓
- Memory Classification ✓
- Memory Size Expansion ✓
- Primary Memory
- Secondary Memory ✓
- ROM and its design ✓
- **RAM and its design** ✓
- Memory Hierarchy ✓
- Cache Memory
- Mapping Techniques
- Different misses occurred in cache
- Different block replacement techniques
- Tag directory design
- Associative Memory

Q. Consider a machine with a byte addressable main memory of  $2^{20}$

bytes, block size of 16 bytes and a direct mapped cache having

$2^{12}$  cache lines. Let the addresses of two consecutive bytes in main memory be  $(E201F)_{16}$  and  $(E2020)_{16}$ . What are the tag and cache line address (in hex) for main memory address  $(E201F)_{16}$ ?

- (a) E, 201

(b) F, 201

- (c) E, E20

(d) 2, 01F

$$\begin{aligned} MMW &= 2^{20} \\ PA &= 20 \\ BW &= 2^4 \\ CL &= 2^{12} \end{aligned}$$

$$E201F = \begin{array}{c} 1110 \\ TA_6 \\ (E) \end{array} \left| \begin{array}{c} \text{Cache line offset} \\ \hline 0010 & 0000 & 0001 \\ (2 & 0 & 1) \end{array} \right| \begin{array}{c} 111 \\ word \\ offset \end{array}$$

- Q. A 64 word cache and 256 word main memories are partitioned into 16 word blocks. The tag information is shown below:  
 (Current values in cache) Direct map

| Block             | Tag |
|-------------------|-----|
| CL <sub>0</sub> 0 | 10  |
| CL <sub>1</sub> 1 | 10  |
| CL <sub>2</sub> 2 | 00  |
| CL <sub>3</sub> 3 | 01  |

$MB = 2^4 = 16$   
 $MmW = 2^6$   
 $CMW = 2^6$   
 $Bw = 2^4$   
 $(CL_0 \text{ to } CL_3)$

| TAG | CL <sub>0</sub> |
|-----|-----------------|
| 10  | CL <sub>0</sub> |
| 10  | CL <sub>1</sub> |
| 00  | CL <sub>2</sub> |
| 01  | CL <sub>3</sub> |

Identify the correct statements with respect to the availability of main memory words in the cache (MMW)

- (a) The words 50 and 132 are available in the cache False  
 (b) The words 150 and 132 are available in the cache True  
 (c) The words 178 and 150 are available in the cache False  $PA = 8 \} TAG$   
 (d) The words 35 and 50 are available in the cache False  $CA = 6 \} (2)$



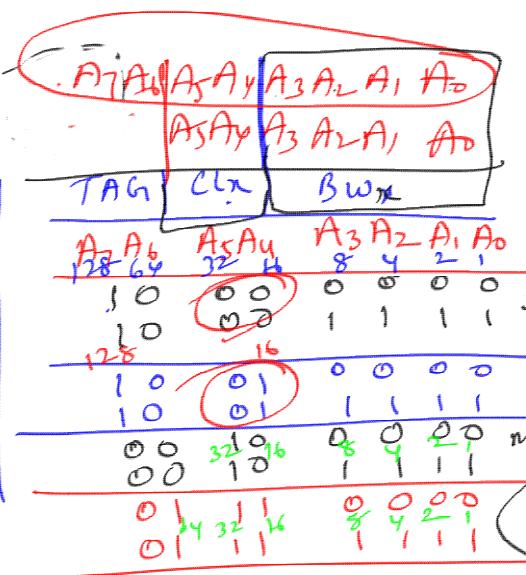
$$PA = 8 \text{ bit} =$$

$$CA = 6 \text{ bit}$$

$$CL = 4$$

|    |                 |    |
|----|-----------------|----|
| 10 | CL <sub>0</sub> | 00 |
| 10 | CL <sub>1</sub> | 01 |
| 00 | CL <sub>2</sub> | 10 |
| 01 | CL <sub>3</sub> | 11 |

$$BW = 2^4$$



MMW<sub>128</sub> to MMW<sub>143</sub>

MMW<sub>144</sub> to MMW<sub>159</sub>

MMW<sub>32</sub> to MMW<sub>47</sub>

MMW<sub>112</sub> to MMW<sub>127</sub>



MMW = No. of words in main memory

BW = No. of words in a block

CMW = No. of words in Cache Memory

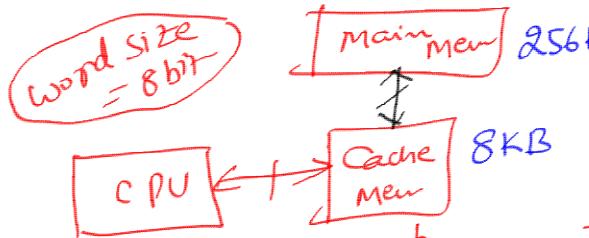
MB = No. of blocks in Main Memory

CL = CB = No. of blocks in cache Memory

M.M. Capacity = MMW \* wordsize

C.M. Capacity = CMW \* word size

VVVIMP Generally size of Main Memory block and size of Cache mem. block are same.



Word size = 8 bit

$$B.W = 64 = 2^6$$

$$TAG = (PA - CA)$$

bits

$$CL = \frac{CMW}{BW} = \frac{2^{13}}{2^6} = 2^7 = 128$$

CL<sub>0</sub> to CL 127

$$\begin{aligned} MM\text{Capacity} &= 256KB \\ &= 2^{18} * 8 \text{ bits} \end{aligned}$$

$$MMW = 2^{18}; PA = MA \\ = 18 \checkmark$$

$$CM\text{Capacity} = 8KB = 2^{13} * 8$$

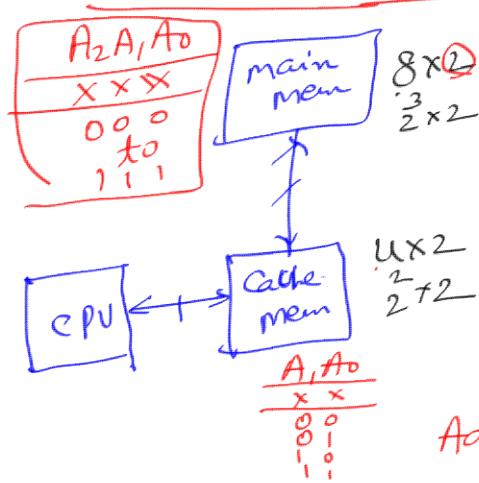
$$CMW = 2^{13}; CA = 13 \checkmark \quad \text{bits}$$

$$MB = \frac{MMW}{BW} = \frac{2^{18}}{2^6} = 2^{12} = 4096$$

MB<sub>0</sub> to MB 4095

$$MMW = MB * BW$$

## Mapping Basic Explanation

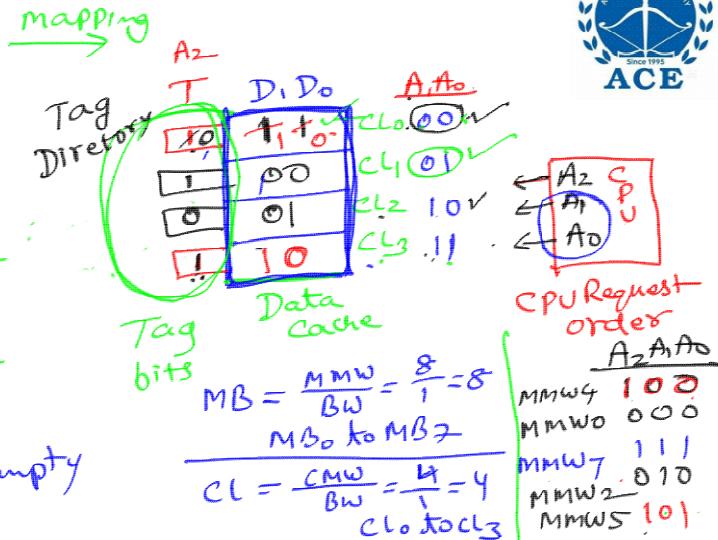


$$\begin{aligned} MMW &= 8 = 2^3 \\ PA &= 3 \text{ bit: } A_2A_1A_0 \\ CMW &= 2^2, CA = 2 \text{ bit } A_1A_0 \\ \text{- Tag Size} &= PA - CA = 1 \end{aligned}$$

since PA Address Size is larger than CA Address Size; the difference Address bits are saved along with Cache known as Tag bits



let cache is empty initially





- With the help of memory word Address Decoder, the Target word will be selected
- It is the Designer responsibility to design Extra Memory known as Tag memory, this Tag memory is used to store the difference Address bits (PA - CA) along with each cache block
  - one separate Tag is required for each cache line

Total Tag Directory size =

$$T * CL = 1 * 4 = 4 \text{ bits}$$

$T = \text{no. of Tag bits per each Cache line}$

$CL = \text{no. of Cache line} =$

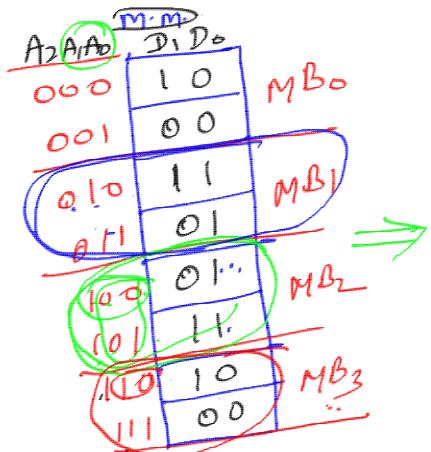
- Associative Memory is used to store Tag bits, and this memory is connected to Cache memory

let Block size = 2 words  
 $MmW = 8$ ,  $CmW = 4$   
 $BW = 2$   
 $MB = 4$  ( $MB_0$  to  $MB_3$ )  
 $CL = 2$  ( $CL_0$  to  $CL_1$ )

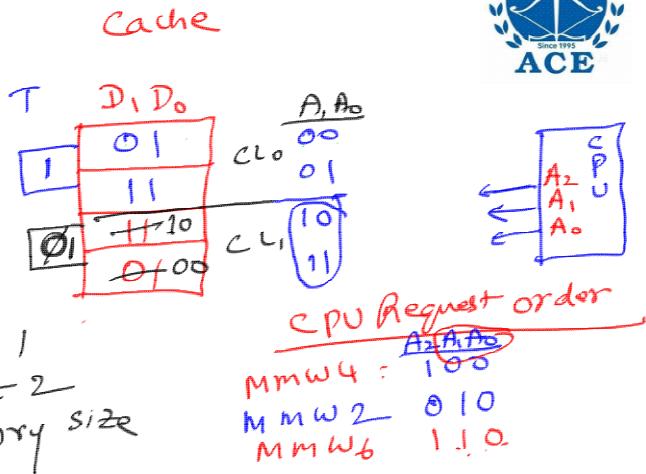


Ex 2  
 $MB = 4$        $MB_0$  to  $MB_3$   
 $CL = 2$        $CL_0$  to  $CL_1$

(Ex 2)



$T = 1$   
 $CL = 2$   
Tag Directory size  
 $= T \times CL = 1 \times 2 = 2 \text{ bits}$



EX3

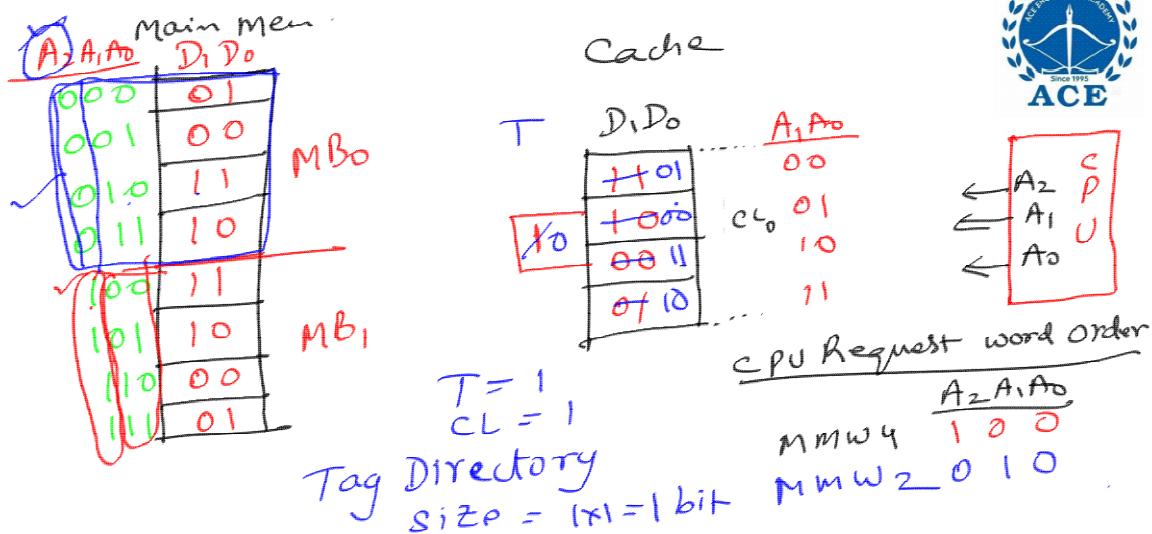
one Block size = 4 words



$$mmw = 8^\circ, MB = \frac{8}{a} = ? \quad MB_0 \text{ to } MB_1$$

$$C_{M\omega} = 4 \quad CL = \frac{4}{\alpha} = 1 \quad \Rightarrow \quad CL_0$$

$$\text{PA Size} = \boxed{A_2, A_1, A_0} \quad CA = A_1, A_0$$





UVVI MP  
while increasing the block size; the size of the Tag directory will be Reduced  
Hence design cost will be Reduced

but it degrades the system performance  
To improve the system performance by controlling the price of Tag directory design;  
Moderate Block size is selected  
(16 words to 1 Kiloword)



### Direct map technique:

- It is easy to implement and design cost is cheapest because only one Tag Comparator is sufficient to declare hit/miss during word reading
- one separate Tag field is required for each cache line
- Tag field size =  $PA - CA = T$
- Tag Directory size =  $T * CL$



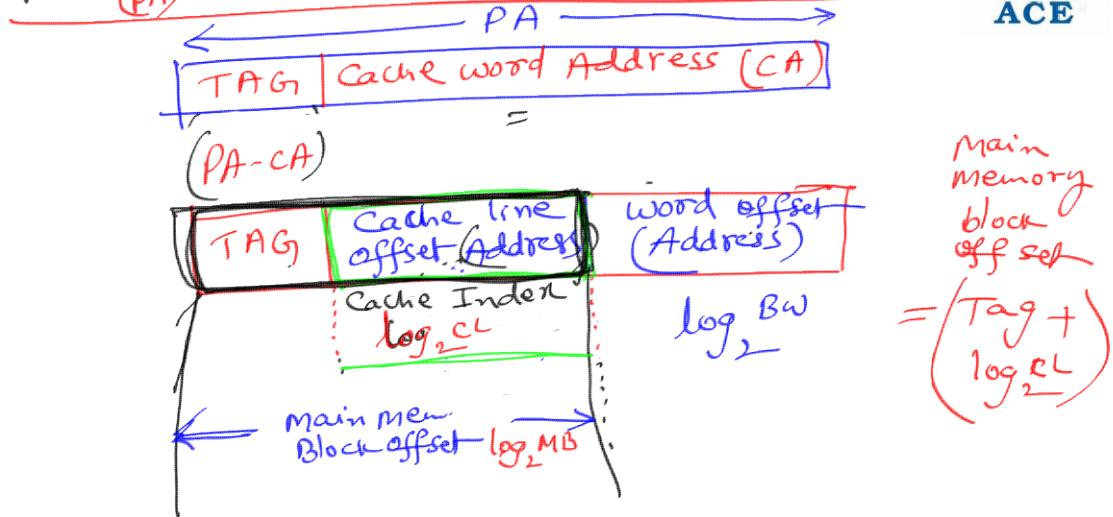
$$\text{Tag field size} = (PA - CA)$$

$$= \log_2 \frac{MB}{CL}$$
$$= PA - (\log_2^{CL} + \log_2^{BW})$$
$$\log_2(32) = 5$$
$$\log_2(5) = 2.3$$

→ In Direct mapped Cache, any Main memory block is having only one unique cache line address while mapping. If that block is already filled, the new block evicts old block. Even though some Vacancy blocks are available in Cache, which leads to occur conflict miss.



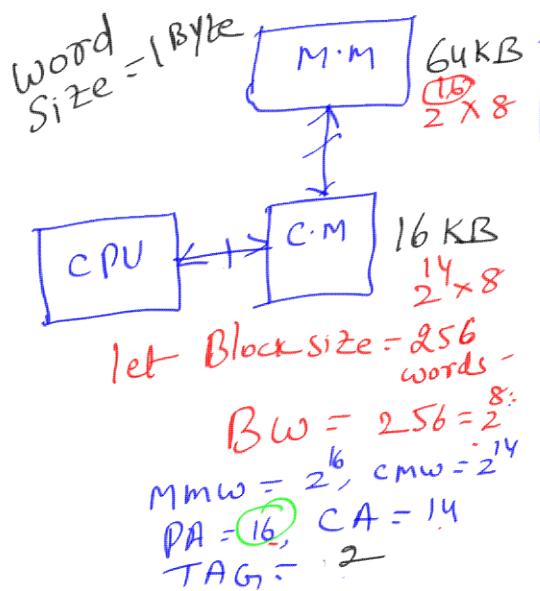
Physical Address format in Direct map:



Cache line Address = No. of bits needed to Select one of the lines in Cache.

Word Address: No. of bits needed to Select one of the words in the Selected block.





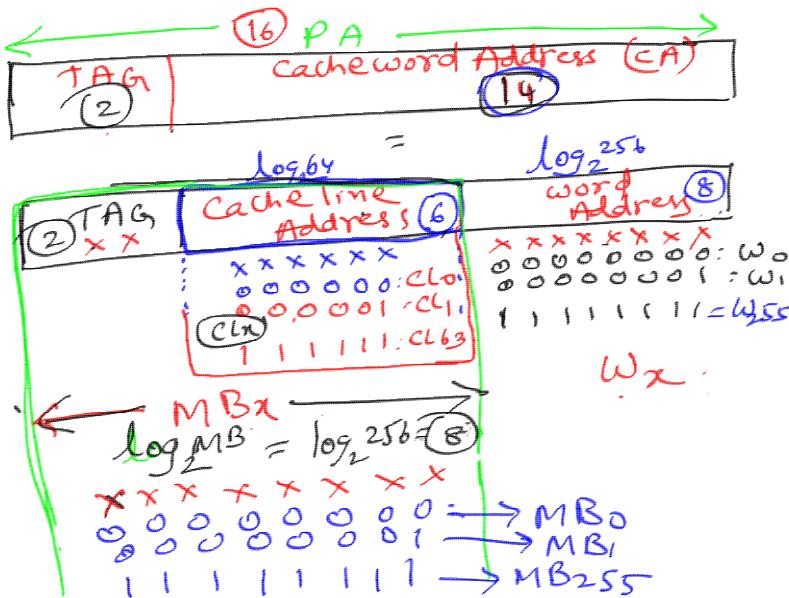
$$MB = \frac{2^{16}}{2^8} = 2^8 = 256$$

MB<sub>0</sub> to MB<sub>255</sub>

$$CL = \frac{2^{14}}{2^8} = 2^6 = 64$$

CL<sub>0</sub> to CL<sub>63</sub>

$$\frac{000000}{6} \text{ to } \frac{111111}{6}$$



TAG field size =  $(PA - CA)/2 = 2$

$$\log_2 \frac{MB}{CL} =$$

$$\log_2 \frac{2^8}{2^6} = \log_2 2^2 = 2$$

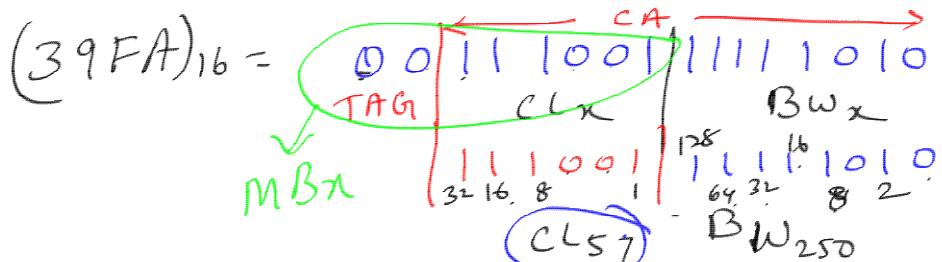
PA - (log<sub>2</sub> CL + log<sub>2</sub> BW)

16 - (6 + 8) = 2



**Ex** Let  $(39FA)_{16}$  is the main word address,

- 18) Its Tag information is 00
- 28) Main memory block number is  $MB_x = MB_{57}$ .
- 38) Cache memory block number  $CL_x = CL_{57}$
- 48) word Address in the selected block ( $Bw_x$ ) is  $BW_{250}$ .



$\begin{matrix} 1 & 2 & 8 & 6 & 4 & 3 & 2 & 1 \\ | & | & | & | & | & | & | & | \\ 0 & 0 & 1 & 1 & 1 & 0 & 0 & 1 \end{matrix}$   
 $MB_{57}$ .



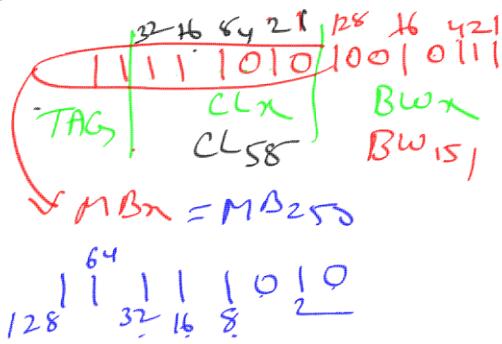
(Ex) Let physical address for the given word is  $(FA97)_{16}$ .

1) Tag information is  $(11)_2$

2) CL<sub>x</sub> is  $\overbrace{CL58}^{MB250}$

3) MB<sub>x</sub> is  $\overbrace{MB250}^{CLx}$

4) BW<sub>x</sub> is  $\overbrace{BW15}^{CL58}$



mapping expression is  $K \bmod CL$

$CL = \text{no. of cache line}$

$K = \text{main memory block number}$  to be mapped.



(Ex)  $37 \bmod 8$ , Answer is 5

$$\begin{array}{r} 37 \\ 8 ) 37 ( 4 \\ \underline{- 32} \\ \quad \quad \quad 5 \end{array}$$



(Ex)

$$MB = 16$$

$$CL = 4$$

K Mod 4

$MB_0$  to  $MB_{15}$

$$K = (0 \text{ to } 15)$$

$TAG$   
size } = 2 bits

| $A_3 A_2 A_1 A_0$ Main | $MB_0$ |
|------------------------|--------|
| 0000                   | 1      |
| 0001                   | 2      |
| 0010                   | 3      |
| 0011                   | 4      |
| 0100                   | 5      |
| 0101                   | 6      |
| 0110                   | 7      |
| 0111                   | 8      |
| 1000                   | 9      |
| 1001                   | 10     |
| 1010                   | 11     |
| 1011                   | 12     |
| 1100                   | 13     |
| 1101                   | 14     |
| 1110                   | 15     |
| 1111                   |        |

TAG

| $A_3 A_0$ | $MB_0$ | $MB_8$ | $MB_{12}$ | $CL_0$ |
|-----------|--------|--------|-----------|--------|
| 00        |        |        |           | 00     |
| 01        |        |        |           | 01     |
| 10        | $MB_6$ |        |           | 10     |
| 11        | $MB_7$ |        |           | 11     |

order

- ①  $MB_0$
- ②  $MB_7$
- ③  $MB_8$
- ④  $MB_{12}$
- ⑤  $MB_6$

CPU Request

| $A_3 A_2 A_1 A_0$ | $MB_0$ |
|-------------------|--------|
| 0000              | 1      |
| 0001              | 2      |
| 0010              | 3      |
| 0011              | 4      |
| 0100              | 5      |
| 0101              | 6      |
| 0110              | 7      |
| 0111              | 8      |
| 1000              | 9      |
| 1001              | 10     |
| 1010              | 11     |
| 1011              | 12     |
| 1100              | 13     |
| 1101              | 14     |
| 1110              | 15     |
| 1111              |        |

$MB = 16$

$MB_0$  to  $MB_{15}$

$K = 0 \text{ to } 15$

Cache

|  |        |
|--|--------|
| $MB_0$ OR $MB_4$ OR $MB_8$ OR $MB_{12}$    | $CL_0$ |
| $MB_1$ OR $MB_5$ OR $MB_9$ OR $MB_{13}$    | $CL_1$ |
| $MB_2$ OR $MB_6$ OR $MB_{10}$ OR $MB_{14}$ | $CL_2$ |
| $MB_3$ OR $MB_7$ OR $MB_{11}$ OR $MB_{15}$ | $CL_3$ |

## ISRO/GATE (IT)

(MMW<sub>0</sub> to MMW<sub>4095</sub>)



Q) A main mem. has 4096 words and  
Direct mapped Cache is having 64 blocks with 16 words  
in each block. The 1206 main memory  
word Address (MMW<sub>1206</sub>) will map to  
cacheline (CLn)

$$Bw = 2^4$$

PA = 12 bit

$$\text{MMW} = 4096 = 2^{12}, \text{ PA} = 12 \text{ bit}$$

$$CL = 64 = 2^6, Bw = 16 = 2^4$$

$$CMW = 2, CA = 10$$

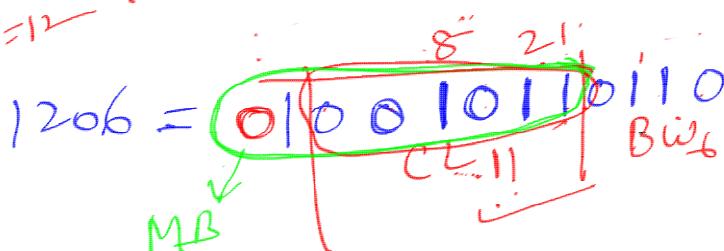
$$\text{Tag} = 2 \text{ bits}$$

$$\text{MMW}_{1206}$$

$1206 \neq \text{block number}$



$$PA = 12$$



K mod CL

K mod 64

K = Main  
Mem.  
Block  
number

$$0 | 001011 = MB_{75}$$

$$75 \text{ mod } 64$$

11



MmW 1206, Block size = 16 words

MmW<sub>0</sub> to } MB<sub>0</sub>      1206 belongs to  
MmW<sub>15</sub>                    MB<sub>n</sub>

$$\begin{array}{r} 16) 1206 \textcircled{15} \\ \underline{112} \\ 86 \\ \underline{80} \\ \textcircled{6} \end{array}$$

MB<sub>75</sub>

$$75 \bmod 64 \\ = \textcircled{11}$$