

Welcome to ACE Engineering Academy - online live class

Subject: **Computer Organization and Architecture**

Faculty: **Y.V. Ramaiah**

**Subject**

Computer organization & Architecture

**Chapters (Topics)**

I. Computer Arithmetic ✓

II. Memory Organization

III. Secondary Memories

IV. Basic processor organization and Design

V. Pipeline organization

VI. Control unit Design

VII. IO Organization

## Chapter 2 Memory Organization

- Introduction
- Memory Basics
- Memory Classification
- Memory Size Expansion
- Primary Memory
- Secondary Memory
- ROM and its design
- RAM and its design
- Memory Hierarchy
- Cache Memory
- Mapping Techniques
- Different misses occurred in cache
- Different block replacement techniques
- Tag directory design
- Associative Memory

Q. A memory has 16-bit address bus. Then how many memory locations are there?

- (a) 64k
- (b) 65,536
- (c)  $2^{16}$
- (d) All

$$\begin{aligned} & 2^{16} \\ & = 2^6 \times 2^{10} = 64 \text{ K} \\ & = 64 \times 1024 \\ & = 65536 \end{aligned}$$

Q. The address bus width of a memory of size  $2048 \times 8$  bits is

- (a) 10
- (b) 11
- (c) 12
- (d) 13

$$\begin{aligned} & \overbrace{2048 \times 8 \text{ bits}}^{\textcircled{11}} \\ & = \underbrace{2^n \times m}_{\text{bit}} \\ & n = 11 \end{aligned}$$

Q. Memory size of a memory IC can be specified as

- (a)  $M \times N$  where  $M = \text{no. of memory locations}$ ,  $N = \text{no. of bits in each location}$  Yes
- (b)  $N \times M$ , where  $N = \text{no. of bits in each location}$ ,  $M = \text{no. of locations}$  False
- (c)  $2^n \times m$ ,  $n = \text{no. of address bits}$ ,  $m = \text{no. of bits in each location}$  Yes
- (d) either a or c

MCQ

Q. The capacity of a memory unit is defined by the number of words multiplied by the number of bits per word. How many separate address and data lines are needed for a memory of  $4\text{ K} \times 16$ ?

- (a) 10 address, 16 data lines
- (b) 11 address, 8 data lines
- (c) 12 address, 16 data lines
- (d) 12 address, 12 data lines

$$4\text{ K} \times 16$$

$$\begin{array}{c} 12 \\ 2 \\ \times 16 \\ \hline A = 12, D = 16 \end{array}$$

Q. The write cycle time of a memory is 200 nsec. The maximum rate at which data can be stored.

- (a) 200 words/sec
- (b)  $5 \times 10^3$  words/sec
- (c)  $5 \times 10^6$  words/sec
- (d)  $5 \times 10^9$  words/sec

write cycle time :-

Amount of time needed to write one word on memory = 200 ns.

Rate : applicable for one second time

$$\left. \begin{array}{l} \text{writing} \\ \text{Rate/one second} \end{array} \right\} = \frac{1}{200 \times 10^{-9}} = \frac{10^9}{200} = \frac{1000 \times 10^6}{200} = 5 \times 10^6 \text{ words/sec}$$



## Memory Space

→ primarily, it is defined as work space, working area and secondarily it is defined as storage device.

Memory Space =  $\frac{\text{No. of Memory Registers} * \text{Storage capacity of one Mem. Register}}{\text{one memory register is also known as one memory pocket, one memory word, one memory location.}}$

→ In Digital Computer, Memory is used to store programs and Data



Ex:- My pendrive memory space is

4 GB

=  $4 \text{ GiB} * 1 \text{ B}$

$\frac{\text{No. of Mem. Regs}}{\text{* one byte}}$



Memory Space = No. of words +  
size of one word

No. of Registers \* size of  
one Reg.

No. of Pockets \* size of one  
pocket

Special definition for memory space  
= No. of Rows \* No. of Columns.

→ Memory Space is the combination of Address and data, Memory Address just gives logical reference but data gives physical Reference.

Ex:- SBI: 855275 : 200/-

A/c No.              Rs.  
Address              Data



bit = 0/1 = binary digit

nibble = 4 bits

Byte = 8 bits

word size = It is different from CPU to CPU and it is equal to the Data Bus size of the given processor  
= ALU size.

General purpose { 8085 CPU :  
Register size { 8086 CPU :  
80486 CPU : Word Size  
8-bit  
16 bit  
32 bit

Special definition  
for memory space :-

$$\frac{\text{No of Rows} * \text{No of Columns}}{\text{No. of Regs}} * \frac{}{\text{size of one Reg.}}$$

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	$D_0$	$D_1$	$D_2$	$D_3$
Row 0 $R_0 \rightarrow$	1	0	1	1
Row 1 $R_1 \rightarrow$	1	1	1	1
$R_2 \rightarrow$	0	0	1	0
$R_3 \rightarrow$	1	1	0	1
$R_4 \rightarrow$	0	1	0	1
$R_5 \rightarrow$	0	0	0	1
$R_6 \rightarrow$	1	1	1	0
Row 7 $R_7 \rightarrow$	1	0	0	1

$\Downarrow \Downarrow \Downarrow \Downarrow$

Mem-Space  
 $8 \times 4$  bits  
 $R \times C$

$MR_0 = MW_0$   
 $MR_1 = MW_1$   
 $MR_2$   
 $MR_3$   
 $MR_4$   
 $MR_5$   
 $MR_6$   
 $MR_7 = MW_7$

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Row 0  $\rightarrow D_0 0 0 0 0 0 P_0 W_0 R_0$

Row 1  $\rightarrow 1 1 1 1 0 P_1 W_1 R_1$

Row 2  $\rightarrow 1 0 0 0 1 0 P_2 W_2 R_2$

Row 3  $\rightarrow 1 1 0 0 0 1 P_3 W_3 R_3$

No. of words \* capacity of one word  
 $4 * 6$  bit

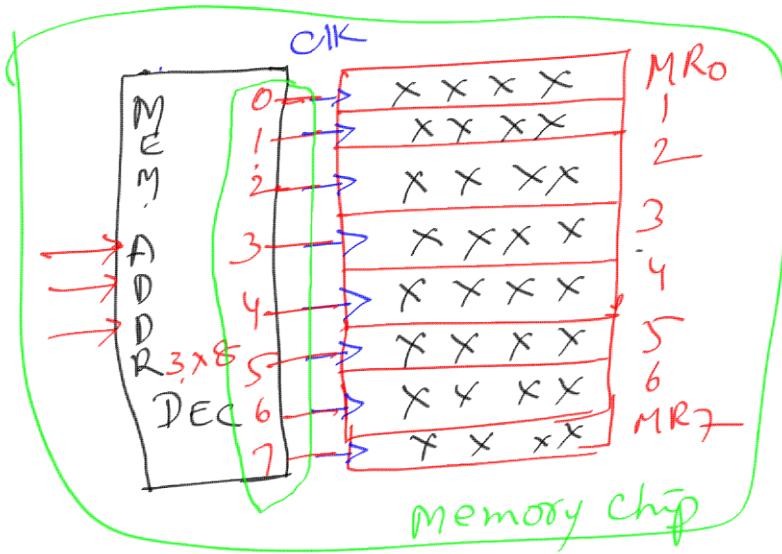


$$\begin{aligned}
 2^5 &= 32, \quad 2^{10} = 1024 \cong 10^3 = 1K \\
 2^{15} &= 2^5 \times 2^{10} = 32K \\
 2^{18} &= 2^8 \times 2^{10} = 256K \\
 2^{20} &= 2^{10} \times 2^{10} = 10^3 \times 10^3 = 1M \\
 2^{30} &= 2^{10} \times 2^{10} \times 2^{10} = 1G = 10^9 \\
 2^{40} &= 2^{10} \times 2^{10} \times 2^{10} \times 2^{10} = 1T = 10^{12}
 \end{aligned}$$

### VVVI MP.



- while designing the memory chip  
the designer fabricates one suitable size of Decoder internally.
- This Decoder is used to select only one Memory during READ/WRITE operation
- The name of the Decoder is known as Memory Address Decoder
- No. of Outputs required for the Decoder  
= No. of Memory Registers in the chip



$8 \times 4$  bits.

$R \times C$

$$f_{clk} = \frac{1}{T}$$

$$\text{let } f_{clk} = 10 \text{ Hz}$$

$$T = 0.1 \text{ sec}$$



### Decoder

Standard size:  $n \times 2^n$

Different sizes

$1 \times 2$

$2 \times 4$

$3 \times 8$

$4 \times 16$

$n \times 2^n$

$n = \text{no. of inputs}$

$2^n = \text{max. no. of o/p's}$

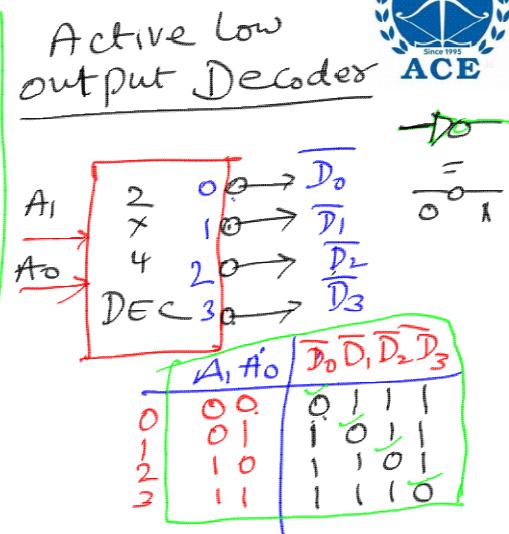
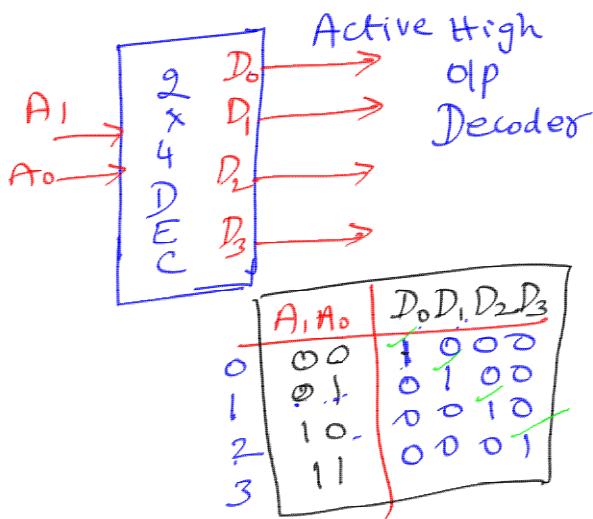


There are 2 types of Decoders  
that depends on the output nature

(i) Active High O/p Decoder

(ii) Active low O/p Decoder.

- In Active High O/p Decoder; always only one O/p bit is high in the given time
- In Active low O/p Decoder; always only one O/p bit is low in the given time





CPU = Processor = Machine = MP  
= Electronic chip

→ All Advanced CPUs are nanoprocessors;  
they complete the target operation

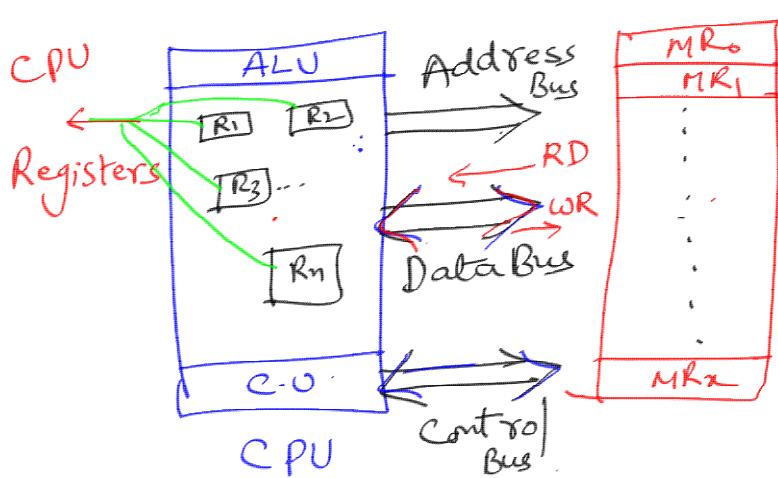
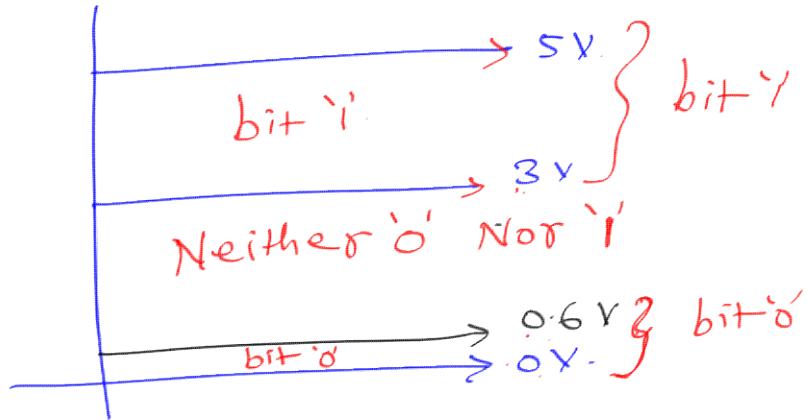
in nanoseconds since they are  
designed with  $> 1 \text{ GHz}$  clock freq.

$$f_{clk} = 1 \text{ GHz}$$

$$T = 1 \text{ ns}$$

$$\begin{aligned}10^{-3} &= \text{m Sec} \\10^{-6} &= \mu\text{sec} \\10^{-9} &= \text{n sec} \\10^{-12} &= \text{p sec}\end{aligned}$$

- while designing the CPU, the design designs 3 buses
- Bus is the group of wires
- one wire can carry only one bit
- when voltage on that line is '0V'  
then it is considered as 'bit '0'
- when voltage on that line is b/w  
3V and 5V, it is considered as  
bit '1'.



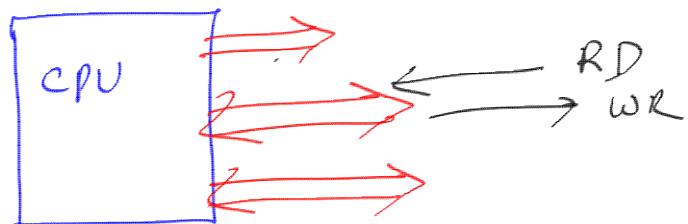
→ CPU Register  
is used to  
store  
operand  
during program  
execution.



- CPU uses these buses for communicating with Memory or Io devices
- Address Bus is used to select one of the Memory Registers in the available memory space.
- Data Bus is used to perform Read / write operation.
- Control Bus is used to send Control signals and Hand shaking signals.



- Data travelled towards CPU is known as READING
- Data travelled from the CPU is known as - WRITING

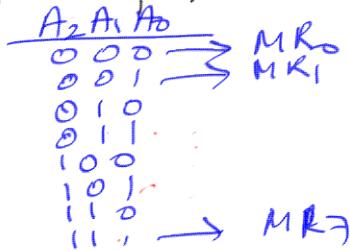




Ex) Let CPU is having 3 Address lines and 4 data lines.

18) word size of the CPU is 4 bits

29) Max no. of Addressable Registers =  $\frac{3}{2}$



→ max. memory space to be addressed =  $2^3 * 4$  bits





Let a CPU has n Address lines  
and m data lines.

- 1) word size is m bit
- 2) max no. of Addressable Registers =  $2^n$
- 3) max Memory space to be Addressed  
 $= 2^n * m \text{ bits}$
- 4) It is also known as m bit CPU

Address Bus Size = n bit



Starting Address: 0 0 0 0 ..... 0 (n)

ending Address: 1 1 1 ..... 1 (n)  
 $= \frac{n}{2}$



e) Let CPU has 16 Address lines and 32 data lines.

18) word size is 32 bits.

20) It is also known as 32 bit CPU

28) Max no. of Addressable Regs =  $2^{16}$

38) Max Memory space to be addressed is  $2^{16} * 32$  bits

(48) 50) Max Memory space to be addressed is \_\_\_\_\_ Kilo Bytes

$$\begin{aligned} & \text{Ans: } 256 \\ & = 2^{16} \times 32 \text{ bits} \\ & = 2^{16} \times 4 \text{ Bytes} = (2^6 \times 2^{10}) \times 4 \text{ Bytes} \\ & = 64 \text{ K} \times 4 \text{ Bytes} \\ & = 256 \text{ K Bytes} \end{aligned}$$