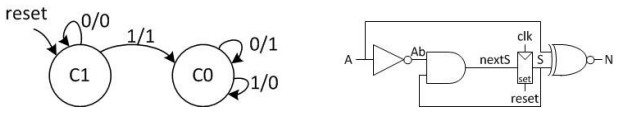
Twos Complementer

Problem Statement

Recall the Serial Two's Complementer you designed as a Mealy FSM in the Chapter 3 practice problems. The FSM takes a binary number one bit at a time, starting with the least significant bit, and puts out its negative (two's complement), one bit at a time. The state transition diagram and circuit are shown below.



The goal of this lab problem is for you to code the **Mealy FSM** in **structural** SystemVerilog. Use only flip-flops, AND, OR, and NOT gates in your solution.

Start with the files below. Modify the twoscomp module to describe the schematic above. Notice that SystemVerilog code for an ordinary flip-flop and for asynchronously resettable and settable flip-flops are provided; you will need to instantiate one of these for your state register. The test bench takes input 0010 and produces an expected output of 1110. Don't change the testbench or test vectors because that would mess up the hash.

Simulate your design and debug any discrepancies.