Kunal Kumar

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Projects

Graduate Research Assistant — *Palaiseau, France*
Laboratoire de Physique de la Matière Condensée, Dept. of Chimie, l'X — Sept 2025 – Current

- Aim to create a QD-LED with ZnO as electron transport layer, organic multitudes as hole transport layer and CdSe/CdTe/CdSe QDs for combination of narrow green and red emission with tunable magnitude of peaks
- Optimized fibre-laser operating parameters for etching of ITO electrodes achieving minimum-linewidth of 18μm

Undergraduate Research Assistant — *Mumbai, India*
Electronics & Materials Physics Lab, MEMS dept., IITB — Aug 2024 – Aug 2025

- Developed a Monte Carlo simulator for improving spin-conditions based on various forces to homogeneously distribute Au Nanoparticles (based on size, surfactant & concentration) on Si/SiO_2 & c-sapphire substrate
- Built a Transfer Matrix Method for determining optical contrast based on Total Color Difference on MATLAB which could predict the z-thickness of MoS_2 crystals on Si/SiO_2 from the OM images within 3-nm accuracy
- Produced & optimized regular-circular growth of WS_2 on c-sapphire using 50-nm AuNP in a LPCVD system

Summer Research Assistant — *Daejeon, South Korea*
Quantum Nanobio & Photonics Lab, Physics Dept., KAIST — June 2024 – Aug 2024

- Developed location marker on InGaN/GaN multi-quantum well sample using UV-photolithograpy, wet-etching and current-controlled e-beam evaporation of nano-scale Cr/Au platings for finer view under OM & PL scopes
- Utilized Monte Carlo simulations (SRIM) to analyze depth profile and collision dynamics of Ga ions and improve FIB milling by tuning accelerating voltage & angle for fabricating 3D confined donuts on quantum-well sample
- Mapped CL & PL spectra for broadband peaks & emission of single-photons through 3D confined regions

Experience

Research Analyst — *Mumbai, India*
Jaguar Land Rover Chiplet Challenge - Inter IIT Tech Meet 12.0 — Sept 2023 – Dec 2023

- Examined architectures of NVIDIA DRIVE Orin (200 TOPS, 200 GB/s) and Tesla FSD (73.7 TOPS, 63 GB/s) — identifying 18% latency reduction potential via chiplet partitioning and interposer-optimized interconnects.
- Designed a chiplet topology through rectangle-packing optimization reducing die area by 23% and power by 15%, while boosting bandwidth 4× (200 → 800 GB/s) and lowering latency 20% versus monolithic SoC layouts.
- Proposed UCIe-based interconnects achieving 40% higher throughput and 30% lower error rate than PCIe 5.0/CXL links, while ensuring ISO 26262, ASIL-D and SAE L4–L5 automotive compliance for vehicle safety

Avionics Engineer & Lead PCB Designer — *Mumbai, India*
IITB Rocket Team — Dec 2022 – Jun 2024

- Designed the flight computer for 30,000-ft sounding rocket on Autodesk Eagle in 3 iterations based on Raspberry Pi Pico coupled with an MPU6050 IMU and BMP280 pressure sensor for data processing and sensor fusion
- Deployed LoRa Sub-GHz transmission module for telemetry, geo-tagging and live feed for the on-ground station
- Optimized a kalman filter sub-routine in MATLAB with variables calculated from test runs and thrust profile

Education

Institut Polytechnique de Paris — Aug 2027 (Expected)
Masters of Science, Chemistry and Interfaces

Indian Institute of Technology Bombay — Nov 2021 - May 2025
Bachelors of Technology, Metallurgical Engineering & Materials Science (Honors) — GPA: 8.23/10

Skills

Equipment: Oscilloscope, Spin-coater, Profilometer, Photolithography system, OM, SEM, AFM, CVD, Digital Multimeter, e-beam evaporator, FIB (basic operation), PL system
Electronics: Arduino, Raspberry Pi, BJTs, Op-Amps, ESP
Programming: MATLAB, Python
Software Tools: Ansys Lumerical, Workbench, EAGLE, LaTeX, Google Suite, Microsoft Office