

# Dev Rajiv Kansara

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LinkedIn | GitHub | Portfolio

## EDUCATION

### Ahmedabad University

B.Tech in Computer Science and Engineering (CGPA: 3.76 / 4.00)

Aug 2023 – May 2027 (Expected)

Ahmedabad, Gujarat

### Gujarat Secondary & Higher Secondary Education Board

HSC (Science) – 91.84% (District Topper)

May 2023

Gujarat

## EXPERIENCE

### Teaching Assistant – Digital Logic & HDL

Ahmedabad University (Prof. Harmeet Kaur)

Aug 2025 – Nov 2025

Ahmedabad, Gujarat

- Mentored undergraduate students in circuit design using **Logisim** and **Verilog HDL**, facilitating weekly 2-hour labs.
- Evaluated 10 comprehensive lab reports covering K-Maps, Boolean Algebra, and FSM design (Mealy/Moore).
- Bridged the gap between theory and practice by resolving queries regarding combinational and sequential logic.

### Web Development Intern

MICA University (Prof. Suresh Malodia)

Jun 2025 – Jul 2025

Ahmedabad, Gujarat

- Developed "Ghaziabad NH-9 Cattle Problem," an interactive game simulating traffic scenarios for research.
- Implemented real-time data synchronization using **Firebase Firestore** to track student performance.
- Built a custom analytics dashboard allowing professors to monitor student interactions with AI prompts.

### Freelance Web Developer

Client: Urjit Mehta (M.Tech CS & AI)

Jun 2025 – Jul 2025

Remote

- Architected "AI Nexus," a high-performance portfolio platform using **React.js** and **Tailwind CSS**.
- Automated CI/CD deployment pipelines using **GitHub Actions** and Firebase Hosting.

## PROJECTS

### Planetary Exploration Rover: Hybrid AI | Python, A\*, Heuristics

Oct 2025 – Dec 2025

- Designed a hybrid reactive-deliberative AI for Martian rover navigation in a probabilistic grid world.
- Integrated a Reflex Agent for hazard avoidance with an A\* Planner for long-term goal optimization.
- Implemented memory-based loop prevention and a three-tier battery management system.

### Five-Cycle RISC Processor (25-bit) | Verilog HDL, GTKWave

Feb 2025 – Apr 2025

- Designed a 25-bit non-pipelined RISC processor adhering to a five-stage architecture (Fetch to Write Back).
- Implemented ALU, Control Unit, and Output Logic; verified datapath via simulation in EDA Playground.

### Decentralized Traffic Route Optimization | Python, Graph Theory

Feb 2025 – Mar 2025

- Implemented a Randomized A\* algorithm using Boltzmann probability distributions to minimize congestion.
- Modeled decentralized networks using graph data structures to optimize travel time in complex topologies.

## TECHNICAL SKILLS

**Languages:** Python, Java, C, JavaScript, Verilog HDL, SQL, RISC-V Assembly

**Web/Tools:** React.js, Tailwind CSS, Firebase, Git/GitHub, GitHub Actions, VS Code, Logisim

**AI & Algorithms:** A\* Search, Heuristic Analysis, NumPy, Pandas, Matplotlib, Scikit-learn, OpenCV

## LEADERSHIP & EXTRACURRICULAR

**Competitive Programming:** Team contributor; authored solutions for complex DSA problems (Aug 2024 – Present).

**Volleyball Teaching Assistant:** Instructed first-year students through the Work-Study Program (Aug 2024 – Apr 2025).