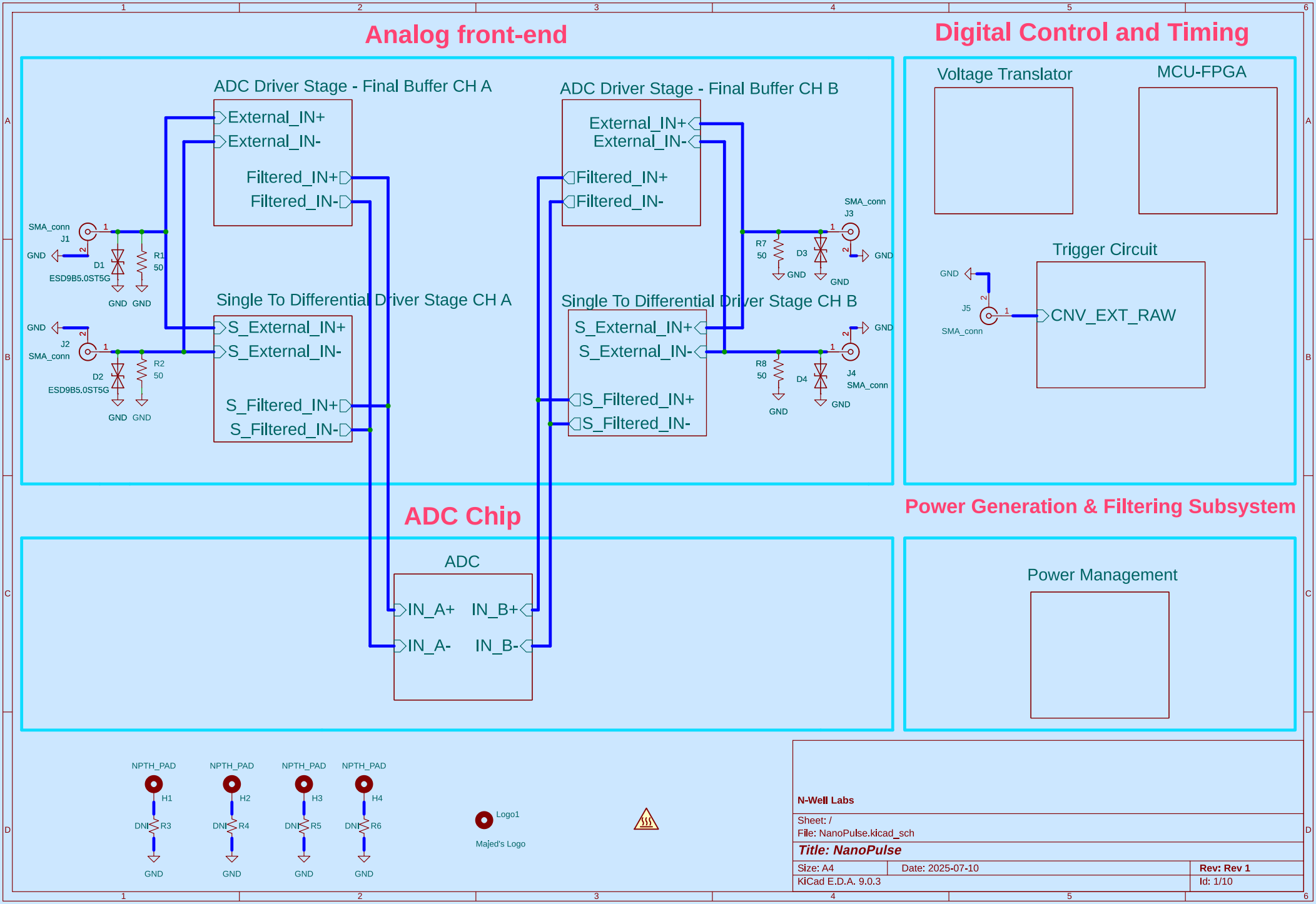
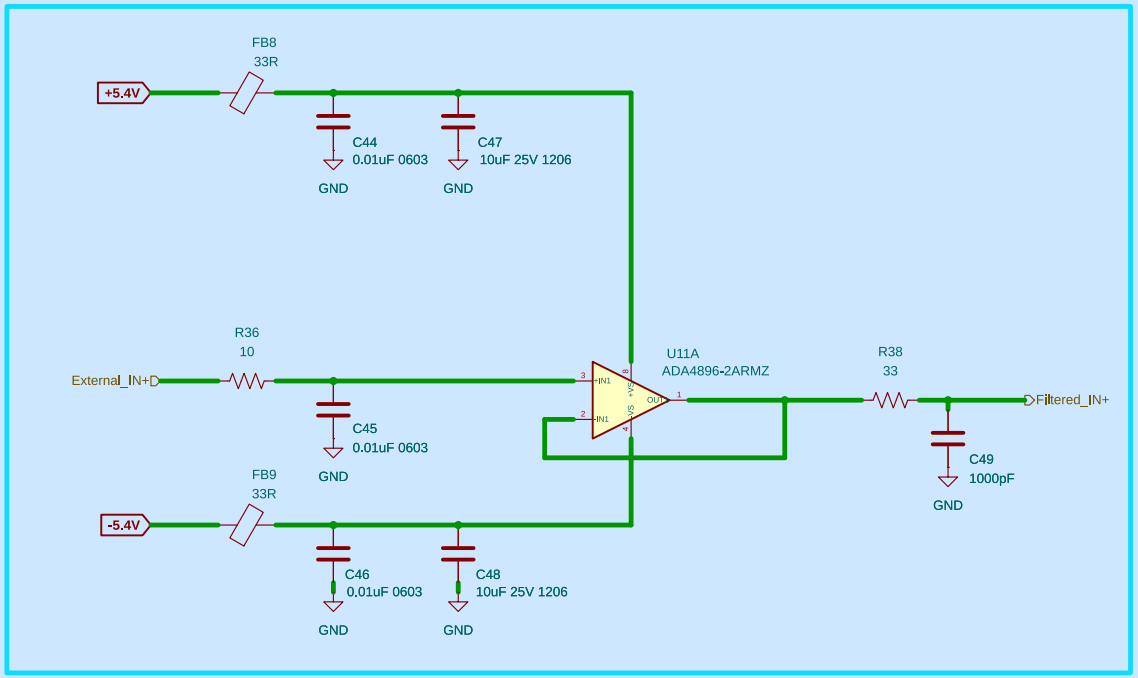
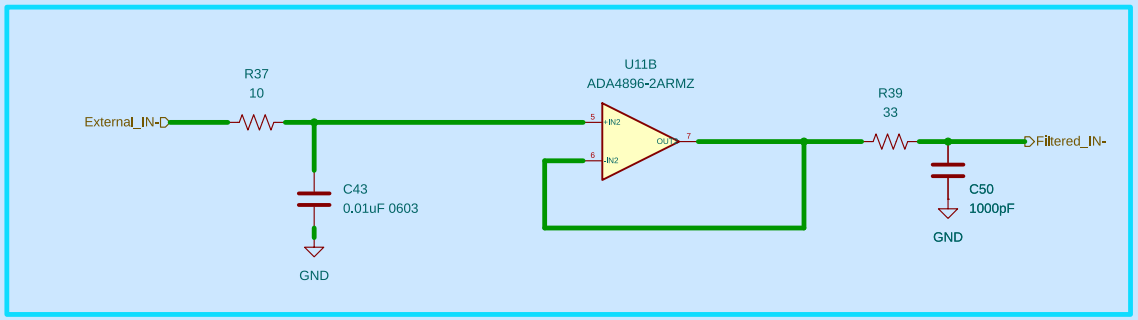

Analog front-end
Digital Control and Timing
ADC Driver Stage - Final Buffer CH A
External_IN+
External_IN-
Filtered_IN+
Filtered_IN-
ADC Driver Stage - Final Buffer CH B
External_IN+
External_IN-
Filtered_IN+
Filtered_IN-
SMA_conn
J1
GND
D1
ESD9B5.0ST5G
R1
50
GND GND
SMA_conn
J3
R7
50
D3
GND
GND
GND
Single To Differential Driver Stage CH A
S_External_IN+
S_External_IN-
S_Filtered_IN+
S_Filtered_IN-
Single To Differential Driver Stage CH B
S_External_IN+
S_External_IN-
S_Filtered_IN+
S_Filtered_IN-
GND
SMA_conn
J2
D2
ESD9B5.0ST5G
R2
50
GND GND
R8
50
D4
J4
SMA_conn
GND
GND
Voltage Translator
MCU-FPGA
Trigger Circuit
GND
J5
SMA_conn
CNV_EXT_RAW
ADC Chip
ADC
IN_A+
IN_B+
IN_A-
IN_B-
Power Generation & Filtering Subsystem
Power Management
NPTH_PAD
H1
DNI
R3
GND
NPTH_PAD
H2
DNI
R4
GND
NPTH_PAD
H3
DNI
R5
GND
NPTH_PAD
H4
DNI
R6
GND
Logo1
Majed's Logo
N-Well Labs
Sheet: /
File: NanoPulse.kicad_sch
Title: NanoPulse
Size: A4
Date: 2025-07-10
Rev: Rev 1
KiCad E.D.A. 9.0.3
Id: 1/10

Signal Conditioning & Buffering [IN +]



Signal Conditioning & Buffering [IN -]



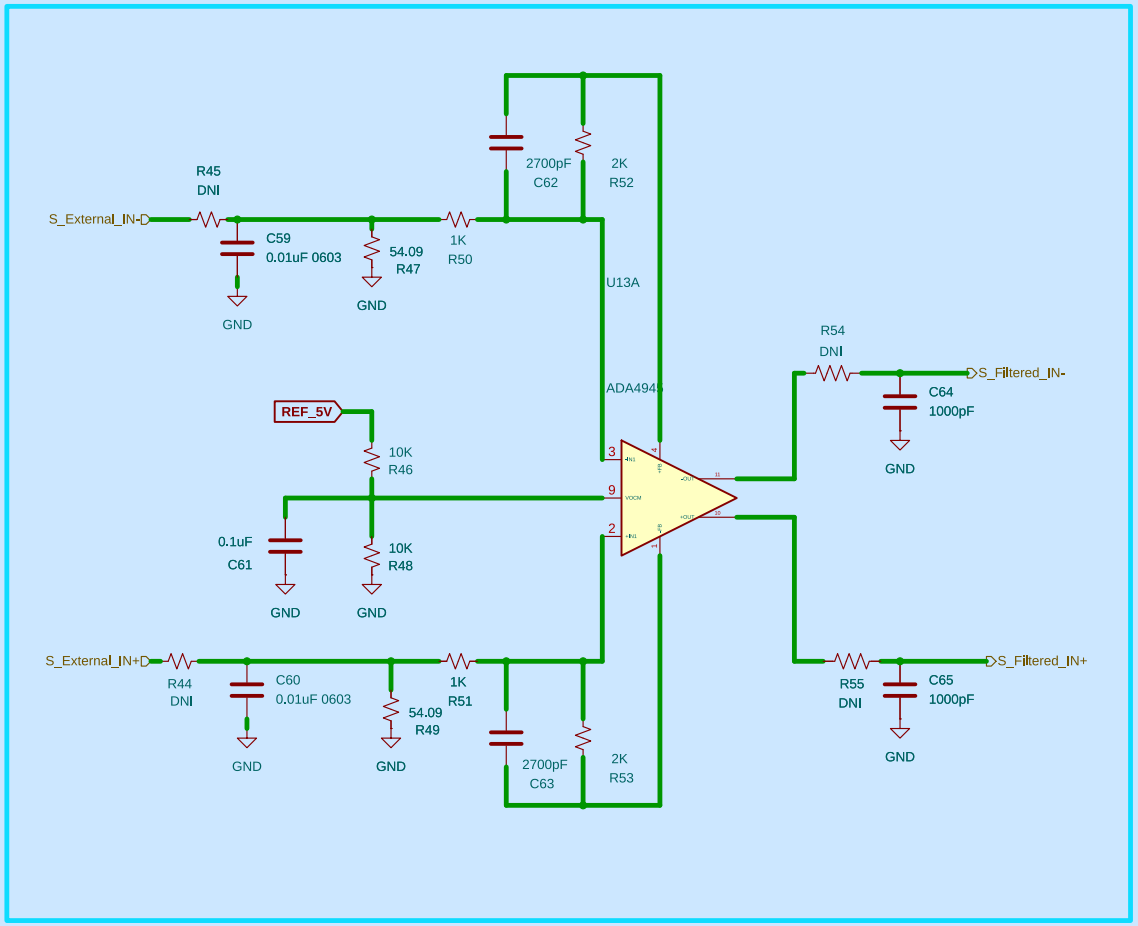
N-Well Labs

Sheet: /ADC Driver Stage - Final Buffer CH A/
File: ADC_Driver_Stage-Final-Buffer.kicad_sch

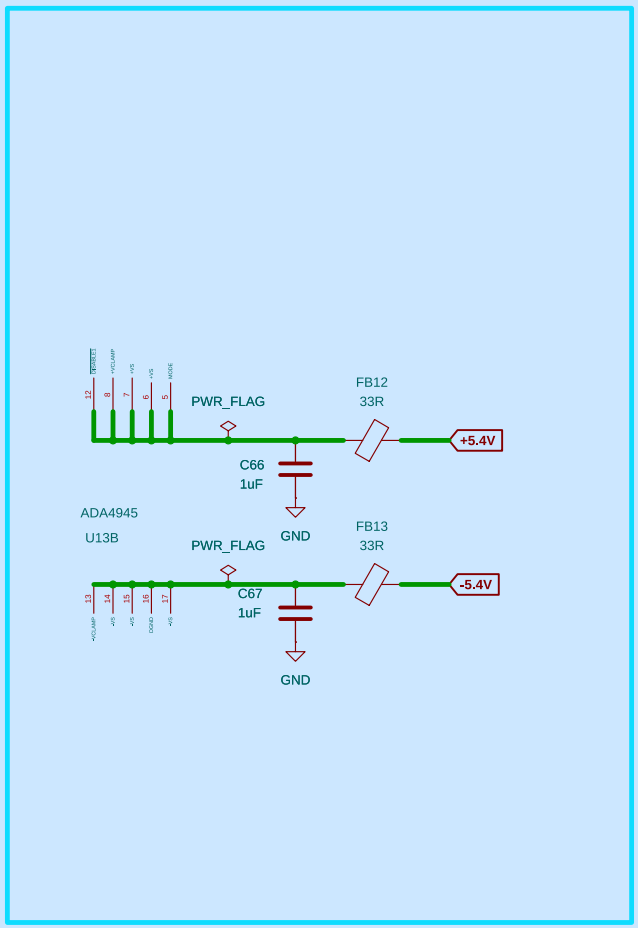
Title: NanoPulse - ADC Driver Stage

Size: A4	Date: 2025-07-10	**Rev: Rev 1**
KiCad E.D.A. 9.0.3		Id: 5/10

Signal Conditioning & ADC Driver [Single to Diff]

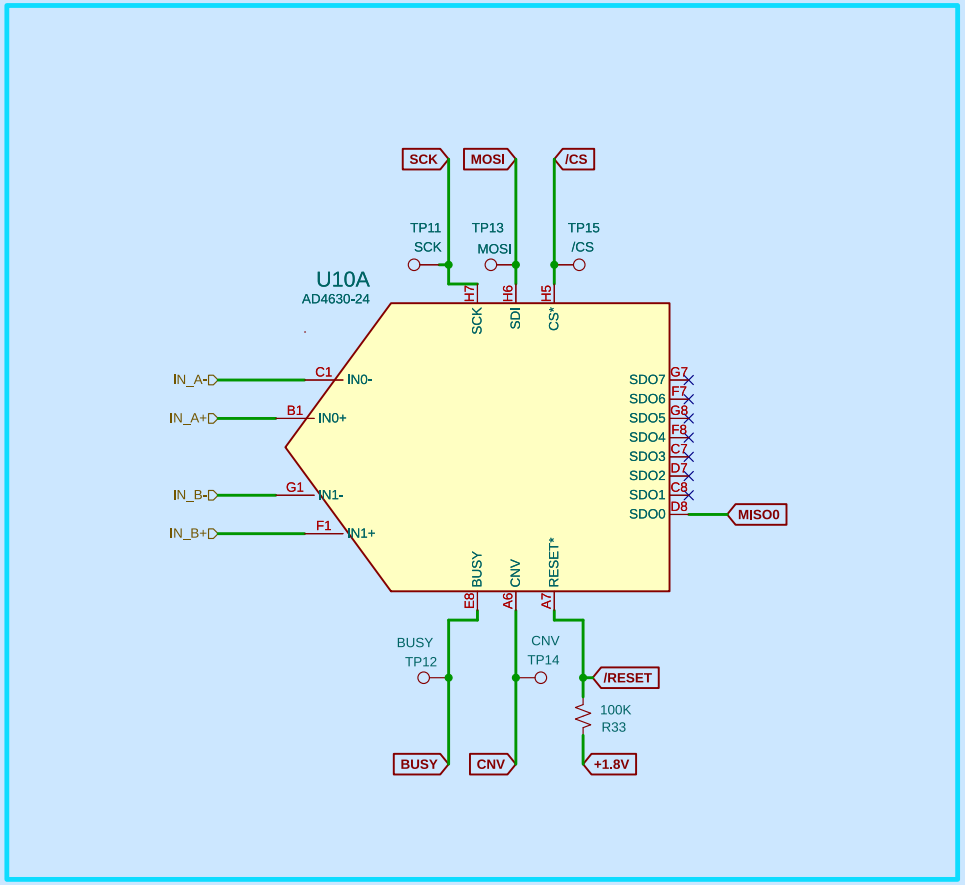


Power Conditioning for Op-Amp

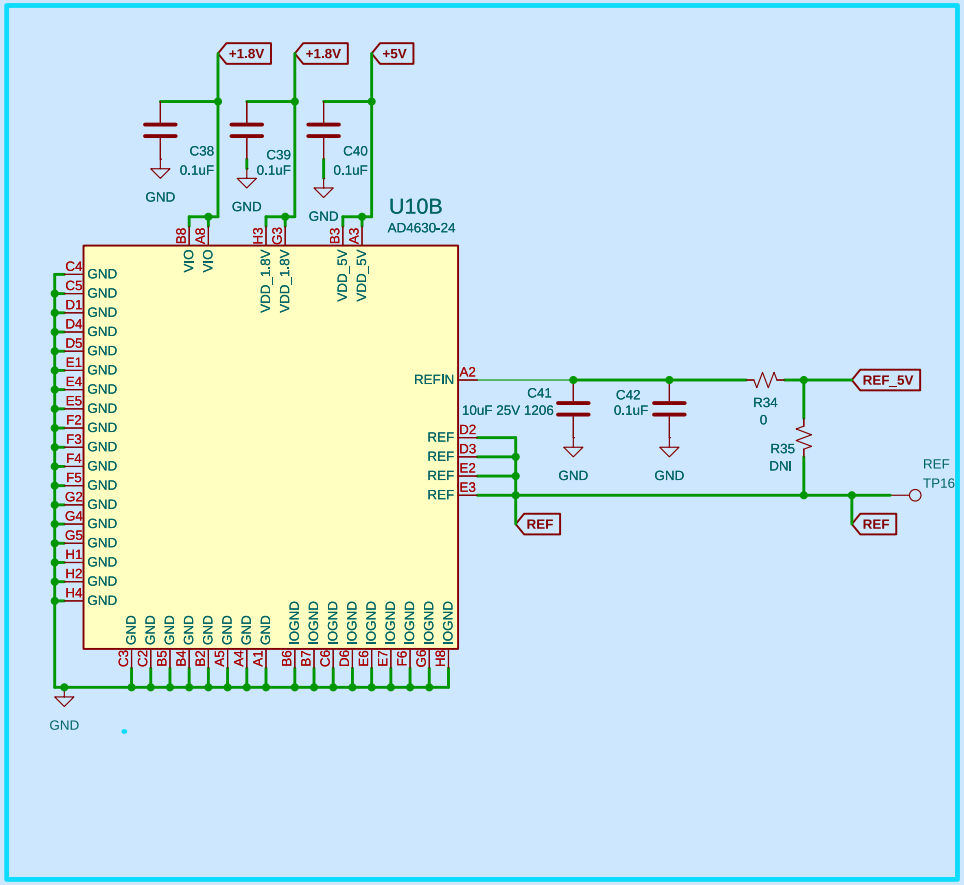


N-Well Labs		
Sheet: /Single To Differential Driver Stage CH A/ File: Single_To_Diff_Driver_Stage.kicad_sch		
Title: NanoPulse - Single to Diff Driver		
Size: A4	Date: 2025-07-11	**Rev: Rev 1**
KiCad E.D.A. 9.0.3		Id: 7/10

Analog Interface

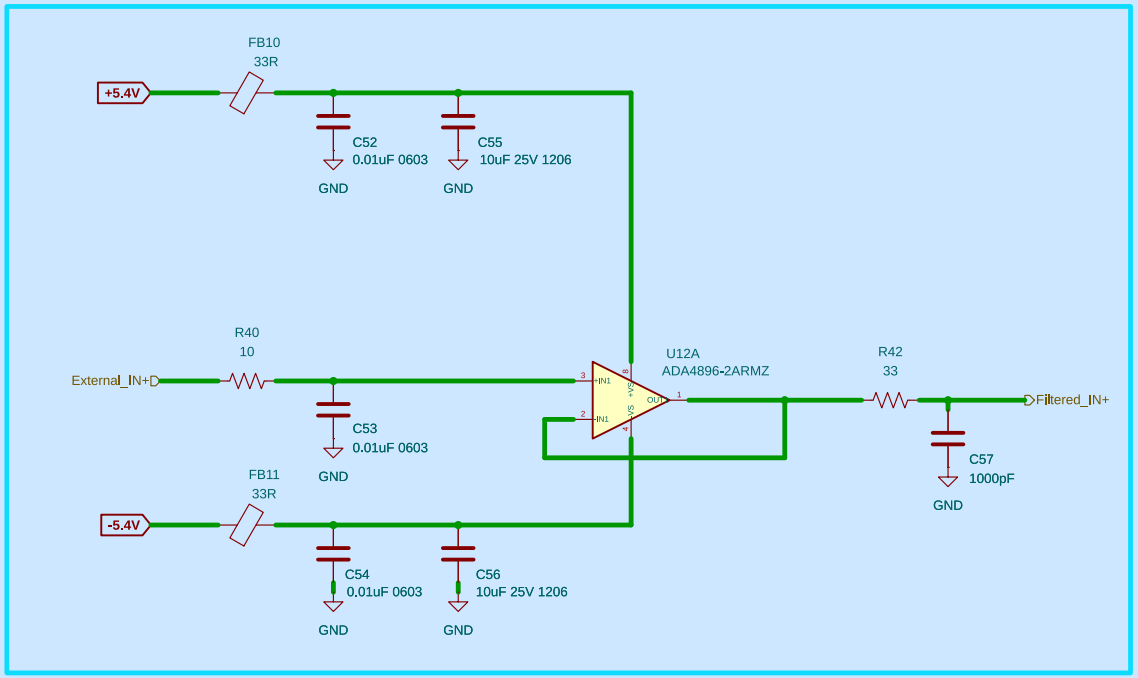


Power and Reference

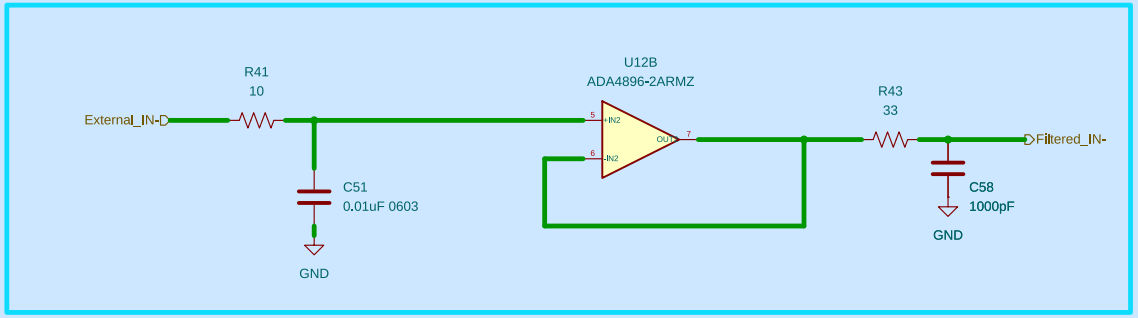


N-Well Labs		
Sheet: /ADC/ File: ADC.kicad_sch		
Title: NanoPulse - ADC		
Size: A4	Date: 2025-07-10	**Rev: Rev 1**
KiCad E.D.A. 9.0.3		Id: 4/10

Signal Conditioning & Buffering [IN +]



Signal Conditioning & Buffering [IN -]



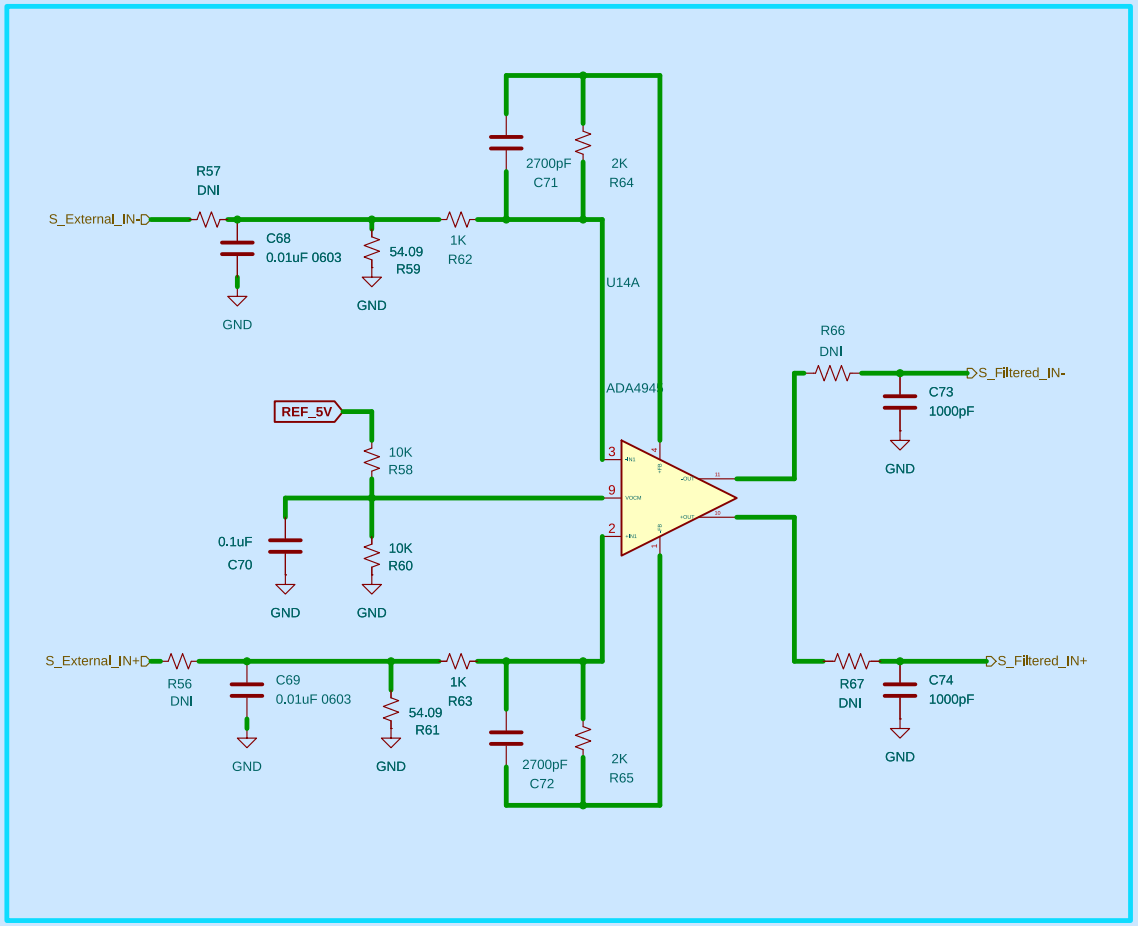
N-Well Labs

Sheet: /ADC Driver Stage - Final Buffer CH B/
File: ADC_Driver_Stage-Final-Buffer.kicad_sch

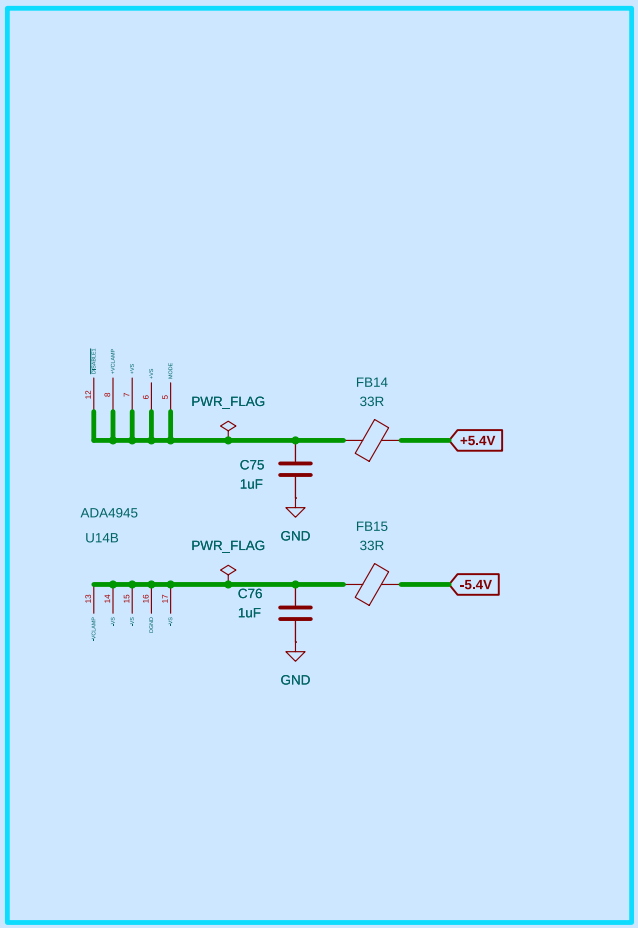
Title: NanoPulse - ADC Driver Stage

Size: A4	Date: 2025-07-10	**Rev: Rev 1**
KiCad E.D.A. 9.0.3		Id: 6/10

Signal Conditioning & ADC Driver [Single to Diff]



Power Conditioning for Op-Amp



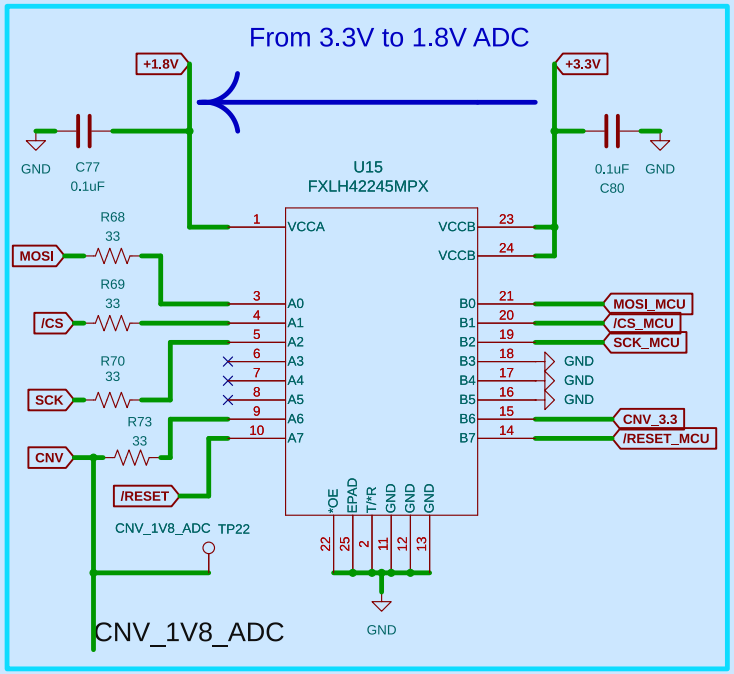
N-Well Labs

Sheet: /Single To Differential Driver Stage CH B/
File: Single_To_Diff_Driver_Stage.kicad_sch

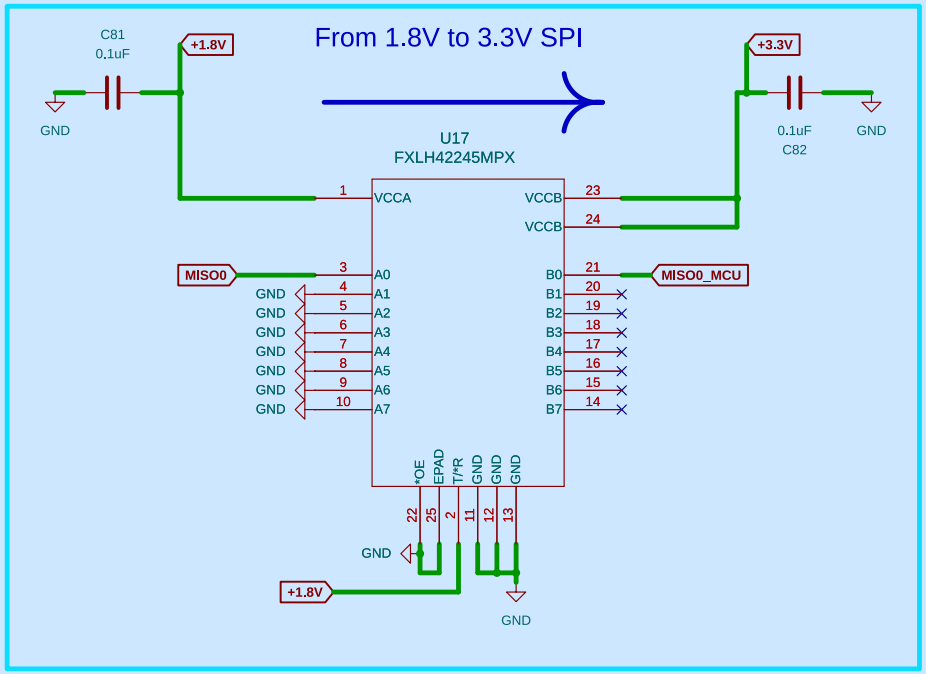
Title: NanoPulse - Single to Diff Driver

Size: A4	Date: 2025-07-11	**Rev: Rev 1**
KiCad E.D.A. 9.0.3		Id: 8/10

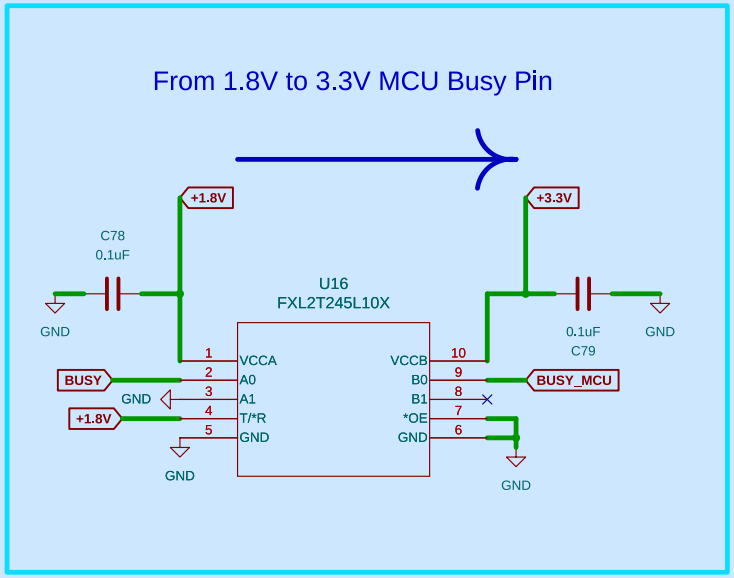
Voltage Level Transilator [1.8V - 3.3V]



Voltage Level Transilator [For Octo-SPI]



Voltage Level Transilator [BUSY]



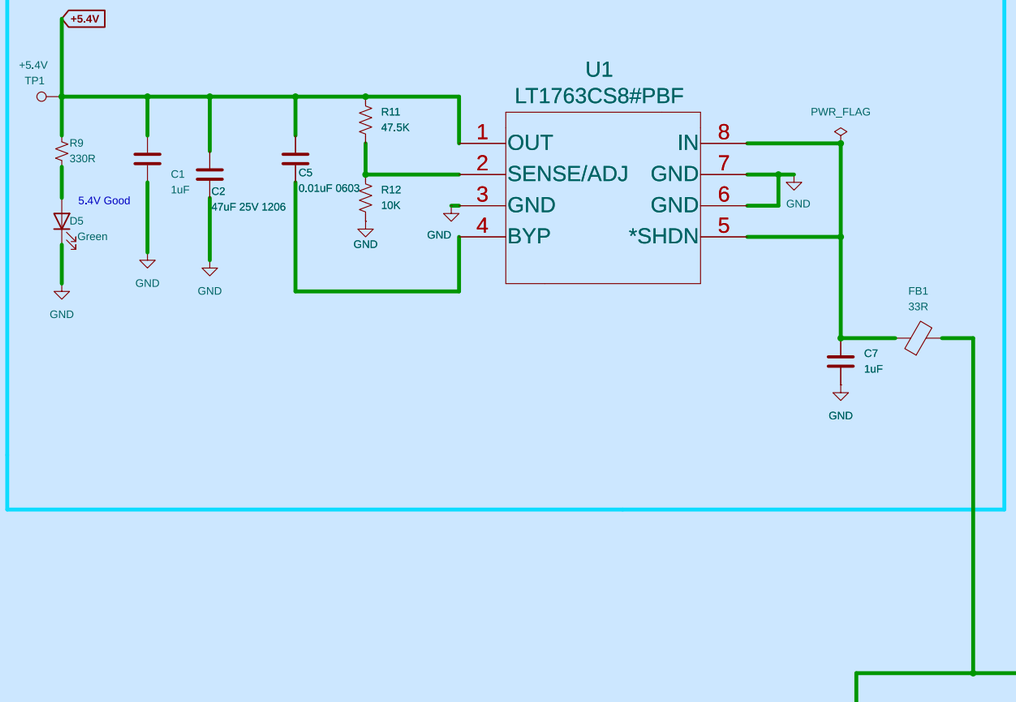
N-Well Labs

Sheet: /Voltage Translator/
File: Voltage_Translator.kicad_sch

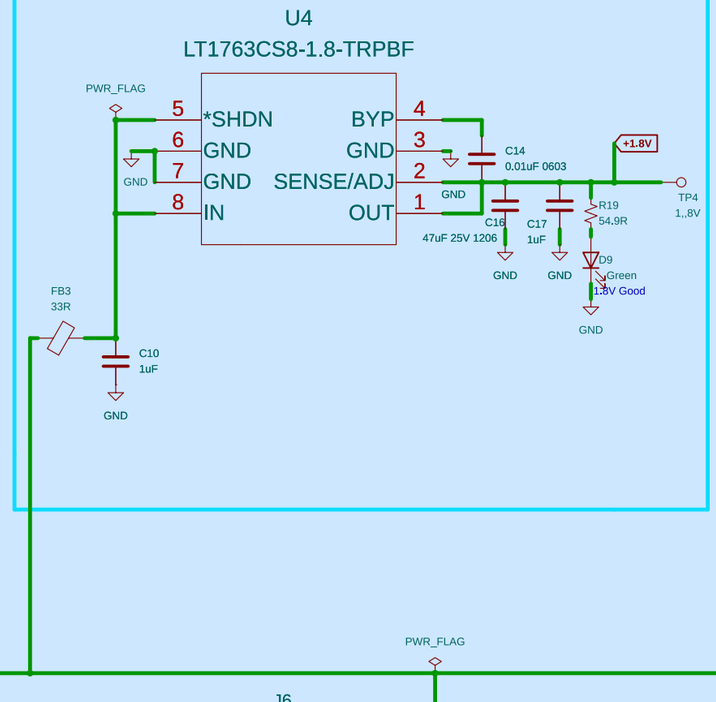
Title: NanoPulse - Violtage Translator

Size: A4	Date: 2025-07-11	**Rev: Rev1**
KiCad E.D.A. 9.0.3		Id: 9/10

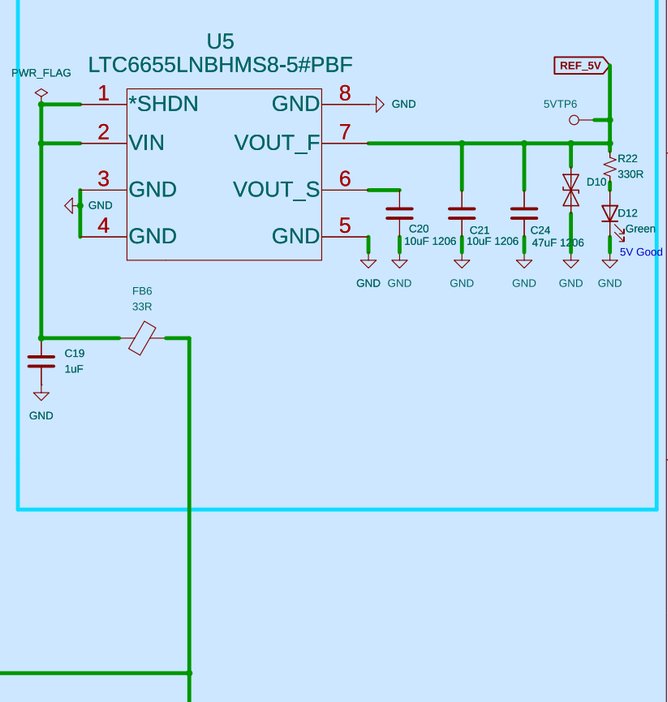
5.4V Analog Positive Rail

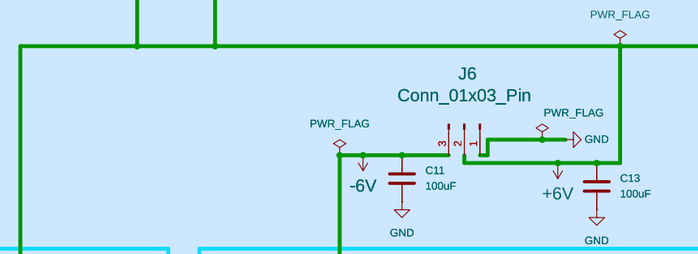


ADC Digital Rail

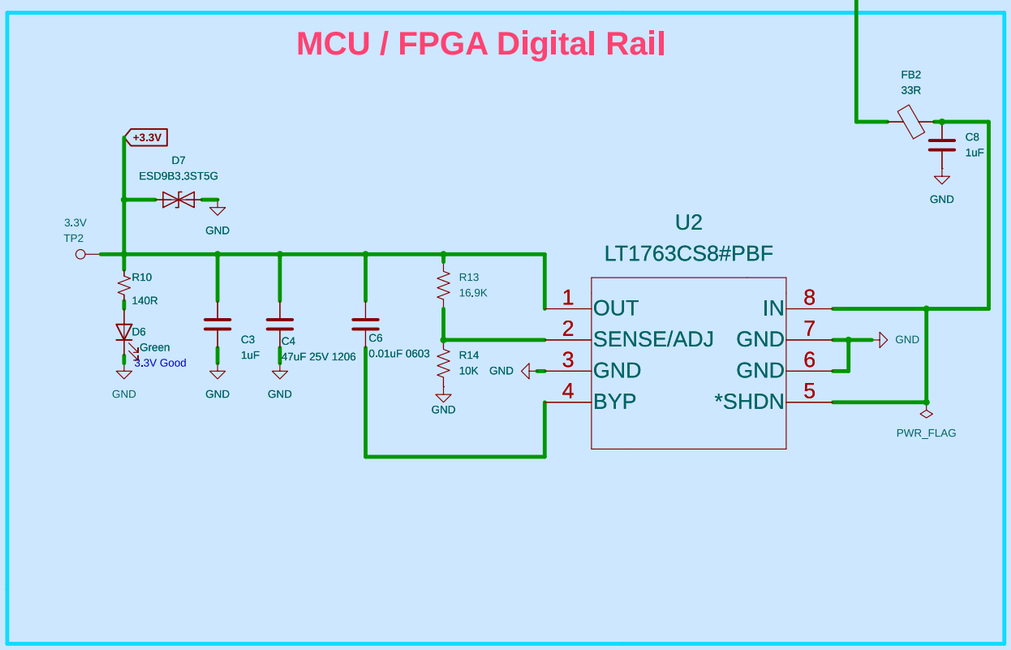


+5V Precision Reference

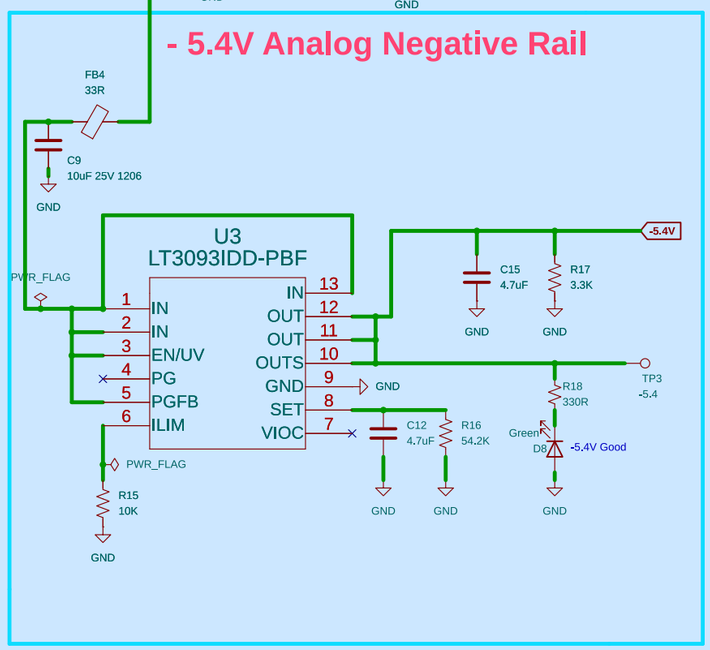




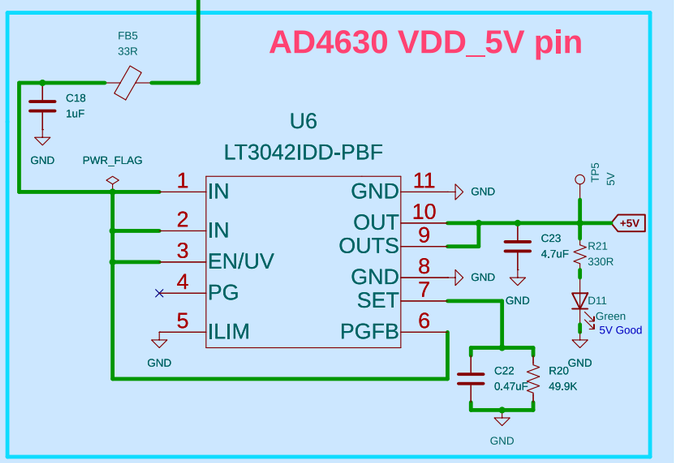
MCU / FPGA Digital Rail



- 5.4V Analog Negative Rail



AD4630 VDD_5V pin



N-Well Labs

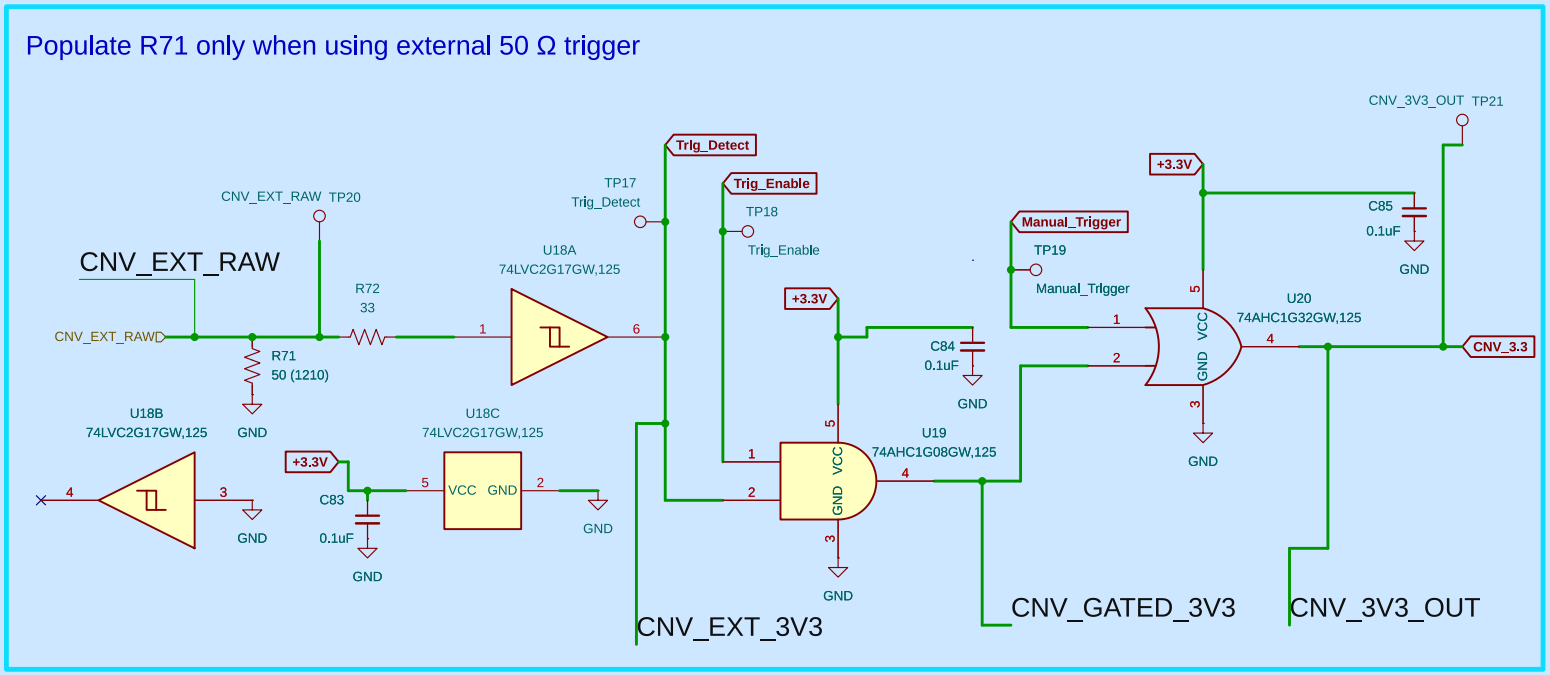
Sheet: /Power Management/
File: Power_Management_sch.kicad_sch

Title: NanoPulse - Power Management

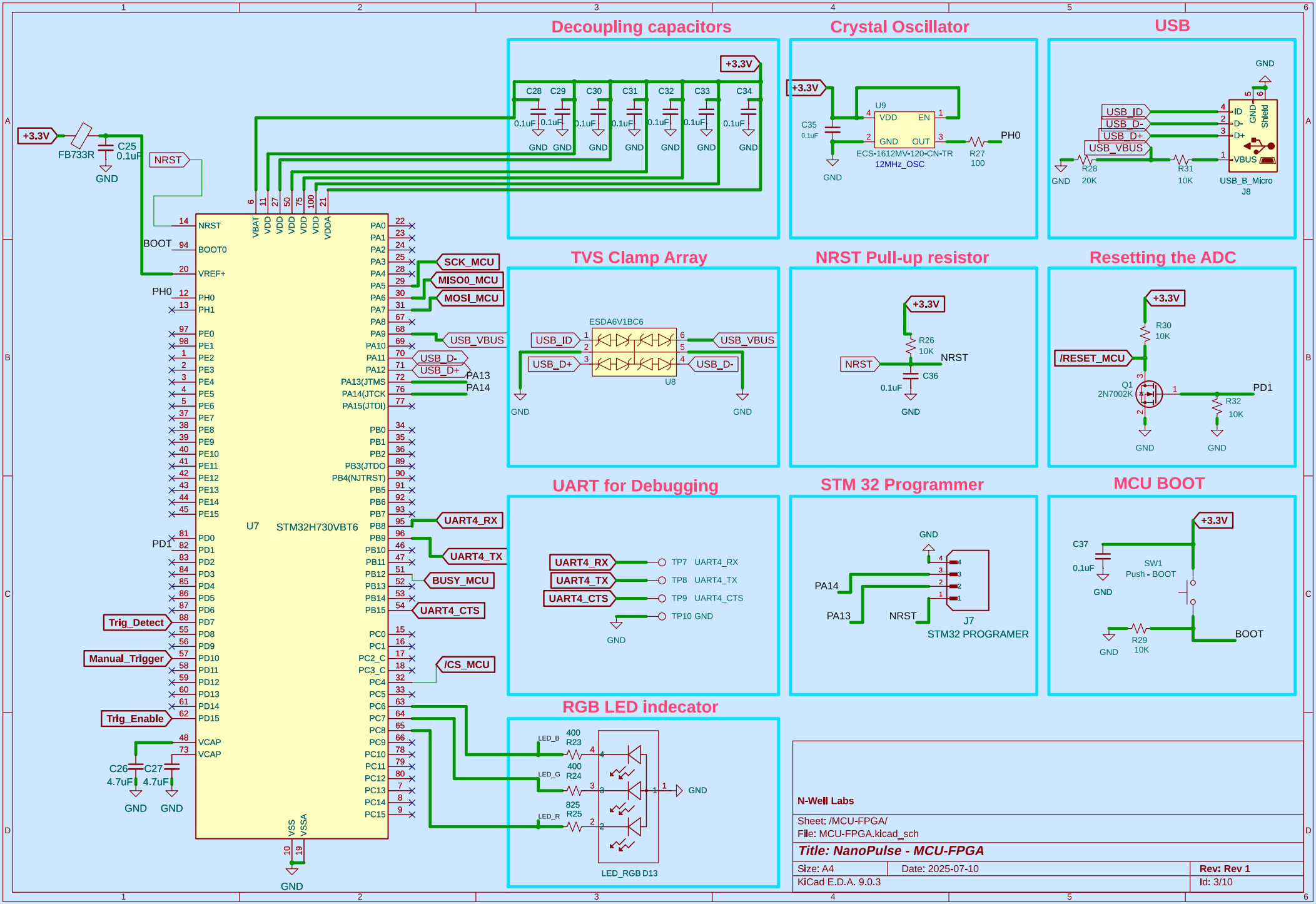
Size: A3	Date: 2025-07-10	**Rev: Rev 1**
KiCad E.D.A. 9.0.3		Id: 2/10

Trigger Circuit

Populate R71 only when using external 50 Ω trigger



N-Well Labs		
Sheet: /Trigger Circuit/ File: Trigger_Circuit.kicad_sch		
Title: NanoPulse - Trigger Circuit		
Size: A4	Date: 2025-07-11	**Rev: Rev 1**
KiCad E.D.A. 9.0.3		Id: 10/10


Decoupling capacitors
Crystal Oscillator
USB
TVS Clamp Array
NRST Pull-up resistor
Resetting the ADC
UART for Debugging
STM 32 Programmer
MCU BOOT
RGB LED indecator
U7 STM32H730VBT6
ECS-1612MV-120-CN-TR
12MHz_OSC
ESDA6V1BC6
USB_B_Micro
J8
STM32 PROGRAMER
J7
SW1
Push - BOOT
LED_RGB D13
N-Well Labs
Sheet: /MCU-FPGA/
File: MCU-FPGA.kicad_sch
Title: NanoPulse - MCU-FPGA
Size: A4
Date: 2025-07-10
Rev: Rev 1
KiCad E.D.A. 9.0.3
Id: 3/10