L J Institute of Engineering and Technology, Ahmedabad.

COA Practice Book_2025

Note: This Practice Book is only for reference purpose. LJU Test question paper may not be completely set from Practice Book.

Sr. No.	subject_code	unit_number	question_text	answer_text	marks	option1	option2	option3	option4
1	017013493	1	What is computer architecture?	b	1	set of categories and methods that specify the functioning, organisation, and implementation of computer systems	set of principles and methods that specify the functioning, organisation, and implementation of computer systems	set of functions and methods that specify the functioning, organisation, and implementation of computer systems	None of the mentioned
2	017013493	1	What is computer organization?	a	1	structure and behaviour of a computer system as observed by the user	structure of a computer system as observed by the developer	structure and behaviour of a computer system as observed by the developer	All of the mentioned
3	017013493	1	8-Bit representation of (-120) in Signed magnitude and signed 2's Complement	a	1	1 1111000 and 1 0001000	1 1111001 and 1 0000111	1 0011001 and 1 1100110	1 1110000 and 0 0001111
4	017013493	1	Using 11 bit 2's complement representation, what is the minimum and maximum integer that can be represented in decimal?	a	1	-1024,1023	-1023,1023	-1023,1024	-1024,1024
5	017013493	1	Using 12-bit 2's complement representation, what is the minimum and maximum integer that can be represented in decimal?	a	1	- 2048 , 2047	-4096, 4096	-2047, 2048	-2047, 2047
6	017013493	1	Which of the following statements is/are correct? 1) 10's complement of a number is its 9's complement -1 2) The 1's complement of a number can be obtain by subtracting each bit of the number from 1. 3) MSB of mantissa is non-zero in a normalized floating-point number.	b	1	Both 1 and 2	Both 2 and 3	Only 1	All of the above
7	017013493	1	Let R1 and R2 be two 4-bit registers that store numbers in 2's complement form. For the operation R1+R2, which one of the following values of R1 and R2 gives an arithmetic overflow?	b	1	R1 = 1011 and R2 = 1110	R1 = 1100 and R2 = 1010	R1 = 0011 and R2 = 0100	R1 = 1001 and R2 = 1111
8	017013493	1	Which of the following 4-bit pattern is 2's complement of sign magnitude number 1010?	c	1	1010	0010	1110	0110
9	017013493	1	The addition of 4-bit, two's complement, binary numbers 1101 and 0100 results in____	c	1	1001 and no overflow	1000 and an overflow	0001 and no overflow	1001 and an overflow
10	017013493	1	What is minimum integer in 14 bit 2's complement representation in decimal	b	1	8191	-8192	-8191	16384
11	017013493	1	Represent fix point representation for Unsigned Binary no 0110110 using 4 integer bits and 3 fractional bits in decimal.	0110.110,(6.75)10	1				
12	017013493	1	Compute(0.75)10 +(-0.625)10 using fixpoint representation.	(0000.0010)2	1				
13	017013493	1	Convert decimal no 7.75 to fixed point binary	(0111.1100)2	1				
14	017013493	1	Perform the addition operationusing signed 10's compliment representation (+375)+(-240)	(0135)10	1				
15	017013493	1	What is the minimum integer in 11 bit 2's compliment representation in decimal	-1024 to 1023	1				
16	017013493	1	Perform the subtraction with following unsigndecimal number by taking 10's compliment representation i)5250-1321 ii)20-100		2				
17	017013493	1	Perform the subtraction with following unsigndecimal number by taking 2's compliment representation i)11010-1101 ii)100-110000		2				
18	017013493	1	Using 2's compliment form convert the following decimal no. into fixed point binary no. stored in 16- bit register having 4-bit after decimal point. a)7.5 b)-45.75	a)(0000 0000 0111.1000)2 b)(1111 1101 0010.0100)2	2				
19	017013493	1	Perform the arithmetic operation (+ 21)10 + (- 30)10 in binary using signed 2's complement representation and also check if overflow occurred or not.		2				
20	017013493	1	Represent (-7.5)10 in i)signed magnitude ii)1's compliment iii) 2's compliment	i)(1111.1000)2 ii)(1000.0111)2 iii)(1000.1000)2	2				
21	017013493	1	1.Compute (-0.75)10 + (0.0625)10 using standard fixed-point representation. Convert result into decimal fraction. 2.Convert (-2.625)10 into floating point representation having MSB bit as signed bit followed by 10 bits mantissa and 6 bits exponent part.		4				
22	017013493	1	What is the result of evaluating following 2 expression using 3 decimal digit floting point arithmetic with rounding a)(113.+-111.)+7.51 b)113.+(-111.+7.51)	a	1	9.51 and 10.0 respectively	10.0 and 9.51 respectively	9.51 and 9.51 respectively	10.0 and 10.0 respectively

23	017013493	1	If the decimal point is placed to the right of the first significant digit, then the number is called _____	b	1	Orthogonal	Normalized	Determinate	None of the mentioned
24	017013493	1	The floating-point representation 1 0000110 1000000 00000000 00000000 corresponds to	b	1	+32	-32	-16	+16
25	017013493	1	01101100000000100 given number in floating point having MSB sign bit followed by 10 bit mantissa and then 6 bits exponents. (options in decimal numbers)	a	1	(13.5)10	(12.5)10	(46.5)10	(3.75)10
26	017013493	1	Which of the following statement/s is/are incorrect? 1. A floating point number is said to be normalized if LSB of mantissa is non-zero. 2. An 8-bits binary numbers 10010001, 11101110 and 11101111 are different possible representations of (-17)10 3. 10's complement of a number is its 9's complement – 1 4. The 1's complement of a number can be obtained by adding each bit of the number with 1	d	1	1,2,4	2,3,4	1,2,3	1,3,4
27	017013493	1	The decimal number (-17)10 would be expressed in 8-bit signed 2's complement representation as -	d	1	11101110	10010001	11011111	11101111
28	017013493	1	Represent (46.5)10 as floating point binary no stored in 24 bit register having 16-bit fractional M and 8 bit Exponent.	0 0000 0110 1011101000000000	1				
29 IMP	017013493	1	Express the decimal number (-1/64) in floating point representation having MSB bit as sign bit followed by 8-bit mantissa and 6-bit exponent part.		2				
30	017013493	1	Express (-21.75)in Explicit form M=8,E=6,S=1	1 000101 10101110	1				
31 See	017013493	1	Assume no using 32 bit representation 1 for sign,15 for integer bits and 16 for fractional part for no (-43.625)10	(1000000000101011.101000000000000)2	2				
32	017013493	1	Represent no in to 32 bit ANSI IEEE format (-0.125)	1 1111110 10000...	2				
33	017013493	1	Convert -17 in standard floting point format.	1 0000101 1000100...	2				
34	017013493	1	Represent binary floting point no in to decimal formate in which 9 bits are for M .Which are followed by MSD bit which is sign bit and last 6 bits are E bits. 0110100000000011	(6.5)10	2				
35	017013493	1	Represent binary floting point no in to decimal formate in which 9 bits are for M .Which are followed by MSD bit which is sign bit and last 6 bits are E bits. 0101010000000010	(2.625)10	2				
36	017013493	1	Represent (263.3)10 in 32 bit floting point notation	0 .100000111*2^9 0 0001001 10000011101001100 0000000	2				
37	017013493	1	Express (5.875)10 in i)explicit and ii)Implicit form.	i)0 0011 10111 ii)0 0010 01111	2				
38	017013493	1	Express (-0.0625)10 in i)explicit and ii)Implicit form.		2				
39	017013493	1	Express (1259.125)10 in i)explicit and ii)Implicit form.	i)0 0001011 10011101011001000 0000000 ii) 0 0001010 00111010110010000 0000000	2				
40 See	017013493	1	x=0.0001101001101, represent x in implicit and explicit floating point number.		2				
41	017013493	1	Express (13)10 and (-17)10 in standard floating point byte format.		2				
42	017013493	1	What is the 16 bits pattern which represent (-13.5) in normalized signed magnitude fraction . S = 1 bit , Exponent = 7 bits , Mantissa = 8 bits . Represent it in hexadecimal also.	(84D8)16	2				
43	017013493	1	Express (-53.5)10 and (13)10 using 32-bit floating point format in which 1-bit sign bit,8-bit Exponent and 23-bit mantissa.		2				
44	017013493	1	The binary number is stored in 2's compliment form having 8 bit integer and 4 bit fractional part.Convert them in decimal fractional. i)0111 1111.1111 ii)1111 1111.1111 iii)0000 0111.0010	i)(127.9375)10 ii)(-0.0625)10 iii)(7.125)10	3				
45	017013493	1	Do as directed: (a) Express the decimal number (-1/32) in floating point representation having MSB bit as sign bit followed by 8 bit mantissa and 6 bit exponent part. (b) Perform the arithmetic operations (- 42) – (- 13) in binary using signed 2's complement representation and also check if overflow occurred or not.		3				
46	017013493	1	Perform arithmetic operation +70 and +80 give the status of overflow bit=_____	OV=1	1				
47	017013493	1	Perform arithmetic operation -70 and -80 give the status of overflow bit=_____	OV=1	1				
48	017013493	1	Perform arithmetic operation +70 and -80 give the status of overflow bit=_____	OV=0	1				
49	017013493	2	The operation executed on data stored in registers is called?	b	1	Data	Micro-operations	Transfer	Control
50	017013493	2	Which micro-operations carry information from one register to another:	a	1	Register transfer	Arithmetic	Logical	Program Control
51	017013493	2	Which are the operation that a computer performs on data that put in register ?	d	1	Register transfer	Arithmetic	Logical	All of mentioned

52	017013493	2	Which micro operations carry information from one register to another?	a	1	Register transfer	Arithmetic	Logical	All of mentioned
53	017013493	2	Micro operation is shown as:	b	1	R1->R2	R1<-R2	Both	None
54	017013493	2	In which shift is used to divide a signed number by two:	b	1	Logical right-shift	Arithmetic right shift	Logical left shift	Arithmetic left shift
55	017013493	2	The third state of Tri-state buffer mainly known as _____	a	1	High impedance	Low impedance	High capacitive	Low Resistance
56	017013493	2	A collection of lines that connects several devices is called_____	a	1	Bus	Wires	Buffer	Gates
57	017013493	2	RTL stands for	b	1	Random transfer language	Register transfer language	Arithmetic transfer language	Read Trasnfer Language
58	017013493	2	In which transfer the computer register are indicated in capital letters for depicting its function:	a	1	Register Transfer	Memory Transfer	Bus Transfer	None
59	017013493	2	Every bit of register has:	c	1	2 common line	4 common line	1 common line	8 common line
60	017013493	2	Represent the following conditional control statements by two register transfer statements with control function. If (P = 1) then (R1 <-- R2) else if (Q=1) then (R1 <-- R3)		3				
61	017013493	2	A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers. The number of multiplexers in the bus and size of multiplexers is respectively _____	c	1	32,32:1	16,16:1	32,16:1	16,32:1
62	017013493	2	A memory system of size 16 K bytes is required to be designed using memory chips which have 12 address lines with 4 data lines each. Then the number of such chips required to design the memory is _____.	d	1	2	16	11	8
63	017013493	2	In memory transfer location address is supplied by _____ that puts this on address bus:	b	1	ALU	CPU	MAR	MDR
64	017013493	2	Operation of memory transfer are:	c	1	Read	Write	Both	None
65	017013493	2	In memory read the operation puts memory address on to a register known as:	c	1	PC	ALU	MAR	All of these
66	017013493	2	By the help which operation we put memory address in memory address register and data in data register?	a	1	Memory Write	Memory Read	I/o Read	I/o Write
67	017013493	2	A digital computer has a common bus system for k registers of n bits each. The bus is constructed with multiplexers. The number of multiplexers in the bus and size of multiplexers is respectively	d	1	k, n:1	k, k:1	n, n:1	n, k:1
68	017013493	2	A digital computer has a common bus system for 16 registers of 32 bits each using multiplexers. The numbers of selection inputs in each multiplexer required to design is ____.	B	1	3	4	16	32
69	017013493	2	What will be the maximum number of addressable locations in memory using 13 address lines?	D	1	2048	1024	4096	8192
70	017013493	2	A memory system of size 128K bytes is required to be designed using memory chips which have logbase2(2048) address lines with 4 data lines each. Then the number of such chips required to design the memory is _____	c	1	64	32	128	16
71	017013493	2	If computer has 15 bit of address line then the memory unit has _____ memory location.	a	1	32768	32727	1024	24235
72	017013493	2	Design and explain a common bus system for four register each of 4 bit using multiplexer.		3				
73	017013493	2	A digital computer has a common bus system for 16 registers of 32 bits each: (i) How many selection input are there in each multiplexer? (ii) What size of multiplexers are needed? (iii) How many multiplexers are there in a bus?		3				
74	017013493	2	Construct of common bus system with three-state buffers using diagram.		3				
75	017013493	2	Design a common bus system using tristate buffer logic for 5 registers of 3 bit each.		3				
76	017013493	2	Register A holds the value 1010 & Register B holds the value 1100. What will be the output of selective-set operation?	c	1	1111	1000	1110	0 0 1 1
77	017013493	2	Register A holds the value 1010 & Register B holds the value 1100. What will be the output of selective-complement operation?	a	1	0 1 1 0	1110	1111	1000
78	017013493	2	Register A holds the value 1010 & Register B holds the value 1100. What will be the output of Selective-clear operation?	d	1	1000	1110	0 1 0 1	0 0 1 0
79	017013493	2	Register A holds the value 1010 & Register B holds the value 1100. What will be the output of Mask operation?	b	1	0 0 1 0	1000	0 1 0 1	1100
80	017013493	2	What will be the value of other logic operand for selective clear operation to be performed on 101001 such that its LSB bit only will be converted to 0?	d	1	101001	101000	100001	0 0 0 0 0 1
81	017013493	2	What will be the value of the other logic operand for the masking operation to be performed on the 1011 operand such that its MSB bit only will be converted to 0?	b	1	1100	0 1 1 1	0 0 1 1	1010
82	017013493	2	Which of the following shift operation is known as rotate operation?	b	1	Arithmetic	Circular	Logical	All of Mentioned
83	017013493	2	How many types of shift micro operation	d	1	2	3	4	6
84	017013493	2	Register A holds the value 1001 0110 & Register B holds the value 0001 1000, the output of selective-complement operation?	a	1	1000 1110	1001 0110	0001 1000	1000 0110
85	017013493	2	Register A holds the value 0101 & Register B holds the value 0011. What will be the output of Selective-clear operation?	d	1	1000	0101	0010	0100
86	017013493	2	The register A and B are 4 bit register. Register A holds 1101 and B holds 1110. What will be the output, if selective set operation is performed between A and B?	b	1	1100	1111	0011	1101
87	017013493	2	Register A holds the 8-bit binary number 11011001. After applying selective complement logic micro-operation, updated content of register A is 01101101, then what will be the value of logic operand B?	d	1	10100100	10110101	10110000	10110100
88	017013493	2	Let R1 and R2 be two 4-bit registers that store numbers in 2's complement form. For the operation R1+R2, which one of the following values of R1 and R2 gives an arithmetic overflow?	d	1	R1 = 1100 and R2 = 1010	R1 = 1101 and R2 = 1001	R1 = 1011 and R2 = 1110	both a and b
89	017013493	2	An 8-bit register contains the binary value 1100 1011. What is the register value after arithmetic shift right?	b	1	1100 1011	1110 0101	0110 0101	0100 1011

90	017013493	2	Which shift is a shift micro operation which is used to shift a signed binary number to the left or right:	a	1	Arithmetic	Circular	Logical	All of Mentioned
91	017013493	2	Arithmetic left shift is used to multiply a signed number by____	a	1	2	4	8	0
92	017013493	2	The ALS represents _____	a	1	Arithmetic Logic Shift Unit.	Auto Logic Shift Unit.	Arithmetic Logic Simple Unit.	Auto Logic Shift Unit.
93	017013493	2	4- Bit Binary Adder can be designed using ____ Full Adder	a	1	4	8	16	2
94	017013493	2	Which statement represent output X (in hex) for the given value Y= D7 (in hex)? X = ashr[shl(Y)]	d	1	X = X^Y	X = Y	X = complement(Y)	both a) & b)
95	017013493	2	Which statement represent output X (in hex) for given value Y= F8 (in hex) ? X = ashr[shl(Y)]	d	1	X = X^Y	X = Y	X = complement(Y)	both a) & b)
96	017013493	2	Which statement represent output X (in hex) for given value Y= E4(in hex)? X=ashr[shl(Y)]	d	1	X=X^Y	X=Y	X=complement(Y)	both a and b
97	017013493	2	Which statement represent output X (in hex) for given value Y = C1 (in hex)? X = ashr[shl(Y)]	c	1	X = X ^ Y	X = X ˅ Y	Both a and b	X = Y XOR X
98	017013493	2	A hexadecimal number FA is stored in 1-byte register R1. Calculate minimum number of times 'ashr' operation need to perform on R1 to set all the bits to 1.	c	1	5	4	3	6
99	017013493	2	A hexadecimal number 7A is stored in 1-byte register R1. Calculate minimum number of times 'ashr' operation need to perform on R1 to set all the bits to 1.	d	1	5	4	3	None
100	017013493	2	An 8-bit register contains the binary value 1011 1011, the register value after two arithmetic shift right?	d	1	0101 1101	1011 1011	1101 1101	1110 1110
101	017013493 nb	2	Design 4-Bit Combinational circuit Decrementer using four full-adder circuits.		2				
102	017013493 nb	2	Design a 4-bit arithmetic unit.		2				
103	017013493	2	Register A holds the 8-bit binary 11011001. Determine the B operand and the logic microoperation to be performed in order to change the value of A to: (i) 01111101 (ii) 11010000 (iii) 11111001		3				
104	017013493 nb	2	Design a digital circuit for 4-bit binary adder.		3				
105	017013493 nb	2	Design 4-Bit Binary Adder-Subtractor Circuit		3				
106	017013493 nb	2	Design 4-Bit Binary Incrementer Circuit		3				
107	017013493 nb	2	Design a simple arithmetic circuit which should implement the following operations: Assume A and B are 3 bit registers. Add : A+B, Add with Carry: A+B+1, Subtract: A+B'+1, Subtract with Borrow: A+B', Increment A: A+1, Decrement A: A-1, Transfer A: A		3				
108	017013493	2	Design a 3-bit binary circuit for following arithmetic operation:(Use logic gates and adder circuit only): Mode:0 – Subtract two operands with borrow, Mode:1 –_Add two operands		3				
109	017013493	2	Consider an I/O Register each of 5 bits for performing the following Operation. R1=10010 R2=00110 R3=11111 1) R7 = R2 ^ R3 2) R7 = R7 V R1 3) R8 = ASHR(R2) 4) R6 = R8 + CIL(R7) 5) R5 = CIR(R6) + R1 6) R9 = SHL (R5 V R6)		3				
110	017013493 nb	2	Design a shift unit which represents logic 0 for logical shift left and logic 1 is applied for logical shift right with its function table.		3				
111	017013493	2	An 8-bit registers contain the following binary values: A = 1101 0011 B = 0011 1010 C = 1010 0101 Perform the following micro-operations and obtain the content of 8-bit register F in hexadecimal value: D = A ^ B E = C ⊕ D F = ashl(A) V cil (E)		3				
112	017013493	2	Consider a 8- registers each of 5-bits for Performing following operations. R1 = 10010 R2 = 00110 R3 = 11111 i) R7 = (R2 ^ R3) ii) R9 = (R7 OR R1) iii) R8 = Ashr (R2) iv) R6 = R8 + (Cil R7) v) R5 = R6 ⊕ (R8 ^ R9) vi) Now How many Times Ashr Operations need to perform on R5 to Set all bits to 1 in R5.		3				
113	017013493	2	Design a 5 bit combinational shift unit having control input 0 : shift left & for control input 1 : shift right.		4				
114	017013493	2	An 8-bit register contains the binary value 10011100. What is the register content after arithmetic shift right? Starting from the initial value 10011100, determine the register content after an arithmetic shift left, and state whether there is an overflow.		4				
115	017013493 nb	2	Design 4-bit Arithmetic Circuit with its Function Table.		4				
116	017013493	2	Construct 4-bit combinational circuit shifter diagram		4				
117	017013493	2	Design an arithmetic circuit with one selection variable S and two n-bit data inputs A and B. The circuit generates the following four arithmetic operations in conjunction with the input carry Cin. Draw the logic diagram for the first two stages. S Cin = 0 Cin = 1 0 D= A+B (add) D= A+1 (increment) 1 D= A-1 (decrement) D= A+B'+1 (subtract)		4				
118	017013493	2	Design 4-Bit Arithmetic circuit using 4 * 1 multiplexer with selection line S1 and S0 where S1S0 = 00 for increment , S1S0= 11 for Subtraction , S1S0 = 01 for decrement and S1S0=10 for Addition.		4				

119	017013493	2	Design 4-Bit Arithmetic circuit using 4 * 1 multiplexer with selection line S1 and S0 where S1S0 = 00 for decrement, S1S0= 11 for increment, S1S0 = 01 for Addition and S1S0=10 for Subtraction		4				
120	017013493	3	Which cycle refers to the time period during which one instruction is fetched and executed by the CPU ?	b	1	fetch cycle	instruction cycle	decode cycle	execute cycle
121	017013493	3	How many stages of instruction cycle ?	c	1	5	6	4	7
122	017013493	3	CPU has built-in ability to execute a particular set of machine instructions, called as _____	a	1	a) Instruction Set	b) Registers	c) Sequence Set	d) User instructions
123	017013493	3	Which of the following is group of bits that instruct the computer to perform a specific operation ?	d	1	address	memory	program counter	instruction code
124	017013493	3	Which of the following register holds the address of instruction ?	b	1	DR	PC	IR	AC
125	017013493	3	Which register holds memory operand ?	a	1	DR	AR	AC	IR
126	017013493	3	Which register holds address of memory ?	b	1	DR	AR	PC	TR
127	017013493	3	Which register holds instruction code ?	c	1	DR	AR	IR	PC
128	017013493	3	_____ Register is also known as Processor register?	c	1	IR	TR	AC	PC
129	017013493	3	Which of the following registers have only a LD control input in common bus system?	a	1	IR and OUTR	INPR and OUTR	IR and INPR	AR and OUTR
130	017013493	3	Which of the following register has 12 bits 1. DR 2. AR 3. AC 4. PC 5. TR 6. IR 7. INPR 8. OUTR	b	1	A) 1 & 2	B) 2&4	C) 3 & 5	D) 7 & 8
131	017013493	3	The basic computer has 16-bit common bus system in which 16 bits output of register A are placed on bus lines when S2S1S0 = 100. The LD pin of 16-bit register B is enabled to load the data available on bus. The output of register B is selected for the bus line when S2S1S0 = 110. Identify the correct transfer micro-operation based on the given description.	c	1	AC ←DR	DR ←IR	TR ←AC	DR ←PC
132	017013493	3	Which of following pair match correct ? 1. 2^n micro operations p. 16 bits 2. PC q. E=0 3. CLE r. 12 Bits 4. CMA s. n bits opcode 5. AC t. 2n bit op code 6. DR u. complement processor register	c	1	(1,s), (2,r), (3,r), (4,q) , (5,p), (6,p)	(1,t), (2,r), (3,r), (4,q) , (5,p), (6,p)	(1,s), (2,r), (3,q), (4,u) , (5,p), (6,p)	(1,t), (2,r), (3,r), (4,u) , (5,p), (6,p)
133	017013493	3	Which of the following pair match correct? 1. $D_7 = 1, I = 1$ — p. Non-MRI 2. Hex code: 7100 — q. A252 3. STA — r. F020 4. INPR — s. 3 nibbles 5. 15th bit of instruction code = 0, $D_7 = 0$ — t. M[AR] ← AC 6. Indirect LDA — u. 1 byte register v. CME w. Direct MRI	C	1	(1,u), (2,v), (3,p), (4, r), (5, s), (6,q)	(1,r), (2,s), (3,t), (4, p), (5, q), (6,u)	(1,r), (2,v), (3,t), (4, u), (5, w), (6,q)	(1,q), (2,v), (3,t), (4, p), (5, r), (6,w)
134	017013494	3	Which of the following pair match correct? 1. 2^n microoperations p. 16 bits 2. PC q. AC = 0 3. CLA r. 12 bits 4. CMA s. n bit opcode 5. AC t. 2n bit opcode 6. TR u. complement processor register	c	1	(1,s), (2,r), (3,r), (4,q) , (5,p), (6,p)	(1,t), (2,r), (3,r), (4,q) , (5,p), (6,p)	(1,s), (2,r), (3,q), (4,u) , (5,p), (6,p)	(1,t), (2,r), (3,r), (4,u) , (5,p), (6,p)
135	017013493	3	Which of the following is used to stores address of memory from which data is collected & sent to CPU ?	c	1	program counter	cache memory	memory address register	memory data register
136	017013493	3	The register which keeps tracks of execution of program & which contains the memory address of instruction currently being executed is called _____.	c	1	index register	memory address register	program counter	instruction register
137	017013493	3	program counter contents indicates ____.	c	1	the time elapsed since execution begins	the count of programs being executed after switching the power ON	the adress where next instruction is stored	the time needed to execute a program
138	017013493	3	what will be the contents of processor register and extended bit after execution of following instruction code if the initial content of AC is F000 and memory locations [300] are 567 and [567] are 200 respectively ? 1 AND 300 0 ADD 567 CME	a	1	200,1	F200,1	200,0	FDFF, 1
139	017013493	3	Which of the following represent the size of processor register and hex code for a register reference instruction ?	b	1	16 , F080	16, 7080	8, F080	8, 7080
140	017013493	3	What will be the content of processor register and Extended bit after execution of following sequence of instructions if the initial content of AC is 089F and Extended bit is 0 and memory locations [312] are 544 and [544] are 600 respectively? 1 ADD 312 0 AND 544 CME CMA	a	1	F9FF, 1	0E9F, 0	0600, 0	F9FF , 0
141	017013493	3	What will be the content of processor register and Extended bit after execution of following sequence of instructions if the initial content of AC is F097 (in hex) and Extended bit is 0 and memory locations [300] are 510 and [510] are 600 respectively? 1 AND 300 0 ADD 510 CME CLA	C	1	0600, 1	0000, 0	0000, 1	F097, 0
142	017013493	3	The register reference instruction having hex code 7100 is _____	a	1	CME	CMA	INC	SPA
143	017013493	3	What will be content of processor register & extended bit (E) after execution of following instruction code if initial content of AC is ABCD & memory location [300] are 567 & [567] are 200 respectively ? 1 AND 300 0 ADD 567 CMA CME	c	1	a) 0400,0	b) 0400,1	c) FBFF,1	d)0200,0

144	017013493	3	The timing signal of Register reference instruction and Input-Output instruction are _____ and _____.	d	1	D7'I'T3 and D7IT3'	D7I'T3 and D7'I'T3	D7'I'T3 and D7IT3	D7I'T3 and D7IT3
145	017013493	3	What will be the contents of processor register and extended bit after execution of following instruction code if the initial content of AC is F000 and memory locations [300] are 567 and [567] are 200 respectively? 1 AND 300 0 ADD 567 CMA	a	1	FDFF, 0	FDFF, 1	F200,1	F200,0
146	017013493	3	Register A holds the 8-bit binary 11011001. Determine the B operand and the logic microoperation to be performed in order to change the value of A to 11111001.	d	1	00100000 , OR	00100000, AND	00100000, XOR	BOTH A) AND C)
147	017013493	3	Which of the following pair match correct? 1. $D_7 = 1, I = 0$ — p. Input-output Instruction 2. AR — q. EXXX 3. AC — r. 7080 4. INPR — s. 3 nibbles 5. 15th bit of instruction code = 1, $D_7 = 1$ — t. Processor Register 6. Indirect ISZ — u. 1 byte v. 12 bytes w. 6XXX	c	1	(1,u), (2,v), (3,p), (4, r), (5, s), (6,q)	(1,r), (2,s), (3,t), (4, p), (5, q), (6,u)	(1,r), (2,s), (3,t), (4, u), (5, p), (6,q)	(1,q), (2,v), (3,t), (4, p), (5, r), (6,w)
148	017013493	3	Which of the following stores operand during execution and result of operation after execution ?	d	1	general purpose register	stack register	flag register	accumulator
149	017013493	3	D2T4: DR← M [AR] D2T5: AC← DR , SC ← 0 this indicate which computer instructions ?	a	1	LDA	STA	ADD	AND
150	017013493	3	An addressing of memory having 16-bit format, out of this its 15th bit is 0 , 14th 13th & 12th bit is having 0, 1, 1 value respectively & rest of the bits value is unknown then find what type of address, which memory reference instruction with its hexcode notation.	b	1	a) Indirect, BUN, CXXX	b) direct , STA, 3XXX	c) Indirect, BSA, DXXX	d) Indirect, ISZ, EXXX
151	017013493	3	Identify the computer instruction, This instruction stores the content of AC into the memory word specified by the effective address. Since the output of AC is applied to the bus and the data input of memory is connected to the bus, we can execute this instruction with one microoperation:	b	1	LDA	STA	ADD	BUN
152	017013493	3	An addressing of memory having 16-bit format, out of this its 15th bit is 0, 14th 13th & 12th bit is having 0 1 0 value respectively & rest of the bits value is unkonwn then find what type of address, which memory referance instruction with its HEXCODE notation	a	1	direct, LDA, 2XXX	Indirect, AND, 8XXX	indirect, ADD, 9XXX	direct, ADD, 1XXX
153	017013493	3	An addressing of memory having 16-bit format, out of this its 15th bit is 1, 14th 13th & 12th bit is having 0 1 1 value respectively & rest of the bits value is unkonwn then find what type of address, which memory referance instruction with its HEXCODE notation	b	1	INDIRECT, BUN, CXXX	INDIRECT, STA, BXXX	INDIRECT, BSA, DXXX	INDIRECT, ISZ, EXXX
154	017013493	3	Which register referance instruction is used for skip next instruction if Accumulator is positive	a	1	SPA	STA	SNA	SZE
155	017013493	3	The register referance instruction having hex code of 7004 is.....	c	1	SZE	SPA	SZA	SNA
156	017013493	3	MAtch the followings HEX code / symbol — Description / hex code 1) CLA — p) 7800 2) HLT — q) 7040 3) SZE — r) 7200 4) SNA — s) 7002 5) CME — t) 7010 u) 7008 v) 7004 w) 7100 x) 7001	a	1	1- P, 2- X, 3- S, 4 -U, 5 - W	1- Q, 2- S, 3- X, 4 -P, 5 -T	1- R, 2- T, 3- V, 4 -W, 5 - X	1- T, 2- U, 3- V, 4 -W, 5 - X
157	017013493	3	Which of the following represents the size of the input-output register and hex code for an I/O instruction?	d	1	a) 16, F080	b) 8, 70FF	c) 8, 7080	d) 8, F080
158	017013493	3	Choose one of the correct 16-bit instruction format for the instruction: 1 STA 256	d	1	0010 001001010110	1001 001001010110	0011 001001010110	1011 0010 0101 0110
159	017013493	3	Write basic single address instruction code to evaluate the following arithmetic statement Y = (A* B) + (C+ D) + 1 . Explain execution of given statement using 16-bit common bus system for basic computer system. Draw timing diagram for loading processor register with content present at M[A].		5				
160	017013493	3	Write basic single address instruction code to evaluate the following arithmetic statement Y = (A+C+D)+1 . Explain execution of given statement using 16-bit common bus system for basic computer system. Draw timing diagram for ADDING processor register with content present at M[C].		5				
161	017013493	3	Consider the instruction formats of the basic computer, for each of the following 16-bit instruction, gives the equivalent four digit hexa decimal code and explain in your own words what it is that the instruction is going to perform. A) 0001 0000 0010 0100 B) 1011 0001 0010 0100 C) 0111 0000 0010 0000		4				
162	017013493	3	Draw the timing diagram of following instruction : D3T4 : SC <-- 0		3				
163	017013493	3	Consider content of instruction register of the basic computer, for each of the following 16-bit instruction, Calculate the equivalent four digit hexa decimal code, type of instruction format, opcode, I bit and identify related instruction. i) 0001 0000 0011 1100 ii) 1010 0001 0010 0111 ii) 0111 0000 0000 1000		3				
164	017013493	3	Write basic single address instruction code to evaluate the following arithmetic statement X = (P + Q) + [(R * S)+1]. Explain execution of given statement using 16-bit common bus system for basic computer system. Draw timing diagram for loading processor register with content present at M[P]		5				
165	017013493	3	Consider the instruction formats of the basic computer, for each of the following 16-bit instruction, gives the equivalent four-digit hexadecimal code and explain in your own words what it is that the instruction is going to perform.A) 1011 0001 0010 0100 B) 0111 0000 0010 0000		2				

166	017013493	3	Write basic single address instruction code to evaluate the following arithmetic statement Z = (A* C) + (B * D) + 1 . Explain execution of given statement using 16-bit common bus system for basic computer system where A, B, C, D are memory locations and Y is output register.		4				
167	017013493	3	Draw timing diagram for the instruction in which data is stored from accumulator to memory.		3				
168	017013493	3	Write basic single address instruction code to evaluate the following arithmetic statement: Y = (A + B) * (C + D) Explain execution of given statement using 16-bit common bus system for basic computer system. Draw timing diagram for loading processor register with content present at M[A].		5				
169	017013493	3	Write basic single address instruction code to evaluate the following arithmetic statement Y = (A*B)*(C+D) . Explain execution of given statement using 16-bit common bus system for basic computer system. Draw timing diagram for ADDING processor register with content present at M[C].		5				
170	017013493	3	An addressing of memory having 16-bit format, out of this its 15th bit is 1, 12th 13th & 14th bit is having 0 1 0 value respectively & rest of the bits value is unknown then find what type of address, which memory reference instruction with its HEXCODE notation.	c	1	direct, LDA, 9XXX	direct, ADD, 1XXX	Indirect, LDA, AXXX	Indirect, STA, AXXX
171	017013493	4	Which of the following instruction is used to skip next instruction if (A-B) < 0 ?	a	1	SNA	SPA	SZE	SZA
172	017013493	4	Which of the following instruction is used to skip next instruction if (A-B) > 0 ?	b	1	SNA	SPA	SZE	SZA
173	017013493	4	Which of the following instruction is used to skip next instruction if (A-B) = 0 ?	d	1	SNA	SPA	SZE	SZA
174	017013493	4	Which of the following machine instructions are used by the computer to represent the negative number in signed 2's complement form?	d	1	CMA	CLA	INC	Both a) and c)
175	017013493	4	Which of the following machine instructions are used by the computer to represent the number in signed 1's complement form?	a	1	a)CMA	b)CLA	c)INC	d)ADD
176	017013493	4	Identify the instruction based on the given micro-operation: If (AC(15)=1) then PC ← PC + 1 i.e. start with 1 i.e. it is negative	a	1	SNA	SZA	SPA	SKI
177	017013493	4	What are the control bits for CMA instruction ?		2				
178	017013493	4	What are the control bits for SZA instruction ?		2				
179	017013493	4	What are the control bits for HLT instruction ?		2				
180	017013493	4	What are the control bits for CIL instruction ?		2				
181	017013493	4	Explain execution time for following instruction with example : a) BSA b) SNA.		3				
182	017013493	4	Explain execution time for following instruction with example: a) ISZ b) SPA c) SKO		4				
183	017013493	4	Explain execution time for following instruction with example: a) ISZ b) SZA c) SKI		4				
184	017013493	4	Explain following instructions with timing states and control signals a) BSA b) CIR		5				
185	017013493	4	Explain execution time for following instruction: a) BSA b) CMA		2				
186	017013493 see	4	What can be interpreted about instruction type if 15th bit (I) of instruction format is 1?	both b & d	1	direct address memory instruction	indirect address memory instruction	register reference instruction	I/O reference instruction
187	017013493 see	4	What can be interpreted about instruction type if 15th bit (I) of instruction format is 0?	both a & c	1	direct address memory instruction	indirect address memory instruction	register reference instruction	I/O reference instruction
188	017013495	4	The ___ Instruction checks the input flag to see if character is available to transfer.	a	1	SKI	SKO	ION	IOF
189	017013493	4	What can be interpreted about the instruction type if the control statement is D7IT3 ?	d	1	direct address memory instruction	indirect address memory instruction	register reference instruction	I/O reference instruction
190	017013493	4	What can be interpreted about instruction type if control statement is D7'I'T3?	a	1	direct address memory instruction	indirect address memory instruction	register reference instruction	I/O reference instruction
191	017013493	4	What can be interpreted about instruction type if control statement is D7I'T3?	c	1	direct address memory instruction	indirect address memory instruction	register reference instruction	I/O reference instruction
192	017013493	4	Consider the following table in which all the numbers are in HEX and the final content of AC is (4B4B)16 before the HLT instruction is executed. Find out the missing instruction at location 025 to get AC = (4B4B)16. Location Instruction 021 CLA 022 ADD 027 023 CLE 024 CIL 025 ? 026 HLT 027 A5A5 AC - 0 AC - A5A5 E - 0 0 1010 0101 1010 0101 = 1 0100 1011 0100 1010 = 4B4A INC = 4B4B	b	1	CIL	INC	SNZ	SNA
193	017013493	4	What will be the contents of processor register after execution of following code? Location Instruction 200 CLA 201 AND 208 202 BUN 204 203 HLT 204 INC 205 CMA 206 BUN 203 207 8184 208 ABCD 0000 0000 0000 0000 0000 0000 0000 0000 --- finish 0000 0000 0000 0001 1111 1111 1111 1110 = FFFE	a	1	FFFE	FFFF	ABCD	1

194	017013493	4	What will be the contents of processor register after execution of following code? Location Instruction 051 LDA 058 052 AND 057 053 BUN 055 054 HLT 055 CMA 056 BUN 054 057 ED19 058 12E4 0001 0010 1110 0100 ^1110 1101 0001 1001 = 0000 ---- finish 1111 = FFFF,0 ----	a	1	FFFF,0	FFF0,1	FFFF,1	0000,0
195	017013493	4	Initially the content of PC is 022, and AC = A937. An address part is equal to 073. Memory word 073 contains the operand B8F2. Find out the contents of PC, AR, DR, AC and IR when an ISZ instruction is executed. (All numbers are in hexadecimal).		2				
196	017013493	4	State timing state for execution of BSA instruction.		3				
197	017013493	4	State timing state for execution of ISZ instruction.		3				
198	017013493	4	State timing state for execution of BUN instruction.		3				
199	017013493	4	State timing state for execution of ADD instruction.		3				
200	017013493	4	State timing state for execution of AND instruction.		3				
201	017013493	4	State timing state for execution of LDA instruction.		3				
202	017013493	4	State timing state for execution of STA instruction.		3				
203	017013493	4	Explain execution time for following instruction: a)BSA b) ISZ		2				
204	017013493	4	What will be status of FGI flag bit if input device is ready to send data to accumulator?	a	1	1	0	x	z
205	017013493	4	What will be status of FGO flag bit if output device is ready to accept data from accumulator?	b	1	0	1	x	z
206	017013493	4	If R is interrupt flip flop then what is the register transfer statement of RT2 from instruction cycle ?	c	1	a) AR <-- 0, TR <-- PC	b) M[AR <-- TR, PC <-- 0	c) PC <-- PC +1, IEN <-- 0, R <-- 0, SC <-- 0	d) both a & c
207	017013493 See	4	Which instruction is a hardware implementation of the interrupt cycle?	b	1	SKI	BSA	STA	OUTR
208	017013493	4	Which of the following control bit is used for checking occurrence of interrupt?	a	1	IEN	ION	INT	SKI
209	017013493	4	State setting condition of R flipflop in interrupt cycle. T0'T1'T2'.IEN(FGI+FGO)		2				
210	017013494	4	Explain effect of before and after interrupt execution with an example.		4				
211	017013493	4	Draw interrupt cycle		3				
212	017013493	4	The first machine cycle of an instruction is always __	a	1	instruction fetch	decode	read effective address	execute
213	017013493	4	The IEN flip flop can be set using _____ instruction and can be cleared using _____ instruction.	d	1	ION, IOFF	IOF, ION	FGI, FGO	ION, IOF
214	017013493	4	Which of following pair match correct? 1. 5 9 2 4 + - * p. 6 2. ISZ q. D5T5 3. BSA r. D6T6 4. CMA s. 15 5. postfix t. reverse polish 6. SP bit size u. rB9	d	1	(1,p), (2,r), (3,t), (4,q), (5,s), (6,s)	(1,s), (2,r), (3,q), (4,u), (5,p), (6,r)	(1,t), (2,r), (3,q), (4,q), (5,p), (6,p)	(1,s), (2,r), (3,q), (4,u), (5,t), (6,p)
215	017013494	4	Find out the symbolic Description that belongs to BSA Instruction	b	1	a)PC ← AR	b)M[AR] ← PC,PC ← AR+1	c)M[AR] ← M[AR]+1,IF M[AR]+1=0 then PC ← PC+1	d)AC ← M[AR]
216	017013495	4	Identify the instruction based on the given micro-operation: AC← M[AR]	a	1	a)LDA	b)CIR	c)SPA	d)SNA
217	017013493	4	What will be the contents of processor register after execution of following code? Location Instruction 010 CLA 011 ADD 016 012 BUN 014 013 HLT 014 AND 017 015 BUN 013 016 C1A5 017 93C5 0000 0000 0000 0000 1100 0001 1010 0101 ---- finish 1001 0011 1101 0101 = 1000 0001 1000 0101 = 8185 ------	b	1	8184	8185	C1A5	93C5
218	017013493	4	What will be the contents of processor register after execution of following code? LocationInstruction 010 CLA 011 AND 016 012 BUN 014 013 HLT 014 CMA 015 BUN 013 016 C1A5 017 93C5 0000 0000 ---- finish 1111 = FFFF ----	c	1	8184	8185	FFFF	93C6
219	017013493	4	What will be the contents of processor register after execution of following code? Location Instruction 010 CLA 011 AND 016 012 BUN 014 013 HLT 014 ADD 017 015 BUN 013 016 C1A5 017 93C5 0000 0000 ---- finish 93C5 ----	d	1	8184	8185	C1A5	93C5
220	017013493	4	Identify Correct sequence of Program to perform logical OR Operation from given sequence. P) CMA Q) ORG 100 R) STA TMP S) LDA B T) AND TMP U) LDA A V) HLT W) BUN TMP X) ADD TMP Q-U-P-R-S-P-T-P-V	a	1	Q,U,P,R,S,P,T,P,V	Q,U,P,R,S,P,T,V	Q,U,P,R,S,T,P,V	Q,U,P,R,S,P,T,V
221	017013493	4	If (AC(15)=0 then (PC ← PC+1) belongs to which instruction.	c	1	SNA	SZA	SPA	SKI

222	017013493	4	Which of the following instruction is used for enabling interrupt?	b	1	IEN	ION	IOF	SKI
223	017013493	4	Which of the following instruction is used for disabling interrupt?	c	1	IEN	ION	IOF	SKI
224	017013493	4	The following instruction when executed, E and AC results to _____ operation. CLE SPA CME CIR	c	1	Circular Right	Logical shift right	Arithmetic Shift Right	Circular Left
225	017013493	4	Identify the computer instruction which having following micro operation is D6T4: DR <-- M [AR] D6T5: DR <-- DR + 1 D6T6: M [AR] <-- DR, if (DR = 0) then (PC ← PC + 1), SC ← 0	c	1	BUN	SKI	ISZ	SPA
226	017013493	4	What will be the content of processor register AC & E after execution of following code (assume initial E & AC is clear) Location Instruction 210 CLA 211 ADD 217 212 INC 213 STA 217 214 LDA 218 215 CME 216 AND 217 217 2324 218 8EC4 0000 0000 0000 0000 0010 0011 0010 0100 0010 0011 0010 0101 STA in 217 1000 1110 1100 0100 E=1 ^0010 0011 0010 0101 = 0000 0010 0000 0100 = 0204	b	1	a)0204, 0	b)0204, 1	c)0202, 0	d)0215, 1
227	017013493	4	What are the two instruction needed in basic computer in order to set E flip flop is 1 ?	d	1	a) CLA, CME	b) CME	c) CLE, CMA	d)CLE, CME
228	017013493	4	Initially E=0, AC = 9000, M[0020] = A2C4 , PC = 0404 After Execution of following two line content of PC ? ADD 0020 SZE 1001 0000 0000 0000 1010 0010 1100 0100 = 1 0011 0010 1100 0100 = 32C4	d	1	a) 405	b) 404	c) 403	d) 406
229	017013493	4	The following program is stored in memory unit of the basic computer. What is the content of the accumulator after the execution of program? (all location number listed below are in hexadecimal). Location Instruction 210 CLA 211 ADD 217 212 INC 213 STA 217 214 LDA 218 215 CMA 216 AND 217 217 1234H 218 9CE2 0000 0000 0000 0000 0001 0010 0011 0100 0001 0010 0011 0101 STA in 217 1001 1100 1110 0010 0110 0011 0001 1101 ^0001 0010 0011 0101 = 0000 0010 0001 0101	d	1	1002	2100	2011	0215
230	017013493	4	Choose the correct statement/s regarding Input-output instructions: (1) I/O instructions are needed for transferring information to and from AC register. (2) I/O instructions are needed for checking the flag bits. (3) I/O instructions are needed for controlling the interrupt facility. (4) I/O instructions are recognized by computer when control function is D7'I'T3	d	1	Only 1 and 4	Only 2 and 3	Only 1 and 2	Only 1,2 and 3
231	017013493	4	1. Explain the following instruction with an example: i) SNA ii) BSA iii) CIL 2. State condition for an interrupt to occur and also state its register transfer statement after interrupt occurs.		5				
232	017013493	4	The number of non-MRI instructions in basic computer are _____.	b	1	6	18	7	10
233	017013493	4	Explain execution time for following instruction: a) BUN b) CMA		2				
234	017013493	5	The program that translates a assembly language into machine language is called ____	b	1	Compiler	Assembler	Translator	Coder
235	017013493	5	The program that translates a high level language language into machine language is called ____	a	1	Compiler	Assembler	Translator	Coder
236	017013493	5	The program that converts a high-level language program to binary is called _____.	c	1	a)Translator e	b)Complementer	c)Compiler	d)Assembler
237	017013493	5	Which of the following is not a pseudoinstructions?	c	1	ORG	DEC	HLT	HEX
238	017013493	5	Which of the following is a pseudo instruction?	d	1	ORG	END	INC	both 1 and 2
239	017013493	5	Match the following. 1) INC p) pB8 2) SNA q) 01110 3) SKO r) rB5 4) COMA s) rB9 5) SHLA t) 10000 u) rB3 v) 11000	b	1	1-q, 2-r, 3-t, 4-v, 5-s	1-r, 2-u, 3-p, 4-q, 5-v	1-v, 2-u, 3-p, 4-r, 5-t	1-p, 2-v, 3-t, 4-u ,5-q
240	017013493	5	Identify the correct statement/s: 1. The value of the program counter is incremented by 1 once its value has been read to the memory address register. 2. Machine instructions are not translated during second pass of assembler. 3. A label symbol contains maximum three characters and is terminated by comma. 4. To perform logic operations, CMA and AND both are useful machine instructions.	a	1	Only 1, 3, 4	Only 2,3,4	Only 1, 2, 4	Only 1, 2, 3
241	017013493	5	In which of the following cases, the assembler prints an error message to inform the programmer that his symbolic program has an error at a specific line of code? Case - 1: Invalid machine code symbol is detected. Case - 2: The symbolic code which is not a pseudo instruction and absent in MRI and non-MRI table is detected. Case - 3: Program has such a symbolic code, for which assembler does not know its binary equivalent value. Case - 4: Error message is printed if the program has a label, which is found in address symbol table.	b	1	Case 1, 3, 4	Case 1, 2, 3	Case 1, 2, 4	Case 2, 3, 4
242	017013493	5	Identify an invalid line of code:	b	1	PLA, ADD Y I	P_L, AND 058	PAL, LDA SB	Both B and C
243	017013493	5	Which are the fields in assembly language?	Label, Instruction, Comment	1				

244	017013493	5	A ____ is defined as an instruction that does not have an address part.	c	1	MRI	Pseudoinstruction	Non-MRI	None of these
245	017013493	5	_____ Instructions are translated during second pass by means of table look up procedures	b	1	High level program	Machine	MRI	None of these
246	017013493	5	Which is /are not correct statements for Pass-1 Assembler from the following. a) it define symbols and remember them in symbol table b) it does actual assembly by translating operations in to machine codes c) Process pseudo- instructions d) Generate object code and data for literals and look for values of symbols e) Keep track of location Counter(LC)	b	1	both (a) and (d)	both (b) and (d)	both (b) and (c)	Only a
247	017013493	5	Which of the following is true for symbolic address? 1. It consists of one, two, or three but not more than three alphanumeric characters. 2. It is terminated with comma in the label field. 3. The first letter must be a letter and next two may be letters or numerals.	a	1	all	only 1	only 2	only 3
248	017013493	5	The symbols ORG, DEC, and END called_____ and it gives command to _____	a	1	pseudo instruction, Assembler	Pseudo instruction, CPU	Machine instruction, Assembler	Machine instruction, CPU
249	017013493	5	Which of the following statements is/are correct? 1. Second pass assembler is followed by first pass assembler to convert binary equivalent of all instructions. 2. First pass assembler do not generate error in line code if instruction is invalid. 3. Pseudo instructions are translated by first pass assembler.	d	1	only 1	only 2	only 3	all
250	017013493	5	Which of the following is true for second pass assembler?. 1.Machine instructions are translated by means of table lookup procedures. 2. Error in line of code cannot be detected. 3. It generates address symbol table for all user defined symbols with equivalent binary value. 4. All the MRI and Non-MRI instructions are decoded with their binary equivalent value.	c	1	BOTH 1) AND 2)	BOTH 2) AND 3)	BOTH 1) AND 4)	All are true
251	017013493	5	Which one of following in invalid pseudo instruction ?	b	1	ORG	HLT	DEC	END
252	017013493	5	Which operation will be performed by following instructions sequence CLE CIR	a	1	logical right shifting of accumulator	logical left shifting of accumulator	circular left shifting of accumulato	circular right shifting of accumulator
253	017013493	5	The content of accumulator after execution of following program is .. ORG 100 LDA X CMA INC ADD X HLT 2s complement of x then add x = -x+x = 0	d	1	a) X	b) 2X	c) 1	d) 0
254	017013493	5	What is the content of the accumulator after the execution of program? LocationInstruction 508 CLA 509 CMA 50A AND 52F 50B STA 52F 50C LDA 53F 50D CMA 50E CMA 50F AND 52F 51F HLT 52F 1234H 53F 9CE2 0000 1111 1234 1234 9CE2 = 1001 1100 1110 0010 0110 0011 0001 1101 1001 1100 1110 0010 ^ 0001 0010 0011 0100 = 0001 0000 0010 0000 = 1020	a	1	1020	2020	FFFF	F1FF
255	017013493	5	To implement logical NOR operation using assembly level program, how many times CMA instruction is used?	c	1	4	5	2	3
256	017013493	5	A set of common instructions that can be used in program many times is called____	c	1	CALL	JUMP	Subroutine	Loop
257	017013493	5	Which of Following instruction used to link between main program and a subroutine?	a & b both	1	BUN	BSA	SKI	SKO
258	017013493	5	In Register Stack, the PUSH instruction is used to ____ the current stack pointer and____ data to the stack. The POP instruction is used to ____the data from the stack and ____ the current stack pointer	b	1	increment,read,store,decrement	increment,write,read,decrement	decrement,write,read,increment	decrement,read,write,increment
259	017013493	5	Specify the control word that must be applied to processor to implement the following microoperations. R6 <-- R4 XOR R5	a	1	10010111001100	11010010111000	11010010110000	10010111010000
260	017013493	5	Find Out the RPN of following expression: [(P * Q) + (M * N)] - (X * Y) PQ* MN* + XY*-	a	1	P Q * M N * + X Y * -	) P Q + * M N *X Y * -	P Q M * + N *X * - Y	P Q + M N * - X Y * *
261	017013493	5	Control word for operation R7<-- R1+R2 00101011100010	a	1	101011100010'	00101010100010'	00101011100110'	00101011100111'
262	017013494	5	What will be answer for 53*23*41*++ 15+6+4 = 25	b	1	5	25	10	40
263	017013493	5	If control word for micro operation is 01011011100101 R7 <-- R2 - R6	d	1	R7--> R3-R6	R7-->R2-R5	R7--> R1-R6	none of above
264	017013493 IMP	5	Which of the following represent the top of the stack value of k bit stack register ?	d	1	2k	logk base 2	2^k	(2^k) - 1
265	017013493	5	The result evaluating the postfix expression 10 5 + 60 6 / * 8 – is____.	b	1	284	142	182	130
266	017013493	5	Which of the following microoperation is true for the given control word: 11100011100110?	d	1	R7--> R7 ⊕ R7	R7 -->R7 ^ Input	R7--> Input v R7	R7 --> R7 -1
267	017013493	5	Which instruction is used to stored data on stack?	d	1	LDA	STA	POP	PUSH
268	017013493	5	What is the content of Stack Pointer in memory stack?	b	1	address of next instruction	address of top element of stack	address of current instruction	address of origin
269	017013493	5	Evaluate & write result of for following reverse polish expression abc*+de*f+g*+ where a=1, b=2, c=3, d=4, e=5, f=6, g=2	b	1	a) 61	b) 59	c) 49	d) 56

270	017013494	5	In memory stack, PUSH instruction is used to_____ the current stack pointer & _____ data to stack, the POP instruction is used to ____ the data from stack & _____ current stack pointer.	d	1	a) increment, read, store, decrement	b) decrement, read, store, increment	c) increment, store, read, decrement	d) decrement, store, read, increment
271	017013493	5	Result of evaluating RPN expression 5 4 6 + * 4 9 3 / + * is ....?	b	1	a) 600	b) 350	c) 650	d) 588
272	017013493	5	What is the control word for micro operation R4 <-- R4 V R5	b	1	a)01001100100101	b)10010110001010	c)10110010101010	d)10010110001011
273	017013493	5	In memory stack, the initial value of SP is 4000. When new item is inserted using ____ operation the value of SP is _____	a	1	PUSH, 3999	POP, 4000	PUSH 4002	POP, 4001
274	017013493	5	What will be the control word to implement the micro-operation: R5 ← R4 ^ R3 ?	d	1	10001110101010'	10001110101100'	111001010100'	10001110101000
275	017013493	5	Write a program to evaluate the arithmetic statement: A*B+C*D+E i. Using an accumulator type computer. ii. Using a stack organized computer.		5	QUESTION - 276 ORG100 LDA SUM LOP, ADD X I STA SUM ISZ X ISZ CTR BUN LOP HLT X, HEX 100 SUM , HEX 0 CTR, DEC -9 END	QUESTION - 277 ORG 100 LDA AL ADD BL STA CL CLA CIL ADD AH ADD BH STA CH HLT AH, DEC 10 BH .... END		
276	017013493	5	Write ALP for addition of 10 numbers		5				
277	017013493	5	Write assembly language program to add two double precision numbers.		5				
278	017013493	5	The following program is store d in the memory unit of basic computer. Show the contents of AC, PC, IR at the end after execution of each instruction.All numbers listed below in hex. Location Instruction 010 CLA 011 ADD 016 012 BUN 014 013 HLT 014 AND 017 015 BUN 013 016 C1A5 017 93C6 0000 0000 0000 0000 PC-011 1100 0001 1010 0101 PC-012 ---------- PC-014 FINISH PC-014 IR-7001 AC-8184 ----------> ANS ^1001 0011 1100 0110 == 1000 0001 1000 0100 PC-015 ---------- PC-013		3				
279	017013493	5	The following program is alist of instructions in hex code. The computer executes the instructions starting from address 100. What are the content of AC and the memory word at address 103 when computer halts? Location Instruction 100 5103 101 7200 102 7001 103 0000 104 7800 105 7020 106 C103 BSA 103 ----------1 CMA ----------6 HLT ----------7 RETURN ADDERESS 101 ----------2 CLA 0000 0000 0000 0000 ----------3 INC 0000 0000 0000 0001----------4 BUN 103 I ----------5		3	QUESTION-280 ORG 100 LDA SUM ADD A ADD B STA SUM LDA C CMA INC ADD DIF STA DIF LDA SUM ADD DIF STA SUM HLT ..... END	QUESTION-281 ORG 100 LDA B CMA INC ADD A SPA BUN 10 SZA BUN 30 BUN 20 HLT ..... END	QUESTION-282 ORG 100 CLA LOP, STA X I ISZ X ISZ CTR BUN LOP HLT X, DEC 500 CTR, DEC -256 END ORG 500 500, _____ 501, _____ ..... 5FF,_____ END	QUESTION-283 ORG 100 LDA A LOP, ADD A ISZ CTR BUN LOP HLT A, DEC 5 B , DEC 4 CTR , DEC -4
280	017013493	5	List the assembly program generated by compiler from the following program. Assume integer variables. SUM=0 SUM = SUM +A+B DIF=DIF-C SUM = SUM + DIF		5				
281	017013493	5	List the assembly program generated by compiler from the following IF statement: IF(A-B) 10,20,30 the program branches to statement 10 if A-B <0; to statement 20 if A-B=0; and to statement 30 if A-B>0.		5	QUESTION-284	QUESTION-285	QUESTION-289	QUESTION-290
282	017013493	5	Write a program loop, using a pointer and a counter that clears to 0 the contents of hexadecimal locations 500 through 5FF. ITERATION = 500-5FF = 0FF F*16 + F*16^0 = (15*16) + 0 = 255		5	LDA A CMA AND B CMA	ORG 100 LDA BL CMA INC ADD AL STA CL CLA CIL STA TMP LDA BH CMA INC ADD AH ADD TMP STA CH HLT ..... END	ORG 100 LDA A CMA STA TMP LDA B CMA AND TMP CMA STA ANS HLT ..... END	ORG 100 LDA A CMA AND B CMA STA TMP LDA B CMA AND A CMA AND TMP STA ANS HLT
283	017013493	5	Write a program to multiply two positive numbers by a repeated addition method.		6	STA A1 LDA B CMA AND A CMA AND A1 CMA STA A1 ADD A1 STA ANS HLT			
284	017013493	5	Write an assembly language program for the logical expression (A XOR B)+ (A' XOR B')		3				
285	017013493 OK	5	Write an assembly language program for multiplication 2*6 by repeated addition method		4				
286	017013493	5	Write a program to substract two double precision numbers.		5				
287	017013493 OK	5	Write an assembly language program for multiplication 5*5 by repeated addition method. For example, 5*5 = 5+5+5+5+5		5	QUESTION-296	QUESTION-297	QUESTION-298	QUESTION-299
288	017013493 OK	5	Write a program that evaluates XOR of two logic operands.		3	ORG 100 LDA A BSA SH4 HLT SH4, HEX 0 CIR CIR CIR CIR BUN SH4 I ..... END	ORG 100 LDA SUM LOP, ADD X I ISZ X ISZ CTR BUN LOP HLT X, HEX 5FF CTR , DEC -150 SUM , HEX 0 END	ORG 100 LDA X CMA AND Y CMA STA T1 LDA Y CMA AND X CMA AND T1 CMA STA T1 LDA Z CMA AND T1 CMA STA T2 LDA T1 CMA AND Z CMA AND T2 CMA HLT	ORG 100 LDA X BSA SH4 STA X LDA Y BSA SH4 STA Y HLT SH4, HEX 0 CLE CIL CLE CIL CLE CIL CLE CIL BUN SH4 I
289	017013493	5	Write a program that evaluates OR of two logic operands.		4				
290	017013493	5	Write a program that evaluates XNOR of two logic operands.		4				
291	017013493 OK	5	Write a program that evaluates NOR of two logic operands.		4				
292	017013493 OK	5	Write a program that evaluates circular left shift of an operand		3				
293	017013493 OK	5	Write a program that evaluates circular right shift of an operand		3				
294	017013493 OK	5	Write a program that evaluates arithmetic shift left of an operand		3				
295	017013493 OK	5	Write a program that evaluates arithmetic shift right of an operand		3				
296	017013493	5	Write a subroutine to circulate E and AC four times to right. If AC contains 079C in hex and E=1 what are contents of AC and E after subroutine is executed?		2				
297	017013493	5	Write an Assembly language program for addition of 150 numbers. Consider starting address of data is at memory location 5FF.		3				
298	017013493	5	Write a program that evaluates XOR of three logic operands.		3				
299	017013493	5	Write a program using subroutine to shift logical left five times in X and Y. Initially X has value A937 and Y has value C305 in hex. What are the contents of X & Y in hex after the execution of above program?		4				
300	017013493 OK	5	Write an assembly language program for addition of 75 numbers stored in memory from the starting hex location 250.		3				

301	017013493	5	Write an ALP for multiplication of data present at A and B respectively. A = 0000 1111 B = 0000 1011 C = A*B		5	QUESTION-301 ORG 100 LOP, CLE LDA Y CIR STA Y SZE BUN ONE BUN ZRO ONE,LDA X ADD P STA P CLE ZRO,LDA X CIL STA X ISZ CTR BUN LOP HLT ..... END			
302	017013493 OK	5	W.A.L.P to implement following logical operation P= A*B*C where P,A,B,C are memory locations stored with non zero positive numbers		4				
303	017013493 OK	5	W.A.L.P to implement following logical operation Z= AB'+A'C+ACD' where Z,A,B,C,D are content of memory locations		3				
304	017013493 OK	5	Write an assembly language program for multiplication 2*4 by repeated addition method. For example, 2*4 = 2+2+2+2		5				
305	017013493 OK	5	Write a assembly language program to multiply two positive signed bit numbers by repeated addition method.		5				
306	017013493	5	A bus oragnised CPU has 16 registers with 32 bits each, an ALU and a destination Decoder. 1. How many Multiplexer are there in the A bus and what is the size of each multiplexers? 32 mux of 16*1 size 2. How many selection inputs are needed for MUX A and MUX B? 4 selection lines 3. How many inputs and outputs are there in decoder? 4 i/p 16 o/p 4. How many inputs and outputs are there in ALU for data including input and output carries? 5. Formulate a control word for the system assuming that ALU has 35 operations.		4				
307	017013493 OK	5	Specify the control word that must be applied to processor to implement the following microoperations. 1. R1<-- R2 + R3 2. R5<--- R5-1 3. R6<--- shl R1 4. R7<--- input		4				
308	017013493 OK	5	Specify the control word that must be applied to processor to implement the following microoperations. (1) R1← R2 + R3 (2) R6← shl R1		2				
309	017013493 OK	5	Determine the microoperations that will be executed in the processor when 14 bit control word is applied 1. 00101001100101 2. 01001001001100 3. 00000100000010 4. 11110001110000		4				
310	017013493	5	Let SP = 000000 in the stack. How many items are there in the stack if: 1. FULL =1 and EMTY = 0? 64 2. FULL = 0 and EMTY = 1? 0		2				
311	017013493	5	Convert the following arithmetic expressions to reverse polish notation. a. A*B+A*(B*D + C*E) b. A+ B*[C*D +E*(F+G)] AB* A BD* CE* + * + c. [A*[B+C*(D+E)]]/[F*(G+H)] AB CD* EFG+*+*+ ABCDE+*+* FGH+*/		3				
312	017013493	5	Convert the following arithmetic expressions from reverse polish notation. a. A B C D E * / - + b. A B C * / D - E F / + A+(B-[C/(D*E)]) c. A B C D E F G +*+*+* ([A/(B*C)]-D)+(E/F) A*[B+([C*(D+[E*(F+G)])])]		3				
313	017013493 OK	5	Evaluate 623+-382/+*2^3+		2				
314	017013493 OK	5	a)Determine the micro-operation that will be executed in processor when 14-bit control words are applied: 00101001100101 b)Specify the control word to implement the following microoperation: R4 ← R5 + R6 c)Convert the following arithmetic expression from RPN to infix notation. 5 9 2 4 + * - 5-[9*(2+4)]		3				
315	017013493	5	1. Convert the following numerical arithmetic expression into reverse polish notation and show the stack operations for evaluating the numerical result. {(3+4+5)/[10*(2+6+8)-5]}*(13-(6*2)) 2.Specify the control word that must be applied to the processor to implement the following microoperations. R1 = R3 or R2		5				
316	017013493	5	1. Convert (2+3) * [7*(5+4) + 10] into postfix notation and evaluate using stack. 2. Specify the control word that must be applied to processor to implement the following microoperations. R2-->R4 ^ R6		3				
317	017013493	5	Convert the following numerical arithmetic expression into reverse polish notation & show the stack operation for evaluating the numerical result (3*4)*[10+(2*9) – 10]		3				
318	017013493	5	Determine the micro-operation that will be executed in the processor of general register organization when the following 14-bit control word are applied. a. 11110001110000 b. 00000100000010		4				
319	017013493	5	a) Determine the micro-operation that will be executed in processor when 14-bit control words are applied: 11111010100101 b) Specify the control word to implement the following microoperation: R4 ← R5 ^ R6 c) Convert the following arithmetic expression from RPN to infix notation. ABCDE + * - /		3				
320	017013493	5	1. Convert the following numerical arithmetic expression into reverse polish notation and show the stack operations for evaluating the numerical result. {(10+5+5)/[10*(2+6+7)-15]}*(13-(5*2)) 2. Specify the control word that must be applied to the processor to implement following microoperations. R6= R4 ^ R1		5				
321	017013493 OK	5	Write an ALP to implement following logical operation Y= P'Q+RST'		3				
322	017013493 OK	5	Convert the following numerical arithmetic expression into reverse polish notation and show the stack operations for evaluating the numerical result. {(140-25)*(10-(4*2))/[5*(2+9)]}		3	140 25 - 10 4 2*-* 5 2 9+*/			
323	017013493 OK	5	Write an ALP for multiplication of data present at A and B respectively. A = 0000 1110 B = 0000 1001 C = A*B		5				
324	017013493	6	A processor has 300 distinct instructions and 70 general-purpose registers. A 32-bit instruction word has an opcode, two register operands, and an immediate operand. The number of bits available for the immediate operand field is_____	b	1	8	9	6	7
325	017013493	6	Only instructions with zero, one, and two addresses are supported by some CPUs. The size of an op-code is 16 bits, whereas the size of an address is 4 bits.What is the Maximum number of two address instructions?	c	1	128	512	256	64

326	017013493	6	A computer has an instruction size of 16 bits and has 16 programmer visible registers. Each instruction has two source and one destination operands and uses only register direct addressing. The maximum number of opcodes that this processor can have is	a	1	16	8	32	64
327	017013493	6	Consider a 32-bit processor which supports 30 instructions. Each instruction is 32 bit long and has 4 fields namely opcode, two register identifiers and an immediate operand of unsigned integer type. Maximum value of the immediate operand that can be supported by the processor is 8191. How many registers the processor has?	b	1	64	128	256	512
328 Doubt	017013493	6	A processor has 64 registers and uses 16-bit instruction format. It has two types of instructions: I-type and R-type. Each I-type instruction contains an opcode, a register name, and a 4-bit immediate value. Each R-type instruction contains an opcode and two register names. If there are 8 distinct I-type opcodes, then the maximum number of distinct R-type opcodes is _____.	a	1	14	16	18	19
329	017013493	6	Consider the following :1) Operation code 2) Source operand reference 3) Result operand reference 4) Next instruction reference, Which of the above are typical elements of machine instructions?	d	1	1,2,3 ONLY	1 AND 2 ONLY	2 ,3,4 ONLY	1,2,3,4
330	017013493	6	Match the followings. 1) ST@ ADR p) DIRECT 2) ST ADR q) INDIRECT 3) ST $ ADR r) AUTO INCREMENT 4) ST R1 s) REGISTER INDIRECT 5) ST (R1) t) RELATIVE 6) ST(R1)+ u) REGISTER v) IMMEDIATE	b	1	1-r, 2-t, 3-s, 4-u, 5-p,6-q	1-q, 2-p, 3-t,4-u, 5-s, 6-r	1-p, 2-q, 3-r, 4-s, 5-t,6-u	1-u, 2-p, 3-u, 4-q,5-r,6-s
331	017013493	6	A processor has 40 distinct instructions and 24 general purpose registers. A 32-bit instruction word has an opcode, two register operands and am immediate operand. The number of bits available for the immediate operand field is _____.	c	1	8	32	16	64
332	017013493	6	A Computer uses a memory unit with 256K word of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code and a register code part to specify one of 64 registers and an address part. How many bits are there in operation code, the register code part and the address part?	b	1	7,7,18	7,6,18	6,7,18	6,6,18
333	017013493	6	A processor has 400 distinct instruction & 74 general purpose register, a 32bit instruction word has opcode, two register operands & an immediate operand field. The number of bits available for immediate operand field is _____	c	1	7	32	9	5
334	017013493	6	A stack-based CPU organization uses_____ address instructions	d	1	2	1	3	0
335 See	017013493	6	Match the pairs in the following questions: (A) Base addressing (p) Reentranecy (B) Indexed addressing (q) Accumulator (C) Stack addressing (r) Array (D) Implied addressing (s) Position independent	c	1	A-R,B-S,C-P,D-Q	A-S, B-R,C-Q,D-P	A-S, B-R,C-P,D-Q	A-Q, B-R,C-S,D-P
336	017013493	6	When we use auto increment or auto decrements, which of the following is/are true? 1) In both, the address is used to retrieve the operand and then the address gets altered 2) In auto increment the operand is retrieved first and then the address altered 3) Both of them can be used on general purpose registers as well as memory locations	a	1	2& 3	2	1& 2	All are true
337	017013493	6	State whether the following statements are true or false. I. With one-address instructions, the programmer generally has available only one general-purpose register the accumulator. II. Zero-address instruction are applicable to a special memory organization called a stack.	d	1	Only I is true	only II is true	both are false	both are true
338	017013493	6	To evaluate arithmetic expressions of data stored in memory, which two instruction formats use LOAD as their first instruction?	d	1	One address, Zero address	RISC, Zero address	RISC, Two address	One address, RISC
339	017013493	6	A Program Counter Contains a number 825 and Address part of instruction contains the number 24. The Effective Address in the Relative Address Mode, when an Instruction is read from the Memory is?	d	1	24	850	801	849
340	017013493	6	Which is used to store critical pieces of data during subroutines and interrupts:	b	1	QUEUE	STACK	ACCUMULATOR	DATA REGISTER
341	017013493	6	Match following 1.Immediate A.LD ADR 2.Indirect B.LD @ADR 3.Relative C.LD $ADR 4.Direct D.LD #ADR	a	1	1-D,2-B,3-C,4-A	1-A,2-B,3-C,4-D	1-D,2-B,3-A,4-A	1-A,2-B,3-C,4-A
342	017013493	6	Match the pairs in the following questions: 1. LD ADR P. Register mode 2. LD @ADR Q. Relative address mode 3. LD $ADR R. Auto increment mode 4. LD #NBR S. Register indirect mode 5. LD ADR(X) T. Direct address 6. LD R1 U. Index addressing mode 7. LD (R1) V. Immediate mode 8. LD (R1)+ W. Indirect address mode	d	1	(1-T), (2-W), (3-V), (4-U), (5-P), (6-P), (7-Q), (8-R)	(1-T), (2-W), (3-Q), (4-R), (5-V), (6-P), (7-U), (8-S)	(1-T), (2-W), (3-S), (4-S), (5-V), (6-Q), (7-U), (8-R)	(1-T), (2-W), (3-Q), (4-V), (5-U), (6-P), (7-S), (8-R)
343	017013493	6	Match the following pair: 1.Indirect mode x. constants 2.Autodecrement mode y. pointers 3.Immediate mode z. loops	b	1	1-x, 2-y, 3-z	1-y, 2-z, 3-x	1-z, 2-y, 3-x	1-y, 2-x, 3-z
344	017013493	6	Which of the following statement/s are false? 1. index addressing mode is used for branch instruction. 2. in auto increment the operand is retrieved first and then the address altered. 3. zero-address instruction are applicable to a special memory organization called a stack.	d	1	1 & 2	2 & 3	1 & 3	None of above
345	017013493	6	An addressing mode in which the address field of instruction specifies a register in CPU, whose content given the address of operand in memory is called _____	d	1	indirect addressing mode	relative addressing mode	register addressing mode	register indirect addressing modes
346	017013493	6	An address field of the instruction LDA refers to a CPU register in which effective address of operand is stored. Identify the addressing mode based on the given description.	b	1	Register mode	Register indirect mode	Immediate addressing mode	Implied Mode
347	017013493	6	Zero-address instructions in a stack-organized computer are _____ instructions.	d	1	Register mode	Register indirect mode	Immediate addressing mode	Implied Mode
348	017013493	6	Which of following pair match correct? (Here, ACC stands for Accumulator) 1. Zero address instruction p. CMA 2. One address instruction q. Y = Y + X 3. Two address instruction r. Y = A – B 4. Three address instruction s. ACC = ACC – X	a	1	(1,p), (2,s), (3,q), (4,r)	(1,p), (2,q), (3,s), (4,r)	(1,p), (2,s), (3,r), (4,q)	(1,p), (2,q), (3,r), (4,s)

349	017013493	6	Match the pairs in the following questions: 1. BGT A)A> B 2. BLT B)A< B 3. BLE C)A=B D)A<=B E)A/= B F)A >= B	a	1	1-A,2-B,3-D	1-A,2-C,3-D	1-A,2-A,3-D	1-A,2-B,3-C
350	017013493	6	consider an 8-bit ALU with a 4-bit status register. The four status bits are symbolized by C, S, Z & V which stands for carry, sign, zero and overflow, respectively. Let A = 1111 0000 & B = 0001 0100 and ALU perform A - B. Which of the following represents the state of 4-bit status register?	b	1	0011	1100	1111	0000
351	017013493	6	Which one of the following is a special characteristic of RISC processor?	d	1	Provide direct manipulation of operands residing in memory	A large variety of addressing modes	Variable length instruction formats	Overlapped register window
352	017013493	6	RISC stands for:	c	1	Remaining Instruction Set of Compiler	Remaining Intermediate Storage of Computer	Reduced Instruction Set Computer	Reduced Instruction Set Complier
353	017013493	6	A computer has 32 bit instructions and 12 bit addresses. if there are 250 two address instructions, how many one address instrcutions can be formulated?		3				
354	017013493	6	A computer uses a memory unit of 512 K words of 32 bits each. A binary instruction code is stored in one word of the memory. The instruction has four parts: an addressing mode field to specify one of the two-addressing mode (direct and indirect), an operation code, a register code part to specify one of the 256 registers and an address part. How many bits are there in addressing mode part, opcode part, register code part and the address part?	1,4,8,19	2				
355	017013493	6	Write a program to evaluate the arithmetic statement: Y = [(A+B) * (C-[D/E])] Using a two-address instruction, three-address instruction, zero address instruction		3				
356	017013493	6	A machine has a 32-bit architecture, with 1-word long instructions. It has 64 registers, each of which is 32 bits long. It needs to support 45 instructions, which have an immediate operand in addition to two register operands. Assuming that the immediate operand is an unsigned integer, the maximum value of the immediate operand is _____	16383	1				
357	017013493	6	In X = (M + N × O) / (P × Q), how many one-address instructions are required to evaluate it?	8	1				
358	017013493	6	The memory unit of a computer has 256K words of 32 bits each. The computer has an instruction format with four fields: an operation code field, a mode field to specify one of seven addressing modes, a register address field to specify one of the 60 processor registers, and a memory address. Specify the instruction format and the number of bits in each field if the instcution is in one memory word.		3	| 5bit | Add : 3 bit | Reg : 6 bit | A18 bit |			
359	017013493	6	Following instructions were executed on a stack machine PUSH X PUSH X MUL POP Y --------> Y = x^x PUSH Y PUSH Y ADD ----------> Y+Y = 2x^2 PUSH Y MUL ----------> 2X^2 * X^2 = 2X^4 POP Z What is value of Z?	2x^4	2				
360	017013493	6	The two word instruction at address 200 and 201 is "load to AC" with an address field equal to 600. Value stored at 600 is 400, at 500 is 900, at 700 is 950 and at 400 is 350.The words stored at 800,801 and 802 are 300,301,302. the content of processor register R1 is 500 and content of index register XR is 100. Evaluate the EA and operand if addressing modes are 1)Direct 4) Immediate 2)Indirect 5) Register indirect 3)Relative 6) Index		3				
361	017013493	6	A two word instrcution is stored in memory at an address designated by thw symbol W.The adddress field of the instrcution stored at W+1 is designated by symbol Y. The operand used during the execution of the instruction is stored at an address symbolised by Z. An index Register contains value X.State how Z is calculated from other addresses if addressing modes of instruction is a. direct b. indirect c. relative d. indexed		5				
362	017013493	6	Write a program to evaluate the arithmethic statement: X = [A-B+C*(D*E-F)]/[G+H*K] Using a. one address instruction, two address instruction, three address instruction, zero address instruction		7				
363	017013493	6	Write a program to evaluate the arithmethic statement: Y = A*B + C* D Using a. one address instruction, two address instruction, three address instruction, zero address instruction		7				
364	017013493	6	Write a program to evaluate the following arithmetic statement using zero,one, two, three address and RISC instruction format. Z = (A+B) * (C+D)		5				
365	017013493	6	Write the given expression in Zero, One, Two, three address and RISC instruction format. Use symbols ADD, SUB, MUL & DIV for arithmetic operations; MOV for Transfer Type Operations; and LOAD and STORE for transfers to and from memory and AC register. Y = ((A * B) + D) / (C - E)		5				
366	017013493	6	A computer uses a memory unit of 4096 words of 32 bits each. A binary instruction code is stored in one word of the memory. The instruction has four parts: an addressing mode field to specify one of four the addressing mode (immediate, direct, indirect and register), an operation code, a register code part to specify one of the 512 registers and an address part. How many bits are there in addressing mode part, opcode part, register code part and the address part?		3				
367	017013493	6	Write a program to evaluate the arithmetic statement: Y = (A* B) + (C / D) Using a one address instruction, two address instruction, three address instruction, zero address instruction and RISC address instruction.		5				
368	017013493	6	A two-word LOAD instruction is located at 200 followed by its address field 300 at location 201. The value stored at location 300 is 500 and value at location 400 is 600.The words stored at location 500, 501,502 is 825, 425, 320 respectively. The value stored at location 600 is 450. A processor register R contains value 400 and an index register contains value 100.Evaluate Effective address and operand in accumulator if addressing modes are: 1) Relative 2) Register indirect 3) Index		3				
369	017013493	6	Consider the following arithmetic expression: A=B*((C+(D*E))-(F/G)) Write a program to evaluate the expression using zero, two and three address instruction formats.		3				

370	017013493	6	Write a program to evaluate the arithmethic statement: X = [A*B]-[[C*D+E]/[G-H]] Using a) one address instruction, b)two address instruction, c)zero address instruction		3				
371	017013493	6	1. A LOAD instruction is stored at 300 with address field in next location the address field has value 400 and value stored at 400 at 550 and 550 is 750. The words stored at 700, 701 and 702 are 805, 850 and 885. A processor register R contains the number 800 and index register has value 150. Evaluate the effective address EA and operand if addressing modes are a) Direct address b) Immediate address c) Relative address d) Indirect address e) Register address f) Index address		3				
372	017013493	6	Write given expression in zero, one, two, three address and RISC instruction format. Use symbols ADD, SUB, MUL for arithmetic operations; MOV for transfer type operations; and LOAD and STORE for transfers to and from memory and AC register. X= (P+Q) * (R-S)		5				
373	017013493	6	The Two Word Instruction at addresses 200 and 201 is “Load to AC” with an address field equal to 500.PC has the value 200 for fetching this instruction. The content of processor Register R1 is 400 and the content of index Reg(XR) is 100. The figure shows some other addresses with their memory content. Find out EA and Content of AC for Different Addressing modes. AddressMemory 200Load to AC Mode201ADD= 500 202Next Instruction		5				
374	017013493	6	Write given expression in Zero, One, Two, three address and RISC instruction format. Use symbol ADD, SUB, MUL for arithmetic operations; MOV for Transfer type Operations; and LOAD and STORE for transfers to and from memory and AC register. Y = (X + A * D) / (B - C)		5				
375	017013493	6	An instruction is stored at location 300 with its address field at location 301. the address field has the value 400. A processor register R1 contains the number 200. Evalaute effective address if addressing mode of the instruction is direct, immediate, relative, register indirect, index with R1 as index register.		3				
376	017013493	6	Perform logic AND, OR, XOR with two binary strings 10011100 and 10101010		2				
377	017013493	6	Given the 16 bit value 1001101011001101. What operation must be performed in under to: a. clear to 0 the first eight bits. b. set to 1 the last eight bits c. complement the middle eight bits.		3				
378	017013493	6	An 8 bit register contains the value 01111011 and carry bit is equal to 1. Perform all shift operations.Each time start from initial value given above		4				
379	017013493	6	Represent the following signed numbers in binary using 8 bits. +83 ; -83; +68; -68 a. Perform the addition -83 + (+68) in binary and interpret the result obatined. b. Perform the substraction (-68)-(+83) in binary and indicate if there is an overflow. c. Shift binary -68 once to the right and convert in decimal. d. Shift -83 once to left and indicate if there is an overflow.		6				
380	017013493	6	Show the circuit labeled in check for zero output is an 8 bit NOR gate		2				
381	017013493	6	A 8 bit computer has a register R. Determine the values of status bit C, S,Z,V after each of the following instructions. The initial vlaue of register R in each case is hexadecimal 72. the numbers below are also in hexadecimal. a. Add immediate operand C6 to R. b. Add immediate operand 1E to R. c. Substract immediate operand 9A from R. d. And immediate operand 8D from R. e. XOR R with R.		7				
382	017013493	6	Consider the two 8 bits A= 01000001 and B= 10000100. a. Give the decimal equivalen of each number assuming tht they are unsigned and they are signed. b. Add two binary numbers and inetrpret sum assuming that numbers are unsigned and signed. c. Determine values of C,S, Z, V after addition. d. List conditional branch instrcution thet will have true condition.		7				
383	017013493	6	Consider the two 8 bits A= 01000001 and B= 10000100. a. Evaluate the difference A-B and interpret binary result. b. Determine values of C,S,Z,V c. List conditional branch instrcution thet will have true condition.		7				
384	017013493	6	Consider the two register A= 49H and B= 2DH. a. Evaluate the difference A-B and interpret binary result. b. Determine values of C,S,Z,V c. List conditional branch instruction that will have true condition.		3				
385	017013493	6	What are basic differences between a branch instruction, a call instruction and a program interrupt?		3				
386	017013493 baki	6	The content of the top of a memory stack is 5320. The content of the stack pointer SP is 3560. A two word call subroutine instruction is located in memory addresses 1120 followed by address field of 6720 at location 1121. What are contents of PC,Sp,and the top of Stack: a. before the call instruction is fetched from memory? b. After call instruction is executed? c. After return from subroutine?		4				
387	017013493	6	Determine the values of status bits C, S, V and Z for given operation having register content R = 9B H. Operation: Subtract R from immediate operand 7C H.		2				
388	017013493 baki	6	The content of the top of a memory stack is 624. The content of the stack pointer SP is 4000. A two-word call subroutine instruction is located in memory addresses 256 followed by address field of 792 at location 257. What are contents of PC, SP and the top of Stack: a. before the call instruction is fetched from memory? b. After call instruction is executed? c. After return from subroutine?		3				
389	017013493	6	Determine the values of status bits C, S, Z, V for given operation having register content 8D H. Operation: Subtract immediate operand 9A from R		2				
390	017013493	6	RISC processor contains 10 global registers,10 local registers,6 in registers and 6 out registers.it contains 3 register windows,what is the size of window and register file of the processor?	b	1	30 and 74 W = 10 + 2(6) + 10 = 32	32 and 58 R =	22 and 64 G + (L+C)W = 10+(10+6)3 = 58	26 and 58
391	017013493	6	The computer use register windows with following charcteristics. Determine the window size and total number of registers. Global Registers= 8 ; Local Registers = 8 ; Common Registers = 8; Number of Windows = 4		2				

392	017013493	6	The computer use register windows with following charcteristics. Determine the window size and total number of registers. Global Registers= 10 ; Local Registers = 10 ; Common Registers = 6; Number of Windows = 8		2				
393	017013493	6	The computer use register windows with following charcteristics. Determine the window size and total number of registers. Global Registers= 16 ; Local Registers = 16 ; Common Registers = 16; Number of Windows = 16		2				
394	017013493	6	A 8-bit computer has a register R. Determine the values of status bit C, S, Z, V after each of following instruction. The initial value of R in each case is hexadecimal 91. The number below are also in hexadecimal. a) add immediate operand A9 to R. b) subtract immediate operand 9A from R.		4				
395	017013493	6	Perform $(-45)_{10}$ - $(-39)_{10}$ using 8-bit signed 2's complement representation		2				
396	017013493	6	An 8-bit register R contains hexadecimal value C9. Determine the values of status bits C, S, V and Z for given operation: Subtract R from immediate operand B8 H.		2				
397	017013493	6	Write given expression in zero, one, two, three address and RISC instruction format. Use symbols ADD, SUB, MUL for arithmetic operations; MOV for transfer type operations; and LOAD and STORE for transfers to and from memory and AC register. Y = ((B + D) / ((C * E) + A))		5				
398	017013493	7	Pipelining is a ----------technique?	b	1	serial	parallel	Scalar operation	Superscalar operation
399	017013493	7	The initial stage for an instruction executing in pipelining is -----?	c	1	Decode	Execute	Fetch	Address generation.
400	017013493	7	The stages of 3 stage pipelining are----?	a	1	Fetch, Decode, Execute	Decode, Fetch, Execute	Execute, Fetch, Decode	none of the above
401	017013493	7	Throughput is calculated as----	a	1	The number of instructions/ Total time to complete the instructions	Total time to complete the instructions/number of instructions	Speed of the processor/ Number of instructions	The number of instructions/speed of the processor
402	017013493	7	By using pipelining, the throughput of the processor----?	c	1	decreases	becomes unity	Increases	Remains the same.
403	017013493	7	Which of the below is not a pipeline conflicts?	d	1	resource conflicts	data dependency	branch difficulties	Balancing of load
404	017013493	7	Which of the following is an advantage of pipelining?	d	1	Instruction throughput increases.	Faster ALU can be designed when pipelining is used.	Pipelining increases the overall performance of the CPU.	All of the above
405	017013493	7	which of the following is not a part of flynn's classification?	a	1	SIDD	SISD	MISD	SIMD
406	017013493	7	which of the following stage is not a part of instruction pipeline?	a	1	DI	FO	EX	FI
407	017013493	7	for large number of task in a pipeline structure,speed-up ratio is nearly equivalent to?	d	1	no of tasks	no of registers	no of operands	no of segments
408	017013493	7	In arithmetic pipeline sub operation performed in ------ segments.	a	1	4	2	1	5
409	017013493	7	_____ represents an organization that includes many processing units under the supervision of a common control unit	c	1	SSMD	MISD	SIMD	SISD
410	017013493	7	Which processor requires more number of registers?	d	1	SIMD	8085	CISC	RISC
411	017013493	7	Each stage in pipelining should be completed within _____ cycle.	a	1	1	2	3	4
412	017013493	7	The RISC processor has a more complicated design than CISC.	a	1	FALSE	TRUE		
413	017013493	7	Which of the following sentences is/are correct for RISC's pipeline? a) Small no of sub-operations b) Variable-length instruction formats c) Single-cycle instruction execution d) It supports register to memory operation	d	1	Both a) and b)	Both b) and d)	Both c) and d)	Both a) and c)
414	017013493	7	In pipelining the task which requires the least time is performed first.	b	1	TRUE	FALSE		
415	017013493	7	To increase the speed of memory access in pipelining, we make use of _____	d	1	Special memory locations	Special purpose registers	Buffers	Cache
416	017013493	7	The computer architecture aimed at reducing the time of execution of instructions is _____	a	1	RISC	CISC	ISA	SIMD
417	017013493	7	Arithmetic pipeline performed in____ segments.	c	1	3	6	4	5
418	017013493	7	Which is the correct pipeline pattern for RISC pipeline structure?	a	1	I,A,E	DA,FO,FI,EX	I,E,A	FI,DA,FO,EX
419	017013493	7	In an arithmetic pipeline, the time delays of 4 segments are 6,7,10 and 8ns respectively.the delay of tr=1ns.the clock cycle time(tp)is------	c	1	6	7	11	9
420	017013493	7	Which is the correct pipeline pattern for the Instruction pipeline structure?	a	1	FI, DA, FO, EX	A, I, E	E, A, I	I, E, A
421	017013493	7	Which of the following sequence is correct for the RISC pipeline? 1.ALU Operation 2.Execute Instruction 3.Instruction Fetch	d	1	1-2-3	2-1-3	1-3-2	3-1-2

422	017013493	7	Which of the following statements is/are correct for major difficulties in instruction pipeline? 1. Data dependency conflicts occurred, when an instruction depends on result of previous instruction, which is available. 2. Resource conflicts caused by access to memory by two segments at different time. 3. It arises from branch and other instruction that change the value of PC.	c	1	only 1	only 2	only 3	Both 1and 2
423	017013493	7	In Arithmetic Pipeline, the floating- point addition and subtraction is done in _____	a	1	4 parts, Compare the exponents, Align the mantissas, Add or subtract mantissas, Normalize result.	4 parts, Compare the exponents, Add or subtract mantissas, Normalize result, Align the mantissas	) 4 parts, Align the mantissas, Compare the exponents, Add or subtract mantissas, Normalize result.	2 parts, Align the mantissas, Add or subtract mantissas
424	017013493	7	How many clock cycle will be needed to execute Ai + Bi * Ci statement in non-pipeline architecture for i = 1, 2, 3 ?	c	1	8	5	9	12
425	017013493	7	How many clock cycles will be needed to execute Ai+Bi*Ci statement in pipeline architecture for i = 1,2,3 ?	b	1	8	5	9	6
426	017013493	7	How many clock cycles will be needed to execute Ai+Bi*Ci statement in pipeline architecture for i=1 TO 5?	c	1	5	6	7	8
427	017013493	7	Which of the following sequence is correct for arithmetic pipeline? 1. Align the mantissas. 2. Compare the exponent. 3. Normalize the result. 4. Add or subtract the mantissas.	c	1	1-2-4-3	4-3-2-1	2-1-4-3	1-2-3-4
428	017013493	7	_____ structure is only of theoretical interest since no practical system has been constructed using it.	c	1	SIMD	SISM	MISD	MIMD
429	017013493	7	Which of the following statement/s is/are incorrect about RISC pipeline? 1. RISC instruction implement on instruction pipeline using small number of sub-operations with each being executed in one clock. 2. Because of Fixed length instruction format the decoding can occur at same time at register selection. 3. All data manipulation have Memory to Memory operation.	b	1	only 2	only 3	Both 1and 2	Both 2 and 3
430	017013493	7	The number of clock cycles it takes to process 200 tasks in six segment pipeline is ___.	b	1	203	205	199	206
431	017013493	7	Which of the following is correct sequence for instruction pipeline? 1.Decode the instruction. 2. Fetch operands from the memory 3. Fetch instruction from memory. 4. Execute the instruction. 5. Calculate effective address. 6. store the result in proper place.	a	1	3,1,5,2,4,6	3,5,1,2,4,6	3,2,5,1,4,6	1,3,2,5,4,6
432	017013493	7	For large number of task & Tn = K Tp (where Tn is non-pipeline time & Tp is pipeline time , K is segment) in a pipeline structure, the Speedup ratio is equivalent to_____	a	1	(n Tn) / (K + n - 1) Tp	n Tn	(K+ n -1)Tp	K
433	017013493	7	We have 2 designs D1 and D2 for a synchronous pipeline processor. D1 has 5 stage pipeline with execution time of 3 ns, 2 ns, 4 ns, 2 ns and 3 ns. While the design D2 has 8 pipeline stages each with 2 ns execution time. How much time can be saved using design D2 over design D1 for executing 100 instructions? (Assume that there is no register delay in pipeline system)	c	1	214ns	210ns	202ns	416ns
434	017013493	7	Which of the following statement/s is/are correct? 1. Pipelining improves CPU performance due to the introduction of parallelism. 2. Data conflict can overcome by use of pipeline with delayed load operation. 3. In space-time diagram, horizontal axis displays the time in clock cycles. 4. There is no practical system has been constructed using MIMD organization. Ans is 1,2,3	d	1	Only 1, 2, 4	Only 4	Only 3 and 4	Only 1 and 4
435	017013493	7	For arithmetic operation (Ai * Bi) + (Ci * Di) with a stream of numbers. specify a pipeline configuration to carry out this task. list the content of all register in the pipeline for i=1 to 6 & determine how many clock cycles used to implement this arithmetic operation.		4				
436	017013493	7	Consider the time delays of the four segment pipeline are as follows t1 = 60ns, t2 = 70ns, t3 = x ns, and t4 = 80 ns. Interface registers have a delay of tr = x/10 ns. A non-pipeline system takes 320ns to process a task. Calculate: Pipeline cycle time Speed up ratio Total non-pipeline time to process 500 tasks Total pipeline time to process 500 tasks		4				
437	017013493	7	consider a pipeline having 4 phases with duration 50ns,50ns,70ns,60ns,given register delay is 10ns. (1) calculate pipeline cycle time (2) non pipeline execution time (3) speedup ratio (4) total non pipeline time for 100 task.		2				
438	017013493	7	consider a pipeline having 4 phases with duration 60ns,50ns,90ns,80ns,given delay is 10ns. (1) calculate pipeline cycle time (2) non pipelineexecution time (3) speedup ratio (4) total non pipeline time for 1000 task (5) pipeline time for 1000 task		4				
439	017013493	7	arithmetic operation (Ai *Bi + Ci) with a stream of seven numbers (i=1 to 7). Specify a pipeline configuration to carry out this task.		4				
440	017013493	7	A non-pipeline system takes to process a task. The same task can be processed in a six segment pipeline with a clock cycle of 10ns. Determine the speedup ratio of the pipeline for 100 tasks.What is the maximum speed up that can be achieved? non-pipeline time is 50ns		4				
441	017013493 ok	7	Draw a space-time diagram for a six -segment pipeline showing the time it takes to process eight tasks		4				
442	017013493 ok	7	For arithmetic operation (Ai+Bi)(Ci+Di) with a stream of numbers.Specify a pipeline configuration to carry out this task.List the content of all registers in the pipeline for i=1 through 6		4				
443	017013493	7	A non-pipeline system takes 80 ns to process a task. The same task can be processed in a ten segments pipeline with a clock cycle of 20 ns. Determine the number of clock cycle required and speedup ratio of the pipeline for 150 tasks. What is the maximum speed up that can be achieved?		3				
444	017013493	7	A 4-stage arithmetic pipeline has a stage delays as 150,120,160,140 nanoseconds respectively. Register delay between stages is 5 nanoseconds. Determine speed up ratio for the system having 1000 tasks.		2				
445	017013493	7	Draw a space-time diagram for a five -segment pipeline showing the time it takes to process seven tasks		2				

446	017013493	7	consider the following 4 instruction 1. LOAD : R1 ← M[address1] 2. LOAD : R2 ← M[address2] 3. ADD : R3 ← R1 + R2 4. STORE : M[address 3] ←R3 how many clock cycle is used for implement this instruction program using RISC pipeline ?	a	1	6	7	8	4
447	017013493	7	Consider a pipeline having 6 phases with duration 250ns, 110ns, 115ns, 95ns, 300ns and 115ns. The registers that are used between pipeline stages have a delay of 25ns. (1) Calculate pipeline cycle time & non-pipeline execution time (2) Maximum Speedup ratio (3) Pipeline time for 525 instructions.		4				
448	017013493	8	1's complement of 1011101 is _____	c	1	101110	1001101	100010	1100101
449	017013493	8	2's complement of 11001011 is _____	c	1	1010111	11010100	110101	11100010
450	017013497	8	On subtracting (01010)2 from (11110)2 using 1's complement, we get _____	d	1	1001	11010	10101	10100
451	017013498	8	On subtracting (001100)2 from (101001)2 using 2's complement, we get _____	b	1	1101100	11101	11010101	11010111
452	017013499	8	On addition of 28 and 18 using 2's complement, we get _____	b	1	101110	101110	101111	1001111
453	17013493	8	On addition of +38 and -20 using 2's complement, we get _____	c	1	11110001	100001110	10010	110101011
454	17013493	8	On addition of -46 and +28 using 2's complement, we get _____	a	1	-10010	-101	1011	100101
455	17013493	8	On addition of -33 and -40 using 2's complement, we get _____	d	1	1001110	-110101	110001	-1001001
456	17013493	8	On subtracting +28 from +29 using 2's complement, we get _____	d	1	11111010	111111001	100001	1
457	17013493	8	_____ is a straightforward method of representing positive and negative numbers.	c	1	Radix	Complement	Sign Magnitude	Encode
458	17013493	8	The 1's complement of 1 in 4 bits is _____ 0001 ---> 1110	d	1	1	0	1001	1110
459	17013493	8	The sign magnitude representation of -9 is _____ 1 00001001 --->	c	1	1001	11111001	10001001	11001
460	17013493	8	if you are given a word of size n-bits, the range of 2's complement of binary number is __	c	1	– (2n +1) to +(2n +1)	–(2n+1) to +(2n)	-2n-1 to +2n-1-1	0 to +(2n-1+1)
461	17013493	8	In both signed magnitude and 2's complement , positive and negative numbers are separated using _____	b	1	LSB	MSB	0	1
462	17013493	8	If m is the 2's complement and n is the binary number, then _____	b	1	m=n'	m=n'+1	m=n'-1	m=n
463	17013493	8	The additive inverse of a number is the number which when added to the original number gives 1 as a result.	FALSE	1				
464	17013493	8	The bitwise complement of 0 is _____	c	1	1	10000000	11111111	11111110
465	17013493	8	Subtraction in computers is carried out by _____	b	1	1's complement	2's complement	3's complement	9's complement
466	17013493	8	Subtract X from Y Where X= (+32) and Y= (-19). Use 8-bit subtraction method and give answer in binary.	b	1	1010101	11001101	110011001	110110101
467	17013493	8	on subtracting (01010)2 from (11110)2 using 1's complement, we get _____	d	1	1001	11010	10101	10100
468	17013493	8	Which of the following decimal number cannot be converted to 8-bit 2's complement notation?	d		135	-144	-107	both a and b
469	17013493	8	The addition of +19 and +43 results as _____ in 2's complement system.	d	1	11001010	101011010	101010	111110
470	17013493	8	The advantage of 2's complement system is that _____	a	1	Only one arithmetic operation is required	Two arithmetic operations are required	No arithmetic operations are required	Different Arithmetic operations are required
471	17013493	8	For arithmetic operations only _____	b	1	1's complement is used	2's complement	10's complement	9's complement
472	17013493 ok	8	0 101101 + 0 011111		1				
473	17013493 ok	8	1 011111 + 1 101101		1				
474	17013493 ok	8	0 101101 +1 100001		1				
475	17013493 ok	8	0101101-0 101101		1				
476	17013493	8	1 011111-0 101101		1				
477	17013493 ok	8	Perform (+12) – (+20) using 8-bit signed 2's complement representation.		2				
478	17013493 ok	8	Let P = (+91)10 and Q = (-19)10. Perform the following arithmetic operation using 8-bits 2's complement method. (i) (-P)+(-Q). Convert the result into equivalent decimal number. (ii) Subtract P from Q. Convert the result into equivalent decimal number.		3				
479	17013493 ok	8	Find result of addition of -55 and -42 using 2's complement use 7 bit.		2				
480	17013493 ok	8	Perform (-9) +(-6) using signed 1's complement representation using only 5 bits including sign		1				
481	17013493 ok	8	On addition of +35 and +40 using 2's complement use 7 bit, we get _____		3				
482	17013493 ok	8	On addition of -35 and -40 using 2's complement use 7 bit, we get _____		3				
483	17013493 ok	8	Perform (+22) – (+30) using 8-bit signed 2's compliment representation.		3				
484	17013493 ok	8	Perform (-13) +(-6) using signed 2's complement representation. Use 8 bits including sign bit. Also convert obtained result in decimal.		3				
485	17013493 ok	8	Perform (+32) – (+40) using 7-bit signed 2's complement representation.		2				
486	17013493 ok	8	Perform (-50) - (-29) using 7 bit signed 2's complement representation.		2				
487	17013493	9	Which of the following is used for binary multiplication ?	b	1	Restoring Multiplication	Booth's Algorithm	Pascal's Algorithm	Digit by Digit Multiplication
488	17013493	9	Booth's Algorithm is applied on	b	1	decimal numbers	binary numbers	hexadecimal numbers	octal Numbers
489	17013493	9	If Booth's Multiplication is performed on the numbers 22*3, then what is 3 referred to as	d	1	accumulator	multiplicand	quotient	multiplier

490	17013493	9	What is the value of n in multiplication of 110* 1000?	c	1	2	3	4	0
491	17013493	9	What will be the value obtained after multiplication of (-2)10 * (-3)10 using Booth's Algorithm?	a	1	6	-6	-2	-3
492	17013493	9	In Booth multiplication algorithm initially value for Q -1 ?	a	1	0	1	11	10
493	17013493	9	In Booth multiplication algorithm initially value for AC ?	a	1	0	1	11	10
494	17013493	9	In Booth multiplication algorithm if value of Q0 is 0 and value of Q -1 is 0 so what will be next step ?	a	1	ASR	A= A+M	N = N-1	A = A-M
495	17013493	9	In Booth multiplication algorithm if value of Q0 is 0 and value of Q-1 is 1 so what will be next step ?	a	1	A= A+M	ASR	A = A-M	N = N-1
496	17013493	9	In Booth multiplication algorithm if value of Q0 is 1 and value of Q-1 is 0 so what will be next step ?	b	1	N = N-1	A = A-M	ASR	A= A+M
497	17013493	9	In Booth multiplication algorithm if value of Q0 is 1 and value of Q-1 is 1 so what will be next step ?	d	1	A = A-M	N = N-1	A= A+M	ASR
498	17013493	9	In Booth Division algorithm if AC < 0 what will be next operation ?	b	1	Q0←1	Q0←0, A←A+M	COUNT ← COUNT-1	A←A+M
499	17013493	9	In Booth Division algorithm if AC > 0 what will be next step ?	d	1	COUNT ← COUNT-1	A←A+M	Q0←1 , A←A+M	Q0←1
500	17013493	9	for (7)10 × (3)10 using booth's algorithm, what will be final data in binary in accumlator for sequence count 4?	c	1	1111	1001	1100	1010
501	17013493	9	for (-9)10 × (-13)10 using booth's algorithm, what will be final data in binary in accumlator for sequence count 4?	c	1	1011	1111	10	1010
502	17013493	9	for (-5)10 × (4)10 using booth's algorithm, what will be final data in binary in accumlator for sequence count 2?	c	1	1011	1111	10	10
503	17013493	9	for (13)10 × (9)10 using booth's algorithm, what will be final value in binary in Q for sequence count 4?	d	1	11011	1111	1011	1010
504	17013493	9	for (23)10 × (-7)10 using booth's algorithm, what will be final value in binary in Q for sequence count 6?	b	1	101110	111100	111	111001
505	17013493	9	for (-7)10 × (-3)10 using booth's algorithm, what will be final value in binary in Q for sequence count 4?	b	1	1100	1110	110	1010
506	17013493	9	for (7)10 / (3)10 using booth's algorithm, what will be final data in binary in accumlator for sequence count 4 ?	b	1	10	0	1101	1011
507	17013493	9	for (11)10 / (3)10 using booth's algorithm, what will be final data in binary in accumlator for sequence count 3 ?	c	1	101	1101	10	1100
508	17013493	9	For (23)10 /(5)10 using booths restoring algorithm what will be the final value in (binary terms) Q register for sequence count 5?	a	1	1110	10110	11100	11001
509	17013493	9	for (23)10 / (5)10 using booth's algorithm, what will be final data in binary in accumlator for sequence count 3 ?	c	1	111	1101	0	1
510	17013493	9	for (23)10 / (5)10 using booth's algorithm, what will be final data in binary in accumlator for sequence count 5 ?	a	1	1	10101	110	11111
511	17013493	9	for (7)10 / (3)10 using booth's algorithm, what will be final value in binary in Q for sequence count 4 ?	a	1	1110	101	1010	11
512	17013493	9	for (11)10 / (3)10 using booth's algorithm, what will be final value in binary in Q for sequence count 3 ?	c	1	101	1101	1100	1111
513	17013493	9	For (10)10 /(3)10 using booths restoring algorithm what will be the final value in (binary terms) accumulator for sequence count 3?	a	1	10	1001	1110	1101
514	17013493	9	for (10)10 / (3)10 using booth's algorithm, what will be final value in binary in Q for sequence count 4 ?	d	1	1101	11	1010	100
515	17013493	9	Perform booth multiplication for given numbers having register size of four bits. Multiplicand : (2)10 Multiplier : (3)10 Convert final result in decimal.		5				
516	17013493	9	Perform booth multiplication for given numbers having register size of four bits. Multiplicand : (7)10 Multiplier : (3)10 Convert final result in decimal.		5				
517	17013493	9	Perform booth multiplication for given numbers having register size of four bits. Multiplicand : (7)10 Multiplier : (-3)10 Convert final result in decimal.		5				
518	17013493	9	Perform booth multiplication for given numbers having register size of six bits. Multiplicand : (-7)10 Multiplier : (3)10 Convert final result in decimal.		5				
519	17013493	9	Perform booth multiplication for given numbers having register size of six bits. Multiplicand : (-7)10 Multiplier : (-3)10 Convert final result in decimal.		5				
520	17013493	9	Perform booth multiplication for given numbers having register size of four bits. Multiplicand : (-5)10 Multiplier : (-4)10 Convert final result in decimal.		5				
521	17013493	9	Perform booth multiplication for given numbers having register size of six bits. Multiplicand : (9)10 Multiplier : (13)10 Convert final result in decimal.		5				
522	17013493	9	Perform booth multiplication for given numbers having register size of five bits. Multiplicand : (9)10 Multiplier : (-13)10 Convert final result in decimal.		5				
523	17013493	9	Perform booth multiplication for given numbers having register size of five bits. Multiplicand : (-9)10 Multiplier : (13)10 Convert final result in decimal.		5				
524	17013493	9	Perform booth multiplication for given numbers having register size of five bits. Multiplicand : (-9)10 Multiplier : (-13)10 Convert final result in decimal.		5				
525	17013493	9	Perform booth multiplication for given numbers having register size of six bits. Multiplicand : (23)10 Multiplier : (-5)10 Convert final result in decimal.		5				
526	17013493	9	Perform booth multiplication for given numbers having register size of six bits. Multiplicand : (-25)10 Multiplier : (-5)10 Convert final result in decimal		5				

527	17013493	9	Perform booth multiplication for given numbers having register size of six bits. Multiplicand : (-26)10 Multiplier : (-4)10 Convert final result in decimal.		5				
528	17013493	9	Perform booth multiplication for given numbers having register size of six bits. Multiplicand : (23)10 Multiplier : (-7)10 Convert final result in decimal.		5				
529	17013493	9	Perform booth multiplication for given numbers having register size of 6 bits: Multiplicand: (+27)10 Multiplier: (-10)10 Convert final result into decimal.		5				
530	17013493	9	Perform booth multiplication for given numbers having register size of six bits. Multiplicand : (25)10 Multiplier : (-7)10 Convert final result in decimal.		5				
531	17013493	9	Perform booth division for given numbers having register size of Four bits. Dividend : (7)10 Divisor : (3)10 Convert final result in decimal.		5				
532	17013493	9	Perform booth division for given numbers having register size of Four bits. Dividend : (10)10 Divisor : (3)10 Convert final result in decimal.		5				
533	17013493	9	Perform booth division for given numbers having register size of Four bits. Dividend : (11)10 Divisor : (3)10 Convert final result in decimal.		5				
534	17013493	9	Perform booth division for given numbers having register size of Four bits. Dividend : (14)10 Divisor : (4)10 Convert final result in decimal.		5				
535	17013493	9	Perform booth division for given numbers having register size of Five bits. Dividend : (23)10 Divisor : (5)10 Convert final result in decimal.		5				
536	17013493	9	Perform booth division for given numbers having register size of Five bits. Dividend : (23)10 Divisor : (7)10 Convert final result in decimal.		5				
537	17013493	9	Perform booth division for given numbers having register size of Five bits. Dividend : (25)10 Divisor : (7)10 Convert final result in decimal.		5				
538	17013493	9	Perform booth multiplication for given numbers having register size of four bits. Multiplicand: (-3)10 Multiplier: (+3)10 Convert final result in decimal.		3				
539	17013493	9	Perform booth division for given numbers having register size of three bits. Dividend: (6)10 Divisor: (2)10		2				
540	17013493	9	Perform booth multiplication for given numbers having register size of 6 bits: Multiplicand: (-19)10 Multiplier: (-04)10 Convert final result into decimal.		5				
541	17013493	9	Perform booth multiplication for given numbers having register size of six bits. Multiplicand : (28)10 Multiplier : (-5)10 Convert final result in decimal.		5				
542	17013493	9	Perform booth multiplication for given numbers having register size of 6 bits: Multiplicand: (+23)10 Multiplier: (-10)10 Convert final result into decimal.		5				
543	17013493	9	Perform booth multiplication for given numbers having register size of four bits. Multiplicand : (6)10 and Multiplier : (-5)10 Convert final result in decimal.		5				
544	17013493	9	Perform booth division for given numbers having register size of four bits. Dividend (6)10 and Divisor (3)10 Convert final result in decimal.		5				
545	17013493	9	Perform booth's multiplication using 6 bits having multiplicand: (-30)10 and multiplier: (7)10. Also convert result in decimal.		5				
546	17013493	9	The memory unit that communicates directly with CPU is called the .	a	1	a) Main mamory	b) secondary memory	c) cache memory	d) auxilary memory
547	17013493	9	The typical access time ratio between cache and main memory is about ?	c	1	a) 1 to 9	b)1 to 10	c) 1 to 7	d) 10 to 15
548	17013493	9	Which of the following statements is/are correct ? 1. The CPU has direct access to main memory. 2. The CPU has direct access to cache memory. 3. The CPU has direct access to auxillary memory.	d	1	a) only 1 and 3	b) only 2 and 3	c) only 1	d) only 1 and 2
549	17013493 See	9	Block size in auxillary memory typically ranges from ?	b	1	a) 248 to 256 words	b) 256 to 2048 words	c) 148 to 248 words	d) 256 to 278 words
550	17013493 See	9	Block size in cache memory typically ranges from ?	a	1	a) 1 to 16 words	b) 8 to 16 words	c) 16 to 24 words	d) 7 to 15 words
551	17013493	9	Which of the following represent ending address for a 64KB size RAM having starting address 1FFFF?	a	1	a) 2FFFE	b) 2FFFF	c) 1FFFE	d) 20000
552	17013493	9	Device that provide back-up storage are called _____ ?	d	1	a) Main mamory	b) secondary memory	c) cache memory	d) auxilary memory
553	17013493	9	A very special high speed memory called a _____ ?	c	1	a) Main mamory	b) secondary memory	c) cache memory	d) auxilary memory
554	17013493	9	In which memory design highest memory capacity and access time ?	a	1	a) Magnatics tapes	b) auxilary memory	c) secondary memory	d) cache memory
555	17013493	9	In which memory design lowest memory capacity and access time ?	b	1	a) Magnatics tapes	b) CPU Register	c) secondary memory	d) cache memory
556	17013493	9	Average access time of auxillary memory is usually___ than of main memory.	c	1	a) 10 times	b) 100 times	c) 1000 times	d) 10000 times
557	17013493	9	Which RAM is designed with flip-flop ?	b	1	a) Dynamic RAM	b) Static RAM	c) ROM	d) None of above
558	17013493	9	Which type of memory have a highest storage capacity in single memory chip?	a	1	a) Dynamic RAM	b) Static RAM	c) ROM	d) None of above
559	17013493	9	_____ is shortest read and write time.	b	1	a) Dynamic RAM	b) Static RAM	c) ROM	d) None of above
560	17013493	9	Which program is use to start computer software operating when power turn on ?	a	1	a) bootstrap loader	b) Static RAM	c) ROM	d) Dynamic RAM
561	17013493	9	_____ is non-volatile memory.	b	1	a) RAM	b) ROM	c) CPU	d) None of above

562	17013493	9	_____ is volatile memory.	a	1	a) RAM	b) ROM	c) CPU	d) None of above
563	17013493	9	Which device is used to provide backup storage ?	b	1	a) Virtual memory	b) Auxillary memory	c) Cache memory	d) Associative memory
564	17013493	9	The tracks are divided into sections is called _____	c	1	a) Seek time	b) latency time	c) Sectors	d) Sub-operation
565	17013493	9	bitas are stored in megnatize surface is called ?	b	1	a) Seek time	b) Read write head	c) ROM	d) cache memory
566	17013493	9	Which memory search time is short and critical ?	a	1	a) Associate memory	b) Auxillary memory	c) Cache memory	d) Virtual memory
567	17013493	9	Cache memory access time is times lesser than main memory.	c	1	a) 15 to 20	b) 22 to 27	c) 5 to 10	d) 20 to 28
568	17013493	9	Fast and small memory is referred as ?	c	1	a) Virtual memory	b) Auxillary memory	c) Cache memory	d) Associative memory
569	17013493	9	is placed between memory and CPU.	c	1	a) Virtual memory	b) Auxillary memory	c) Cache memory	d) Associative memory
570	17013493	9	performance of cache memory is measured in terms of quantity callled ?	a	1	a) Hit ratio	b) Miss ratio	c) Seek ratio	d) None of above
571	17013493	9	CPU refers memory, if the word is in cache, it will produce a if word not found in cache and it is in main memory then it counts as a .	b	1	a) Hit, Hit	b) hit,miss	c) Miss, Hit	d) Miss, Miss
572	17013493	9	The time taken to move the read write head to the desired track is known as .	b	1	a) latency time	b) seek time	c) data transfer rate	d) access time
573	17013493	9	The rate at which data is written to disk or read from disk is known as ?	c	1	a) latency time	b) seek time	c) data transfer rate	d) access time
574	17013493	9	Memory Access time is given by ?	b	1	a) seek time * latency time	b) seek time + latency time	c) seek time - latency time	d) seek time / latency time
575	17013493	9	Every word stored in cache there is duplicate copy in ?	a	1	a) Main mamory	b) secondary memory	c) cache memory	d) auxilary memory
576	17013493	9	In associative mapping pair replace is determine from which algorithm?	a	1	a) Replacement	b) displacement	c) location	d) None of above
577	17013493	9	Which of the given procedure is used to replace cell of cache ?	a	1	a) Round-robin	b) Robin-round	c) Robin-Robin	d) Round-Round
578	17013493	9	Word is requested from main memory it constitutes a _____ replacement policy.	d	1	a) LIFO	b) PIFO	c) SIFO	d) FIFO
579	17013493	9	In direct mapping, n-bit memory address is divided into _____ part.	b	1	a) 1	b) 2	c) 3	d) 4
580	17013493	9	The n-bits divided into 2 fields k bits for ____ and n-k bits for_____ .	c	1	a) index field , index field	b) Tag field , Tag field	c) index field , Tag field	d) None of above
581	17013493	9	Direct mapping 2k words in_____ and 2n words in _____ .	a	1	a) cache memory, Main memory	b) main Memory, Cache memory	c) SRAM	d) DRAM
582	17013493	9	In Direct mapping, ___ words in cache memory and ____ words in main memory.	c	1	a) 2x, 2y	b) 2n, 2k	c) 2k, 2n	d) 2s, 2kt
583	17013493	9	Direct Mapping the CPU address of____ bits is divided in ____ parts.	a	1	a) 15, 2	b) 14, 2	c) 20, 3	d) 15, 1
584	17013493	9	If CPU address of 15-bits, then in case of Direct mapping___ bits constitute the index field and remaining_____ bits from the tag field.	b	1	a) nine, four	b) nine, six	c) six, nine	d) nine,six
585	17013493	9	Direct mapping nine bits constitute the and remaining six bits from the _____ in case of 15-bits CPU address.	c	1	a) index field , index field	b) Tag field , Tag field	c) index field , Tag field	d) None of above
586	17013493	9	Which of the following techniques are used in associative mapping? 1) random replacement 2) first in frist out 3) last in first out 4) least recently used 5) last in last out	d	1	a) Only 3),4) and 5)	b) Only 1),2)	c) Only 1),2) and 5)	d) Only 1),2) and 4)
587	17013493	9	Main memory always contains same data as .	d	1	a) Associative Memory	b) Magnatic disc	c) Auxillary Memory	d) Cache Memory
588	17013493	9	_____ location is updated during write operation in write back.	b	1	a) Auxillary	b) Cache	c) Main	d) None of above
589	17013493	9	To overcome the slow operating speeds of the secondary memory we make use of faster flash drives.	a	1	TRUE	FALSE	-	-
590	17013493	9	What is true about memory unit?	c	1	A memory unit is the collection of storage units or devices together.	The memory unit stores the binary information in the form of bits.	Both A and B	None of the above
591	17013493	9	When when power is switched off which memory loses its data?	b	1	Non-Volatile Memory	Volatile Memory	Both A and B	None of the above
592	17013493	9	Which of the following is correct example for Auxiliary Memory?	d	1	Magnetic disks	Tapes	Flash memory.	Both A and B
593	17013493	9	Which of the following is correct refreshed rate for DRAM?	c	1	10-1000 ms	10-50 ms	10-100 ms	10-500 ms
594	17013493	9	Which of the following is true?	a	1	To overcome the slow operating speeds of the secondary memory we make use of faster flash drives.	If we use the flash drives instead of the harddisks, then the secondary storage can go above primary memory in the hierarchy.	In the memory hierarchy, as the speed of operation increases the memory size also increases.	Both A and C
595	17013493	9	_____ number of lines are required to select _____memory locations.	a	1	10, 1024	2, 2	5, 1024	5, 5K
596	17013493	9	Calculate the address lines required for 8 Kilobyte memory chip?	b	1	8	13	16	24
597	17013493	9	1 gigabyte is equal to ?	c	1	1391 megabytes	1024 kilobytes	1024 megabytes	1150 megabytes
598	17013493	9	_____ is the fastest to read from and write to than the other kinds of storage in a computer.	d	1	Floppy disk	Hard disk	CD-ROM	RAM
599	17013493	9	Which of the following is a volatile memory?	a	1	Cache memory	Hard Disk	DVD	CD
600	17013493	9	The CPU clock speed refers to the number of:	d	1	CPUs it can have	RAMs it can have	Clocks it can have	Number of cycles CPU executes per second
601	17013493	9	A 24-bit address bus has maximum accessible memory capacity of _____.	b	1	a) 64 MB	B) 16 MB	c) 1 GB	d) 4 GB
602	17013493	9	A 26-bit address bus has maximum accessible memory capacity of ____.	a	1	64 MB	16 MB	1 GB	4 GB
603	17013493	9	Which of the following memory improves the speed of execution of a program?	b	1	Primary memory	Cache memory	Secondary memory	Virtual memory
604	17013493	9	Which of the following is not a valid category of Read Only Memory (ROM)?	d	1	PROM	EPROM	EEPROM	EEEPROM
605	17013493	9	A byte is a group of ?	c	1	2 bits	4 bits	8 bits	16 bits
606	17013493	9	What will be the size of tag field (bits) for direct mapping of cache memory of 512*12 for main memory of 32K*12 size?	d	1	1	0	9	6
607	17013493	9	What will be size if index field (in bits) for direct mapping of cache memory of 64xN and main memory of 32kx12?	d	1	9	3	12	6
608	17013493	9	What will be the size of tag field (bits) for direct mapping of cache memory of 64x12 for main memory of 32Kx12 size?	a	1	9	6	15	3
609	17013493	9	Which of the following represent starting address for a 64KB size RAM having ending address 2FFFE?	b	1	0	1FFFF	FFFFE	1FFFE

610	17013493	9	Given argument register A= 11000101 and key register K= 10100000, what will be the matching pattern generated by match register (M) for following 5 words? Word 1: 11100001 Word 2: 11000001 Word 3: 11010001 Word 4: 01100111 Word 5: 01000001	d	1	0,0,1,1,1	1,0,0,0,1	1,0,0,1,0	0,1,1,0,0
611	17013493	9	Given argument register A=10100101 and key register K= 11000000, what will be the matching pattern generated by matching register (M) for following 5 words? Word 1 00111111 Word 2 10000000 Word 3 11000101 Word 4 10100101 Word 5 10011010	b	1	a) 10110	b) 01011	c) 11001	d) 11100
612	17013493	9	Given argument register A = 10101011 and key register K = 10001101, what will be the matching pattern generated by match register (M) for following 5 words ? Word 1 : 10010110 Word 2 : 10100010 Word 3 : 10011011 Word 4 : 10011001 Word 5 : 11001001	d	1	a) 0,1,1,1,0	b) 1,0,0,1,1	c) 1,0,0,0,1	d) 0,0,1,1,1
613	17013493	9	Which type of memory avoids address based search?	c	1	RAM	DRAM	CAM	ROM
614	17013493	9	Match the following pair: 1. Auxiliary memory — x. SRAM 2. Cache Memory — y. bootstrap loader 3. Read Only Memory — z. Magnetic disks/tapes 4. Main Memory — w. DRAM	b	1	1-y, 2-z, 3-x, 4-w	1-z, 2-x, 3-y, 4-w	1-z, 2-x, 3-w, 4-y	1-Z, 2-y, 3-x, 4-w
615	17013493	9	In Auxiliary Memory; the average time required to reach a storage location in memory and obtain its contents is called_____ time and it consists of a _____ time required to position the read-write head to a location and a _____ time required to transfer data to or from the device.	a	1	Access, Seek, Transfer	Access, Seek, Storage	Rising, Seek, Transfer	Storage, Access, Transfer
616	17013493	9	If starting address of ROM is 8000 H and ending address is FFFF H then size of ROM is _____	a	1	32 k	4 k	16 k	24 k
617	17013493	9	The main memory is 8K x 9 and cache memory is 256 x 9 in associative mapping. What is the size of argument register?	a	1	13	8	12	512
618	17013493	9	Which of the following refers to the associative memory?	b	1	the address of the data is generated by the CPU	the address of the data is supplied by the users	there is no need for an address i.e. the data is used as an address	the data are accessed sequentially
619	17013493	9	A microprocessor based system uses 4K x 8 bit RAM whose starting address (AA00) H. The ending address will be _____	c	1	a) B00F	b) A0001	c) B9FF	d) C9FF
620	17013493	9	Choose the correct statement/s from following . 1. Disadvantage of direct mapping is that 2 word with same index in their address but different tag value can not reside in cache memory at same time. 2. Set associative mapping in which each word of cache can store two or more word of memory under same index address. 3. The number of bits in index field is equal to number of address bit required to accessed the cache memory.	d	1	1, 3 only	1 only	2 only	1, 2, 3
621	17013493	9	_____ memory is also known as content addressable memory (CAM)	c	1	dynamic RAMs	static RAMs	associative memory	cache memory
622	17013493	9	Design memory address map for four 64 * 8 RAM and two 128 * 8 ROM. Take starting address map as 0000 H.		3				
623	17013493	9	Given RAM of 32KB size having starting address 8000 H find ending address.		3				
624	17013493	9	Show memory interfacing with CPU along with memory address map for one 128*8 RAM and one 512*8 ROM using chip select pins. Take starting address map as 0840 H.		3				
625	17013493	9	Show memory interfacing with CPU along with memory address map for one 128*8 RAM and one 512*8 ROM using chip select pins. Take starting address for memory address map as 0180H.		3				
626	17013493	9	Show memory interfacing with CPU along with memory address map for two 128*8 RAM and one 512*8 ROM using chip select pins. Take starting address for memory address map as 0100 H.		3				
627	17013493	9	Show memory interfacing with CPU along with memory address map for four 128*8 RAM and one 512*8 ROM using chip select pins. Take starting address map as 0000 H.		3				
628	17013493	9	Show memory interfacing with CPU along with memory address map for Two 512*8 RAM and Two 512*8 ROM using chip select pins. Take starting address map as 0000 H. Consider CPU is having 16 bit address line and 8 bit data line.		4				
629	17013493	9	Show memory interfacing with CPU having 2 RAM chips of size 128*8 and 1 ROM chip of size 256*8 with a starting address of 6000 H. (H represents hexadecimal representation).		3				
630	17013493	9	Given RAM of 64KB size having starting address 00000 H find ending address.		3				
631	17013493	9	Given RAM of 32KB size having starting address 00000 H find ending address.		3				
632	17013493	9	Given RAM of 64KB size having starting address FFFF H find ending address.		3				
633	17013493	9	Given RAM of 32KB size having starting address FFFF H find ending address.		3				
634	17013493	9	If starting address of ROM is 3000 H having 1K size find ending address .		3				
635	17013493	9	Given RAM of 4K byte size having starting address 0000 H find ending address.		3				
636	17013493	9	Given RAM of 1K byte size having starting address 2000 H find ending address.		3				
637	17013493	9	Given RAM of 32KB size having starting address 1234 H find ending address.		3				
638	17013493	9	Static RAM (SRAM) is faster than Dynamic RAM (DRAM) because .	c	1	SRAM uses capacitors	SRAM is costlier	SRAM does not require refreshing	SRAM is cheaper
639	17013493	9	refers to the amount of time required to position the read - white head of a hard disk on appropriate sector.	a	1	Seek time	Rotational latency	Access time	Load time
640	17013493	9	A hard disk is divided into tracks which are further subdivided into ?	b	1	clusters	sectors	vectors	heads
641	17013493	9	How many 128 × 8 RAM chips are needed to provide a memory capacity of 2048 bytes?	d	1	2	8	4	16
642	17013493	9	Which of the following sets of words best describes the characteristics of a primary storage device, like RAM.	c	1	Cheap, non-volatile, fast access	Volatile, expensive, slow access	Expensive, volatile, fast access	Fast access, non-volatile, cheap
643	17013493	9	Which of the following memories must be refreshed many times per second?	b	1	Static RAM	Dynamic RAM	EPROM	ROM
644	17013493	9	A computer uses RAM chips of 1024 × 1 capacity. How many chips are needed to provide memorycapacity of 16K bytes?	d	1	8	16	1024	128
645	17013493	9	How many 16 K × 1 RAM chips are needed to provide a memory capacity of 256 K-bytes?	d	1	8	32	64	128
646	17013493	9	How many 32 K × 1 RAM chips are needed to provide a memory capacity of 256 K-bytes ?	c	1	8	32	64	128
647	17013493	9	Among the following the volatile memory is	b	1	Bubble memory	RAM	ROM	Magnetic disc

648	17013493	9	How many 128 × 8 RAM chips are needed to provide a memory capacity of 2048 bytes?	d	1	2	8	4	16
649	17013493	9	Which of the following technology can give high speed RAM?	b	1	TTL	CMOS	ECL	NMOS
650	17013493	9	Consider the following statements regarding memory: 1. Integrated circuit RAM chips are available in both static and dynamic modes. 2. The dynamic RAM stores the binary information in the form of electric charges that are applied to capacitors. 3. The static RAM is easier to use and has shorter read and write cycles. 4. RAM and ROM chips are not available in a variety of physical sizes. Which of the above statements are correct ?	a	1	1 and 2 only	1, 3 and 4 only	2, 3 and 4 only	1, 2, 3 and 4
651	17013493	9	What is the formula for Hit Ratio?	a	1	Hit/(Hit + Miss)	Miss/(Hit + Miss)	(Hit + Miss)/Miss	(Hit + Miss)/Hit
652	17013493	9	If cache has 51 hits and 3 misses over a period of time. What will be hit and miss ratio of cache ?	c	1	a) 10%, 90%	b) 6%, 94%	c) 94%, 6%	d) 90%, 10%
653	17013493	9	If cache has 55 hits and 45 misses over a period of time. What will be hit and miss ratio of cache ?	c	1	a) 55%, 65%	b) 45%, 55%	c) 55%, 45%	d) 55%, 55%
654	17013493	9	If cache has 89 hits and 71 misses over a period of time. What will be hit and miss ratio of cache ?	c	1	a) 55%, 65%	b) 45%, 55%	c) 55%, 45%	d) 55%, 55%
655	17013493	9	If cache has 25 hits and 75 misses over a period of time. What will be miss and hit ratio of cache?	b	1	a) 25%, 75%	b) 75%, 25%	c) 55%, 45%	d) 55%, 55%
656	17013493	9	If cache has 76 hits and 34 misses over a period of time. What will be hit and miss ratio of cache?	a	1	69 %, 31%	76 %, 34%	31 %, 69%	50 %, 50%
657	17013493	9	A cache is accessed by Mark 89 times. From which Mark is only not able to found data 49 times. What is the Hit and Miss Ratio (%) of mark accessing the cache memory?	a	1	45%, 55%	55%, 55%	55%, 50%	49%, 40%
658	17013493	9	Which of the following statements are not correct about cache memory?	d	1	Cache memory is used to store data temporarily.	It holds that data and program which has to be executed within a short	It consumes less access time as compared to the RAM.	All are true
659	17013493	9	If cache has 69 hits and 44 misses over a period of time. What will be hit and miss ratio of cache?	b	1	39 %, 61 %	61%, 39%	69%, 44%	44%, 69%
660	17013493	9	A cache is accessed accessed by mark 73 times, from which mark is only able to found data 49 times. What is the hit and miss ratio (%) of mark accessing the cache memory ?	c	1	a) 77%, 33%	b) 33%, 77%	c) 67%, 33%	d) 33%, 67%
661	17013493	10	Input or output devices that are connected to computer are called	b	1	Input/Output Subsystem	Peripheral Devices	Interfaces	Interrupt
662	17013493	10	The main functions of input-output interface circuits is / are -	d	1	Data conversion	synchronization	device selection	all a,b and c
663	17013493	10	The process of matching of operating speeds of CPU and other peripherals is known as -	b	1	Data conversion	synchronization	device selection	cycle stealing
664	17013493	10	A special synchronization hardware which is required between CPU and peripherals called	a	1	Interface Unit	Memory Unit	Processor	Accumulator
665	17013493	10	I/O bus consists of -	d	1	data lines	address lines	control lines	all a,b and c
666	17013493	10	Which of the following is/are correct regarding I/O bus? (a) The I/O bus from the processor is attached to all peripheral interfaces. (b) I/O bus consists of data lines and control lines only (c) I/O bus is used for the selection of I/O devices by CPU	c	1	only 1 and 2	only 2	only 1	All 1, 2 and 3
667	17013493	10	How many types of commands that an interface may receive?	c	1	2	3	4	5
668	17013493	10	Which of the given command is not a valid command for I/O interface?	d	1	Status command	control command	Data output command	Interrupt command
669	17013493	10	Which I/O command is issued to rewind the magnetic tape or to start the tape moving in the forward direction?	b	1	Status command	control command	Data output command	Data input command
670	17013493	10	In which case the interface receives an item of data from the peripheral and places it in its buffer register?	d	1	Status command	control command	Data output command	Data input command
671	17013493	10	The control lines which are enabled during a memory transfer are -	a	1	memory read and memory write	I/O read and I/O write	Interrupt enable and disable	both a and b
672	17013493	10	In which configuration only one set of read and write signals employed ?	a	1	Memory mapped I/O	Isolated I/O	Interrupt Initiated I/O	both a and b
673	17013493	10	Match the following: 1. Skip next instruction if flag is set. P - Data input command 2. Read interface status register. Q - Control command 3. Move printer paper to beginning of next page. R - Status command	c	1	1-P, 2-Q, 3-R	1-Q, 2-P, 3-R	1-R, 2-P, 3-Q	1-P, 2-R, 3-Q
674	17013493	10	Indicate whether following constitute control, status or data transfer command 1. skip the next instruction if flag is set 2. seek a given record on magnetic disk	b	1	control, status	status, control	control, control	status, status
675	17013493	10	In memory-mapped I/O	a	1	The I/O devices and the memory share the same address space	The I/O devices have a separate address space	The memory and I/O devices have an associated address space	A part of the memory is specifically set aside for the I/O operation
676	17013493	10	Which type of instructions are used by Computers with memory-mapped I/0 to access I/0 data?	b	1	Register type	Memory type	I/O type	none of the above
677	17013493	10	Which of the given mapping technique will provide simpler hardware, simple instruction set and provides all addressing modes? (i) Memory mapped I/O (ii) Isolated I/O	c	1	Both (i) and (ii)	Only (ii)	only (i)	Neither (i) nor (ii)
678	17013493	10	Which of the following is not an advantage of memory mapped technique? (i) Simple hardware (ii) Simple Instruction Size (iii) All address modes available (iv) More memory address space	b	1	(i), (iv) only	(iv) only	(i), (ii), (iii) only	(iii), (iv) only
679	17013493	10	In which mode of transfer, each data transfer is initiated by an instruction in the program?	a	1	Programmed I/O	DMA	Interrupt initiated I/O	None
680	17013493	10	Choose the correct option/s from the following regarding programmed I/O mode of transfer. (i) CPU stays in a program loop until the I/O unit indicates that it is ready for data transfer. (ii) Processor keeps busy needlessly in programmed I/O mode (iii) An interrupt facility is used to issue an interrupt request when data is available from the device.	a	1	All 1, 2 and 3	only 1 and 2	only 2	only 1 and 3
681	17013493	10	The advantage of I/O mapped devices to memory mapped is	c	1	The former offers faster transfer of data.	The devices connected using I/O mapping have a	The devices have to deal with fewer address lines.	None
682	17013493	10	Which of the following I/O transfer mode uses polling method ?	a	1	programmed I/O	intruppt initiative I/O	DMA initiated	Priority Interrupt
683	17013493	10	If the register in the interface share a common clock with the CPU register, the transfer between the two units is said to be...	b	1	DMA transfer	synchronous transfer	asynchronous transfer	write back
684	17013493	10	What is/are the drawback/s of programmed I/O type data transfer method?	d	1	CPU involvement	Wasted CPU cycles	No parallelism	All a, b and c
685	17013493	10	Priority is provided by _____ for access to memory by various I/O channels and processors.	c	1	a register	a counter	a controller	the processor scheduler
686	17013493	10	Which of the following statement/s is/are correct? (a) Keyboard and Mouse Comes under output periferal devices. (b) The method which offers higher speeds of I/O transfers is DMA (c) The data transfer rate of peripherals is usually slower than the transfer rate of the CPU	b	1	Only a and b	only b and c	only a	only c

687	17013493	10	Which mode of tranfer has time consuming transfer process as CPU monitors peripheral devices constantly?	a	1	Programmed I/O	Interrupt I/O	DMA	Both a and b
688	17013493	10	Which of the following statement is / are incorrect ? 1. memory mapped I/O shares common instruction set for both memory and I/O 2. control command test various flag conditions of I/O peripherals. 3. Handshaking is used for synchronous data transfer 4. I/O mapped I/O uses separate memory or I/O R/W lines	c	1	all 1,2,3,4	Only 1 and 4	only 2 & 3	only 3
689	17013493	10	Which of the following is true about DMA? 1.DMA is an approach of performing data transfers in bulk between memory and the external device without the intervention of the processor 2. The DMA controller acts as a processor for DMA transfers and overlooks the entire process 3.The DMA controller has 3 registers.	a	1	All 1, 2 and 3	only 1 and 2	only 2	only 1 and 3
690	17013493	10	The CPU activities the_____output to inform the external DMA that the buses are in the high-impedance state.	b	1	Bus request	bus grant	cycle stealing	none of these
691	17013493	10	In which mode, the I/O module and main memory exchange data directly, without processor involvement ?	a	1	DMA	Programmed I/O	Interrupt I/O	both b and c
692	17013493	10	During DMA transfer, the DMA controller takes over the buses to manage the transfer -	d	1	Directly from CPU to memory	Directly from memory to CPU	Directly between the memory and registers	Directly between the I/O device and memory
693			_____input is used by DMA controller to request the CPU to hand over the control of buses.	d	1	Interrupt I/O	programmed I/O	Bus Grant	Bus Request
694	17013493	10	The term “cycle stealing” refers to:	c	1	Interrupt-based data transfer	Polling mode data transfer	DMA-based data transfer	Clock cycle overriding
695	17013493	10	Which type of register specifies the mode of transfer in DMA controller?	b	1	Address register	control register	word count register	Status register
696	17013493	10	In which type of data transfer method , the CPU is in idle & has no control of memory bus	c	1	programmed I/O	intruppt initiative I/O	DMA transfer	Priority Interrupt
697	17013493	10	The DMA transfer is initiated by ____.	d	1	Processor	Processor	OS	I/O devices
698	17013493	10	How many types of modes of I/O Data Transfer?	d	1	2	4	5	3
699	17013493	10	In which mode of transfer, interrupt request is initiated when the data is available from the device?	b	1	Programmed I/O	Interrupt I/O	DMA	Both a and b
700	17013493	10	In case of Data transfer between two independent units, where internal timing in each unit is independent from the other is known as _____ data transfer.	b	1	Synchronous	Asynchronous	Control	None
701	17013493	10	Choose the correct statement/s: 1. The strobe may be activated by either the source or the destination unit 2. The source removes the data from the bus before that it disables its strobe pulse. 3. One of the Disadvantages of the strobe method is Source unit that initiates the transfer has no way of knowing whether the destination unit has actually received the data item that was placed in the bus.	d	1	Only 1	Only 3	All 1, 2, 3	Both 1 and 3
702	17013493	10	By the help of_____ method we can solve the problem of strobe method.	c	1	IOP	Direct	handshaking	Indirect
703	17013493	10	In the programmed I/O method, the I/O device does not have direct access to	b	1	CPU	Memory	register	none
704	17013493	10	The method which offers higher speeds of I/O transfers is	d	1	Interrupt	Memory mapping	Programmed Control I/O	DMA
705	17013493	10	The DMA transfers are performed by a control circuit called as	a	1	DMA Controller	Memory unit	Control unit	CPU
706	17013493	10	Which register is not a part of DMA controller?	d	1	Address register	control register	word count register	Status register
707	17013493	10	Which of the following value will be passed to (PI, PO) of each device in sequence if interrupt request is generated by third device in a daisy chain priority arrangement?	c	1	(1,0),(0,0),(0,0)...	(1,1),(1,1),(0,1),...	(1,1),(1,1),(1,0),...	(0,0),(0,0),(0,1),...
708	17013493	10	Removing the CPU from the path and letting the peripheral device manage the memory buses directly would improve the speed of transfer. This technique is known as	d	1	Programmed I/O	Interrupt I/O	priority interrupt	DMA
709	17013493	10	Which of the register of DMA controller is incremented after transferring each word to memory?	a	1	Address register	control register	word count register	Status register
710	17013493	10	Which of the register of DMA controller is decremented after transferring each word to memory?	c	1	Address register	control register	word count register	Status register
711	17013493	10	In which mode of transfer CPU is idle and has no control of the memory buses?	c	1	Programmed I/O	Interrupt I/O	DMA transfer	priority interrupt
712	17013493	10	The method of accessing the I/O devices by repeatedly checking the status flags is	a	1	Programmed I/O	Memory mapped I/O	I/O Mapped	None
713	17013493	10	The process wherein the processor constantly checks the status flags is called as	a	1	Polling	Inspection	Reviewing	Echoing
714	17013493	10	Match the columns: **Units** / **Activities** a) Input unit — i) Executes instructions b) Output unit — ii) Receives data for processing c) Memory unit — iii) Displays computed result d) Processing unit — iv) Stores programs and computed values	d	1	(a,ii), (b,iv), (c,iii), (d,i)	(a,ii), (b,iii), (c,i), (d,iv)	(a,iii), (b,ii), (c,iv), (d,i)	(a,ii), (b,iii), (c,iv), (d,i)
715	17013493	10	Choose the correct statement/s: 1. The strobe may be activated by either the source or the destination unit 2. The source removes the data from the bus before that it disables its strobe pulse. 3. One of the Disadvantages of the strobe method is Source unit that initiates the transfer has no way of knowing whether the destination unit has actually received the data item that was placed in the bus.	d	1	Only 1	Only 3	All 1, 2, 3	Both 1 and 3
716	17013493	10	On receiving an interrupt from an I/O device, the CPU	b	1	halts for predetermined time	branches off to the interrupt service routine after	branches off to the interrupt service routine immediately.	hands over control of address bus and data bus to the
717	17013493	10	Which of the following is not considered as a peripheral device?	a	1	CPU	Key board	Mouse	all of the given
718	17013493	10	The method of synchronizing the processor with the I/O device in which the device sends a signal when it is ready is_____	d	1	Exceptions	Signal Handling	DMA	Interrupts
719	17013493	10	Which of the following value will be passed to (PI, PO) of each device in sequence if interrupt request is generated by fourth device in a daisy chain priority arrangement?	c	1	(1,1),(1,1),(0,1),(0,1)...	B) (1,1),(1,1),(1,0),(0,1)...	(1,1),(1,1),(1,1),(1,0)...	(1,1),(1,1),(1,1),(0,1)...
720	17013493	10	Which type of I/O command is used for moving printer paper to beginning of next page?	a	1	Control command	status command	Data input command	None
721	17013493	10	If the registers in the interface share a common clock with the CPU registers, the transfer between the two units is said to be -	a	1	Synchronous data transfer	Asynchronous data transfer	Common data transfer	None of these
722	17013493	10	Which of the given methods are asynchronous data transfer method?	d	1	Handshaking Method	Strobe Pulse Method	cycle stealing	both a and b
723	17013493	10	Identify the type of command if user starts moving a magnetic tape in forward direction	b	1	status command	control command	data output command	data input command
724	17013493	10	In which method there is no acknowlegement received for placing the data on bus by source?	a	1	Strobe method	Asynchronous data transferring	Handshaking	synchronous data transferring
725	17013493	10	In case of Data transfer between two independent units, where internal timing in each unit is independent from the other is known as _____ data transfer.	b	1	Synchronous	Asynchronous	Control	None
726	17013493	10	What is the correct sequence for destination initiated handshaking data transfer? 1. Place data on data bus & Enable data valid. 2. Data valid disable and invalidate the data. 3. Ready for data. Enable ready for data. 4. Accept data from bus. Disable data ready for bus.	a	1	3,1,4,2	3,1,2,4	3,2,4,1	4,3,2,1

727	17013493	10	Which of the following sequence is correct for source-initiated transfer using handshaking? 1.Accept data from bus.Enable data accepted 2. Disable data accepted.ready to accept data(initial state) 3. Place data on bus.Enable data valid. 4. Disable data valid.invalidate data on bus.	d	1	1-2-3-4	4-3-2-1	3-4-2-1	3-1-4-2
728	17013493	10	Which of the following value will be passed to (PI, PO) of each device in sequence if interrupt request is generated by first device in a daisy chain priority arrangement?	a	1	(1,0), (0,0), (0,0) ...	(1,1), (0,0), (0,0) ...	(1,1), (1,1), (1,0), ...	(0,1), (0,0), (0,1), ...
729	17013493	10	_____ method is used to establish priority by serially connecting all devices that request an interrupt in which 0 will pass the signal only if it has_____	a	1	Daisy chain, No interrupt request	Daisy chain, interrupt request	Polling, No interrupt request	Polling, interrupt request
730	17013493	10	Which of the following value will be passed to (PI,PO) of each device in sequence if interrupt request generated by second device in a daisy chain priority arrangement ?	a	1	(1,1),(1,0),(0,0)...	(1,1),(1,0),(0,1)...	(1,1),(0,0),(0,1)...	(0,0),(1,0),(0,0)...
731	17013493	10	Create Daisy Priority Chain diagram for following devices with priority in descending order as Mouse, Keyboard, Printer. Assume all necessary required signals.		1				
732	17013493	10	What is the difference between isolated and memory-mapped I/O?		2				
733	17013493	10	Why are the read and write control lines in a DMA controUer bidirectional? Under what condition and for what purpose are they used as inputs? Under what condition and for what purpose are they used as outputs?		2				
734	17013493	10	Draw the timimg signals of source initiated strobe for data transfer.		2				
735	17013493	10	Draw the timimg signals of destination initiated strobe for data transfer.		2				
736	17013493	10	Enlist the sequence of events occured in source initiated transfer using handshaking.		2				
737	17013493	10	Draw the timimg diagram of destination initiated handshaking for data transfer.		2				
738	17013493	10	Draw the timimg diagram of source initiated handshaking for data transfer.		2				
739	17013493	10	Draw the timing diagram and mention sequence of events for a type asynchronous data transfer in which the source unit does not place data on the bus until after it receives the Ready for data signal from the destination unit.		5				