Programme/Class: **Diploma**	Year: **Second**	Semester: **Fourth**
Subject: **Computer Science**		
Course Code: B070401T	Course Title: **Computer System Architecture**	

Course outcomes:

The student will be able to understand the basic arithmetic of a Computer System; how the data is represented, how the various operation are performed on the data, the basic circuits to perform these operations, how instructions are formatted and how these instructions are executed to accomplish a particular operation. Student can also learn the organization of the peripheral devices, the interface between these devices to the system. Student can also understand the architecture of a basic computer, its registers, bus system and the interaction flow among them.

Credits: **4**	**Core Compulsory**
Max. Marks: **25+75**	Min. Passing Marks:

Total No. of Lectures-Tutorials-Practical (in hours per week): **4-0-0**

Unit	Topic	No. of Lectures
I	**Data Representation and basic Computer Arithmetic:** Number systems, complements, fixed and floating point representation, character representation, addition, subtraction, magnitude comparison.	7
II	**Logic gates and circuits:** logic gates, boolean algebra, combinational circuits, circuit simplification, introduction to flip-flops and sequential circuits, decoders, multiplexers, registers, counters.	8
III	**Basic Computer Organization and Design:** Computer registers, bus system, instruction set, timing and control, instruction cycle, memory reference, input-output and interrupt.	7
IV	**Central Processing Unit:** Register organization, arithmetic and logical micro-operations, stack organization, Hardwired vs. micro programmed control. Pipeline control: Instruction pipelines, pipeline performance, super scalar processing, Pipelining, RISC & CISC	8
V	**Programming the Basic Computer:** Instruction formats, addressing modes, instruction codes, assembly language	7
VI	**Memory Organization:** Memory device characteristics, random access memories, serial access memories, Multilevel memories, address translation, memory allocation, Main features, address mapping, structure versus performance.	8
VII	**Input-output Organization:** Peripheral devices, I/O interface, Modes of data transfer: Programmed, Interrupt Driven and Direct Memory Access.	

VIII	**Parallel processing:** Processor-level parallelism, multiprocessor architecture	7

Suggested Readings:

1. M. Mano, "Computer System Architecture", Pearson Education, New Jersey, 2017,Third Edition.
2. W. Stallings, "Computer Organization and Architecture Designing for Performance",Prentice Hall of India, 2015, Tenth Edition.
3. M. Mano, "Digital Design", Pearson Education, New Jersey, 2018, Sixth Edition.
4. Vranasic and Hamacher, Computer Organization, TMH"

This course can be opted as an elective by the students of following subjects:
B.Sc. in Electronics, B.Sc. in Physics, B.Sc. in Engineering, BCA, B.E, B.Tech.

Suggested Continuous Evaluation Methods:

1. **Assessment Type: Class Tests (Max. Marks 14)**
   Suggested Usage:
   Include all types of questions-essay, short answer, objective; Design to test all levels of domain; Exam Blue Print be prepared to ensure inclusion of all types & levels of questions and proper sampling of content; Marking Criteria made known to students; Teacher should provide written feedback selectively and discuss answers in the class; Only Role/Code numbers , not names be written to avoid bias in marking; Display of model answer copies.

   After Completion of Unit I and Unit II, a first class test of max. marks of 7 shall be conducted.
   After Completion of Unit III and IV, a second class test of max. marks of 7 shall be conducted.
   If any student does not appear in any one or both class test, a makeup test shall be conducted of max. marks of 5 instead of total 14 marks.

2. **Assessment Type: Quizzes/ Objective Tests / Recognition Type (such as MCQs; True or False; Matching; Classifying) /Recall Type -Filling Blanks; One word / Phrase Answers (Max Marks: 5)**

   Suggested Usage: Teachers be trained in construction, advantages, disadvantages and precautions while preparing different types of objective items; Go beyond factual information to High Order Thinking (HOT) Skills. It shall be "End of the class quiz".

3. **Assessment Type: Assignments (Max Marks: 4)**

Programme/Class: **Diploma**	Year: **Second**	Semester: **Fourth**
Subject: **Computer Science**		
Course Code: B070402P	Course Title: Computer System Architecture Lab	

Course outcomes:
An ability to understand:

CO1 The functions of various hardware components and their building blocks
CO2 Boolean algebraic expressions to digital design
CO3 And implementation of different sequential and Combinational circuits
CO4 computer buses and input/output peripherals
CO5 memory hierarchy and design of primary memory

Credits: **2**	Max. Marks: **25+75**	Min. Passing Marks:

Total No. of Lectures-Tutorials-Practical (in hours per week): **0-0-4**

Practical: 60 Lab Periods

Memory	Instruction format
4096 words 16 bits per word	0 3 4 15 Opcode | Address

Basic Computer Instructions

Memory Reference	Register Reference	Input-Output

1. Create a machine based on the following architecture:

Register Set

IR	DR	AC	AR	PC	FGI	FGO	S	I	E
0 15	0 15	0 15	011	011	1 Bit	1 Bit	1 Bit	1 bit	1 Bit

Symbol	Hex		Symbol	Hex	Symbol	Hex
AND	0xxx		CLA	E800	INP	F80 0
ADD	2xxx		CLE	E400	OUT	F40 0
ISZ	Cxxx		INC	E020		

AND_I	1xxx		SPA	E010		
ADD_I	3xxx		SNA	E008		
LDA_I	5xxx	Indirect	SZA	E004		
STA_I	7xxx	Addressing	SZE	E002		
BUN_I	9xxx		HLT	E001		
BSA_I	Bxxx					
ISZ_I	Dxxx					

Refer to Chapter-5 of Morris Mano for description of instructions.

ii) Create the micro operations and associate with instructions as given in the chapter (except interrupts). Design the register set, memory and the instruction set. Use this machine for the assignments of this section.

iii) Create a Fetch routine of the instruction cycle.

iv) Simulate the machine to determine the contents of AC, E, PC, AR and IR registers in hexadecimal after the execution of each of following register reference instructions:

a. CLA
b. CLE
c. CMA
d. CME
e. CIR
f. CIL
g. INC
h. SPA
i. SNA
j. SZA
k. SZE
l. HLT

Initialize the contents of AC to $(A937)_{16}$, that of PC to $(022)_{16}$ and E to 1.

5. Simulate the machine for the following memory-reference instructions with I= 0 and address part = 082. The instruction to be stored at address 022 in RAM. Initialize the memory word at address 082 with the operand B8F2 and AC with A937. Determine the contents of AC, DR, PC, AR and IR in hexadecimal after the execution.

a. ADD
b. AND
c. LDA
d. STA
e. BUN
f. BSA
g. ISZ

6. Simulate the machine for the memory-reference instructions referred in above question with I= 1 and address part = 082. The instruction to be stored at address 026 in RAM. Initialize the memory word at address 082 with the value 298. Initialize the memory word at address 298 with operand B8F2 and AC with A937. Determine the contents of AC, DR, PC, AR and IR in hexadecimal after the execution.

7. Modify the machine created in Practical 1 according to the following instruction format: