RGPVNOTES.IN

Program : **B.Tech**

Subject Name: **Digital Systems**

Subject Code: **CS-304**

Semester: **3rd**

Subject Notes

UNIT-IV

Introduction to A/D & D/A convertors & their types, sample and hold circuits, Voltage to Frequency & Frequency to Voltage conversion. Multivibrators :Bistable, Monostable, Astable, Schmitt trigger, IC 555 & Its applications. TTL, PMOS, CMOS and NMOS logic. Interfacing between TTL to MOS.

ANALOG TO DIGITAL CONVERTER (ADC):

Figure 4.1 shows the general block diagram of ADC. An ADC takes an analog input voltage and after a certain amount of time produces a digital output code that represents the analog input.

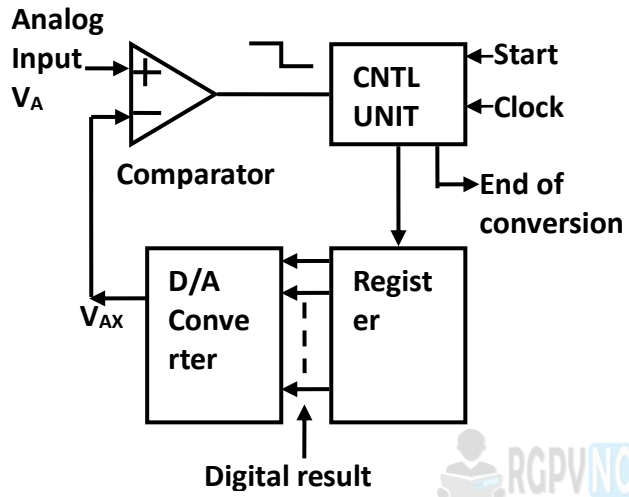


Figure 4.1: General block diagram of ADC

Timing for operation is provided by the input clock signal.

Control (CNTL) unit contains the logic circuitry for generating the proper sequence of operations in response to the start command, which initiates the conversion process.

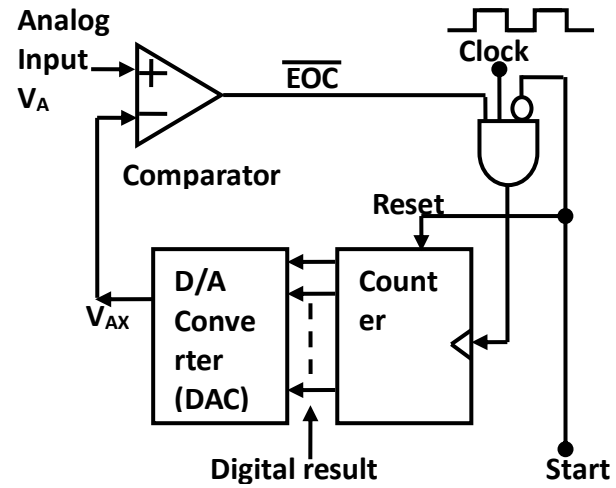
OPAMP comparator has two analog inputs and a digital output that switches states, depending upon which analog input is greater.

Operation: START command pulse initiates the operation. At a rate determined by the clock, the control unit continually modifies the binary number that is stored in register. The binary number in register is converted into analog voltage, V_{AX}, by DAC. The comparator compares V_{AX} with V_A. When $V_{AX} < V_A$, comparator output stays HIGH. When $V_{AX} > V_A$, by atleast an amount equal to threshold voltage, the comparator output goes LOW and stops the process of modifying the register number. At this point V_{AX} is close approximation with V_A.

The digital number in the register, which is the digital equivalent of V_{AX}, is also the digital equivalent of V_A, within the resolution and accuracy of the system. The control logic activates the end of conversion signal, when the conversion is complete.

DIGITAL RAMP ADC (COUNTER TYPE ADC):

Figure 4.2 shows the diagram of digital ramp ADC.



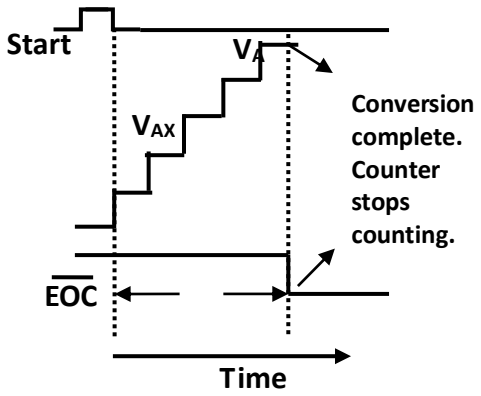


Figure 4.2: Digital Ramp ADC

Operation: Assume that V_A is positive. START pulse is applied to RESET the counter to 0 and AND gate is disabled. With all 0s as its input, DAC output will be V_{AX} = 0v. Since $V_{AX} < V_A$, comparator output, (EOC)', is HIGH. When START is LOW, AND gate is enabled and clock pulses get through to the counter. As the counter advances, DAC output, V_{AX}, increases one step at a time. This continues until $V_{AX} > V_A$ by an amount equal or greater than threshold voltage (typically 10 to 100µv). At this point comparator output, (EOC)', goes LOW and counter stop counting. The conversion process is now complete and the contents of the counter are the digital representation of V_A. Counter will hold the digital value until the next START pulse initiates a new conversion.

Conversion time, Tc, is the interval between the end of the START pulse and the activation of the (EOC)' output. Tc depends upon V_A.

For N-bit converter: $Tc_{(max)} = (2^N - 1)$ clock cycles. $Tc_{(avg)} = Tc_{(max)} / 2$ clock cycles.

Major disadvantage of digital ramp ADC is that it is not suitable for where the repetitive A/D conversion of a fast changing analog signal occurs. In this method the conversion time essentially doubles for each bit that is added to the counter.

SUCCESSIVE-APPROXIMATION ADC (SAC):

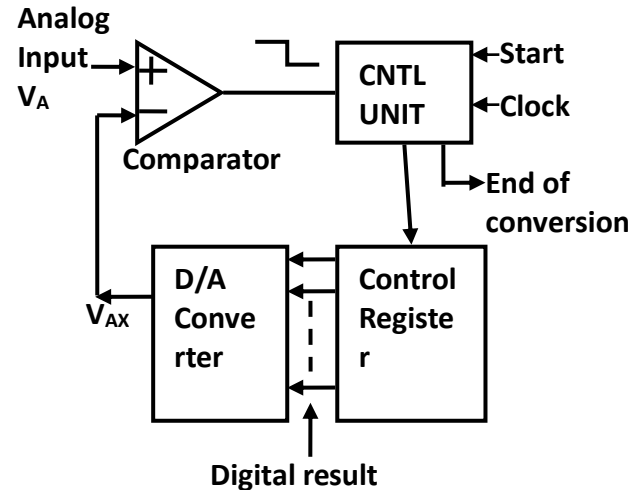
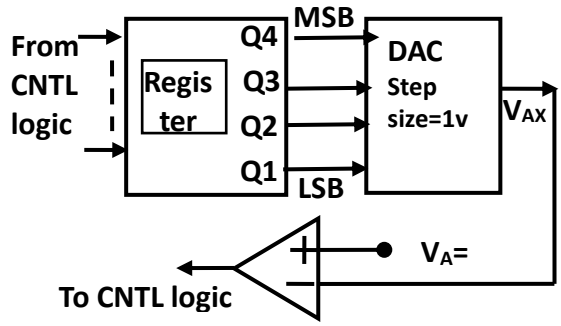


Figure 4.3: General block diagram of SAC

Figure 4.3 shows the general block diagram of SAC. Basic arrangement is similar to digital ramp ADC except that, instead of counter SAC uses a control register. The control logic modifies the contents of the register bit by bit until the register data are the digital equivalent of the analog input V_A within the resolution of the converter.

Most widely used ADC. Circuitry is more complex but much shorter conversion time

Operation of 4-bit SAC using DAC step size of 1Volt and V_A = 10.4 Volts:



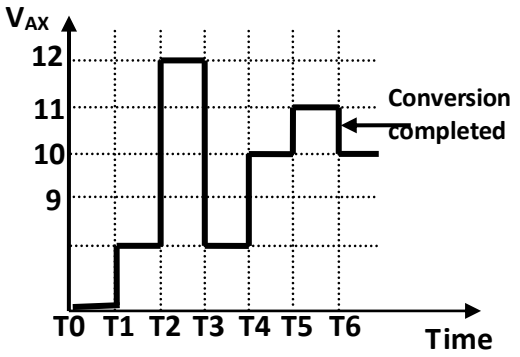


Figure 4.4: 4-bit SAC using step size 1V

Operation: Figure 4.4 shows the 4-bit SAC using DAC step size of 1Volt. Let assume that the analog input is V_A=10.4V.

At time T0, V_{AX} = 0V, i.e $V_A > V_{AX}$, comparator output is HIGH. Control logic clearing all bits so, Q3=Q2=Q1=Q0=0 ie [Q]= 0000.

At time T1, control logic (CNTL) sets MSB = 1. So [Q]= 1000. This produces V_{AX} = 8V. Since, $V_A > V_{AX}$, comparator output is HIGH. This HIGH tells the CNTL logic that the setting of MSB did not make V_{AX} exceeds V_A, so that MSB is kept at 1.

Now, CNTL logic proceeds to next lower bit, Q2. Q2=1 to produce [Q] = 1100 and V_{AX} = 12V at time T2. Since $V_{AX} > V_A$, comparator output goes LOW. The value of V_{AX} is too large, so CNTL logic then clears register contents back to 1000 ie V_{AX} = 8V. Thus, at T3, V_{AX} = 8V.

At time T4, CNTL logic sets the next lower bit Q1 = 1, ie [Q] = 1010 and V_{AX} = 10V. With $V_A > V_{AX}$, comparator output is HIGH and tells the CNTL logic to keep Q1 set at 1.

Final step, time T5, CNTL logic sets the next lower bit Q0 =1 ie [Q] = 1011 and V_{AX} = 11V. Since $V_{AX} > V_A$, comparator goes LOW to signal that V_{AX} is too large, and the CNTL logic clears back Q0 to 0 at time T6.

At this point, all of the register bits have been processed, the conversion is complete and the CNTL logic activates (EOC)' output to signal that is digital equivalent of V_A is now in the register. So, digital output for V_A = 10.4V is [Q] = 1010.

Conversion time,Tc, for SAC: The control logic goes to each register bit, set it to 1, decides whether or not to keep it at 1, and goes on to the next bit. The processing of each bit takes one clock cycle, so that the total conversion time for an N-bit SAC will be N-clock cycles.

Tc = N x 1 clock cycles

FLASH ADC: It is the highest speed ADC, but its circuitry requires much more than other

types ADC. Example: 6-bit flash ADC requires 63 analog comparators; 8-bit requires 255 comparators.

3-Bit Flash Converter:

Figure 4.5 shows the 4-bit flash converter.

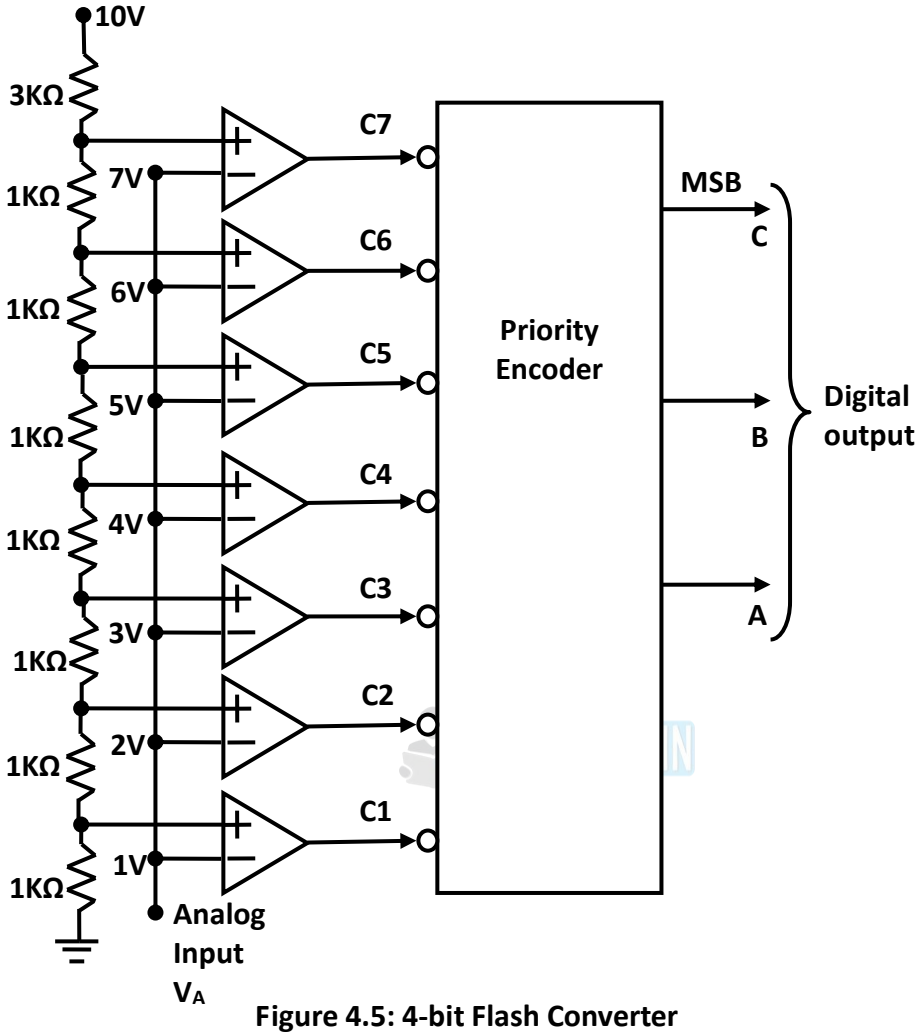


Figure 4.5: 4-bit Flash Converter

Operation: 3-bit flash converter has a resolution (step size) of 1V. Voltage divider set up a reference levels for each comparator, so that there are seven levels corresponding to 1V (weight of LSB), 2V, 3V, 4V, 5V, 6V and 7V (Full Scale). Analog input is connected to other input of each comparator. 3-bit flash converter ADC operation table is shown below:

Analog In	Comparator outputs							Digital Outputs		
(V_A)	C1	C2	C3	C4	C5	C6	C7	C	B	A
0V -1V	1	1	1	1	1	1	1	0	0	0
1V - 2V	0	1	1	1	1	1	1	0	0	1
2V - 3V	0	0	1	1	1	1	1	0	1	0
3 V- 4V	0	0	0	1	1	1	1	0	1	1
4V - 5V	0	0	0	0	1	1	1	1	0	0
5V - 6V	0	0	0	0	0	1	1	1	0	1
6V - 7V	0	0	0	0	0	0	1	1	1	0
>7V	0	0	0	0	0	0	0	1	1	1

TABLE of 3-bit Flash Converter ADC

With V_A < 1V, all comparator output is HIGH. With V_A > 1V, one or more comparators output

will be LOW. Comparator output is feed into active low priority encoder that generates a binary output corresponding to the highest numbered comparator output, that is LOW. For example, if V_A is between 3V – 4V, output C1, C2 and C3 will be LOW and all others are HIGH. Priority encoder will respond only to the LOW at C3 and will produce binary output CBA = 011.

Conversion Time, Tc of flash converter: Flash converter uses no clock signals. Conversion time depends only on the propagation delays of the comparators and encoder logic. So, flash converter has extremely short conversion times.

ADC USING VOLTAGE TO FREQUENCY CONVERTER:

Figure 4.6 shows the ADC using voltage to frequency converter.

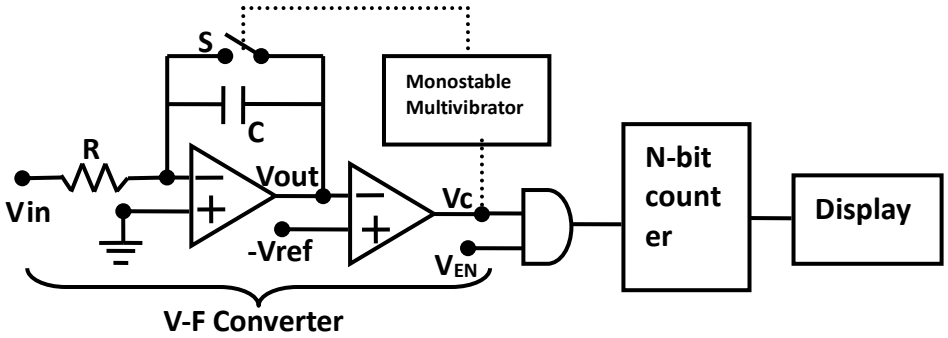


Figure 4.6: ADC using V-F converter

Voltage to frequency ADC does not require DAC. Instead it uses a linear voltage controlled oscillator (VCO), that produces an output frequency that is proportional to its input voltage. The analog input (Vin) that is to be converted, is applied to the VCO to generate the output frequency. This frequency is fed to the counter to be counted for a fixed time interval (V_{EN}). The final count is proportional to the value of the analog voltage. Circuit diagram of ADC using V-F converter shown in figure.

Operation: The Vin is applied to an integrator whose output is applied at the inverting terminal of a comparator. Non-inverting terminal is connected to –Vref. When switch S is open, Voltage Vout decreases linearly with time. Thus AND gate is disabled as long as Vout < Vref. As soon as Vout = Vref, the output Vc becomes positive, enabiling AND gate and hence counter starts counting. When the switch S is closed, the capacitor discharges and thereby returning the integrator output, Vout, to zero. After the delay time of multivibrator the switch S is again open and Vout starts decreasing again and ADC repeats its function.

FREQUENCY TO VOLATGE CONVERTER (INTEGRATING TYPE):

Block diagram of a voltage to frequency converter is shown in figure4.7 . The analog input is applied to an integrator. The integrator produces a ramp signal whose slope is proportional to the input voltage signal.

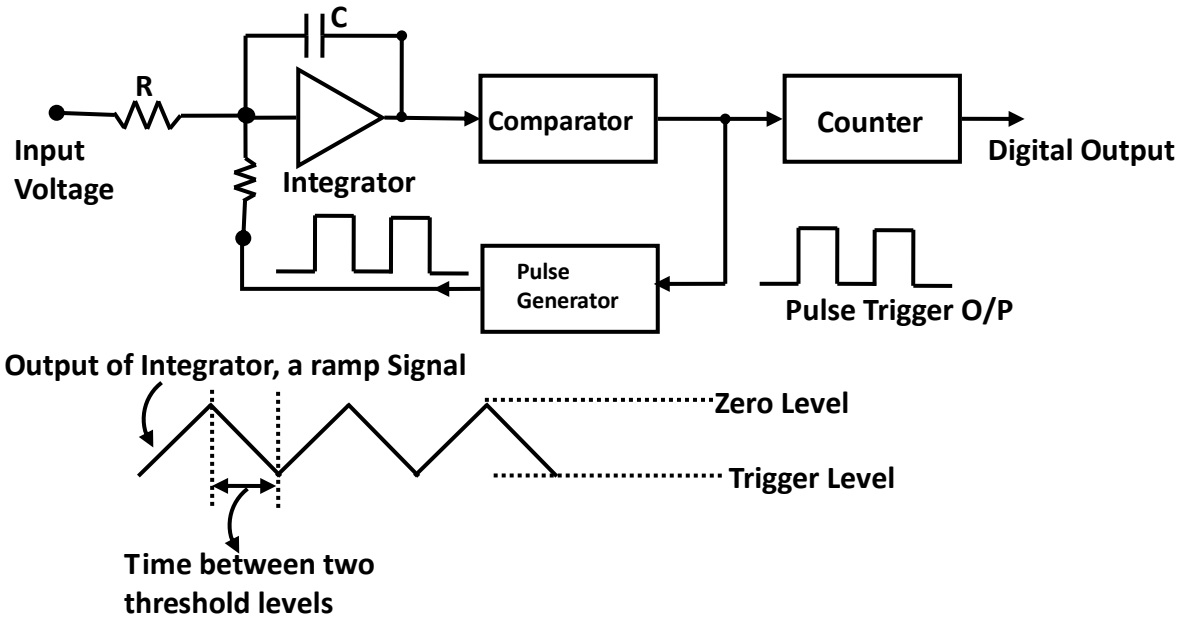


Figure 4.7: Frequency to Volatge converter

When this ramp signal reaches a preset threshold voltage level, a trigger pulse is produced. Also a current pulse is produced which discharges the capacitor of the integrator, after which a new ramp is initiated. The time between successive threshold level crossings is inversely proportional to the slope of the ramp. Since the slope of the ramp is proportional to the input analog voltage, hence the frequency of output pulses from the comparator is directly proportional to input voltage. The output frequency can be measured with the help of digital frequency meter.

SAMPLE AND HOLD CIRCUIT:

When an analog voltage is connected directly to the input of an ADC, the conversion process can be affected if the analog voltage is changing during the conversion time. This stability of conversion process can be improved by using a sample-and-hold circuit to hold the analog voltage constant while the A/D conversion is taking place.

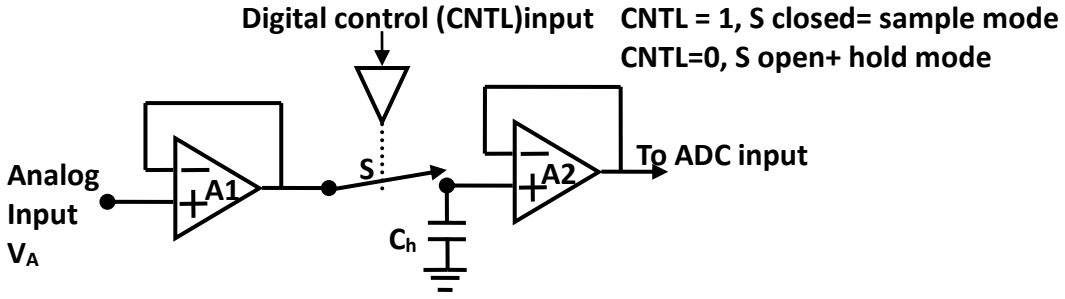


Figure4.8: Sample and Hold Circuit

Sample and hold circuit as shown in figure4.8, contains a unity gain buffer amplifier A1 that presents a high impedance to the analog signal and low output impedance that can rapidly charge the hold capacitor, C_h . Capacitor C_h is connected to output of A1 when digitally controlled switch is closed. This is called sample operation. The switch is closed long enough for C_h to charge to the current value of the analog input.

When switch opens, C_h will hold this voltage so that the output of A2 will apply this voltage to the ADC. The unity gain buffer amplifier A2 presents high input impedance that will not

discharge the capacitor voltage during the conversion time of the ADC.

DIGITAL TO ANALOG CONVERSION (DAC):

DAC is the process of taking digital code as input and converting it to a voltage or current that is proportional to digital value.

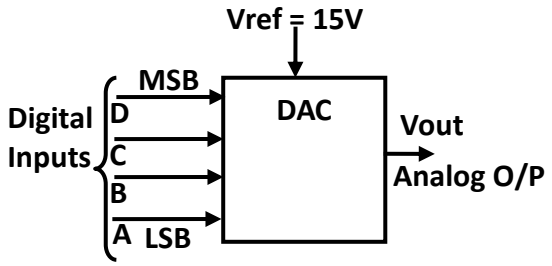


Figure 4.9:Block diagram 4-bit DAC

TABLE of 4-bit DAC:

Inputs				Output
D	C	B	A	Vout
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

From the block diagram as shown in figure 4.9 of 4-bit DAC ,Vref as input is used to determine the full scale output or maximum value that DAC can produce. For each input number, DAC output voltage is unique value. In general, **Analog output (Vout) = K x Digital Input;** Where, K is proportionality constant. In above block , DAC has K=1, so that, **Vout = 1 x Digital Input.**

Example: For digital input $(1100)_2 = (12)_{10}$, we obtain Vout = 1 x 12 = 12V.

RESOLUTION OR STEP SIZE OF DAC: Resolution of DAC is defined as the smallest change that can occur in the analog output as a result of a change in the digital input. Resolution is always equal to the weight of the LSB and also referred to as step size, since it is the amount that Vout will change as the digital input value is changed from one step to the next.

Resolution= K = A_{FS} / (2^n – 1) where, A_{FS} is analog full scale output; n is the number of bits

% Resolution = (Step size / A_{FS}) x 100 OR % Resolution = (1 / Total no. of steps) x 100

DAC USING OP-AMP SUMMING AMPLIFIER WITH BINARY WEIGHTED RESISTOR:

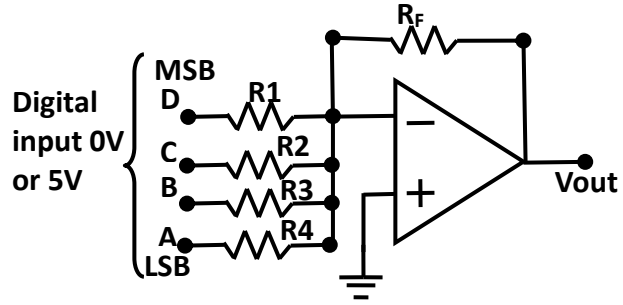


Figure4.10: OP-AMP as Summing Amplifier

Resistor R1 = 1KΩ
Resistor R2 = 2KΩ
Resistor R3 = 4KΩ
Resistor R_F = 8KΩ

From the figure4.10 , opamp as summing amplifier, inputs A, B, C and D are binary inputs that

are assumed to have a values either 0V or 5V. OP-AMP as summing amplifier, which produces the weighted sum of the input voltages. So that, **Vout = –(V_D + 1/2 V_C + 1/4 V_B + 1/8 V_A)**

So, the summing amplifier output is the analog voltage which represents a weighted sum of the digital inputs. The resolution of this DAC using opamp as summing amplifier using binary weighted resistor, is equal to the weighting of the LSB, which is 1 / 8 x 5 = 0.625V.

DAC USING R / 2R LADDER CIRCUIT:

In R/2R ladder circuit, the resistor values span a range of only 2 to 1.

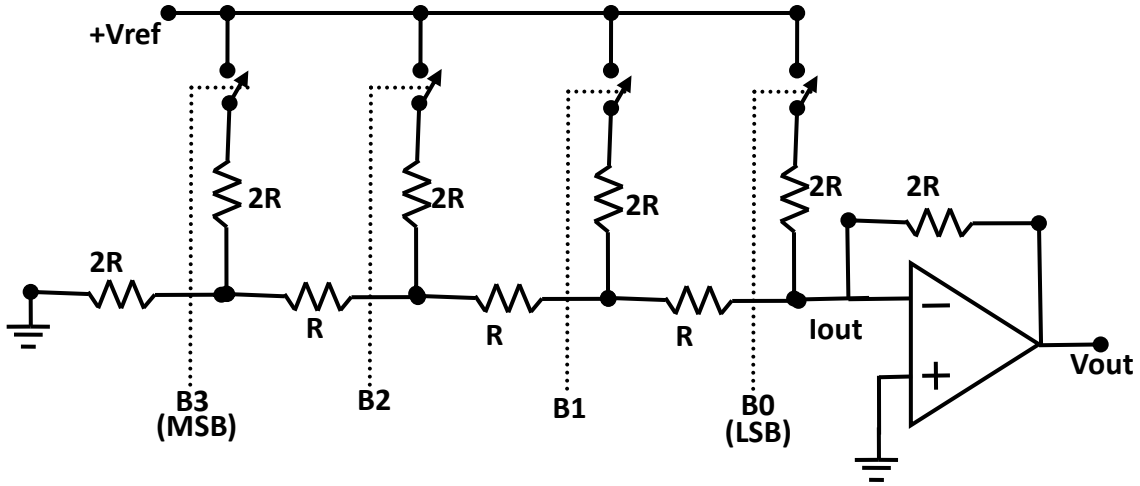


Figure 4.11: R/2R Ladder Circuit

In R/2R ladder network as shown in figure 4.11, only two different values are used, R and 2R. Current Iout depends on the positions of the 4- switches and the binary inputs B3, B2, B1 and B0, which controls the states of the switches.

Vout = (–Vref / 8) x B where "B" value of binary input from 0000 to 1111.

Example: Assume the Vref = 5V. What are the resolution and full scale output of this R/2R converter?

Solution: Resolution is equal to weight of LSB. Suppose, [B] = 0001 = $(1)_{10}$

Resolution = (-5V x 1)/ 8 = -0.625V. The full scale output occur for [B]=1111 = $(15)_{10}$

So, full scale output = (-5V x 15)/ 8 = -9.375V.

BISTABLE MULTIVIBRATOR:

If both the states of a multivibrator are stable i.e. the circuit which is in a particular state continues to remain in that state until it is triggered from an external source to change the state. Flip Flops are bistable multivibrator circuits as shown in figure 4.12.

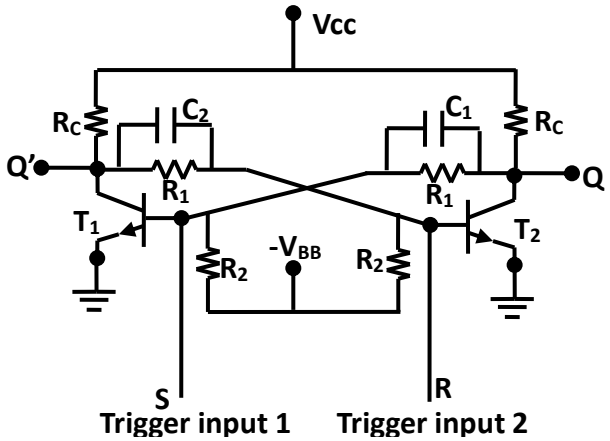
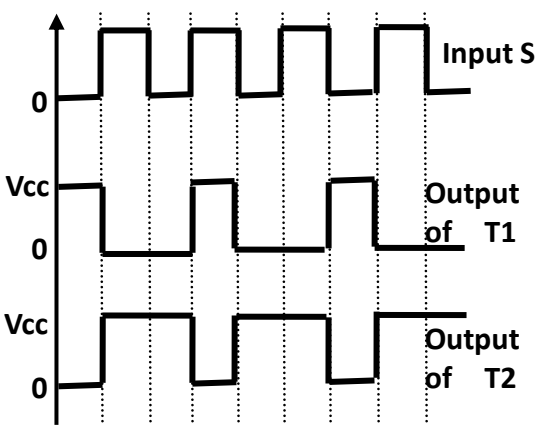


Figure4.12: Bistable Multivibrator



Transistor T_1 and T_2 are npn transistors and are resistively crosscoupled with each other. Q and Q' are outputs. Rc is the collector resistance. C_1 and C_2 are commutating capacitors, to fast turn OFF and ON of two transistors (C_1 for T_2 and C_2 for T_1). Supply $-V_{BB}$ and resistor R_2 are used to keep the base of the transistors at negative in one state and in other state provides large base current to drive the transistor into saturation.

Operation: When supply is ON, say T_1 is ON, so, $V_{c1} = 0v$, the base of T_2 is connected to V_{c1}, so T_2 is OFF. This makes $V_{c2} = V_{cc}$, since base of T_1 is connected to V_{c2}, so T_1 is ON. This is the first stable state (ie. T_1=ON and T_2=OFF ie. Q=1 and Q'=0).

To change the state of transistor T_2, a positive pulse is applied at the base of T_2. The OFF transistor T_2 will be forced to turn ON ($t_p > t_{on}$ ie. Pulse width should be greater than turn ON time of transistor). Thus V_{c2} is forced to 0v. Since base of T_1 is connected to V_{c2}, so T_1 is OFF. This is the second stable state (ie. T_1=OFF and T_2=ON ie. Q=0 and Q'=1).

MONOSTABLE MULTIVIBRATOR:

Monostable multivibrator as shown in figure 4.13 has one stable state and the other one is not stable (quasi stable).It is also called as one-shot multivibrator. Transition from stable state to quasi stable state is done by an external trigger pulse. After transition from stable to quasi stable state, the multivibrator remains in the quasi stable state for a definite period of time, decided by comoponents R and C, and then returns to the stable state automatically.

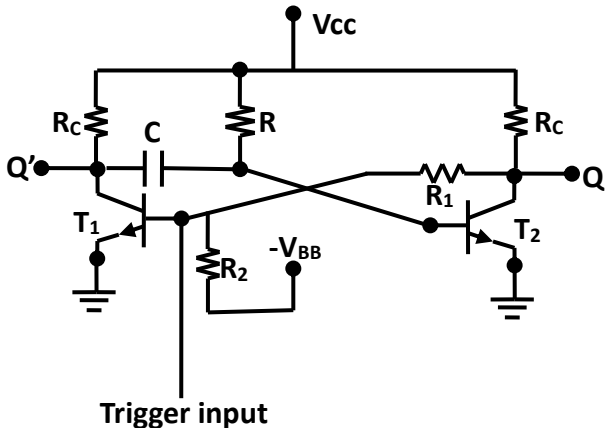
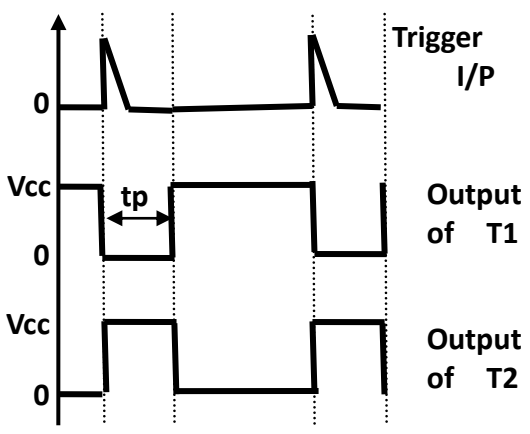


Figure4.13: Monostable Multivibrator



In this circuit the base of transistor T_2 is capacitively coupled to the collector of T_1, while the base of T_1 is resistively coupled to the collector of T_2.

Operation: When no trigger pulse applied, T_2 is ON, a proper base drive through Vcc and R to the base of T_2. So, V_{c2} = 0v. T_1 is OFF, because of resistively coupled of base T_1 with V_{c2}(V_{c1} = V_{cc}). At the instant when T_2 is ON, capacitor C charged towards V_{cc} through R_c. This is the stable state of multivibrator.

When a sufficient positive trigger pulse is applied to the base of T_1, T_1 is ON, so V_{c1} = 0v. Now the capacitor discharges through T_1 and R. Thus discharge current through R creates a negative potential at the base of T_2. Thus T_2 is OFF as long as the voltage drop across R is negative. This condition is quasi stable state. When the capacitor fully discharges the negative voltage at the base of T_2 reduces to zero and V_{cc} now drives the T_2 ON, so V_{c2} = 0v. So, T_1=OFF and V_{c1}=V_{cc}. This is the stable state and circuit remains in the stable state until the next trigger pulse is applied.

Time duration of quasi stable state or the pulse width: t_p = 0.693(R.C)

ASTABLE MULTIVIBRATOR:

Astable multivibrator as shown in figure 4.14, has no stable states but has two quasi stable states. The output oscillates between two quasi stable states without any external triggering ,therefore this circuit is also called as free running multivibrator. The output at the collector of transistors is a square wave, therefore also called as square wave generator.

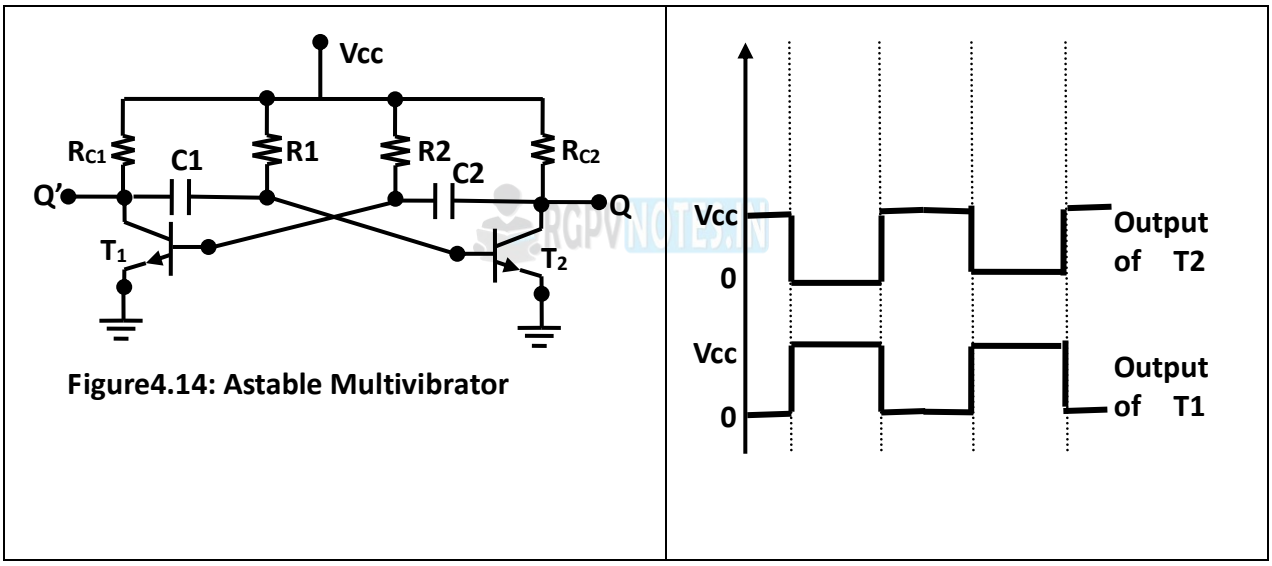


Figure4.14: Astable Multivibrator

Operation: Initially assume that T_1 is ON and T_2 is OFF due to circuit unbalance. So, V_{c1} = 0v and V_{c2} = V_{cc}. Since T_1 is ON, C_2 charges towards Vcc through R_{c2}. Meanwhile C_1 which was charged to V_{cc} when T_2 was ON will discharge through T_1 and R_1. This makes the potential at V_{B2} negative and causes T_2 to turn OFF. T_1 is kept ON by the base current provided by V_{cc} through R_2. The charging current of C_2 through R_{c2} has reduced to zero. The time duration for which T_2 is held OFF is determined by the R_1.C_1. Once T_2 turns ON due to the base drive from V_{cc} through R_1, then C_1 gets charged through R_{c1} and T_2. At the same time C_2 discharges through T_2 and R_2 making V_{B1} negative so that T_1 is turned OFF, thus V_{c1} = V_{cc}. T_1 is held OFF by the discharging current for the time duration R_2.C_2. After this T_1 turns ON and allow C_1 to discharge through T_1 and then C_2 recharges through T_1.

SCHMITT TRIGGER:

In digital circuits, fast waveforms are required so that the circuit remans in the active region for a very short time (of order of nano seconds) to eliminate the effects of noise or undesired parasitic oscillations causing malfunction of the circuit. Also if the rise time of the input waveform is long, it requires a large oupling capacitor. Therefore circuits which ca convert a slow-changing waveform (long rise time) into a fast-changing waveform (small rie time) are

required. The circuit which performs this waveform is known as Schmitt trigger.

In a Schmitt trigger circuit, the output is in one of the two levels, LOW or HIGH. From the figure 4.15,when the input voltage is rising, the level of the output changes when the input passes through a specific voltage V_{T+} (upper triggering level). Similarly, when the input voltage is falling, the level of the output changes when the input passes through a specific voltage V_{T-} (lower triggering level), the level of the output changes. V_{T+} (upper triggering level) is always greater than V_{T-} (lower triggering level). The difference of these two voltages is known as hysteresis as shown in figure 4.16.

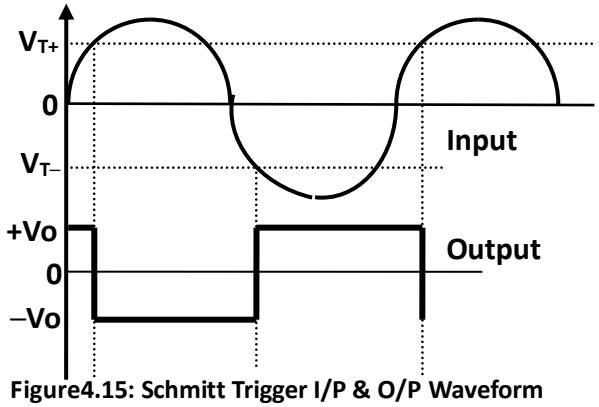


Figure4.15: Schmitt Trigger I/P & O/P Waveform

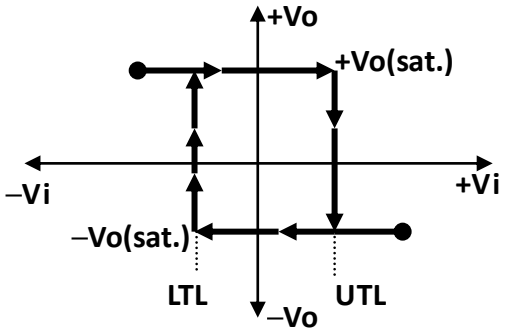


Figure4.16: Hysteresis Loop

Schmitt Trigger circuits:

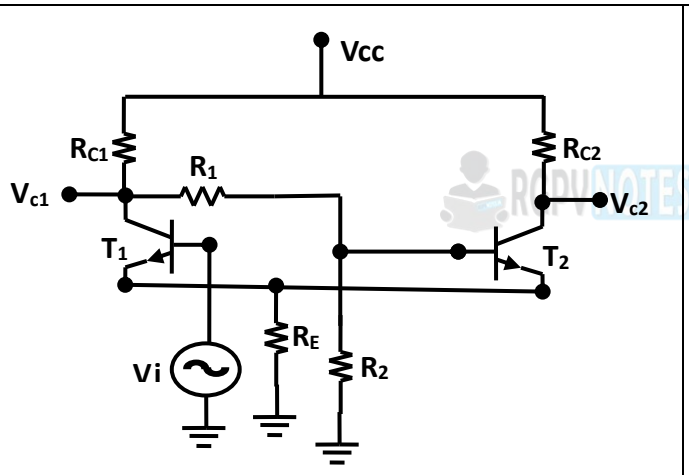


Figure4.17: Transistor Schmitt Trigger

From the figure 4.17 of transistor Schmitt trigger, resistor R_1 and R_2 are voltage divider resistors.

Operation: When Vi = 0V, when circuit is ON, T_2 is ON (V_{c2} = 0V). As T_2 is ON, there is a voltage drop across R_2. This drop acts as a reverse bias across emitter-base junction of T_1, due to which T_1 is OFF ($V_{c1} = V_{cc}$). This V_{cc} is coupled to base of T_2 through R_1. So T_2 is ON ie. In saturation($V_{c2} = V_{CE(sat)}$ = 0V).

When Vi = applied AC input, and approaches till it crosses V_{T+} (upper triggering level). Now, Vi > V_{T+} (upper triggering level), T_1 conducts. So, V_{c1} = 0V. This fall of voltage is coupled through resistor R_1 to the base of T_2, which reduces its forward bias voltage. So, T_1 = ON and T_2 = OFF ie. $V_{c1} = V_{CE(sat)}$ and $V_{c2} = V_{cc}$. The T_1 continues to conduct till the input voltage falls below V_{T-} (lower triggering level). When Vi > V_{T-} (lower triggering level), base-emitter junction of T_1 is reverse biased. So, T_1 is OFF. So, $V_{c1} = V_{cc}$ and $V_{c2} = V_{CE(sat)}$.

IC-555 TIMER:

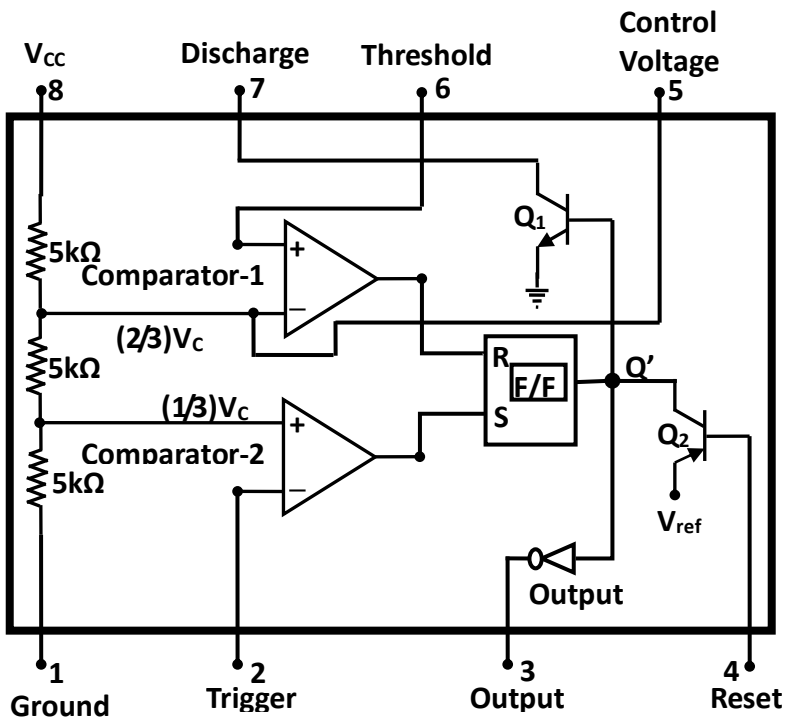


Figure 4.18: Functional block diagram of IC-555 Timer

Figure 4.18 shows the functional block diagram of IC-555 timer. It consists of a voltage divider network, which provides bias voltage of (2/3)Vcc to the inverting input of the comparator-1 and (1/3)Vcc to the non-inverting input of the comparator-2. These two voltages fix the comparator threshold voltage and also determine the timing interval. Electronically, possible to vary time by applying a modulation voltage to the control voltage input (pin-5).

If no such modulation is proposed, a 0.01µF capacitor is connected between control voltage and ground to bypass noise and ripple from supply. The other two inputs to the comparator are threshold and trigger inputs. The output of these two comparators, SET or RESET the flip flop, whose Q'output is fed to base of transistor Q_1. When Q' = high, Q_1 is ON and capacitor (externally connected between pin 7 and ground) will discharge.

The output stage is basically an inverting buffer stage used to provide a low output resistance and also to invert the flip flop output. Output stage has a capability of sourcing and sinking 200mA current. Q_2 (PNP transistor) whose emitter is connected to an internal reference voltage which is less than Vcc. When V_{ref} > Vcc (Pin-4 potential is less than Vcc), Q_2 is ON, which causes Q_1 to turn ON and output at pin-3 is brought to ground level.

Applications include oscillator, pulse generator, ramp and square wave generator, voltage monitor and may more applications.

IC-555 AS MONOSTABLE MULTIVIBRATOR:

Figure 4.19 (a) shows the circuit diagram of IC-555 as monostable multivibrator and (b) shows the waveform of trigger pulse, capacitor voltage and output pulse. Since it has only one stable state (output low), hence name monostable.

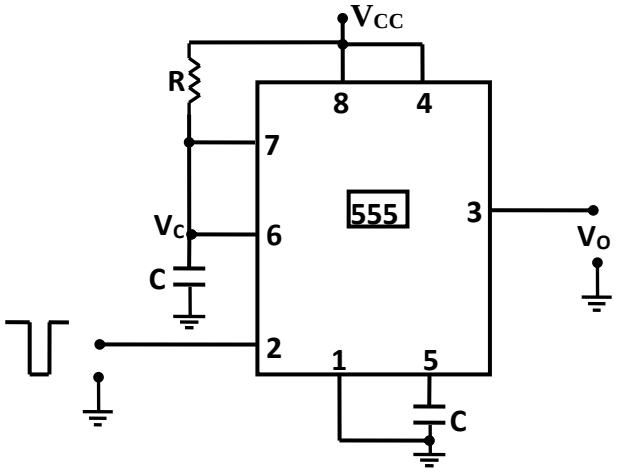


Figure 4.19(a): Monostable Multivibrator

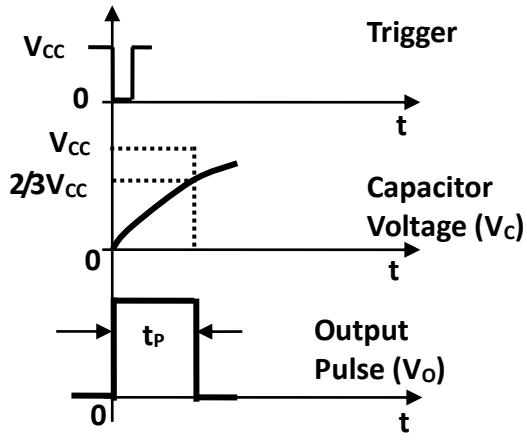


Figure 4.19(b): Waveforms

It is also called as one-shot multivibrator. From the circuit diagram, Pin-8 is connected to Vcc and pin-4 (reset pin) also connected to Vcc so that reset condition is disabled. The time interval for which the output remains high (t_P, pulse width) is decided by the external RC network. The capacitor C is connected between pin 7 and 1 so that it charges through the resistance R when the transistor Q_1 is OFF.

Operation: Initially, trigger pulse is high (Vcc), this drives the output of comparator-2 to low condition. As the capacitor C is in discharged state, pin-6 and 7 are at ground potential. The inputs to the flip flop will be S=R=0, hence Q' = high, so, Q_1 is ON, and C discharges to 0V ie. Vc = 0V. Since Q' = 1, output pin-3 = 0 is actually the stable state of multivibrator.

When the trigger input (negative trigger pulse) goes low (from Vcc to 0), comparator-2 output = high ie. S = 1. The comparator-1 output continue to be 0 ie. R=0, hence the flip flop is in set condition ie. Q' = 0, pin-3 = 1(High state). Since Q' = 0, transistor Q_1 is OFF and the capacitor C starts charging exponentially towards Vcc through the resistor R. When Vc becomes greater than ((2/3) Vcc), comparator-1 output changes form low to high ie. R = 1. Since the trigger input has returned back to Vcc from 0, comparator-2 output is equal to zero ie. S =0. So, S = 0 and R= 1, RS flip flop get RESET and Q' = 1. AS Q' = 1, transistor Q_1 = ON and capacitor C starts discharging towards zero through the transistor Q_1 and capacitor voltage Vc becomes zero. While discharging, when Vc < ((2/3) Vcc), the comparator-1 output goes to zero ie. R=0. Since the trigger input = Vcc, the comparator-2 output will be = 0 ie. S=0. Hence, S=0 and R=0, so no change in the Q' output condition and hence continuous to be High. Thus, pin-3 output = LOW (0-state).

The monostable multivibrator, thus goes from stable state into quasistable state and then returns back to the stable state after a time, $t_P = (1.1)R.C$

The output remains to be in LOW state until the next trigger pulse is applied to change the state.

IC-555 AS ASTABLE MULTIVIBRATOR:

Figure 4.20 (a) shows the circuit diagram of IC-555 as astable multivibrator and (b) shows the waveform of capacitor voltage and output pulse. Since no stable state, hence name astable.

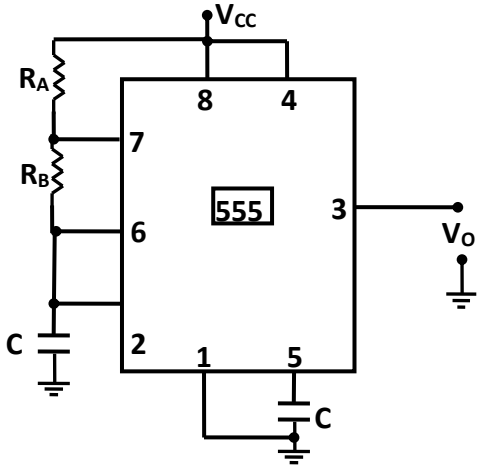


Figure 4.20(a): Astable Multivibrator

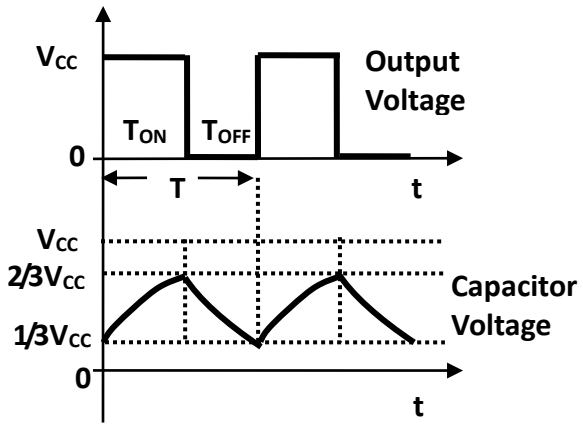


Figure 4.20(a): Waveforms

Astable multivibrator does not requires an external trigger pluse to change the output state, hence called as free-running multivibrator. The time duration for which the output will remain high or low is decided by the externally connected two resistors (R_A and R_B) and a capacitor (C).

Operation: Initially, when output is high (pin-3 = High), Flip flop output Q' = 0, hence transistor Q_1 is OFF. Now the capacitor C starts charging towards Vcc through R_A and R_B. As soon as the voltage across the capacitor Vc, becomes equal to[(2/3)Vcc], the comparator-1 output is high and will RESET the flip flop ie. Q' = 1. Hence the output = 0. As, Q' =1 , transistor Q_1 = ON and the capacitor C starts discharging through resistor R_B and transistor Q_1. During discharging mode of capacitor C, as soon as the voltage across the capacitor C becomes equal to [(1/3)Vcc], comparator-2 output will SET the flip flop, Q' = 0, and output = high. Then the cycle repeats.

Charging time duration of the capacitor C, is equal to the time the output is high is given by the expression: $t_C = T_{ON} = 0.69(R_A + R_B)C$

Discharging time duration of the capacitor C, is equal to the time the output is low is given by the expression: $t_d = T_{OFF} = 0.69(R_B)C$

Hence the total time period of output waveform: $T = t_C + t_d = T_{ON} + T_{OFF} = 0.69(R_A + 2R_B)C$

Hence, the frequency of oscillation is, $f_O = 1/T = \frac{1.45}{(R_A+2R_B)C}$

From the equation of frequency of oscillation fo, frequency is independent of the supply voltage Vcc.

Duty Cycle: Duty cycle is the ratio of the time during which the output is high (T_{ON}) to the total time period T.

% duty cycle = [T_{ON} / T] x 100 = $\frac{R_A+R_B}{R_A+2R_B} \times 100$

Applications: Astable multivibrator can be used to produce a square wave output. It can be used as a free running ramp generator.

DIGITAL IC LOGIC FAMILIES:

1. RTL- Resistor Transistor Logic **2.DTL-Diode Transistor Logic**
3.TTL- Transistor Transistor Logic **4.ECL-Emitter Coupled Logic**
5.I^2L- Integrated Injection Logic **6.PMOS- P-Channel Metal Oxide Semiconductor**
7.NMOS- N-Channel Metal Oxide Semiconductor
8.CMOS- Complementary Metal Oxide Semiconductor

Characteristics of Digital IC's:

1.FAN-IN: Number of inputs connected to gate, without the degradation in the voltage levels.
2.FAN-OUT: Number of standard loads that the output of the gate can drive without degrading the normal operation.
3.POWER DISSIPATION: Power consumed by the gate, available from power supply.
4.PROPAGATION DELAY: Average transition time for the signal to propagate from input to output.
5.NOISE MARGIN: Noise margin is the limit of noise voltage which may be present without imparing or degrading the proper operation of the circuit.

TTL- Transistor Transistor Logic:

A) TTL-2 input NAND gate having totem pole (active pull-up) output stage:-

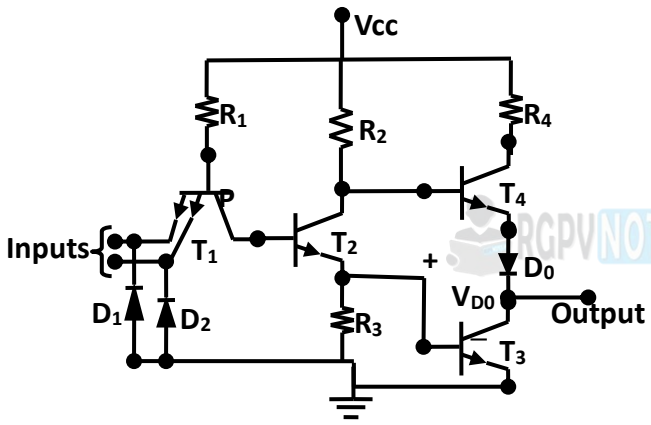


Figure 4.21: TTL- 2-Input NAND Gate(Totem Pole O/P)

The circuit diagram of a 2-input TTL NAND gate having an active pull-up (totem-pole) output stage is shown in figure 4.21. In this circuit, if one or both of the inputs are at logic 0, the corresponding B-E junction of T_1 will be forward biased, and the voltage at point P will become nearly equal to 0.7V which will keep the T_2 and T_3 OFF. (The voltage at P must be at least equal to 1.8V for turning T_2 and T_3 ON.) Therefore, the output voltage will be at logic 1, equal to Vcc – (drop across R_4)-(V_{CE} of T_4) – V_{D0}, which is nearly equal to 3.5V.

If both the inputs are held at logic 1 level, the B-E junctions of T_1 will be reverse biased, and the current flowing through R_1 and the C-B junction of T_1 will turn ON the transistors T_2 and T_3. Hence, the output voltage will be at logic 0, equal to V_{CEsat} of T_3. When the voltage at the input terminal corresponds to 1 level, the gate sinks an input current (reverse saturation current of the B-E junction of T_1), whereas when the voltage at the input terminal corresponds to 0 level, the gate sources an input current(forward current of the B-E junction of T_1).

Advantages: 1)when T4 is OFF and T3 is ON, no current through R4, so, no power dissipation. 2)If output is high, T4 is ON and T3 is OFF, hence T4 is acting in the emitter follower mode, its output impedance is low. Therefore output time constant for charging of any capacitive load is very short.	**Disadvantage:** T3 turns OFFmore slowly than T4 turns ON. So, before T3 completely turns OFF, T4 comes into conduction. So, for a very short duration of time both T3 and T4 are ON. This is called cross conduction and draws large current.

B) TTL- 2 input open-collector TTL NAND gate :

The circuit diagram of a 2-input open collector TTL NAND gate is shown in figure 4.23 and TTL-logic symbol (open collector) is shown in figure 4.22. Note that the collector of the transistor T_3 is floating. For the proper functioning of the device, this open collector terminal of T_3 must be tied to Vcc through resistor R, known as pull-up resistor (passive pull-up). Once a suitable pull-up resistor is connected, the characteristic of open collector and totem pole will be almost same.

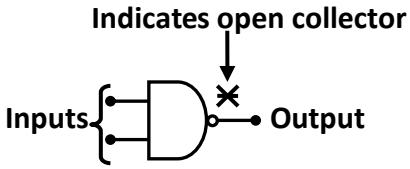


Figure 4.22: TTL- Logic Symbol (Open Collector)

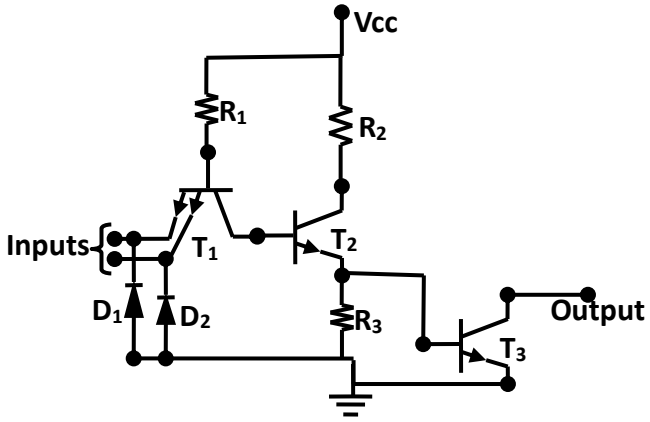


Figure 4.23: TTL- 2-Input NAND Gate(Open Collector O/P)

Advantage of open collector output is that wired ANDing becomes possible.

Wired ANDing as shown in figure 4.24, means tieing the outputs of gates together to obtain AND function.

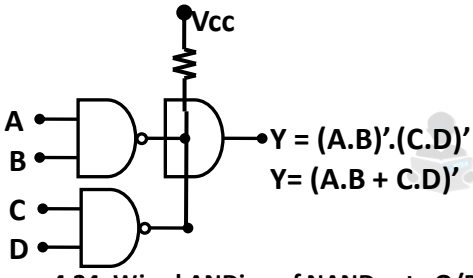


Figure 4.24: Wired ANDing of NAND gate O/P

It is possible to connect the outputs of two or more gates together.

Comparision of Totem-Pole and Open-Collector outputs:

Parameters	Totem-Pole	Open-collector
Circuit components on output side	T4 (pull up transistor), T3 (pull down transistor) and diode D0.	Only T3 (pull down transistor)
Wired ANDing	NO	Yes
External pull up resistor	Not required	Required
Power Dissipation	Low due to Pull up transistor.	High due to current flowing through external pull up resistor.
Speed	High	Low

C) TTL- TRI-STATE TTL Gate:

In a normal logic circuits there are two states of the output- LOW and HIGH. When a number of such outputs are connected to a common line, there are loading problems. To avoid this, tri-state outputs are used. In tri-state output circuits, there are three distinct states of which two are the logic 0 and logic 1 states and third is a high impedance state. In the figure 4.25 of a tri-state TTL inverter circuit, when control input is LOW, the drive is removed from T_1 and T_2 and the output is in the third state (High impedance). When the control input is high, the output is 1 or 0 depending on the input. Figure 4.26 logic symbol of tristate TTL inverter.

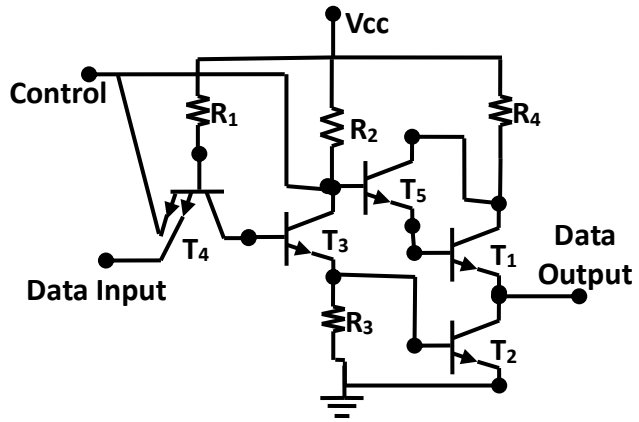


Figure4.25: Tri-state TTL inverter

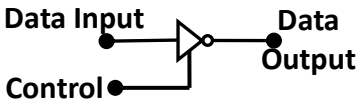
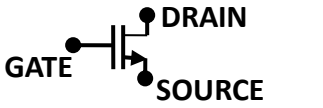
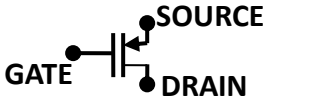
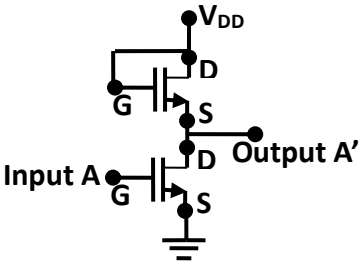


Figure 4.26 : Tri-state TTL inverter logic symbol

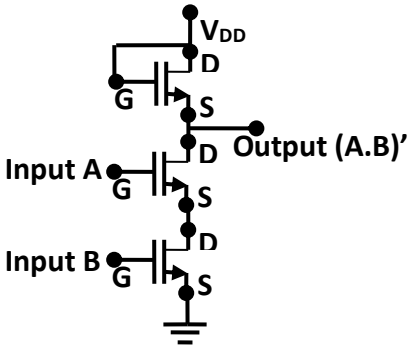
PMOS, NMOS, and CMOS logic:

 Logic Symbol of NMOS	A NMOS switch is closed when controlling signal is HIGH. An arrow indicates the direction of positive current flow from drain (D) to source (S) in NMOS.
 Logic Symbol of PMOS	A PMOS switch is closed when controlling signal is LOW. An arrow indicates the direction of positive current flow from source (S) to drain (D) in PMOS.

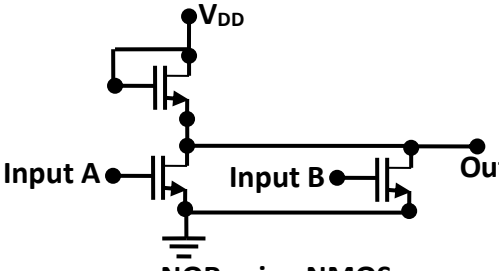
Realization of logic gates using MOS logic family:



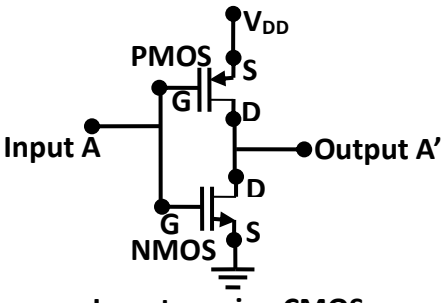
Inverter using NMOS



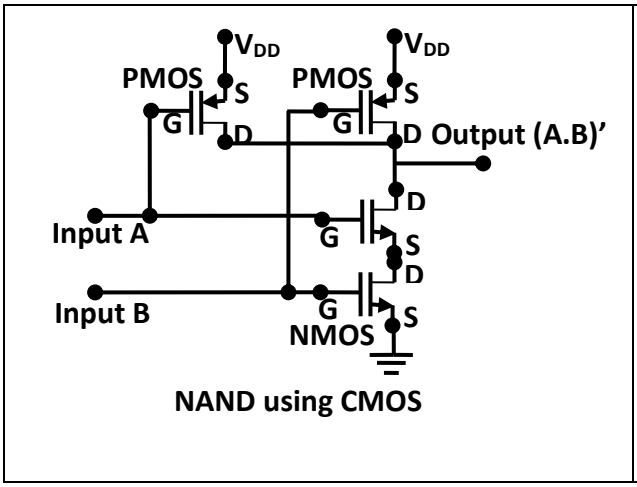
NAND using NMOS



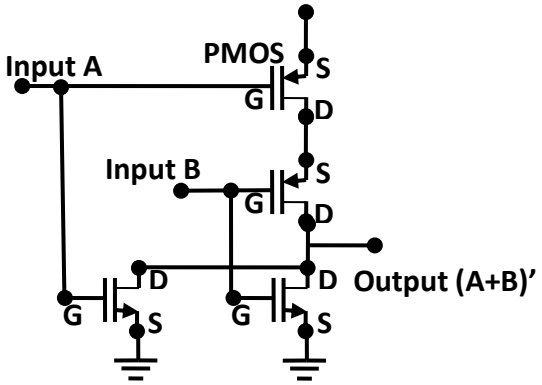
NOR using NMOS



Inverter using CMOS



NAND using CMOS



NOR using CMOS

Advantages of MOS logic: 1)Low power dissipation. 2)Excellent noise immunity. 3)High packing density. 4)Wide range of supply voltages (+3V to +18V)

INTERFACING BETWEEN TTL to MOS:

Interfacing refers the way a driving device is connected to a loading device. Here TTL is the driving device and CMOS is the loading device. TTL device needs a supply voltage of 5V and CMOS needs of +3V to +15V.

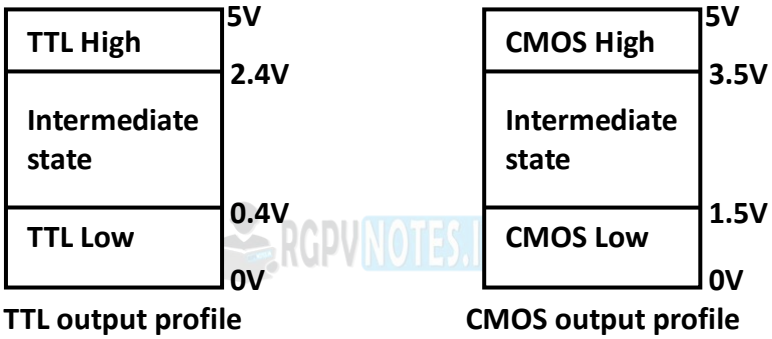


Figure 4.26: Outprofile of TTL and CMOS

Figure 4.26 shows the output profile of TTL and CMOS, a TTL low fits inside the CMOS low ie. CMOS load always interprets the TTL low state drive as a low. The problem is with TTL high state ie. there is indeterminate action ie. no reliable operation. So, the standard solution is to use a pull up resistor between TTL driver and CMOS load. It raises the high state to approximate 15V.

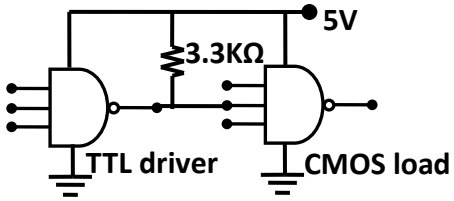


Figure 4.27:TTL driver & CMOS interface

In figure 4.27, When TTL output is low, 3.3K resistor is grounded, therefore TTL driver sink current of 1.52mA. when TTL output is high, pull up resistor, output raises above +2.4V ie. The supply voltage is pulling up the output upto +5V (1.52mAx3.3K). If more than one TTL chip is being interfaced to the CMOS load, connect each TTL driver to a separate pull-up resistor.

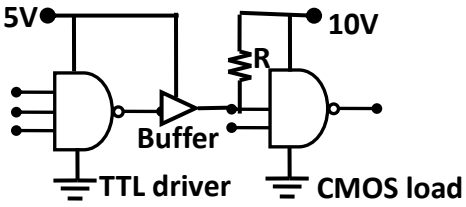


Figure4.28:TTL driving high voltage CMOS

If CMOS IC is operated with V_{DD} greater than 5V then the TTL driving high voltage CMOS design is used as shown in figure 4.28. Buffer is used to interface between TTL and CMOS. IC7406 as inverting buffer has an output voltage rating of 30V.

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