RGPVNOTES.IN

Program : **B.Tech**

Subject Name: **Digital Systems**

Subject Code: **CS-304**

Semester: **3rd**

Subject Name: Digital Systems **Subject Code**: CS303

Subject Notes

UNIT-III

Sequential logic: flip flops, D,T, S-R, J-K Master- Slave, racing condition, Edge & Level triggered circuits, Shift registers, Asynchronous and synchronous counters, their types and state diagrams. Semiconductor memories, Introduction to digital ICs 2716, 2732 etc. & their address decoding, Modern trends in semiconductor memories such as DRAM, FLASH RAM etc. Designing with ROM and PLA.

3.1 SEQUELTIAL LOGIC:

A flip flop is a basic data storage element. A NAND or NOR gate individually act as a storage element when they are cross coupled with feedback. Such cross coupled NAND or NOR gates with feedback are known as flip flops. A flip flop is a bistable (output will remain permanently either 0 or 1 until it is forced to change the state by an external trigger) circuit. A flip flop have two outputs Q and Q', and are complement to each other.

(a) R-S (RESET-SET)FLIP FLOP USING NOR GATES:

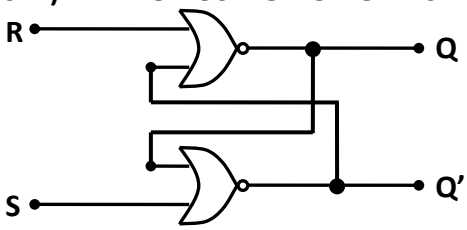


Figure 3.1.1 RS Flip Flop using NOR Gate

Truth Table:

S	R	Q (output)
0	0	No Change
1	0	1 (SET)
0	1	0 (RESET)
1	1	Invalid

The truth table shown for NOR gate flip flop is similar to that of transistor flip flop.

(b) R-S (RESET-SET) FLIP FLOP USING NAND GATES:

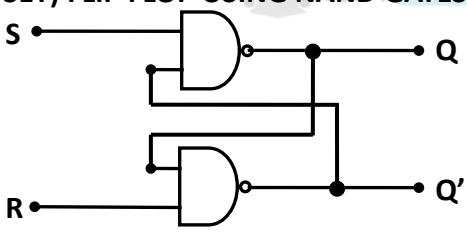


Figure 3.1.2 RS Flip Flop using NAND Gate

Truth Table:

S	R	Q (output)
0	0	Invalid
1	0	0 (RESET)
0	1	1 (SET)
1	1	No Change

The truth table shown for NAND gate flip flop is inverted to that of NOR gate flip flop, hence inverters gates are used to drive the inputs to the gates as shown:

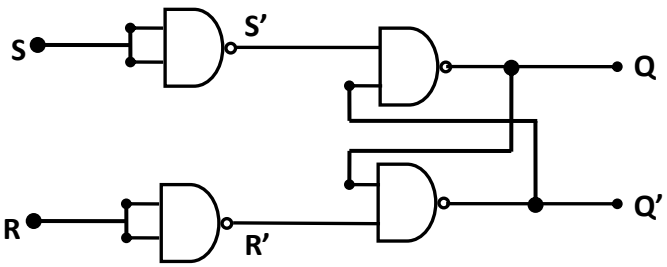


Figure 3.1.3 RS Flip Flop

Truth Table:

S	R	Q (output)
0	0	No Change
1	0	1 (SET)
0	1	0 (RESET)
1	1	Invalid

The truth table for NAND gate flip flop with inverters is similar to that of transistor flip flop, hence this flip flop is used to realize the desired flip flop.

(c) CLOCKED R-S FLIP FLOP:

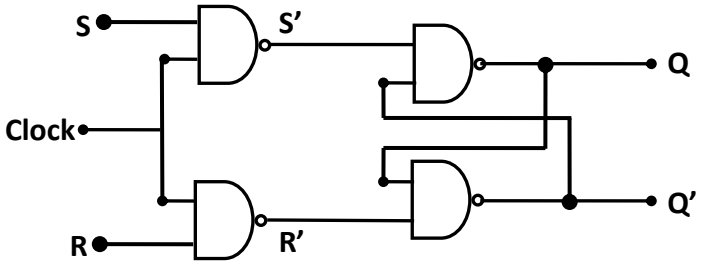


Figure 3.1.4 Clocked RS Flip Flop

Truth Table:

Clock	S	R	Q (output)
1	0	0	No Change
1	1	0	1 (SET)
1	0	1	0 (RESET)
1	1	1	Invalid

The clock signal or the enabling signal which makes the circuit to perform the required operation. If clock = 0, the circuit output will remain unchanged. If clock = 1, the flip flop is enabled and respond to the applied input signal.

(d) J-K FLIP FLOP:

In order to overcome the invalid condition in R-S Flip Flop, the J-K Flip Flop is used.

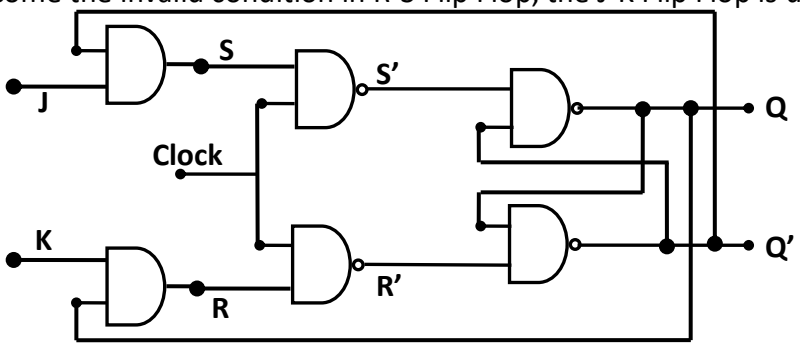


Figure 3.1.5 JK Flip Flop

Truth Table of J-K Flip Flop:

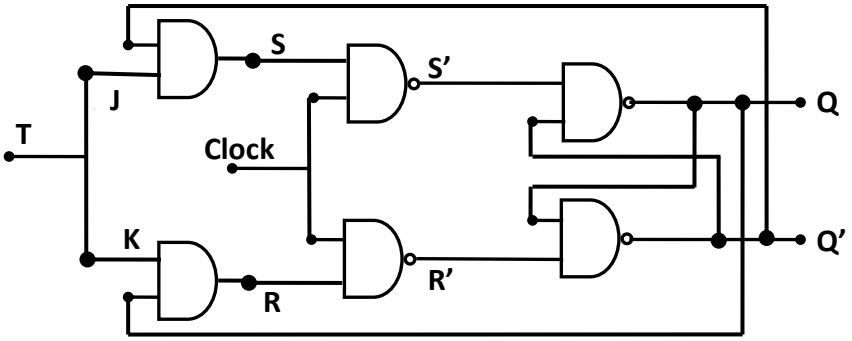
CLK	J	K	Qn	S	R	Q_{n+1} (output)	Remarks
1	0	0	0	0	0	0	Qn (No change)
1	0	0	1	0	0	1	
1	0	1	0	0	0	0	0 (RESET)
1	0	1	1	0	1	0	
1	1	0	0	1	0	1	1 (SET)
1	1	0	1	0	0	1	
1	1	1	0	1	0	1	Toggle or complement
1	1	1	1	0	1	0	

Qn represent the past state; Qn+1 represent the present state i.e. the state of the output after the clock pulse is applied.

The J-input is analogous to the S input and K to the R input. So, when J=1 and K=0, the J-K flip flop is in SET state and when, J = 0 and K = 1, the flip flop is in RESET state. When J=K=1, the flip flop will complement its output condition, with high clock signal. This is the RACE around condition and it is a problem in JK flip flop. To overcome the problem of race around condition, Master-Slave JK flip flop is used.

(e) T- Flip Flop (Toggle or change state):

T- flip flop is a single input version of the JK flip flop. T flip flop is obtained if both the inputs of JK flip flop are tied together.



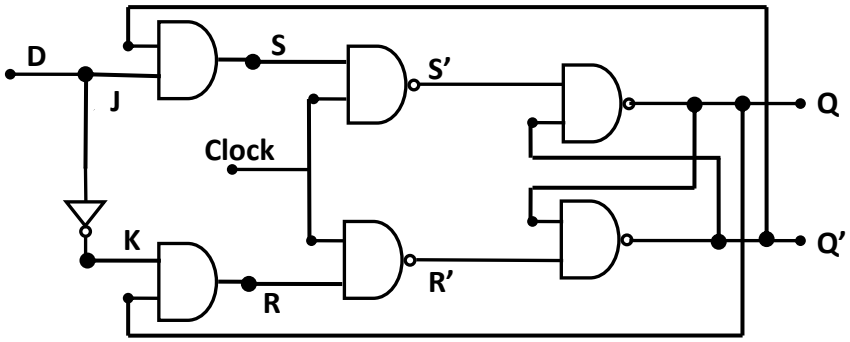
Truth Table:

Clock	T	Qn+1 (output)
1	0	Qn
1	1	Qn'

Figure 3.1.6 JK Flip Flop

D-Flip Flop:

The SR or JK flip flop can be converted into a delay (D) flip flop. The D flip flop receives the designation from its ability to transfer data into a flip flop i.e when clock is high the output Q follows the state of the input line D.



Truth Table:

Clock	D	Qn+1 (output)
1	0	0
1	1	1

Figure 3.1.7 D Flip Flop

3.2 EDGE & LEVEL TRIGGERED CIRCUITS:

Triggering is very important in the sequential circuits. The circuits operates with the clock waveforms. The circuit can be made to work on either level or edge triggering.

Level Triggered Circuits:

We know that the clock pulse is having the two levels. Therefore if the output is changing during the positive or negative levels of the clock pulse, then the triggering is called the Level Triggered Circuits. In level triggering the circuit gets activated when the clock waveform reaches certain level i.e. either 1 or 0. Clock waveform for level triggering is shown in figure 3.2.01 (a).

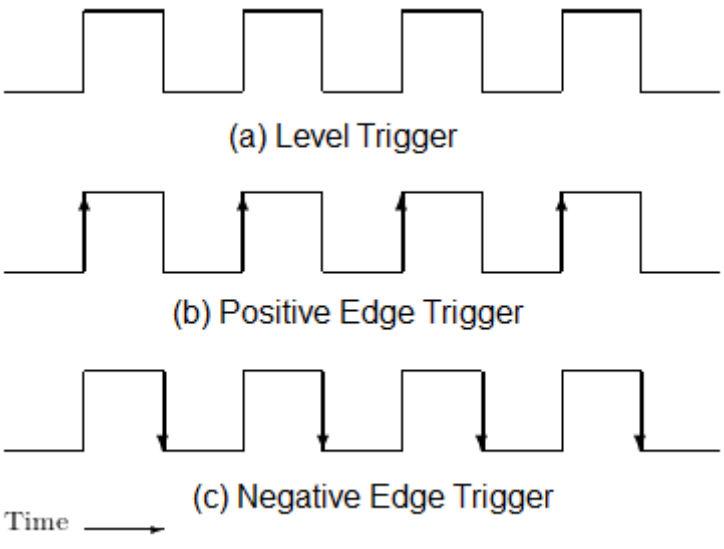


Figure 3.2.01 Level and Edge Triggering

Edge Triggered Circuits:

If the output of any sequential circuits is changing during the transition period of the clock waveform then the triggering is called the Edge Triggering. This can be seen in figure 3.2.01 (b) and (c).

Edge triggered circuits are those circuits which reads the data available at the input pins i.e. gets activated only on the edge of the clock cycle. The edge may be positive or negative depending on that the circuits are called Positive Edge Triggered Circuits and Negative Edge Triggered Circuits.

In positive edge triggered circuts the circuit gets activated when the clock pulse is moving from level 0 to level 1, whereas in negative edge triggered circuits the circuit gets activated when the clock amplitude is moving towards 0 from 1.

3.3 SHIFT REGISTERS:

The register capable of shifting itsbinary information either to the right or to the left is called shift register. Shift register consists of array of flio flops connected in cascade. All flip flops receive a common clock pulse which causes the shift from one stage to the next stage.

Shift registers are classified depending upon the way data are loaded and retrieved.

Classified as- 1.Serial Input Serial Output Shift Register 2. Serial Input Parallel Output Shift Register 3. Parallel Input Serial Output Shift Register 4. Parallel Input Parallel Output Shift Register.

1. Serial Input Serial Output Shift Register (SISO):

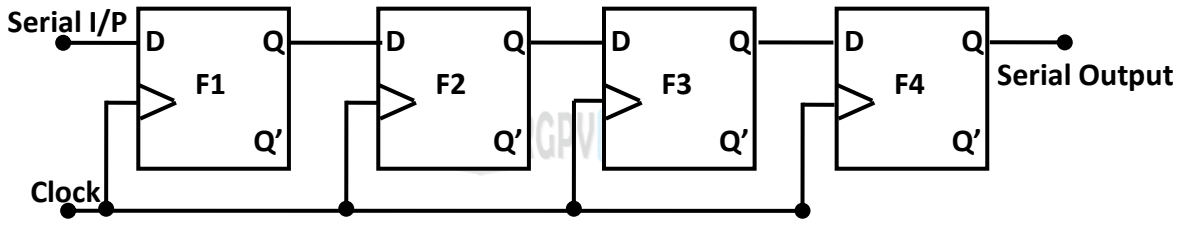


Figure 3.3.01Serial Input Serial Output Shift Register

From the above diagram of SISO shift register, output of eah flip flop is connected to the input of the next flip flop at its right. Each clock pulse shifts the contents of the register one bit to the right.

Operation:

Serial loading of Information or data:

Input Sequence	F1	F2	F3	F4	Clock Pulse
1 1 0 1	0	0	0	0	Initial state
	1	0	0	0	After 1 CP
	0	1	0	0	After 2 CP
	1	0	1	0	After 3 CP
	1	1	0	1	After 4 CP
Serial Loading of data					

Serial retriving of Information or data:

Clock Pulse	F1	F2	F3	F4	Output Sequence
After 4 CP	1	1	0	1	-----
After 5 CP	X	1	1	0	1
After 6 CP	X	X	1	1	01
After 7 CP	X	X	X	1	101
After 8 CP	X	X	X	X	1101
Serial retriving of data					

2. Serial Input Parallel Output Shift Register (SIPO):

In SIPO, data is loaded serially, one bit at a time but data can be read simultaneously.Clock pulse stop at the movement the binary information is stored. Each output is available on a separate line, and they may be read simultaneously.

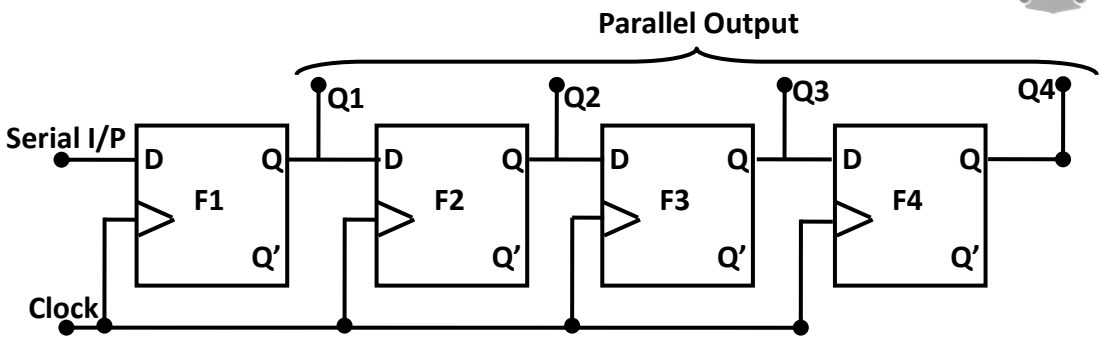


Figure 3.3.02 Serial Input Parallel Output Shift Register

3. Parallel Input Parallel Output Shift Register (PIPO):

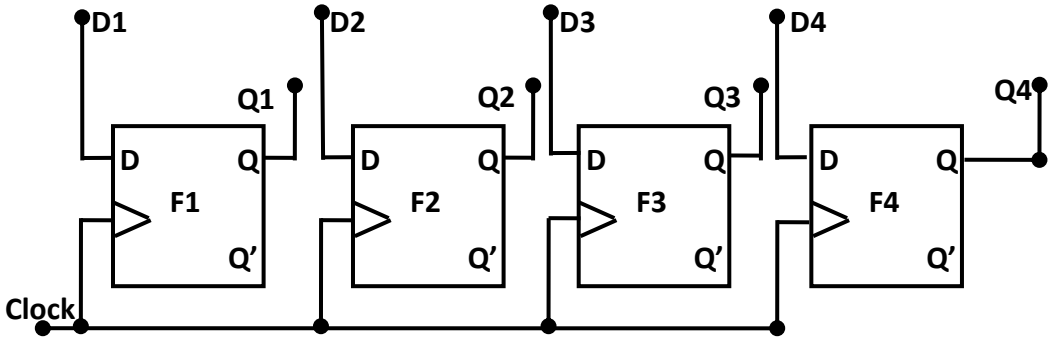


Figure 3.3.03 Parallel Input Parallel Output Shift Register

In PIPO shift register, input data D1,D2,D3 and D4 can be loaded into the flip flop simultaneously through enable pulse and can be retrived simultaneously also from outputs Q1,Q2,Q3 and Q4.

4. Parallel Input Serial Output Shift Register (PISO):

In PISO shift register, all flip flops are preset and the input binary information is written into the register, all bits in parallel, by the preset enable pulse. The stored information may be read serially by applying clock pulses. Since the data can be loaded into the flip flop simultaneously and can be read from the register one bit at a time by clock pulse, this shift register is a parallel to serial converter.

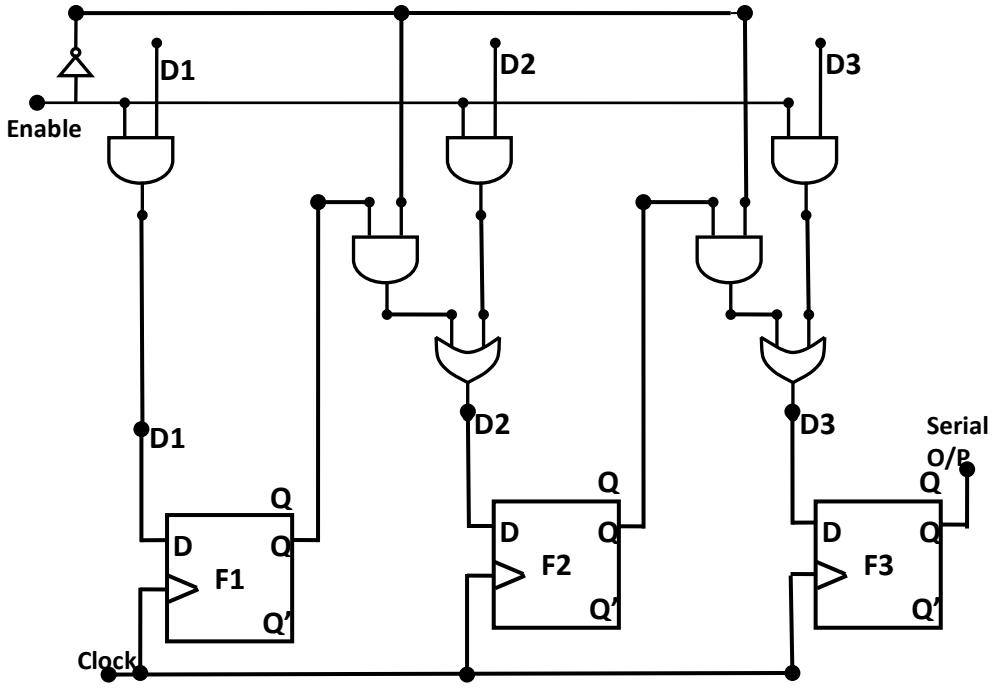


Figure 3.3.04 Parallel Input Serial Output Shift Register

From the above figure of PISO shift register, data input D1,D2 and D3 are loaded

simultaneously, when Enable = 1. When Enable = 0, loaded data is taken out serially from Q3 output of F3 flip flop. On application of clock pulse.

APPLICATIONS OF SHIFT REGISTERS:

1.The SISO shift register is used to provide a time delay from input to output. If N is the number of flip flop and fc is the clock frequency, then the time delay is-

$$T_d = N \times 1 / fc$$

2. RING COUNTER: Ring counter is a shift register, in which output of last stage is feedback to the input of first stage.

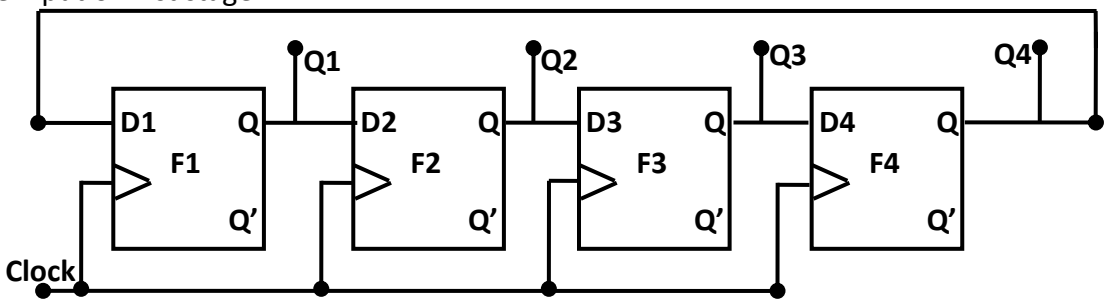


Figure3.3.05: 4-bit Ring Counter

	Q1	Q2	Q3	Q4	Clock pulse
Reference State	1	0	0	1	
	1	1	0	0	1
	0	1	1	0	2
	0	0	1	1	3
	1	0	0	1	4

Table 3.3.01: Count Sequence

Above table shows the count sequence of 4-bit ring counter. Assuming the starting state as Q1=1,Q2=0,Q3=0 and Q4=1. After a clock pulse 1, Q1 bit is shifted to Q2, Q2 to Q3, Q3 to Q4 and from Q4 to Q1 and counter is in 1100 state. The second and third clock pulse produces 0110 and 0011 respectively. Further clock pulses causes the sequence to repeat. Since it has 4-different states before the sequence repeats, therefore it is also called MOD-4 counter.

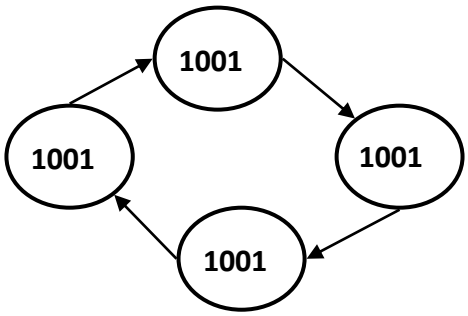


Figure 3.3.06: State Diagram of Ring Counter

3. JOHNSON COUNTER (Twisted Ring Counter or Moebius Counter):

In johnson counter, the complement output of last stage flip flop is feedback to input of first stage.

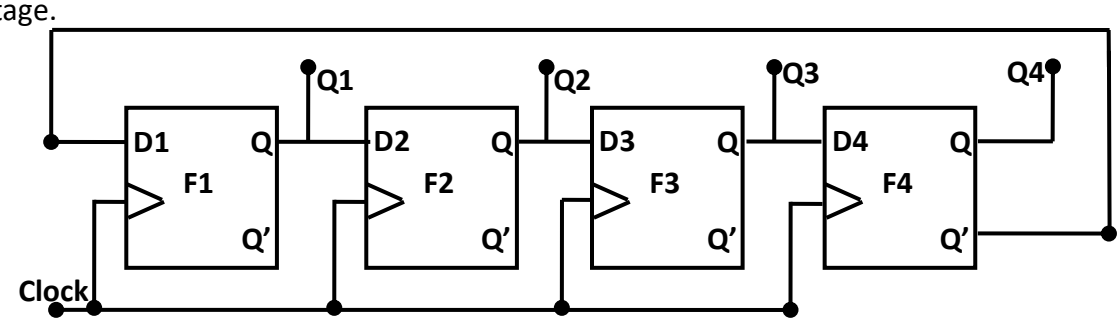


Figure3.3.07: 4-bit Johnson Counter

	Q1	Q2	Q3	Q4	Clock pulse
Reference State	0	0	0	0	
	1	0	0	0	1
	1	1	0	0	2
	1	1	1	0	3
	1	1	1	1	4
	0	1	1	1	5
	0	0	1	1	6
	0	0	0	1	7
	0	0	0	0	8

Table: Johnson Counter Count Sequence

4. SERIAL ADDER:

In serial adder, the pair of bits in A and B are transferred serially, one at a time, to the single full adder to produce a string of output bits for the sum.

Operation: In serial adder shown in below figure, register A stores augend bits and B stores addend bits. The two binary numbers are added serially stored in two shift registers. One pair of bits are added, one at a time, through full adder. The carry out is transferred to D Flip flop input. The output of D flip flop is used as an input carry to next pair bits. Register A is used for storing the SUM and augend bits.

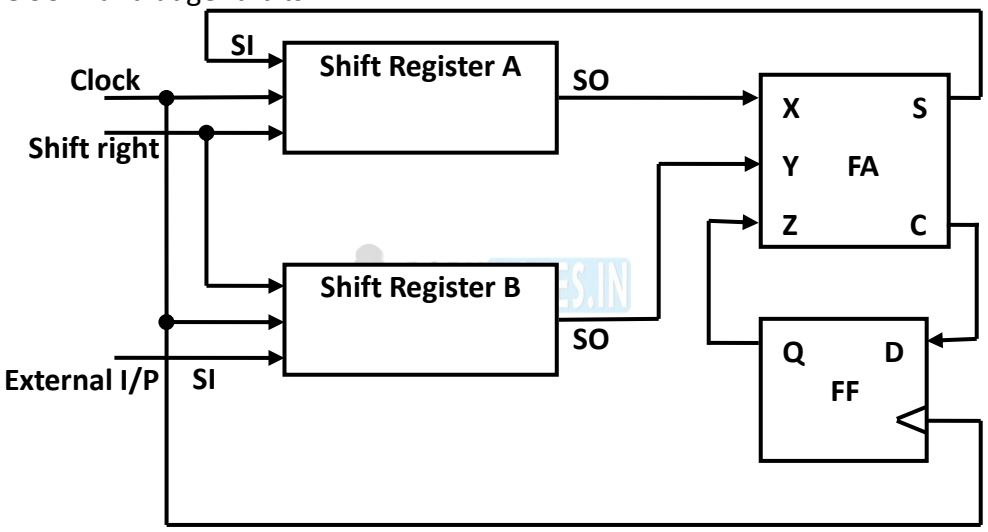


Figure3.3.08: Serial Adder

3.4 ASYNCHRONOUS AND SYNCHRONOUS COUNTERS:

Counters are digital circuit which is used to count the clock pulses or to generate the sequence of states. Science clock pulses occur at known intervals, the counter can be used for measuring time and therefore period or frequency.

Asynchronous Counter or Serial Counter:

1.Each flip flop is triggered by the previous flip flop. Except the first flip flop.
2.Counter is simple and straight forward in operation.
3.Construction usually requires a minimum number of hardware.
4.Counters has a cumulative settling time.

Synchronous Counter or Parallel Counter:

1.Every flip flop is triggered by the clock (in synchronism).
2.Increase in speed of operation.
3.Construction- Increased in hardware.
4.Settling time is equal to the delay time of a single flip flop.

Modulus of Counter(MOD): Modulus of counter is the number of different states before the sequence repeats. Example- 3-bit binary counter has 8 different states, so MOD-8 counter.

ASYNCHRONOUS UP- COUNTER (BINARY RIPPLE COUNTER):

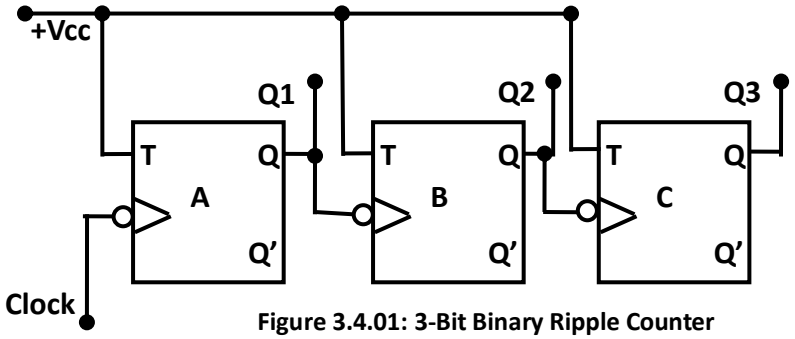


Figure 3.4.01: 3-Bit Binary Ripple Counter

3-bit binary ripple counter using T-Flip flop is shown above. From the figure, negative edge triggered clock drives the flip flop "A". Output Q1 of flip flop "A" drives the flip flop "B" and output Q2 of flip flop "B" drives flip flop "C". Flip flop "A" change state before it can trigger the flip flop "B" and flip flop "B" has to change state before it can trigger the flip flop "C". The trigger moves through the flip flop like a ripple in water, hence the name Ripple Counter.

Operation: Let assume all flip flop are reset to produce "0". Consider flip flop "A" as least significant bit (LSB) and flip flop "C" as most significant bit (MSB), so the content of counter is CBA = 0 0 0.

Cloc	Q	Q	Q	Coun
	0	0	0	**0**
a	0	0	1	**1**
b	0	1	0	**2**
c	0	1	1	**3**
d	1	0	0	**4**
e	1	0	1	**5**
f	1	1	0	**6**
g	1	1	1	**7**
h	0	0	0	**0**

TRUTH TABLE

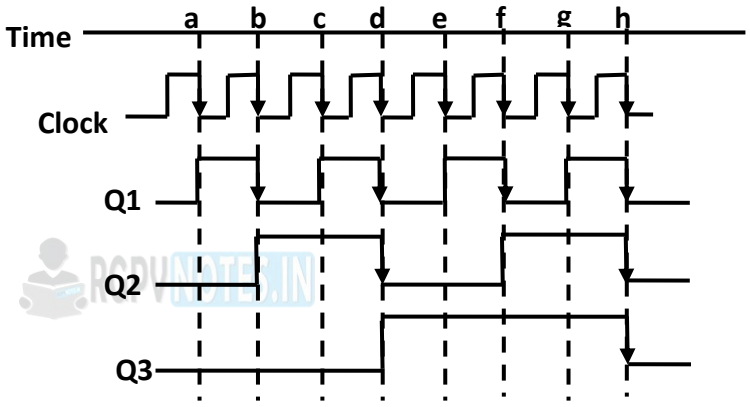


Figure 3.4.02: Waveforms

From the waveform, for every negative clock transition, output Q1 of flip flop A will change the state. Since flip flop A output Q1, act as a clock for flip flop B, each time the waveform at Q1 goes low, output Q2 of flip flop B will toggle (change the state). Each time the output Q2 of flip flop B goes low, output Q3 of flip flop C will toggle (change the state).

ASYNCHRONOUS DOWN COUNTER:

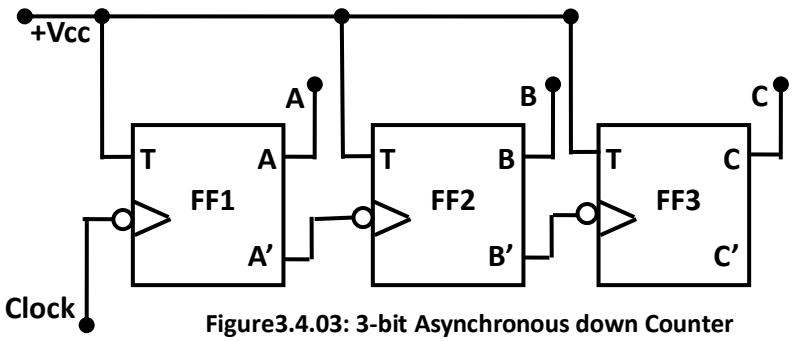


Figure3.4.03: 3-bit Asynchronous down Counter

System clock is used to drive flip flop 1, but the complement A' of flip flop-1, is used to drive the flip flop-2 and complement B' of flip flop-2, is used to drive the flip flop-3. Output A of flip flop-1 toggles with every negative clock transition. But flip flop 2 will toggle each time A goes high i.e. A' goes low and it is this negative transition that triggers flip flop-2. On the time line,

flip flop-2 toggles at point a,c,e,g and i. similarly, flip flop-3 is triggered by B' and so flip flop-3 will toggle each time flip flop-2 goes high. Thus flip flop-3 toggles high at point a on time line and toggles back at point e and high at point i. Notice that the counter content are reduced by one count with each clock transition i.e in count down mode.

TRUTH TABLE

Clock	C	B	A	Count
	1	1	1	**7**
a	1	1	0	**6**
b	1	0	1	**5**
c	1	0	0	**4**
d	0	1	1	**3**
e	0	1	0	**2**
f	0	0	1	**1**
g	0	0	0	**0**
h	1	1	1	**7**

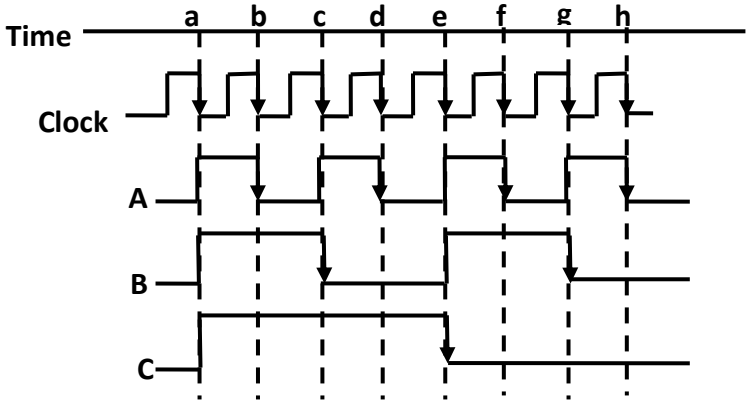


Figure 3.4.04: Waveforms

SYNCHRONOUS COUNTER OR PARALLEL COUNTER:

In a ripple counter (asynchronous counter) flip flop delay times are additive and the total settling time for the counter is approximate the delay times the total number of flip flops. These problem is overcome by the use of a synchronous counter or parallel counter. Here every flip flop is triggered in synchronism with the clock.

SYNCHRONOUS 3-BIT BINARY UP COUNTER OR MOD-8 PARALLEL COUNTER:

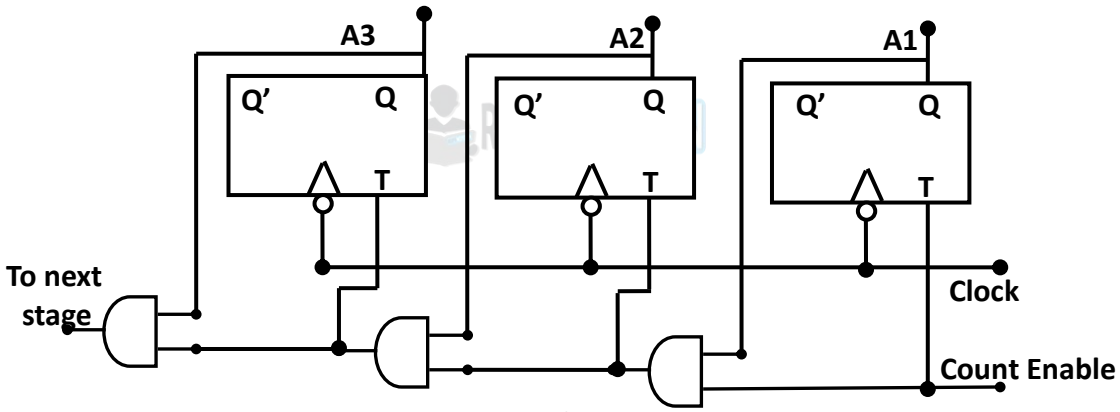


Figure 3.4.05: 3- Bit Synchronous Up Counter

Truth Table:

Count Enable	Clock pulse	A3	A2	A1	count
		0	**0**	**0**	**0**
1	**1**	**0**	**0**	**1**	**1**
1	**1**	**0**	**1**	**0**	**2**
1	**1**	**0**	**1**	**1**	**3**
1	**1**	**1**	**0**	**0**	**4**
1	**1**	**1**	**0**	**1**	**5**
1	**1**	**1**	**1**	**0**	**6**
1	**1**	**1**	**1**	**1**	**7**
1	**1**	**0**	**0**	**0**	**0**

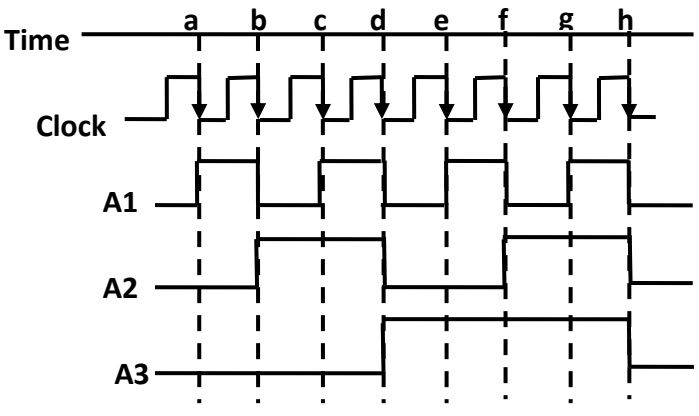


Figure 3.4.06: Waveforms

The truth table and waveforms of 3-bit synchronous up counter is shown above.

SYNCHRONOUS 3-BIT BINARY DOWN COUNTER :

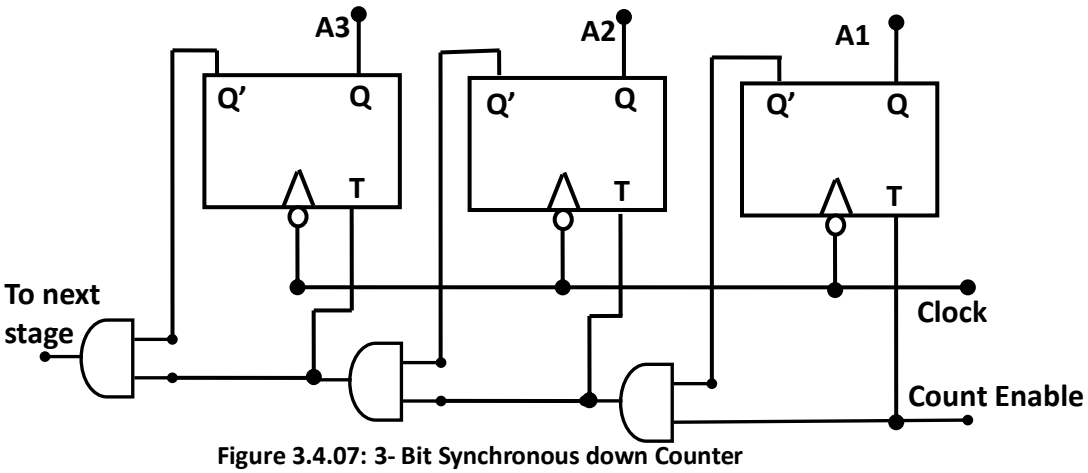


Figure 3.4.07: 3- Bit Synchronous down Counter

TRUTH TABLE

Clock	A3	A2	A1	Count
a	1	1	1	7
b	1	1	0	6
c	1	0	1	5
d	1	0	0	4
e	0	1	1	3
f	0	1	0	2
g	0	0	1	1
h	0	0	0	0
	1	1	1	7

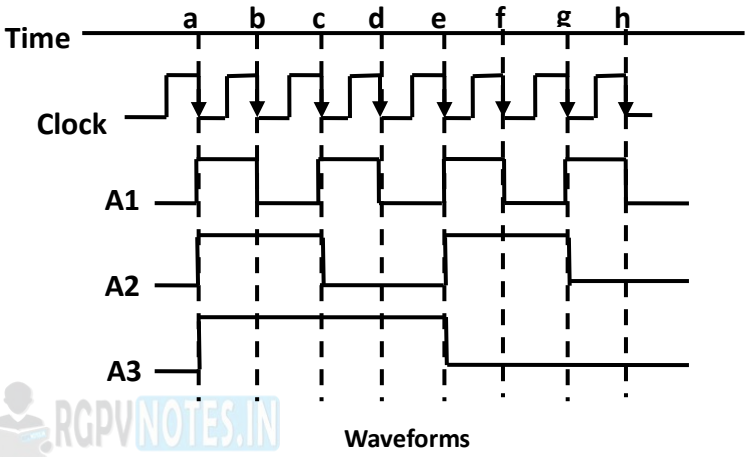


Figure 3.4.08: Waveform and truth table of 3-bit binary down counter

3.5 SEMICONDUCTOR MEMORIES:

MODERN TRENDS IN SEMICONDUCTOR MEMORIES SUCH AS DRAM, FLASH RAM ETC. DESIGNING WITH ROM AND PLA:

Memory is the ability to store information. The circuits or systems design, needs for data storage is called memory. A computer uses a number of memory devices of different technologies such as semiconductor memory, magnetic memory etc.

Memory Organization:

The basic element of a semiconductor memory is flip flop. There are number of memory locations in a memory chip, each location being ment for one word.

Size of a memory chip = M x N bits.

Where M represents the number of locations in memory and N represents the number of bits at each location.

Block diagram of memory device consists of M locations of memory and is defined by unique address and therefore for accessing any one of the M locations, P inputs are required, where $M = 2^P$. This is referred to as address lines. The number of inputs required to store the data into or read the data from any memory location is N.

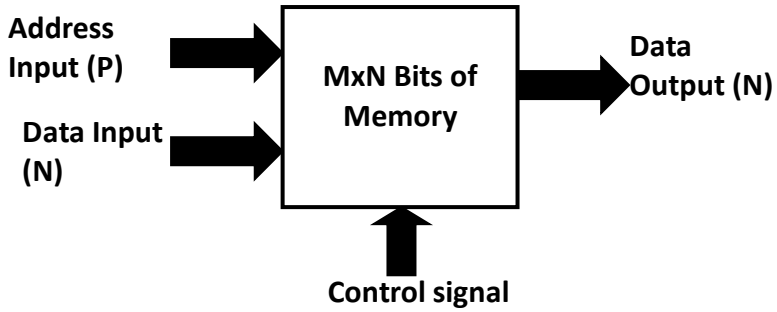


Figure 3.5.01: Block diagram of memory device

The number of distinct address possible with 'n' input variable is 2^n. The number of bits per word is equal to number of output lines.
Example: 1k-byte of memory chip has 1024 registers with 8-bits each.
The total capacity of memory having P address lines and N data lines is defined as 2^p x N.

Classification of Memories:

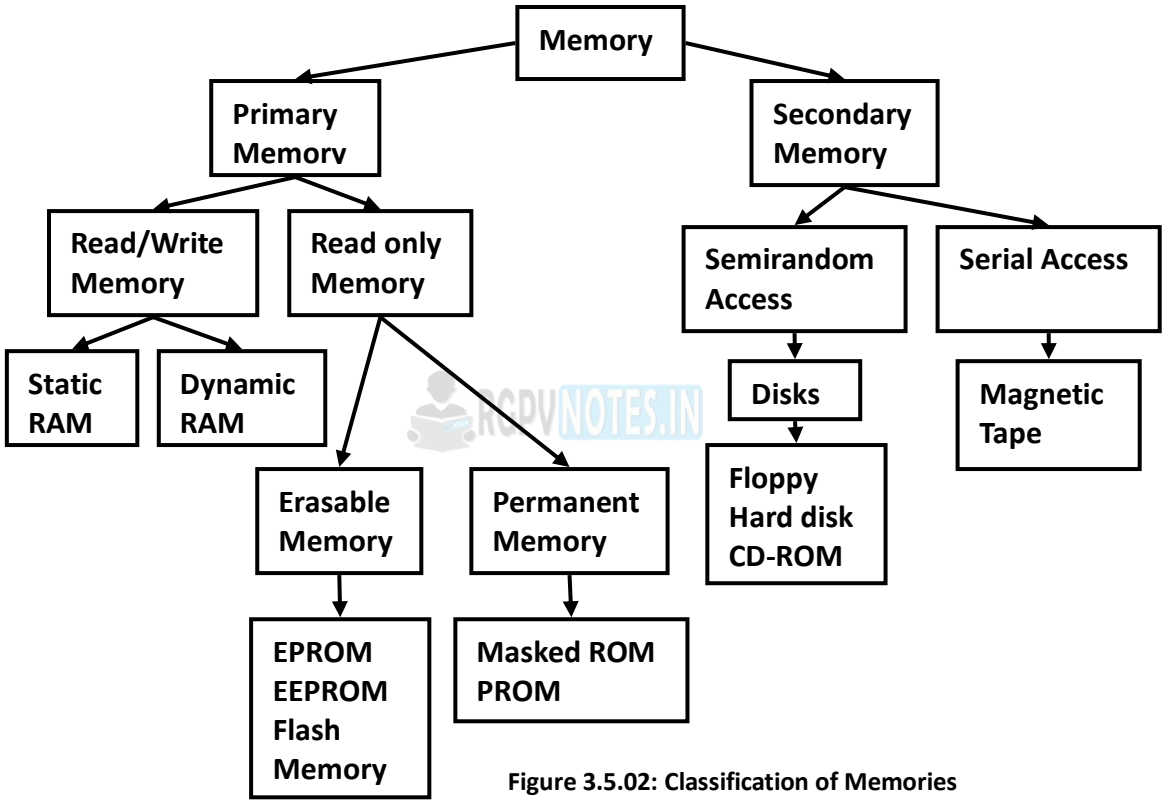


Figure 3.5.02: Classification of Memories

Volatile and Non volatile memories: The memory that required electrical energy to stored the information is called volatile memory. Information stored in memory is lost when electrical power is off. RAM is a volatile memory.
In a non volatile memory, the information once stored remain intact. ROM is non volatile.

Read Only Memory(ROM): It is used to store information which is permanent or semipermanent in nature. The permanent group includes: masked ROM and PROM and semipermanent group include: EPROM and EEPROM.
Masked ROM: Programming is done through masking and metallization process. User cannot write into this memory.
PROM:Programmable ROM: User can program(write) the PROM through PROM programmer.It can be programmed once only, user cannot rewrite this memory.
EPROM: Erasable Programmable ROM: User can rewrite this memory, many times. Program erasing is done using ultra violet light through a window over the memory chip. This window

is exposed in UV light. Entire information is erased at once when exposed in UV.

EEPROM: Electrical Erasable PROM: Information can be altered by using electrical signals at the register level rather than erasing all the information i.e information can be erased byte by byte.

Flash Memory: Erasing is done sector by sector not byte by byte.

RAM: Random Access Memory: Read and Write Memory: In such memories, the data stored at any location can be changed during the operation of the system. This type of memory is known as read write (RAM) memory. RAM is a volatile memory. Two types of RAM are there, static RAM and dynamic RAM.

Static RAM: The stored data will remain permanently stored as long as power supplied, without the need for periodically rewriting the data into memory. The basic memory cell is flip flops. One static RAM uses six transistors. Static RAM is faster than dynamic. More expensive and high durability.

Dynamic RAM: Stored data will not remain permanently stored, even with power applied, unless the data are periodically rewritten into memory i.e. the refresh operation. Basic memory cell is capacitor. Dynamic RAM uses 4-MOS transistors. Extra refreshing circuitry is present to accomplish refresh operation. Low power consumption.

ROM Organisation:

Diode Matrix ROM:

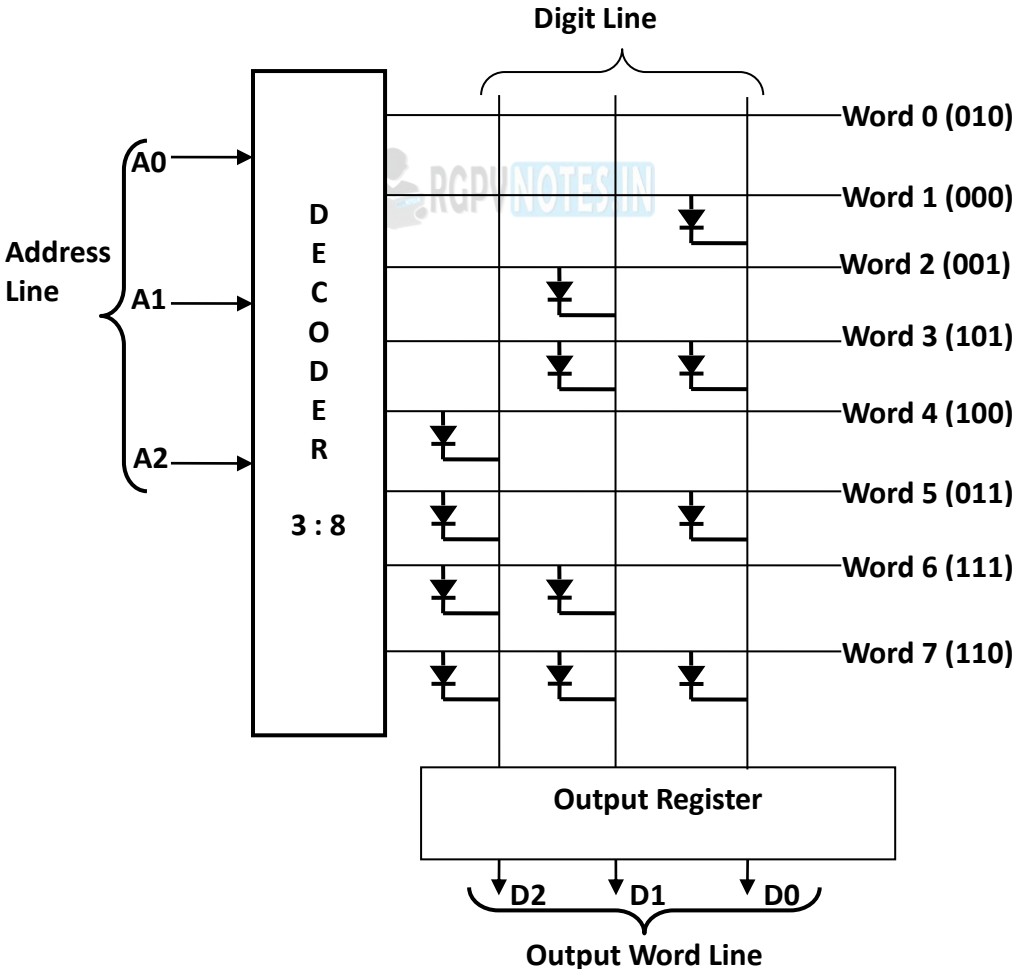


Figure3.5.03: 8-Bit ROM Array

From the above figure,8-bit ROM array, each horizontal row is a register. A diode present at the intersection represent logic 1 where as absence of a diode represent logic 0. The decoder selects one of the 8-word by increasing the voltage of the corresponding word line. This

forward bias the diodes, thus shorting the digit line to the word line. In this way the data is read across the output register.

Truth Table of 8-bit ROM Array:

Address Lines			Output of ROM		
A_2	A_1	A_0	D_2	D_1	D_0
0	0	0	0	1	0
0	0	1	0	0	0
0	1	0	0	0	1
0	1	1	1	0	1
1	0	0	1	0	0
1	0	1	0	1	1
1	1	0	1	1	1
1	1	1	1	1	0

Bipolar ROM: The bipolar transistor is used to connect the word line with digit line in place of diodes in diode matrix. Below figure shows the bipolar ROM cell.

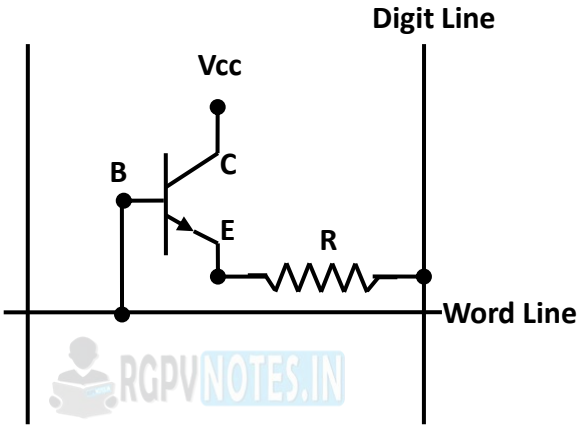


Figure 3.5.04: Bipolar ROM cell

When decoder selects one of the word by raising the voltage of corresponding word line, the emitter base junction of transistor is forward biased, which allows current to flow through resistor R, and tht bit of the word is a 1. When decoder output line is low, it is not selected and that bit of the word is a 0. The advantage of bipolar ROM over diode ROM are high packing density, low power consumption and high speed.

MOS ROM: In MOS ROM cell the gate and drain terminal of MOSFETare connected to word line and substrate and sourse terminals are connected to digit line as shown below.

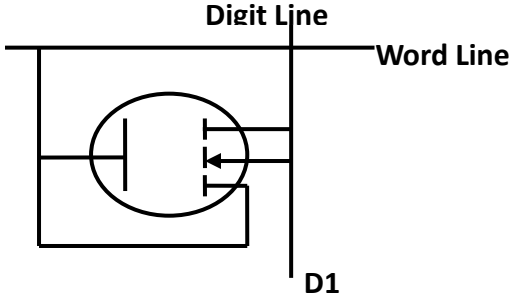


Figure 3.5.05: MOS ROM cell

The decoder selects one of the words by raising the voltage of the corresponding word line. MOSFET resistance is near zero ohms, thus shorting the digit lines to the word line and causing a high voltage to appear on these digit lines. A low at gate and drain terminals causes the FET to open, thus the digit line will remain to ground voltage. I this way the bits of the

addressed word are read.

PROGRAMMABLE LOGIC DESIGN (PLD):

PLD are special type of IC that contains a large number of logic gates whose interconnections are programmed by the user to generate the desired logic relationship between inputs and outputs. Types of PLDs:

a) Read only memories (ROMs)
b) Programmale logic array (PLAs)
c) Programmable array logic (PALs)
d) Simple Programmale logic array (SPLAs)
e) Complex Programmale logic array (CPLAs)
f) Field programmable gate arrays (FPGAs)

ROM as PLD: A ROM is a device that includes both the decoder and the OR gates within a single IC packages. A ROM of size MxN has M number of locations and each location can store N bit word. There are P number of address lines to access M locations hence the relation between P and M is given by $2^P = M$.

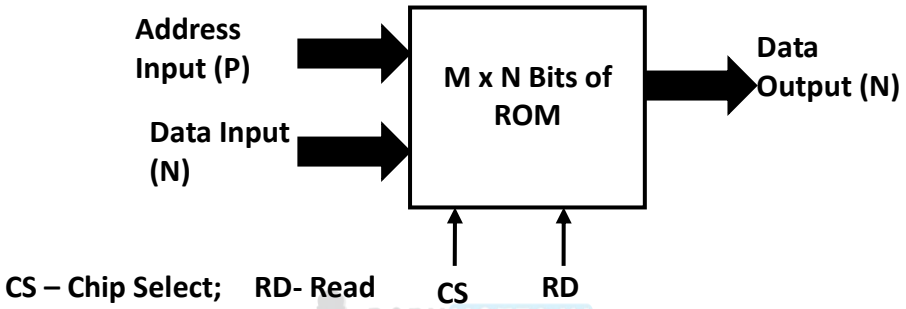


Figure 3.5.06: Block diagram of a ROM

There are N number of data lines, on which the stored data can be outputted, when the read (RD) input is active.

Internal Logic of a ROM:

Let us understand the internal logic of a 8 X 4 ROM. A 8 X 4 ROM consists of 8 words of 4 bit each. To access 8 locations, we have to use 3 input lines which form the binary words equivalent to 0 to 7 i.e. 000 to 111. Figure below shows the internal structure of ROM.

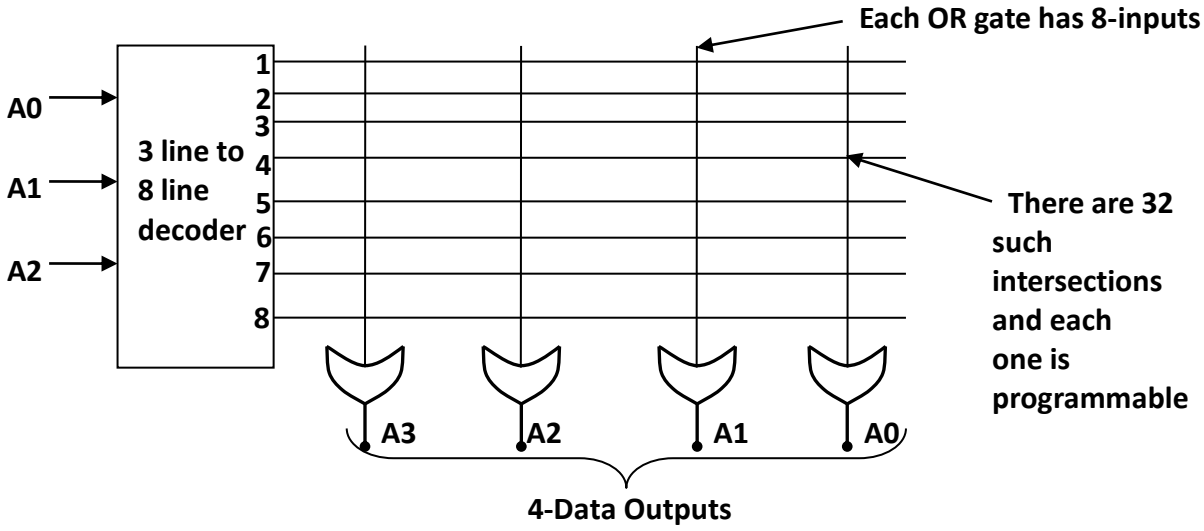


Figure 3.5.07: Internal structure of 8 x 4 ROM

The 3-inputs, A0,A1,A2 are decoded into 8 lines with the help of 3:8 line decoder. Each output of decoder represents a memory address. The 8-outputs are connected to each of the four OR gates. This means that each OR gate has 8-inputs, hence 32 internal connections. All 32 intersections are programmable (each interconnection is equivalent to a switch, ON or OFF, where ON means connection between two intersecting lines where as OFF means no connection). The programmable intersections is called as a crosspoint. The cross point is implemented using fuse link.

ROM TRUTH TABLE:

Location No.	Inputs			Outputs				
	A2	A1	A0	A3	A2	A1	A0	
0	0	0	0	**1**	**0**	**0**	**0**	**Data in location 0**
1	0	0	1	**1**	**1**	**0**	**0**	**Data in location 1**
2	0	1	0	**1**	**0**	**1**	**0**	**Data in location 2**
3	0	1	1	**0**	**0**	**1**	**1**	**Data in location 3**
4	1	0	0	**1**	**1**	**1**	**1**	**Data in location 4**
5	1	0	1	**0**	**0**	**0**	**0**	**Data in location 5**
6	1	1	0	**0**	**1**	**0**	**1**	**Data in location 6**
7	1	1	1	**1**	**0**	**0**	**1**	**Data in location 7**

The truth table shows that there are 3-input lines and 4-output lines. There are 8 locations (addresses) and at each location, an 4-bit word is stored.

Programming of a ROM:

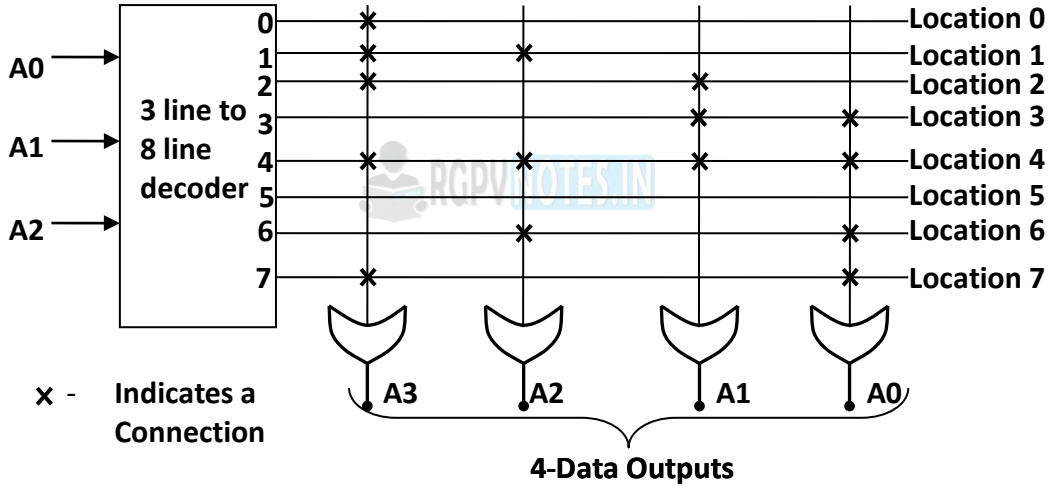


Figure 3.5.08: ROM Programmed according Truth Table

We consider location 0 of above figure. The word 1000 has been stored in this location. The 0's are stored by blowing OFF the fuse links between output 0 of decoder and input lines of OR gates, associated with A2,A1 and A0. The one 1 is marked by X.

PROGRAMMABLE LOGIC ARRAY (PLA):

Based on the idea that output logic functions can be realized in Sum –of – Product (SOP) form. As shown below in structure of PLA- PLA's inputs X1----- Xn, pass through set of buffers and inverters (which provide both the true and complement of each input) into a circuit block called AND plane or AND array. AND plane outputs are set of product terms P1-------Pk i.e. each product terms can be configured to implement any AND function of X1------Xn. Product terms (P1----Pk) serves as the input to OR-Plne which produces the output F1----Fk. Each output can be configured to realize any sum of P1-------Pk.

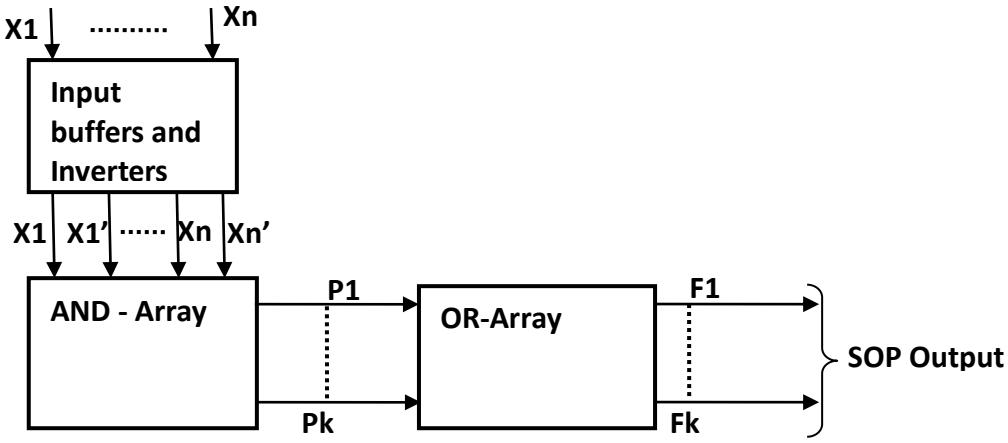


Figure 3.5.09: Block diagram of General Structure of PLA

Example: Implement the circuit using PLA with 3-inputs, 3-product terms and 2-outputs.

$F1(A,B,C) = \sum m(4,5,7)$ and $F2(A,B,C) = \sum m(3,5,7)$

Solution: On simplifying the function using K-Map method, we get the output expression as-

$F1 = A.B' + A.C$ and $F2 = A.C + B.C$

So, comparing F1 and F2, we get 3-product terms i.e. A.B', AC, BC

So, PLA table is-

Product Terms	Inputs			Outputs	
	A	B	C	F1	F2
A.C	1	-	1	1	1
B.C	-	1	1	-	1
A.B'	1	0	-	1	-

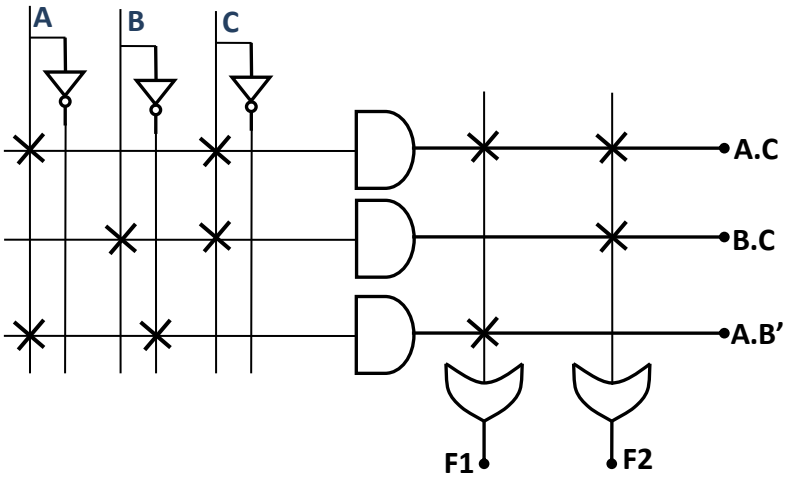


Figure 3.5.10 Circuit Implementation using PLA of above Example

3.6 INTRODUCTION TO DIGITAL ICS 2716 (NMOS EPROM), 2732 (NMOS EPROM) ETC.

Digital ICs M2716 is NMOS 16Kbit (2Kb x 8) UV EPROM and M2732 is NMOS 32Kbit (4Kb x 8) UV EPROM.

The M2716 is a 16,384 bit UV erasable and electrically programmable memory EPROM. The transparent window allows the user to expose the chip to ultraviolet light to erase the bit pattern.
VCC: Supply Voltage
VPP: Program Supply Voltage
G': Output Enable
E'P: Chip Enable
A0-A10: Address Line
Q0-Q7: Data Line

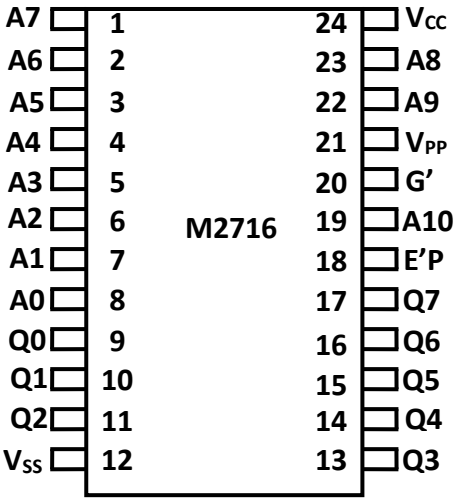


Figure 3.6.1 IC 2716 PIN Configuration

DEVICE OPERATION
The M2716 has 6 modes of operation shown in table below.

MODE	E'P	G'	V_{PP}	Q0-Q7
Read	V_{IL}	V_{IL}	V_{CC}	Data Out
Program	V_{IH} Pulse	V_{IH}	V_{PP}	Data In
Verify	V_{IL}	V_{IL}	V_{CC} or V_{PP}	Data Out
Program Inhibit	V_{IL}	V_{IH}	V_{PP}	Hi-Z
Deslect	X (V_{IH} or V_{IL})	V_{IH}	V_{CC}	Hi-Z
Standby	V_{IH}	X (V_{IH} or V_{IL})	V_{CC}	Hi-Z

V_{IH}: Input High Voltage; V_{IL}: Input Low Voltage

Read Mode. The M2716 read operation requires that G' = V_{IL}, E'P = V_{IL} and that addresses A0-A10 have been stabilized. Valid data will appear on the output pins after some switching time depending on which is limiting.
Deselect Mode. The M2716 is deselected by making G' = V_{IH}. This mode is independent of E'P and the condition of the addresses. The outputs are Hi-Z when G' = V_{IH}. This allows tied-OR of 2 or more M2716's for memory expansion.
Standby Mode (Power Down). The M2716 may be powered down to the standby mode by making E'P = V_{IH}. This is independent of G' and automatically puts the outputs in the Hi-Z state. The power is reduced to 25% (132 mW max) of the normal operating power. V_{CC} and V_{PP} must be maintained at 5V.
Programming
Table shows the 3 programming modes.
Program Mode. The M2716 is programmed by introducing "0"s into the desired locations. This is done 8 bits (a byte) at a time. Any individual address, sequential addresses, or addresses chosen at random may be programmed. Any or all of the 8 bits associated with an address location may be programmed with a single program pulse applied to the E'P pin. All input voltage levels including the program pulse on chip enable are TTL compatible. The programming sequence is: with V_{PP} = 25V, V_{CC} = 5V, G' = V_{IH} and E'P = V_{IL}, an address is selected and the desired data word is applied to the output pins (V_{IL} = "0" and V_{IH} = "1" for both address and data). After the address and data signals are stable the program pin is pulsed from V_{IL} to V_{IH} with a pulse width between 45ms and 55ms. Multiple pulses are not needed but will not cause device damage. No pins should be left open. A high level (V_{IH} or

higher) must not be maintained longer on the program pin during programming. M2716's may be programmed in parallel in this mode.

Program Verify Mode. The programming of the M2716 may be verified either one byte at a time during the programming or by reading all of the bytes out at the end of the programming sequence. This can be done with V_{PP} = 25V or 5V in either case. V_{PP} must be at 5V for all operating modes and can be maintained at 25V for all programming modes.

Program Inhibit Mode. The program inhibit mode allows several M2716's to be programmed simultaneously with different data for each one by controlling which ones receive the program pulse. All similar inputs of the M2716 may be paralleled. Pulsing the program pin (from V_{IL} to V_{IH}) will program a unit while inhibiting the program pulse to a unit will keep it from being programmed and keeping G' = V_{IH} will put its outputs in the Hi-Z state.

ERASURE OPERATION

The M2716 is erased by exposure to high intensity ultraviolet light through the transparent window. This exposure discharges the floating gate to its initial state through induced photo current. It is recommended that the M2716 be kept out of direct sunlight. The UV content of sunlight may cause a partial erasure of some bits in a relatively short period of time.

The M2716 to be erased should be placed 1 inch away from the lamp and no filters should be used. Lamps lose intensity as they age, it is therefore important to periodically check that the UV system is in good order.This will ensure that the EPROMs are being completely erased. Incomplete erasure will cause symptoms that can be misleading.

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