Sequential Logic circuits

Introduction to Sequential Logic Circuits

Sequential logic circuit are the Digital circuits where output is determined by the present input and past inputs

These type of circuits contains memory as feedback and sequence of inputs determines the output

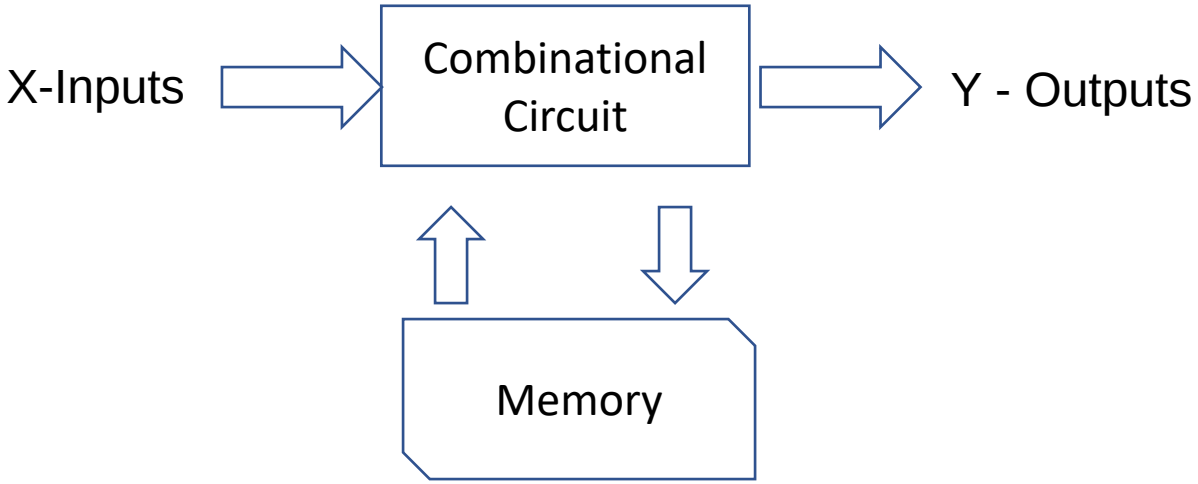
> E.g., flip-flops, data storage cells in registers, memory, counters, & control logic in processor

Therefore, these circuits produce different outputs for the same set of inputs depending on what is stored in memory

Block diagram of a sequential logic circuit

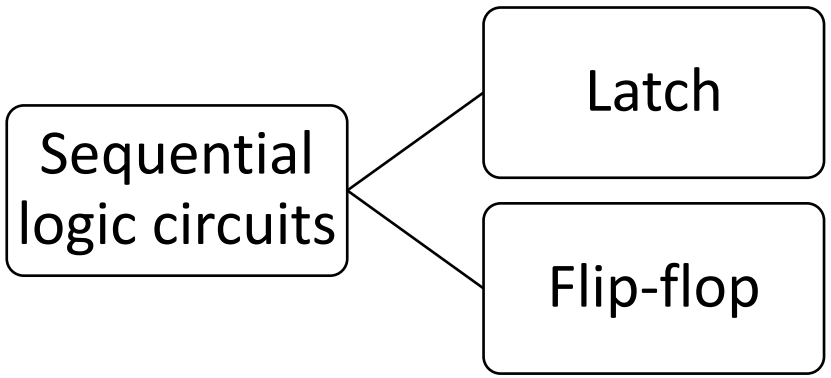
- Main features

1. At least one feedback path from the input to the output of the system
2. System has memory capability to hold past inputs
3. The circuits that output depends to inputs only known as combinational logic circuits where for sequential logic circuit's output depends on not only inputs but also the past outputs



- Sequential logic circuits ate basically two types

  - Synchronous logic circuit- Response to the input when discrete time intervals
  - Asynchronies logic circuit- Response to the input only at input level change

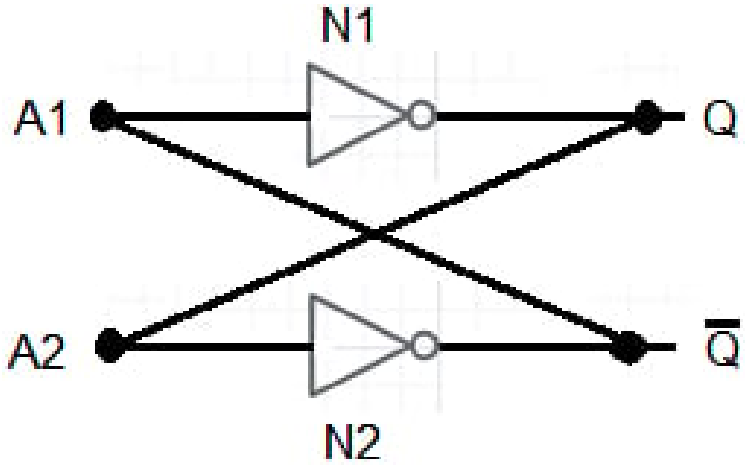


Sensitive for input level changes. When input change occurs the output get change where know as level triggered

Sensitive for input only at a clock transmission. Flip-flop has edge triggered (raising or falling edge triggered) memory element

Latch

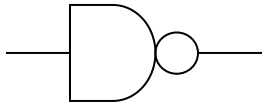
- A latch is a data storage (memory) device that can store one bit of information.
- The basic type of Latch is two NOT gate Latch
- A logic gate itself doesn’t have an ability to hold a logic value rather than passing the logic through logic gate
- Combination of two logic gates has an ability to hold a logic value and act as a memory

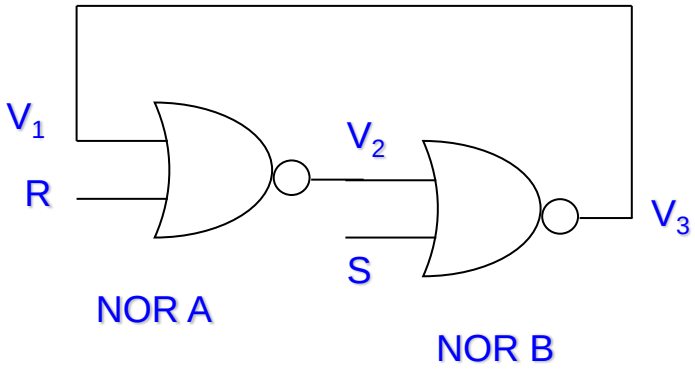


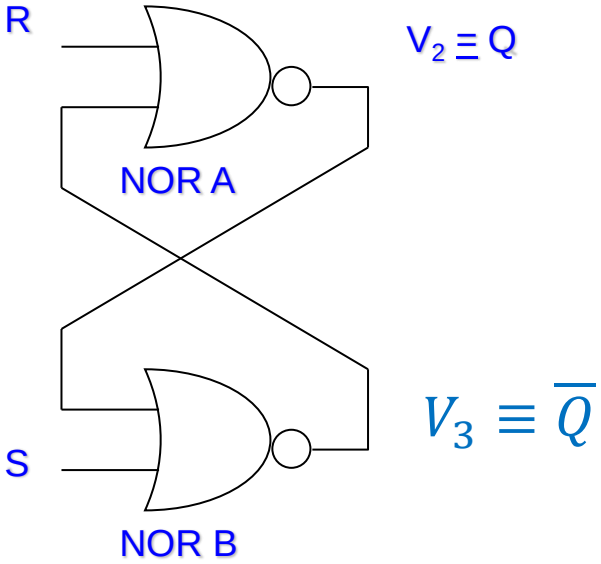
Latch

- Latches are basically two types
  - NOR Gate Latch
  - NAND Gate Latch

NOR Gate Latch







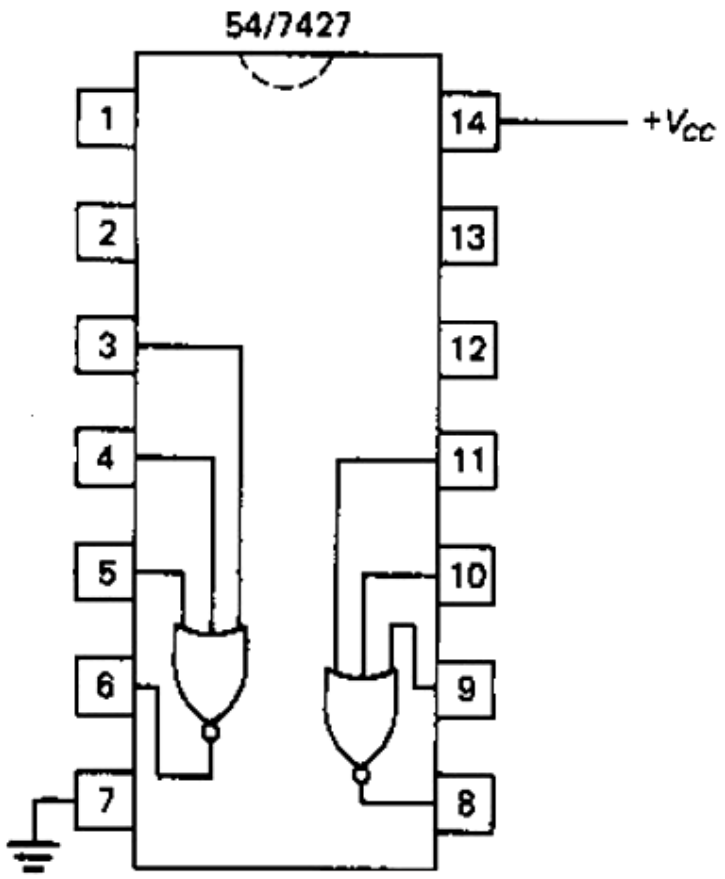
R	S	Q	Action
0	0	Last Value	No Change
0	1	1	Set
1	0	0	Reset
1	1	?	Not Allowed

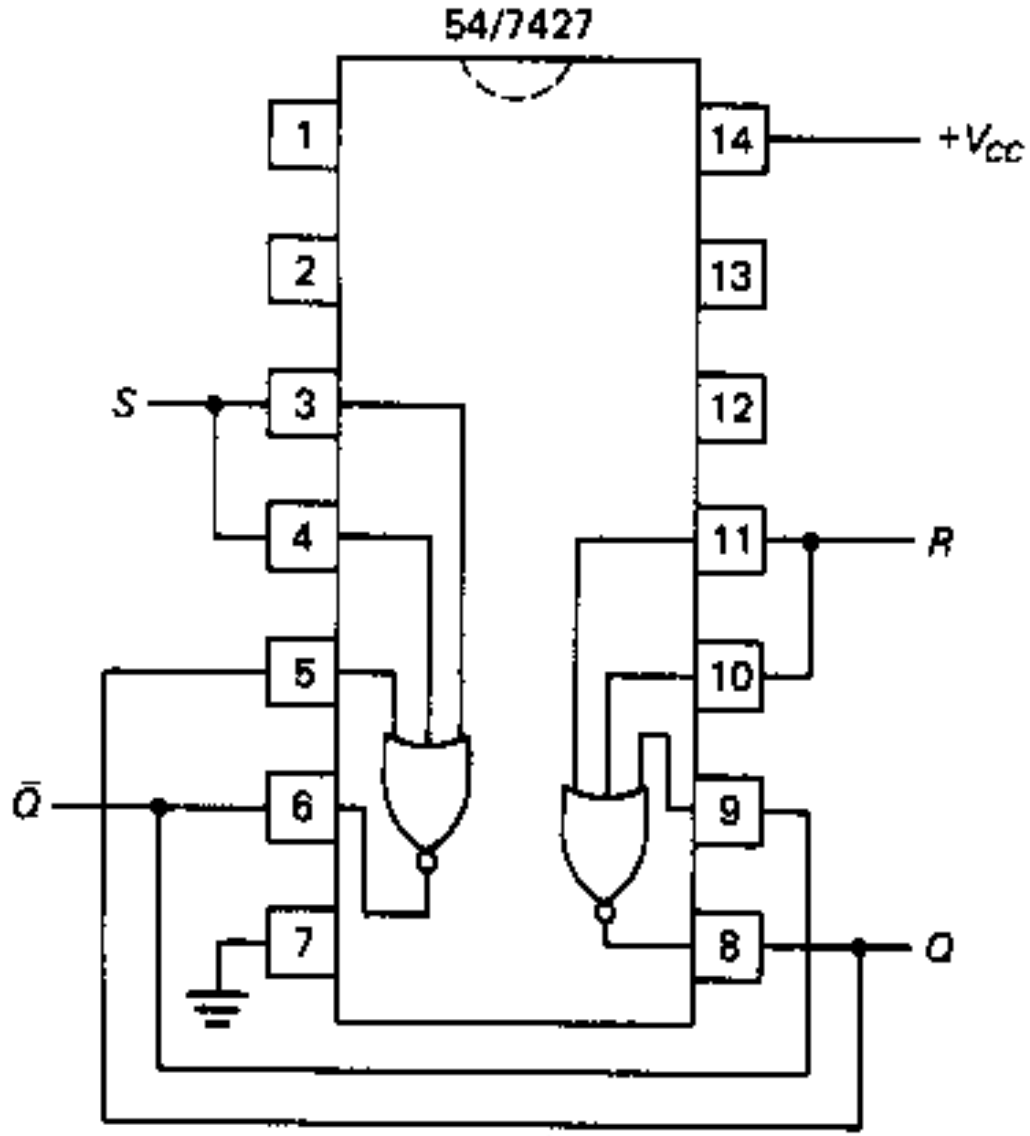
Truth table with all states :

S	R	Qn	$\overline{Q}$n	Q_{n+1}	$\overline{Q_{n+1}}$
0	0	0	1	0	1
		1	0	1	0
0	1	0	1	0	1
		1	0		
1	0	0	1	1	0
		1	0		
1	1	0	1	Not allowed	
		1	0		

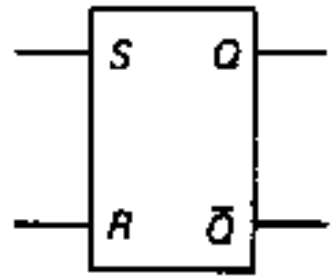
EXAMPLE

Use the pinout diagram for a 54/7427 triple 3-input NOR gate and show how to connect a simple *RS* flip-flop.





54/7427



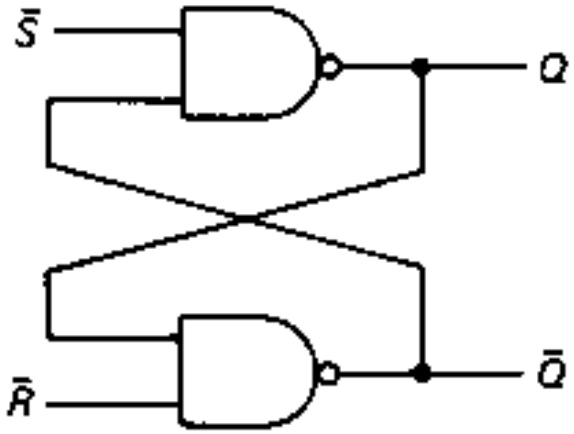
(*a*) Logic symbol

R	*S*	*Q*
0	0	Last state
0	1	1
1	0	0
1	1	? (Forbidden)

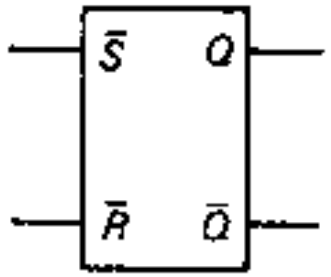
(*b*) Truth table

RS flip-flop

NAND Gate Latch



(a) NAND gate latch



(b) Logic symbol

$\bar{R}$	$\bar{S}$	Q
1	1	Last state
1	0	1
0	1	0
0	0	? (Forbidden)

(c) Truth table

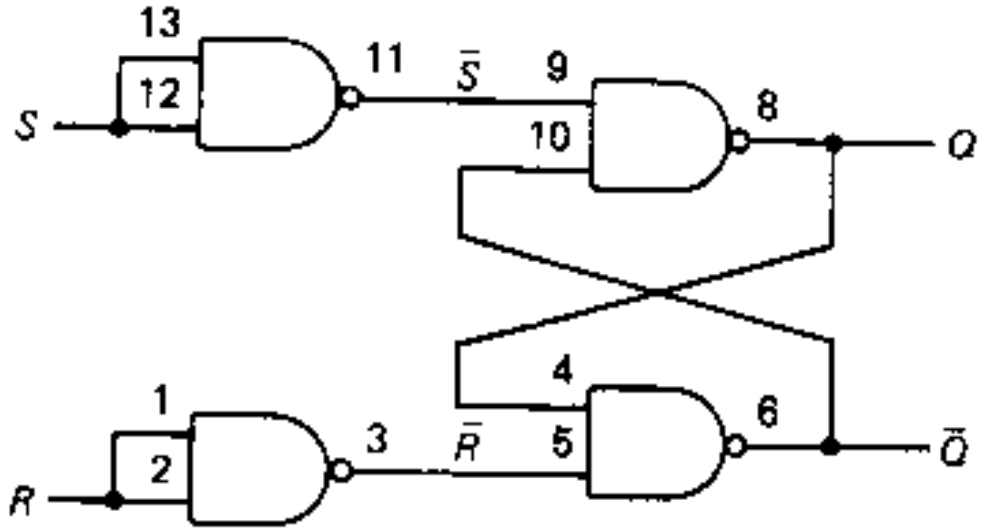
$\overline{R}\overline{S}$ flip-flop

EXAMPLE

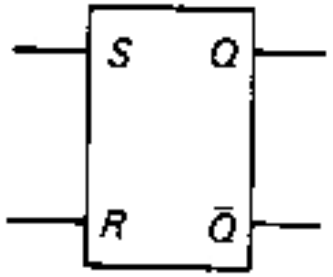
Show how to convert the $\overline{R}\overline{S}$ flip-flop into an RS flip-flop.

Solution:

By placing an inverter at each input shown in figure below, 2 inputs are now R and S, and resulting circuit behaves exactly as the RS flip-flop



(a) 54/7400



(b) Symbol

R	S	Q
0	0	Last state
0	1	1
1	0	0
1	1	? (Forbidden)

(c)

An RS flip-flop (latch)

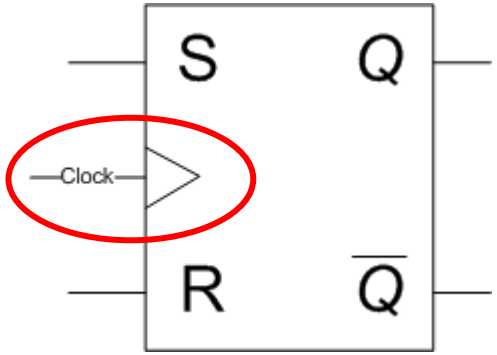
Flip – Flop

Flip Flops can change it’s state continues either 0 0r 1 logic levels

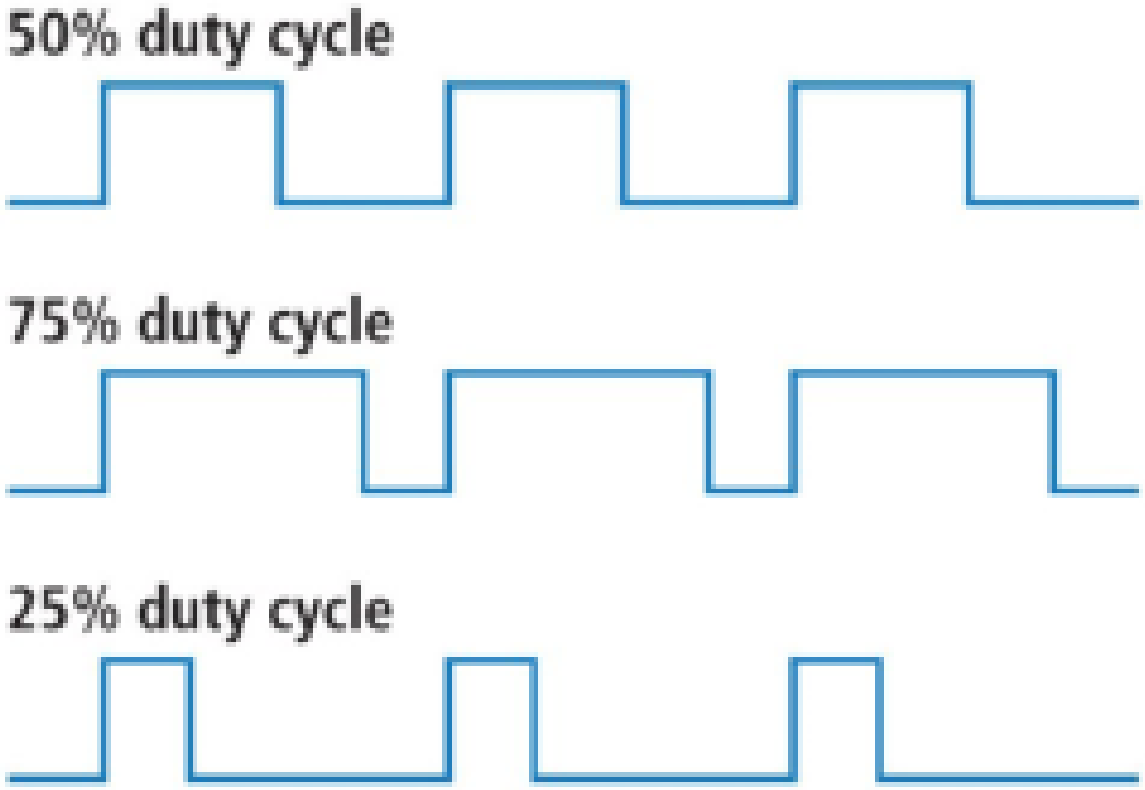
A Clock cycle has been provided additionally with the inputs of the flip – flops where it differs from Latches

Continues logic level changing occurs when input got triggered with a clock cycles

There are level triggered and edge triggered (riding or falling edge) flip flops according to the clock cycles



Types of Clock Cycles



Equal time of on and off time

Raising time is high falling time is low

Raising time is low falling time is high

In Physically clock cycles are provided by 555 timer IC’s

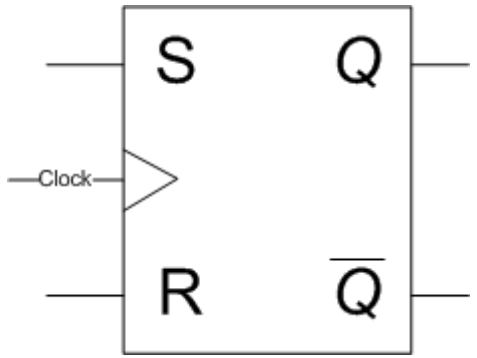
Type of Flip- Flops

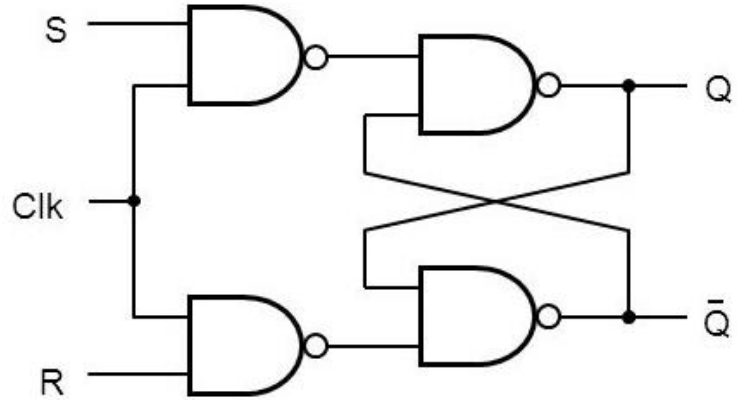
- SR Flip Flop
- JK Flip Flop
- D- Flip Flop
- T – Flip Flop

S-R Flip Flop

Truth Table

S	R	Q_{n-1}
0	0	Q_n
0	1	0 (Reset)
1	0	1 (Set)
1	1	Not allowed





Excitation Table

Qn		S	R
0	0	0	0
		0	1
0	1	1	0
1	0	0	1
1	1	0	0
		1	0

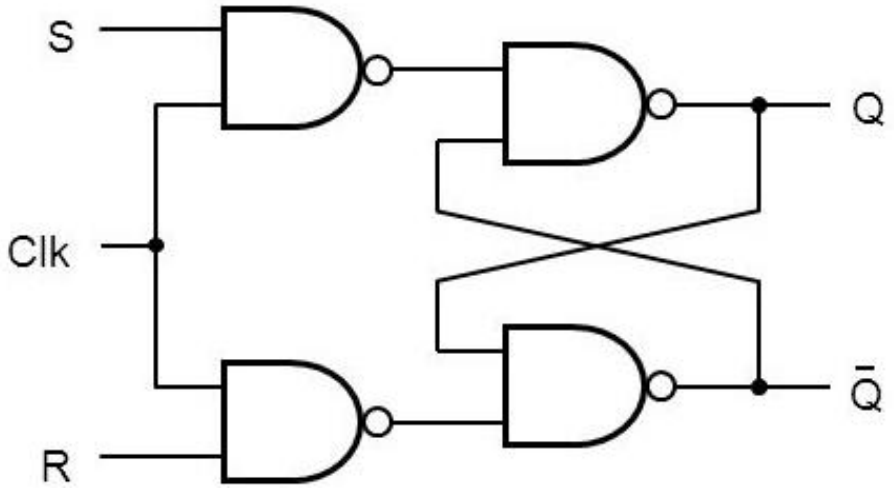
Qn		S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

SR Flip Flop with NAND Gate

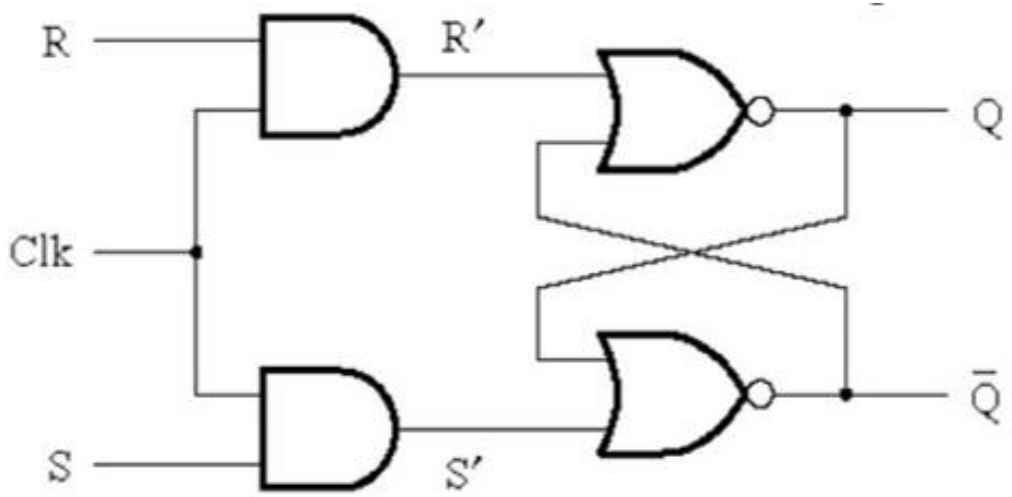
CK	S	R	Q_{n+1}
0	0	0	Q_n
0	0	1	Q_n
0	1	0	Q_n
0	1	1	Q_n
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	NA

When CK is low $Q_{n+1} = Q_n$

Clk	S	R	Q_n
0	X	X	Q_{n-1}
1	0	0	Q_{n-1}
1	0	1	0
1	1	0	1
1	1	1	X

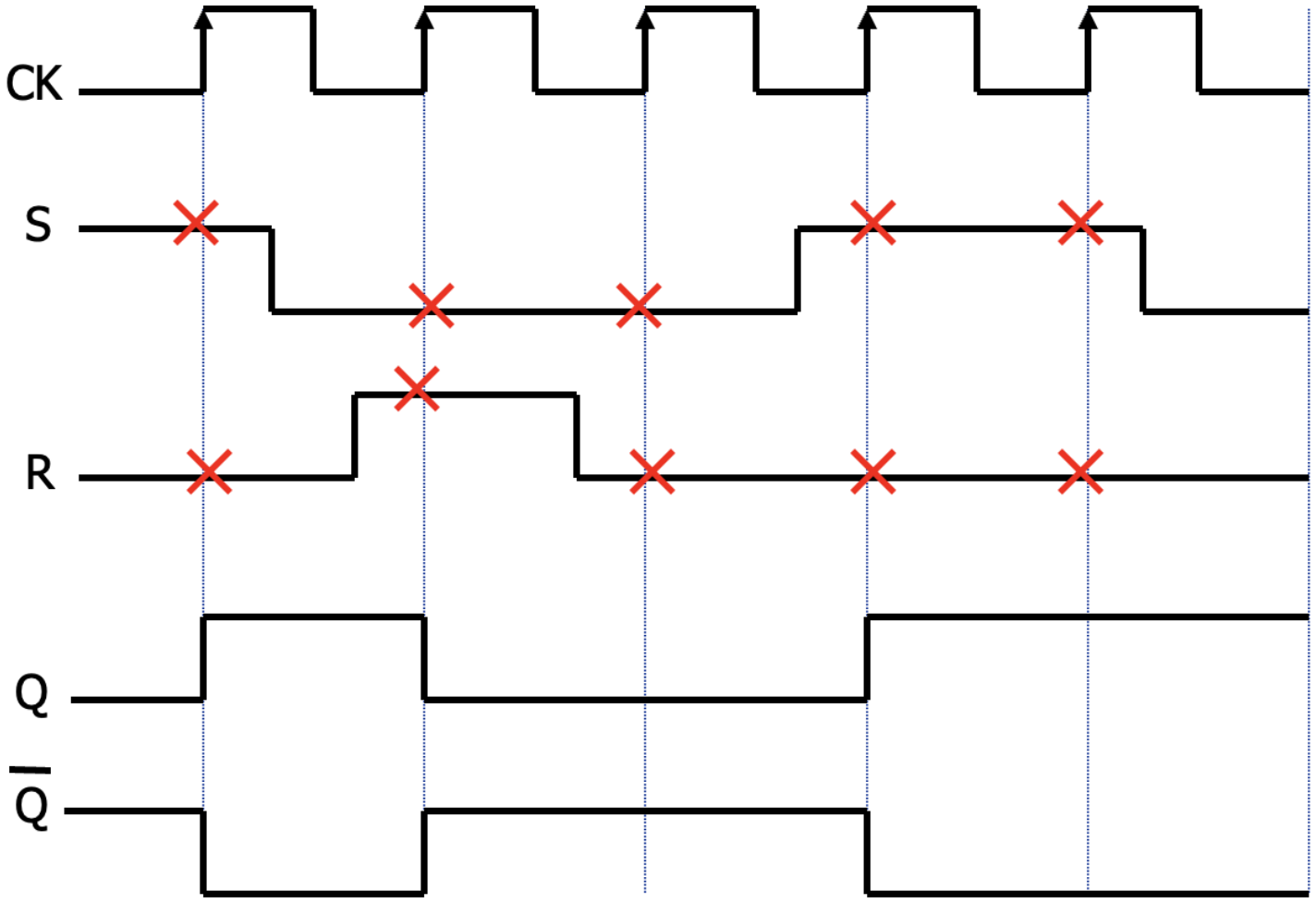


SR Flip Flop NOR Gate

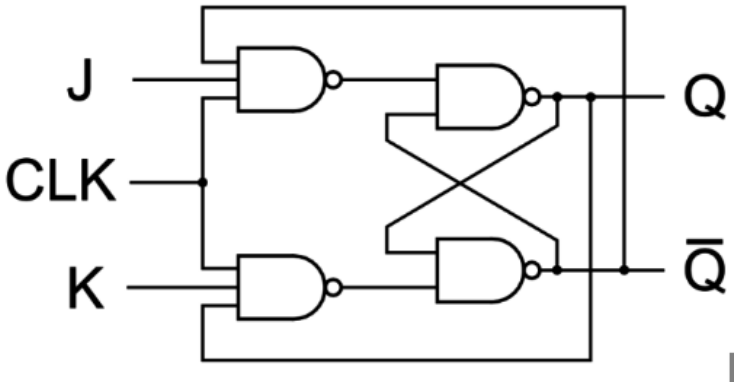


Clk	S	R	Q_n
0	X	X	Q_{n-1}
1	0	0	Q_{n-1}
1	0	1	0
1	1	0	1
1	1	1	X

Draw the output waveform for the (+)ve edge triggered SR FF

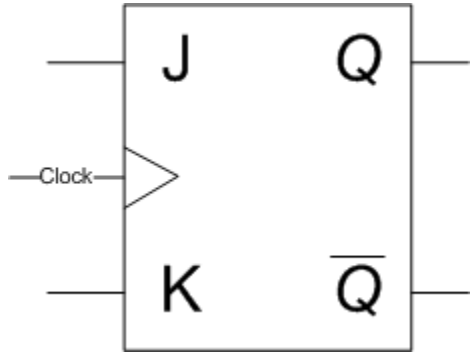


JK Flip- Flop



Truth Table

J	K	Q_n
0	0	Q_{n-1}
0	1	0
1	0	1
1	1	Q_{n-1}'

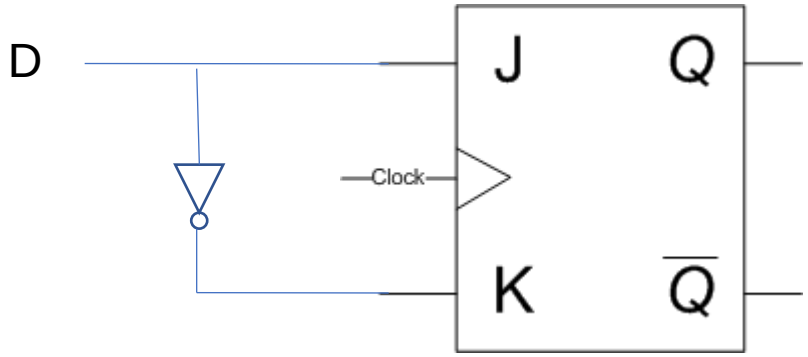


Excitation Table

Qn		J	K
0	0	0	0
		0	1
0	1	1	0
		1	1
1	0	0	1
		1	1
1	1	0	0
		1	0

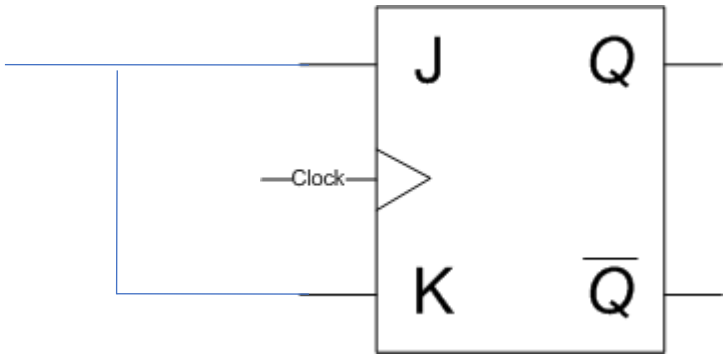
Qn		J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

D Flip - Flop



J (= D)	K (=D')	Q_n
0	1	0
1	0	0

T Flip – Flop (Toggle)



J (= K)	K (=J)	Q_n
0	0	Q_{n-1}
1	1	Q_{n-1}'