128Gb Based NAND Flash

128Gb, 256Gb, 512Gb, 1Tb and 2Tb NAND Flash

Specification

1. Introduction for 1xnm 128Gb TLC Product

■ **Toggle DDR**
- Density : 16GB, 32GB, 64GB, 128GB and 256GB
- Interface Speed : 400M B/s or 200M B/s
- Voltage : Vcc=3.3V, VccQ=1.8V or Vcc=3.3V, VccQ=3.3V
- Package Type : 132Ball fBGA or 316Ball fBGA

■ **Legacy**
- Density : 16GB
- Interface Speed : Legacy mode speed
- Voltage : Vcc=3.3V
- Package Type : 48pin TSOP

1.1. Product List

Table 1-1. 400Mbps product list

Toggle DDR 400Mbps (max)					
P/N	**Density**	**Vcc/VccQ**	**I/O Speed**	**# of CE RB#**	**PACKAGE**
H27QDG8M2M5R-BCF	16GB (128Gb)	Vcc 3.3V / VccQ 1.8V	400Mb/s	1$\overline{CE}$ & 1R/$\overline{B}$, single	132Ball fBGA
H27QEG8NDM5R-BCF	32GB (256Gb)	Vcc 3.3V / VccQ 1.8V	400Mb/s	2$\overline{CE}$ & 2R/$\overline{B}$, dual	132Ball fBGA
H27QFG8PEM5R-BCF	64GB (512Gb)	Vcc 3.3V / VccQ 1.8V	400Mb/s	4$\overline{CE}$ & 4R/$\overline{B}$, dual	132Ball fBGA
H27Q1T8QEM6R-BCF	128GB (1Tb)	Vcc 3.3V / VccQ 1.8V	400Mb/s	4$\overline{CE}$ & 4R/$\overline{B}$, dual	132Ball fBGA
H27Q1T8QAM6R_BCF	128GB(1Tb)	Vcc 3.3V / VccQ 1.8V	400Mb/s	8$\overline{CE}$ & 4R/$\overline{B}$, dual	132Ball fBGA
H27Q2T8LAM9R-BCF	256GB(2Tb)	Vcc 3.3V / VccQ 1.8V	300Mb/s	8$\overline{CE}$ & 4R/$\overline{B}$, dual	152Ball fBGA
H27QFG8PQM2R-BCF	64GB (512Gb)	Vcc 3.3V / VccQ 1.8V	400Mb/s	4$\overline{CE}$ & 4R/$\overline{B}$, quad	316Ball fBGA
H27Q1T8QQM3R-BCF	128GB (1Tb)	Vcc 3.3V / VccQ 1.8V	400Mb/s	4$\overline{CE}$ & 4R/$\overline{B}$, quad	316Ball fBGA
H27Q1T8QRM3R-BCF	128GB (1Tb)	Vcc 3.3V / VccQ 1.8V	400Mb/s	8$\overline{CE}$ & 4R/$\overline{B}$, quad	316Ball fBGA
H27Q2T8LQM3R-BCF	256GB (2Tb)	Vcc 3.3V / VccQ 1.8V	400Mb/s	4$\overline{CE}$ & 4R/$\overline{B}$, quad	316Ball fBGA

The SKHynix Toggle mode NAND Flash memory contain 128Gb TLC devices in 132Ball fBGA and 316 Ball fBGA packages. The H27Qxx8(M/N/P/Q/L)xxxR-BCF Series series are also available as one, two, four, or eight 128Gb based devices. Not all possible configurations are currently available.

Table 1-2. 200Mbps product list

Toggle DDR 200Mbps (max)					
P/N	**Density**	**Vcc/VccQ**	**I/O Speed**	**# of CE RB#**	**PACKAGE**
H27QDG882MLR-BCC	16GB (128Gb)	Vcc 3.3V / VccQ 1.8V	200Mb/s	1CE & 1R/$\overline{B}$, single	132Ball fBGA
H27QEG89DMLR-BCC	32GB (256Gb)	Vcc 3.3V / VccQ 1.8V	200Mb/s	2CE & 2R/$\overline{B}$, Dual	

H27Qxx8(8/9)xxxR-BCC Series are support an emerging product like a USB3.0 by 200Mbps operation product without external power voltage. It is backward compatible with the functions and commands supported in toggle H27Qxx8(M/N/P/Q/L)xxxR-BCF Series.

Table 1-3. Legacy product list

Legacy Product				
P/N	**Density**	**Vcc**	**# of CE RB#**	**PACKAGE**
H27UDG8M2MTR-BC	16GB (128Gb)	Vcc 3.3V	1CE & 1R/$\overline{B}$, single	48 pin TSOP

The H27UDG8M2MTR-BC is 48 pin TSOP package for legacy operation.

1.2. Part number Information

H	2	7	x	x	x	x	x	x	x	x	x	-	x	x	x
1~3			4	5~6		7	8	9	10	11	12	13	14	15	16

#1 ~ #3: Memory
H27: SKHynix NAND Flash

#4: Power supply
U: 3.3V Vcc
Q: 3.3V Vcc, 3.3V or 1.8V VccQ

#5 ~ #6: Density
DG: 128Gb
EG: 256Gb
FG: 512Gb
1T: 1Tb
2T: 2Tb

#7: Input/Output Bus width
8: x8 input/output

#8: Die stack
M: TLC SDP
N: TLC DDP
P: TLC QDP
Q: TLC ODP
L: TLC HDP
8: Channel TLC SDP
9: Channel TLC DDP

#9: Configuration
2: 1CE & 1R/B, single
D: 2CE & 2R/B, dual
E: 4CE & 4R/B, dual
Q: 4CE & 4R/B, quad
A: 8CE & 4R/B, dual

#10: Generation
M: 1st product
A: 2nd product
B: 3rd product

#11: Package
T: 48 pin TSOP
5: 132-fBGA (12x18, t=1.0, D=550um)
6: 132-fBGA (12x18, t=1.35, D=550um)
2: 316-fBGA (14x18, t=1.0, D=550um)
3: 316-fBGA (14x18, t=1.35, D=550um)
D: Wafer (PGD-2)

#12: Package material
R: Green (Lead & Halogen free)
A: Wafer

#14: Bad block
B: Included bad block
P: All good block

#15: Temperature
C: Commercial temp. product
I: Industrial temp. product

#16: Input/output speed
Blank: Legacy speed
C: 100MHz (200Mb/s)
F: 200MHz (400Mb/s)

128Gb (3bit/cell) Based NAND Flash

Toggle DDR Specification

Document Title

Revision History

Revision No.	History	Date	Remark
1.0	- Release	July. 2014	Draft
1.1	- Updated contents and fixed typos - Add Table 3-5. for the number of valid blocks	Sep. 2014	
1.2	- Fixed some typos - Add VPP contents - Change tITC to tFEAT on page 40 - tDQSH/tDQSL is modified to tDQS*0.45 at table 4-4 - tREH/tRP is modified to tRC*0.45 at table 4-4 - Add tDQSRE min. and tRPP min. at table 4-4 - tDTBSY1/2 is updated at table 4-5 on page 57 , 2-5 on page 105 - Modified Register Read Out Mode figuer 5-33 on page 83 - Deleted MULTI-PLANE CACHE READ ENHANCED command at table 1-4 on page 102	Oct.2014	
1.3	- Change tBERS (SLC part) to 5ms(typ.) - Change tR(SLC part) to 65us(typ.) - Add tPROG (Channel) 2.2ms(typ.) - Change ISB to 50uA(max.) at table 2-7, 2-8 - Modify A3 of Figure 2-4	Oct.2014	
1.4	- Change tBERS of TLC from 5ms to 6.5ms - Add tCBSY to Table 4-5 - Add more descriptions about power on sequence - Add VCCQ setting method and set/get parameter sequence - Fix typos	Dec.2014	
1.5	- Add 8CE ODP 132ball, 8CE HDP 152ball to product list - Change tRST(program) 30us to 200us - Fix the FFh reset time after power-up on figure 5-1 of page 128 - Fix the figures of write protect on page 130	Feb. 2015	
1.6	- Remove ODT contents - Add note 3) to Figure 4-5 - Add VID(DC) to Table 2-12 - Add note to Figure 5-31	Apr. 2015	

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1. Toggle DDR Key Features

Key features

■ Multilevel Cell technology

■ NAND INTERFACE

- Toggle DDR Command Interface
- x8 bus width
- Multiplexed Command, Address and data signal port

■ Supply Voltage

Vcc : 2.7V ~ 3.6V, VccQ : 1.7V ~ 1.95V
- P/N: H27Qxx8(M/N/P/Q/L)xxxR-BCF Series (400Mbps)

Vcc : 2.7V ~ 3.6V, VccQ : 2.7V ~ 3.6V
- P/N: H27Qxx8(8/9)xxxR-BCC Series (200Mbps)

■ Organization

- (16,384+2,048)bytes x 258pages x (2,048 + 60)blocks x 2plane
- Page size : 16,384+2,048bytes
- Block size : 258pages x (16,384 + 2,048) bytes
- Pages per block: 258pages (86WL x 3bit)
- 2-Plane size : (4,096 blocks + 120 Extended blocks)

■ Page Read Time

	tR	
	Typ	**Max**
TLC part	100us	-
SLC part	65us	-

■ Page Read / Program Time

	tPROG		tPROG (Channel)	
	Typ	**Max**	**Typ**	**Max**
TLC part	2.0ms	-	2.2ms	-
SLC part	0.5ms	-	0.5ms	-

■ Block Erase

- Block Erase Time : 5ms (Typ)

	tBERS	
	Typ	**Max**
TLC part	6.5ms	10ms
SLC part	5ms	10ms

■ DQ performance

- Read cycle time :
  tRC = 5ns (H27Qxx8xxMxR-BCF)
  or tRC = 10ns (H27QxG8xxMLR-BCC)
- Read/Write throughput per pin : 400Mbps or 200Mbps

■ Single Die Operating Current

- Page Read : 50 mA (max.)
- Page Program : 50 mA (max.)
- DQ Burst Read (I_{CC4R}) : 80 mA (max.)
- DQ Burst Program(I_{CC4W}) : 80 mA (max.)
- BUS Idle : 20 mA (max.)
- Standby : 50 uA (max.)

■ Package

- 132Ball fBGA , Size : 12x18 mm^2
- 316Ball fBGA, Size : 14x18 mm^2
- 48-Pin TSOP, Size : 12x20 mm^2

■ Product

- 16GByte: single die stack
- 32GByte: two-die stack
- 64GByte: four-die stack
- 128GByte: eight-die stack

2. Physical specification

2.1. Packaging

132Ball fBGA assignments (top view)

Figure 2-1. H27QDG8M2M5R-BCF and H27QDG882MLR-BCC: 132ball 1$\overline{CE}$ & 1R/$\overline{B}$, Single Channel

	1	2	3	4	5	6	7	8	9	10	11
A	NC	NU	NC						NC	NC	NC
B	NC	NU	NC						NC	NC	NC
C	NC	NC	NC						NC	NC	NC
D	NC	VccQ	VccQ	NC	Vss		Vcc	NC	VccQ	VccQ	NC
E	NC	VssQ	NC	VssQ	NC		NC	VssQ	NC	VssQ	NC
F		NC	NC	NC	NC		NC	NC	NC	NC	
G		VssQ	VccQ	NC	NC		NC	NC	VccQ	VssQ	
H		NC	NC	NC	NC		NC	NC	NC	NC	
J		Vss	Vcc	R/$\overline{B}$	NC		NC	NC	Vcc	Vss	
K		NC	NC	$\overline{CE}$	NC		VPP	$\overline{WP}$	NC	NC	
L		VssQ	VccQ	NC	NC		CLE	ALE	VccQ	VssQ	
M		DQ7	DQ6	VREFQ	$\overline{WE}$		RE	$\overline{DQS}$	DQ1	DQ0	
N	NC	VssQ	DQ5	VssQ	$\overline{RE}$		DQS	VssQ	DQ2	VssQ	NC
P	NC	VccQ	VccQ	DQ4	Vcc		Vss	DQ3	VccQ	VccQ	NC
R	NC	NC	NC						NC	NC	NC
T	NC	NC	NC						NC	NC	NU
U	NC	NC	NC						NC	NC	NU

Note:
1) H27QDG882MR-BCC product Vpp and VREFQ pin is NU.
2) Vpp Pin: Depends on the use of customer. If you can't supplied External Vpp, this pin is NU.

Figure 2-2. H27QEG8NDM5R-BCF and H27QEG89DNLR-BCC: 132ball 2$\overline{CE}$ & 2R/$\overline{B}$, Dual Channel

	1	2	3	4	5	6	7	8	9	10	11
A	NU	NU	NC						NC	NC	NC
B	NU	NU	NC						NC	NC	NC
C	NC	NC	NC						NC	NC	NC
D	NC	VccQ	VccQ	DQ3_1	Vss		Vcc		VccQ	VccQ	NC
E	NC	VssQ	DQ2_1	VssQ	DQS_1		$\overline{RE}$_1	VssQ	DQ5_1	VssQ	NC
F		DQ0_1	DQ1_1	$\overline{DQS}$_1	RE_1		$\overline{WE}$_1	VREFQ_1	DQ6_1	DQ7_1	
G		VssQ	VccQ	ALE_1	CLE_1		NC	NC	VccQ	VssQ	
H		NC	NC	$\overline{WP}$1_1	NC		NC	$\overline{CE}$0_1	NC	NC	
J		Vss	Vcc	R/$\overline{B}$0	NC		NC	R/$\overline{B}$1	Vcc	Vss	
K		NC	NC	$\overline{CE}$0_0	NC		VPP	$\overline{WP}$_0	NC	NC	
L		VssQ	VccQ	NC	NC		CLE_0	ALE_0	VccQ	VssQ	
M		DQ7_0	DQ6_0	VREFQ_0	$\overline{WE}$1_0		RE_0	$\overline{DQS}$_0	DQ1_0	DQ0_0	
N	NC	VSSQ	DQ5_0	VssQ	$\overline{RE}$_0		DQS_0	VssQ	DQ2_0	VssQ	NC
P	NC	VccQ	VccQ	DQ4_0	Vcc		Vss	DQ3_0	VccQ	VccQ	NC
R	NC	NC	NC						NC	NC	NC
T	NC	NC	NC						NC	NU	NU
U	NC	NC	NC						NC	NU	NU

Note:
1) H27QEG89DNLR-BCC product Vpp and VREFQ pin is NU.
2) Vpp Pin: Depends on the use of customer. If you can't supplied External Vpp, this pin is NU.

Figure 2-3. H27QFG8PEM5R-BCF H27Q1T8QEM6R-BCF : 132ball 4$\overline{CE}$ & 4R/$\overline{B}$, Dual Channel

	1	2	3	4	5	6	7	8	9	10	11
A	NU	NU	NC						NC	NC	NC
B	NU	NU	NC						NC	NC	NC
C	NC	NC	NC						NC	NC	NC
D	NC	VccQ	VccQ	DQ3_1	Vss		Vcc	DQ4_1	VccQ	VccQ	NC
E	NC	VssQ	DQ2_1	VssQ	DQS_1		$\overline{RE}$_1	VssQ	DQ5_1	VssQ	NC
F		DQ0_1	DQ1_1	$\overline{DQS}$_1	RE_1		$\overline{WE}$_1	VREFQ_1	DQ6_1	DQ7_1	
G		VssQ	VccQ	ALE_1	CLE_1		NC	NC	VccQ	VssQ	
H		NC	NC	$\overline{WP}$1	NC		$\overline{CE}$1_1	$\overline{CE}$0_1	NC	NC	
J		Vss	Vcc	R/$\overline{B}$0	R/$\overline{B}$2		R/$\overline{B}$3	R/$\overline{B}$1	Vcc	Vss	
K		NC	NC	$\overline{CE}$0_0	$\overline{CE}$1_0		VPP	$\overline{WP}$_0	NC	NC	
L		VssQ	VccQ	NC	NC		CLE_0	ALE_0	VccQ	VssQ	
M		DQ7_0	DQ6_0	VREFQ_0	$\overline{WE}$1_0		RE_0	$\overline{DQS}$_0	DQ1_0	DQ0_0	
N	NC	VSSQ	DQ5_0	VssQ	$\overline{RE}$_0		DQS_0	VSSQ	DQ2_0	VssQ	NC
P	NC	VccQ	VccQ	DQ4_0	Vcc		Vss	DQ3_0	VccQ	VccQ	NC
R	NC	NC	NC						NC	NC	NC
T	NC	NC	NC						NC	NU	NU
U	NC	NC	NC						NC	NU	NU

Note:
1) Vpp Pin: Depends on the use of customer. If you can't supplied External Vpp, this pin is NU.

Figure 2-4. H27Q1T8QAM6R_BCF : 132ball 8$\overline{CE}$ & 4R/$\overline{B}$, Dual Channel

	1	2	3	4	5	6	7	8	9	10	11
A	NC	NC	NC						NC	NC	NC
B	NC	NC	NC						NC	NC	NC
C	NC	NC	NC						NC	NC	NC
D	NC	VccQ	VccQ	DQ3_1	Vss		Vcc	DQ4_1	VccQ	VccQ	NC
E	NC	VssQ	DQ2_1	VssQ	DQS_1		$\overline{RE}$_1	VssQ	DQ5_1	VssQ	NC
F		DQ0_1	DQ1_1	$\overline{DQS}$_1	RE_1		$\overline{WE}$_1	VREF1	DQ6_1	DQ7_1	
G		VssQ	VccQ	ALE_1	CLE_1		$\overline{CE3}$_1	$\overline{CE2}$_1	VccQ	VssQ	
H		NC	NC	$\overline{WP}$1	NC		$\overline{CE1}$_1	$\overline{CE0}$_1	NC	NC	
J		Vss	Vcc	R/$\overline{B}$0	R/$\overline{B}$2		R/$\overline{B}$3	R/$\overline{B}$1	Vcc	Vss	
K		NC	NC	$\overline{CE0}$_0	$\overline{CE1}$_0		NC	$\overline{WP}$_0	NC	NC	
L		VssQ	VccQ	$\overline{CE2}$_0	$\overline{CE3}$_0		CLE_0	ALE_0	VccQ	VssQ	
M		DQ7_0	DQ6_0	VREF_0	$\overline{WE1}$_0		RE_0	$\overline{DQS}$_0	DQ1_0	DQ0_0	
N	NC	VSSQ	DQ5_0	VssQ	$\overline{RE}$_0		DQS_0	VSSQ	DQ2_0	VssQ	NC
P	NC	VccQ	VccQ	DQ4_0	Vcc		Vss	DQ3_0	VccQ	VccQ	NC
R	NC	NC	NC						NC	NC	NC
T	NC	NC	NC						NC	NC	NC
U	NC	NC	NC						NC	NC	NC

132 ball fBGA, ODP (2-Ch, 8CE#)

Note:
1) Vpp Pin: Depends on the use of customer. If you can't supplied External Vpp, this pin is NU.

Figure 2-5. BGA-132 ball spacing requrements (top & view, dimensions in millimeters)

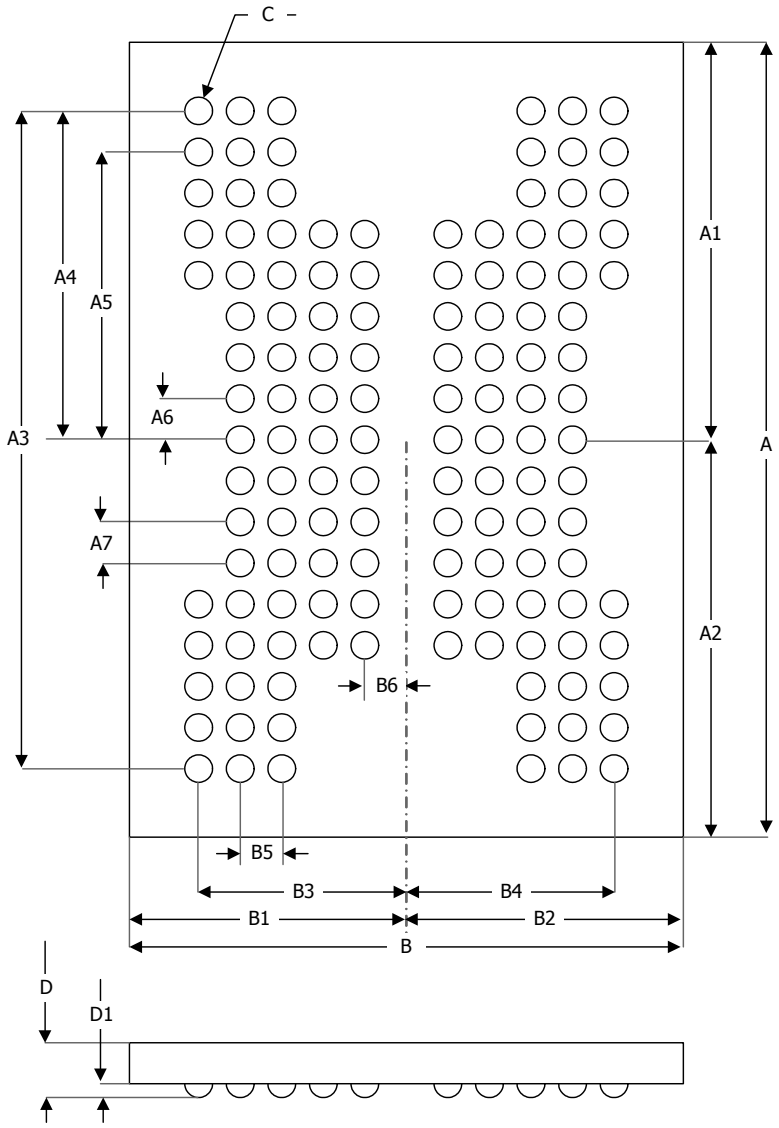


Figure 2-4. defines the ball spacing requirements for the 132-ball BGA package. The solder ball diameter is 0.55mm post reflow. The 132-ball BGA has one package size : 12mm x 18mm.

Table 2-1. BGA-132 ball 12mmx18mm, Package Mechanical Data

Symbol	Milimeters			Symbol	Milimeters		
	Min	Typ	Max		Min	Typ	Max
A	17.90	18	18.10	B	11.90	12	12.10
A1	-	9	-	B1	-	6	-
A2	-	9	-	B2	-	6	-
A3	-	16	-	B3	-	5	-
A4	-	8	-	B4	-	5	-
A5	-	7	-	B5	-	1	-
A6	-	1	-	B6	-	1	-
A7	-	1	-				
Symbol	**Milimeters**			**Symbol**	**Milimeters**		
	Min	**Typ**	**Max**		**Min**	**Typ**	**Max**
C	0.45	0.5	0.55	D Note1)	0.8	0.9	1.0
				D Note 2)	1.15	1.25	1.35
				D1	0.27	0.32	0.37

Note 1) H27QDG8M2M5R-BCF, H27QDG8M2M5R-BCF, H27QFG8PEM5R-BCF, H27QDG882MR-BCC and H27QEG89DNLR-BCC
Note 2) H27Q1T8QEM6R-BCF

Figure 2-6. H27Q2T8LAM9R-BCF: 152fBGA, 8$\overline{CE}$ & 4R/$\overline{B}$ Dual Channel

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	NC	NC	NC	NC						NC	NC	NC	NC
B	NC	NC	NC	NC						NC	NC	NC	NC
C	NC	NC	NC	NC						NC	NC	NC	NC
D	NC	NC	VccQ	VccQ	DQ3_1	Vss		Vcc	DQ4_1	VccQ	VccQ	NC	NC
E	NC	NC	VssQ	DQ2_1	VssQ	DQS_1		$\overline{RE}$_1	VssQ	DQ5_1	VssQ	NC	NC
F			DQ0_1	DQ1_1	$\overline{DQS}$_1	RE_1		$\overline{WE}$_1	VREF1	DQ6_1	DQ7_1		
G			VssQ	VccQ	ALE_1	CLE_1		$\overline{CE}$3_1	$\overline{CE}$2_1	VccQ	VssQ		
H			NC	NC	$\overline{WP}$1	NC		$\overline{CE}$1_1	$\overline{CE}$0_1	NC	NC		
J			Vss	Vcc	R/$\overline{B}$0	R/$\overline{B}$2		R/$\overline{B}$3	R/$\overline{B}$1	Vcc	Vss		
K			NC	NC	$\overline{CE}$0_0	$\overline{CE}$1_0		NC	$\overline{WP}$_0	NC	NC		
L			VssQ	VccQ	$\overline{CE}$2_0	$\overline{CE}$3_0		CLE_0	ALE_0	VccQ	VssQ		
M			DQ7_0	DQ6_0	VREF_0	$\overline{WE}$1_0		RE_0	$\overline{DQS}$_0	DQ1_0	DQ0_0		
N	NC	NC	VSSQ	DQ5_0	VssQ	$\overline{RE}$_0		DQS_0	VSSQ	DQ2_0	VssQ	NC	NC
P	NC	NC	VccQ	VccQ	DQ4_0	Vcc		Vss	DQ3_0	VccQ	VccQ	NC	NC
R	NC	NC	NC	NC						NC	NC	NC	NC
T	NC	NC	NC	NC						NC	NC	NC	NC
U	NC	NC	NC	NC						NC	NC	NC	NC

152 ball fBGA, (2-Ch, 8CE#)

Note:

1) Vpp Pin: Depends on the use of customer. If you can't supplied External Vpp, this pin is NU.

Figure 2-7. BGA-152 ball spacing requrements (top & view, dimensions in millimeters)

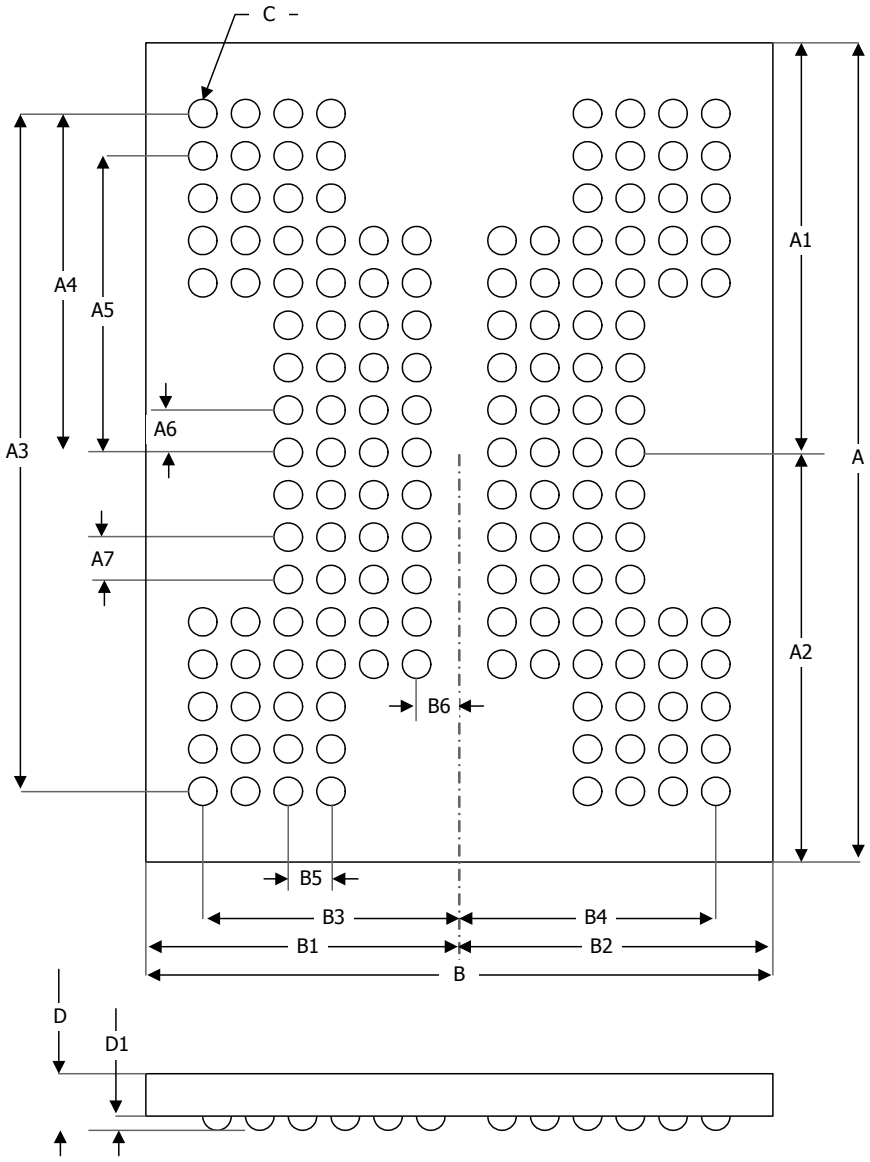


Figure 2-5. defines the ball spacing requirements for the 152-ball BGA package. The solder ball diameter is 0.55mm post reflow. The 152-ball BGA has one package size : 14mm x 18mm.

Table 2-2. 152-fBGA 14x18mm, Package Mechanical Data

Symbol	Milimeters			Symbol	Milimeters		
	Min	Typ	Max		Min	Typ	Max
A	17.90	18	18.10	B	13.90	14	14.10
A1	-	9	-	B1	-	7	-
A2	-	9	-	B2	-	7	-
A3	-	16	-	B3	-	6	-
A4	-	8	-	B4	-	6	-
A5	-	7	-	B5	-	1	-
A6	-	1	-	B6	-	1	-
A7	-	1	-				
Symbol	**Milimeters**			**Symbol**	**Milimeters**		
	Min	**Typ**	**Max**		**Min**	**Typ**	**Max**
C	0.50	0.55	0.60	D	0.8	0.9	1.0
				D	1.15	1.25	1.35
				D1	0.27	0.32	0.37

Figure 2-8. H27QFG8PQM2R-BCF H27Q1T8QQM3R-BCF and H27Q2T8LQM3R-BCF: 316ball 4$\overline{CE}$ Quad-Channel

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
B	NC	NC	NC	VCCQ	VssQ	VCCQ	VSSQ	VREF	VCC	VSS	VCC	VSS	VCC	NC	NC	NC
C	NC	NC	VSSQ	VCC	VSS	DQ7_2	DQ7_0			VCCQ	NC	NC	NC	VPP	NC	NC
D	NC	VCC	VSS	NC	NC	DQ6_2	DQ6_0			VSSQ	NC	NC	NC	VSS	VCC	NC
E	NC	VCCQ	VSSQ	NC	NC	DQ5_2	DQ5_0			NC	R/$\overline{B}$0_2	NC	NC	NC	NC	NC
F	NC	NC	NC	VCCQ	VSSQ	DQ4_2	DQ4_0			NC	R/$\overline{B}$0_0	NC	NC	NC	VSS	NC
G	NC	VCCQ	VSSQ	VCC	VSS	DQS_2	DQS_0			$\overline{WP}$_0	$\overline{WP}$_2	NC	NC	NC	VCC	NC
H	NC	VCC	VSS	VCCQ	VSSQ	$\overline{DQS}$_2	$\overline{DQS}$_0			CLE_0	CLE_2	NC	NC	NC	NC	NC
J	NC	NC	NC	NC	DQ3_2	DQ3_0	RE_2			RE_0	ALE_2	$\overline{CE}$0_2	NC	NC	VSS	NC
K	NC	VCCQ	VSSQ	NC	DQ2_2	DQ2_0	$\overline{RE}$_2			$\overline{RE}$_0	ALE_0	$\overline{CE}$0_0	NC	NC	VCC	NC
L	NC	NC	VREF	NC	DQ1_2	DQ1_0	$\overline{WE}$_2			$\overline{WE}$_0	DQ0_1	DQ0_3	NC	VSSQ	VCCQ	NC
M	NC	VCCQ	VSSQ	NC	DQ0_2	DQ0_0	$\overline{WE}$_1			$\overline{WE}$_3	DQ1_1	DQ1_3	NC	VREF	NC	NC
N	NC	VCC	NC	NC	$\overline{CE}$0_1	ALE_1	$\overline{RE}$_1			$\overline{RE}$_3	DQ2_1	DQ2_3	NC	VSSQ	VCCQ	NC
P	NC	VSS	NC	NC	$\overline{CE}$0_3	ALE_3	RE_1			RE_3	DQ3_1	DQ3_3	NC	NC	NC	NC
R	NC	NC	NC	NC	NC	CLE_3	CLE_1			$\overline{DQS}$_1	$\overline{DQS}$_3	VSSQ	VCCQ	VSS	VCC	NC
T	NC	VCC	NC	NC	NC	$\overline{WP}$_3	$\overline{WP}$_1			DQS_1	DQS_3	VSS	VCC	VSSQ	VCCQ	NC
U	NC	VSS	NC	NC	NC	R/$\overline{B}$0_1	NC			DQ4_1	DQ4_3	VSSQ	VCCQ	NC	NC	NC
V	NC	NC	NC	NC	NC	R/$\overline{B}$0_3	NC			DQ5_1	DQ5_3	NC	NC	VSSQ	VCCQ	NC
W	NC	VCC	VSS	NC	NC	NC	VSSQ			DQ6_1	DQ6_3	NC	NC	VSS	VCC	NC
Y	NC	NC	VPP	NC	NC	NC	VCCQ			DQ7_1	DQ7_3	VSS	VCC	VSSQ	NC	NC
AA	NC	NC	NC	VCC	VSS	VCC	VSS	VCC	VREF	VSSQ	VCCQ	VSSQ	VCCQ	NC	NC	NC
AB	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC

316 ball fBGA (4-Ch, 4CE#)

Note:

1) Vpp Pin: Depends on the use of customer. If you can't supplied External Vpp, this pin is NU.

Figure 2-9. H27Q1T8QRM3R-BCF: 316ball 8$\overline{CE}$ Quad-Channel

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
B	NC	NC	NC	VCCQ	VssQ	VCCQ	VSSQ	VREF	VCC	VSS	VCC	VSS	VCC	NC	NC	NC
C	NC	NC	VSSQ	VCC	VSS	DQ7_2	DQ7_0			VCCQ	NC	NC	NC	VPP	NC	NC
D	NC	VCC	VSS	NC	NC	DQ6_2	DQ6_0			VSSQ	NC	NC	NC	VSS	VCC	NC
E	NC	VCCQ	VSSQ	NC	NC	DQ5_2	DQ5_0			NC	R/$\overline{B}$0_2	NC	NC	NC	NC	NC
F	NC	NC	NC	VCCQ	VSSQ	DQ4_2	DQ4_0			NC	R/$\overline{B}$0_0	NC	NC	NC	VSS	NC
G	NC	VCCQ	VSSQ	VCC	VSS	DQS_2	DQS_0			$\overline{WP}$_0	$\overline{WP}$_2	$\overline{CE}$1_2	NC	NC	VCC	NC
H	NC	VCC	VSS	VCCQ	VSSQ	$\overline{DQS}$_2	$\overline{DQS}$_0			CLE_0	CLE_2	$\overline{CE}$1_0	NC	NC	NC	NC
J	NC	NC	NC	NC	DQ3_2	DQ3_0	RE_2			RE_0	ALE_2	$\overline{CE}$0_2	NC	NC	VSS	NC
K	NC	VCCQ	VSSQ	NC	DQ2_2	DQ2_0	$\overline{RE}$_2			$\overline{RE}$_0	ALE_0	$\overline{CE}$0_0	NC	NC	VCC	NC
L	NC	NC	VREF	NC	DQ1_2	DQ1_0	$\overline{WE}$_2			$\overline{WE}$_0	DQ0_1	DQ0_3	NC	VSSQ	VCCQ	NC
M	NC	VCCQ	VSSQ	NC	DQ0_2	DQ0_0	$\overline{WE}$_1			$\overline{WE}$_3	DQ1_1	DQ1_3	NC	VREF	NC	NC
N	NC	VCC	NC	NC	$\overline{CE}$0_1	ALE_1	$\overline{RE}$_1			$\overline{RE}$_3	DQ2_1	DQ2_3	NC	VSSQ	VCCQ	NC
P	NC	VSS	NC	NC	$\overline{CE}$0_3	ALE_3	RE_1			RE_3	DQ3_1	DQ3_3	NC	NC	NC	NC
R	NC	NC	NC	NC	$\overline{CE}$1_1	CLE_3	CLE_1			$\overline{DQS}$_1	$\overline{DQS}$_3	VSSQ	VCCQ	VSS	VCC	NC
T	NC	VCC	NC	NC	$\overline{CE}$1_3	$\overline{WP}$_3	$\overline{WP}$_1			DQS_1	DQS_3	VSS	VCC	VSSQ	VCCQ	NC
U	NC	VSS	NC	NC	NC	R/$\overline{B}$0_1	NC			DQ4_1	DQ4_3	VSSQ	VCCQ	NC	NC	NC
V	NC	NC	NC	NC	NC	R/$\overline{B}$0_3	NC			DQ5_1	DQ5_3	NC	NC	VSSQ	VCCQ	NC
W	NC	VCC	VSS	NC	NC	NC	VSSQ			DQ6_1	DQ6_3	NC	NC	VSS	VCC	NC
Y	NC	NC	VPP	NC	NC	NC	VCCQ			DQ7_1	DQ7_3	VSS	VCC	VSSQ	NC	NC
AA	NC	NC	NC	VCC	VSS	VCC	VSS	VCC	VREF	VSSQ	VCCQ	VSSQ	VCCQ	NC	NC	NC
AB	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC

316 ball fBGA (4-Ch, 8CE#)

Note:
1) Vpp Pin: Depends on the use of customer. If you can't supplied External Vpp, this pin is NU.

Figure 2-10. BGA-316 ball spacing requrements (top & view, dimensions in millimeters)

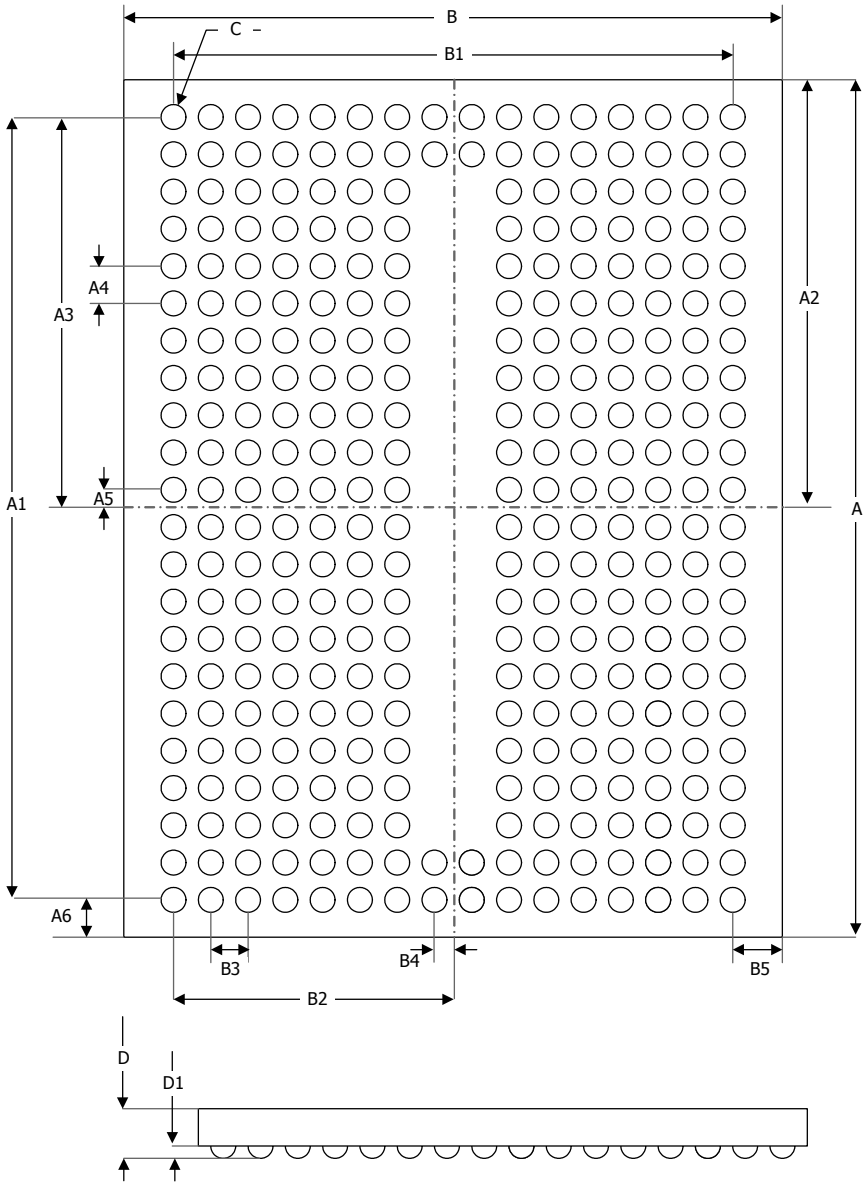


Figure 2-7 defines the ball spacing requirements for the 316-ball BGA package. The solder ball diameter is 0.55mm post reflow. The 316-ball BGA has one package size : 14mm x 18mm.

Table 2-3. BGA-316 ball 14mmx18mm, Package Mechanical Data

Symbol	Milimeters			Symbol	Milimeters		
	Min	Typ	Max		Min	Typ	Max
A	17.90	18.0	18.10	B	13.90	14.0	14.10
A1	-	16.8	-	B1	-	12.0	-
A2	-	9.0	-	B2	-	6.0	-
A3	-	8.4	-	B3	-	0.8	-
A4	-	0.8	-	B4	-	0.4	-
A5	-	0.4	-	B5	-	1.0	-
A6	-	0.6	-				
Symbol	**Milimeters**			**Symbol**	**Milimeters**		
	Min	**Typ**	**Max**		**Min**	**Typ**	**Max**
C	0.45	0.5	0.55	D[1)]	0.8	0.9	1.0
				D[2)]	1.15	1.25	1.35
				D1	0.27	0.32	0.37

Note 1) H27QFG8PQM2R-BCF
Note 2) H27Q1T8QQM3R-BCF, H27Q1T8QRM3R-BCF and H27Q2T8LQM3R-BCF

2.2. PIN DESCRIPTION

Pin Name	Description
DQ[7:0]	**DATA INPUTS/OUTPUTS** The DQ pins are used to input command, address and data, and to output data during read operations. The DQ pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the DQ ports on the rising edge of the $\overline{WE}$ signal.
ALE	**ADDRESS LATCH ENABLE** The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of $\overline{WE}$ with ALE high.
$\overline{CE}$	**CHIP ENABLE** The $\overline{CE}$ input is the device selection control. When the device is in the Busy state, $\overline{CE}$ high is ignored, and the device does not return to standby mode in program or erase operation.
$\overline{RE}$	**Read Enable (True)**. RE_t The $\overline{RE}$ input is the serial data-out control, and when active, drives the data onto the DQ bus. Data is valid after t_{DQSRE} of rising edge & falling edge of $\overline{RE}$, which also increments the internal column address counter by each one. $\overline{RE}$ is paired with differential signal RE(RE_c) to provide differential pair signaling to the system during reads.
RE	**Read Enable Complement**. RE_c The Read Enable Complement signal is the complementary signal to Read Enable.
$\overline{WE}$	**WRITE ENABLE** The WE input controls writes to the DQ port. Commands, addresses are latched on the rising edge of the $\overline{WE}$ pulse.

$\overline{WP}$	**WRITE PROTECT** The $\overline{WP}$ pin provides inadvertent program/erase protection during power transitions. The internal high voltage generator is reset when the $\overline{WP}$ pin is active low.
R/$\overline{B}$	**READY/BUSY OUTPUT** The R/$\overline{B}$ output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
DQS	**DATA STROBE.** DQS_t Data output is aligned with DQS falling/rising edge, and data inputs at DQS falling/rising.
$\overline{DQS}$	**Data Strobe Complement.** DQS_c The Data Strobe Complement signal is the complementary signal to Data Strobe.
Vcc	**POWER** VCC is the power supply for device.
VccQ	**DQ POWER** The VccQ is the power supply for input and/or output signals.
Vss	**GROUND**
VssQ	**DQ GROUND** The VssQ is the power supply ground
VREFQ [3)]	**REFERENCE VOLTAGE**
VPP [4)]	**EXTERNAL HIGH VOLTAGE**
NC	**NO CONNECTION** Lead is not internally connected.
NU	**NOT USE** Nothing should be connected with it.

NOTE :
1) Connect all Vcc and Vss pins of each device to common power supply outputs.
2) Do not leave all Vcc, VccQ, Vss and VssQ disconnected.
3) VREFQ : VREFQ shall be used when data inpupt/output speed is over 200Mbps.
4) VPP : Depends on the use of customer. If you can't supplied External Vpp, this pin is NU.

2.3. Absolute Maximum DC Ratings

Stresses greater than those listing in Table of "*Absolute maximum rating*" may cause permanent damage to the device. This is a stress rating only. Operation beyond the operating conditions specified in Table of "*Absolute maximum rating*" is not recommended. Extended exposure beyond these conditions may affect device reliability.

Table 2-4. Absolute maximum DC ratings

Parameter	Symbol	Symbol	Rating	Units
Voltage on any pin relative to VSS	VCC		-0.6 to +4.6	V
	VIN	VCCQ 3.3V	-0.6 to +4.6	
		VCCQ 1.8V	-0.2 to +2.4	
	VI/O	VCCQ 3.3V	-0.6 to +4.6	
		VCCQ 1.8V	-0.2 to +2.4	
	VPP		-0.6 to +16.0	

2.4. Operating temperature condition

Table 2-5. Operating Temperature Condition

Symbol	Parameter	Rating	Unit
TOPER	Operating Temperature Range for Commercial	0 to +70	degree

Note 1) Operating Temperature(TOPER) is the case surface temperature on the center/top side of the NAND.

2.5. Recommended Operating Conditions

Table 2-6. Recommended Operating Condition

			Normal Range			
Symbol	**Parameter**		**Min**	**Typ.**	**Max**	**Unit**
VCC	Power Supply Voltage		2.7	3.3	3.6	V
VSS	Ground Voltage		0	0	0	
VCCQ	Supply Voltage for Input/Output signaling	1.8V I/O	1.7	1.8	1.95	
VCCQ	Supply Voltage for Input/Output signaling	3.3V I/O	2.7	3.3	3.6	
VSSQ	Ground Voltage for Input/Output signaling		0	0	0	
VPP	External high Voltage		11	12	13	
VREFQ	Reference voltage		0.49 * VccQ	0.50 * VccQ	0.51 * VccQ	

Note
1) VCCQ and VCC can be distinct and unique voltages. The device supports one of the following VCCQ/VCC combinations:
(VCC = 3.3V, VCCQ = 3.3V) or (VCC = 3.3V, VCCQ = 1.8V)
2) If the transfer rate is greater than 100 MHz (200 MB/s), VCCQ = 3.3V is not supported.
VccQ 3.3V product: H27QDG882MLR-BCC and H27QEG89DNLR-BCC
3) The maximum external Vpp supply current per LUN is 5mA
4) All parameters, timing modes, and other characteristics are related to the supported voltage combination.

2.6. AC Overshoot/Undershoot Requirements

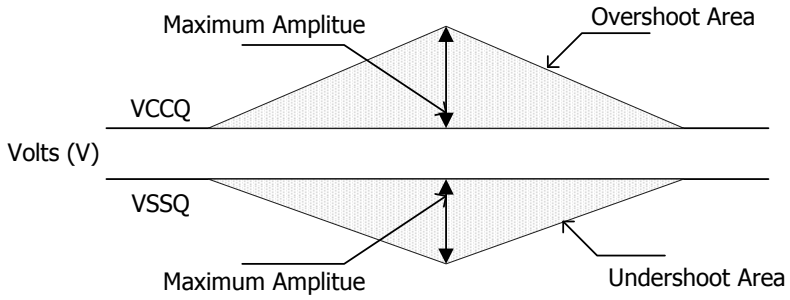
The device may have AC overshoot or undershoot from VccQ and VssQ levels. Table for *"AC Overshoot/Undershoot Specification"* defines the maximum values that the AC overshoot or undershoot may attain. These values apply for both 3.3V and 1.8V VCCQ operation.

Table 2-7. AC Overshoot/Undershoot Specification (Normal Vcc & Extended Vcc)

Parameter	Normal Range Product							Unit
	Maximum Value							
	~50	51~66	67~83	84~100	100~133	133~166	166~200	Mhz
Max. peak amplitude allowed for overshoot area	1	1	1	1	1	1	1	V
Max. peak amplitude allowed for undershoot area	1	1	1	1	1	1	1	
Max. overshoot area above VccQ	3	2.25	1.8	1.5	1.13	0.9	0.75	V *ns
Max. undershoot area above VssQ	3	2.25	1.8	1.5	1.13	0.9	0.75	

NOTE :
1) This specification is intended for devices with no clamp protection and is guaranteed by design.

Figure 2-11. Overshoot/Undershoot Diagram



2.7. DC and Operating Characteristics

Table 2-8. DC & Operating Characteristics for VccQ=3.3V (Single Die)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Array Read Current	ICC1	-	-	-	50	mA
Array Program Current	ICC2	-	-	-	50	mA
Array Erase Current	ICC3	-	-	-	50	mA
DQ Burst Read Current	ICC4R	$\overline{CE}$=VIL, Half data switching, tRC=10ns (100MHz)	-	-	80	mA
I/O burst write Current	ICC4W	$\overline{CE}$=VIL	-	-	80	mA
Bus idle Current	ICC5	-	-	-	20	mA
Standby current, CMOS	ISB	$\overline{CE}$=VCCQ-0.2, $\overline{WP}$=0V/VCCQ	-	-	50	uA
Input Leakage Current	ILI	VIN=0 to VCCQ	-	-	+/-10	uA
Output Leakage Current	ILO	VOUT=0 to VCCQ	-	-	+/-10	uA
Output High Voltage Level	VOH	IOH=-400uA	VccQ-0.1	-	-	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Output Low Voltage Level	VOL	IOL= 2.1mA	-	-	0.1	V
Output Low Current(R/$\overline{B}$)	IOL(R/$\overline{B}$)	VOL=0.4V	3	4	-	mA

NOTE :
1) Typical value is measured at Vcc=3.3V, TA=25°C. Not 100% tested.
2) ICC1, ICC2, and ICC3 as listed in this table are active current values.
3) During cache operations, increased ICC current is allowed while data is being transferred on the bus and an array operation is ongoing. For a cached read this value is ICC1 + ICC4R; for a cached write this value is ICC2(active) + ICC4W.
4) For ICC4R the test conditions specify in tRC(min) and CE# = VIL, IOUT = 0 mA. When outputs are not static, additional VccQ current will be drawn that's highly dependent on system configuration. IccQ calculated for each output pin assuming 50% data switching as (IccQ = 0.5 * CL * VccQ * frequency), where CL is the capacitive load.

Table 2-9. DC & Operating Characteristics for VccQ=1.8V (Single Die)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Page Read Operation Current	ICC1	-	-	-	50	mA
Page Program Operation Current	ICC2	-	-	-	50	mA
Erase Operation Current	ICC3	-	-	-	50	mA
DQ Burst Read Current	ICC4R	$\overline{CE}$=VIL, Half data switching	-	-	80	mA
	ICCQ4R	CLOAD=0pF (IOUT=0mA) $\overline{CE}$=VIL, tRC=5ns(200Mhz)	-	-	50	mA
I/O burst write current	ICC4W	$\overline{CE}$=VIL, Half data switching tDSC=5ns(200Mhz)	-	-	80	mA
	ICCQ4W		-	-	20	mA
Bus idle current	ICC5	-	-	-	20	mA
Standby current, CMOS	ISB	$\overline{CE}$=VCCQ-0.2, $\overline{WP}$=0V/VCCQ	-	-	50	uA
Input Leakage Current	ILI	VIN=0 to VCCQ(max)	-	-	+/-10	uA
Output Leakage Current	ILO	VOUT=0 to VCCQ(max)	-	-	+/-10	uA
Output High Voltage Level	VOH	IOH=-100uA	VCCQ-0.1	-	-	V
Output Low Voltage Level	VOL	IOL= 100uA	-	-	0.1	V
Output Low Current(R/$\overline{B}$)	IOL(R/$\overline{B}$)	VOL=0.2V	3	4	-	mA
Vpp Idle current (Optional)	IPPI 4)	-	-	-	TBD	uA
Vpp Activecurrent (Optional)	IPPA 4)	-	-	-	TBD	mA

NOTE :
1) Typical value is measured at Vcc=3.3V, TA=25°C. Not 100% tested.
2) VOH and VOL should be available on these two conditions; Output Strength is nominal and VccQ=1.8V, Rpd/Rpu are all VccQx0.5. If the driver strength settings are supported, Table of *"DQ Driver Strength Settings"* be used to derive the output driver impedence values.
3) For ICC4R the test conditions specify IOUT = 0 mA
4) IPP Idle current is IPP current measured when Vpp is supplied and Vpp is not enabled via Set Feature. IPP Active current is IPP current measured when Vpp is supplied and Vpp is enabled via Set Feature.

2.9. AC Test Condition

Table 2-10. Characteristics for VccQ=3.3V, without VREFQ AC & DC input level

Parameter	Symbol	Min	Typ	Max	Units
DC Input high voltage	VIH (DC)	VCCQ * 0.8	-	VCCQ + 0.3	V
AC Input high voltage	VIH (AC)	VCCQ * 0.8	-	-	V
DC Input low voltage	VIL (DC)	-0.3	-	VCCQ * 0.2	V
AC Input low voltage	VIL (AC)	-	-	VCCQ * 0.2	V

NOTE:
1) VIL can undershoot to -0.3V and VIH can overshoot to VCCQ +0.3V for durations of 20 ns or less.
2) VrefQ be used at high interface speed above 200Mbps

Table 2-11. Characteristics for VccQ=1.8V with VREFQ AC & DC input level

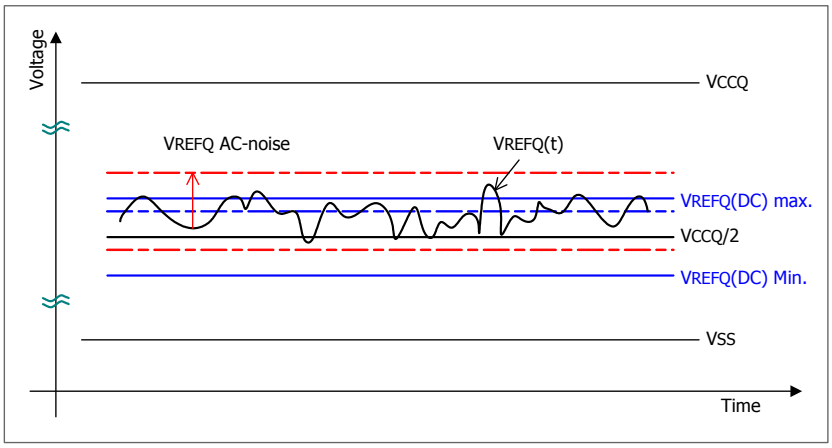
Parameter	Symbol	Min	Typ	Max	Units
DC Input high voltage	VIH (DC)	VREFQ + 0.15	-	VCCQ + 0.3	V
AC Input high voltage	VIH (AC)	VREFQ + 0.3	-	-	V
DC Input low voltage	VIL (DC)	-0.3	-	VREFQ - 0.15	V
AC Input low voltage	VIL (AC)	-	-	VREFQ - 0.3	V
Reference Voltage	VREFQ(DC)	VCCQ * 0.49		VCCQ * 0.51	V

NOTE:
1) VREFQ is used only for VCCQ 1.8V

2.10. VREFQ Tolerance

The DC-tolerance and AC-noise limits for the reference voltages. Figure for *"VREFQ(DC) tolerance and VREFQ AC-noise limits"* shows a valid reference voltage VREFQ(t) as a function of time.
VREFQ(DC) is the linear average of VREFQ(t) over a very long period of time (e.g. 1sec). This average has to meet the min/max requirements in Table of *"Characteristics for VccQ=1.8V with VREFQ AC & DC input level"*.
VREFQ(t) may temporarily deviate from VREFQ(DC) by no more than +/- 1% VCCQ
The voltage levels for setup and hold time measurements VIH(AC), VIH(DC), VIL(AC) and VIL(DC) are dependent on VREFQ.
"VREFQ" be understood as VREFQ(DC), as defined in Figure for *"VREFQ(DC) tolerance and VREFQ AC-noise limits"* .

Figure 2-12. VREFQ(DC) tolerance and VREFQ AC-noise limits



2.11. Differential Input/Output AC Characteristics (VCCQ=1.8V only)

Table 2-12. Differential AC Input Logic Level

Parameter	Symbol	Min	Max	Units
AC differential input voltage [1)]	VID (AC)	0.5	VCCQ + 0.6	V
AC differential cross point voltage [2)]	VIX(AC)	VCCQ * 0.5 - 0.175	VCCQ * 0.5 + 0.175	V
DC differential input voltage	VID (DC)	0.3	VCCQ + 0.3	V

NOTE:
1) VID(AC) specifies the input differential voltage |VTR -VCP | required for switching, where VTR is the "true" input signal and VCP is the "complementary" input signal. The minimum value is equal to VIH(AC) - VIL(AC).
2) The typical value of VIX(AC) is expected to be about 0.5 * VCCQ of the transmitting device and VIX(AC) is expected to track variations in VCCQ . VIX(AC) indicates the voltage at which differential input signals must cross.

Figure 2-13. Differential signal levels

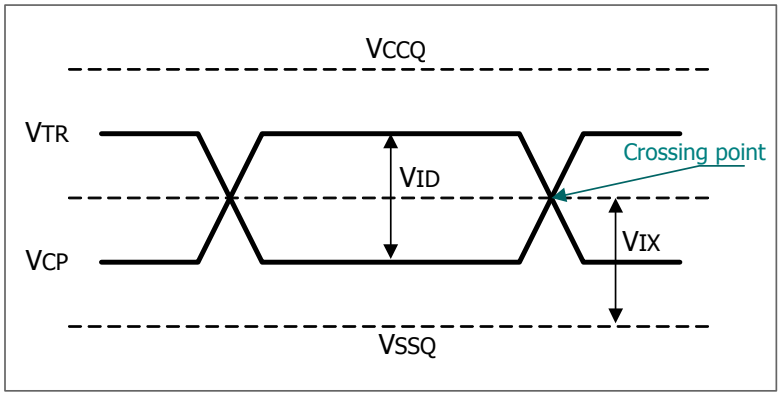


Table 2-13. Differential AC output Logic Level

Parameter	Symbol	Min	Max	Units
AC differential cross point voltage [1)]	VOX (AC)	VCCQ * 0.5 - 0.2	VCCQ * 0.5 + 0.2	V

NOTE:
1) The typical value of VOX(AC) is expected to be about 0.5 * VCCQ of the transmitting device and VOX(AC) is expected to track variations in VCCQ . VOX(AC) indicates the voltage at which differential output signals must cross.

2.12. Input/Output Capacitance(Ta=25°C, VCC=3.3V, f=100MHz)

Table 2-14. 132Ball fBGA Input/ Output capacitance (TA=25C, VCC=3.3V, f=100MHz)

Item	Symbol	Test Condition	Device		Min	Max	Unit
Input/Output Capacitance	CDQ	VIL=0V	H27QDG8M2M5R-BCF H27QDG882MLR-BCC	128Gb (16GB)	-	6.7	pF
			H27QEG8NDM5R-BCF H27QEG89DNLR-BCC	256Gb (32GB)	-		
			H27QFG8PEM5R-BCF	512Gb (64GB)	-	10.0	
			H27Q1T8QEM6R-BCF	1Tb (128GB)	-	16.9	
Input Capacitance	CIN	VIN=0V	H27QDG8M2M5R-BCF H27QDG882MLR-BCC	128Gb (16GB)	-	6.4	
			H27QEG8NDM5R-BCF H27QEG89DNLR-BCC	256Gb (32GB)	-		
			H27QFG8PEM5R-BCF	512Gb (64GB)	-	9.2	
			H27Q1T8QEM6R-BCF	1Tb (128GB)	-	14.3	

Note: Capacitance is periodically sampled and not 100% tested.

Table 2-15. 316Ball fBGA Input/ Output capacitance (TA=25C, VCC=3.3V, f=100MHz)

Item	Symbol	Test Condition	Device		Min	Max	Unit
Input/Output Capacitance	CDQ	VIL=0V	H27QFG8PQM2R-BCF	512Gb (64GB)	-	6.7	pF
			H27Q1T8QQM3R-BCF H27Q1T8QRM3R-BCF	1Tb (128GB)	-	10.0	
			H27Q2T8LQM3R-BCF	2Tb (256GB)	-	16.9	
Input Capacitance	CIN	VIN=0V	H27QFG8PQM2R-BCF	512Gb (64GB)	-	6.4	
			H27Q1T8QQM3R-BCF H27Q1T8QRM3R-BCF	1Tb (128GB)	-	9.2	
			H27Q2T8LQM3R-BCF	2Tb (256GB)	-	14.3	

Note: Capacitance is periodically sampled and not 100% tested.

2.13. DQ Driver Strength

The device may be configured with multiple driver strengths with 'SET FEATURE' command. There are Underdrive, Nominal options. The Toggle DDR supports all two driver strength settings. Devices that support driver strength settings comply with the output driver requirements in this section. A device is only required to meet driver strength values for either 3.3V VccQ or 1.8V VccQ, and is not required to meet driver strength values for both 3.3V VccQ and 1.8V VccQ.

Table 2-16. DQ Driver Strength Settings

Setting	Driver Strength	VccQ
Underdrive	0.7x = 50 Ohms	3.3V
Norminal	1.0x = 35 Ohms	
Overdrive 1	1.4x = 25 Ohms	
Overdrive 2	2.0x = 18 Ohms	
Underdrive	0.7x = 50 Ohms	1.8V
Norminal	1.0x = 35 Ohms	
Overdrive 1	1.4x = 25 Ohms	
Overdrive 2	2.0x = 18 Ohms	

The impedance values corresponding to several different VccQ values are defined in Table of *"Output Driver Strength Impedance Values"* for 3.3V and 1.8V VccQ. The test conditions that be used to verify the impedance values are specified in Table of "*Testing Conditions for Impedance Values*". The terms TOPER(Min) and TOPER(Max) are in reference to the minimum and maximum operating temperature defined for the device.

Table 2-17. Testing Conditions for Impedance Values (Normal Vcc Range)

Condition	Temperaturen	VCCQ(3.3V)	VCCQ(1.8V)	Process
Minimum Impedance	TOPER (Min) degrees Celsius	3.6V	1.95V	Fast - fast
Nominal Impedance	25 degrees Celsius	3.3V	1.8V	Typical
Maximum Impedance	TOPER (Max) degrees Celsius	2.7V	1.7V	Slow-slow

Table 2-18. Output Driver Strength Impedance Values

Output Strength	Rpd/ Rpu	VOUT to VssQ	Minimum		Nominal		Maximum		Units
			VCCQ 3.3V	VCCQ 1.8V	VCCQ 3.3V	VCCQ 1.8V	VCCQ 3.3V	VCCQ 1.8V	
Underdrive	Rpd	0.2 X VCCQ	18.4	24.0	45.0	40.0	80.0	72.0	
		0.5 X VCCQ	25.0	30.0	50.0	50.0	100.0	87.0	
		0.8 X VCCQ	32.0	38.0	57.0	67.0	136.0	122.0	
	Rpu	0.2 X VCCQ	32.0	38.0	57.0	67.0	136.0	122.0	
		0.5 X VCCQ	25.0	30.0	50.0	50.0	100.0	87.0	
		0.8 X VCCQ	18.4	24.0	45.0	40.0	80.0	72.0	
Norminal	Rpd	0.2 X VCCQ	12.8	16.0	32.0	26.7	58.0	47.5	ohm
		0.5 X VCCQ	18.0	21.0	35.0	35.0	70.0	61.0	
		0.8 X VCCQ	23.0	26.5	40.0	47.0	95.0	85.3	
	Rpu	0.2 X VCCQ	23.0	26.5	40.0	47.0	95.0	85.3	
		0.5 X VCCQ	18.0	21.0	35.0	35.0	70.0	61.0	
		0.8 X VCCQ	12.8	16.0	32.0	26.7	58.0	47.5	
Overdrive 1	Rpd	0.2 X VCCQ	9.3	11.4	22.3	19	40	35	
		0.5 X VCCQ	12.6	15	25	25	50	44	
		0.8 X VCCQ	16.3	18.2	29	34	68	61	
	Rpu	0.2 X VCCQ	16.3	18.2	29	34	68	61	
		0.5 X VCCQ	12.3	15	25	25	50	44	
		0.8 X VCCQ	9.3	11.4	19	19	40	35	
Overdrive 2	Rpd	0.2 X VCCQ	7	8.2	16.2	13.5	28.7	27	
		0.5 X VCCQ	9	10.8	18	18	36	31.5	
		0.8 X VCCQ	11.8	13.2	21	23.5	50	42.7	
	Rpu	0.2 X VCCQ	11.8	13.2	21	23.5	50	42.7	
		0.5 X VCCQ	9	10.8	18	18	36	31.5	
		0.8 X VCCQ	7	8.2	14	13.5	28.7	27	

Table 2-19. Pull-up and Pull-down Output Impedance Mismatch

Output Strength	VCCQ 3.3V		VCCQ 1.8V		Units
	Minimum	Maximum	Minimum	Maximum	
Underdrive	0	17.5	0	8.8	ohm
Norminal	0	12.3	0	6.2	
Overdrive 1	0	8.8	0	4.4	
Overdrive 2	0	6.3	0	3.2	

NOTE :
1) Mismatch is the absolute value between pull-up and pull-down impedances. Both are measured at the same temperature and voltage.
2) Test conditions: VccQ = VccQ(min), Vout = VccQ × 0.5, TA = TOPER

2.14. Input/Output Slew rate

The input slew rate requirements that the device comply with are defined in Table of *"Derating factor"* and Table of *"Input Slew rate"*. The output slew rate requirements that the device comply with are defined in Table of *"Output Slew Rate Requirements"* . The testing conditions that be used to verify the input slew rate are listed in Table for *"Testing Conditions for Input Slew Rate"* and *"Testing Conditions for Output Slew Rate"*.

Table 2-20.Derating factor

1) Differential signaling

Input Slew Rate	200Mbps				400Mbps				Units
	VREFQ not used		VREFQ used		VREFQ not used		VREFQ used		Units
	VCCQ 3.3V	VCCQ 1.8V	VCCQ 3.3V	VCCQ 1.8V	VCCQ 3.3V	VCCQ 1.8V	VCCQ 3.3V	VCCQ 1.8V	
1.0V/ns	0	0	0	0	-	-	-	0	ps
0.8V/ns	166	90	50	50	-	-	-	50	
0.6V/ns	442	241	134	134	-	-	-	134	

NOTE :
1) Derating factor listed in this table shall be applied to data setup time (tDS) and data hold time (tDH) as additional value if the slew rate is less than the minimum value defined in Table of *"Input Slew rate"*.

2) Single ended signaling

Output Strength	200Mbps				Units
	VREFQ not used		VREFQ used		Units
	VCCQ 3.3V	VCCQ 1.8V	VCCQ 3.3V	VCCQ 1.8V	
1.0V/ns	0	0	0	0	ps
0.8V/ns	332	180	100	100	
0.6V/ns	884	482	268	268	

NOTE :
1) Derating factor listed in this table shall be applied to data setup time (tDS) and data hold time (tDH) as additional value if the slew rate is less than the minimum value defined in Table of *"Input Slew rate"*.

Table 2-21.Input Slew rate

VCCQ	VIL	VIH	Normal Vcc Range	
			Min	
			200Mbps	400Mbps
3.3V	VCCQ * 0.2	VCCQ * 0.8	1.0V/ns	2.0V/ns
1.8V	VCCQ * 0.2	VCCQ * 0.8	1.0V/ns	1.0V/ns

Table 2-22. Testing Conditions for Input Slew Rate

Parameter	Value
Positive Input Transition	VIL (DC) to VIH (AC)
Negative Input Transition	VIH (DC) to VIL (AC)

Table 2-23. Output Slew Rate Requirements

Parameter	VCCQ 3.3V		VCCQ 1.8V		Units
	Minimum	Maximum	Minimum	Maximum	
Underdrive	1.0	5.5	0.60	4.0	V/ns
Norminal	1.2	7.0	0.75	4.0	
Overdrive 1	1.5	9.0	0.85	5.0	
Overdrive 2	1.5	10.0	1.0	5.5	

NOTE :
1) Measured with a test load of 5pF connected to VssQ.
2) The ratio of pull-up slew rate to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maxiumum difference between pull-up and pull-down drivers due to process variation.

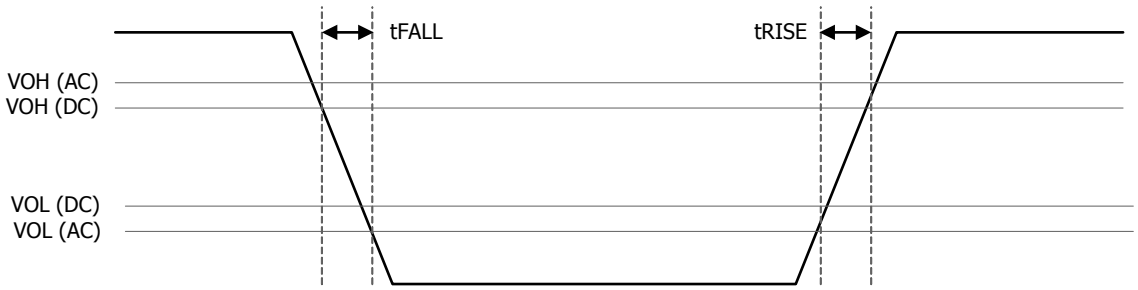
Table 2-24. Testing Conditions for Output Slew Rate

Parameter	Value
VOL (DC)	VCCQ * 0.3
VOH (DC)	VCCQ * 0.7
VOL (AC)	VCCQ * 0.2
VOH (AC)	VCCQ * 0.8
Positive Output Transition	VOL (DC) to VOH (AC)
Negative Output Transition	VOH (DC) to VOL (AC)
$tRISE^{(1)}$	Time during Rising Edge from VOL (DC) to VOH (AC)
$tFALL^{(1)}$	Time during Falling Edge from VOH (DC) to VOL (AC)

Parameter	Value
Output Slew Rate Rising Edge	(V_{OH} (AC) - V_{OL} (DC)) / tRISE
Output Slew Rate Falling Edge	(V_{OH} (DC) - V_{OL} (AC)) / tFALL
Output Capacitive load	C_L = 5pF

NOTE :
1) Refer to Figure of *"tRISE and tFALL Definition for Output Slew Rate"*.
2) Output slew rate is verified by design and characterization. It may not be subject to production test.
3) The minimum slew rate is the minimum of the rising edge and the falling edge slew rate. The maximum slew rate is the maximum of the rising edge and the falling edge slew rate.

Figure 2-14. tRISE and tFALL Definition for Output Slew Rate



tRISE and tFALL Definition for Output Slew Rate

2.15. AC and DC Input Measurement Levels

Table 2-25. AC Test condition

Parameter	H27xxG8xxMxR
Input Pulse Levels	V_{IL} to V_{IH}
Input Rise and Fall Times	1.0V/ns
Input and Output Timing Levels	V_{CCQ}/2
Output Load	C_L= 5pF

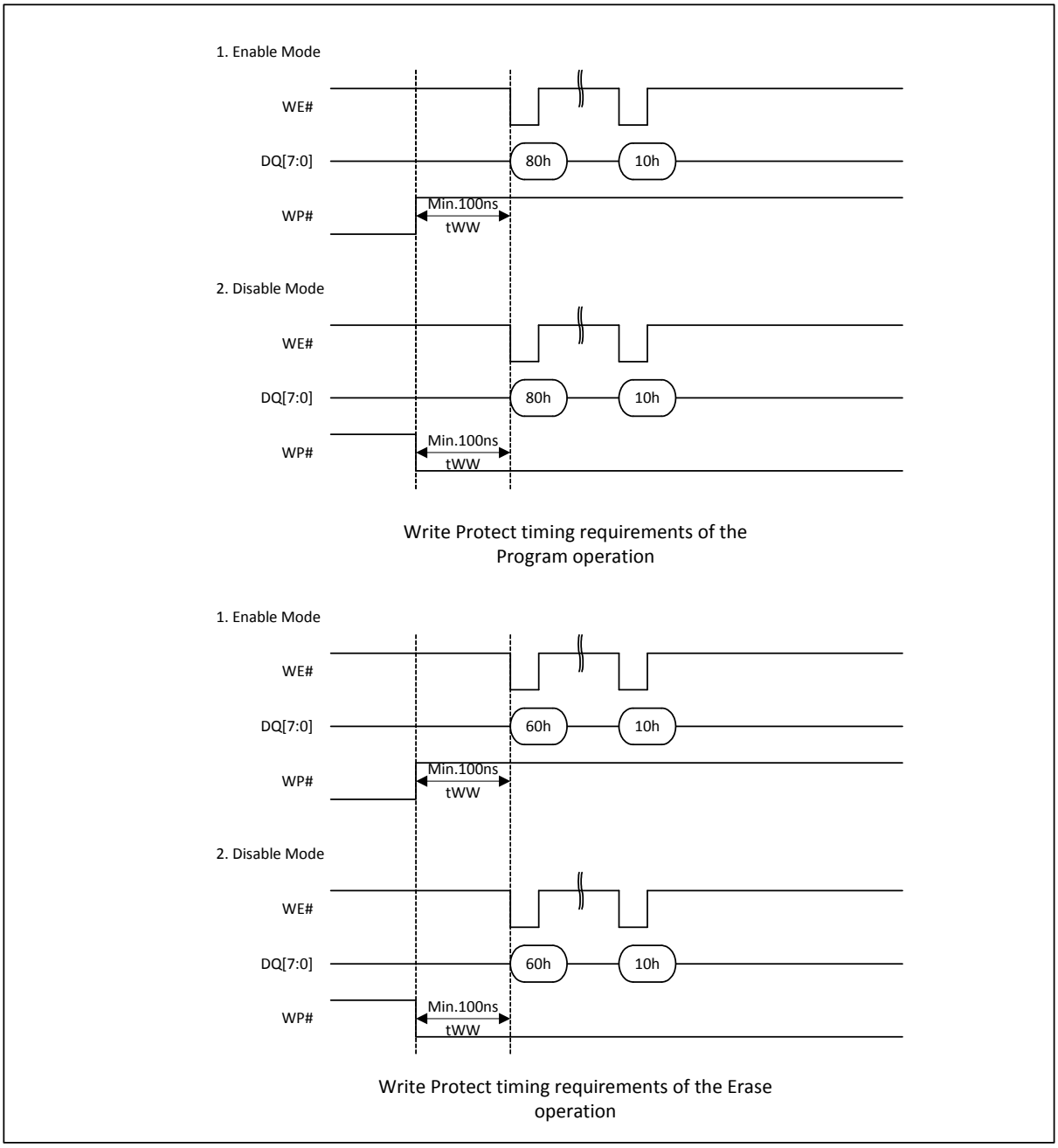
2.16. R/$\overline{B}$ and SR[6] Rlationship

R/$\overline{B}$ represents the status of the selected target. R/$\overline{B}$ goes busy when only a single LUN is busy while rests of LUNs on the same target are idle.

2.17. Write Protect

When $\overline{WP}$ is enabled, Flash array is blocked from any program and erase operations. This signal shall only be transitioned when a target is idle. The host shall be allowed to issue a new command after tWW once $\overline{WP}$ is enabled. Figure *"Write protect timing"* describes the tWW timing requirement, shown with the start of a Program and Erase command.

Figure 2-15. Write protect timing



3. Memory Organization

A device contains one or more targets. A target is controlled by one CE# signal. A target is organized into one or more logical units (LUNs).

A logical unit (LUN) is the minimum unit that can independently execute commands and report status.

A block is the smallest erasable unit of data within the Flash array of a LUN. There is no restriction on the number of blocks within the LUN. A block contains a number of pages.

A page is the smallest addressable unit for read and program operations. A page consists of a number of bytes.

Each LUN shall have at least one page register. A page register is used for the temporary storage of data before it is moved to a page within the Flash array or after it is moved from a page within the Flash array.

The byte location within the page register is referred to as the column.

There are two mechanisms to achieve parallelism within this architecture. There may be multiple commands outstanding to different LUNs at the same time. To get further parallelism within a LUN, plane addressing may be used to execute additional dependent operations in parallel.

Figure 3-1. Target Memory Organization

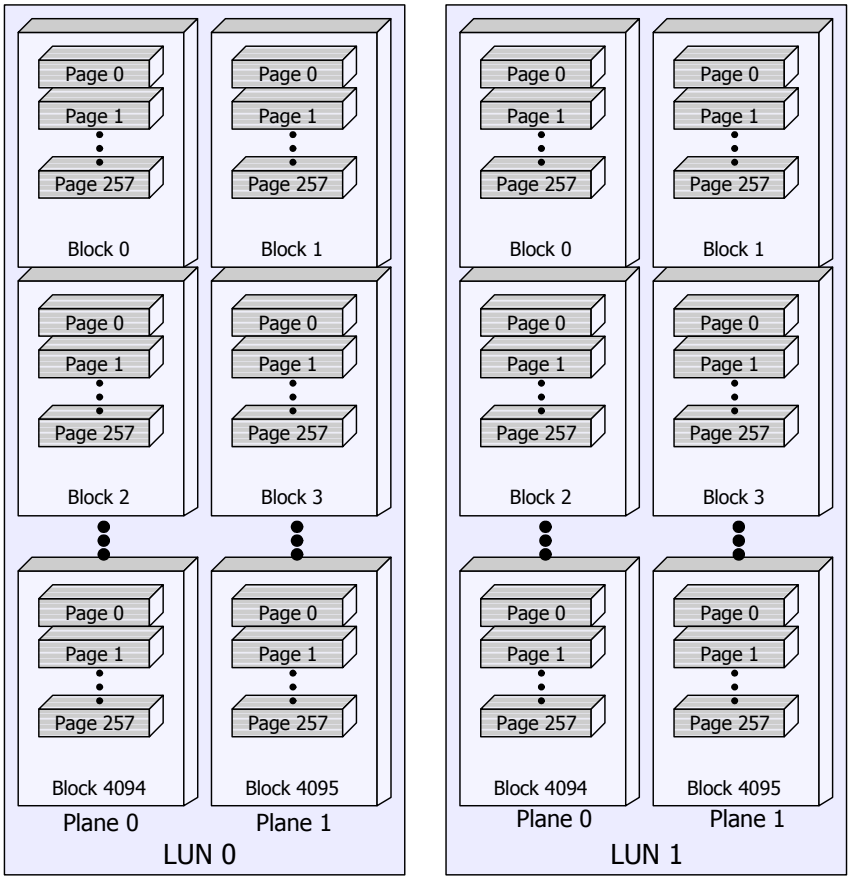
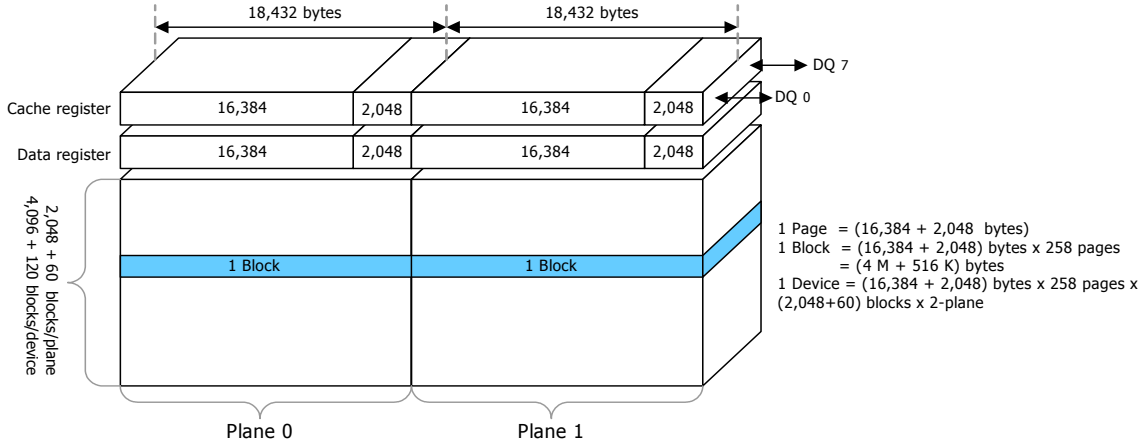


Figure 3-2. Memory organization for 128Gb TLC Logical Unit



3.1. Addressing

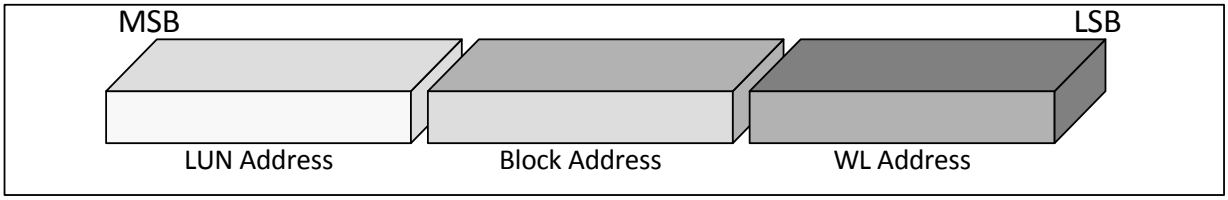
There are two address types used: the column address and the row address. The column address is used to access bytes within a page, i.e. the column address is the byte offset into the page. The least significant bit of the column address shall always be zero for a DDR interface, i.e. an even number of bytes is always transferred. The row address is used to address pages, blocks, and LUNs.

When both the column and row addresses are required to be issued, the column address is always issued first in one or more 8-bit address cycles. The row addresses follow in one or more 8-bit address cycles. There are some functions that may require only row addresses, such as Block Erase. In this case the column addresses shall not be issued.

For both column and row addresses the first address cycle always contains the least significant address bits and the last address cycle always contains the most significant address bits. If there are bits in the most significant cycles of the column and row addresses that are not used then they are required to be cleared to zero.

The row address structure is shown in Figure of *"Row Affress Layout"* with the least significant row address bit to the right and the most significant row address bit to the left.

Figure 3-2. Row Address Layout

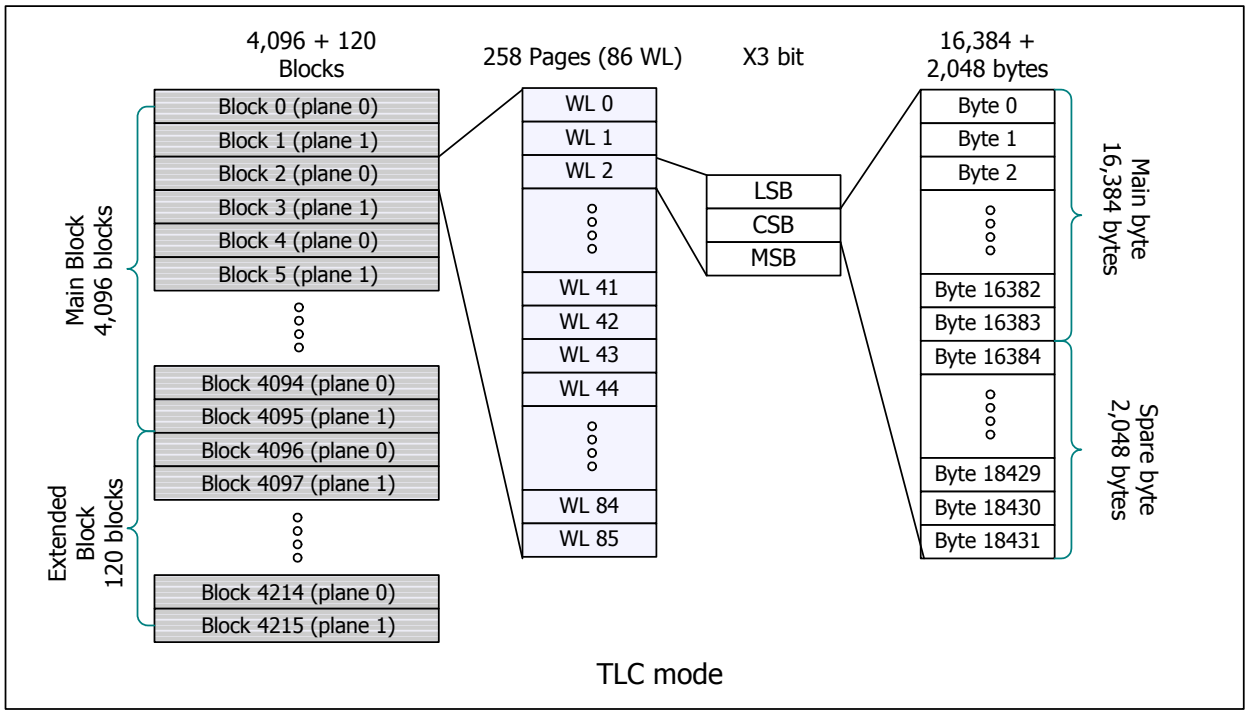


The WL address is set by the least significant row address bits, and the LUN address is set by the most significant row address bit(s). The block address is between a WL address and a LUN address.

A host shall not access an address of a page or block beyond maximum WL address or block address. The Addressing of this device is shown in Table of "*Memory addressing*".

3.1.1. TLC and SLC Address

Figure 3-3. Address Assignment



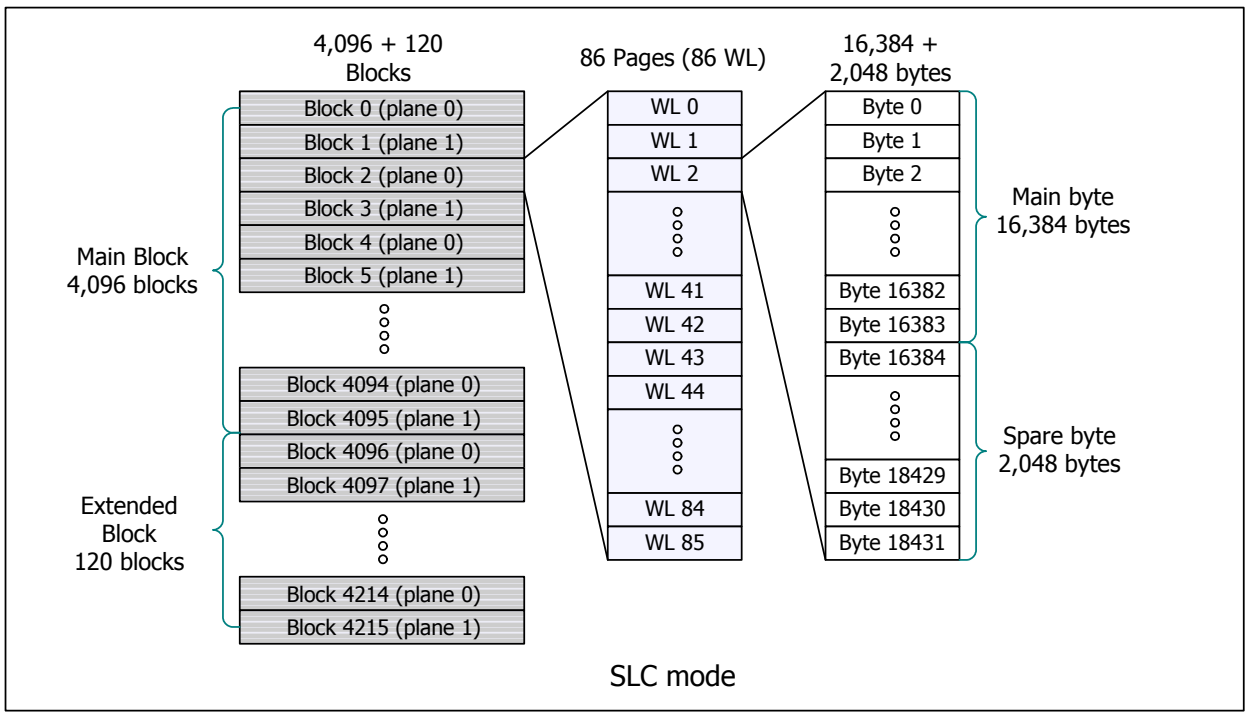


Table 3-1. TLC addressing

Bus Cycle	DQ0	DQ1	DQ2	DQ3	DQ4	DQ5	DQ6	DQ7
1st Cycle (Column address 1)	C0-0	C0-1	C0-2	C0-3	C0-4	C0-5	C0-6	C0-7
2nd Cycle (Column address 2)	C1-0	C1-1	C1-2	C1-3	C1-4	C1-5	C1-6	L(1)
3rd Cycle (Row address 1)	R0-0	R0-1	R0-2	R0-3	R0-4	R0-5	R0-6	L(1)
4th Cycle (Row address 2)	R1-0	R1-1	R1-2	R1-3	R1-4	R1-5	R1-6	R1-7
5th Cycle (Row address 3)	R2-0	R2-1	R2-2	R2-3	R2-4	R2-5	R2-6	R2-7

Note:
1) C0-0 to C1-6: Column Address – 16KB (Main) + 2KB (Spare)
2) R0-0 to R0-6: WL Address (LSB, CSB, and MSB Page Addresses are differentiated with 01h, 02h, and 03h commands) / For SLC Mode, WL Address is equal to Page Address
3) R1-0: Plane Address
4) R1-1 to R2-4: Block Address – 4096(Main) + 120(Extended)
5) R2-5 to R2-7: LUN Address
6) The least significant bit of block address is also regarded as Plane Address bit.
7) If the target of the device has only one LUN, no LUN Address bits are assigned.

3.1.2. TLC and SLC Addressing For Program Operation

The 128Gb TLC series are programmed on a page basis, and each page be programmed only once before being erased. The addressing order be sequential within a block. The contents of the page register are programmed into the Flash array specified by row address. SR[0] is valid for this command after SR[6] transitions from zero to one until the next transition of SR[6] to zero. "*Page Program Operation*" define the Page Program behavior and timings. Writing beyond the end of the page register is undefined. In case of SLC Mode, Page Program requires the A2h command.

The following program order is required for programming the pages witnin one block. Random page program is not allowed. LSB, CSB, and MSB be inputted and programmed three times in the page. Data from the three pages in one WL can be read out only after the 3rd program cycle. The data in the last WL can be read out after the third program cycle is done.
Below table shows the programming order.

Table 3-2. Program ordering Information (TLC)

WL	Page Number (1/2)			Program Order (1/2)			WL	Page Number (2/2)			Program Order (2/2)		
	LSB	CSB	MSB	1st PGM	2nd PGM	3rd PGM		LSB	CSB	MSB	1st PGM	2nd PGM	3rd PGM
WL 0	0	1	2	0	2	5	WL 43	129	130	131	126	130	134
WL 1	3	4	5	1	4	8	WL 44	132	133	134	129	133	137
WL 2	6	7	8	3	7	11	WL 45	135	136	137	132	136	140
WL 3	9	10	11	6	10	14	WL 46	138	139	140	135	139	143
WL 4	12	13	14	9	13	17	WL 47	141	142	143	138	142	146
WL 5	15	16	17	12	16	20	WL 48	144	145	146	141	145	149
WL 6	18	19	20	15	19	23	WL 49	147	148	149	144	148	152
WL 7	21	22	23	18	22	26	WL 50	150	151	152	147	151	155
WL 8	24	25	26	21	25	29	WL 51	153	154	155	150	154	158

WL	Page Number (1/2)			Program Order (1/2)			WL	Page Number (2/2)			Program Order (2/2)		
	LSB	CSB	MSB	1st PGM	2nd PGM	3rd PGM		LSB	CSB	MSB	1st PGM	2nd PGM	3rd PGM
WL 9	27	28	29	24	28	32	WL 52	156	157	158	153	157	161
WL 10	30	31	32	27	31	35	WL 53	159	160	161	156	160	164
WL 11	33	34	35	30	34	38	WL 54	162	163	164	159	163	167
WL 12	36	37	38	33	37	41	WL 55	165	166	167	162	166	170
WL 13	39	40	41	36	40	44	WL 56	168	169	170	165	169	173
WL 14	42	43	44	39	43	47	WL 57	171	172	173	168	172	176
WL 15	45	46	47	42	46	50	WL 58	174	175	176	171	175	179
WL 16	48	49	50	45	49	53	WL 59	177	178	179	174	178	182
WL 17	51	52	53	48	52	56	WL 60	180	181	182	177	181	185
WL 18	54	55	56	51	55	59	WL 61	183	184	185	180	184	188
WL 19	57	58	59	54	58	62	WL 62	186	187	188	183	187	191
WL 20	60	61	62	57	61	65	WL 63	189	190	191	186	190	194
WL 21	63	64	65	60	64	68	WL 64	192	193	194	189	193	197
WL 22	66	67	68	63	67	71	WL 65	195	196	197	192	196	200
WL 23	69	70	71	66	70	74	WL 66	198	199	200	195	199	203
WL 24	72	73	74	69	73	77	WL 67	201	202	203	198	202	206
WL 25	75	76	77	72	76	80	WL 68	204	205	206	201	205	209
WL 26	78	79	80	75	79	83	WL 69	207	208	209	204	208	212
WL 27	81	82	83	78	82	86	WL 70	210	211	212	207	211	215
WL 28	84	85	86	81	85	89	WL 71	213	214	215	210	214	218
WL 29	87	88	89	84	88	92	WL 72	216	217	218	213	217	221
WL 30	90	91	92	87	91	95	WL 73	219	220	221	216	220	224
WL 31	93	94	95	90	94	98	WL 74	222	223	224	219	223	227
WL 32	96	97	98	93	97	101	WL 75	225	226	227	222	226	230
WL 33	99	100	101	96	100	104	WL 76	228	229	230	225	229	233
WL 34	102	103	104	99	103	107	WL 77	231	232	233	228	232	236
WL 35	105	106	107	102	106	110	WL 78	234	235	236	231	235	239
WL 36	108	109	110	105	109	113	WL 79	237	238	239	234	238	242
WL 37	111	112	113	108	112	116	WL 80	240	241	242	237	241	245
WL 38	114	115	116	111	115	229	WL 81	243	244	245	240	244	248
WL 39	117	118	119	114	118	122	WL 82	246	247	248	243	247	251
WL 40	120	121	122	117	121	125	WL 83	249	250	251	246	250	254
WL 41	123	124	125	120	124	128	WL 84	252	253	254	249	253	256
WL 42	126	127	128	123	127	131	WL 85	255	256	257	252	255	257

Table 3-3. Program ordering Information (SLC)

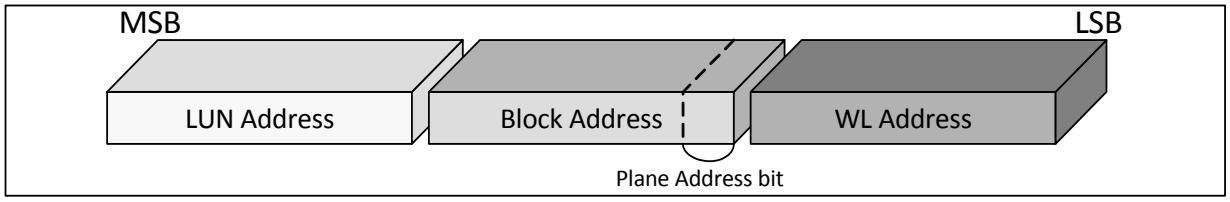
WL	Page Number (1/2)	Program Order (1/2)	WL	Page Number (2/2)	Program Order (1/2)	WL	Page Number (2/2)	Program Order (1/2)
WL 0	0	0	WL 29	29	29	WL 58	58	58
WL 1	1	1	WL 30	30	30	WL 59	59	59
WL 2	2	2	WL 31	31	31	WL 60	60	60
WL 3	3	3	WL 32	32	32	WL 61	61	61
WL 4	4	4	WL 33	33	33	WL 62	62	62
WL 5	5	5	WL 34	34	34	WL 63	63	63
WL 6	6	6	WL 35	35	35	WL 64	64	64
WL 7	7	7	WL 36	36	36	WL 65	65	65
WL 8	8	8	WL 37	37	37	WL 66	66	66
WL 9	9	9	WL 38	38	38	WL 67	67	67
WL 10	10	10	WL 39	39	39	WL 68	68	68
WL 11	11	11	WL 40	40	40	WL 69	69	69
WL 12	12	12	WL 41	41	41	WL 70	70	70
WL 13	13	13	WL 42	42	42	WL 71	71	71
WL 14	14	14	WL 43	43	43	WL 72	72	72
WL 15	15	15	WL 44	44	44	WL 73	73	73
WL 16	16	16	WL 45	45	45	WL 74	74	74
WL 17	17	17	WL 46	46	46	WL 75	75	75
WL 18	18	18	WL 47	47	47	WL 76	76	76
WL 19	19	19	WL 48	48	48	WL 77	77	77
WL 20	20	20	WL 49	49	49	WL 78	78	78
WL 21	21	21	WL 50	50	50	WL 79	79	79
WL 22	22	22	WL 51	51	51	WL 80	80	80
WL 23	23	23	WL 52	52	52	WL 81	81	81
WL 24	24	24	WL 53	53	53	WL 82	82	82
WL 25	25	25	WL 54	54	54	WL 83	83	83
WL 26	26	26	WL 55	55	55	WL 84	84	84
WL 27	27	27	WL 56	56	56	WL 85	85	85
WL 28	28	28	WL 57	57	57			

3.1.3. Plane Addressing

The plane address comprises the lowest order bits of the block address as shown in Figure for "*Position of Plane Address*". The plane address is used when performing a Two-plane command sequence on a particular LUN:

The plane address bit(s) shall be different within address setting sequences for the Two-plane-related operation, while the WL address shall stay the same within address setting sequences for the multi-plane-related operation.

Figure 3-3. Position of Plane Address



3.1.4. Extended Blocks Arrangement

The device offer 120 extended blocks to increase valid blocks.

Table 3-4. Extended blocks Arrangement

Row Address	Block Number	DQ2
000000h ~ 000055h	Block 0 (Plane 0)	Main Block (4096 Blocks)
000056h ~ 0000FFh	Block Gap	
000100h ~ 000155h	Block 1 (Plane 1)	
000156h ~ 0001FFh	Block Gap	
000200h ~ 000255h	Block2 (Plane 0)	
000256h ~ 0002FFh	Block Gap	
000300h ~ 000355h	Block 3 (Plane 1)	
000356h ~ 0003FFh	Block Gap	
-	-	
-	-	
-	-	
-	-	
0FFE00h ~ 0FFE55h	Block 4094 (Plane 0)	
0FFE56h ~ 0FFEFFh	Block Gap	
0FFF00h ~ 0FFF55h	Block 4095 (Plane 1)	
0FFF56h ~ 0FFFFFh	Block Gap	

Row Address	Block Number	DQ2
100000h ~ 100055h	Block 4096	Extended Block (120 Blocks)
100056h ~ 1000FFh	Block Gap	
100100h ~ 100155h	Block 4097	
100156h ~ 1001FFh	Block Gap	
-	-	
-	-	
107700h ~ 107755h	Block 4215	
107756h ~ 1077FFh	Block Gap	

3.1.5. Valid Blocks

Table 3-5. The number of valid block

Prodduct	Density	Symbol	Min	Typ.	Max	Unit
128Gb (16GB) Single Die	128Gbit	NVB	4012	4096	4216	Blocks

Notes:
1. The 1st block is guaranteed to be a valid block at the time of shipment.
2. This single device has a maximum of 4216 valid blocks.
3. Invalid blocks are one that contains one or more bad bits. The device may contain bad blocks on shipment.

4. FUNCTION DESCRIPTION

4.1. Data Interface / Timing Mode Transitions

4.1.1. The following transitions between data interface are supported:

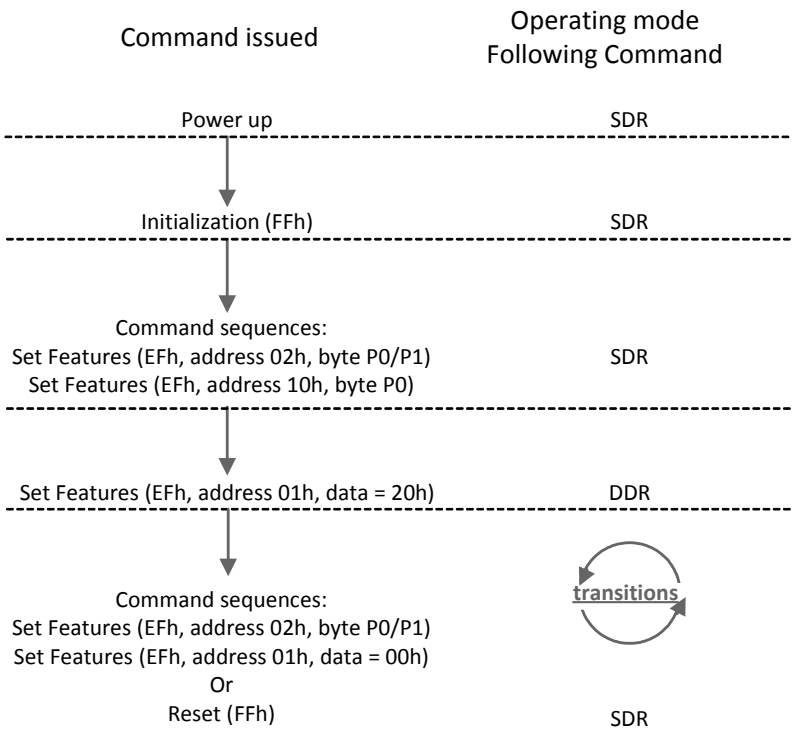
Device power-up is in SDR Mode. After the power supply is stable and VCC and VCCQ are within their normal operating range (2.7~3.3V/1.8V), a Reset command (FFh) must be issued to initialize the device.

- SDR to DDR
- DDR to SDR

To change the data interface to DDR, the Set Features command is used. The Set Features command (EFh), Feature Address, and the four parameters are entered using the previously selected data interface. When issuing the Set Features command, the host shall drive the DQS signal high (if supported) during the entirety of the command (including parameter entry). After the fourth parameter is entered until the tFEAT time has passed the host shall not issue any commands to the device.
Prior to issuing any new commands to the device, the host shall transition $\overline{CE}$ high. The new data interface is active when the host pulls $\overline{CE}$ low.

For Toggle Mode (with differential clock signals DQS and/or $\overline{RE}$ and/or VREF), bytes P0 and P1 must first be loaded at Set Features register address 02h using the Set Features command and the desired values (see "*Table 5-4. Toggle 2.0 specific setting assignment*," and "*Table 5-5. Definition of Toggle 2.0 specific setting*"). If the Set Features register address 02h is not loaded, it defaults to 00h, and the device operates as SDR mode.

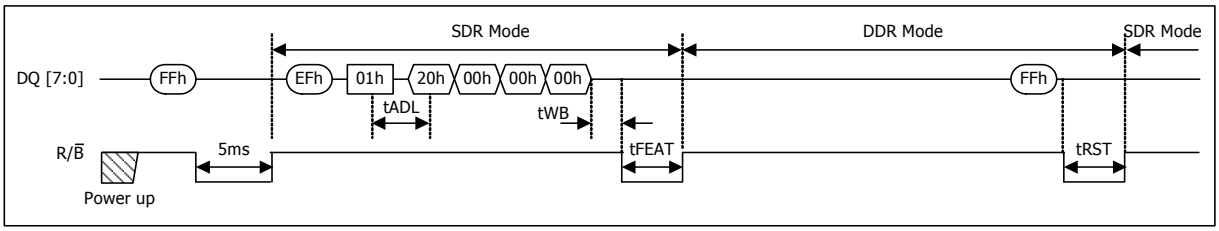
Figure 4-1. SDR to DDR, DDR to SDR Mode after Power up



4.1.2. SDR Transition from DDR

To transition from DDR to the SDR data interface, the host shall use the Reset (FFh) command or Set Feature sequence. After the Reset is issued, the host shall not issue any commands to the device until after the tFEAT time has passed. Note that after the tFEAT time has passed, only status commands may be issued by the host until the Reset completes.
After $\overline{CE}$ has been pulled high and then transitioned low again, the host should issue a Set Features to select the appropriate SDR timing mode.

Figure 4-2. SDR to DDR, DDR to SDR Mode Transition Diagram



4.1.3. VCCQ Setting Method

The NAND default interface mode is set to 3.3V, SDR mode after power up. Refer to the next table below when the Set paramer setting is avaliable in VccQ. As for "*Set parameter*" is given on Addendum 1.1.

Table 4-3. VCCQ setting and Read ID

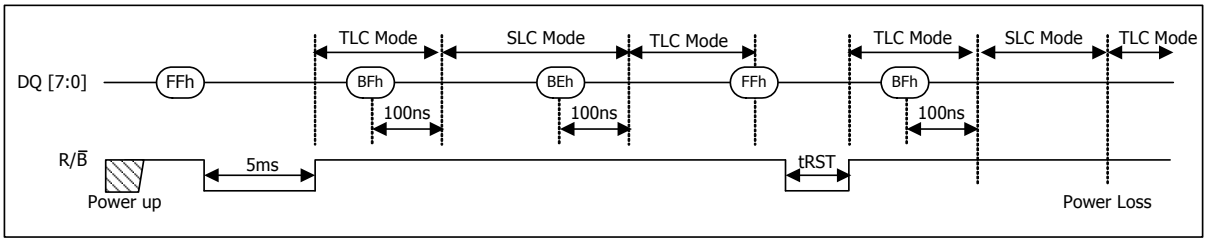
Command Cycle	Address	Data	VccQ	Read ID
36h	70h	01h	1.8V	ADh, 5Ah, 18h, A3h, 61h, 65h
		00h	3.3V	ADh, 3Ah, 18h, A3h, 61h, 25h

4.1.4. TLC to SLC mode transition (TLC2SLC)

TLC NAND flash supports two different cell types: TLC and SLC. It is provided with an additional feature which allows for a host to access one or more blocks in SLC mode. Program, read, and erase operation in SLC mode are much faster than standard TLC operations, and also the reliability is higher than normal TLC blocks.
The NAND supports two different cell types, TLC and SLC. The overhead to execute a SLC operation is small, just one command cycle to activate/deactivate SLC session. At power on, the device starts in TLC mode, and could be switched in SLC mode to providing TLC2SLC command (BFh). If a power loss occurs during SLC operation mode, the device will switch in TLC operation mode automatically. Either SLC2TLC command (BEh) or RESET (FFh) command could be used for to switch device in TLC operation mode. Erase/Program/Read within block boundary should be done in same mode. For example, read operation in SLC mode isn't allowed in the block programmed in TLC mode.

A block assigned to operate in on mode (TLC or SLC mode) should always stay to operate in the same mode during the life of the device. One command cycle is required to enter SLC session without busy state. After power-up, the device begins in TLC mode, and then TLC mode is switched to SLC mode with BFh command. Either BEh command or FFh command (reset) can be used to exit from TLC mode.

Figure 4-4. SLC/TLC Mode Transition Diagram



4.2. Discovery and Initialization

Toggle DDR NAND is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below about 2V.
The Reset command(FFh) must be issued to all CE#s as the first command after the NAND Flash device is powered on. Each $\overline{CE}$ will be busy for 5ms at the maximum after the Reset command is issued. During busy time of resetting, the acceptable command is the Read Status(70h).

$\overline{WP}$ pin provides hardware protection and is recommended to be kept at VIL during power-up and power-down. The two step command sequence for program/erase provides additional software protection. "*Figure 4-4. Initialization Timing*" defines the Initialization behavior and timings.

4.2.1. Single Channel Discovery

Host shall set to 'Low' the $\overline{CE}$ which is to enable the target if connected, while all other $\overline{CE}$ are set to 'High'. Host shall then issue the Reset command(FFh) to the target. Following the reset, the host should then issue the Read ID command to the target.
If the Host read out 6 cycles data by the Read ID command with address 00h, then the corresponding target is connected.
If the ID values are not returned or any error/timeout is encountered within the sequence, then the corresponding target may not be connected properly and no further use of the target shall be done.

4.2.2. Dual Channel Discovery

If there are dual channel in a package, host should issues the Reset command(FFh) to both channels to initialize all LUNs. Note that the relationships are described between several CE# and dual channels. See the Table of *"Data Bus to $\overline{CE}$ mapping"* for further information.

Table 4-1. Data Bus to $\overline{CE}$ mapping

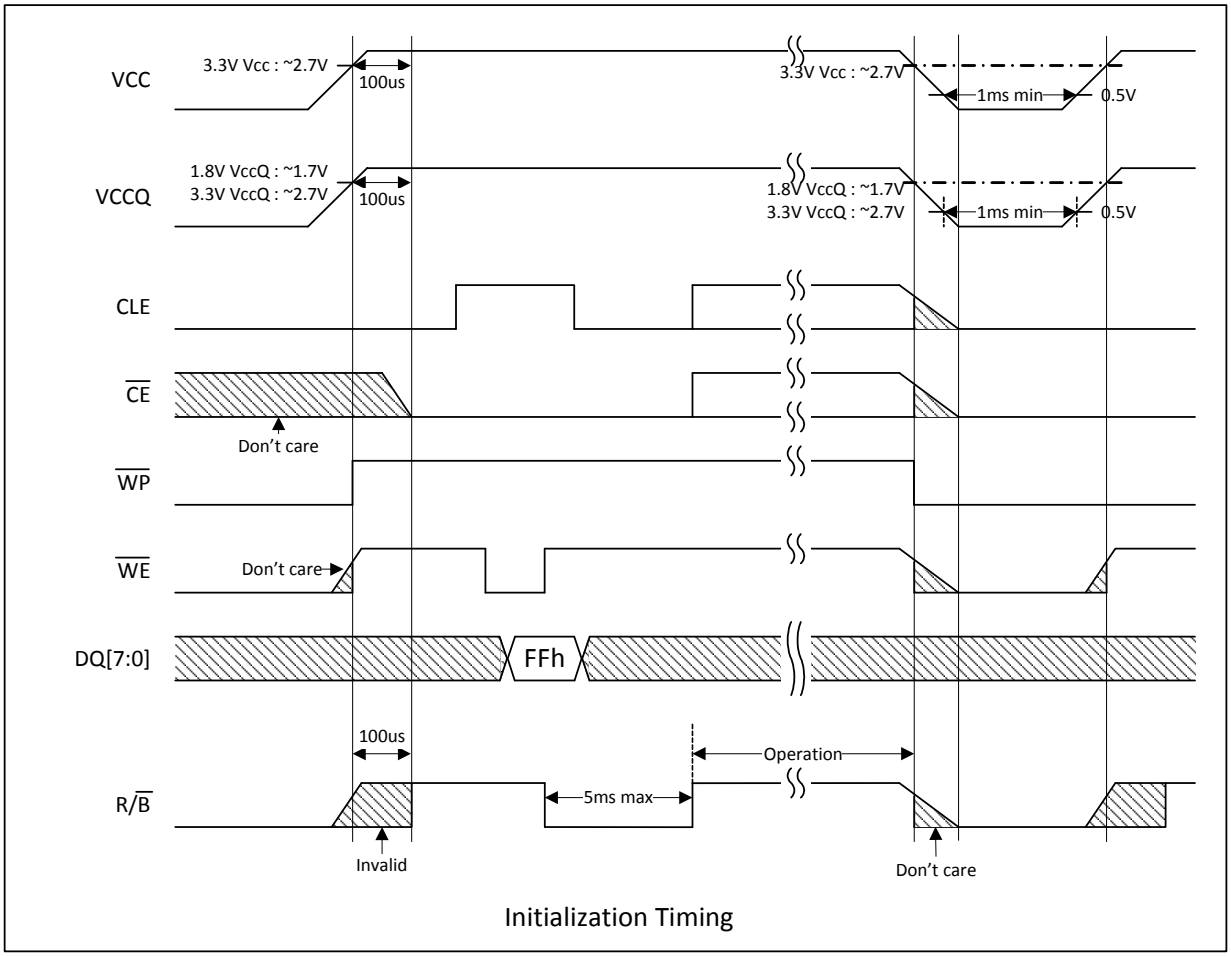
Signal Name	$\overline{CE}$
R/$\overline{B}$0	$\overline{CE}$0, $\overline{CE}$4
R/$\overline{B}$1	$\overline{CE}$1, $\overline{CE}$5
R/$\overline{B}$2	$\overline{CE}$2, $\overline{CE}$6
R/$\overline{B}$3	$\overline{CE}$3, $\overline{CE}$7
$\overline{RE}$0	$\overline{CE}$0, $\overline{CE}$2, $\overline{CE}$4, $\overline{CE}$6
$\overline{RE}$1	$\overline{CE}$1, $\overline{CE}$3, $\overline{CE}$5, $\overline{CE}$7
CLE0	$\overline{CE}$0, $\overline{CE}$2, $\overline{CE}$4, $\overline{CE}$6
CLE1	$\overline{CE}$1, $\overline{CE}$3, $\overline{CE}$5, $\overline{CE}$7
ALE0	$\overline{CE}$0, $\overline{CE}$2, $\overline{CE}$4, $\overline{CE}$6
ALE1	$\overline{CE}$1, $\overline{CE}$3, $\overline{CE}$5, $\overline{CE}$7
$\overline{WE}$0	$\overline{CE}$0, $\overline{CE}$2, $\overline{CE}$4, $\overline{CE}$6
$\overline{WE}$1	$\overline{CE}$1, $\overline{CE}$3, $\overline{CE}$5, $\overline{CE}$7
$\overline{WP}$0	$\overline{CE}$0, $\overline{CE}$2, $\overline{CE}$4, $\overline{CE}$6
$\overline{WP}$1	$\overline{CE}$1, $\overline{CE}$3, $\overline{CE}$5, $\overline{CE}$7
DQS0	$\overline{CE}$0, $\overline{CE}$2, $\overline{CE}$4, $\overline{CE}$6
DQS1	$\overline{CE}$1, $\overline{CE}$3, $\overline{CE}$5, $\overline{CE}$7

The sequence of initialization is the same as the sequence for single channel discovery. Host shall set to 'Low' the $\overline{CE}$ which is to enable the target if connected, while all other $\overline{CE}$ are set to 'High'. Host shall then issue the Reset command(FFh) to the target. Following the reset, the host should then issue a Read ID command to the target. If the Host read out 6 cycles data by the Read ID command with address 00h, then the corresponding target is connected. If the ID data is not returned or any error/timeout is encountered within the sequence, then the corresponding target may not be connected properly and no further use of the target shall be done. and no further use of the target shall be done.

4.2.3. Initialization

For NAND devices that support VCCQ for Data Input/Output power supply, VCCQ must not exceed VCC during power up. The host must wait for R/$\overline{B}$ to be valid High before issuing Reset command (FFh) to initialize any targets that share same $\overline{CE}$. The R/$\overline{B}$ signal becomes valid after 100us since both VCC and VCCQ reach 2.7V (1.7V for 1.8V VCCQ). The RESET command (FFh) must be issued to all targets as the first command after the NAND device is powered up and R/B_n becomes valid.

Figure 4-5. Initialization Timing



Initialization Timing

NOTE :
1) During the initialization, the device consumes a maximum current of ICC1.
2) Vcc should be reached the valid voltage no later than VccQ.
3) Once Vcc drops under 2.5V, Vcc is recommended that it be driven down to 0.5V and stay low under 0.5V for at least 1ms before Vcc powered up. Floating Vcc/VccQ during power-down is prohibited.

4.3. Mode Selection

Table of "*Mode Selection*" describes the bus state for the Toggle DDR. Commands, addresses and data is all written through DQ's by bringing WE to low while CE is low. Those are latched on the rising edge of WE. Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the DQ pins.

Host reads or writes data to the device using DQS signal. And data is latched on the falling and rising both edge of DQS on data input.

Table 4-2. Mode Selection

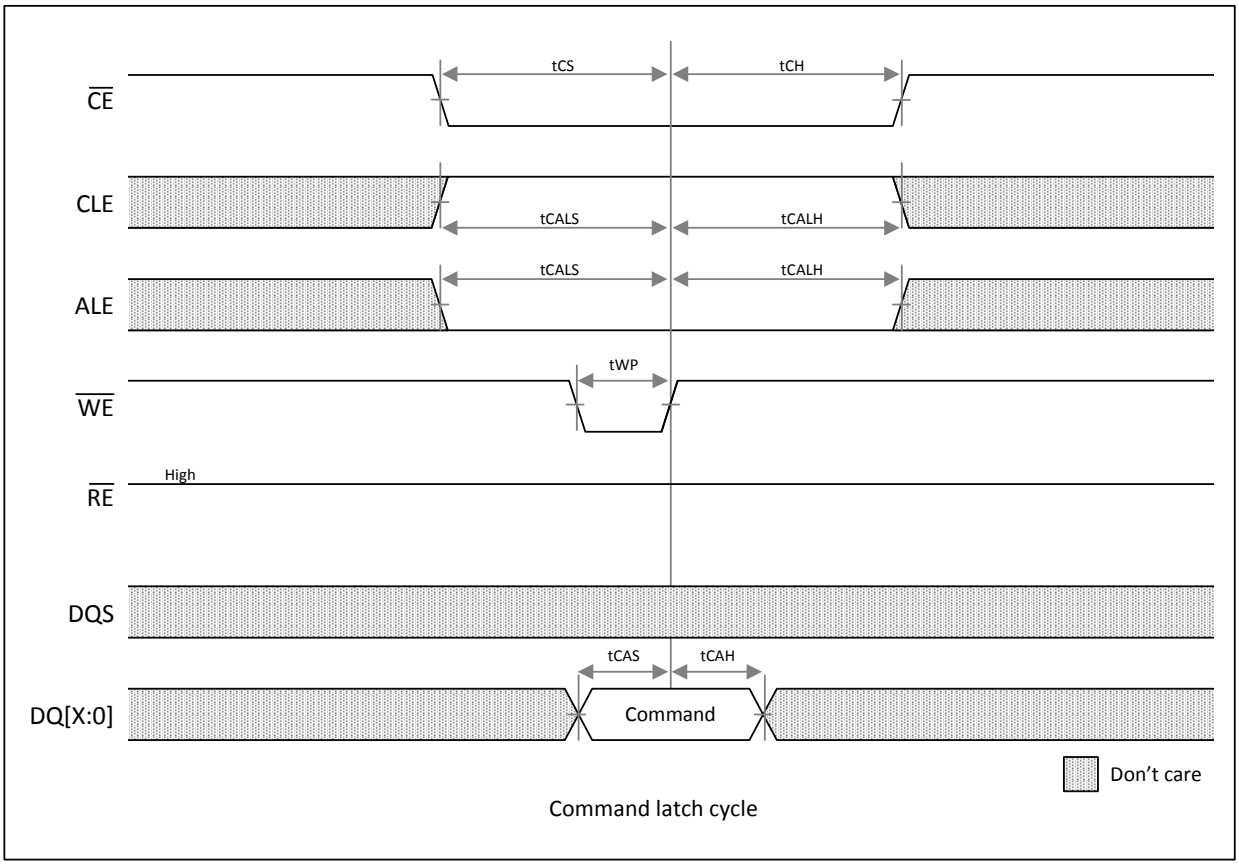
CLE	ALE	CE	WE	RE	DQS	WP	Mode	
H	L	L	Rising	H	X[1]	X	Read Mode	Command Input
L	H	L	Rising	H	X	X		Address Input (5 cycles)
H	L	L	Rising	H	X	H	Write Mode	Command Input
L	H	L	Rising	H	X	H		Address Input (5 cycles)
L	L	L	H	H	falling / Rising	H	Data Input	
L	L	L	H	falling / Rising	falling / Rising	X	Data Output	
X	X	X	X	X	X	L	Write Protect	
X	X	H	X	X	X	0V/VCC [2]	Stand-by	
L	L	L	H	H	H	X	Idle	

NOTE :
1) X can be VIL or VIH.
2) WP should be biased to CMOS high or CMOS low for standby.

4.4. General Timing

4.4.1. Command Latch Cycle

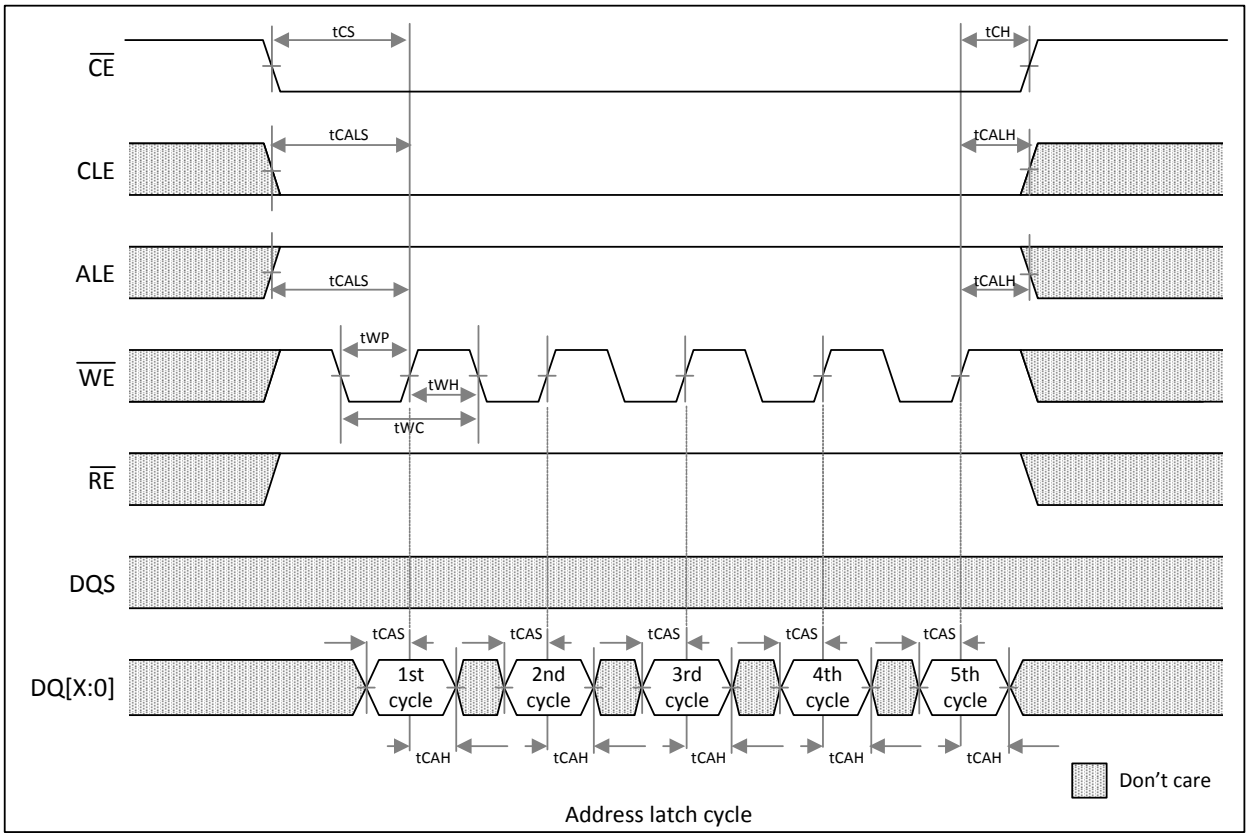
Figure 4-6. Command Latch CycleI



NOTE :
1) Command information is latched by $\overline{WE}$ going 'High' when $\overline{CE}$ is 'Low', CLE is 'High', and ALE is 'Low'.

4.4.2. Address Latch Cycle

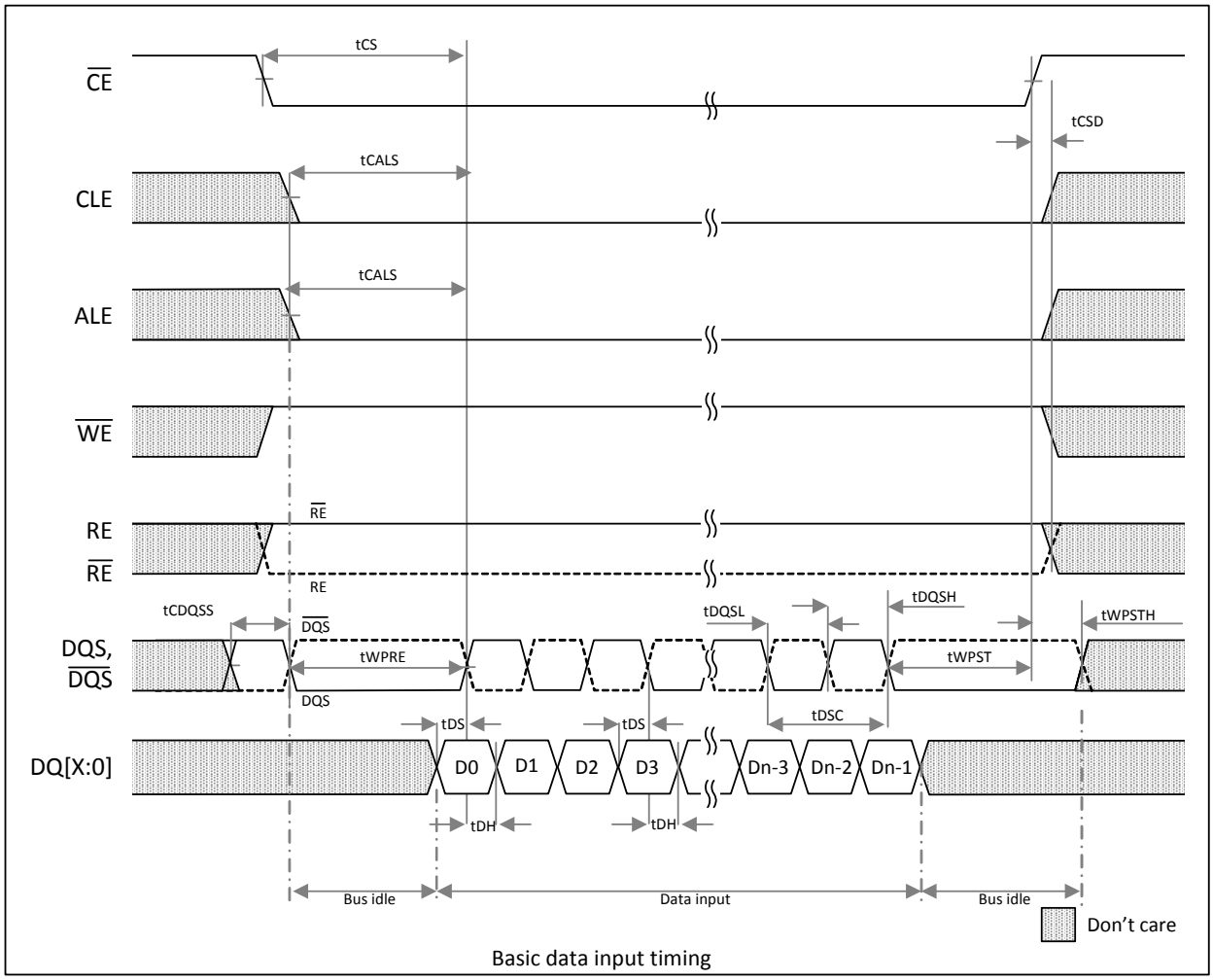
Figure 4-7. Address Latch Cycle



NOTE:
1) Address information is latched by $\overline{WE}$ going 'High' when $\overline{CE}$ is 'Low', CLE is 'Low', and ALE is 'High'.

4.4.3. Basic Data Input Timing

Figure 4-8. Basic Data Input Timing



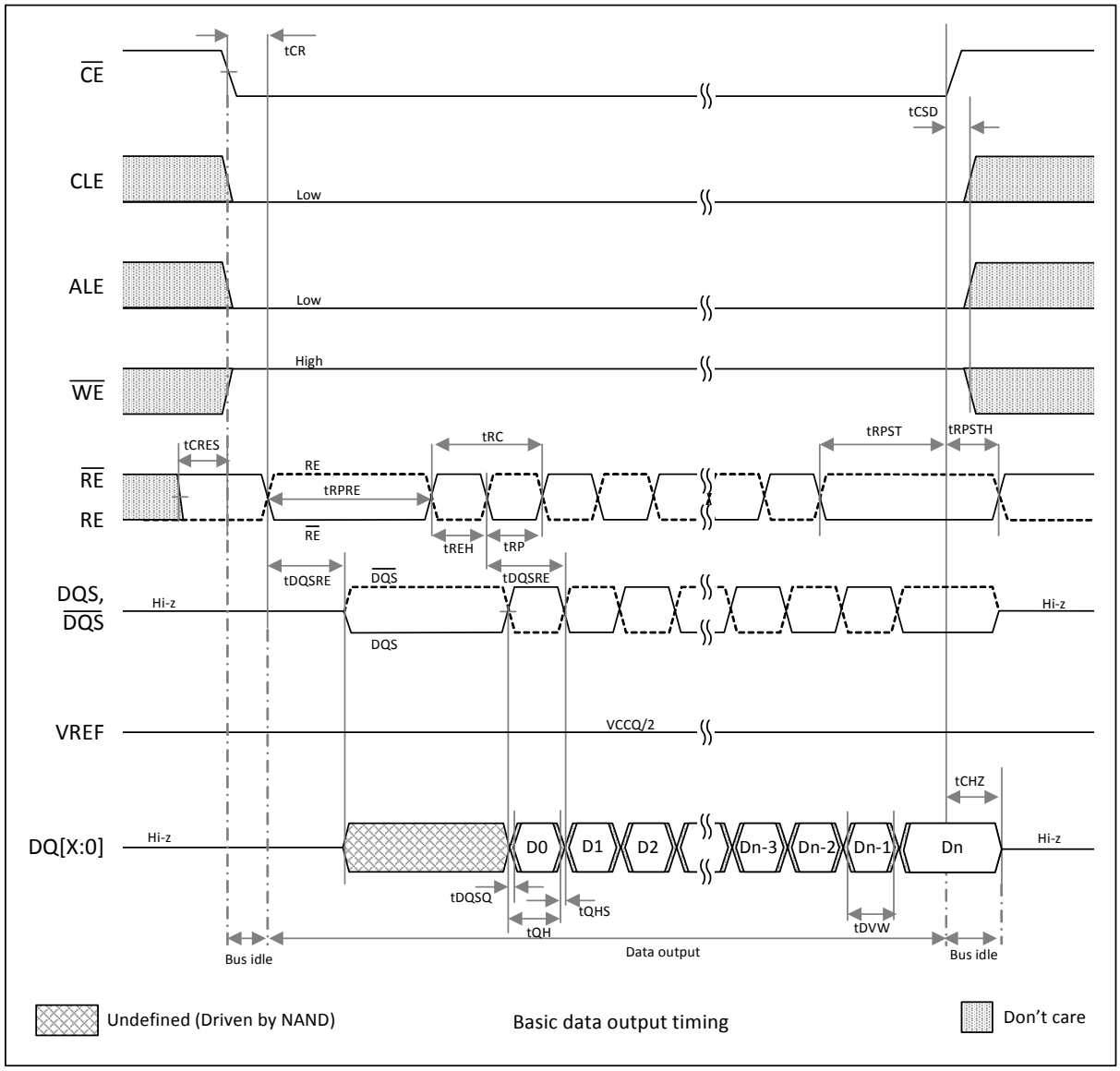
Basic data input timing

NOTE :

1) DQS, DQS and Data input buffers are turned-on when CE and DQS goes 'Low' and Data inputs begin with DQS, DQS toggling simultaneously.
2) ALE and CLE should not toggle during tWPRE period during tCALS.
3) DQS and Data input buffers are turned-off if either CLE or CE goes 'High'.
4) tCDQSS is defined from the last data input condition of the control signals such as CE falling, CLE and ALE.
   It is minimum 100ns before the latest falling edge among CE falling, CLE and ALE.
5) DQS should be fixed high or low during tCDQSS and remained the status(high or low) before tWPRE

4.4.4. Basic Data Output Timing

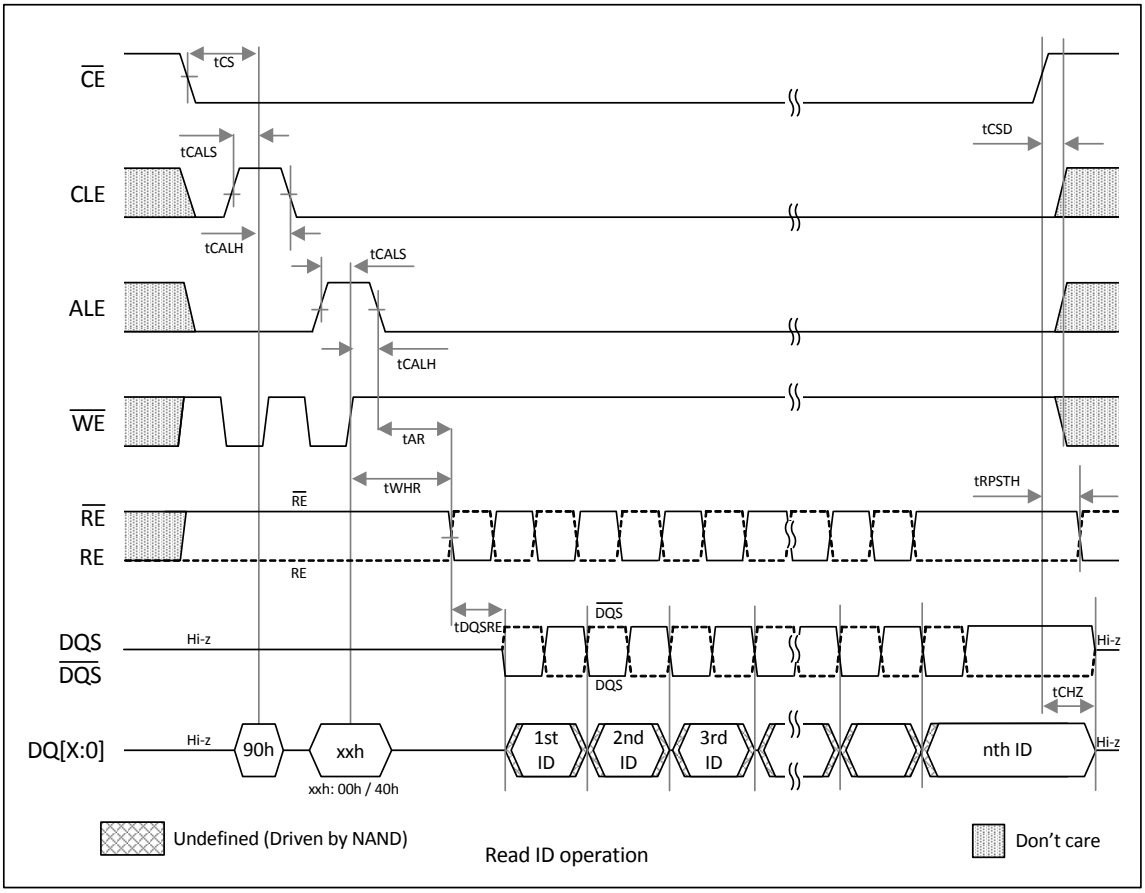
Figure 4-9. Basic Data Output Timing



NOTE :
1) DQS, DQS and DQ drivers are turned-on when CE and RE goes Low for data out operation.
2) ALE and CLE should not toggle during tRPRE period regardless of tCALS.
3) DQS and DQ drivers turn from valid value to high-z if either CLE or CE goes high.
4) The least significant bit of the column address always be zero.

4.4.5. Read ID Operation

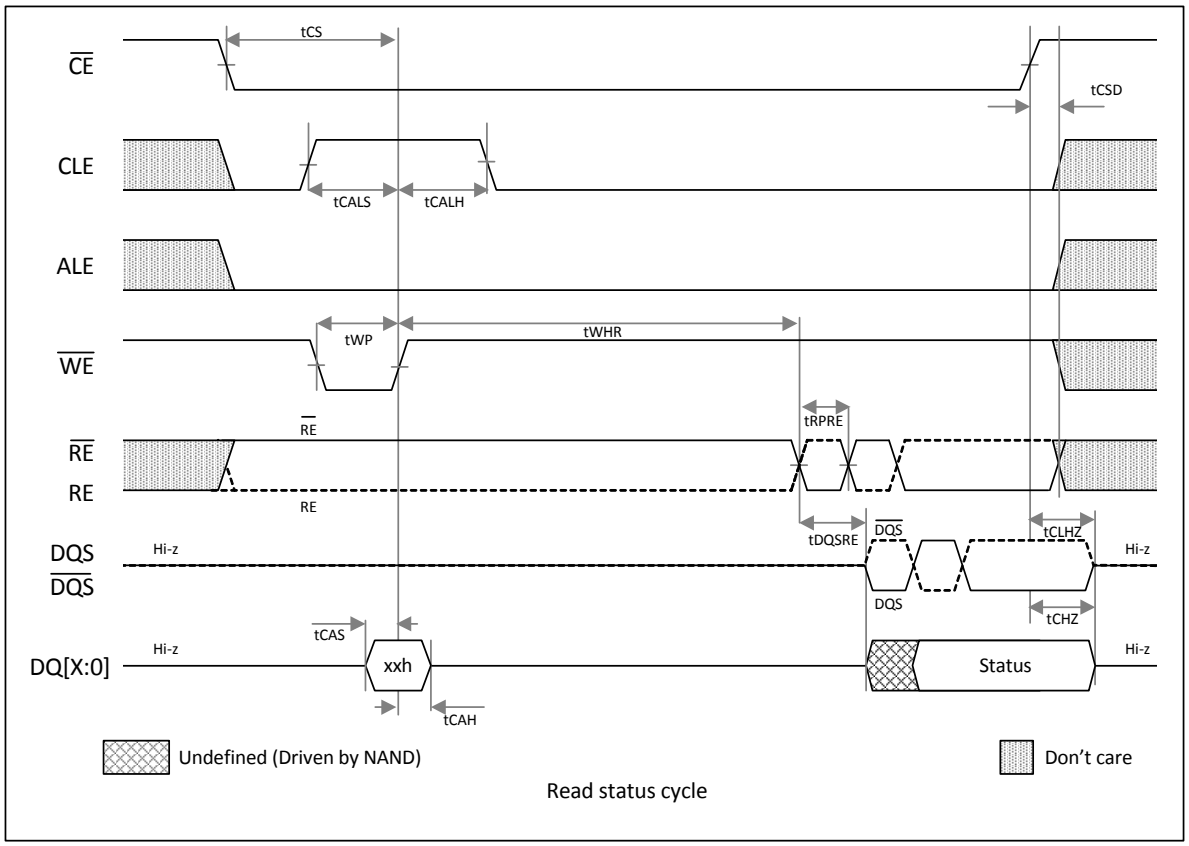
Figure 4-10. Read ID Operation



NOTE :
1) Even though toggle-mode NAND uses both low- and high-going edges of DQS for reads, ID read operation repeats each data byte twice, so that ID read timing becomes identical to that of conventional NAND
2) DQS and DQ drivers turn from valid value to high-z when CE or CLE goes High.
3) Address 00h is for SK hynix conventional and 40h is for new JEDEC ID information.
4) The Read ID shall work on lower than 200Mbps.

4.4.6. Read Status Cycle

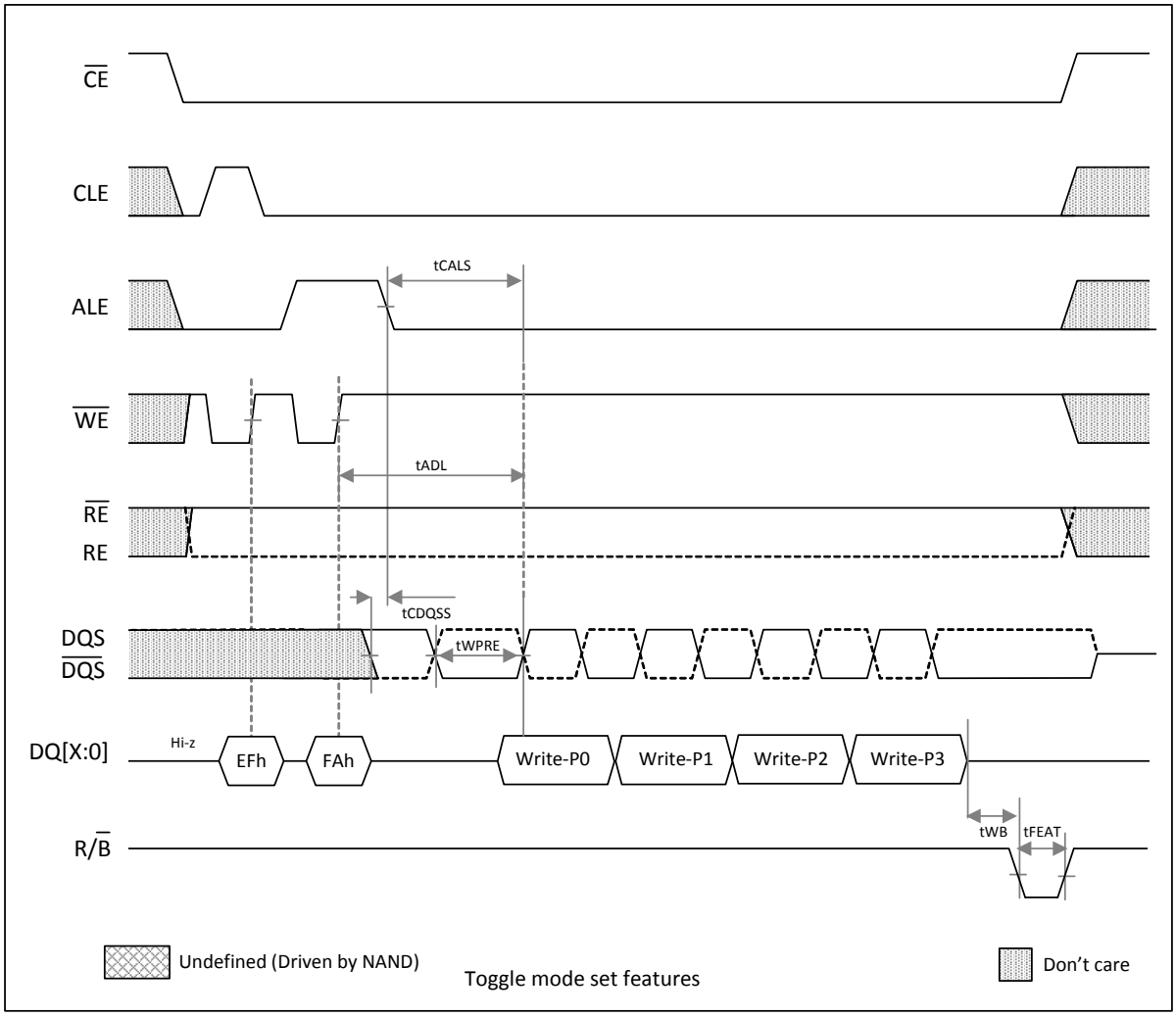
Figure 4-11. Read Status Cycle



NOTE :
1) Status may be continually read by pulsing $\overline{RE}$ or leaving $\overline{RE}$ low.
2) The device supports updating status while RE# is held low.
3) Read Status Enhanced command(78h) requires row address setting steps before reading status value although it is omitted in the above figure.

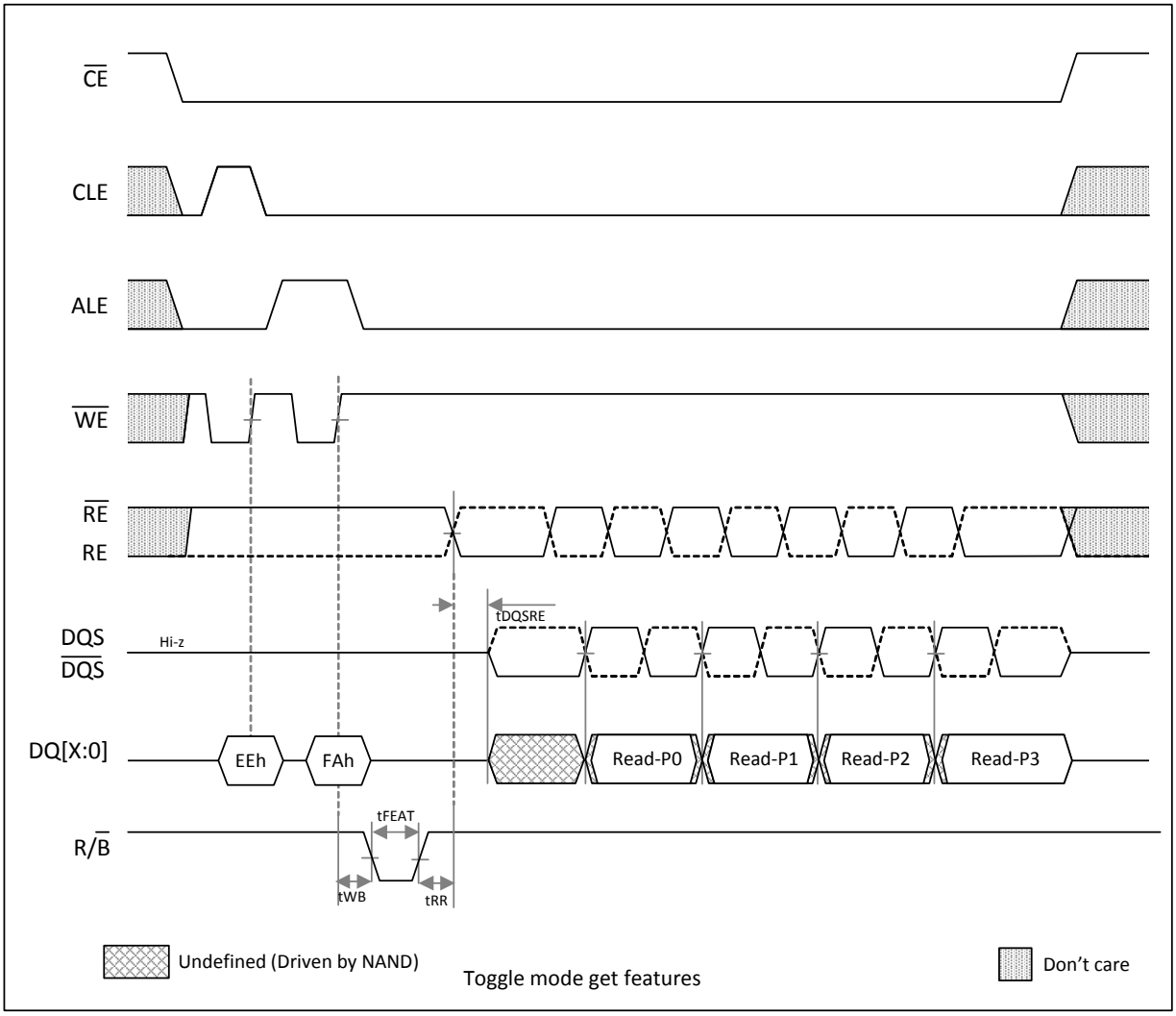
4.4.7. Set Feature

Figure 4-12. Set Feature



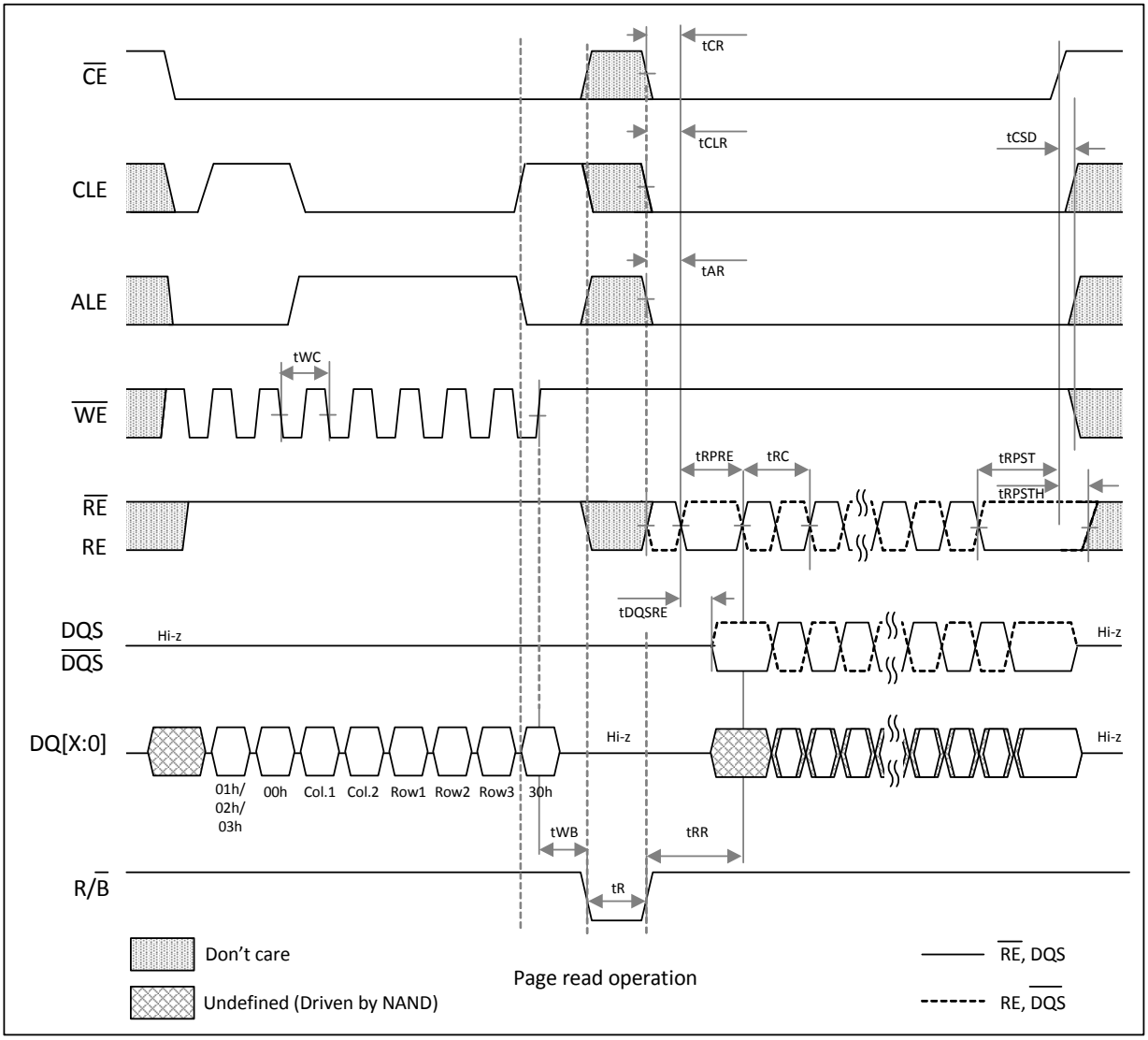
4.4.8. Get Feature

Figure 4-13. Get Feature



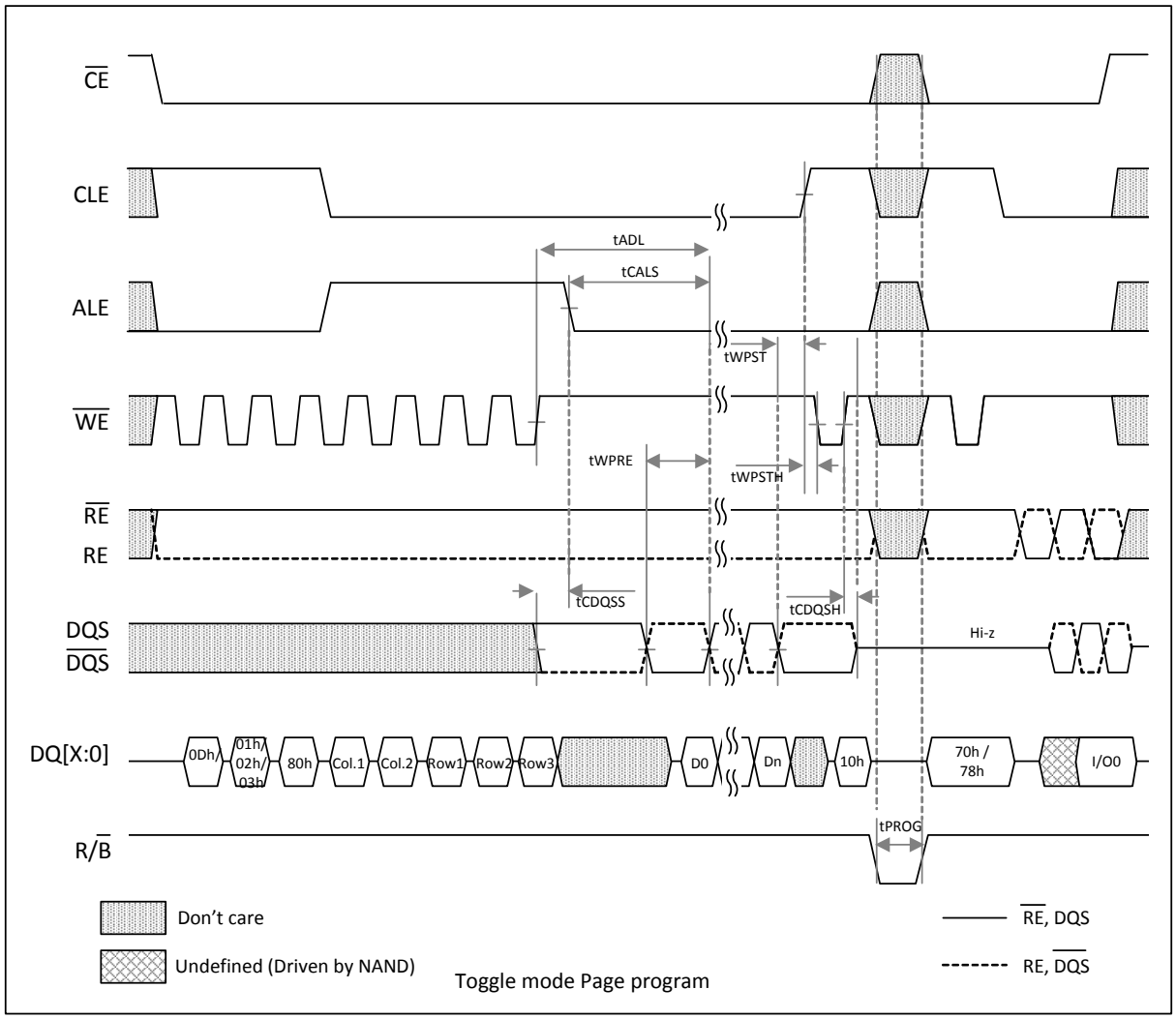
4.4.9. Page Read Operation

Figure 4-14. Page Read Operation



4.4.10. Page Program Operation

Figure 4-15. Page Program Operation



Note:
1) Three pages of LSB/CSB/MSB stored in the same WL are programmed simultaneoudly. Three pages data is required when one WL is programmed at each program stage (1st Coase / 2nd Coarse / Fine).
2) Read Status Enhanced command (78h) requires row address setting steps before reading status value although it is omitted in the above figure.
3) In case of 1st program for 1st Coarse / 2nd program for 2nd Coarse, 09h/0Dh command is needed before the 80h command(3rd Program for Fine, no command is required).
4) In case of LSB and CSB page program operation, 1Ah command is needed after Data in.

4.5. AC Timing Characteristics

4.5.1. Timing Parameters Description

Table 4-3. Toggle DDR Timing Parameters Description

Parameter	Description	Parameter	Description
tR	Data Transfer from Flash array to Register	**tDS**	Data Setup Time
tPROG	Program Time	**tDVW**	Output data valid window
tBERS	Erase Time	**tFEAT**	Busy time for Set Feature and Get Feature
tADL	Address to Data Loading Time	**tQH**	Output hold time from DQS
tAR	ALE Low to $\overline{RE}$ Low	**tQHS**	DQS hold skew factor
tCALH	CLE/ALE Hold Time	**tRC**	Read Cycle Time
tCALS	CLE/ALE Setup Time	**tREH**	$\overline{RE}$ High pulse width
tCAH	Command/Address Hold Time	**tRP**	$\overline{RE}$ Low pulse width
tCAS	Command/Address Setup Time	**tRPP**	$\overline{RE}$ Low width for Read Status at power-up
tCH	$\overline{CE}$ Hold Time	**tRPRE**	Read Preamble
tCDQSH	DQS Hold Time for data input finish	**tRPST**	Read Postamble
tCDQSS	DQS Setup Time for data input start	**tRPSTH**	Read Postamble Hold Time
tCHZ	$\overline{CE}$ High to Output Hi-Z	**tRR**	Ready to $\overline{RE}$ High
tCLHZ	CLE High to Output Hi-Z	**tRST**	Device Resetting Time(Read/Program/Erase)
tCLR	CLE to $\overline{RE}$ Low	**tWB**	$\overline{WE}$ High to Busy
tCOH	Data Hold Time after $\overline{CE}$ disable	**tWC**	Write Cycle Time
tCR	$\overline{CE}$ Low to $\overline{RE}$ Low	**tWH**	$\overline{WE}$ High pulse width
tCRES	$\overline{RE}$ Set up Time	**tWR**	$\overline{WE}$ High to RE Low
tCS	$\overline{CE}$ Setup Time	**tWHR2**	$\overline{WE}$ High to RE Low for Random data out
tCSD	$\overline{CE}$ Disable to signal (CLE, ALE, $\overline{WE}$) don't care	**tWP**	$\overline{WE}$ Low pulse Width
tCWAW	Command Write Cycle to Address Write Cycle Time for Random Data Input and Register Read Out mode	**tWPRE**	Write Preamble
tDH	Data Hold Time	**tWPST**	Write Postamble
tDQSH	DQS Input High Pulse Width	**tWPSTH**	Write Postamble Hold Time
tDQSL	DQS Input Low Pulse Width	**tWW**	$\overline{WP}$ High/Low to $\overline{WE}$ low
tDQSQ	Output skew among data output and corresponding DQS	**tDBSY**	Dummy Busy Time for Multi-Plane Program
tDQSRE	$\overline{RE}$ to DQS and DQ delay	**tCBSY**	Dummy Busy Time for Cache Setting
tDSC	Data Strobe Cycle Time	**tDCBSYR**	Cache Busy in Cache Read
NOTE : 1) Commands (including read status/read status enhanced) shall not be issued until after tWB is complete.			

4.5.2. Timing Parameters Table

Table 4-4. AC Timing Characteristics

Parameter	100MHz		133MHz		166MHz		200MHz		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
tADL	300	-	300	-	300	-	300	-	ns
tAR	10	-	10	-	10	-	10	-	ns
tCALH	5	-	5	-	5	-	5	-	ns
tCALS	15	-	15	-	15	-	15	-	ns
tCAH	5	-	5	-	5	-	5	-	ns
tCAS	5	-	5	-	5	-	5	-	ns
tCDQSH	100	-	100	-	100	-	100	-	ns
tCDQSS	100	-	100	-	100	-	100	-	ns
tCH	5	-	5	-	5	-	5	-	ns
tCHZ	-	30	-	30	-	30	-	30	ns
tCLHZ	-	30	-	30	-	30	-	30	ns
tCLR	10	-	10	-	10	-	10	-	ns
tCOH	5	-	5	-	5	-	5	-	ns
tCR	10	-	10	-	10	-	10	-	ns
tCRES	10	-	10	-	10	-	10	-	ns
tCS	20	-	20	-	20	-	20	-	ns
tCSD	10	-	10	-	10	-	10	-	ns
tCWAW	300	-	300	-	300	-	300	-	ns
tDH	0.9	-	0.75	-	0.55	-	0.40	-	ns
tDQSH	tDSC *0.45	-	tDSC *0.45	-	tDSC *0.45	-	tDSC *0.45	-	ns
tDQSL	tDSC *0.45	-	tDSC *0.45	-	tDSC *0.45	-	tDSC *0.45	-	ns
tDQSQ	-	0.8	-	0.6	-	0.5	-	0.4	ns
tDQSRE	5	25	5	25	5	25	5	25	ns
tDSC	10	-	7.5	-	6	-	5	-	ns
tDS	0.9	-	0.75	-	0.55	-	0.40	-	ns
tDVW	tDVW = tQH - tDQSQ								ns
tFEAT	-	1	-	1	-	1	-	1	us
tQH	tQH = min[tREH, tRP] - tQHS								ns
tQHS	-	0.8	-	0.6	-	0.5	-	0.4	ns
tRC	10	-	7.5	-	6	-	5	-	ns
tREH	tRC*0.45	-	tRC*0.45	-	tRC*0.45	-	tRC*0.45	-	ns
tRP	tRC*0.45	-	tRC*0.45	-	tRC*0.45	-	tRC*0.45	-	ns

Parameter	100MHz		133MHz		166MHz		200MHz		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
tRPP	30	-	30	-	30	-	30	-	ns
tRPRE	15	-	15	-	15	-	15	-	ns
tRPST	tDQSRE + tRC*0.5	-	tDQSRE + tRC*0.5	-	tDQSRE + tRC*0.5	-	tDQSRE + tRC*0.5	-	ns
tRPSTH	25	-	25	-	25	-	25	-	ns
tRR	20	-	20	-	20	-	20	-	ns
tRST	10 /200/ 200								us
tWB	-	100	-	100	-	100	-	100	ns
tWC	25	-	25	-	25	-	25	-	ns
tWH	11	-	11	-	11	-	11	-	ns
tWHR	120	-	120	-	120	-	120	-	ns
tWHR2	300		300		300		300		ns
tWP	11		11		11		11		ns
tWPRE	15		15		15		15		ns
tWPST	6.5		6.5		6.5		6.5		ns
tWPSTH	25		25		25		25		ns
tWW	100		100		100		100		ns

4.5.3. Read/Program / Erase Characteristics

Table 4-5. NAND Read/Program/Erase Characteristics

Parameter	Symbol	Cell Type	Min	Typ	Max	Units
Data Transfer from Flash array to Register	tR (16KB)	TLC	-	100	-	us
		SLC	-	65	-	us
	tR (8KB)		-	70	-	us
Program Time	tPROG	TLC	-	2.0	-	ms
		SLC	-	0.5	-	ms
	tPROG (Channel)	TLC	-	2.2	-	ms
		SLC	-	0.5	-	ms
Dummy Busy Time for Multi-Plane setting	tDBSY	-	-	0.5	1	us
Dummy Busy Time for Cache Setting	tCBSY	-	-	-	tPROG	us
Data Transfer Time for LSB	tDTBSY1	TLC	-		20us	us
Data Transfer Time for CSB	tDTBSY2	TLC	-		20us	us
Cache Busy in Cache Read	tDCBSYR	-	-	-	tR	us
Number of Partial Program Cycles in the Same Page	Nop	-	-	-	1	cycle
Block Erase Time	tBERS	TLC	-	6.5	10	ms
		SLC	-	5	10	ms

NOTE :

1) Typical program time is measured at Vcc=3.3V, TA=25^{o}C. Not 100% tested.
2) Typical Program time is defined as the time within which more than 50% of the whole pages are programmed at 3.3V Vcc and 25^{o}C temperature.

5. FUNCTION DESCRIPTION AND DEVICE OPERATION

5.1. Basic Command Sets

Toggle DDR NAND Flash Memory has addresses multiplexed into 8-Data Input/Output. Command, address and data are all written through DQ[7:0] by bringing WE# to low while CE is low. Those are latched on the rising edge of WE. Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the DQ[7:0] pins. Commands which apply to a specific page or block typically have a second command and ones that apply to a target or a LUN have a first command only.

Table 5-1. Basic Command Set

Command	Primary or secondary	1st Set	Address Cycles for 1st Set	2nd Set	Acceptable while Accessed LUN is Busy	Acceptable while Other LUNs are Busy
1st Program for 1st Coarse[2)]	Primary	09h	-	-	-	Y
2nd Program for 2nd Coarse[2)]	Primary	0Dh	-	-	-	Y
3rd Program for Fine[2)]	Primary	-	-	-	-	Y
LSB Page	Primary	01h	-	-	-	
CSB Page	Primary	02h	-	-	-	
MSB Page	Primary	03h	-	-	-	
Page Read	Primary	00h	5	30h	-	Y
Sequential Cache Read	Primary	31h	-	-	-	Y
Read Start for Last Page Cache Read	Primary	3Fh	-	-	-	Y
Random Cache Read	Primary	00h	5	31h	-	Y
Page Program	Primary	80h	5	10h	-	Y
Transfer Data to Page Buffer	Primary	1A	-	-	-	Y
Cache Program	Primary	80h	5	15h	-	Y
Block Erase	Primary	60h	3	D0h	-	Y
Read for Copy-Back	Primary	00h	5	35h	-	Y
Copy-Back Program	Primary	85h	5	10h	-	Y
Random Data Input[1)]	Primary	85h	2	-	-	Y
Random Data Output[1)]	Primary	05h	2	E0h	-	Y
Set Features	Primary	EFh	1	-	-	-
Get Features	Primary	EEh	1	-	-	-
Read ID	Primary	90h	1	-	-	-
Read Status	Primary	70h	-	-	Y	Y
Reset	Primary	FFh	-	-	Y	Y
Reset LUN	Primary	FAh	3	-	Y	Y

Command	Primary or secondary	1st Set	Address Cycles for 1st Set	2nd Set	Acceptable while Accessed LUN is Busy	Acceptable while Other LUNs are Busy
SLC Mode Change	Primary	A2h	-	-	-	Y
Half Page Read	Primary	00h	5	2Dh/2Eh	-	Y

Note:
1) Random Data Input / Output can be executed in a page.
2) In case of 1st Program for 1st Coarse / 2nd Program for 2nd Coarse, 09h/0Dh command is needed before the 80h command(3rd Program for Fine, no command is required).
3) In case of LSB and CSB Page Program operation, 1Ah command is needed after Data In.
In case of MSB Page Program operation, 10h command is needed after Data In.

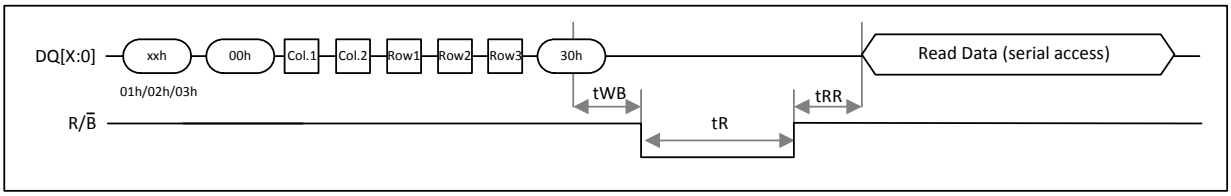
Caution:
1) Any undefined command Inputs are prohibited except for above command set.
2) Cache read and program operation should be operated at lower than 100MHz
3) Cache program operation is available for only SLC blocks.

5.2. BASIC OPERATION

5.2.1. Page Read Operation

The Page Read function reads a page of data identified by row address for the selected LUN. The page of data is made available to be read from the page register starting at the specified column address. Figure of "*Page Read Operation*" defines the Page Read behavior and timings. Reading beyond the end of a page results in indeterminate values being returned to the host.

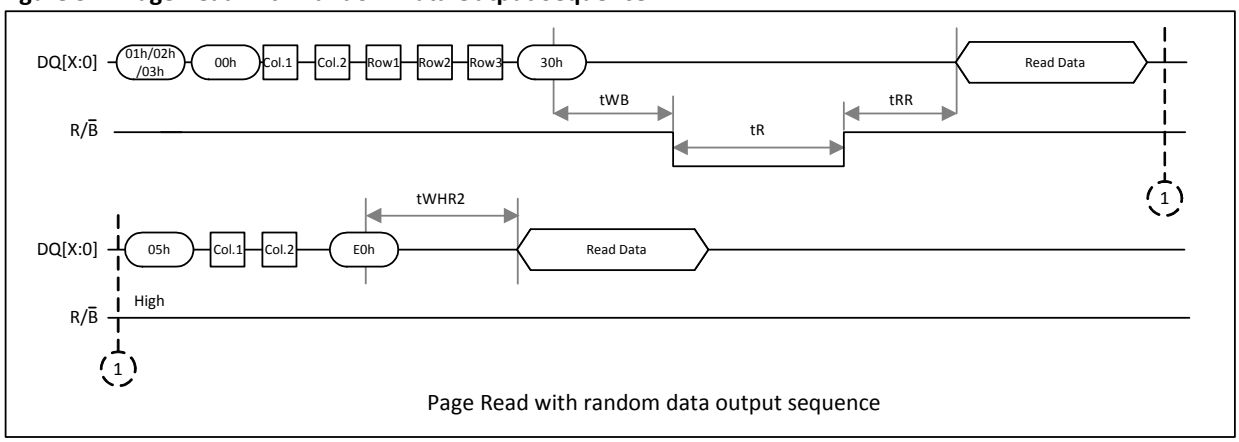
Figure 5-1. Page Read Operation



5.2.1.1. Page Read Operation with Random Data Output

TThe Random Data Output function changes the column address from which data is being read in the page register for the selected LUN. The Random Data Output command shall only be issued when the LUN is in a read idle condition. Figure of *"Page Read with Random Data Output Sequence"* defines the Random Data Output behavior and timings. The host shall not read data from the LUN until tWHR(ns) after the second command (i.e. E0h) is written to the LUN.

Figure 5-2. Page Read with Random Data Output Sequence

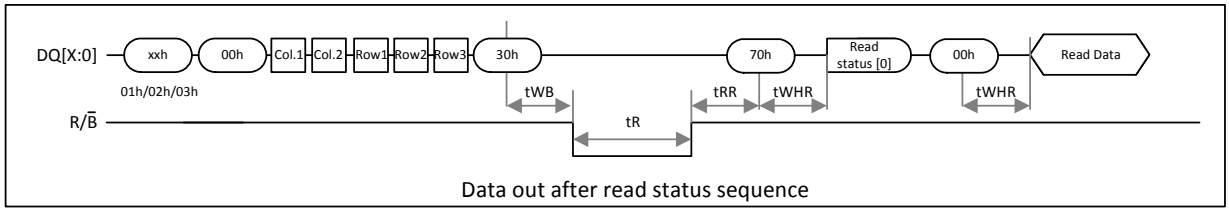


Page Read with random data output sequence

5.2.1.2. Data Out After Read Status

While monitoring the read status to determine when the tR (transfer from Flash array to apage register) is complete, the host re-issue the 00h command to start reading data. Issuing the 00h command will cause data to be returned starting at the selected column address.

Figure 5-3. Data Out After Read Status Sequence

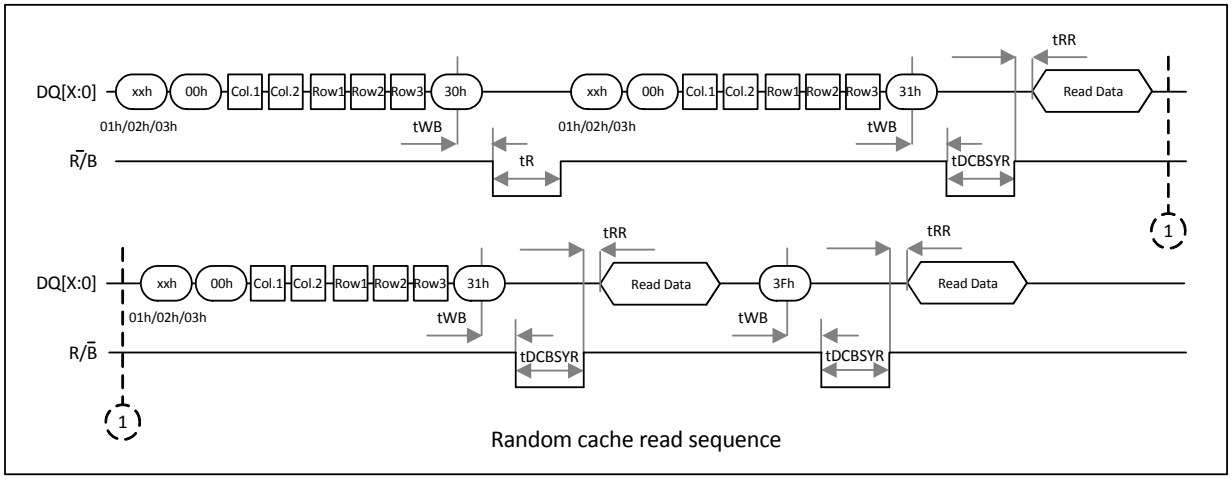


Data out after read status sequence

5.2.2. Random Cache Read Operation

A Read Page command shall be issued prior to the initial Random Cache Read command in a cache read sequence like the Sequential Cache Read operation. A Random Cache Read command shall be issued prior to the Read Start for Last Page Cache Read command(3Fh) being issued. The page and block address can be accessed in a random manner. Figure of "*Random Cache Read Timing*" defines the Random Cache Read behavior and timings.

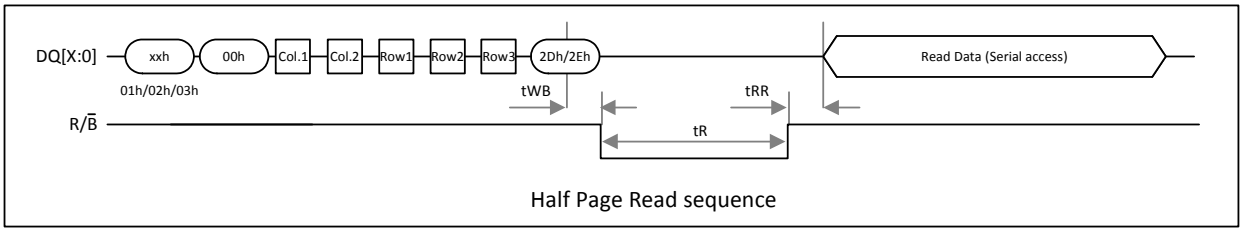
Figure 5-4. Random Cache Read Timing



5.2.3. Half Page Read

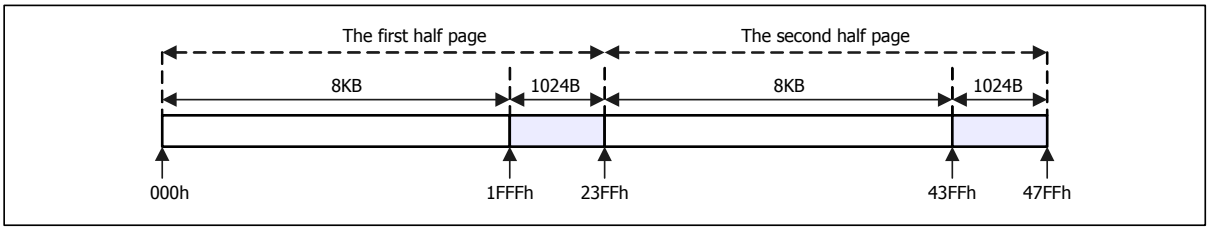
The Fast Half Read function transfers only half page data in NAND array to page register. This function helps applications maximize random read or write throughput. Fast Half Read operation supports only a single plane based Read operation.

Figure 5-5. Half Page READ sequence



There are the first half page or the second half page which is determined by confirm command and column address. The first half page data is transferred when the confirm command 2Dh is issued with column address between 0000h and 23FFh. The second half page data is transferred when the confirm command 2Eh is issued with column address between 2400h to 47FFh. Figure of "*Page layout for Half Page READ*" represents the page layout when Fast 8KB Read is used.

Figure 5-6. Page layout for Half Page READ



5.2.5. Page Program Operation

The device is programmed on a page basis, and each page shall be programmed only once before being erased. The addressing order shall be sequential within a block. The contents of the page register are programmed into the Flash array specified by row address. SR[0] is valid for this command after SR[6] transitions from zero to one until the next transition of SR[6] to zero. Figure of "*Program Timing for SLC Block*" and Figure of "*Program Timing for TLC Block*" define the Page Program behavior and timings. Writing beyond the end of the page register is undefined.

The following program order is required for programming the pages within one block. Random page program is not allowed. LSB, CSB, and MSB shall be inputted and programmed three times in the page. Data from the three pages in one WL can be read out only after the 3rd program cycle. The data in the last WL can be read out after the third program cycle is done.

5.2.5.1. SLC Mode and TLC Mode

In addition to the TLC mode, the device provides an SLC mode for the data required for frequent updates, high performance, and high reliability. To switch TLC mode to SLC mode, an A2h command shall be prefixed before Normal SLC operation including program, read, and erase. SLC mode will reset to TLC mode automatically at the end of each SLC operation.

Once a block is assigned to operate in one mode, the block should always stay to operate in the same mode during the life of the device. The block selected to TLC mode has to complete programming the whole pages in a block before program operation for another block begins.

Figure 5-7. Program Timing for SLC Block

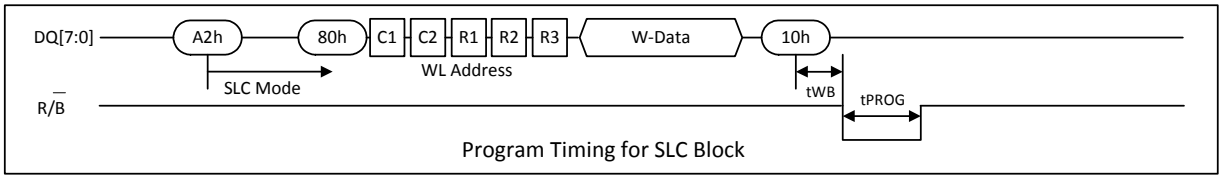
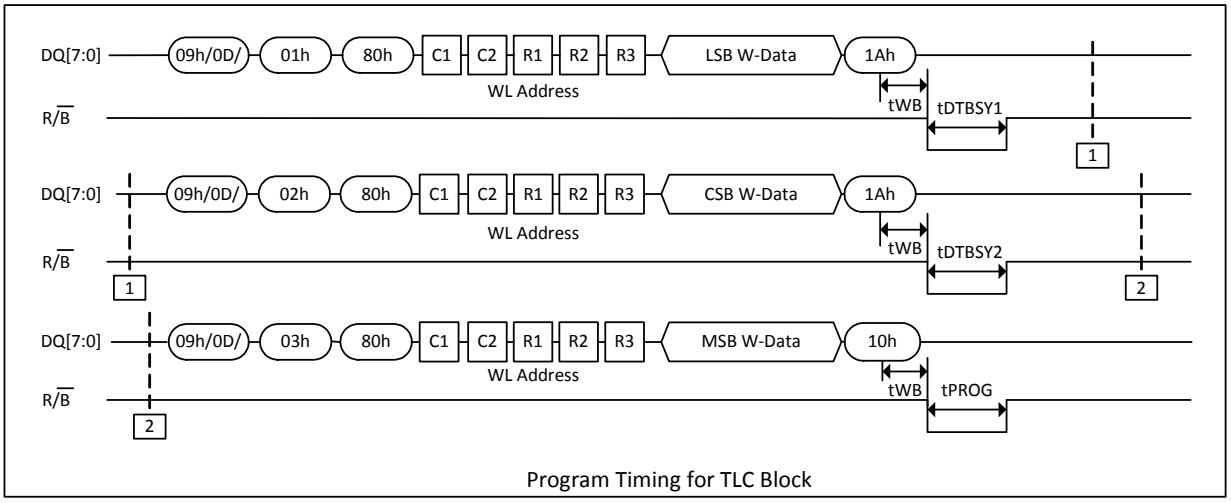


Figure 5-8. Program Timing for TLC Block



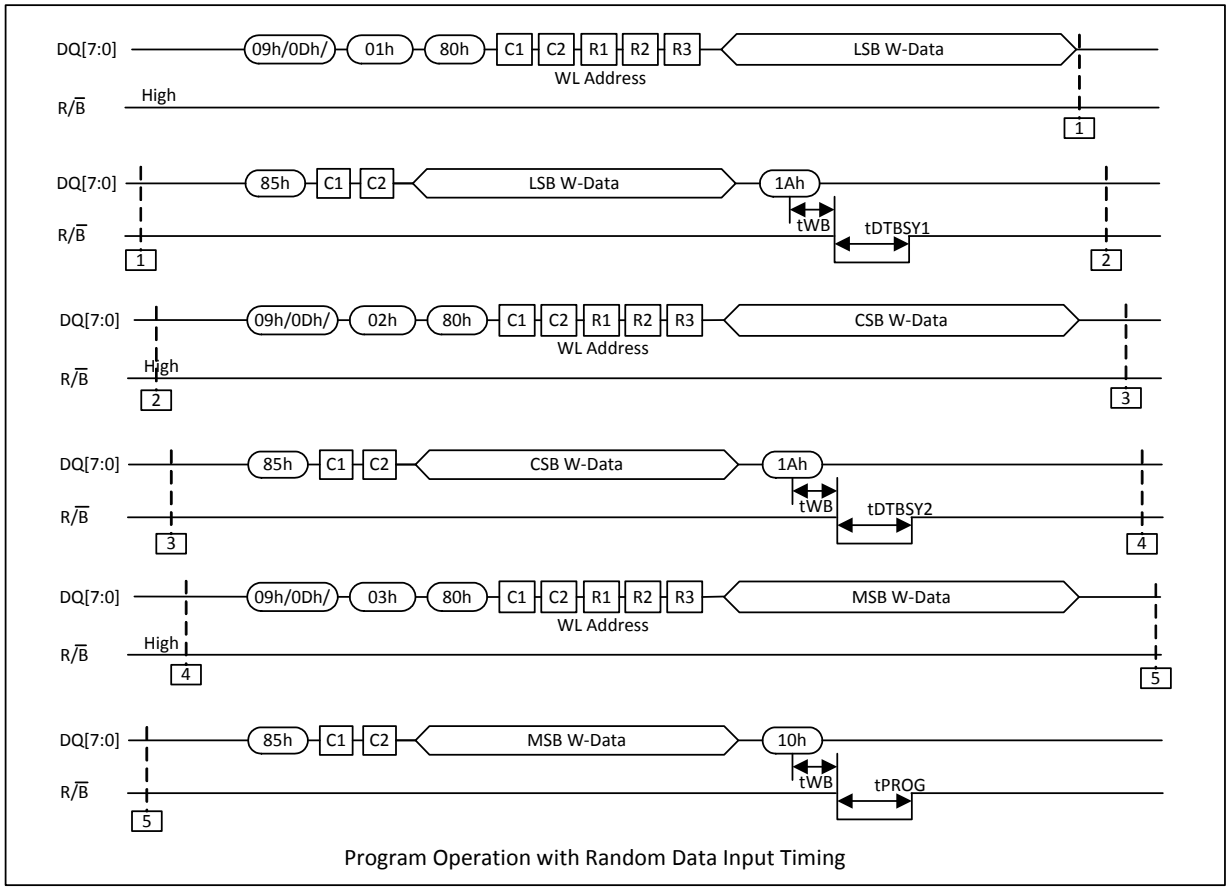
Note:
1) Three Pages of LSB/CSB/MSB stored in the same WL are programmed simultaneously. Three pages data is required when one WL is programmed at each program stage (1st Coarse / 2nd Coarse / Fine).

2) Read Status Enhanced command (78h) requires row address setting steps before reading status value although it is omitted in the above figure.
3) In case of 1st Program for 1st Coarse/2nd Coarse for 2nd Coarse, 09h/0Dh command is needed before the 80h command (3rd Program for Fine, no command is required).
4) In case of LSB and CSB Page Program operation, 1Ah command is needed after Data In

5.2.5.2. Program Operation with Random Data Input

The device supports random data input in a page. The column address for the next data, which will be written, may be changed to the address using Random data input command(i.e. 85h). Random data input may be operated multiple times without limitation.

Figure 5-9. Program Operation with Random Data Input Timing



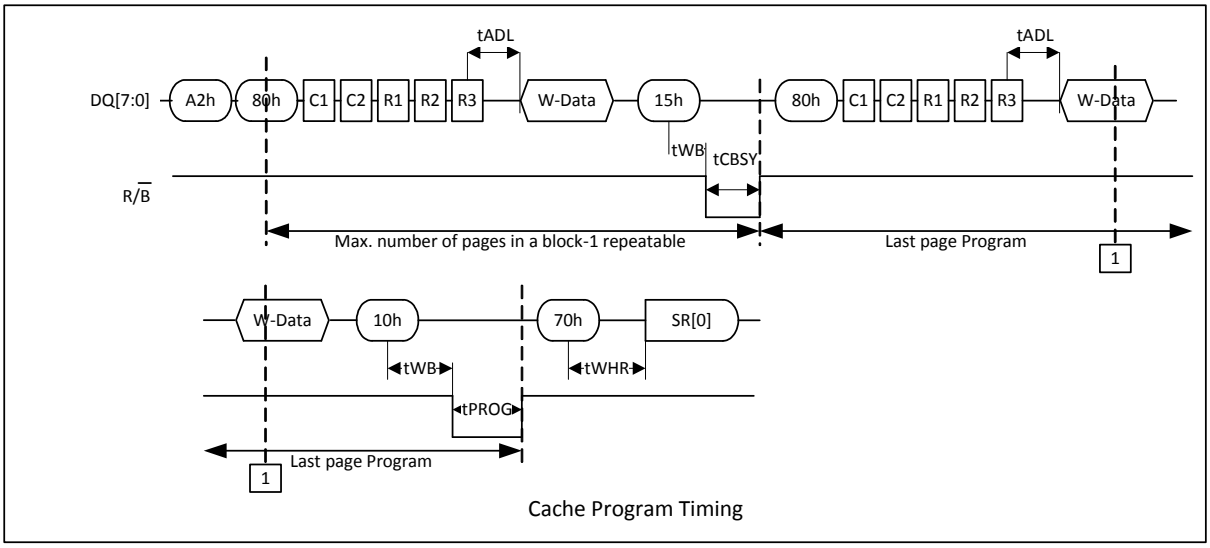
Program Operation with Random Data Input Timing

Note:
1) Three Pages of LSB/CSB/MSB stroed in the same WL are programmed simultaneously. Three pages data is required when one WL is programmed at each program stage (1st Coarse / 2nd Coarse / Fine).
2) Read Status Enhanced command (78h) requires row address setting steps before reading status value although it is omitted in the above figure.
3) In case of 1st Program for 1st Coarse/2nd Coarse for 2nd Coarse 09h/0D command is needed before the 80h command (3rd Program for Fine, no command is required).
4) In case of LSB and CSB Page Program operation, 1Ah command is needed after Data In.

5.2.6. Cache Program Operation - For SLC mode

The Cache Program function allows the host to write the next data for another page to the page register while a page of data to be programmed to the Flash array for the selected LUN. When command 15h is issued, R/B# returns high (i.e. ready) when a cache register is ready to be written after data in the cache register is transferred to a page register. However, when command 10h is issued for the final page, R/B turns to high after outstanding program operation performed by previous Cache Program command and the program operation for the final page is completed. SR[0] is valid for this command after SR[5] transitions from zero to one until the next transition. SR[1] is valid for this command after SR[6] transitions from zero to one, and it is invalid after the first Cache Program Command completion since there is no previous Cache Program operation. Cache Program operation shall work only within a block. Figure of "Cache Program Timing" defines the Cache Program behavior and timings.
Note that tPROG at the end of the caching operation may be longer than typical as this time also includes completing the programming operation for the previous page. Writing beyond the end of the page register is undefined.

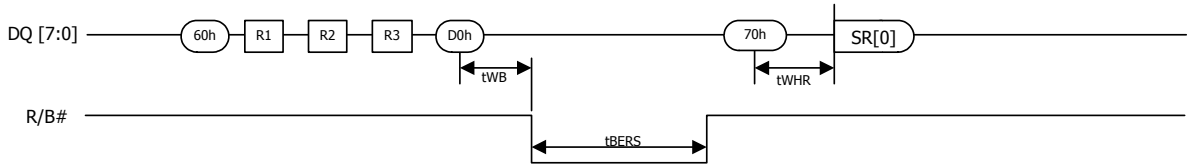
Figure 5-10. Cache Program Timing



5.2.7. Block Erase Operation

The Block Erase operation is done on a block basis. Only three cycles of row addresses are required for Block Erase operation and a WL address within the cycles is ignored while plane and block address are valid.
After Block Erase operation passes, all bits in the block shall be set to one. SR[0] is valid for this command after SR[6] transitions from zero to one(i.e. the selected LUN is ready) until the LUN goes in busy state by a next command.
Figure of *"Block Erase Timing"* defines the Block Erase behavior and timings.

Figure 5-11. Block Erase Timing



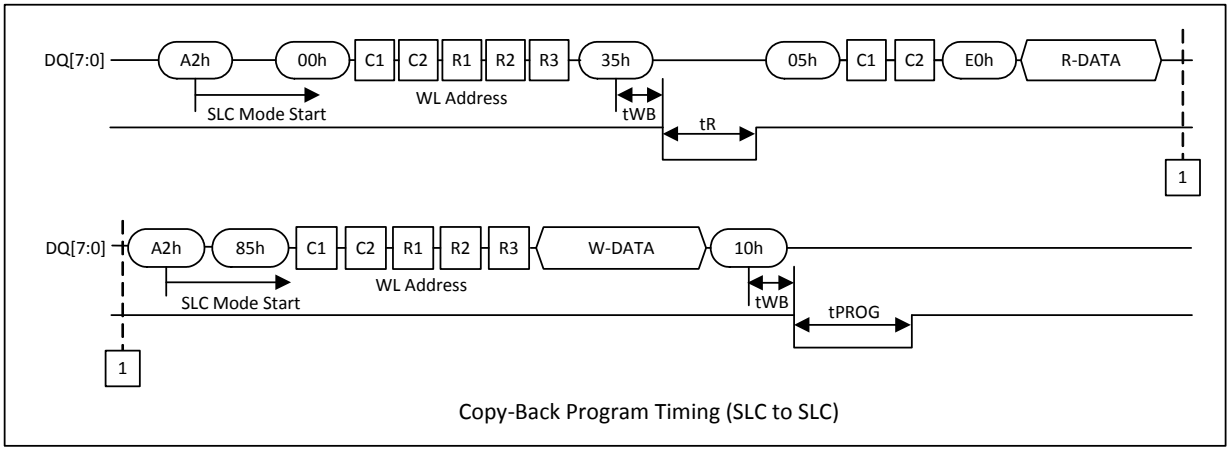
5.2.8. Copy-Back Program Operation

The Copy-Back Program with Read for Copy-Back is configured to efficiently rewrite data stored in a page without data re-loading when no error within the page is found. Since the time-consuming re-loading cycles are removed, copy-back operation helps the system performance improve. The benefit is especially obvious when a part of a block is updated and the rest of the block also needs to be copied to the newly assigned free block.

The Copy-Back operation consists of 'Read for Copy-Back' and 'Copy-Back Program'. A host reads a page of data from a source page using 'Read for Copy-Back' and copies read data back to a destination page on the same LUN by 'Copy-Back Program' command. Copy-Back Program Operation shall work only within the same plane. After a host completes to read data from a page register, the host may modify data using Random Data Input command if required. We provide three kinds of copy-back operations for each mode (SLC and TLC mode).

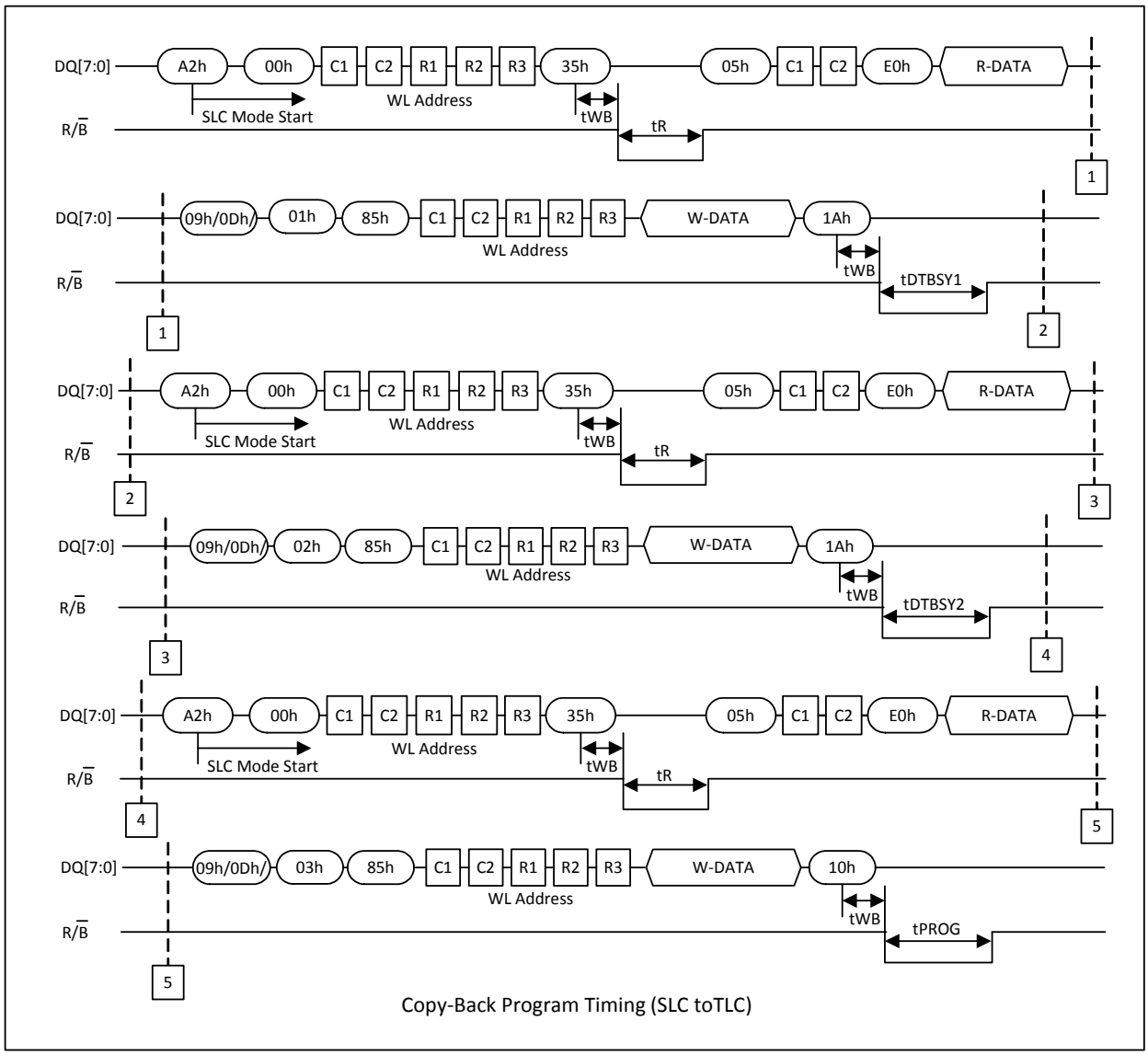
Figure *"Copy-Back Program Timing (SLC to SLC)*, Figure *"Copy-Back Program Timing (SLC to TLC)",* and Figure *"Copy-Back Program Timing (TLC to TLC)"* defines the Copy-Back Program behavior and timings.

Figure 5-12. Copy-Back Program Timing (SLC to SLC)



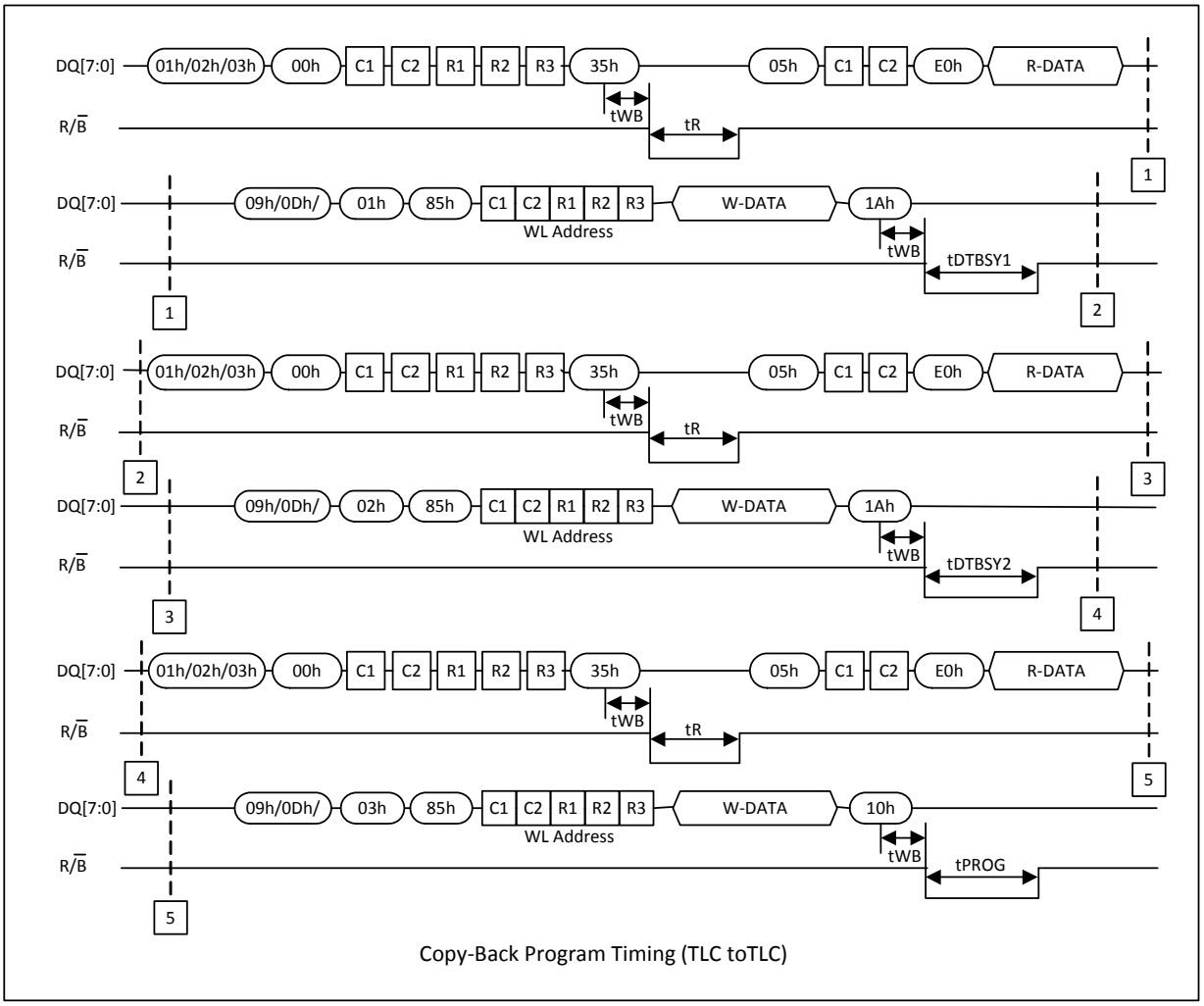
Copy-Back Program Timing (SLC to SLC)

Figure 5-13. Copy-Back Program Timing (SLC to TLC)



Copy-Back Program Timing (SLC toTLC)

Figure 5-14. Copy-Back Program Timing (TLC to TLC)



Copy-Back Program Timing (TLC toTLC)

5.2.8. Set Feature Operation

Users may set particular features using 'Set Feature' operation. Every feature will be reset by power down or FFh(i.e. Reset, except 1st FFh). Figure of "*Set Feature Timing*" defines the Set Features behavior and timings and Table *"Set Feature addresses"* defines features that users can change. Once Set feature operation begins, the operation shall be completed without any disturbance and interruption such as Reset operation.

Figure 5-15. Set Feature Timing

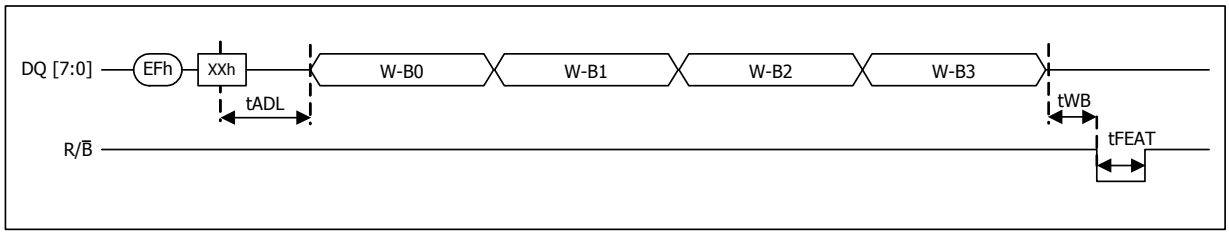


Table 5-2. Set feature addresses

1st Cycle	2nd Cycle	Description
EFh	01h	Timing mode setting
	02h	Toggle 2.0 specific setting
	10h	Driver strength setting
	30h	External VPP setting

5.2.8.1. Timing mode setting (01h)

If the Reset (FFh) command is issued when the Data Interface is configured as DDR, then the host shall use the SDR data interface until a new data interface is selected with Set Features.

The results of the host using Set Features to transition from the DDR to the SDR is indeterminate.
To transition to the SDR data interface, the host should use the Reset (FFh) command.

Table 5-3. Timing mode setting assignment

	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
B0	Reserved		Data Interface		Reserved			
B1	Reserved							
B2	Reserved							
B3	Reserved							

NOTE : B1, B2 and B3 are reserved and shall be written with 00h.

	Description
Data Interface	00 : SDR (default power-on value) 10 : DDR others : Reserved

5.2.8.2. Toggle 2.0 specific setting (02h)

This setting is required in order to use reference voltage and complementary signal. DQS latency cycle can also be configured by this SET FEATURE operation to read the first valid data correctly.

Table 5-4. Toggle 2.0 specific setting assignment

	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
B0	Reserved				Reserved	$\overline{RE}$	$\overline{DQS}$	VREFQ
B1	# of Latence DQS cycle for Write				# of Latence DQS cycle for Read			
B2	Reserved							
B3	Reserved							

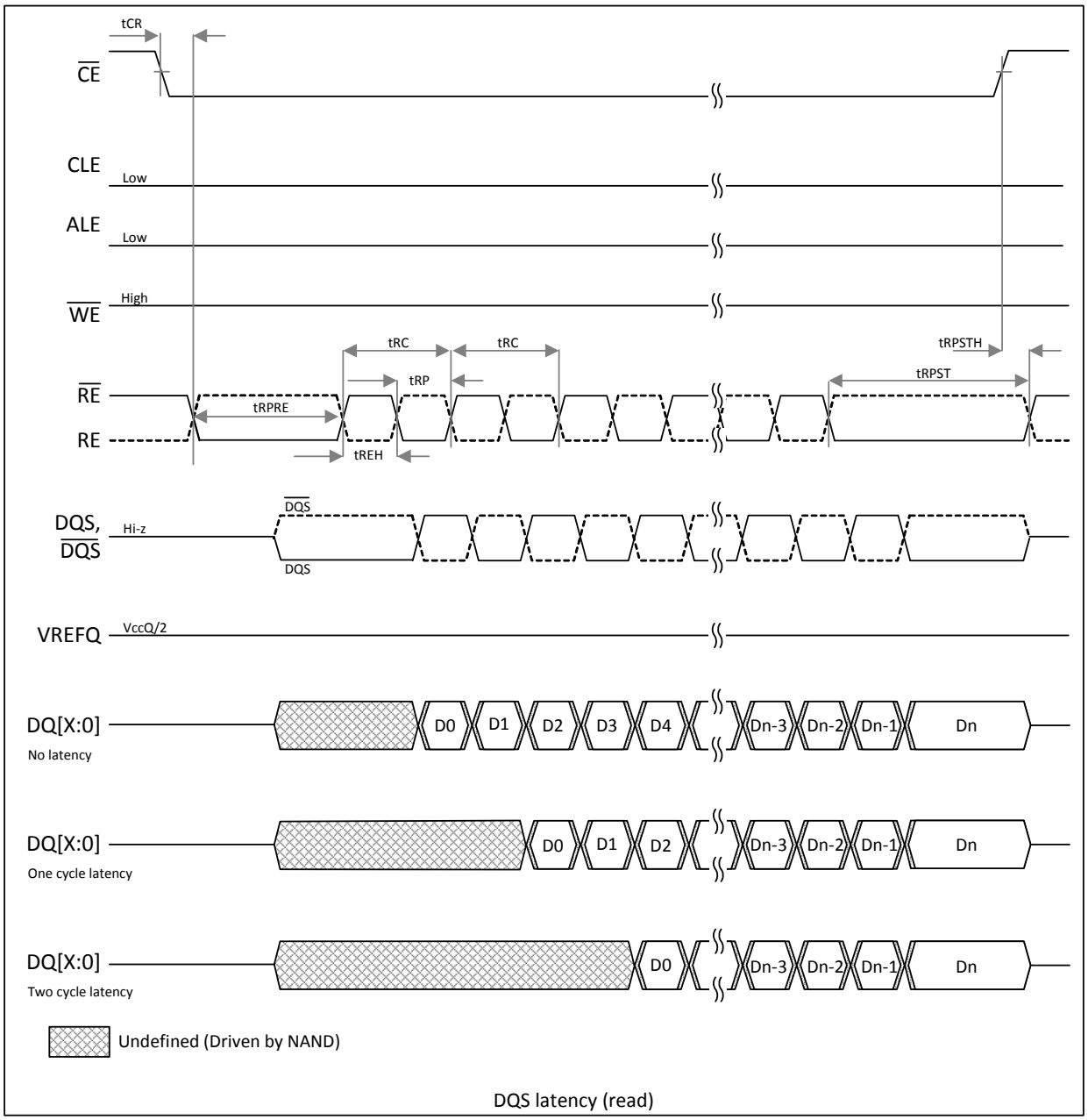
NOTE :
1)B3 are reserved and shall be written with 00h.

Table 5-5. Definition of Toggle 2.0 specific setting

	Description
VREFQ	0 : Disabled (dafault) 1 : Enabled
$\overline{DQS}$	0 : Disabled (default) 1 : Enabled
RE_c	0 : Disabled (default) 1 : Enabled
# of Latency DQS cycle (READ/Write)	0000 : No latency DQS cycle (default) 0001 : One latency DQS cycle 0010 : Two latency DQS cycle 0011 : Four latency DQS cycle

NOTE :
1) B2 and B3 are reserved and shall be written with 00h.

Figure 5-16. Example of DQS latency



DQS latency (read)

5.1.8.3. Driver strength setting (10h)

Driver strength is configured according to the B0 value.

Table 5-6. Definition of Driver strength setting

P0 Value	Description
00h ~ 01h	Reserved
02h	Driver Multiplier : Underdriver
03h	Reserved
04h	Driver Multiplier : 1 (default)
05h	Reserved
06h	Driver Multiplier : Overdriver 1
07h	Reserved
08h	Driver Multiplier : Overdriver 2
09h ~ FFh	Reserved

NOTE:
B1, B2 and B3 are reserved and be written with 00h.

5.1.6.4. External VPP (30h)

External high voltage(i.e. typical 12V) feature offers power saving on program and read operations. The external high voltage shall be supplied prior to the feature setting and it shall persist within 11.5V to 12.5V until it is set to defalut(i.e. off). The maximum external Vpp supply current per LUN is 5mA.

Table 5-7. Definition of External Vpp

P0 Value	Description
00h	OFF(default)
01h	ON
02h ~ FFh	Reserved

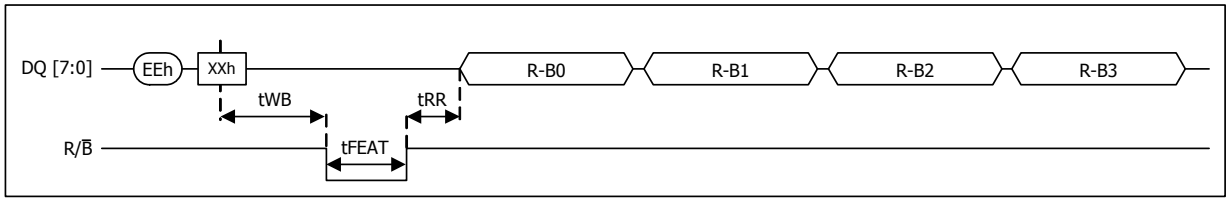
NOTE :
P1, P2 and P3 are reserved and shall be written with 00h.

5.2.9. Get Feature Operation

Users find how the target is set through 'Get Feature' command. The function return the current setting information. If a host starts to read the first byte of data (i.e. B0 value), the host complete reading all four bytes of data before issuing another command (including Read Status or Read Status Enhanced). Figure of "*Get Feature Timing*" defines the Get Features behavior and timings.

If Read Status (or Read Satus Enhanced) is used to monitor whether the tFEAT time is complete, the host issue Read command (i.e. 00h) to read B0-B1-B2-B3.

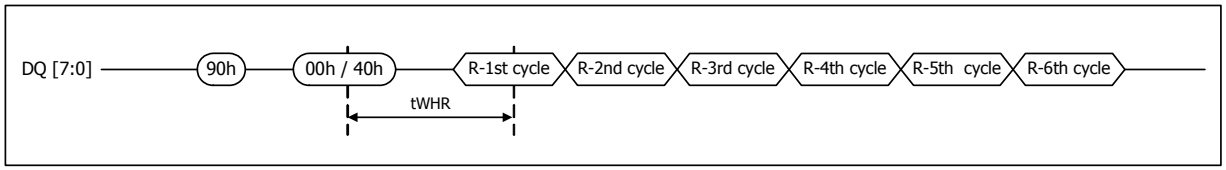
Figure 5-17. Get Feature Timing



5.2.10. Read ID Operation

The ID of a target is read by command 90h followed by 00h or 40h address. Read ID operation work on lower than 200Mbps. Figure of "*Read ID Timing*" defines Read ID operation behavior and timings.

Figure 5-18. Read ID Sequence



5.2.10.1. 00h Address ID Definition

Users can read six bytes of ID containing manufacturer code, device code and architecure information of the target by command 90h followed by 00h address. The command register remains in Read ID mode until another command is issued.

Table 5-8. 00h address ID cycle

Device	Density	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle	6th Cycle
H27QDG8M2M5R-BCF	16GB (128Gb)	ADh	5Ah	18h	A3h	61h	65h
H27QEG8NDM5R-BCF	32GB (256Gb)	ADh	5Ah	18h	A3h	61h	65h
H27QFG8PEM5R-BCF	64GB (512Gb)	ADh	5Ah	18h	A3h	61h	65h
H27Q1T8QEM6R-BCF	128GB (1Tb)	ADh	5Ch	19h	A3h	62h	65h
H27QFG8PQM2R-BCF	64GB (512Gb)	ADh	5Ah	18h	A3h	61h	65h
H27Q1T8QQM3R-BCF	128GB (1Tb)	ADh	5Ch	19h	A3h	62h	65h
H27Q1T8QRM3R-BCF	128GB (1Tb)	ADh	5Ah	18h	A3h	61h	65h

Device	Density	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle	6th Cycle
H27Q2T8LQM3R-BCF	256GB (2Tb)	ADh	5Eh	1Ah	A3h	63h	65h
H27QDG882MLR-BCC	16GB (128Gb)	ADh	5Ah	18h	A3h	61h	65h
H27QEG89DNLR-BCC	32GB (256Gb)	ADh	5Ah	18h	A3h	61h	65h

Table 5-9. Read ID Definition - Address ID cycle

	Description
1st Byte	Maker Code
2nd Byte	Device Code
3rd Byte	Internal Number, Cell Type, Number of Program pages, Cache program
4th Byte	Page size (without Spare area), Block size (without Additional Block), Redundant Area size
5th Byte	Plane Number, ECC Level
6th Byte	NAND Technology, Interface

5.2.10.2. 40h Address ID Definition

Toggle DDR NAND also provide a six bytes of JEDEC standard signature ID. Users can read the ID by command 90h followed by 40h address. Any data returned after the six bytes of JEDEC standard signature is considered reserved for future use.

Table 5-10. 40h Address ID Cycle

1st Cycle	2nd	3rd Cycle	4th Cycle	5th Cycle	6th Cycle
4Ah	45h	44h	45h	43h	42h

Table 5-11. 40h Address ID Cycle

Cycle	Description	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
1st	J	0	1	0	0	1	0	1	0
2nd	E	0	1	0	0	0	1	0	1
3rd	D	0	1	0	0	0	1	0	0
4th	E	0	1	0	0	0	1	0	1
5th	C	0	1	0	0	0	0	1	1
6th	Async. SDR Toggle DDR	0	1	0	0	0 0	0 0	0 1	1 0

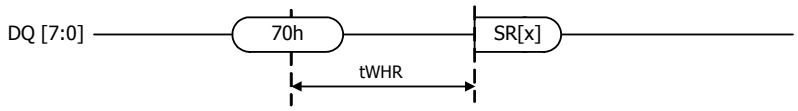
5.2.11. Read Status Operation

In the case of non-multi-plane operations, the Read Status function retrieves a status value for the last operation issued. If multiple multi-plane operations are in progress on a single LUN, then Read Status returns the composite status value. Specifically, Read Status return the combined status value of the independent status register bits according to Table for *"Read Status Definition"* Figure of "*Read Status Sequence*" defines the Read Status behavior and timings.

Table 5-12. Read Status Definition

	DQ0	DQ1	DQ2	DQ3	DQ4	DQ5	DQ6	DQ7
Definition of value	Pass : "0" Fail : "1"	Pass : "0" Fail : "1"	Reserved	Reserved	Reserved	Busy : "0" Ready : "1"	Busy : "0" Ready : "1"	Protected : "0" Not Protected : "1"
Block Erase	Pass/Fail	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready	Write Protect
Page Program	Pass/Fail	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready	Write Protect
Cache Program	Pass/Fail for the current page	Pass/Fail for the previous page	Not Use	Not Use	Not Use	Busy/Ready for Flash array	Busy/Ready for Host	Write Protect
Read	Not Use	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready	Write Protect
Cache Read	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready for Flash array	Busy/Ready for Host	Write Protect

Figure 5-19. Read Status Timing

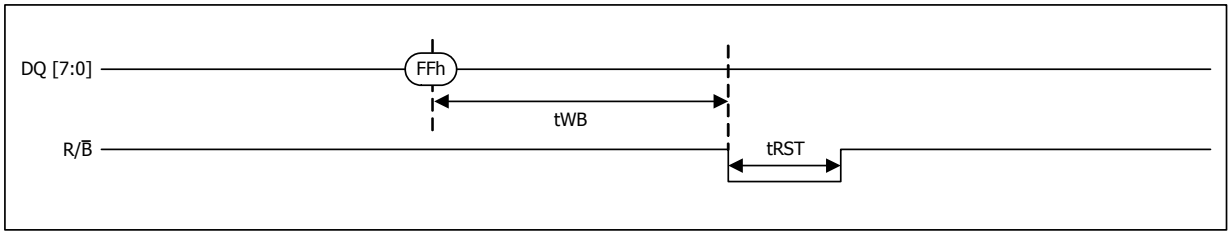


Note:
1) During Block Erase, Page Program, DQ0 is only valid when DQ6 shows the Ready state
3) During Cache Program operation, DQ0 is only valid when DQ5 shows the Ready state, and DQ1 is only valid when DQ6 shows the Ready state.

5.2.12. Reset Operation

Toggle DDR NAND offers a reset function by command FFh. When the device is in 'Busy' state during any operation, the Reset operation will abort these operations except during power-on when Reset shall not be issued until R/$\overline{B}$ is set to one (i.e. ready). The contents of memory cells being programmed are no longer valid, as the data will be partially programmed or erased. Although the device is already in process of reset operation, a new reset command will be accepted. Figure of *"Reset Timing"* defines the Reset behavior and timings.

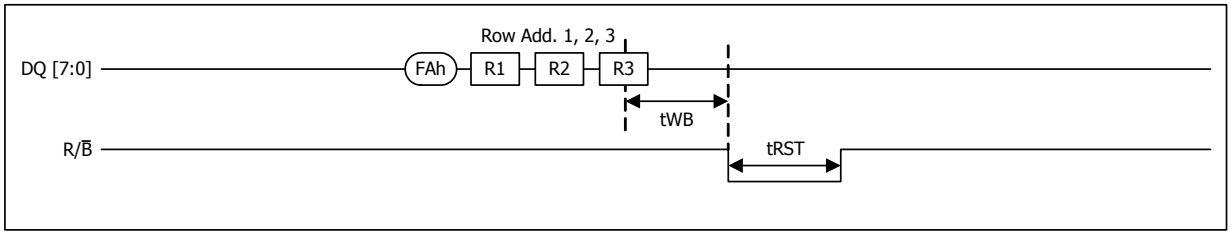
Figure 5-20. Reset Timing



5.2.13. Reset LUN operation

A certain LUN within a target can be reset by command FAh followed by row addresses. Row addresses are required to set a LUN to be reset. Figure of "*Single Chip Reset Timing*" defines the Reset LUN behavior and timings.

Figure 5-21. Single Chip Reset Timing



5.3. Extended OPERATION

5.3.1. Extended Command Sets

Table of "*Extended Command Sets*" defines the Extended Command Sets. Primary and Secondary Commands are also categorized in the table. Primary commands are recommended to use when a particular function is implemented, while Secondary commands are for alternative implementation for backward compatibility.

Table 5-13. Extended Command Sets

Function	Primary or secondary	1st Set	Address Cycles for 1st Set	2nd Set	Address Cycles for 2nd Set
Two-Plane Page Read / Two-Plane Page Cache Read	Primary	00h--32h	5	00h--30h	5
Two-Plane Random Cache Read	Primary	00h--32h	5	00h--31h	5
Two-Plane Random Data Output 1)	Primary	00h---05h	5	--E0h	2
Two-Plane Page Program	Primary	80h--11h 2)	5	80h--10h	5
Two-Plane Cache Program	Primary	80h--11h 2)	5	80h--15h	5
Two-Plane Block Erase	Primary	60h--D1	3	60h--D0h	3
Two-Plane Read for Copy-Back	Primary	00h--32h	5	00h--35h	5
Two-Plane Copy-Back Program	Primary	85h--11h	5	85h--10h	5
Device Identification Table Read	Primary	ECh--	1	-	-
Read status enhanced	Primary	78h	3	-	-
Read LUN#0 Status	Secondary	F1h	-	-	-
Read LUN#1 Status	Secondary	F2h	-	-	-
Read LUN#2 Status	Secondary	F3h	-	-	-
Read LUN#3 Status	Secondary	F4h	-	-	-

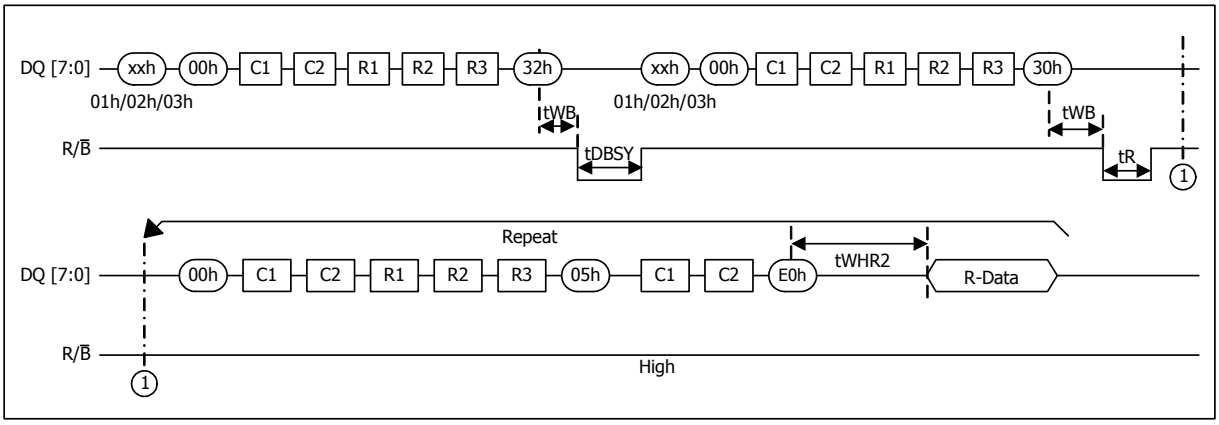
NOTE :
1) Two-Plane Random Data out must be used after Two-Plane Page Read or Two-Plane Cache Read operation. The address between 00h--05h is for selecting plane address.
2) Any operation between Multi Plane Operation Command set is prohibited except status read commands as 70h/78h/F1h/F2h and FFh.

5.3.2. Two-Plane Page Read Operation

The Two-Plane Page Read operation is an extension of the Page Read operation. The device supporting Two-plane page read operation also allows multi Random data-output from each plane(i.e. Two-Plane Random Data Output) once multi-pages from each plane are loaded to page registers. With the primary command, R/$\overline{B}$ returns to ready in a short time(i.e. tDBSY) after the first command 32h since it does not load data from a selected page, and the selected page data of each plane are transferred to the cache registers via page registers in less than tR after command 30h. When setting page and WL addresses of each plane, the page and WL addresses be identical although block addresses differ.

Once the data is loaded into the cache registers, the data on the first plane can be read out by issuing the Two-Plane Random Data Output command. The data on the other plane can be also read out using the identical command sequences. Figure of "*Example Timing with Two-plane Page Read*" define Two-plane Page Read and Two-Plane Random Data Output behavior and timings.

Figure 5-22. Example Timing with Two-plane Page Read

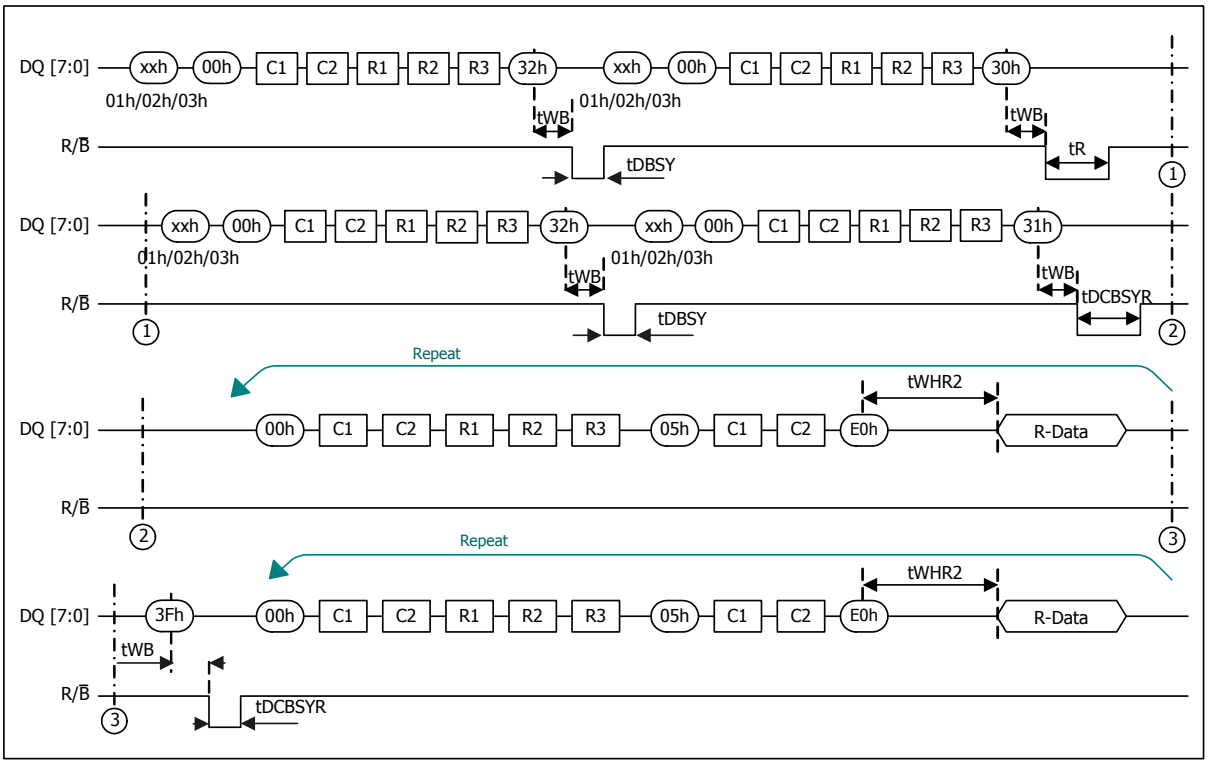


5.3.3. Two-Plane Random Cache Read

Two-Plane Random Cache Read function requires multiple address setting ahead of command 31h to load data of particular pages. Since the selected pages are loaded to page register while a host read data from cache register where previous data is loaded, R/B returns high (i.e. ready) in a short time unless the previous data is still being loaded.

The activated planes for the first Two-Plane Random Cache Read be kept using in the next address sequence until the Two-Plane Random Cache operation is completed by command 3Fh. Figure of "*Example Timing with Two-plane Random Cache Read*" defines Two-Plane Random Cache Read behavior and timings.

Figure 5-23. Example Timing with Two-plane Random Cache Read

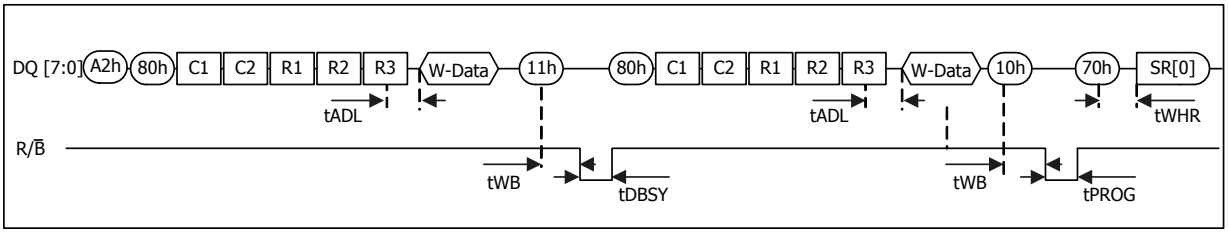


5.3.4. Two-Plane Page Program Operation

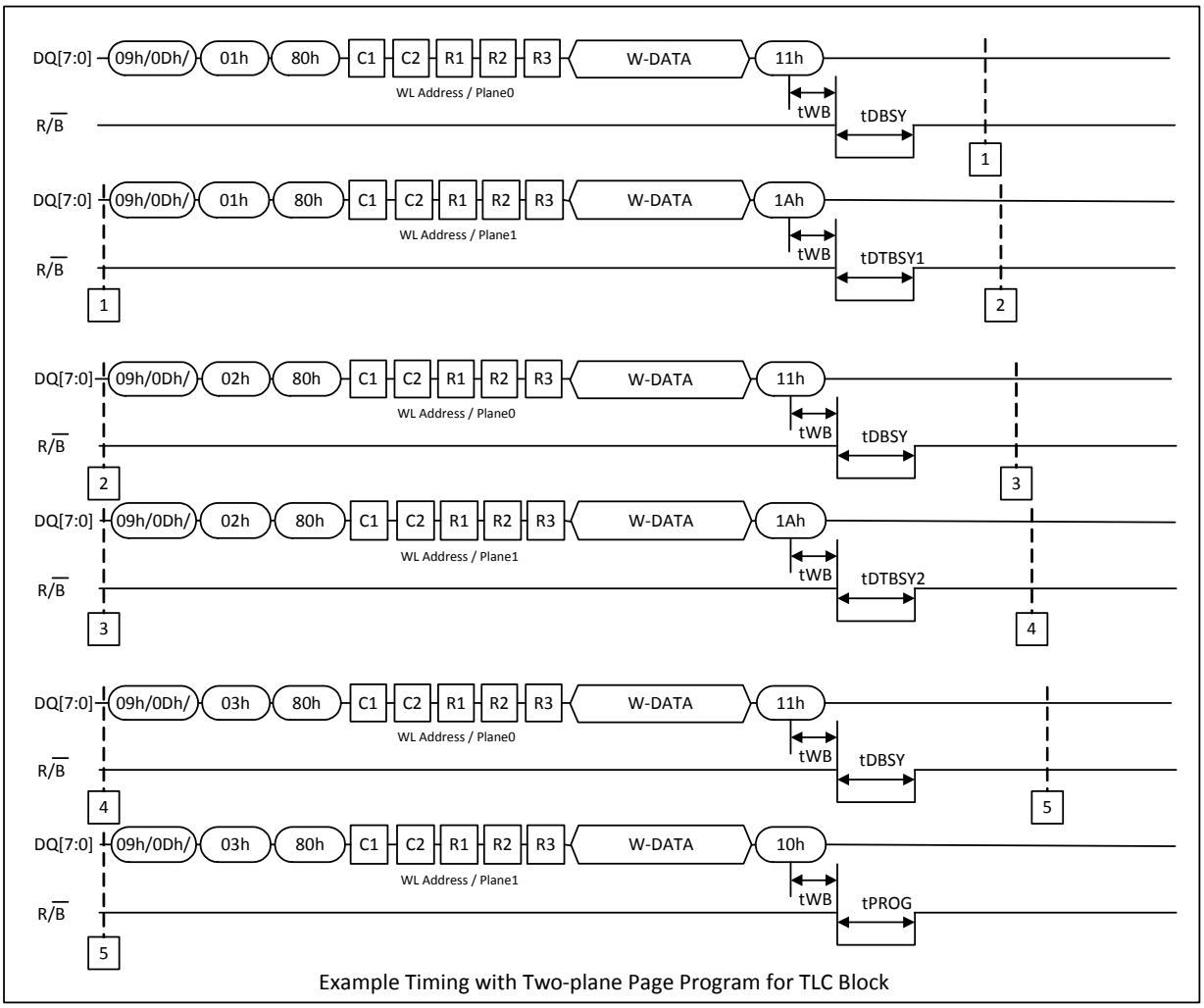
Two-Plane Page Program function extends an effective programmable page size using two planes.
When a host moves on a plane for loading another data, command 11h for the second command is used. After 11h command, R/B returns high (i.e. ready) in a short period of time since it is not actual programing operation. At the last page loading, command 80h is issued before loading data and command 10h after data loading is issued for the second command. After command 10h, all loaded data in each plane starts to be programmed to Flash array simultaneously.

Figures of "*Example Timing with Two-plane Page Program for SLC Block*" and "*Example Timing with Two-plane Page Program for TLC Block*" defines Two-Plane Page Program behavior and timings.

Figure 5-24. Example Timing with Two-plane Page Program for SLC Block



igure 5-25. Example Timing with Two-plane Page Program for TLC Block



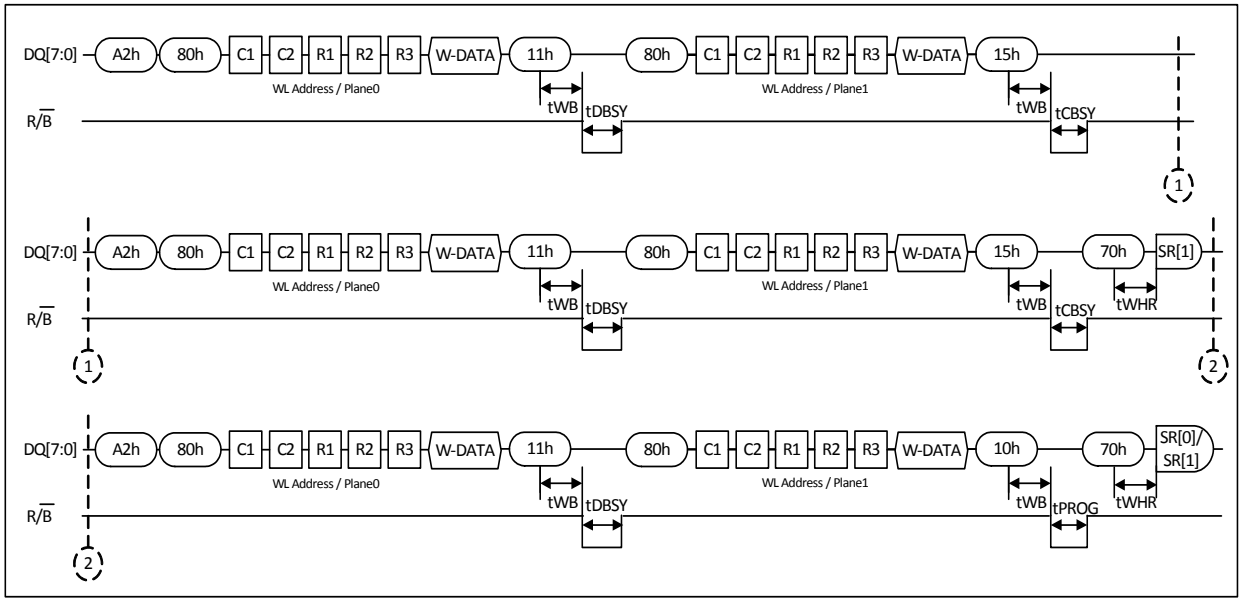
Example Timing with Two-plane Page Program for TLC Block

5.3.5. Two-Plane Cache Program Operation (only available for SLC mode)

The Two-Plane Cache Program is an extension of the Cache Program. After loading pages into planes for Two-Plane Cache Program, command 15h is issued. After command 15h, R/B# returns high once transferring data from cache register to page register is completed. Internal program operation is in progress after R/B# returns while other pages are loaded by a host. At the last page loading for the entire Two-Plane Cache Program, command 10h is required to finalize the operation and R/B# stays busy as long as tPROG.

Figures of "*Example Timing with Two-plane Cache Program*" defines Two-Plane Cache Page Program behavior and timings.

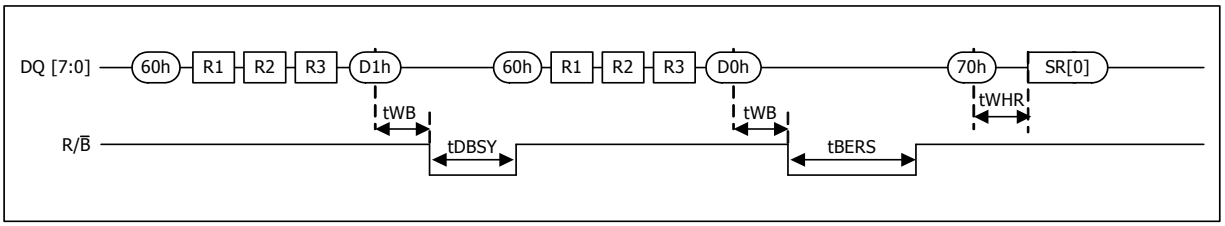
Figure 5-26. Example Timing with Two-plane Cache Page Program



5.2.6. Two-Plane Block Erase Operation

Two-Plane Block Erase allows users to erase multiple blocks comprising a block of each plane simultaneously. Figure of "*Example Timing with Two-plane Block Erase*" defines Two-Plane Block Erase behavior and timings.

Figure 5-27. Example Timing with Two-plane Block Erase

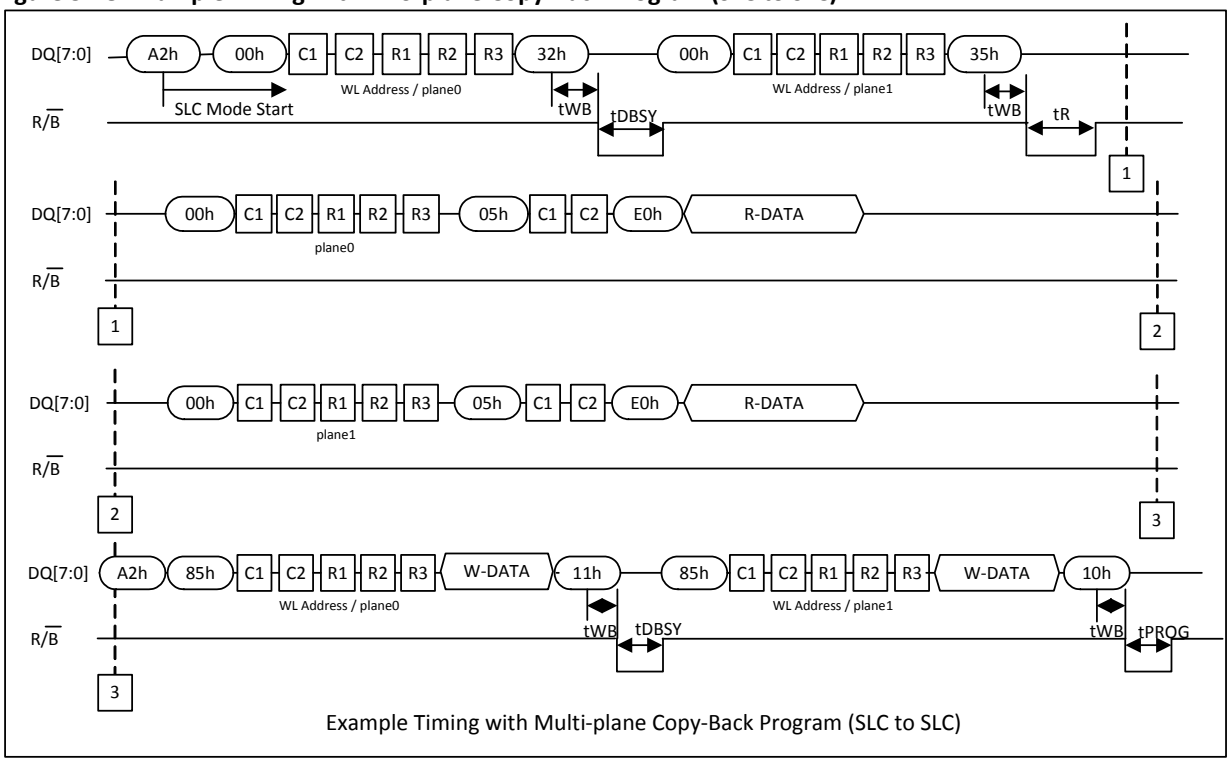


5.2.7. Two-Plane Copy-Back Program Operation

The Two-Plane Copy-Back Program is an extension of the Copy-back Program. Two-Plane Copy-Back Program operation is executed two sets of commands, Two-Plane Read for Copy-Back and Two-Plane Copy-Back Program.

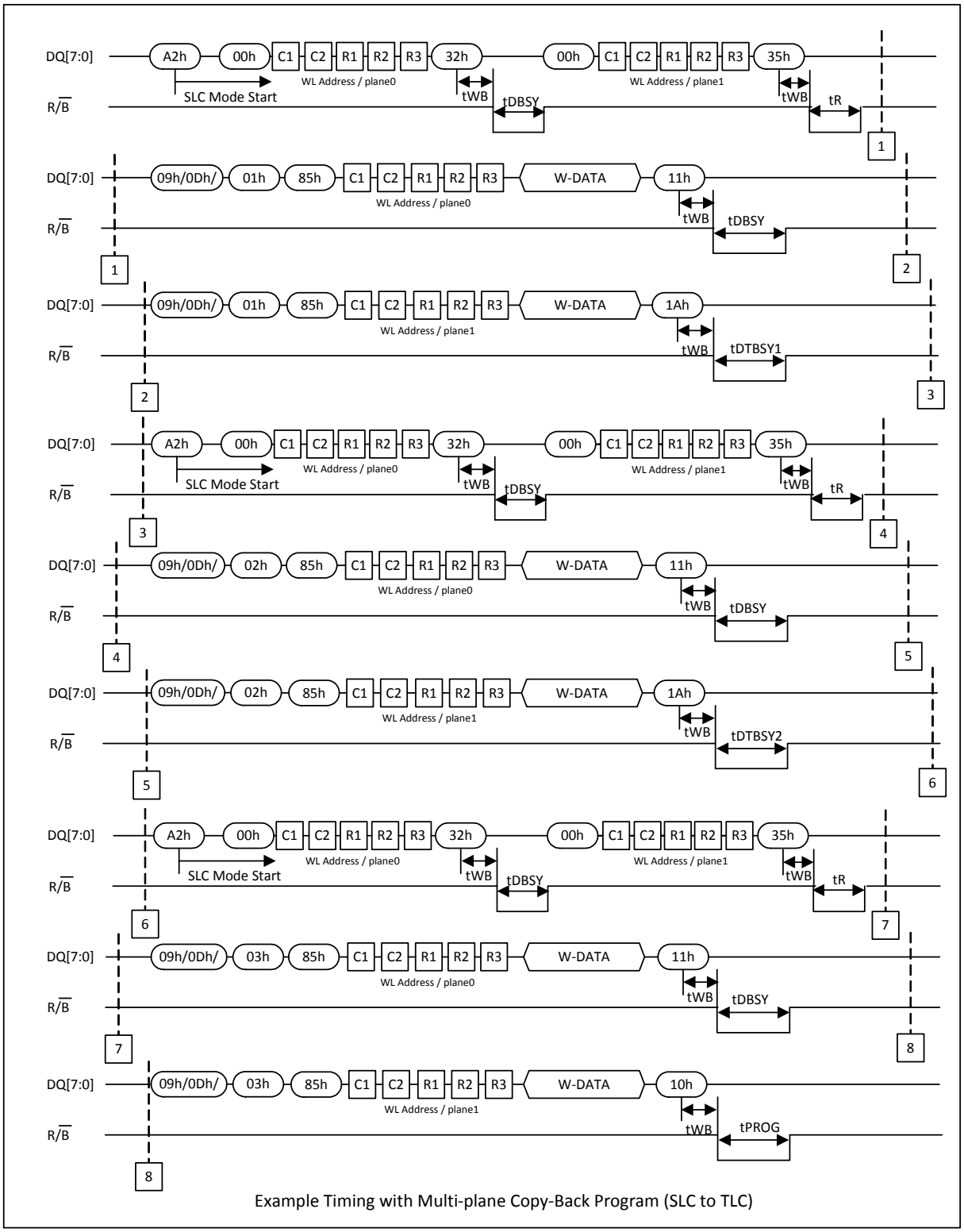
Figure of "*Example Timing with Two-plane Copy-Back Program (SLC to SLC)*" defines Two-Plane Copy-Back Program behavior and timings.

Figure 5-28. Example Timing with Two-plane Copy-Back Program (SLC to SLC)



Example Timing with Multi-plane Copy-Back Program (SLC to SLC)

Figure 5-29. Example Timing with Two-plane Copy-Back Program (SLC to TLC)



Example Timing with Multi-plane Copy-Back Program (SLC to TLC)

5.2.8. Read Status Enhanced

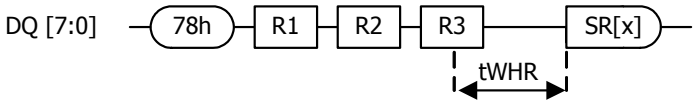
Read Status Enhanced function is used to check status of selected plane of a LUN. Thus, the function requires row address setting steps before reading status value. Table of "*Read Status Enhanced Definition*" defines status values of each operation and Figure of "*Read Status Sequence*" defines Read Status Enhanced behavior and timings.

Table 5-14. Read Status Enhanced Definition

	DQ0	DQ1	DQ2	DQ3	DQ4	DQ5	DQ6	DQ7
Definition of value	Pass : "0" Fail : "1"	Pass : "0" Fail : "1"	Reserved	Reserved	Reserved	Busy : "0" Ready : "1"	Busy : "0" Ready : "1"	Protected : "0" Not Protected : "1"
Block Erase	Pass/Fail	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready	Write Protect
Page Program	Pass/Fail	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready	Write Protect
Cache Program	Pass/Fail for the current page	Pass/Fail for the previous page	Not Use	Not Use	Not Use	Busy/Ready for Flash array	Busy/Ready for Host	Write Protect
Read	Not Use	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready	Write Protect
Cache Read	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready for Flash array	Busy/Ready for Host	Write Protect

Note:
1) During Block Erase, Page Program, DQ0 is only valid when DQ6 shows the Ready state.
2) During Cache Program operation, DQ0 is only valid when DQ5 shows the Ready state, and DQ1 is only valid when DQ6 shows the Ready state.

Figure 5-30. Read Status Sequence



5.2.9. Read LUN Status Operation

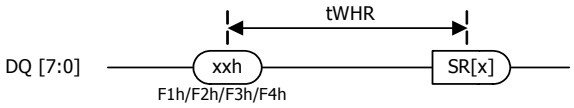
Read LUN Status provides status value of LUN without address setting. The function retrieves plane0 and plane1 status only. Table for "*Read LUN Status Definition*" defines the status values and Figure of "*Read LUN Status Timing*" defines Read LUN Status behavior and timings.

Table 5-15. Read LUN Status Definition

	DQ0	DQ1	DQ2	DQ3	DQ4	DQ5	DQ6	DQ7
Definition of value	Pass : "0" Fail : "1"	Pass : "0" Fail : "1"	Pass : "0" Fail : "1"	Pass : "0" Fail : "1"	Pass : "0" Fail : "1"	Busy : "0" Ready : "1"	Busy : "0" Ready : "1"	Protected : "0" Not Protected : "1"
Block Erase	Pass/Fail for LUN#N	Pass/Fail for Plane#0	Pass/Fail for Plane#1	Not Use	Not Use	Not Use	Busy/Ready	Write Protect
Page Program	Pass/Fail for LUN#N	Pass/Fail for Plane#0	Pass/Fail for Plane#1	Not Use	Not Use	Not Use	Busy/Ready	Write Protect
Cache Program	Pass/Fail for LUN#N	Pass/Fail for Plane#0(N)	Pass/Fail for Plane#1(N)	Pass/Fail for Plane#0(N-1)	Pass/Fail for Plane#1(N-1)	Not Use	Busy/Ready	Write Protect
Read	Not Use	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready	Write Protect

	DQ0	DQ1	DQ2	DQ3	DQ4	DQ5	DQ6	DQ7
Cache Read	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready for Flash array	Busy/Ready for Host	Write Protect

Figure 5-31. Read LUN Status Timing

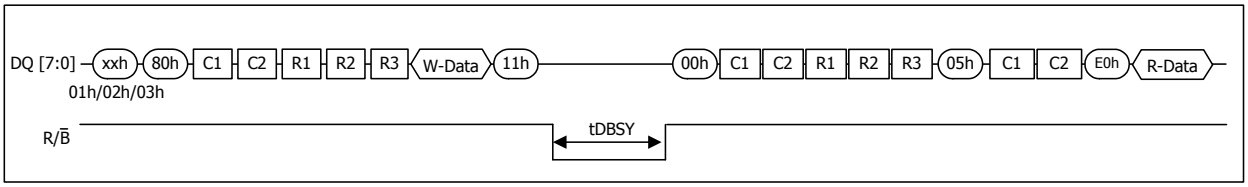


Note:
1) F1h and F2h could be used in DDP per CE.
2) F1h, F2h, F3h and F4h could be used in QDP per CE

5.2.13. Register Read Out Mode 1

At program operation, loaded data to the register can be read out before program confirm command(10h). The sequence is as follows. To continue program operation after reading data, Copy-back Program operatiion (i.e. 85h- Address(5cycle) - Data - 10h) is required.

Figure 5-33. Register Read Out

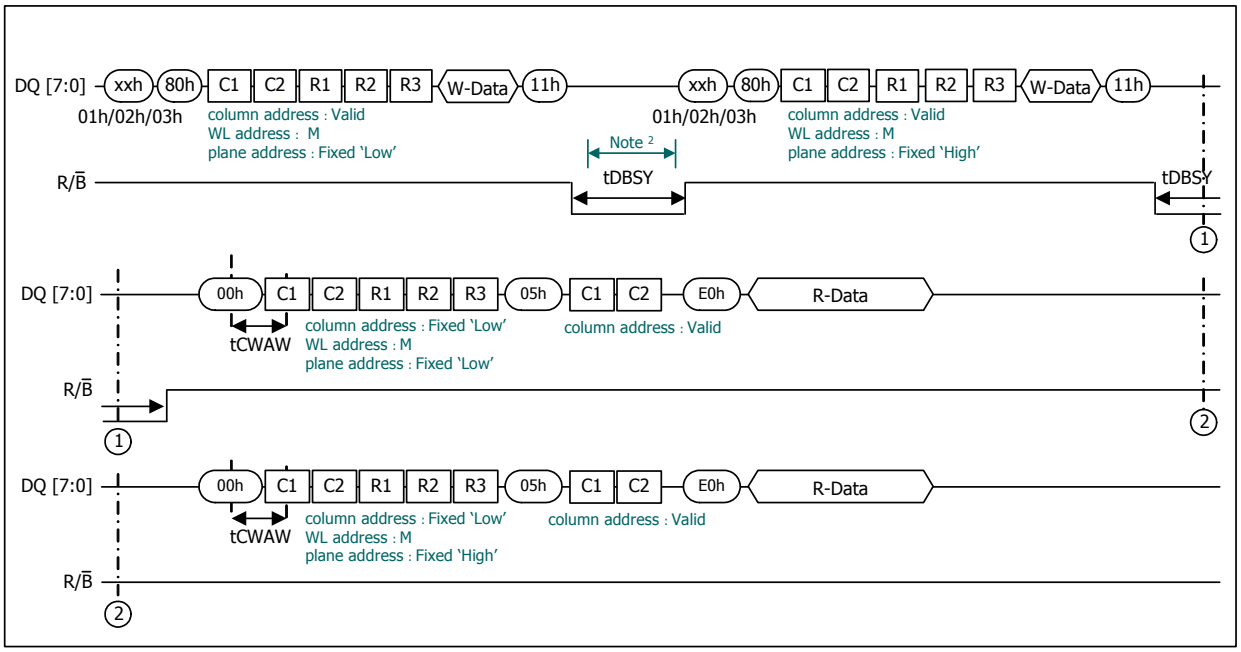


NOTE :
Register read out operation is prohibited during cache program operation.

5.2.14. Two-Plane Register Read Out Mode 1

At Two-Plane program operation, loaded data to the register can be read out before program confirm command(10h). The sequence is as follows.To continue Two-Plane program operation after reading data, Two-Plane Random Data Copy-back Program sequence is required.

Figure 5-35. Two-Plane Register Read Out Mode 1



NOTE :
1) Any command between 11h and 81h is prohibited except 70h/78h/F1h and FFh.
2) Register read out operation is prohibited during cache program operation.

5.3. Interleaving Operation

When multiple LUNs share a common CE, it provides interleaving operation between LUNs.

At first, the host issues a operation command to one of the LSB chips, say (LUN #0). Due to DDP device goes into busy state. During this time, MSB chip (LUN #1) is in ready state. So it can execute the operation command issued by the host.

After the execution of operation by LSB chip (LUN #0), it can execute another operation regardless of MSB chip (LUN #1). Before that the host needs to check the status of LSB chip (LUN #0) by issuing 78h/F1h command. Only when the status of LSB chip (LUN #0) becomes ready status, host can issue another operation command. If LSB chip (LUN #0) is in busy state, the host has to wait for LSB chip (LUN #0) to get into ready state.

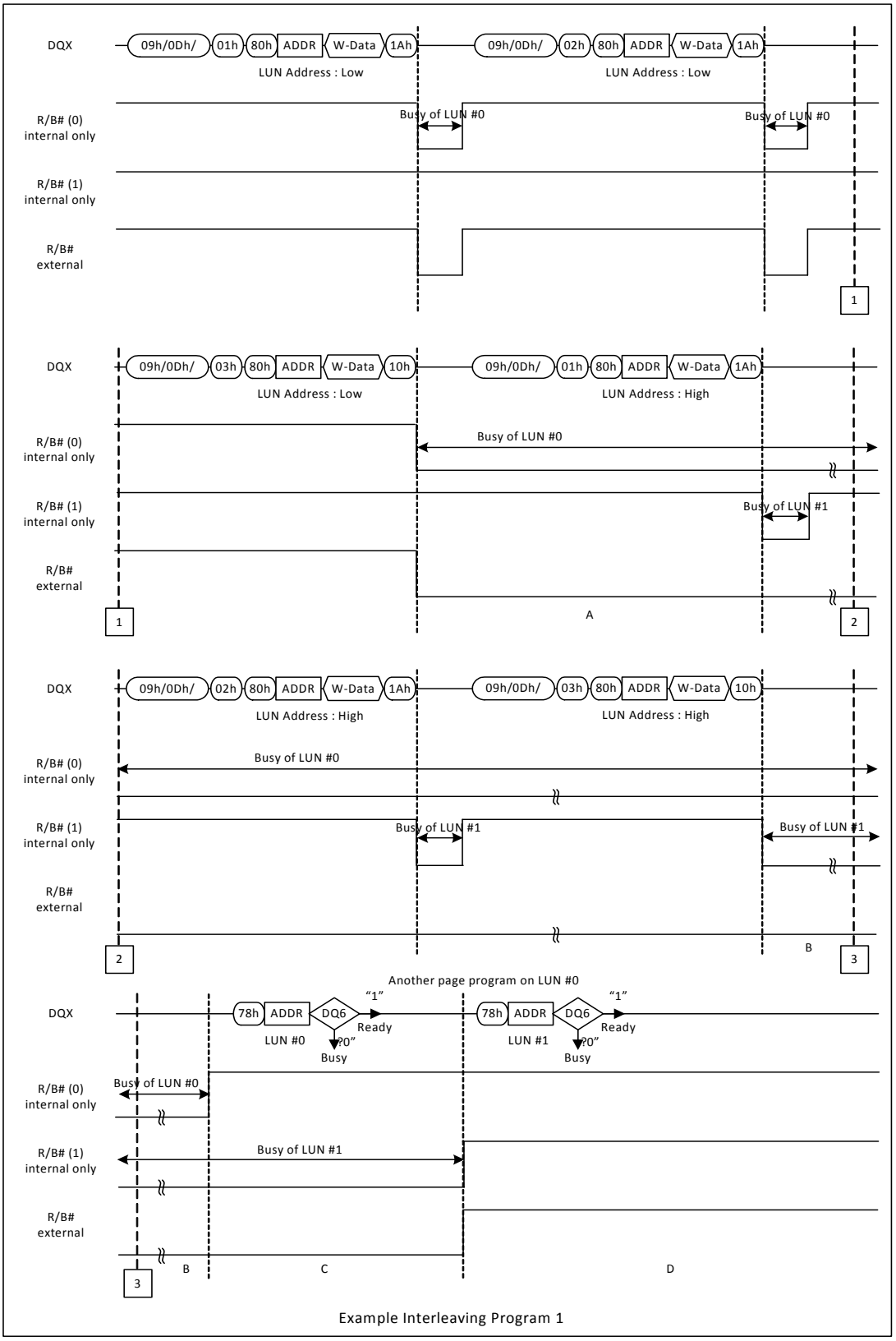
Similarly, MSB chip (LUN #1) can execute another operation after the completion of the previous operation. The host can monitor the status of MSB chip (LUN #1) by issuing 78h/F2h command. When MSB chip (LUN #1) goes ready state, host can issue another operation command to MSB chip (LUN #1).

This interleaving operation helps the system improve the system throughput.

NOTE :
During interleave operations, 70h command is prohibited.

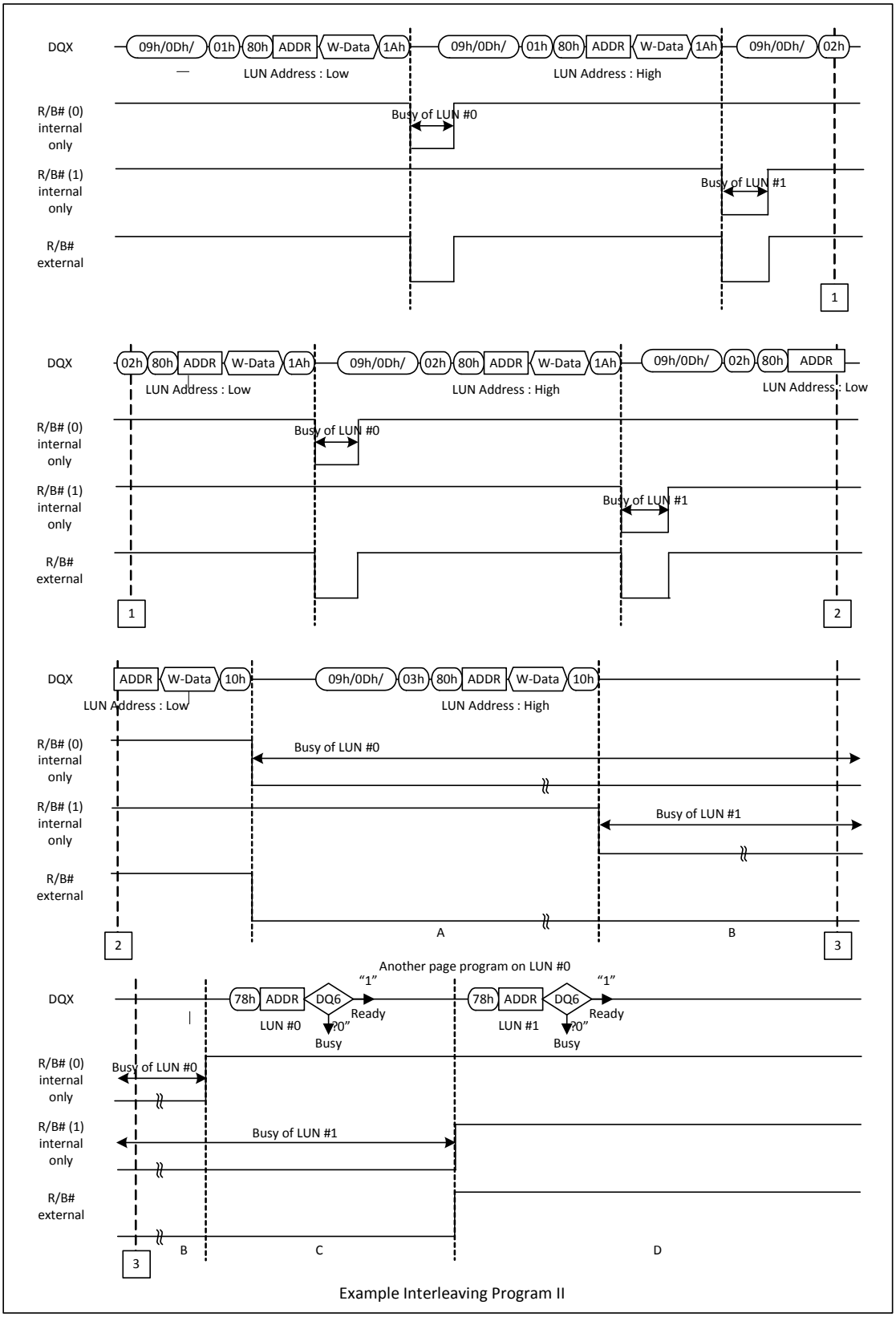
5.3.1. Interleaving Page Program

Figure 5-34. Interleaving Page Program I



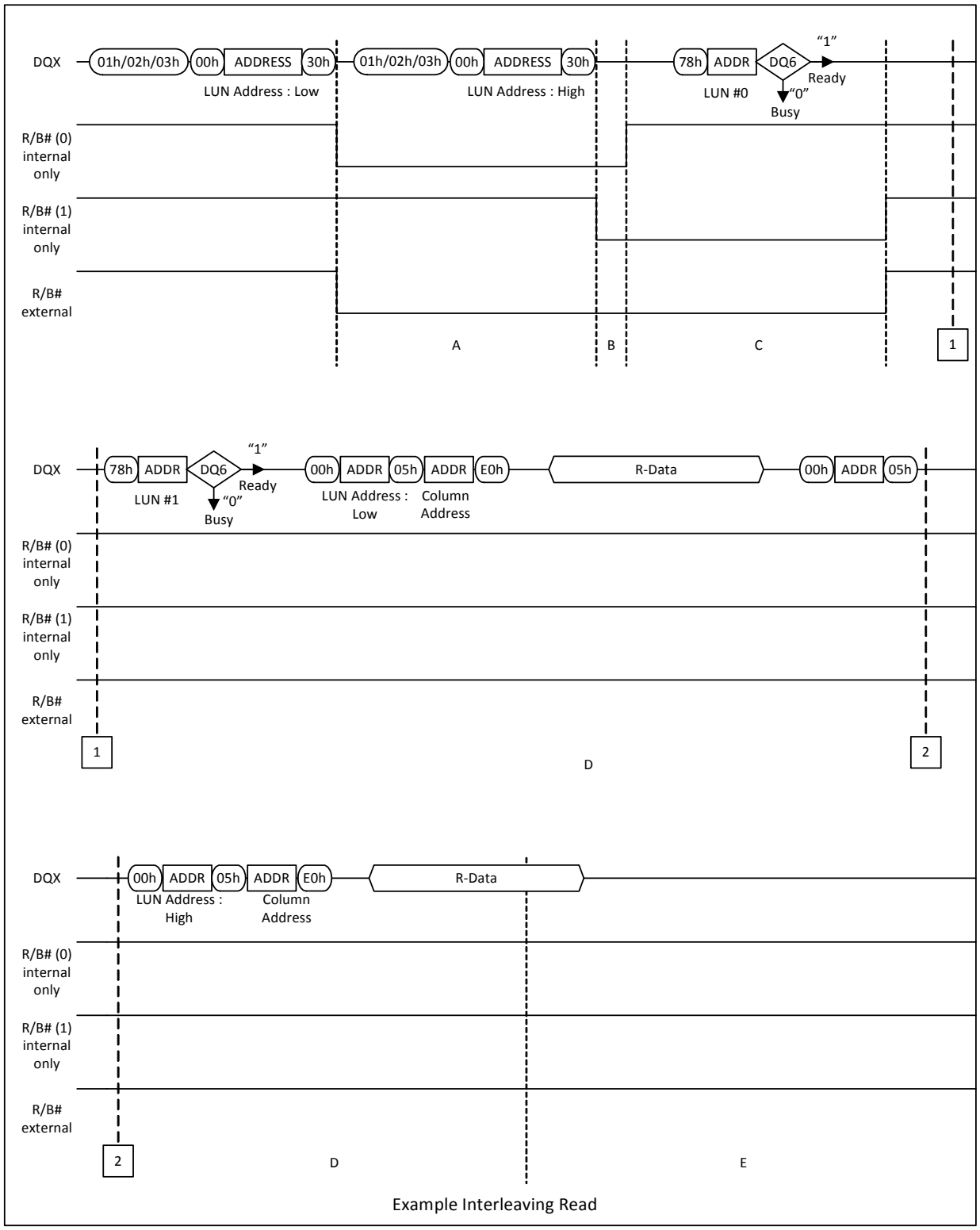
Example Interleaving Program 1

Figure 5-35. Interleaving Page Program II



5.3.2. Interleaving Page Read

Figure 5-36. Interleaving Page Read

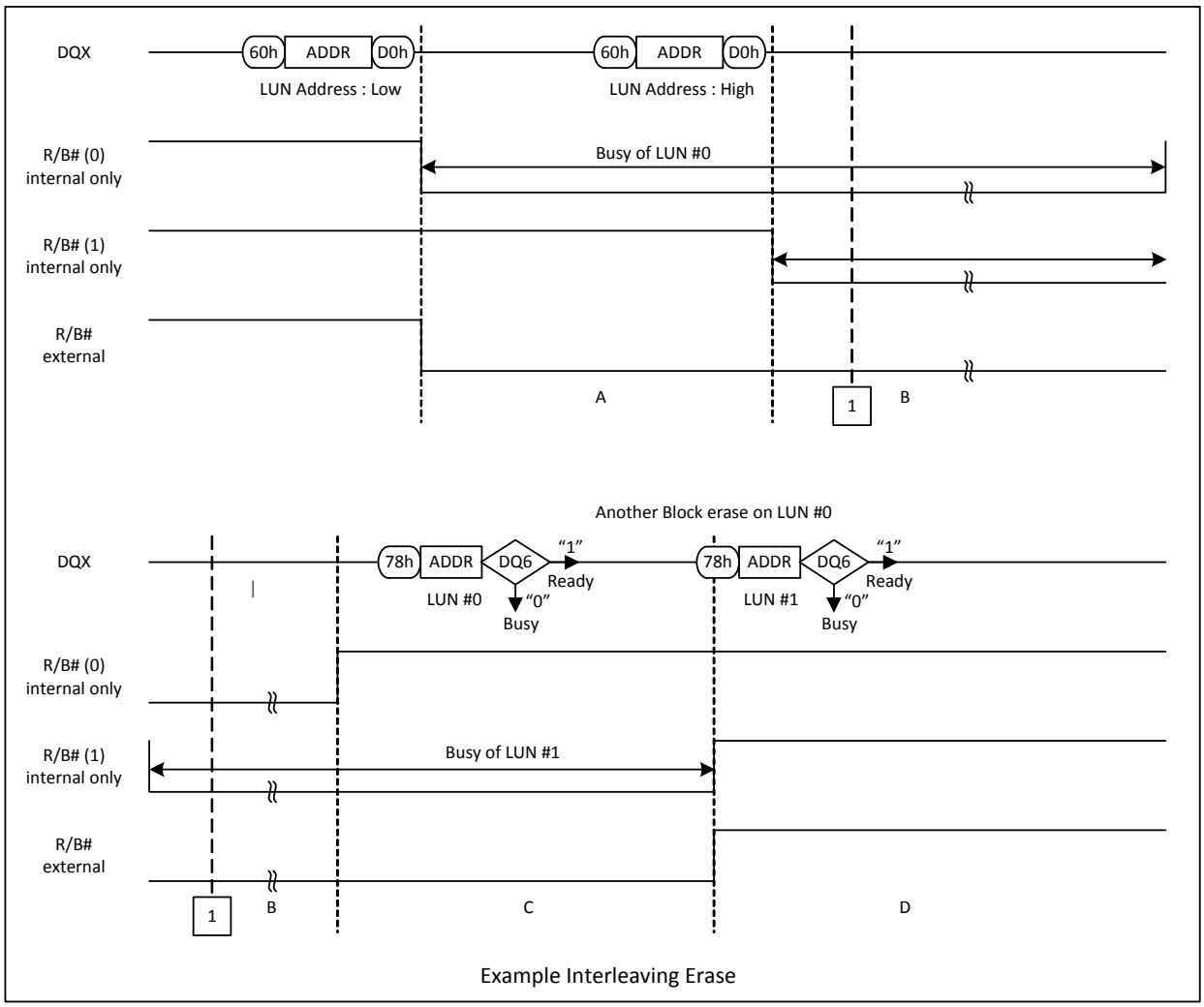


Example Interleaving Read

State A : LUN #0 is executing page read operation, and LUN #1 is in ready state.
So the host can issue page read command to LUN #1.
State B : Both LUN #0 and LUN #1 are executing page read operation.
State C : Page read on LUN #0 is completed and LUN #1 is still executing page read operation.
State D : Before the host read the data, the host should check the Ready/Busy status for both LUNs by 78h commands.
State E : LUN #0 and LUN #1 are ready.

5.3.3. Interleaving Block Erase

Figure 5-37. Interleaving Block Erase

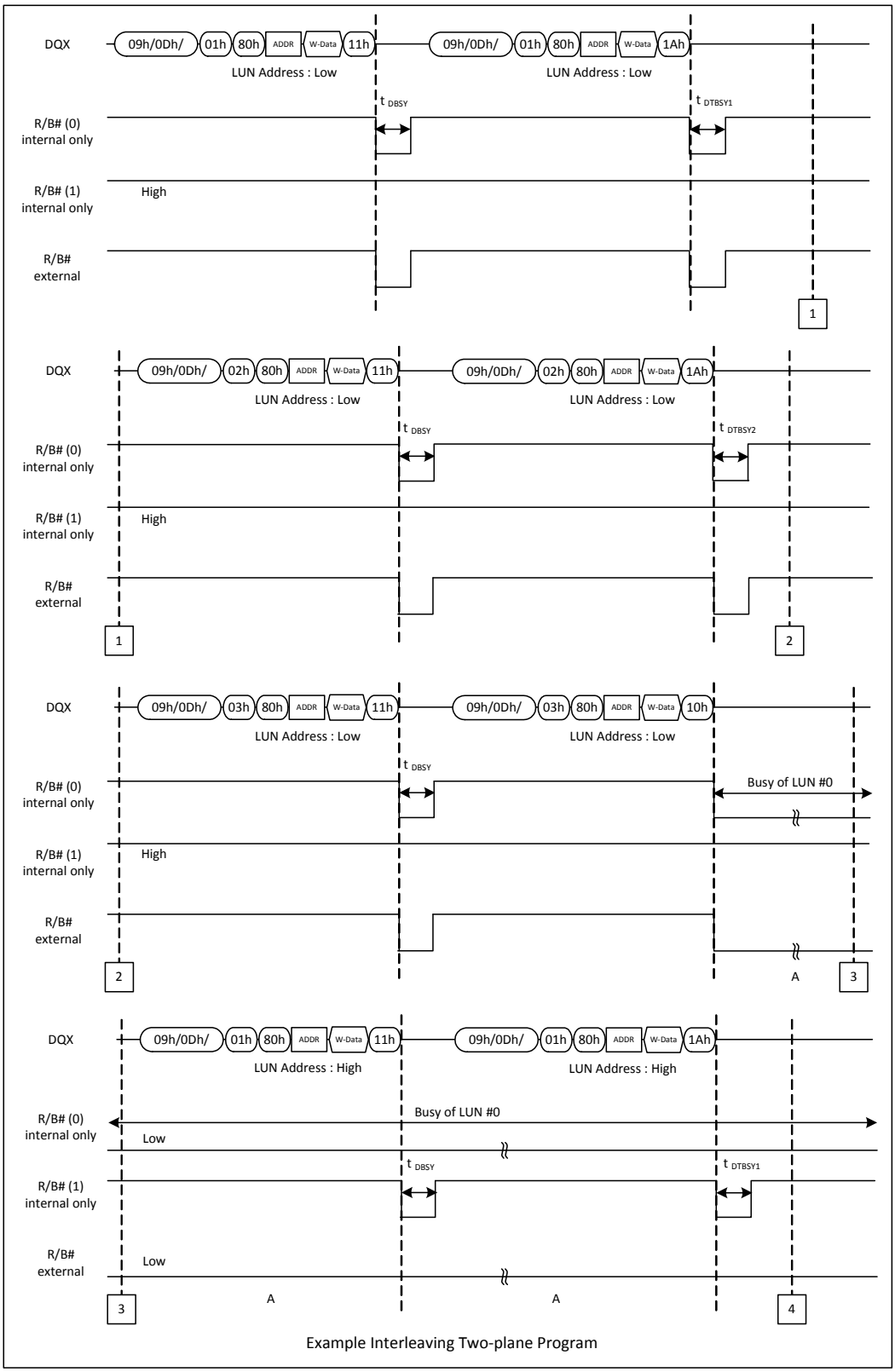


Example Interleaving Erase

State A : LUN #0 is executing block erase operation, and LUN #1 is in ready state.
So the host can issue block erase command to LUN #1.
State B : Both LUN #0 and LUN #1 are executing block erase operation.
State C : Block erase on LUN #0 is terminated, but block erase on LUN #1 is still operating. And the system should issue F1h command to detect the status of LUN #0.
If LUN #0 is ready, status I/O6 is "1" and the system can issue another block erase command to LUN #0.
State D : LUN #0 and LUN #1 are ready.

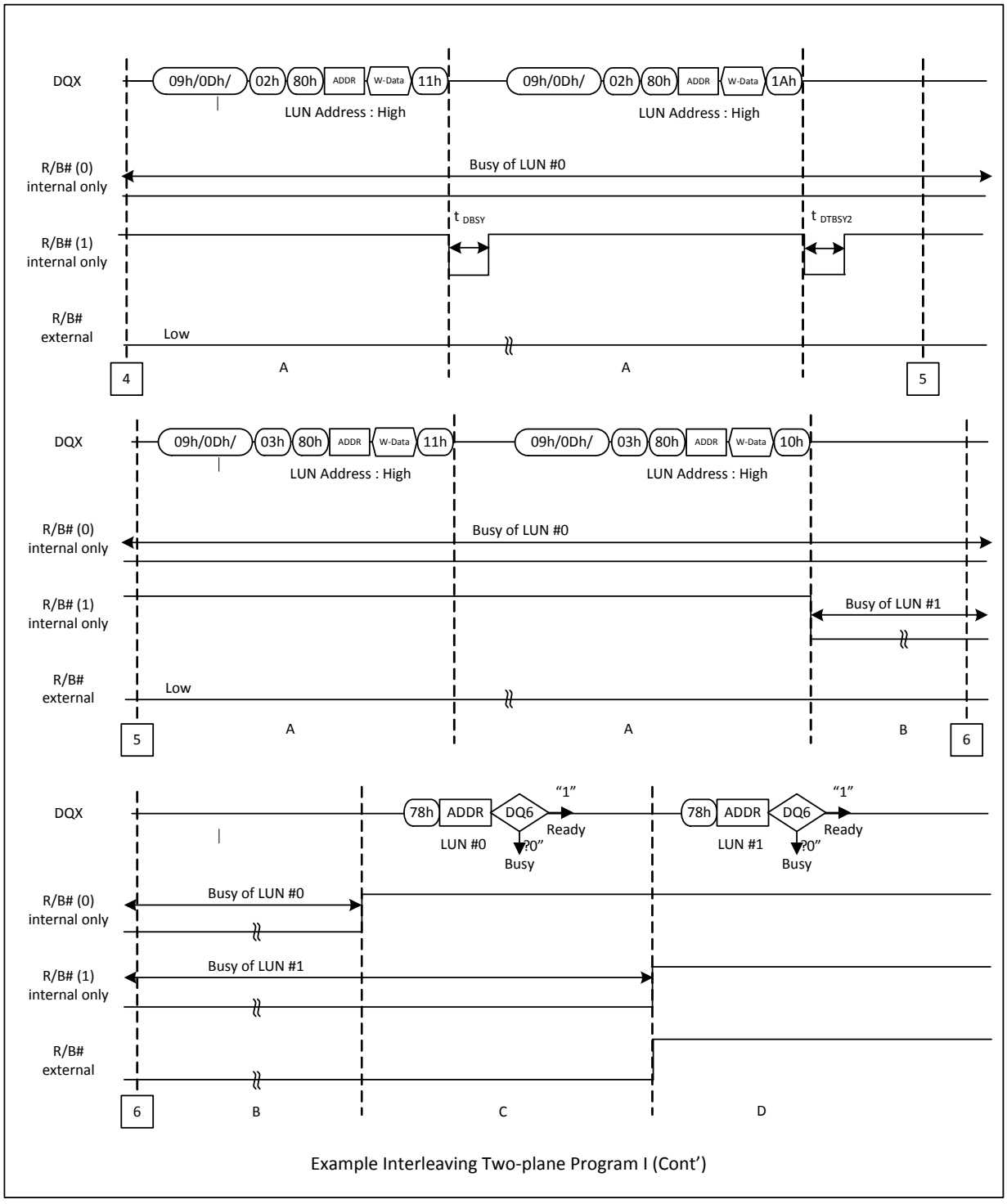
5.3.4. Interleaving Two-Plane Page Program

Figure 5-38. Interleaving Two-Plane Page Program I



Example Interleaving Two-plane Program

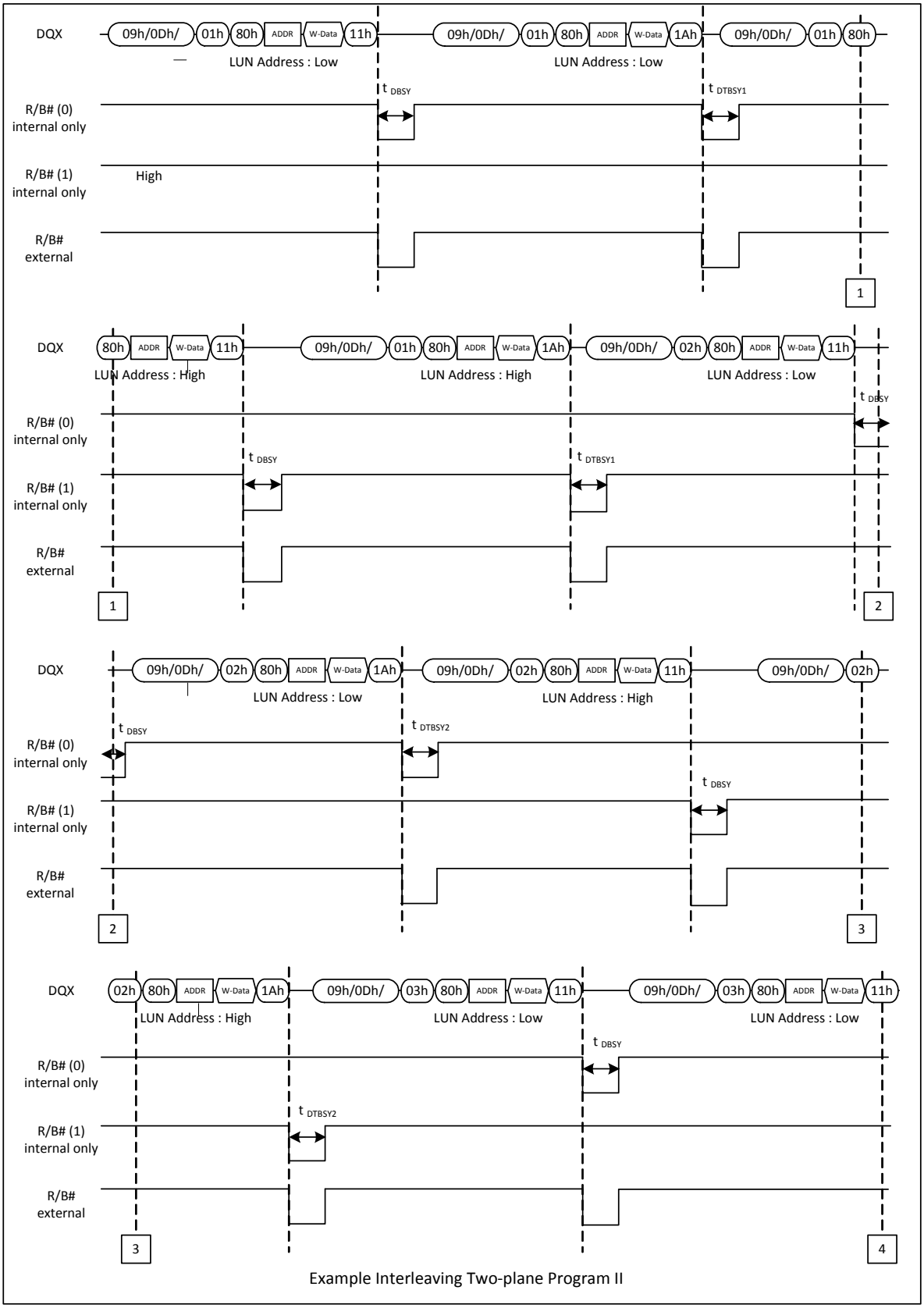
Figure 5-39. Interleaving Two-Plane Page Program I (cont')



Example Interleaving Two-plane Program I (Cont')

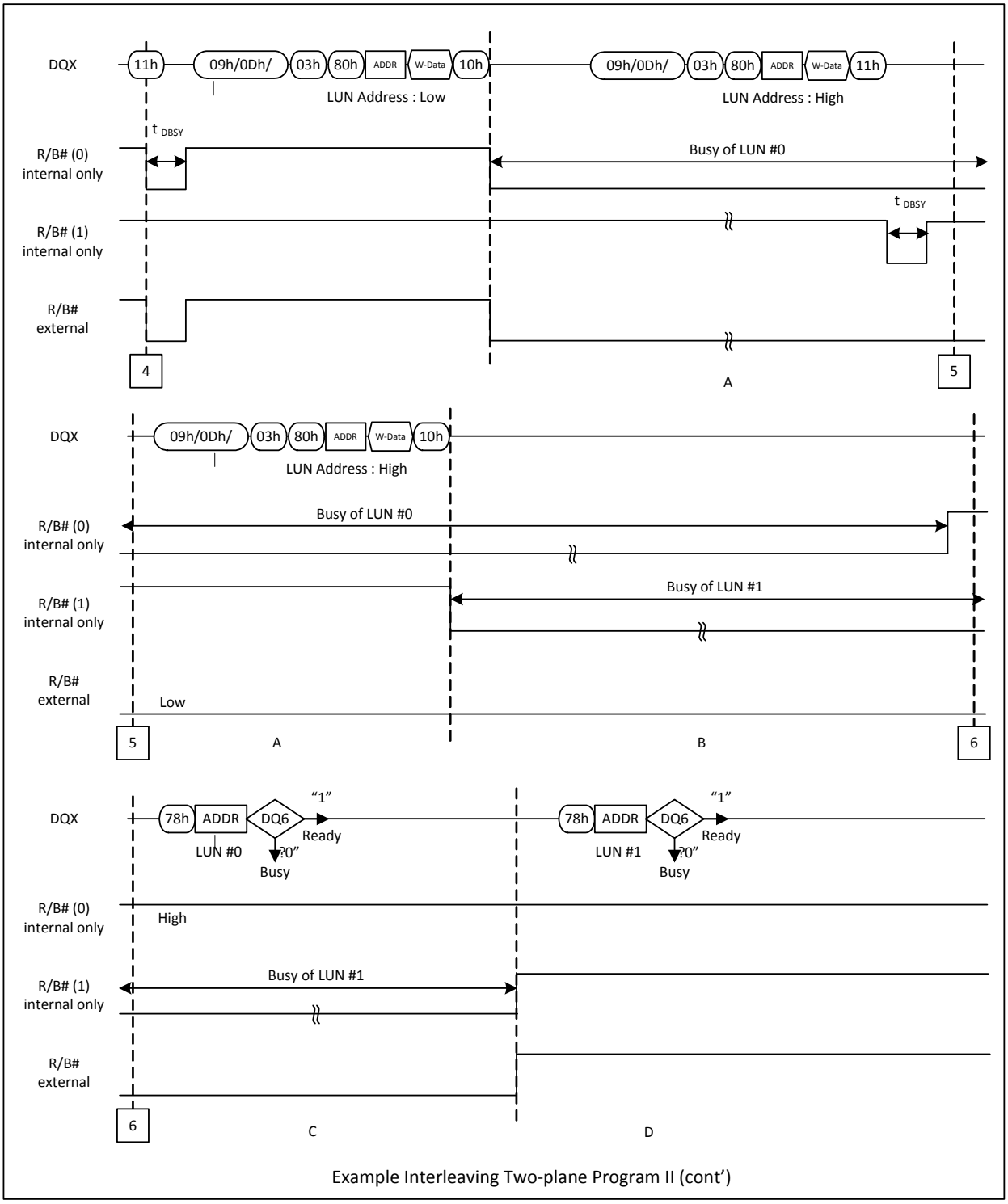
State A : LUN #0 is executing Two-plane page program operation, and LUN #1 is in ready state.
So the host can issue Two-plane page program command to LUN #1.
State B : Both LUN #0 and LUN #1 are executing Two-plane page program operation.
State C : Two-plane page program on LUN #0 is completed and LUN #0 is ready for the next operation. LUN #1 is still executing Two-plane page program operation.
State D : LUN #0 and LUN #1 are ready.

Figure 5-40. Interleaving Two-Plane Page Program II



Example Interleaving Two-plane Program II

Figure 5-41. Interleaving Two-Plane Page Program II (cont')



Example Interleaving Two-plane Program II (cont')

5.4. Ready/$\overline{\text{Busy}}$

The device has a R/$\overline{\text{B}}$ output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/$\overline{\text{B}}$ pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/$\overline{\text{B}}$ outputs to be Or-tied. Because pull-up resistor value is related to tr(R/$\overline{\text{B}}$) and current drain during busy(ibusy) , an appropriate value can be obtained with the following reference chart. Its value can be determined by the following guidance.

Figure 5-42. Rp vs tr ,tf & Rp vs ibusy

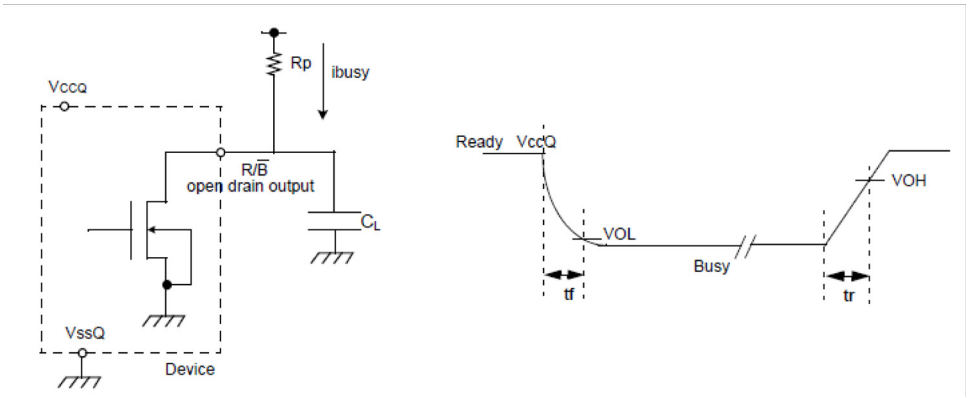
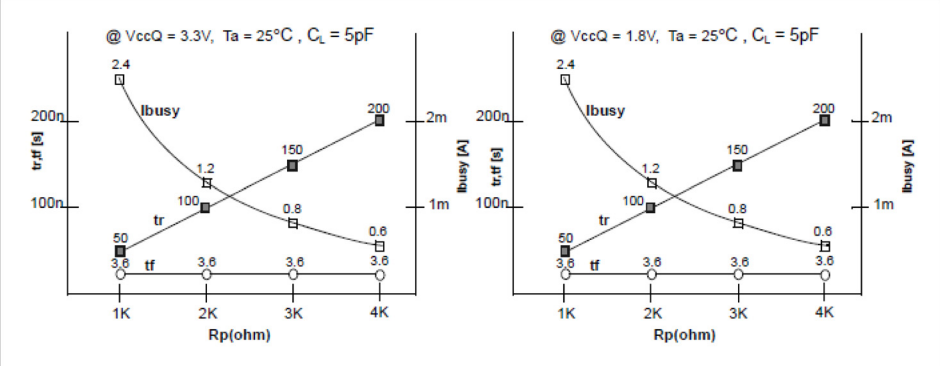


Figure 5-43. Rp value guidance



$$\text{Rp(min, 3.3V part)} = \frac{\text{Vcc(Max.)} - \text{VoL(Max.)}}{\text{IoL} + \Sigma\text{IL}} = \frac{3.2\text{V}}{8\text{mA} + \Sigma\text{IL}} \qquad \text{Rp(min, 1.8V part)} = \frac{\text{Vcc(Max.)} - \text{VoL(Max.)}}{\text{IoL} + \Sigma\text{IL}} = \frac{1.85\text{V}}{3\text{mA} + \Sigma\text{IL}}$$

where IL is the sum of the input currents of all devices tied to the R/$\overline{\text{B}}$ pin.
Rp(max) is determined by maximum permissible limit of tr

128Gb (3bit/cell) Based NAND Flash

Legacy Async. SDR Specification

H27UDG8M2MTR-BC

Legacy TSOP

Key features

■ **x3 Cell technology**

■ **NAND INTERFACE**
- x8 bus width

■ **Supply Voltage**
- Vcc : 2.7V ~ 3.6V

■ Organization
- (16,384+2,048)bytes x 258pages x (2,048 + 60)blocks x 2plane
- Page size : 16,384+2,048bytes
- Block size : 258pages x (16,384+2,048) bytes
- Pages per block: 258pages (86WL x 3bit)
- 2-Plane size : (4,096blocks + 120 Extended block)

■ **Page Read / Program Time**
- Random Read Time(tR) : 100 us
- Sequential Access (tRC/tWC) : 16ns(Min.)
(Read/Write throughput per pin : up to 62.5MHz)
- Page Program Time : 2.2 ms

■ **Block Erase**
- Block Erase Time : 5 ms (Typ)

■ **Operating Current**
- Page Read : 50 mA (max)
- Page Program : 50 mA (max)
- Block Erase: 50 mA (max)
- Standby (CMOS): 50uA (max)

■ **Hardware Data Protection**
- Program/Erase locked during power transitions

■ **Package**
- T-SOP :Size : 12x20mm
- Pin count : 48
- 128Gbit: single die stack, H27UDG8M2MTR-BC

1. Summary Description

The product part No. H27UDG8M2MTR-BC is a 3.3V 64Gbit NAND flash memory. The Device contains 2 planes in a single die. Each plane is made up of the 4,096 blocks. Each block consists of 256 programmable pages. Each page contains 16,384 data bytes + 2,048 spare bytes. The pages are subdivided into an 16,384 byte main data storage area with a spare 2,048 byte district. Page program operation can be performed in typical 2.2ms, and a single block can be erased in typical 5ms.

1. 1. Product List

Table1-1. List of supported versions / packages

Product information				
P/N	**Density**	**Vcc**	**Operating range**	**PACKAGE**
H27UDG8M2MTR-BC	128Gb	3.3V	2.7 to 3.6V	48pin TSOP

1.2. PIN DESCRIPTION

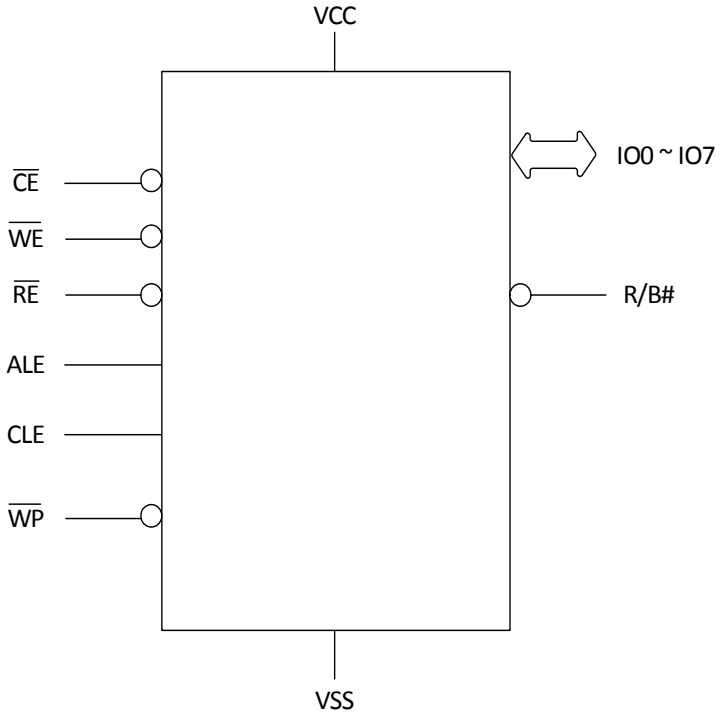
Table 1-2. Signal description

Pin Name	Type	Description
I/O 0 - I/O 7	Input	**DATA INPUTS/OUTPUTS** The I/O pins is used to COMMAND LATCH cycle, ADDRESS INPUT cycle, and DATA in-out cycles during read / write operations. The I/O pins float to High-Z when the device is deselected or the outputs are disabled.
CLE	Input	**COMMAND LATCH ENABLE** This input activates the latching of the I/O inputs inside the Command Register on the Rising edge of Write Enable ($\overline{WE}$).
ALE	Input	**ADDRESS LATCH ENABLE** This input activates the latching of the I/O inputs inside the Address Register on the Rising edge of Write Enable ($\overline{WE}$).
$\overline{CE}$	Input	**CHIP ENABLE** This input controls the selection of the device. When the device is busy, $\overline{CE}$ low does not deselect the memory. The device goes into Stand-by mode when $\overline{CE}$ goes High during the device is in Ready state. The $\overline{CE}$ signal is ignored when device is in Busy state, and will not enter Standby mode even if the $\overline{CE}$ goes high.
$\overline{WE}$	Input	**WRITE ENABLE** This input acts as clock to latch Command, Address and Data. The I/O inputs are latched on the rise edge of $\overline{WE}$.
$\overline{RE}$	Input	**READ ENABLE** The $\overline{RE}$ input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid t_{REA} after the falling edge of $\overline{RE}$ which also increments the internal column address counter by one.
$\overline{WP}$	Input	**WRITE PROTECT** The $\overline{WP}$ pin, when Low, provides a hardware protection against undesired write operations. Hardware Write Protection is activated when the Write Protect pin is low. In this condition modify operation do not start and the content of the memory is not altered. Write Protect pin is not latched by Write Enable to ensure the protection even during the power up phases.
R/$\overline{B}$	Output	**READY / BUSY** The Ready/Busy output is an Open Drain pin that signals the state of the memory.
VCC	Supply	**POWER SUPPLY VOLTAGE PIN** The VCC supplies the power for all the operations. (Read, Write, and Erase).
VSS	Supply	**GROUND CONNECTION PIN**
NC		**NO CONNECTED**

NOTE:
A 0.1uF capacitor be connected between the Vcc (Supply Voltage) pin and the Vss (Ground) pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.

1.3. Pin Diagram

Figure 1-1. Pin diagram



1.4. Pin Assignments

Figure 1-2. 48-pin TSOP

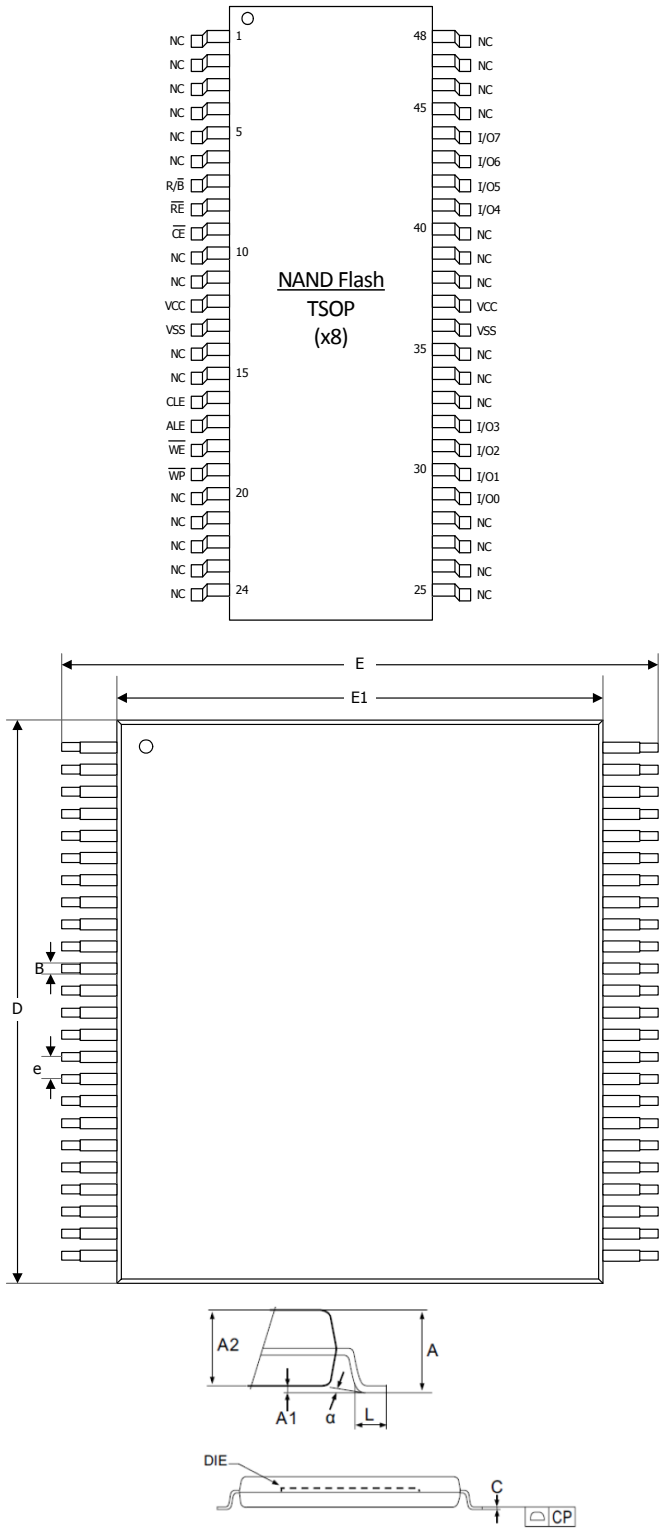


Table 1-3. 48-pin TSOP, Package Mechanical Data

Symbol	Milimeters			Symbol	Milimeters		
	Min	Typ	Max		Min	Typ	Max
A	-	-	1.200	D	11.91	12.00	12.12
A1	0.050	-	0.150	E	19.90	20.00	20.10
A2	0.980	-	1.030	E1	18.30	18.40	18.50
B	0.170	-	0.250	e	-	0.500	-
C	0.100	-	0.200	L	0.50	-	0.68
Symbol	**Milimeters**			**Symbol**	**Milimeters**		
	Min	**Typ**	**Max**		**Min**	**Typ**	**Max**
alpha	0	-	5	CP	-	-	0.10

1.5. Command Set

Table 1-4. Command Set table

	1st CYCLE	Number of Address cycles	Data Input cycles	2nd CYCLE	Number of Address cycles	Data Input cycles	3rd CYCLE	Acceptable command during busy
1st Program for 1st Coarse[7)]	09h	-	-	-	-	-	-	No
2nd Program for 2nd Coarse[7)]	0Dh	-	-	-	-	-	-	No
3rd Program for Fine[7)]	-	-	-	-	-	-	-	No
LSB Page	01h	-	-	-	-	-	-	No
CSB Page	02h	-	-	-	-	-	-	No
MSB Page	03h	-	-	-	-	-	-	No
PAGE READ	00h	5	-	30h	-	-	-	No
READ FOR COPY-BACK	00h	5	-	35h	-	-	-	No
RANDOM DATA OUTPUT [1)]	05h	2	-	E0h	-	-	-	No
SINGLE/MULTI-PLANE CACHE READ [5)]	31h	-	-	-	-	-	-	No
SINGLE/MULTI-PLANE CACHE READ END [5)]	3Fh	-	-	-	-	-	-	No
READ ID	90h	1	-	-	-	-	-	No
READ STATUS REGISTER	70h	-	-	-	-	-	-	Yes
PAGE PGM (start)/ CACHE PGM [5)] (end)	80h	5	Yes	10h	-	-	-	No
RANDOM DATA INPUT[1)]	85h	2	Yes	-	-	-	-	No
COPY-BACK PGM	85h	5	Option	10h	-	-	-	No
CACHE PGM (start)[5)]	80h	5	Yes	15h	-	-	-	No

	1st CYCLE	Number of Address cycles	Data Input cycles	2nd CYCLE	Number of Address cycles	Data Input cycles	3rd CYCLE	Acceptable command during busy
BLOCK ERASE	60h	3	-	D0h	-	-	-	No
RESET	FFh	-	-	-	-	-	-	Yes
MULTI-PLANE PAGE READ	00h	5	-	32h-00h	5	-	30h	No
MULTI-PLANE CACHE READ START [5) 6)]	00h	5	-	32h-00h	5	-	31h	No
MULTI-PLANE READ FOR COPY-BACK	00h	5	-	32h-00h	5	-	35h	No
MULTI-PLANE BLOCK ERASE	60h	3	-	D1h-60h	3	-	D0h	No
MULTI-PLANE RANDOM DATA OUTPUT [1) 3)]	00h	5	-	05h	2	-	E0h	No
MULTI-PLANE READ STATUS REGISTER	78h	3	-	-	-	-	-	Yes
MULTI-PLANE READ STATUS REGISTER (legacy)	75h	-	-	-	-	-	-	Yes
MULTI-PLANE PAGE PGM/ MULTI-PLANE CACHE PGM (end)	80h	5	Yes	11h-80h [2)]	5	Yes	10h	No
MULTI-PLANE COPY-BACK PGM	85h	5	Option	11h-80h [2)]	5	Option	10h	No
MULTI-PLANE CACHE PGM (start) [5)]	80h	5	Yes	11h-80h [2)]	5	Yes	15h	No
CACHE READ ENHANCED	00h	5	-	31h	-	-	-	No

Notes:
1) Random Data Input/Output must be performed in a selected page.
2) Any command between 11h and 80h is prohibited except 70h, 78h, 75h and FFh.
3) Multi-plane Random data-out must be used after multi-plane read operations
(Multi-plane Page Read, Multi-plane Cache Read and Multi-plane Read for Copy Back).
4) Do not change plane address order when using all multi-plane operations.
5) Cache read is available only within a block.
6) It's possible to confirm the multi-plane cache read first step using both 30h and 31h.
7) In case of 1st Program for 1st Coarse / 2nd Program for 2nd Coarse, 09h/0Dh command is needed before the 80h comand (3rd Program for Fine, no command is required).
8) In case of LSB and CSB Page Program operation, 1Ah command is needed after Data In.
In case of MSB Page Program operation, 10h command is needed after Data In.

Caution:
1. Any undefined command inputs are prohibited except for above command set.
2. Multi-plane page read, multi-plane cache read, and multi-plane read for copy-back must be used after multi-plane programmed page, and multi-plane copy-back program.

1.6. Mode Selection

Table 1-5. Mode Selection

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	Mode	
H	L	L	Rising	H	X	Read Mode	Command Input
L	H	L	Rising	H	X		Address Input (5 Cycles)
H	L	L	Rising	H	H	Write Mode	Command Input
L	H[1)]	L	Rising	H	H		Address Input (5 Cycles)
L	L	L	Rising	H	H	Data Input	
L	L[1)]	L	H	Falling	X	Sequential Read and Data Output	
L	L	L	H[3)]	H[3)]	X	During Read (Busy)	
X	X[1)]	X	X	X	H	During Program (Busy)	
X	X	X	X	X	H	During Erase (Busy)	
X	X	X	X	X	L	Write Protect	
X	X	H	X	X	0V/Vcc[2)]	Stand-By	

Notes:
1. X can be VIL or VIH. H = Logic level “High”. L = Logic level “Low”.
2. $\overline{WP}$ should be biased to CMOS high or CMOS low for stand-by mode.
3. $\overline{WE}$ and $\overline{RE}$ during Read Busy must be keep on high to prevent unplanned command/address/data input or to avert unintended data out. In this time, only Reset, Read Status, and Multi-plane Read Status can be inputted to the device.

2. Electrical Characteristics

2.1. Absolute Maximum Ratings

Table 2-1. Absolute maximum ratings

Item	Symbol	Value	Unit
		Min	
Ambient Operating Temperature (Commercial Temperature Range) *P/N: H27UDG8M2MTR-BC	TA	0 to +70	degree
Temperature Under Bias	TBIAS	-50 to +125	
Storage Temperature	TSTG	-65 to +150	
Input or Output Voltage	VIO	-0.6 to 4.6	V
Supply Voltage	VCC	-0.6 to 4.6	

Notes:
1. Except for the rating “Operating Temperature Range”, stresses above those listed in the Table “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.
2. Minimum voltage may undershoot to -2V during transition and for less than 20ns during transitions.
Maximum voltage may overshoot to Vcc+2V during transition and for less than 20ns during transitions.

2.2. Recommended DC Operating Conditions

Table 2-2. Recommended DC operating conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	VCC	2.7	3.3	3.6	V
Ground voltage supply	VSS	0	0	0	V

2.3. Capacitance

The input capacitance requirements are defined in nest Table. The TSOP testing conditions that be used to verify the input capacitance requirements are: temperature of 25 degrees, VIN = 0V, and a frequency of 1MHz.

Table 2-3. TSOP Input/ Output capacitance (TA=25C, VCC=3.3V, f=100MHz)

Item	Symbol	Test Condition	Device	Min	Max	Unit
Input/Output Capacitance	CI/O	VIL=0V	H27UDG8M2MTR-BC	-	10	pF
Input Capacitance	CIN	VIN=0V		-	10	

2.4. Electrical DC and Operating Characteristics

Table 2-4. DC Characteristics

Parameter		Symbol	Test Conditions	H27UDG8M2MTR-BC			Units
				Typ	Typ	Max	
Power on reset current		ICC0	FFh command input after power on	-	-	50	mA
Operating Current	Read	ICC1	tRC= tRC(min), CE#=VIL, IOUT=0 mA	-	-	50	mA
	Program	ICC2	-	-	-	50	mA
	Erase	ICC3	-	-	-	50	mA
Stand-by Current (CMOS)		ICC5	CE#=VCC-0.2, WP#=0V/VCC	-	10	50	uA
Input Leakage Current		ILI	VIN=0 to VCC(MAX)	-	-	+/-10	uA
Output Leakage Current		ILO	VOUT=0 to VCC(MAX)	-	-	+/-10	uA
Input High Voltage		VIH	-	VCC*0.8	-	VCC+0.3	V
Input Low Voltage		VIL	-	-0.3	-	0.2*VCC	V
Output High Voltage Level		VOH	IOH=-400uA	2.4	-	-	V
Output Low Voltage Level		VOL	IOL=2.1mA	-	-	0.4	V
Output Low Current (R/B#)		IOL (R/B#)	VOL=0.4V	8	10	-	mA

2.5. Program/ Read / Erase Characteristics

Table 2-5. Program/ Read / Erase Characteristics

Parameter	Symbol	Typ.	Max	Unit
Program (following 10h)	tPROG	2200	-	uS
Multi-plane Program / Multi-plane Copy-back Program (following 11h)	tDBSY	0.5	-	uS
Data Transfer Time for LSB	tDTBSY1	-	20	uS
Data Transfer Time for CSB	tDTBSY2	-	20	uS
Cache Read / Multi-plane Cache Read (following 31h/3Fh)	tCBSYR	-	tR	uS
Block Erase / Multi-plane Block Erase	tBERS	6.5	10	mS
Number of partial Program Cycles in the same page	NOP	-	1	Cycle

Notes:
Typical value is measured at VCC=3.3V, TA=25C. Not 100% tested.

2.6. AC Test condition

Table 2-6. AC Test Conditions

Parameter	Value
Input Pulse Levels	0 V to VCC
Input Rise and Fall Times	5ns
Input and Output Timing Levels	VCC*0.5
Output Load (2.7V-3.6V)	CL= 50pF

Note:
These parameters are verified device characterization and are not 100% tested.

2.7. AC Characteristics for Command, Data and Address Input

Table 2-7. Parameter Descriptions

Parameter	Symbol	H27UDG8M2MTR-BC		Unit
		Min	Max	
CLE setup time	tCLS	6	-	ns
CLE Hold time	tCLH	3	-	ns
$\overline{CE}$ setup time	tCS	20	-	ns
$\overline{CE}$ hold time	tCH	5	-	ns
$\overline{WE}$ pulse width	tWP	8	-	ns
ALE setup time	tALS	6	-	ns
ALE hold time	tALH	3	-	ns

Parameter	Symbol	H27UDG8M2MTR-BC		Unit
		Min	Max	
Data setup time	tDS	6	-	ns
Data hold time	tDH	2	-	ns
Write cycle time	tWC	16	-	ns
$\overline{WE}$ high hold time	tWH	6	-	ns
ALE to $\overline{RE}$ delay	tAR	10	-	ns
CLE to $\overline{RE}$ delay	tCLR	10	-	ns
Ready to $\overline{RE}$ low	tRR	20	-	ns
$\overline{RE}$ pulse width	tRP	8	-	ns
$\overline{WE}$ high to busy	tWB	-	100	ns
Read cycle time	tRC	16	-	ns
$\overline{RE}$ access time	tREA	-	16	ns
$\overline{RE}$ high to output high Z	tRHZ	-	100	ns
$\overline{CE}$ high to output high Z	tCHZ	-	50	ns
$\overline{RE}$ high to output hold	tRHOH	15	-	ns
$\overline{RE}$ low to output hold	tRLOH	5	-	ns
$\overline{RE}$ or $\overline{CE}$ high to output hold	tCOH	15	-	ns
$\overline{RE}$ high hold time	tREH	6	-	ns
$\overline{WE}$ high to $\overline{RE}$ low	tWHR	80	-	ns
$\overline{WE}$ high to $\overline{RE}$ low for Random data out	tWHR2	300	-	ns
$\overline{RE}$ high to $\overline{WE}$ low	tRHW	100	-	ns
Output high Z to $\overline{RE}$ low	tIR	0	-	ns
$\overline{CE}$ low to $\overline{RE}$ low	tCR	10	-	ns
Address to data loading time	tADL	300	-	ns
Device resetting time (Read/Program/Erase)	tRST	-	20/30/500	ns
Write protection time	tWW	100	-	ns

Notes:
1. If Reset Command (FFh) is written at Ready state, the device goes into Busy for maximum 5us.
2. Program / Erase Enable Operation: $\overline{WP}$ high to $\overline{WE}$ High. Program / Erase Disable Operation: $\overline{WP}$ Low to $\overline{WE}$ High.
3. The transition of the corresponding control pins must occur only while $\overline{WE}$ is held low.
4. tADL is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ rising edge of first data cycle.

2.8. Status Register Coding

Table 2-8. Status Register Coding For 70h/78h command

I/O	Page Program	Block Erase	Read	Cache Read	Coding
					70h / 78h
0	Pass / Fail	Pass / Fail	N/A	N/A	N page Pass : '0' Fail : '1'
1	N/A	N/A	N/A	N/A	N-1 page Pass : '0' Fail : '1'
2	N/A	N/A	N/A	N/A	'0'
3	N/A	N/A	N/A	N/A	'0'
4	N/A	N/A	N/A	N/A	'0'
5	N/A	N/A	N/A	Ready / Busy	Ready / Busy Busy : '0' Ready : '1'
6	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Data Cache Ready / Busy Busy : '0' Ready : '1'
7	Write Protect	Write Protect	Write Protect	Write Protect	Protected : '0' Not Protected : '1'

Notes:
1. I/O0 : This bit is only valid for Program and Erase operations.
2. I/O5 : If set to one, then there is no array operation in progress. If cleared to zero, then there is a command being processed (I/O6 is cleared to zero) or an array operation in progress. When overlapped interleaved operations or cache commands are not supported, this bit is not used.

3. I/O6 : If set to one, then the device or interleaved address is ready for another command and all other bits in the status value are valid. If cleared to zero, then the last command issued is not yet complete and Status Register bits<5:0> are invalid value. When cache operations are in use, then this bit indicates whether another command can be accepted, and I/O5 indicates whether the last operation is complete.

Table 2-9. Status Register Coding For 75h command

I/O	Page Program	Block Erase	Read	Cache Read	Coding
					75h
0	/ Fail	/ Fail	N/A	N/A	N page Pass : '0' Fail : '1'
1	Plane 0 Pass / Fail	Plane 0 Pass / Fail	N/A	N/A	N page Pass : '0' Fail : '1'
2	Plane 1 Pass / Fail	Plane 1 Pass / Fail	N/A	N/A	N page Pass : '0' Fail : '1'
3	N/A	N/A	N/A	N/A	N-1 page Pass : '0' Fail : '1'
4	N/A	N/A	N/A	N/A	N-1 page Pass : '0' Fail : '1'
5	N/A	N/A	N/A	Ready / Busy	Ready / Busy Busy : '0' Ready : '1'

I/O	Page Program	Block Erase	Read	Cache Read	Coding
					75h
6	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Data Cache Ready / Busy Busy : '0' Ready : '1'
7	Write Protect	Write Protect	Write Protect	Write Protect	Protected : '0' Not Protected : '1'

2.9. Device Identifier Coding

Table 2-10. Product Read ID

	Description
1st Byte	Maker Code
2nd Byte	Device Code
3rd Byte	Internal Number, Cell Type, Number of Program pages
4th Byte	Page size (without Spare area), Block size (without Additional Block), Redundant Area size
5th Byte	Plane Number, ECC Level
6th Byte	NAND Technology, Interface

Device	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle	6th Cycle
H27UDG8M2MTR-BC	ADh	3Ah	18h	A3h	61h	25h

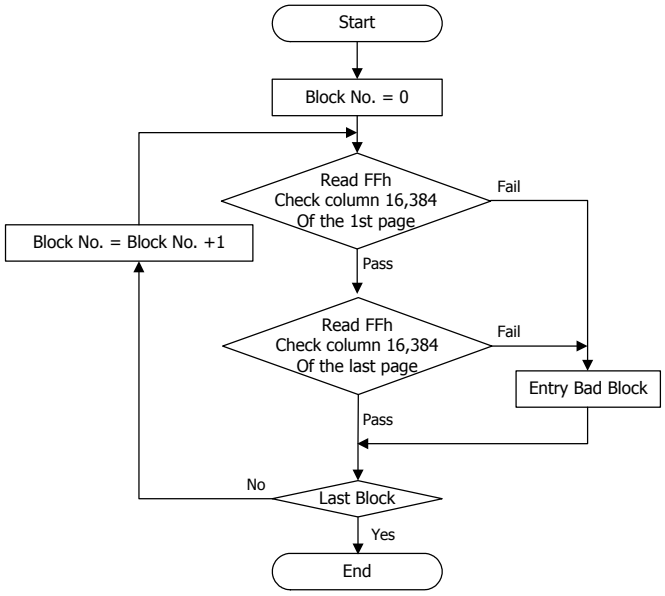
Note: The Read ID is setted by default value.

3. Application notes and comments

3.1. System Bad Block Replacement

Devices with Bad Blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A Bad Block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor. The devices are supplied with all the locations inside valid blocks erased (FFh). The Bad Block Information is written prior to shipping. Any block where the 1st Byte in the spare area of the first and last page does not contain FFh is a Bad Block. The Bad Block Information must be read before any erase is attempted as the Bad Block Information may be erased. For the system to be able to recognize the Bad Blocks based on the original information it is recommended to create a Bad Block table following the flowchart shown in Figure of *"Bad block management flow chart"*. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment.

Figure 3-1. Bad block management flow chart



Notes:
1. Do not try to erase the detected bad blocks, because the bad bock information will be lost.
2. Do not perform program and erase operation in invalid block, it is impossible to guarantee the input data and to ensure that the function is normal.

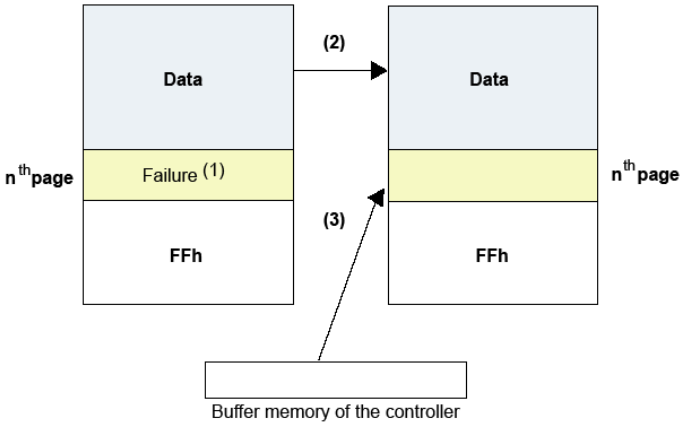
3.2. Bad Block Replacement

This device may have the invalid blocks when shipped from factory. An invalid block is one that contains one or more bad bits. Over the lifetime of the device additional Bad Blocks may develop. In this case, the block has to be replaced by copying the data to a valid block. These additional Bad Blocks can be identified as attempts to program or erase them will give errors in the Status Register.
The failure of a page program operation does not affect the data in other pages in the same block. Bad block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block. Refer to Table for "*Block failure*" and Figure of "*Block replacement*" for the recommended procedure to follow if an error occurs during an operation.

Table 3-1. Block failure

Operation	Recommended Procedure
Erase	Block Replacement
Program	Block Replacement
Read	ECC

Figure 3-2. Block replacement



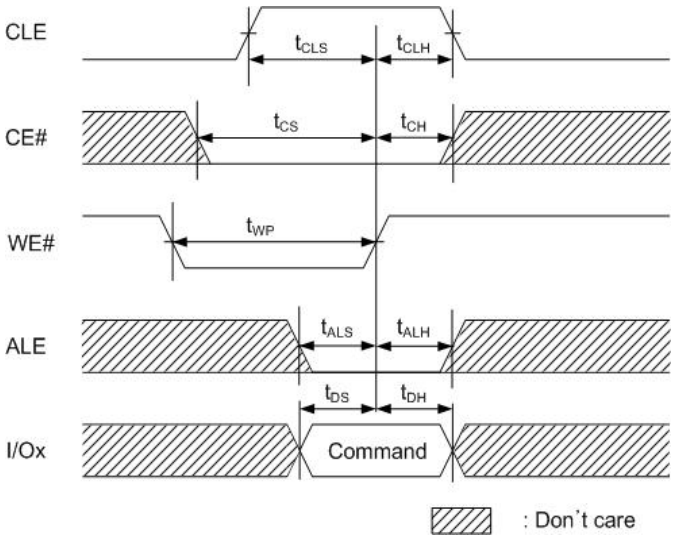
Notes:
1. An error occurs on nth page of the Block A during Program or Erase operation.
2. Data in Block A is copied to same location in Block B which is valid block.
3. Nth page of block A which is in controller buffer memory is copied into nth page of Block B
4. Bad block table should be updated to prevent from erasing or programming Block A.

4. Device Operation

4.1. General Timing

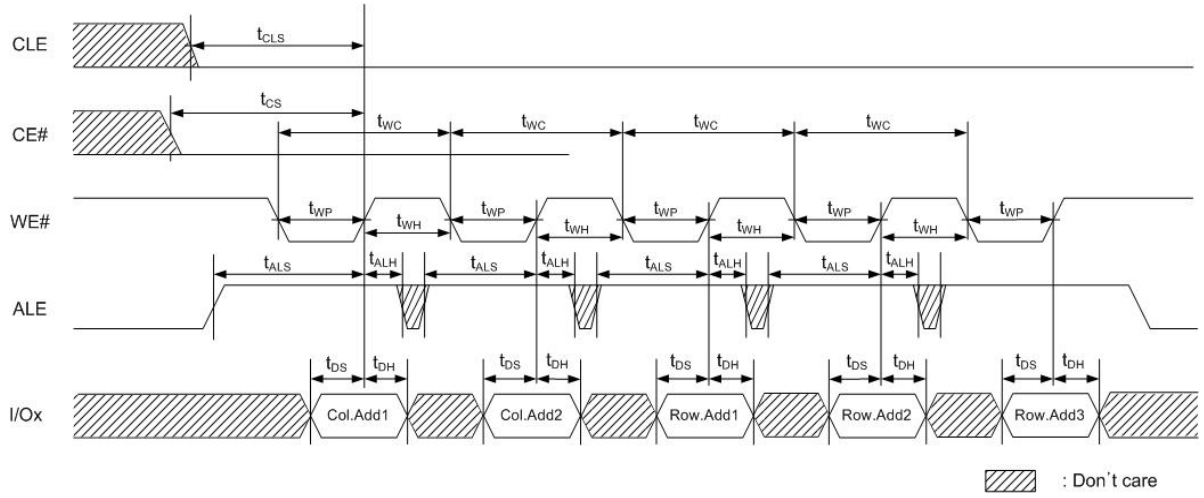
4.1.1 Command Latch Cycle

Figure 4-1. Command Latch Cycle Timings



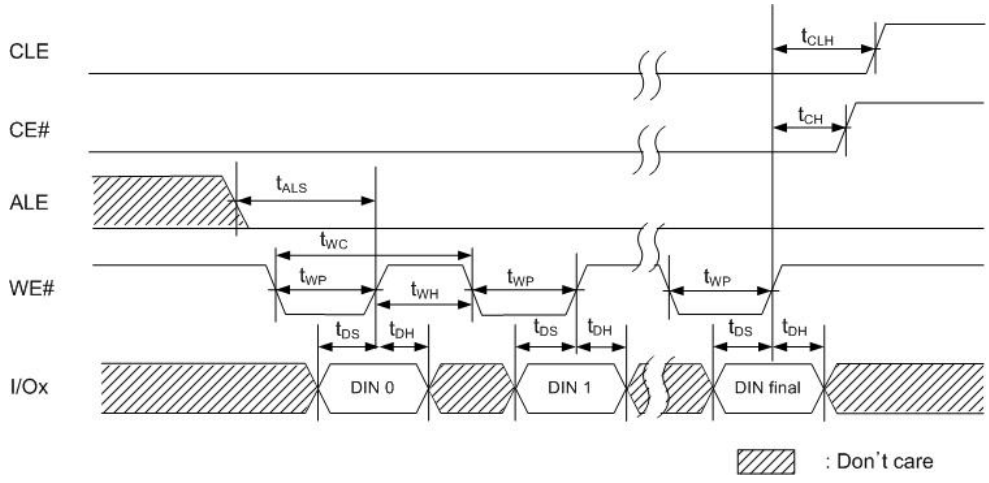
4.1.2 Address Latch Cycle

Figure 4-2. Address Latch Cycle Timings



4.1.3 Basic Data Input Timing

Figure 4-3. Input Data Latch Cycle Timings



4.1.4 Basic Data Output Timing

Figure 4-4. Data Output Cycle Timings (CLE=L, $\overline{WE}$=H, ALE=L, $\overline{WP}$=H)

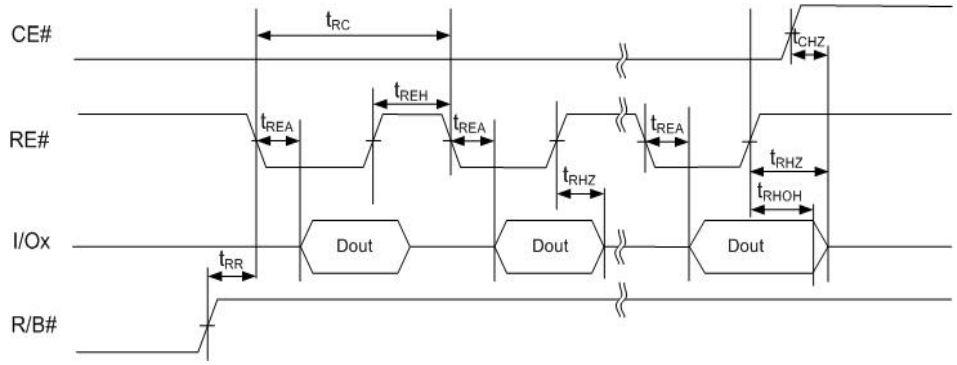
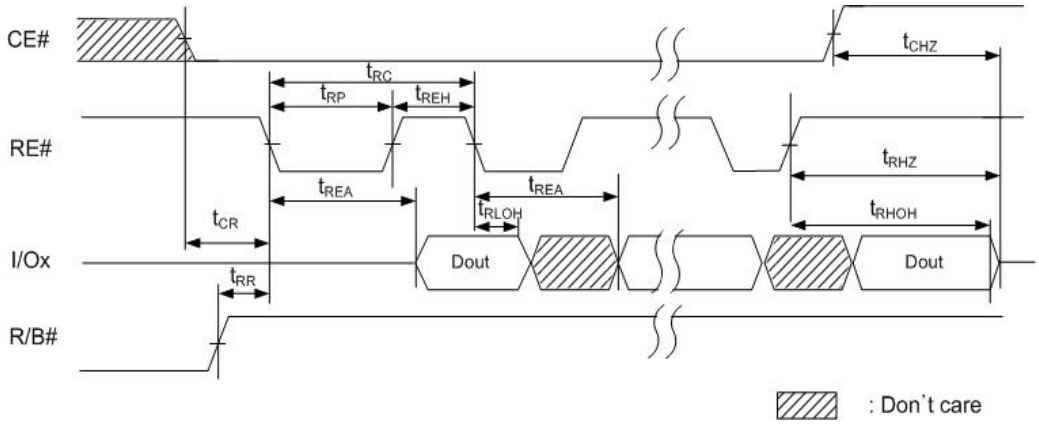
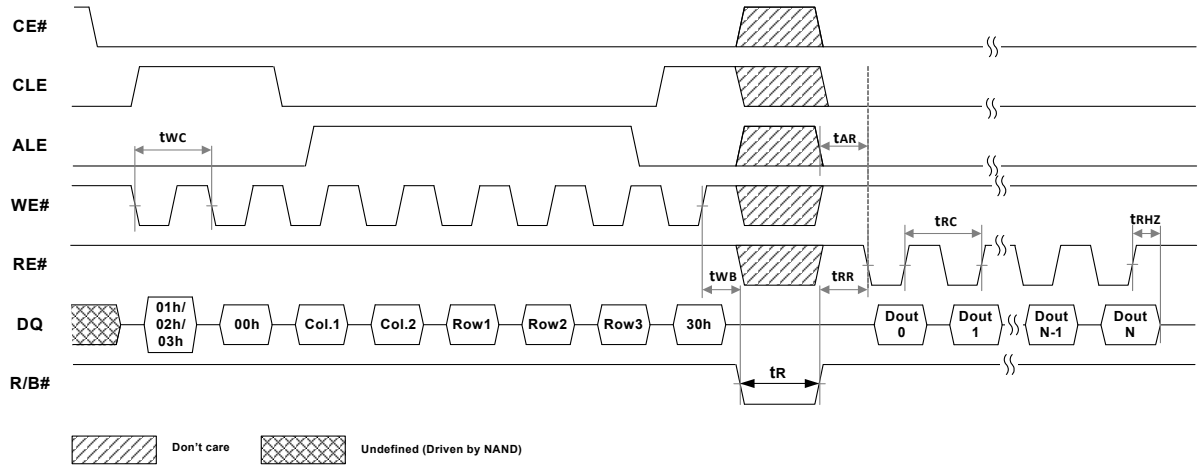


Figure 4-5. Data Output Cycle Timings (EDO type, CLE=L, $\overline{WE}$=H, ALE=L)



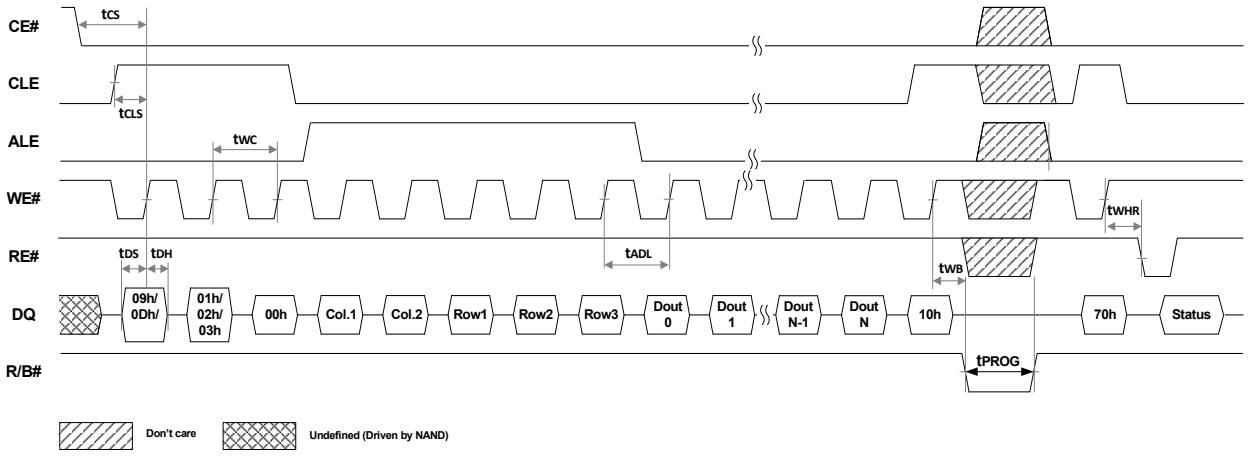
4.1.5 Page Read Timing

Figure 4-6. Page Read Timings



4.1.6 Page Program Timing

Figure 4-7. Page Program Timings

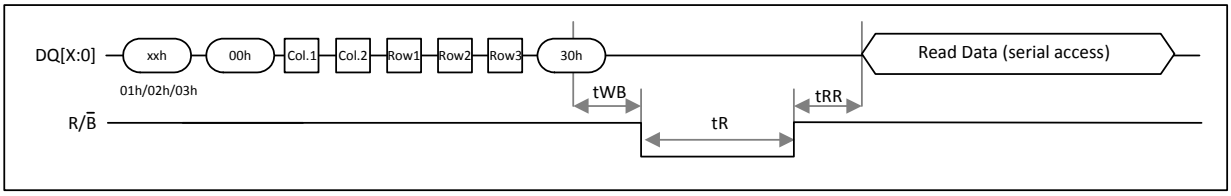


4.2. Page Read Operation

This operation is initialized by 00h-30h to the command register along with followed by five address input cycles.
The 18,432 bytes of data within the selected page are transferred to the data registers in less than tR. The system controller may detect the completion of this data transfer tR by analyzing the output of R/B pin. Once the data in a page is loaded into the data registers, they may be read out in 20ns cycle time by sequentially pulsing RE#. The repetitive high to low transitions of the RE clock make the device output the data starting from the selected column address up to the last column address.

The device may output random data in a page instead of the consecutive sequential data by random data output command. The column address of next data, which is going to be out, may be changed to the address, which follows random data output command. Random data output can be operated multiple times, regardless of how many times it is done in a page.

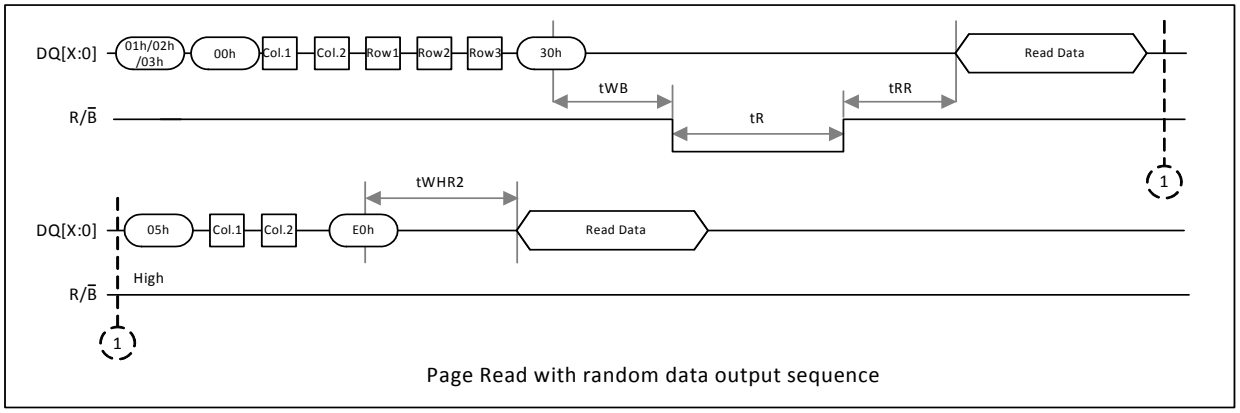
Figure 4-8. Page Read Operation



Random data output

Random data output operation changes the column address from which data is being read in the page register. Random data output is only issued in Ready state. Refer to Figure of "*Random data output*".

Figure 4-9. Random data output

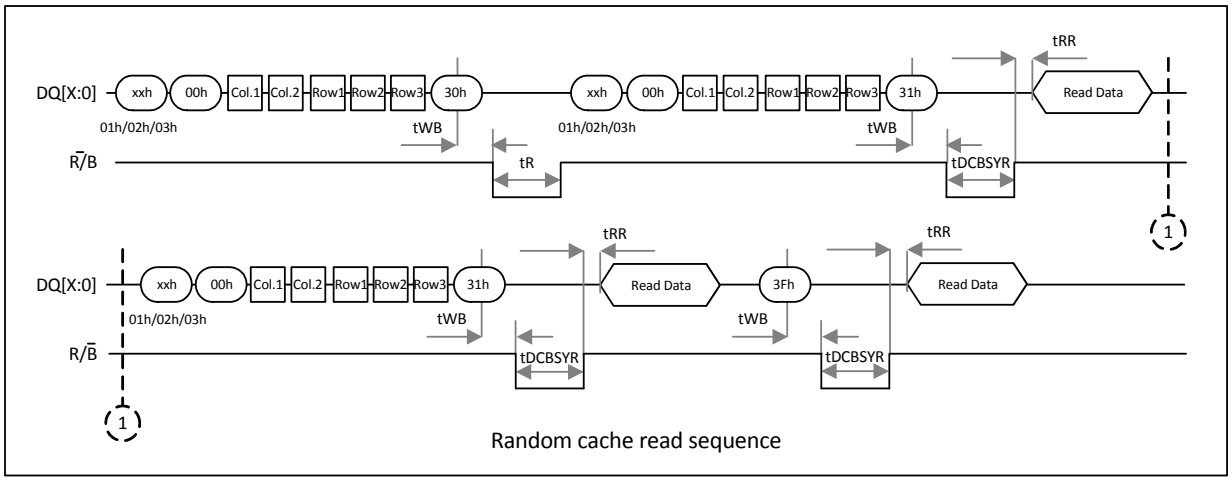


Page Read with random data output sequence

4.3. Random Cache Read

To improve page read throughput, cache read operation is used within a block. First step is same as normal page read, issuing a page read sequence (00-30h). After random access (R/$\overline{B}$ returns to high), 31h command is latched into the command register. Data is being transferred from the data register to the cache register. While cache register data is outputted, next page is transferred from memory cell to data register. R/$\overline{B}$ will stay low during present page random accessing and previous page transferring to cache register. Because it is not necessary to output a whole page data before issuing another 31h command, if serial data output time exceeds random access time (t_R), the random access time can be hidden. The subsequent pages are issued additional 31h commands. To terminate cache read, 3Fh command should be issued. This command transfer data from data register to the cache register without issuing next page read. During the Cache Read Operation, device doesn't allow any other command except Cache Read command (31h), Read Status (70h, 78h, 75h), Read (00h), and Reset (FFh). To carry out other operations after cache operation, cache read must be ended by 3Fh command or issue reset (FFh) before next operation.

Figure 4-10. Random Cache read



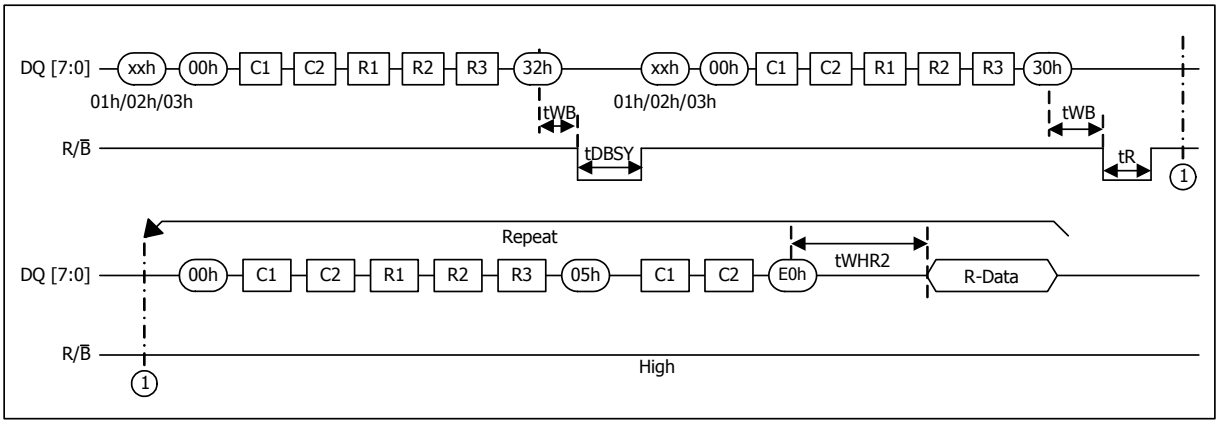
4.4. Multi Plane Page Read

Multi-Plane Page Read is an extension of Page Read, for a single plane with 18,432byte page registers. Since the device is equipped with two memory planes, activating the two sets of 18,432byte page resisters enables a random read of two pages. Multi-Plane Page Read is initiated by repeating command 60h followed by three address cycles twice. In this case, only same page of each block can be selected from each plane.

After Read Confirm command (30h) the 18,432bytes of data within the selected two pages are transferred to the data registers in less than tR. The system controller can detect the completion of data transfer (tR) by monitoring the output of R/B pin.

Once the data is loaded into the data registers, the data output of first plane can be read out by issuing command 00h with Five Address Cycles, command 05h with two column address and finally E0h. The data output of second plane can be read out using the identical command sequences. The restrictions for Multi-Plane Page Read are shown in Figure of "*Multi plane page read*". Multi-Plane Page Read must be used in the block which has been programmed with Multi-Plane Page Program.

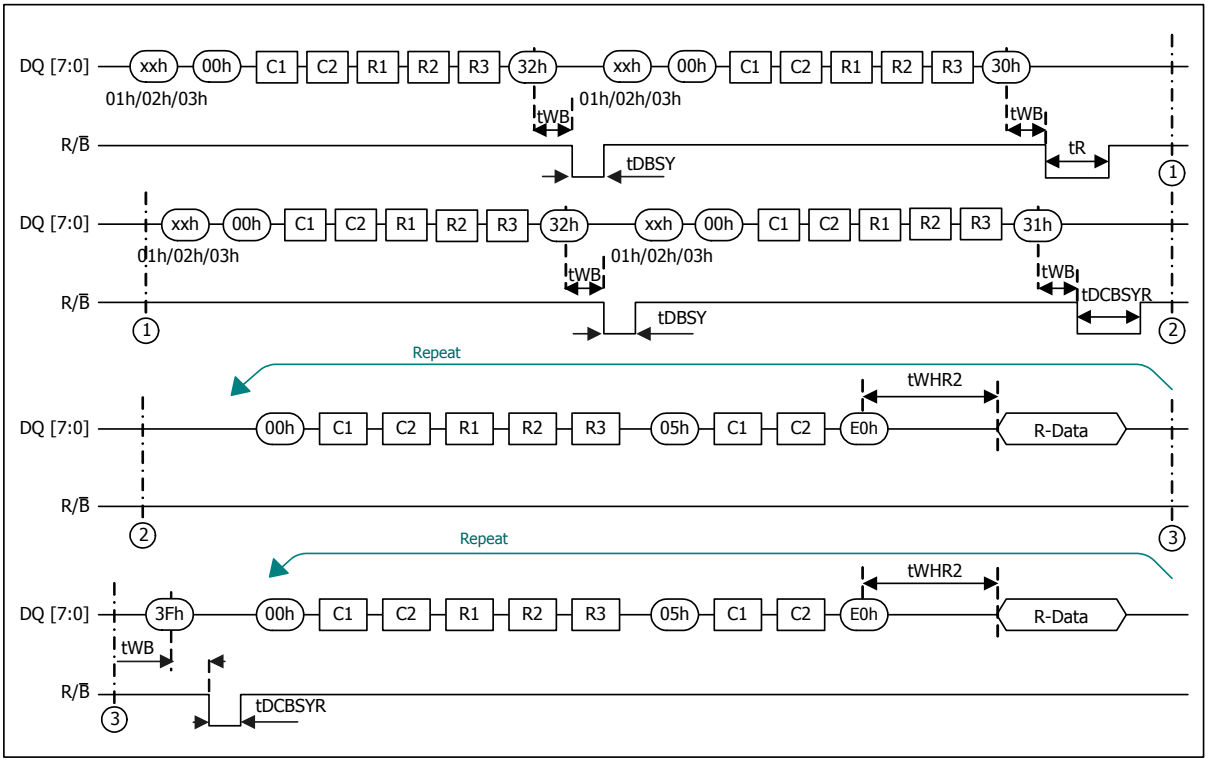
Figure 4-11. Multi plane page read



4.5. Multi Plane Cache Read (available only within a block)

The device supports multi-plane cache read, which enables high read throughput by reading two pages in parallel. Figure of "*Multi plane cache read*" shows the command sequence for the multi-plane cache read operation. Both confirm commands, 30h and 33h, are valid for the first page read sequence.

Figure 4-12. Multi plane cache read

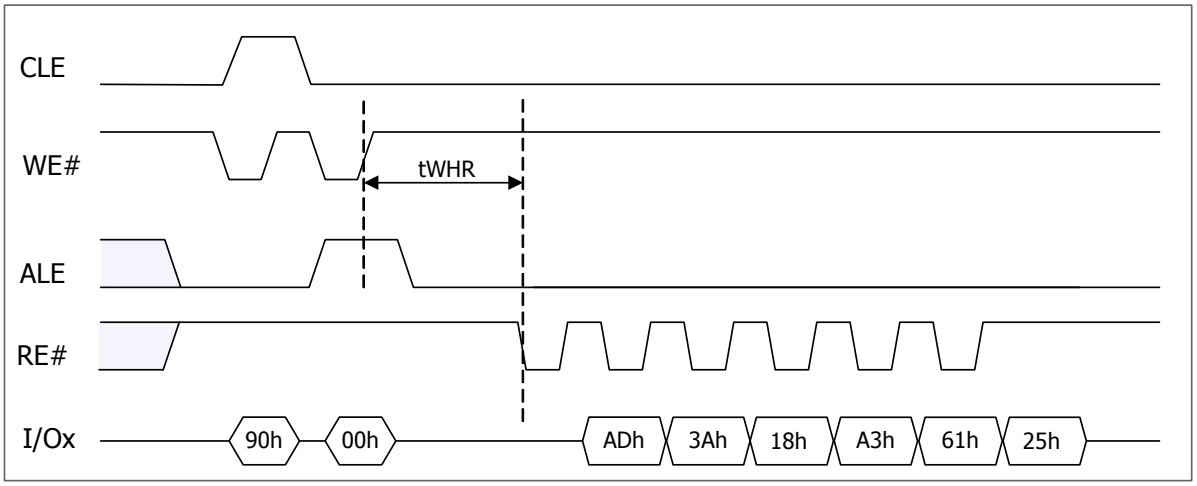


Notes:
1. plane 0 and plane 1 should be selected within the same chip
2. Only one block should be selected from the each plane.
3. Multi plane cache read is available only within a block per plane.
4. Selected WL address except R1-0 within two blocks must be same.
5. The operation has to be terminated with "3Fh" command.
6. It's possible to confirm the multi-plane cache read first step using both 30h and 33h.

4.6. Read ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Six read cycles sequentially output the manufacturer code (ADh), and the device code and 3rd, 4th, 5th, 6th cycle ID, respectively. The command register remains in Read ID mode until further commands are issued to it. Figure of "*Read ID*" shows the operation sequence, while table of "2-10 *Product Read ID*" explain the byte meaning.

Figure 4-13. Read ID



4.9. Read Status Register

The device contains a Status Register which may be read to find out whether read, program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing Read Status (70h) or Multi Plane Read Status (78h,75h) command to the command register, a read cycle outputs the content of the Status Register to the I/O pins only if $\overline{CE}$ and $\overline{RE}$ are low, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/$\overline{B}$ pins are common-wired. Refer to "2.8. STATUS REGISTER CODING" for specific Status Register definitions and Figure of "*Read status*", Figure "*Multi plane read status*" for Read Status. The command register remains in Read Status mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the read command (00h) should be given before starting read cycles.

Figure 4-14. Read status

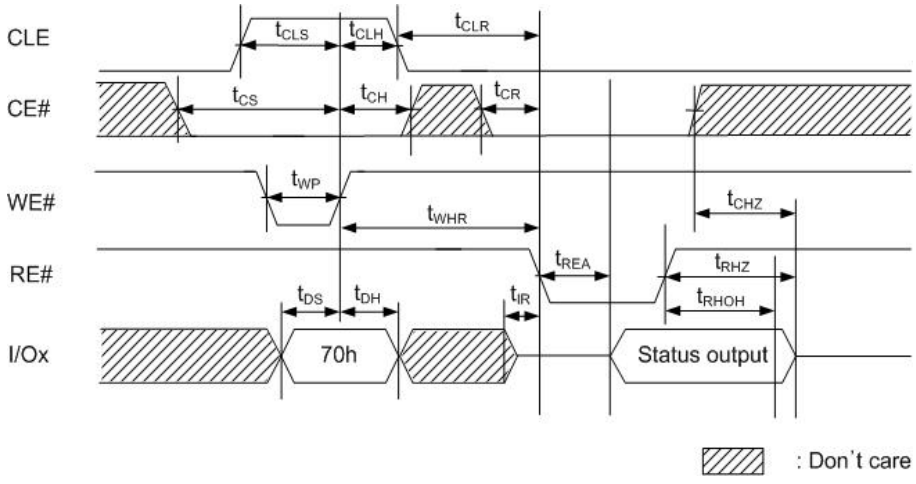
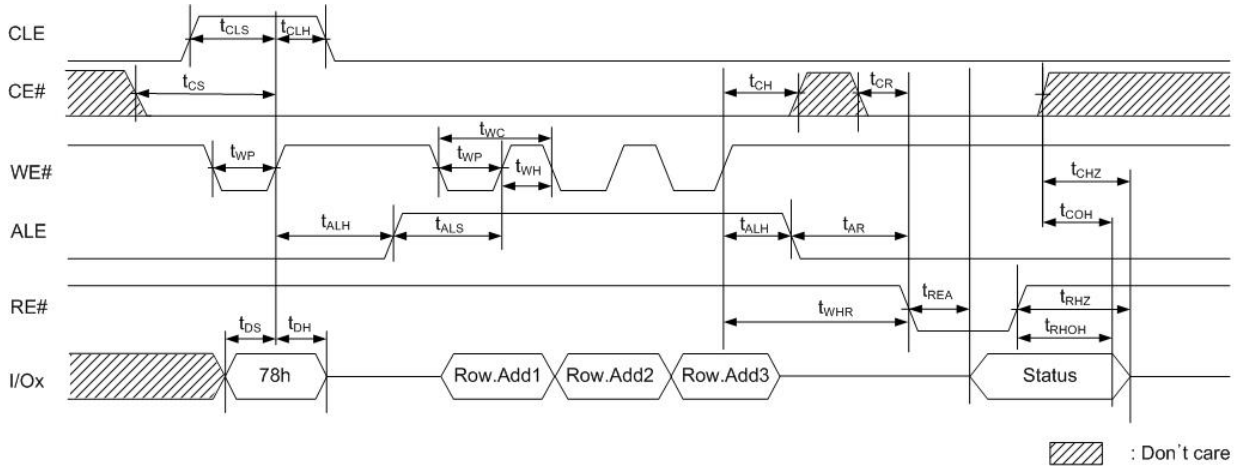


Figure 4-15. Multi plane read status



4.10. Page Program

The device is programmed as a page unit. The number of consecutive partial page programming operation within the same page without an intervening erase operation must not exceed 1 times. The program addressing should be done in sequential order in a block. A page program cycle consists of a serial data loading period in which up to 18,432 bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. The serial data-loading period begins by inputting the Serial Data Input command (80h), followed by the five cycle address inputs and then serial data.

The words other than those to be programmed do not need to be loaded. The device supports random data input in a page. The column address of next data, which will be entered, may be changed to the address which follows random data input command (85h). Random data input may be operated multiple times, regardless of how many times it is done in a page. The Page Program Confirm command (10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process.

The internal write state controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered to read the status register.

The system controller can detect the completion of a program cycle by monitoring the R/$\overline{B}$ output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. The Write Status Bit (I/O 0) is valid, when all internal operations are complete (status bit I/O 6 = high).
The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s.
The command register remains in Read Status command mode until another valid command is written to the command register.
Figure of "*Page Program*" and Figure of "*Random data input*" details the sequence.

Figure 4-16. Page Program for SLC Block

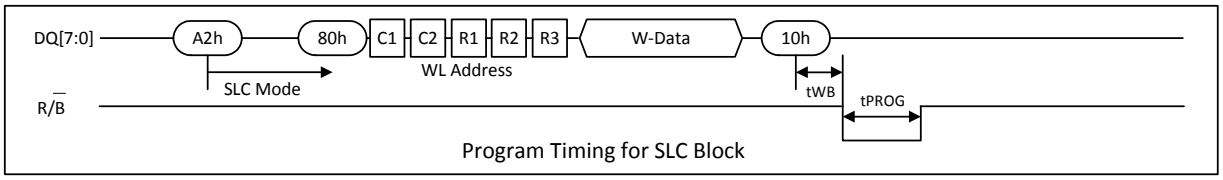


Figure 4-17. Page Program for TLC Block

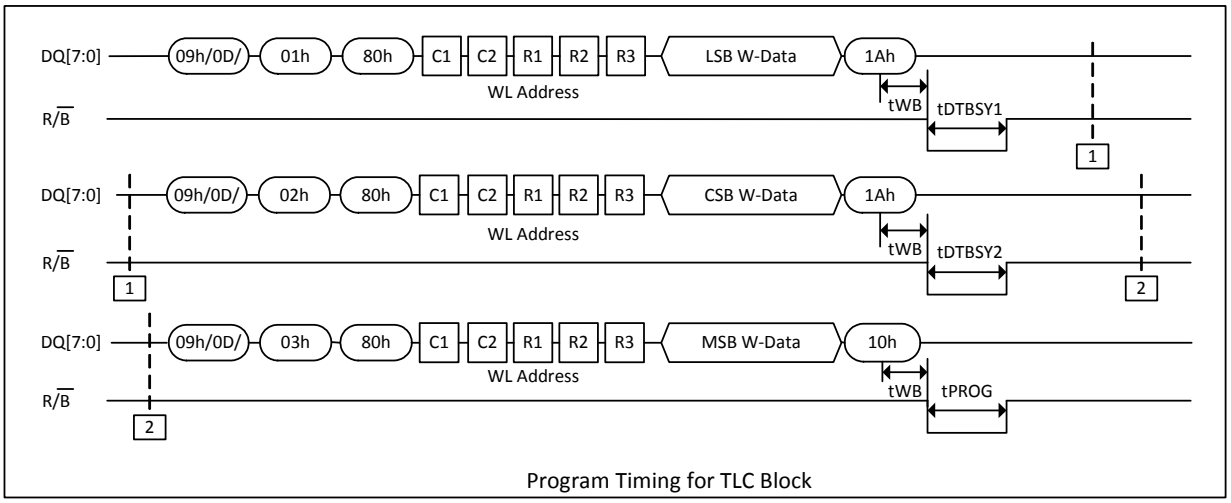
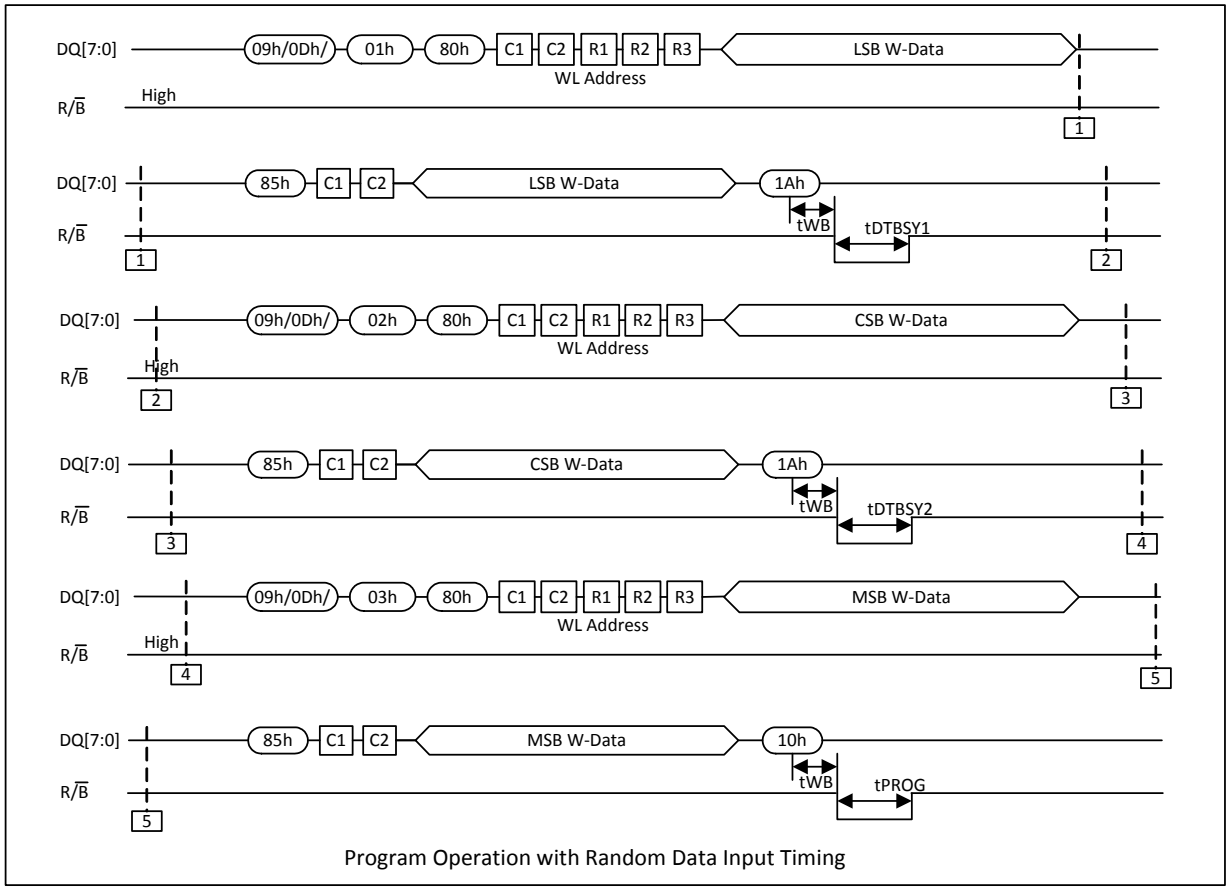


Figure 4-18. Random data input



Program Operation with Random Data Input Timing

4.11. Multi Plane Program

Device supports multiple plane program. It is possible to program in parallel 2 pages, one per each plane.
A multiple plane program cycle consists of a double serial data loading period in which up to 18,432bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. The serial data loading period begins by inputting the Serial Data Input command (80h), followed by the five cycle address inputs and then serial data for the 1st page. Address for this page must be within first plane (R1-0=0). The data of first page other than those to be programmed do not need to be loaded. The device supports random data input exactly like page program operation. The Dummy Page Program Confirm command (11h) stops 1st page data input and the device becomes busy for a short time (tDBSY).

Once it has become ready again, 80h command must be issued, followed by second address (5 cycles) and its serial data input. Address for this page must be within second plane (R1-0=1). The data of second page other than those to be programmed do not need to be loaded. Program Confirm command (10h) makes parallel programming of both pages start. User can check operation status by R/B pin or read status register command, as if it were a normal page program; status register command is also available during Dummy Busy time (tDBSY). In case of fail in first plane or second plane page program, fail bit of status register will be set: Pass/Fail status of each plane can be checked by Multi Plane Read Status. Figure of "*Multi plane page program*" details the sequence.

Figure 4-19. Multi Plane Page Program for SLC Block

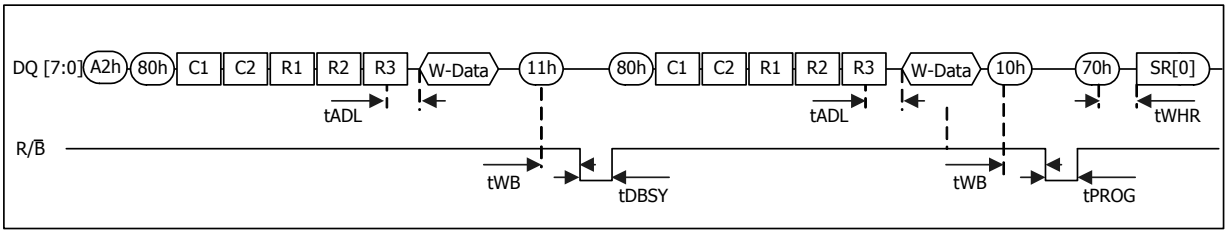
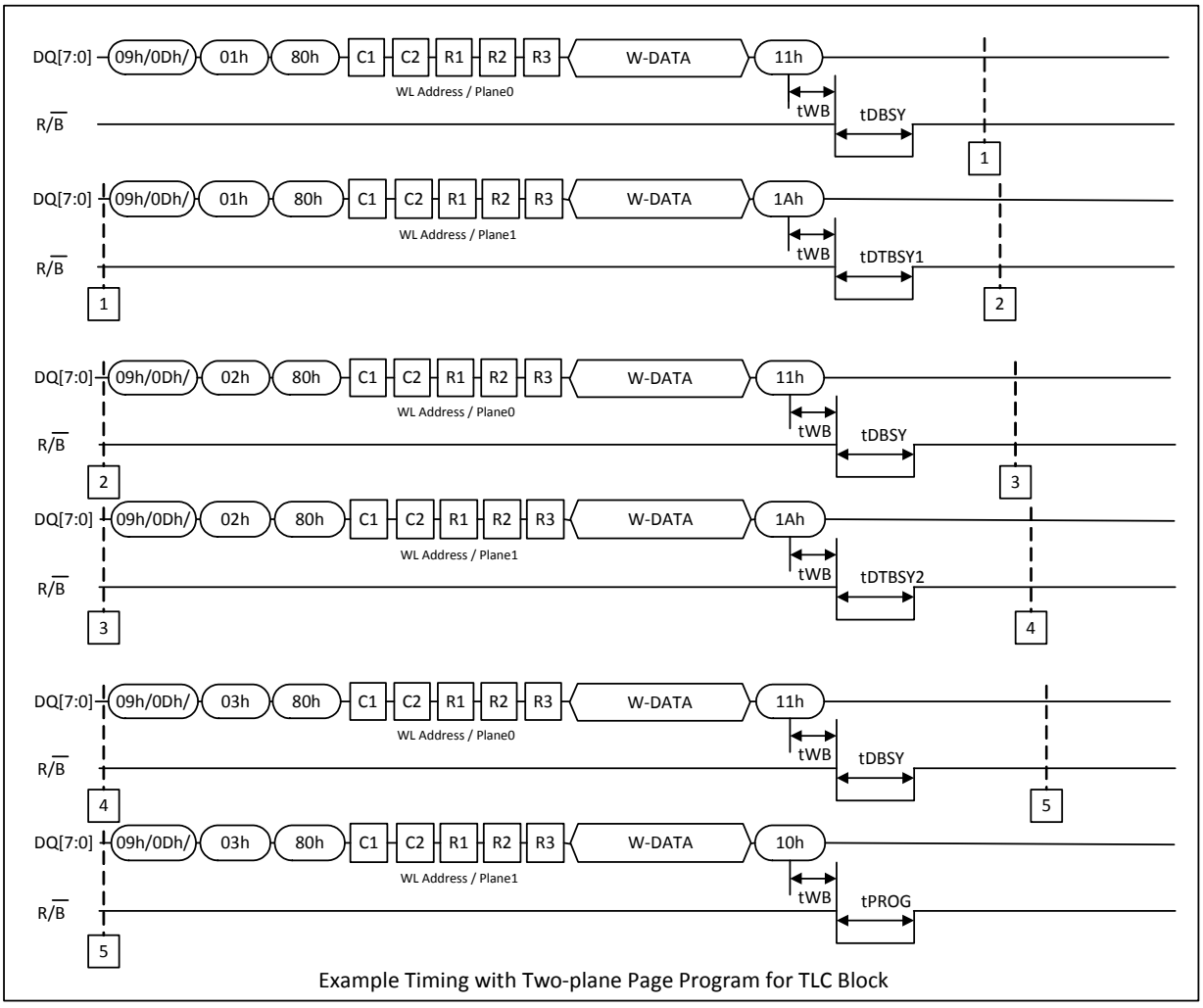


Figure 4-20. Multi Plane Page Program for TLC Block



Example Timing with Two-plane Page Program for TLC Block

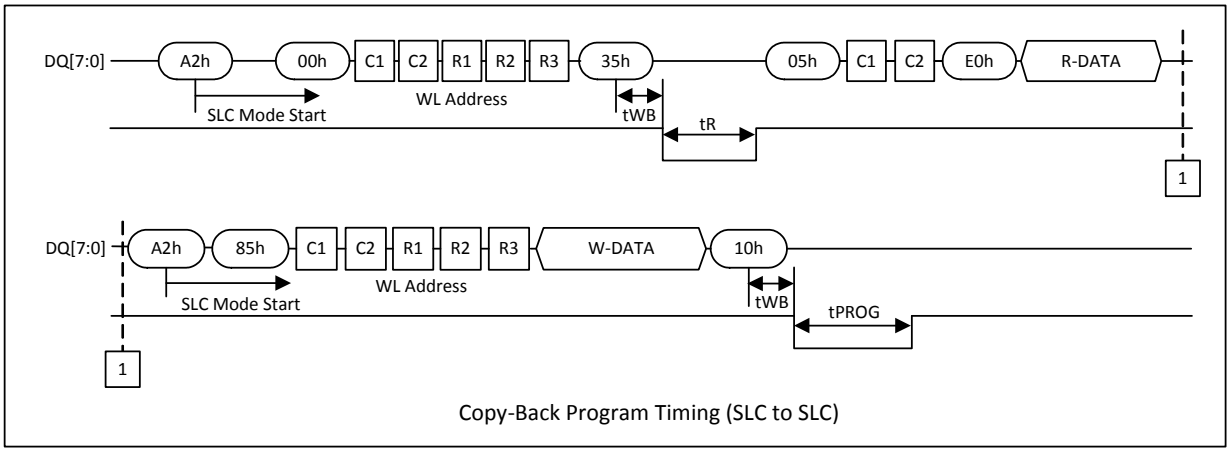
Notes:
1. plane 0 and plane 1 should be selected within the same chip.
2. Only one block should be selected from the each plane.
3. Selected WL address except R1-0 within two blocks must be same.
4. Any command between 11h and 80h is prohibited except 70h/78h/75h and FFh.
5. Read Status command can be 70h or 78h or 75h.

4.12. Copy-Back Program

Copy-Back program with Read for Copy-Back is configured to quickly and efficiently rewrite data stored in one page without data reloading when the bit error is not in data stored. Since the time-consuming re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block needs to be copied to the newly assigned free block. Copy-Back operation is a sequential execution of Read for Copy-Back and of copy-back program with the destination page and WL address. A read operation with "35h" command and the address of the source page moves the whole 18,432byte data into the internal data buffer. A bit error is checked by sequential reading the data output. In the case where there is no bit error, the data do not need to be reloaded. Therefore, Copy-Back program operation is initiated by issuing

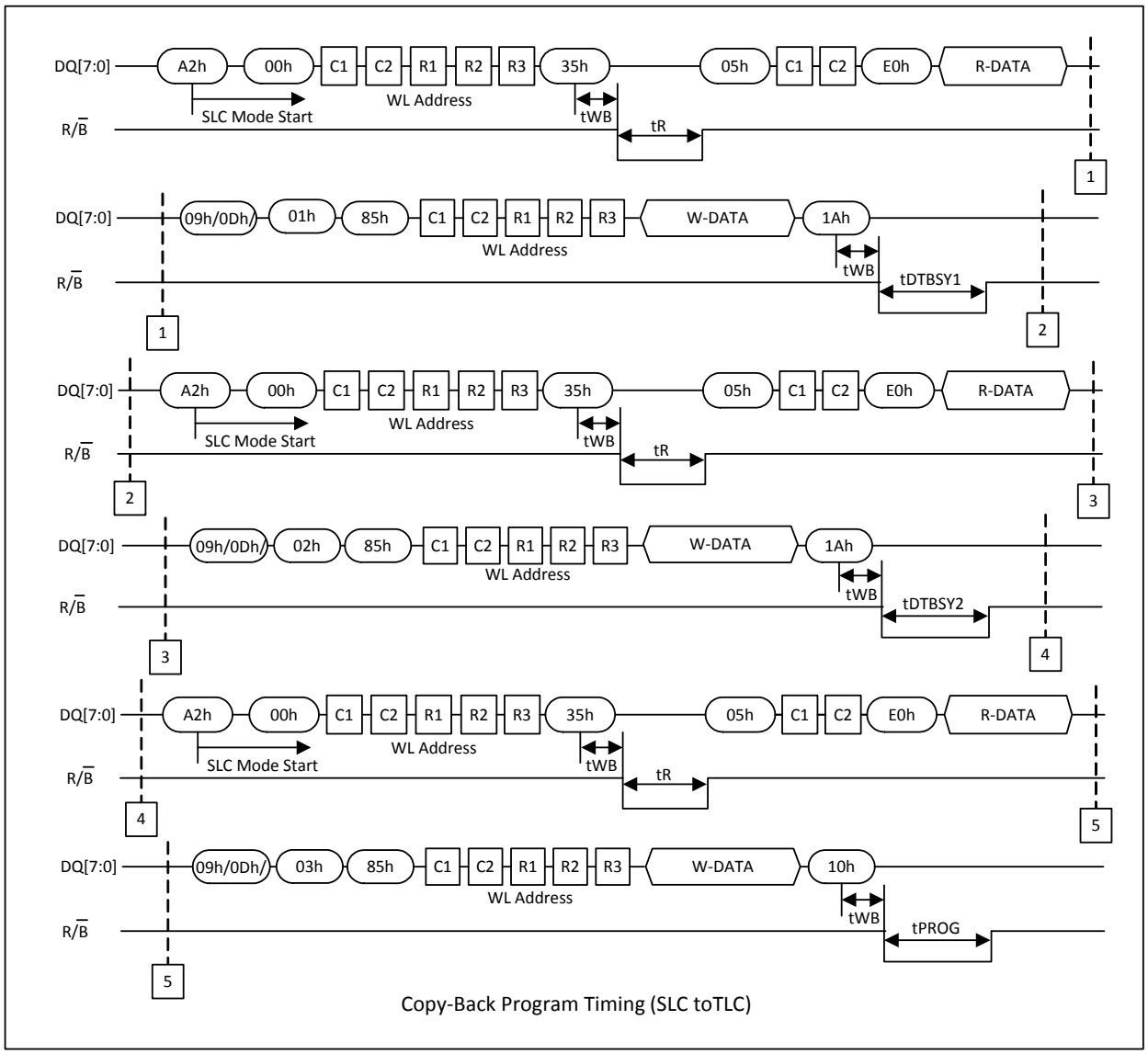
Page-Copy Data-Input command (85h) with destination page and WL address. Actual programming operation begins after Program Confirm command (10h) is issued. Once the program process starts, the Read Status Register command (70h) may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the $\overline{R/B}$ output, or the Status bit (I/O 6) of the Status Register. When the Copy-Back Program is complete, the Write Status Bit (I/O 0) may be checked. The command register remains in Read Status command mode until another valid command is written to the command register. During copy-back program, data modification is possible using random data input command (85h) as shown in Figure of "*Copy-back program*".

Figure 4-21. Copy-back program (SLC to SLC)



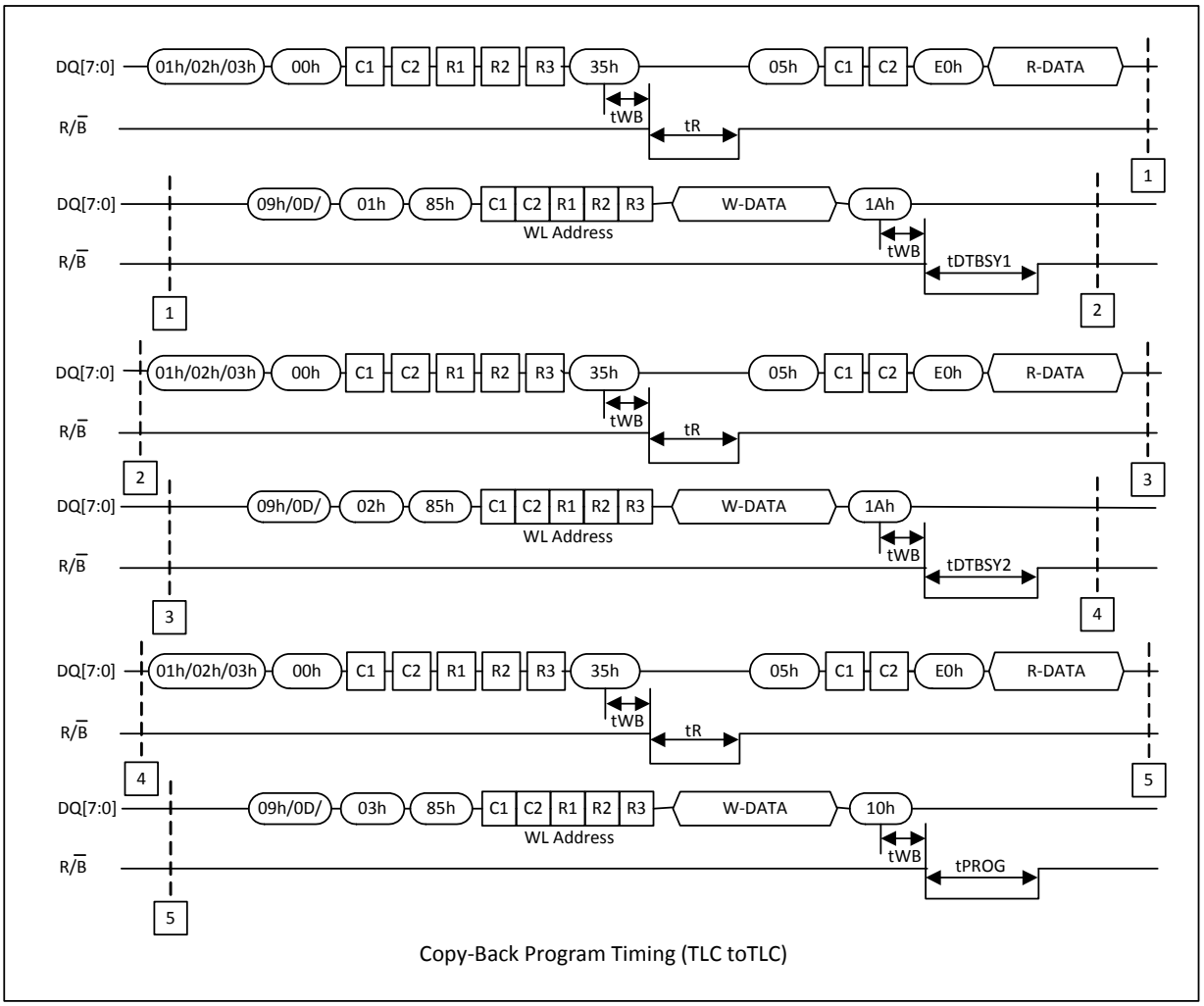
Copy-Back Program Timing (SLC to SLC)

Figure 4-22. Copy-back program (SLC to TLC)



Copy-Back Program Timing (SLC toTLC)

Figure 4-23. Copy-back program (TLC to TLC)

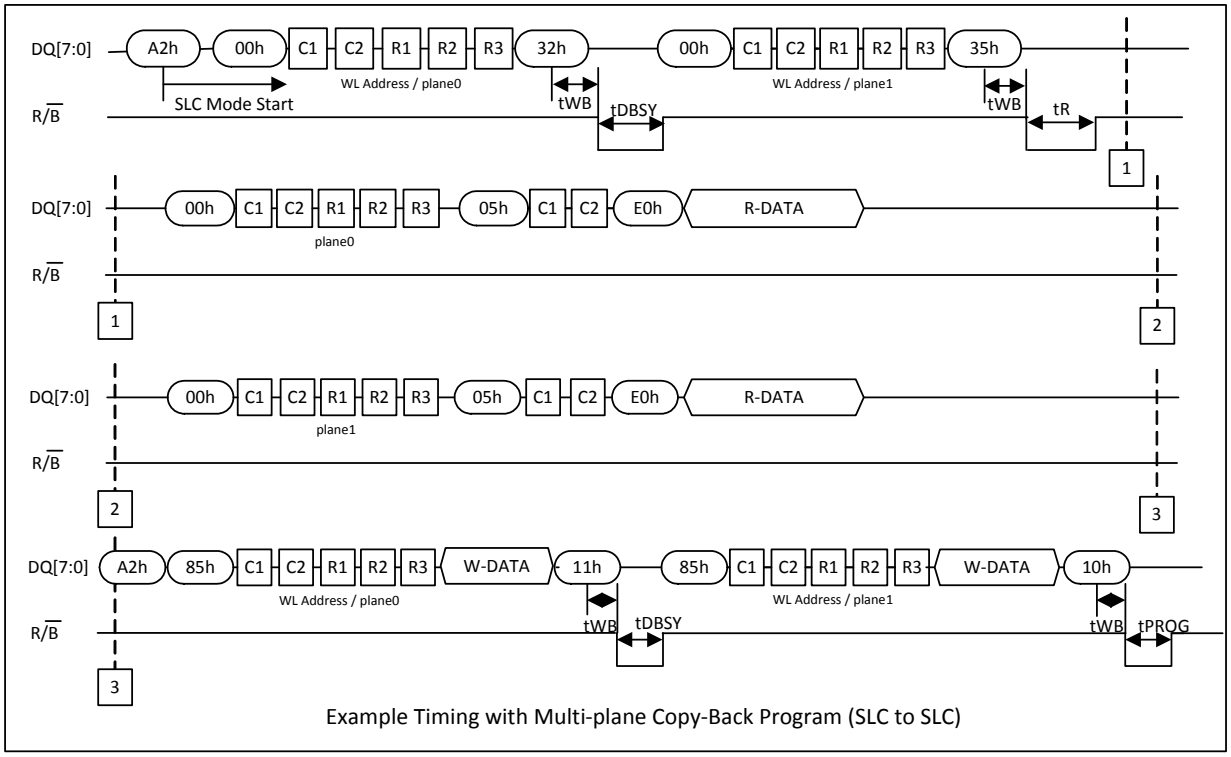


Copy-Back Program Timing (TLC toTLC)

4.13. Multi-Plane Copy-Back Program

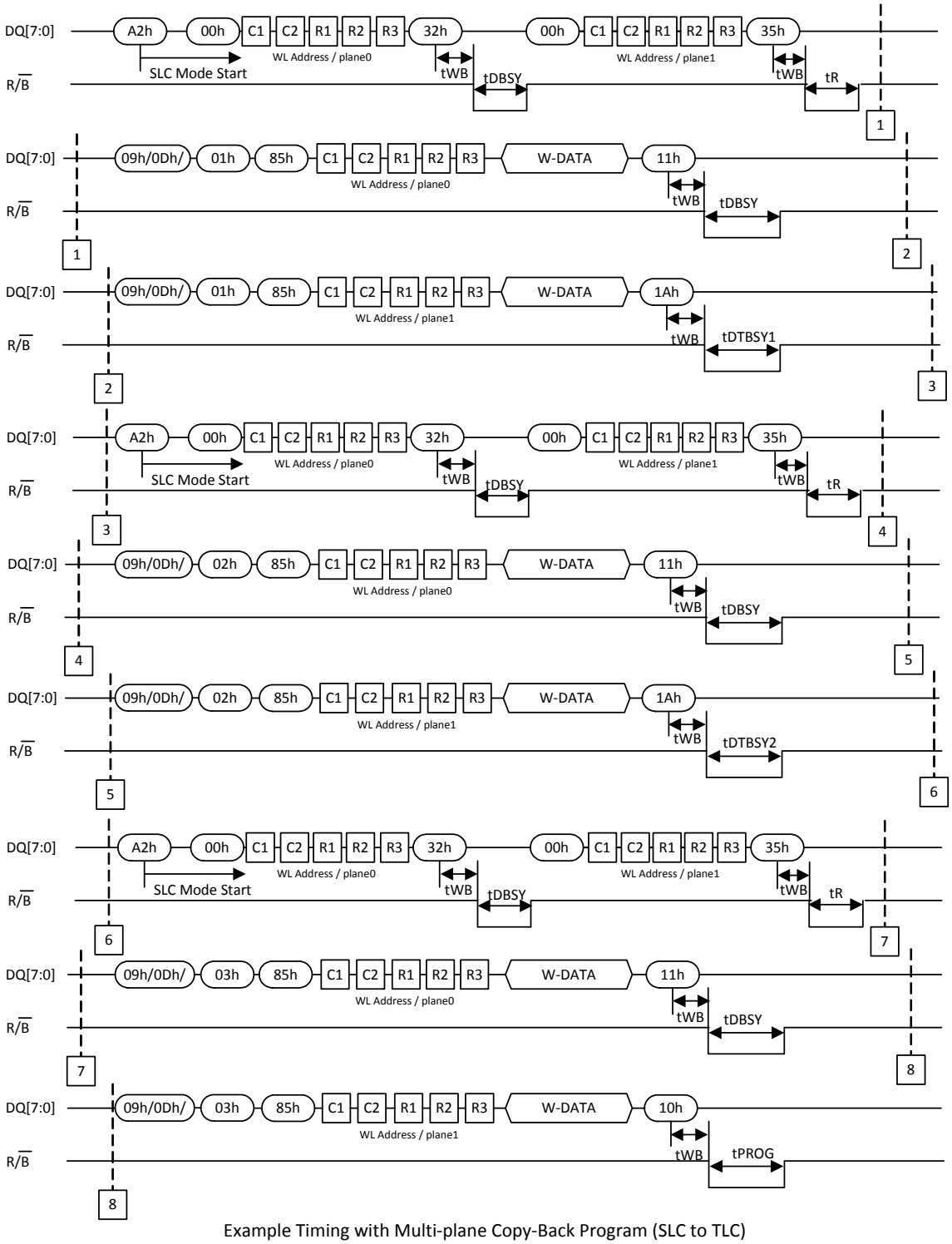
Multi-Plane Copy-Back Program is an extension of Copy-Back Program, for a single plane with 18,432 byte page registers. Since the device is equipped with two memory planes, activating the two sets of 18,432 byte page registers enables a simultaneous programming of two pages. Figure of "*Multi plane Copy-back program(I)*" and Figure of "*Multi plane Copy-back program(II)*" show command sequence for the multi-plane copy-back operation. First case, Figure of "*Multi plane Copy-back program(I)*", shows random data input of two planes that started right after finishing random data output of previous two planes. Second case, Figure of "*Multi plane Copy-back program(II)*", shows the random data input of each plane which started right after finishing the random data output of each plane.

Figure 4-24. Multi plane Copy-back program(SLC to SLC)



Example Timing with Multi-plane Copy-Back Program (SLC to SLC)

Figure 4-25. Multi plane Copy-back program (SLC to TLC)



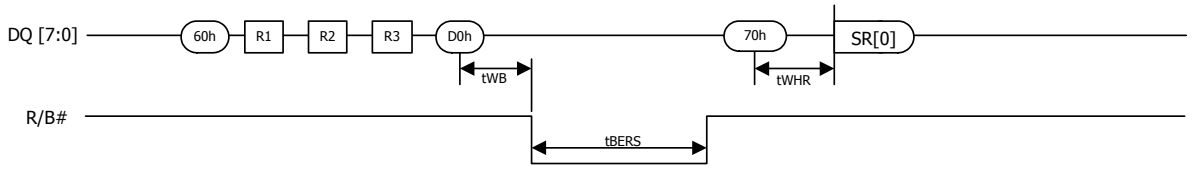
Example Timing with Multi-plane Copy-Back Program (SLC to TLC)

4.14. Block Erase

The Erase operation is done on a block basis. Block address loading is accomplished in two cycles initiated by an Erase Setup command (60h). Only address pland address(R1-0) and block address(R1-1 to R2-4) is valid. The Erase Confirm command (D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.

At the rising edge of $\overline{WE}$ after the erase confirm command input, the internal write controller handles erase and erase verify. Once the erase process starts, the Read Status Register command may be entered to read the status register.
The system controller can detect the completion of an erase by monitoring the R/B# output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while erasing is in progress. When the erase operation is completed, the Write Status Bit (I/O 0) may be checked.

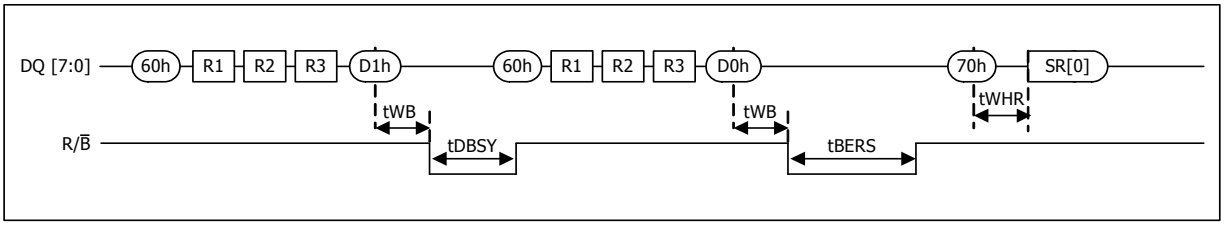
Figure 4-26. Block Erase



4.15. Multi Plane Block Erase

Multiple plane erase, allows parallel erase of two blocks, one per each memory plane.
Block erase setup command (60h) must be repeated two times, each time followed by first block and second block address respectively (3 cycles each). As for block erase, D0h command makes embedded operation start. Address limitation required for Multiple Plane Program applies also to multiple plane erase, as well as operation progress can be checked like for Multiple Plane Program. Refer to the detail sequence as shown below.

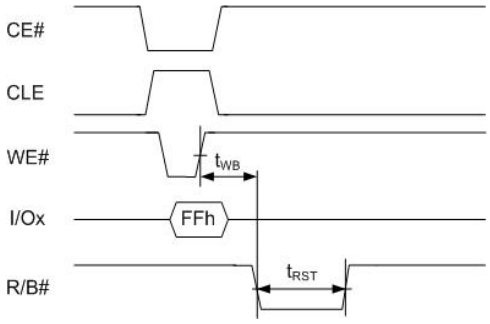
Figure 4-27. Multi plane Block Erase



4.16. Reset

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value E0h when WP is high. Refer to "2.8. Status Register Coding" for device status after reset operation. If the device is already in reset state, the command register will not accept a new reset command. The R/B pin goes low for tRST after the Reset command is written. Refer to Figure of "*Reset*".

Figure 4-28. Reset

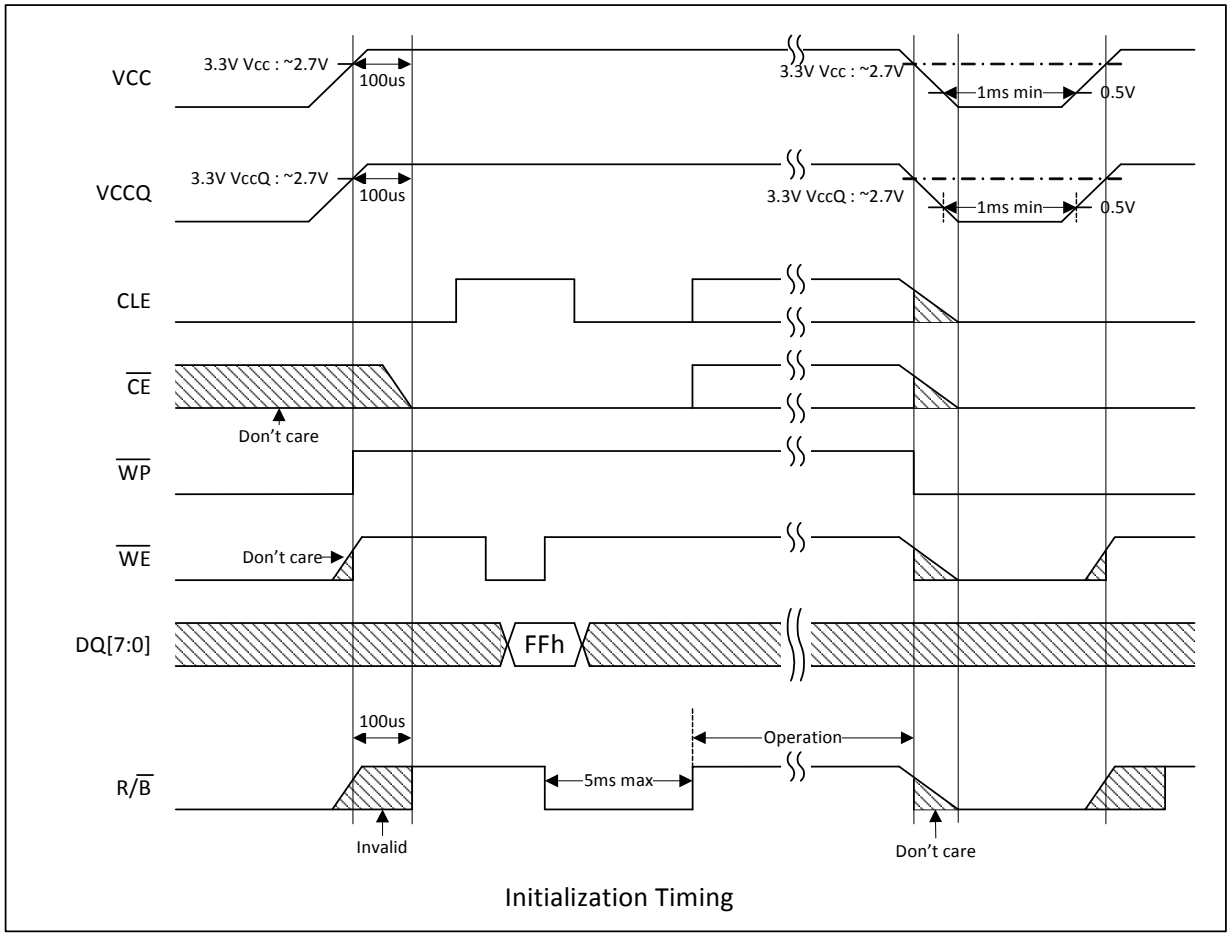


5. Other Features

5.1. Data Protection & Power on/off Sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever VCC is below about 2.0V (3.3V device). $\overline{WP}$ pin provides hardware protection and is recommended to be kept at VIL during power-up and power-down.
The reset command (FFh) must be issued to all dies as the first command after device is power up. Each R/$\overline{B}$ will be busy for maximum of 2ms after reset command is issued. In this time, the acceptable command is 70h or 78h or 75h.

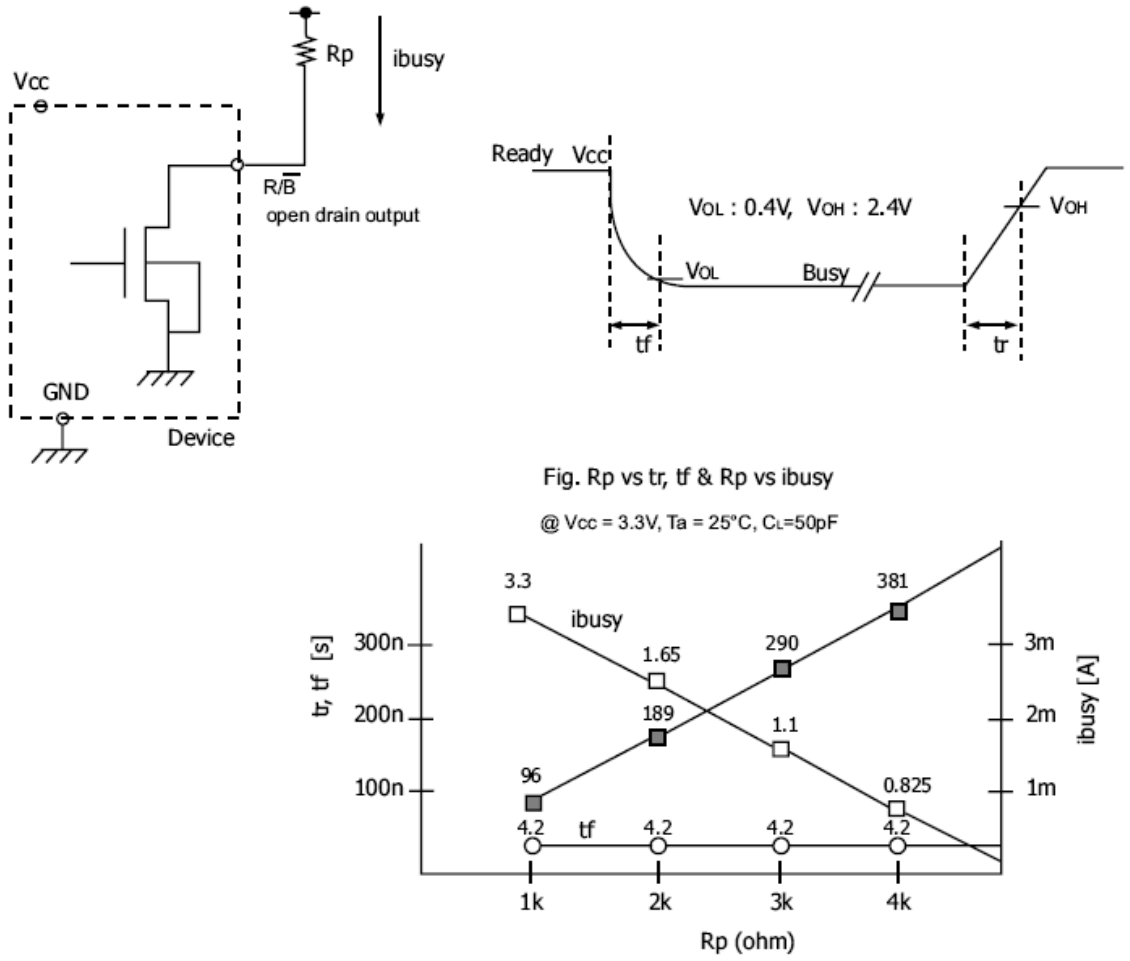
Figure 5-1. Data protection and power on / off



5.2. Ready / Busy

The device has a Ready/Busy output that provides method of indicating the completion of a page program, erase, copy-back and random read completion. The R/B pin is normally high and goes to low when the device is busy (after a reset, read, program, and erase operation). It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/B outputs to be Or-tied. Because pull-up resistor value is related to t_R (R/B) and current drain during busy (Ibusy), an appropriate value can be obtained with the following reference chart (Figure of "*Ready / Busy*"). Its value can be determined by the following guidance.

Figure 5-2. Ready / Busy



Rp value guidence

$$Rp\ (min) = \frac{Vcc\ (Max.) - V_{OL}\ (Max.)}{I_{OL} + \sum I_L} = \frac{3.2V}{8mA + \sum I_L}$$

where IL is the sum of the input currnts of all devices tied to the R/B pin.

Rp(max) is determined by maximum permissible limit of tr

5.3. Write Protect Operation

The Erase and Program Operations are automatically reset when $\overline{WP}$ goes Low (tWW = 100ns, min). The operations are enabled and disabled as follows.

Figure 5-3. Enable and Disable Programming

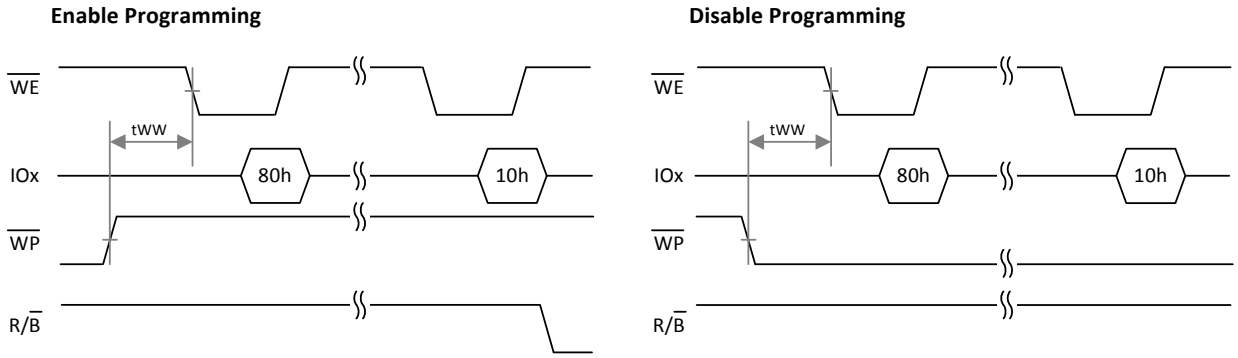
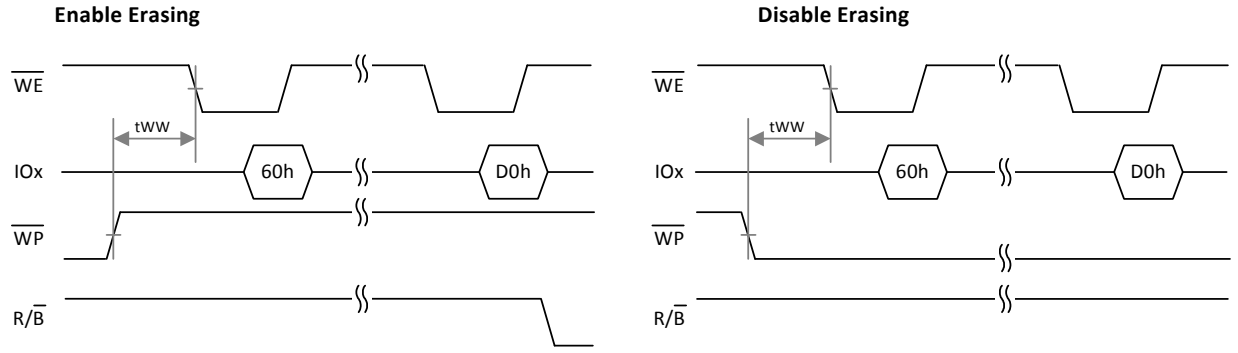


Figure 5-4. Enable and Disable Erasing



128Gb Based NAND Flash
Addendum

1. Command Description

1.1. Set Parameter

1.1.1. Command Sequence

Command Cycle	N x Parameter Input Cycle	Command Cycle	Required Time before Next Operation
36h	N x (address cycle + data input cycle)	16h	tSPARAM

1.1.2. Timing Diagram

Figure 1. Set Parameter for SDR

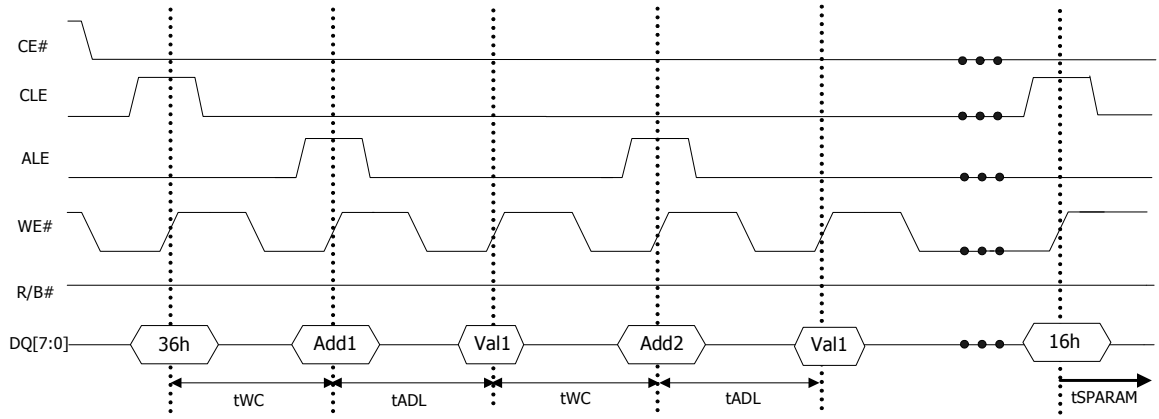
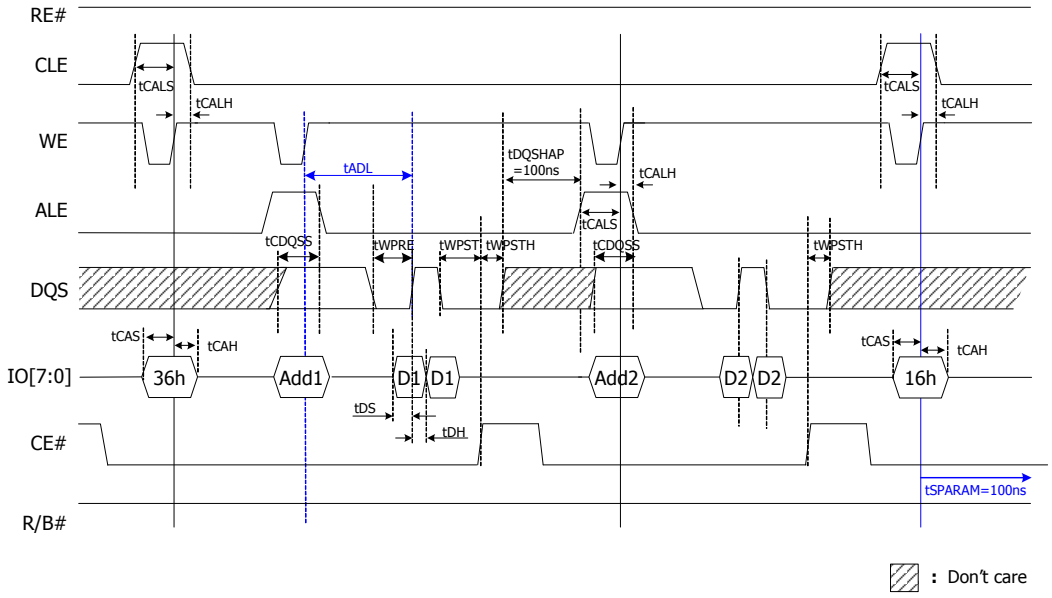


Figure 2. Set Parameter for DDR mode



1.1.3. Rules and Limitations

- In case the same parameter is given more than once, only the last update is valid.
- (Backward Compatibility) It is possible to insert a dummy address latch cycle after the Set Parameter setup command (36h).

1.2. Get Parameter

1.2.1. Command Sequence

Command Cycle	Required Time before First Parameter Output Cycle	N x Parameter Output Cycle
37h	tRPARAM	N x (address cycle + data output cycle)

Figure 3. Get Parameter for SDR

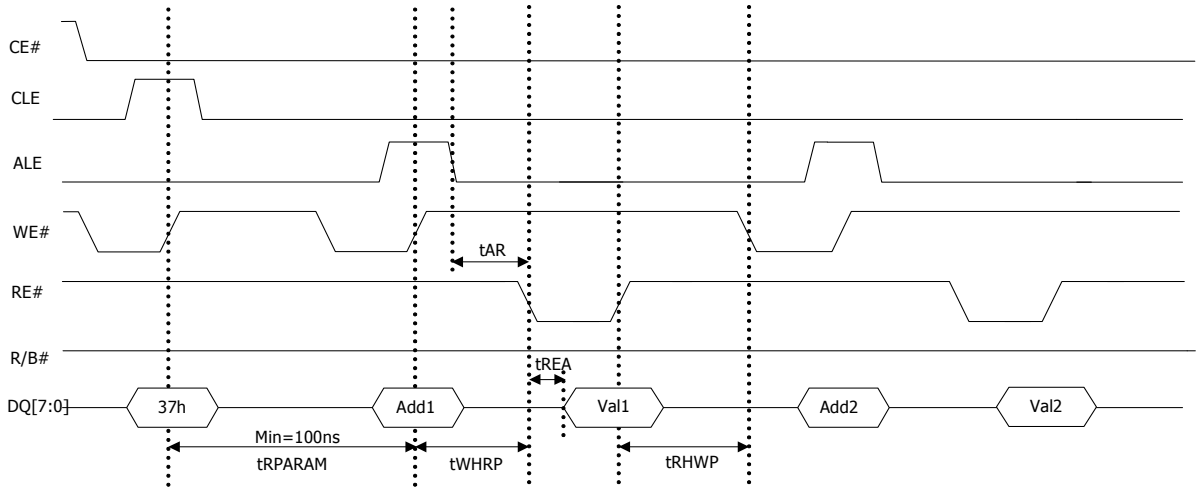
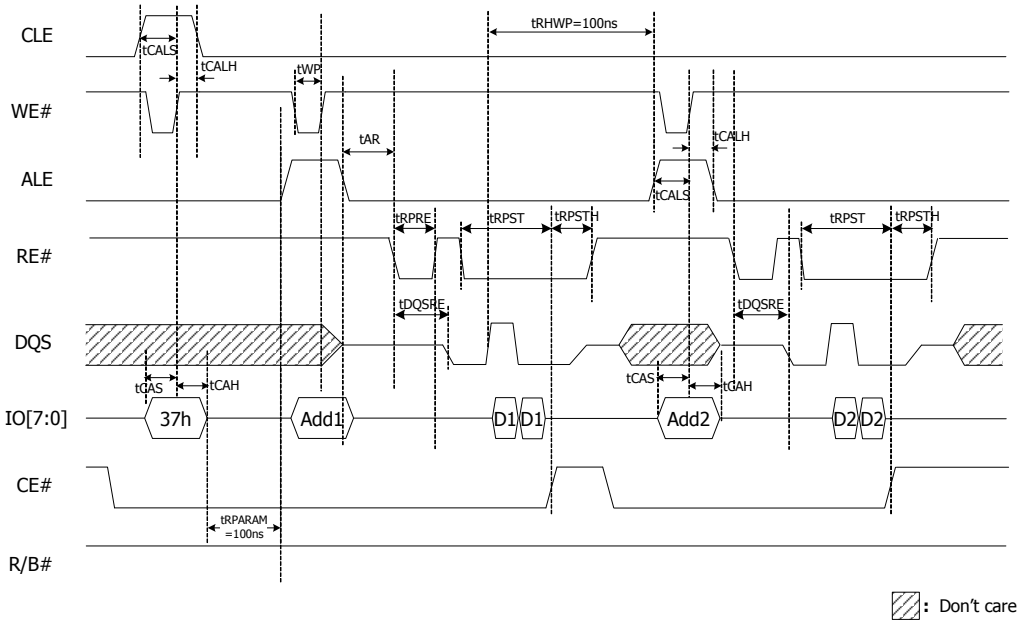


Figure 4. Get Parameter for DDR mode



1.2.3. Rules and Limitations

- When get parameter command is performed immediately after set parameter command, the parameters which are represented by shadow register are invalid. The parameters are valid after running internal algorithm.
- When the device is in internal busy state, the device is not allowed to execute get parameter command.