Started on	Tuesday, 26 October 2021, 2:33 PM
State	Finished
Completed on	Tuesday, 26 October 2021, 4:00 PM
Time taken	1 hour 26 mins
Grade	Not yet graded

Question 1
Correct
Mark 2 out of 2

Identify the instruction from the given options that exactly matches to the given microinstructions shown in the Figure. 2

Micro - instruction	..	PC_{in}	PC_{out}	MAR_{in}	Read	MDR_{out}	IR_{in}	Y_{in}	Select	Add	Z_{in}	Z_{out}	$R1_{out}$	$R1_{in}$	$R3_{out}$	WMFC	End
1		0	1	1	1	0	0	0	1	1	1	0	0	0	0	0	0
2		1	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0
3		0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0
4		0	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0
5		0	0	0	0	0	0	1	0	0	0	0	1	0	0	1	0
6		0	0	0	0	1	0	0	0	1	1	0	0	0	0	0	0
7		0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1

Figure.2

(2 marks – [U/C, 2])

- A. Add (R3), R1
- B. Mov (R1),R2
- C. Sub R1,R2,R3
- D. Add R1,LocA

The correct answer is: Add (R3), R1

Question 2
Complete
Marked out of 3

The three bus organization of the data path is shown in the Figure.1

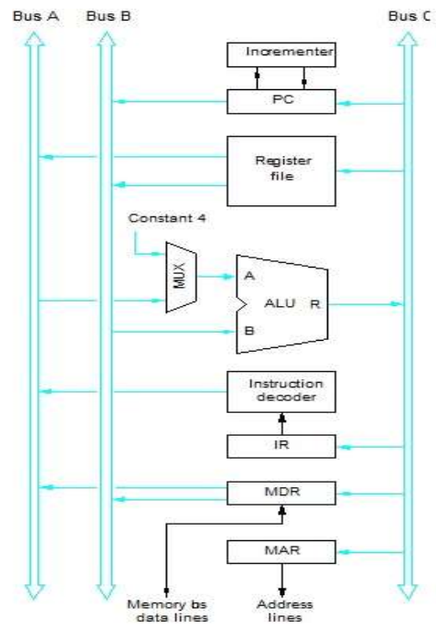


Figure . 1

Generate the control signals for the given instruction by referring the above diagram

ADD R4, R5, R6 // R6 ß R4+R5

[Add the content of Register R4 with the content of Register R5 and stores the result in Reigster R6]

(3 marks – [An/C, 2])

1. PCout, R = B, MARin, Read, IncPc
2. WMFC
3. MDRoutB, R = B, IRin

4. R4outA, R5outB, SelectA, Add, R6in, END

Question **3**

Complete

Marked out of 3

Consider the instruction

Sub (R3), R1

Adds the content of memory location pointed by R3 to Register R1]

Executing the above instruction requires the following actions:

Fetch the instruction

Fetch the first operand (the contents of the memory location pointed to by R3)

Perform the addition with R1

Load the result into R1

Select the control signals form the given table whics exactly matches against each actions [A,B,C & D]

Control Signals
MDR_{out},IR_{in}
Z_{out}, PC_{in}, Y_{in},WMFC
$R1_{out}$,Y_{in},WMFC
PC_{out} , MAR_{in} , Read, Select 4, Sub, Z_{in}
Z_{out},$R1_{in}$,End
$R3_{out}$,MAR_{in},Read
MDR_{out},Select Y,Add,Z_{in}

(3 marks – [An/C, 2])

Control Signals:

- PCout, MARin, Read, Select 4, Sub Zin
- Zout, PCin, Yin, WMFC.
- MDRout, IRin
- R3out, MARin, Read
- R1out, Yin, WMFC.
- MDRout, Select Y, ADD, Zin
- Zout, R1in, End

Question **4**

Complete

Marked out of 2

The four stage pipeline involved in the execution of instruction is shown in Figure.3

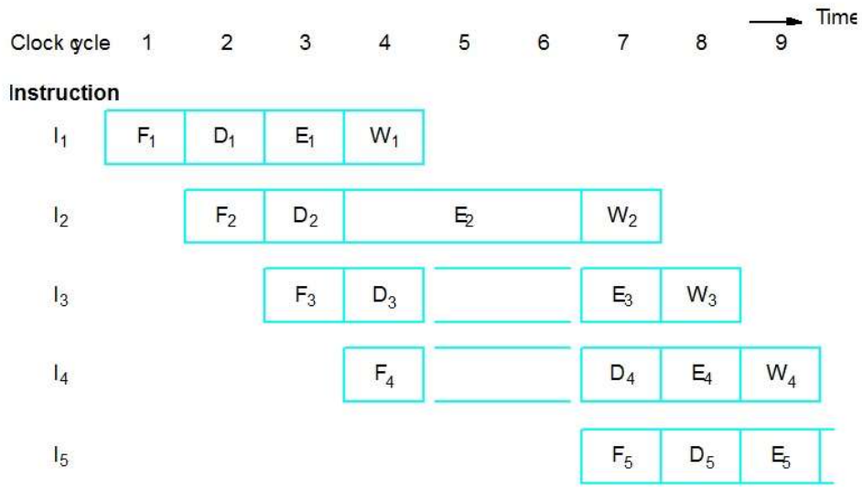


Figure.3

Provide the hardware implantation for the above diagram.

(2 marks – [U/C , 2])

Any text entered here will be displayed in the response input box when a new attempt at the question starts.

ca.4.pdf

Question 5
Complete
Marked out of 3

Consider the given instructions and answer the following questions

I1 : Add R1,R2,R3

I2 : Sub R4,R1,R6

Executing the above instructions using pipelining will cause a hazard – True/False.

Show the execution of above instructions using pipeline Timing diagram.

(1+2 marks- [An/C, 2])

True: The above instructions will cause the data hazard.

IF	**I1**	**I2**				
ID		ADD	SUB			
DF			R2, R3	**R1, R6**		
EX				R2 + R3	**R1 - R6**	
NR					R1 - RESULT	**R4 RESULT**
	1	2	3	4	5	6

Question **6**

Partially correct

Mark 1 out of 2

Identify the Figures 4 & 5 related to type of interrupts by referring the given options.

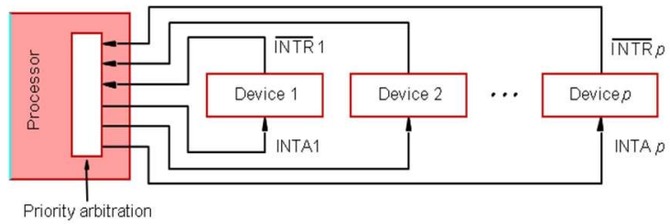


Figure. 4

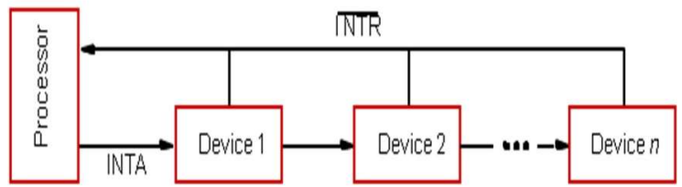


Figure.5

(2 marks- [U/C, 2])

- [ ] A. Single bus structure
- [ ] B. Centralized bus arbitration structure
- [ ] C. Distributed bus arbitration structure
- [x] D. Priority structure
- [x] E. Daisy chain structure

The correct answers are: Priority structure, Distributed bus arbitration structure

Question 7
Complete
Marked out of 3

Consider the given diagram of Direct Memory Access (DMA) shown in Figure. 7 which is used to transfer of a block of data directly b/w an external device & main-memory and State whether the given statements are True/False.

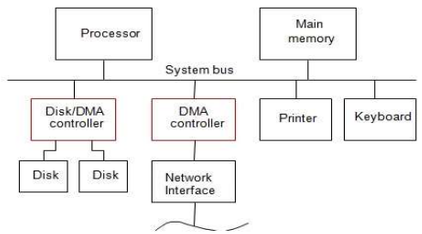


Figure. 7

Statement 1 : DMA controller performs the functions that would normally be carried out by processor

Statement 2 : In Cycle stealing, DMA controller is given exclusive access to main-memory to transfer a block of data without any interruption.

Statement 3 : More than one I/O devices may be attached with one DMA controller.

Statement 4 : DMA controller cannot transfer a block of data from an external device to the processor.

Statement 5 : Processor and DMA controllers have to use the bus in an interwoven fashion to access the memory

(3 marks- [An/C, 2])

- Statement 1: True
- Statement 2: False
- Statement 3: True
- Statement 4: False
- Statement 5: True

Question 8
Complete
Marked out of 4

The standard I/O interface circuit of a computer system is shown in the Figure 8.

(4 marks- [U/C, 2])

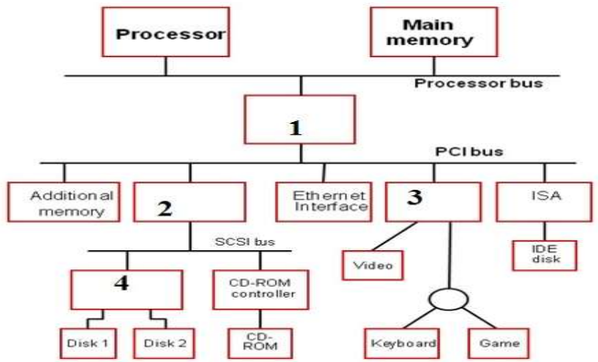


Figure. 8

Identify the missing parts [1-4] in the given diagram related to standard I/O interface circuit of a computer system.

Map the following statements against each standard I/O interfaces

PCI

SCSI

USB

Statements
It uses a serial transmission to suit the needs of equipment ranging from keyboard to game control to internal connection
It is developed as a low cost bus that is truly processor independent
It has plug and play capability for connecting I/O devices
The burst of data are transferred at high speed

1. Bridge
2. SCSI Controller
3. USB Controller
4. Disk controller

- **PCI->** It is developed as a low-cost bus that is truly processor-independent. It has plug and play capability for connecting I/O devices.
- **USB ->** It uses a serial transmission to suit the needs of equipment ranging from keyboard to game control to internal connection.
- **SCSI->** The burst of data are transferred at high speed.

Question 9
Complete
Marked out of 4

The timing diagram related to read operation of the PCI bus is shown in the Figure.9. Provide the functions of each data transfer signals shown in the timing diagram.

(4 marks- [U/C, 2])

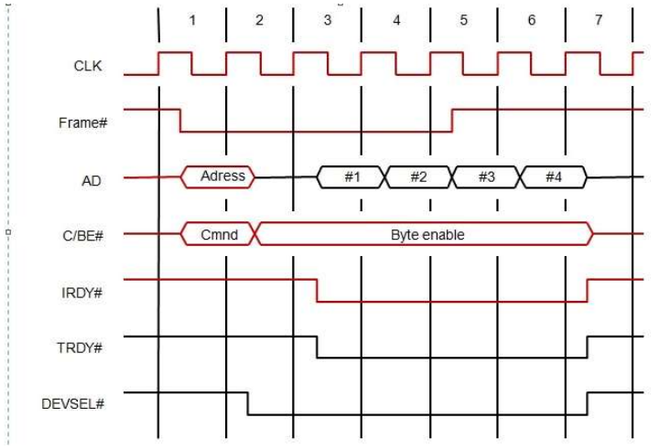


Figure.9

S.No	Name	Function
1	TRDY#	
2	FRAME#	
3	AD	
4	C/BE#	
5	DEVSEL#	

S.NO	NAME	FUNCTION
1	TRDY#	Ready signal from target

S.NO	NAME	FUNCTION
2	FRAME#	Indicates start of bus cycle
3	AD	Address/ Data bus
4	C/BE#	Bus command(address phase) Byte enables(data phase)
5	DEVSEL#	Address recongnized

Question 10
Complete
Marked out of 4

A block-set-associative cache consists of a total of 64 blocks, divided into 4-block sets. The main- memory contains 4096 blocks, each consisting of 32 words. Assuming a 32-bit byte-addressable address-space.

(a) How many bits are there in main-memory address?

(b) How many bits are there in each of the Tag, Set, and Word fields?

(2+2 marks- [An/C,2])

Assume 1 word = 1 Byte (as nothing is mention)

so Block size = 32 word = 32 Byte = 5 bits

so Block offset = 5 bits

No of blocks in cache memory = 64 and cache is 4 ways set associative

so No of sets = 64block / 4 ways = 16 sets

So Set number bits = 4 bit

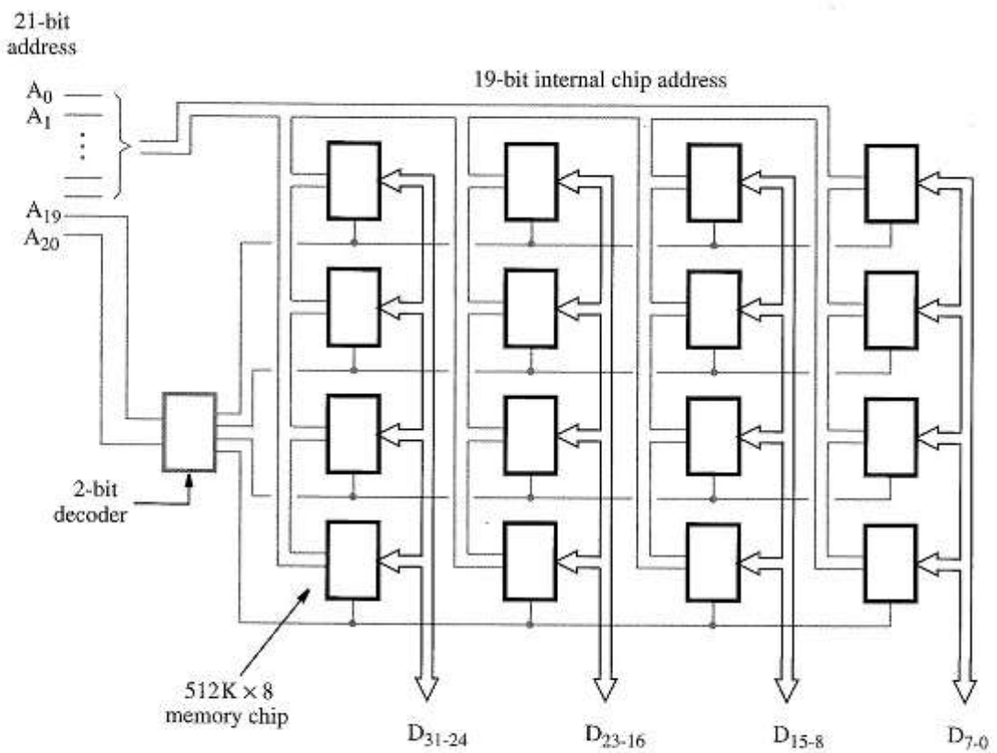
Main memory size = No of block * block size = 4096 * 32 Bytes = 128 KB = 17 bits

so Tag bits = 17 – (set bits + Block offset bits)= 17- 9 = 8 bits

Question 11
Complete
Marked out of 4

The organization of 2M X 32 memory module using 512K X 8 static memory chips is shown in the figure.11. By referring this diagram, provide the necessary changes to be done for the organization of 8M X 32 memory system using 512K X 8 static memory chips.

(4 marks- [Ap/C,2])



The Necessary changes are,

No.of.Memory chips required will be changed from 8M X 32 / 512K X 8=64

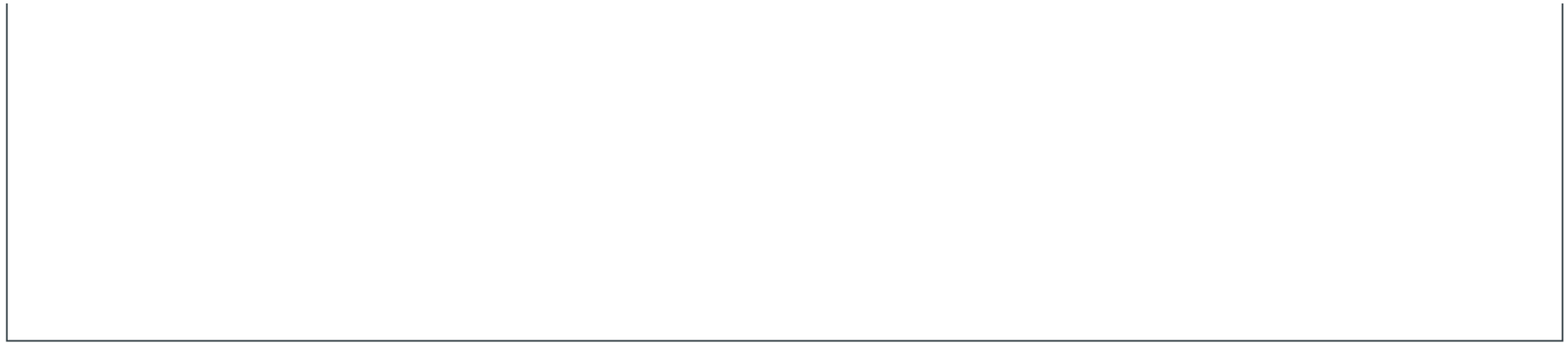
Arrangement changes to 8 rows and 8 columns

Question 12
Not answered
Marked out of 4

A Tape drive has the following parameters:
(4 marks- [An/C,2])

S.No	Parameters	Units
1	Bit density	1600 bits/cm
2	Tape Speed	200 cm/sec
3	Minimum Time spent at an interrecord gap	3 ms
4	Average record Length	1000 characters

Find how many bytes can be stored on a tape reel of length 1200 ft written on such drive.



Question 13
Not answered
Marked out of 6

A virtual memory address translation method based on the concept of fixed length page is shown in the Figure. 12.

(6 marks- [Ap/C,2])

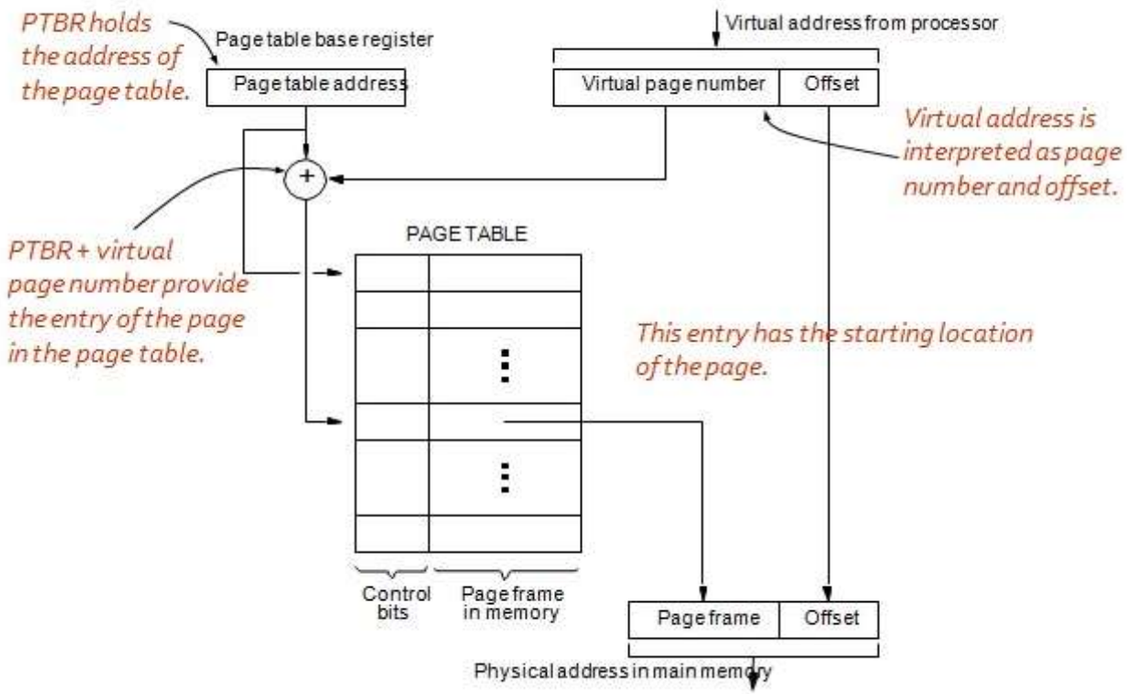


Figure.12

Provide a design a possible organization of a TLB using Associative Mapping technique, if a small cache called the Translation Lookaside Buffer(TLB) is incorporated into Memory Mangament Unit (MMU) .

Question **14**
Complete
Marked out of 6

A simple processor has the following specification:

(3+3 marks – [Ap/C, 2])

Total size of cache is 2048 (2K) words.

Cache consisting of 128 blocks of 16 words each.

Main memory has 64K words.

Main memory has 4K blocks of 16 words each.

Determine how memory blocks are placed in the cache using

Direct Mapping

b. Associative Mapping

DIRECT MAPPING:

1)The simplest way to determine cache locations in which store Memory blocks is direct Mapping technique.

2) In this block J of the main memory maps on to block J modulo 128 of the cache. Thus main memory blocks 0,128,256,….is loaded into cache is stored at block 0. Block 1,129,257,….are stored at block 1 and so on.

3) Placement of a block in the cache is determined from memory address. Memory address is divided into 3 fields, the lower 4-bits selects one of the 16 words in a block.

4) When new block enters the cache, the 7-bit cache block field determines the cache positions in which this block must be stored.

5) The higher order 5-bits of the memory address of the block are stored in 5 tag bits associated with its location in cache. They identify which of the 32 blocks that are mapped into this cache position are currently resident in the cache.

6) It is easy to implement, but not Flexible

ASSOCIATIVE MAPPING:

1) This is more flexible mapping method, in which main memory block can be placed into any cache block position.

2) In this, 12 tag bits are required to identify a memory block when it is resident in the cache.

3) The tag bits of an address recevied from the processor are compared to the tag bits of each block of the cache to see, if the desired block is present. This is known as Associative Mapping technique.

4) Cost of an associated mapped cache is higher than the cost of direct-mapped because of the need to search all 128 tag patterns to determine whether a block is in cache. This is known as associative search.

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