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Module- 4 (Interfacing chips):

Programmable Peripheral Input/output port 8255 - Architecture and modes of operation- Programmable interval timer 8254-Architecture and modes of operation- DMA controller 8257 Architecture (Just mention the control word, no need to memorize the control word of 8254 and 8257)

I. Programmable Peripheral Input/output port 8255 8255 - Architecture and modes of operation

8255 is a programmable peripheral interface, which means it is a programmable device used to interface I/O devices with the processor. In reality, we are not supposed to connect I/O devices directly with the data bus of the processor, instead there should be some device to which I/O ports should be there to connect I/O devices.

- It has 3 8-bit ports, all ports are bidirectional (Can be used as Input port or output port). They are Port – A (PA) and PB, PC. Port A contains one 8-bit output latch/buffer and one 8-bit input buffer.
- Port B is similar to PORT A.
- Port C can be split into two parts, i.e. PORT C lower (PC0-PC3) and PORT C upper (PC7-PC4) by the control word.

These three ports are further divided into two groups, i.e. Group A includes PORT A and upper PORT C. Group B includes PORT B and lower PORT C. These two groups can be programmed in three different modes, i.e. the first mode is named as mode 0, the second mode is named as Mode 1 and the third mode is named as Mode 2.

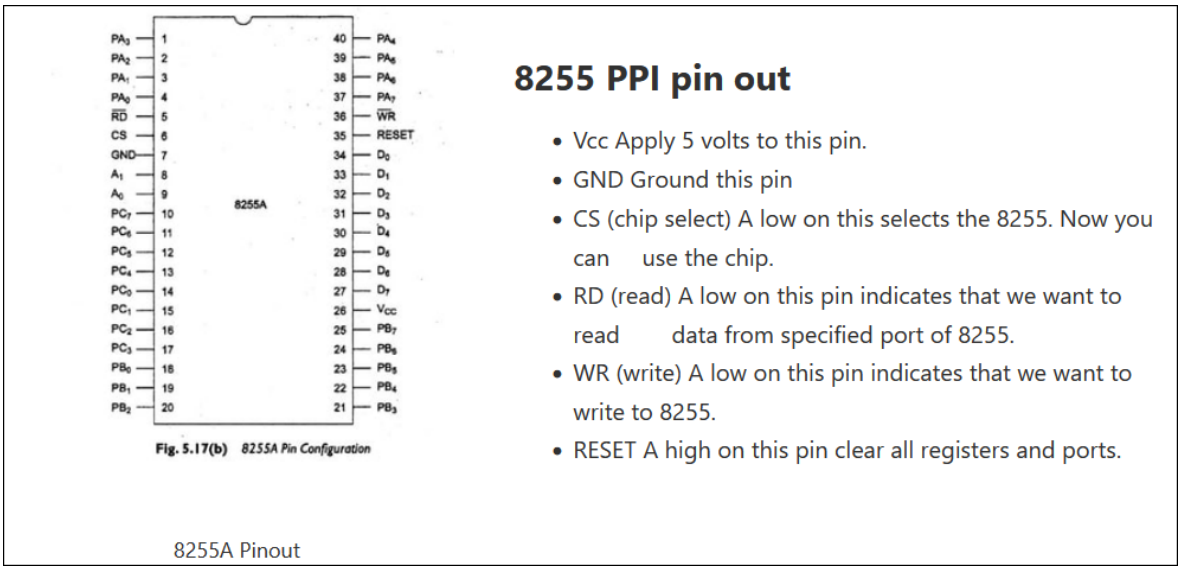
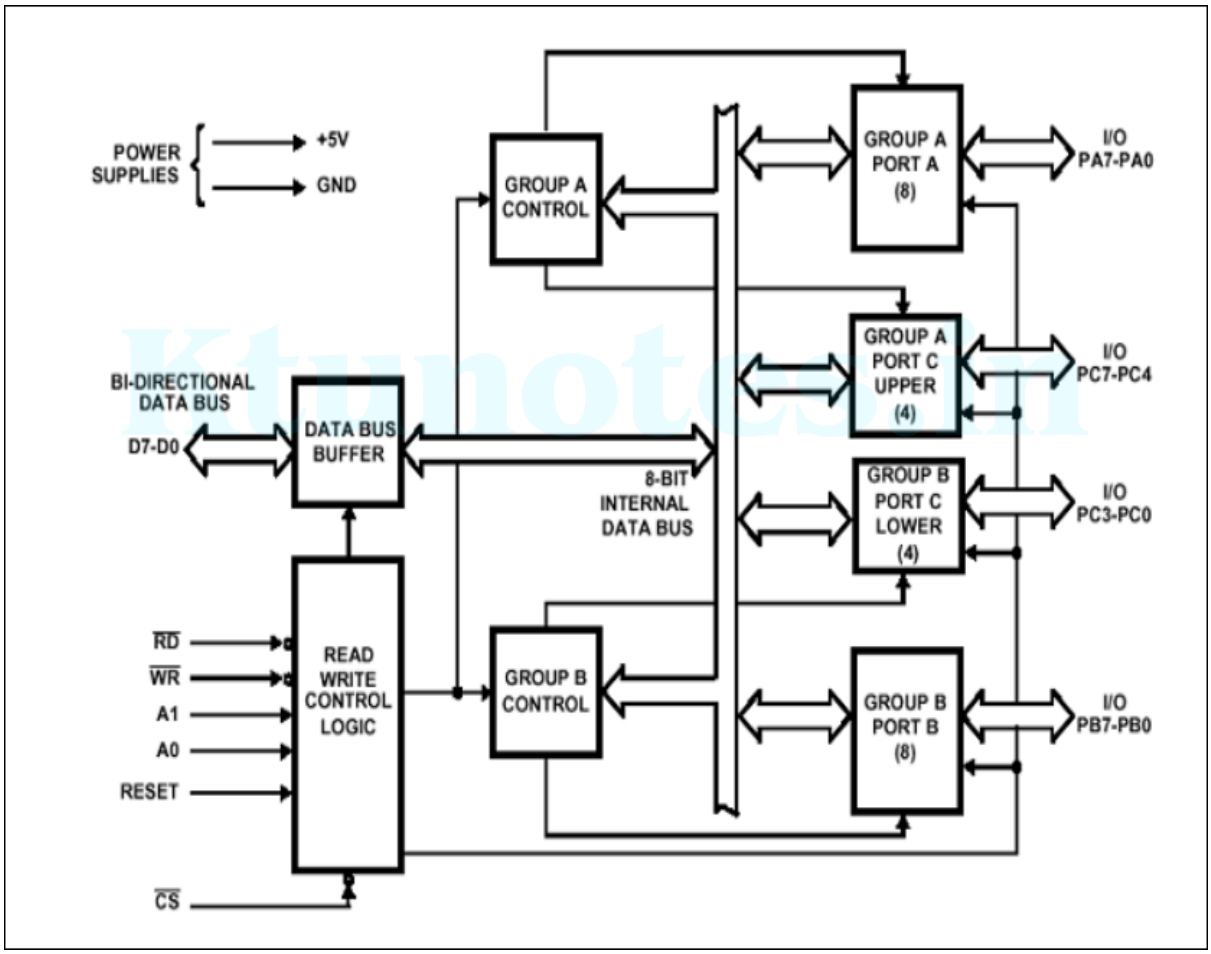


Fig. 5.17(b) 8255A Pin Configuration

8255A Pinout

Architecture

It has 24 input/output lines which may be individually programmed in two groups of twelve lines each, or three groups of eight lines. The two groups of I/O pins are named as Group A and Group B. Each of these two groups contains a subgroup of eight I/O lines called as 8-bit port and another subgroup of four lines or a 4-bit port.



Thus, Group A contains an 8-bit port A along with a 4-bit port. C upper. The port A lines are identified by symbols PA0-PA7 while the port C lines are identified as PC4-PC7. Similarly, Group B contains an 8-bit port B, containing lines PB0-PB7 and a 4-bit port C with lower bits PC0- PC3. The port C upper and port C lower can be used in combination as an 8-bit port C. Both the port C are assigned the same address. Thus, one may have either three 8-bit I/O ports

or two 8-bit and two 4-bit ports from 8255. All of these ports can function independently either as input or as output ports. This can be achieved by programming the bits of an internal register of 8255 called as control word register (CWR). This buffer receives or transmits data upon the execution of input or output instructions by the microprocessor. The control words or status information is also transferred through the buffer.

Functional Descriptions

Data Bus Buffer

It is a tri-state 8-bit buffer, which is used to interface the microprocessor to the system data bus. Data is transmitted or received by the buffer as per the instructions by the CPU. Control words and status information is also transferred using this bus.

Read/Write Control Logic

This block is responsible for controlling the internal/external transfer of data/control/status word. It accepts the input from the CPU address and control buses, and in turn issues command to both the control groups.

CS

It stands for Chip Select. A LOW on this input selects the chip and enables the communication between the 8255A and the CPU. It is connected to the decoded address, and A0 & A1 are connected to the microprocessor address lines.

Their result depends on the following conditions −

CS	A_1	A_0	Result
0	0	0	PORT A
0	0	1	PORT B
0	1	0	PORT C
0	1	1	Control Register

1 X X No Selection

WR

It stands for write. This control signal enables the write operation. When this signal goes low, the microprocessor writes into a selected I/O port or control register.

RESET

This is an active high signal. It clears the control register and sets all ports in the input mode.

RD

It stands for Read. This control signal enables the Read operation. When the signal is low, the microprocessor reads the data from the selected I/O port of the 8255.

A0 and A1

These input signals work with RD, WR, and one of the control signals. Following is the table showing their various signals with their result.

A_1	A_0	RD	WR	CS	Result
0	0	0	1	0	**Input Operation** PORT A → Data Bus
0	1	0	1	0	PORT B → Data Bus
1	0	0	1	0	PORT C → Data Bus
0	0	1	0	0	**Output Operation** Data Bus → PORT A
0	1	1	0	0	Data Bus → PORT A
1	0	1	0	0	Data Bus → PORT B
1	1	1	0	0	Data Bus → PORT D

Modes of Operation

8255A has three different operating modes –

1. **INPUT/OUTPUT MODE**

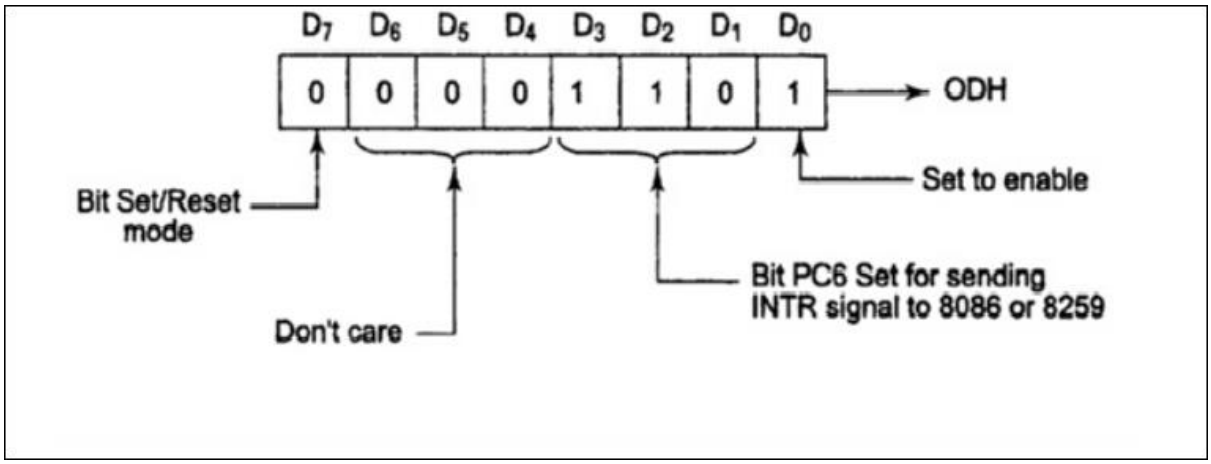
There are three basic modes of operation than can be selected by the system software:

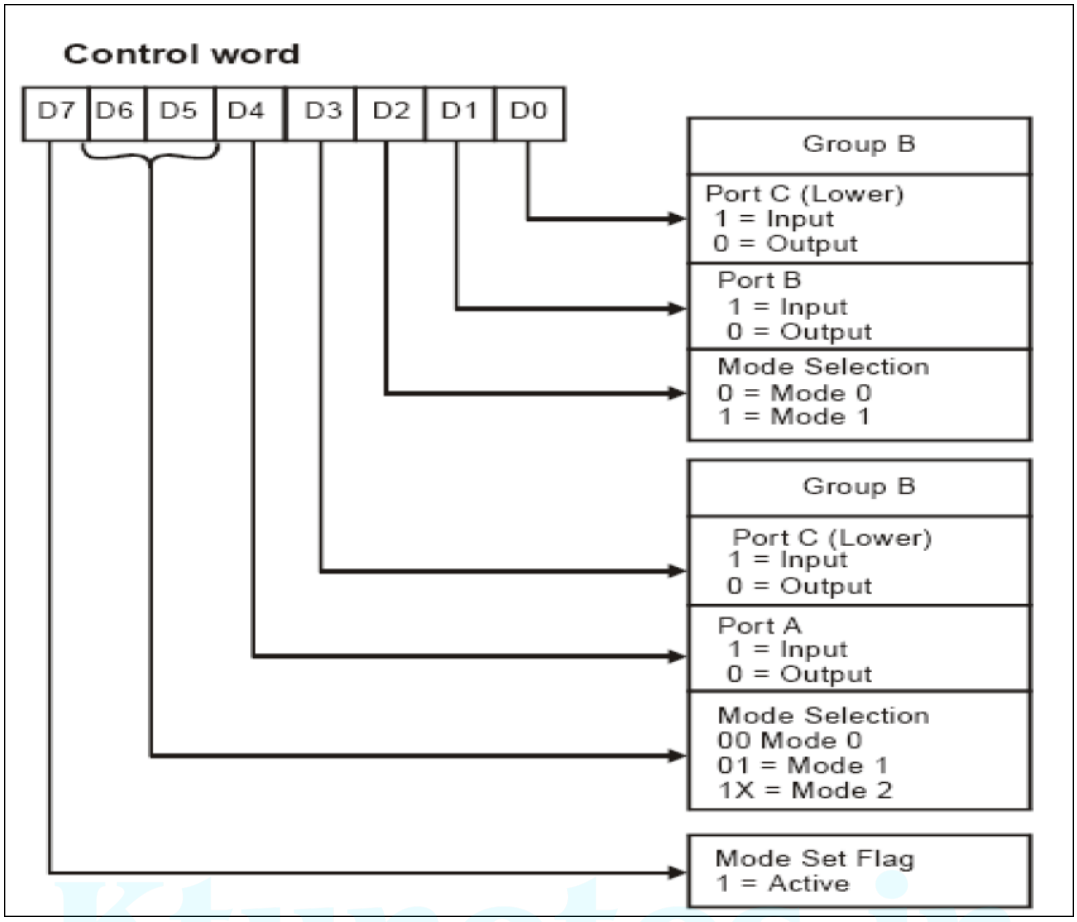
- **Mode 0 -Basic Input/Output**
- **Mode 1 -Strobed Input/Output**
- **Mode 2 -Bi-directional Bus**

- **Mode 0** − In this mode, Port A and B is used as two 8-bit ports and Port C as two 4-bit ports. Each port can be programmed in either input mode or output mode where outputs are latched and inputs are not latched. Ports do not have interrupt capability.

In mode 0 each group can be used as input or output. Port A, port B and Port C can be used as input or output. Port C has the specialty that it can be divided in to two nibbles upper and lower. Both upper and lower can now be programmed to use as input or output. Mode 0 is also known as input/output mode (I/O mode). Question arises how we can do so. Yes, it's simple. Just send a control word to 8255 and it will set itself according to your control word. The control word for mode 0 is like this.

In mode 0 you can also access individual bits of port C. For bit set reset mode D7 will always be 0.



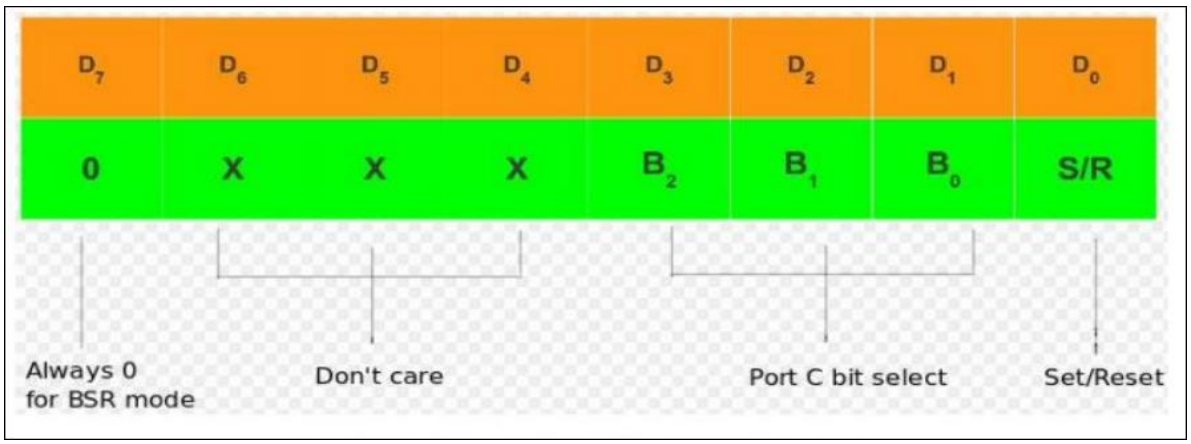


- **Mode 1** - In mode 1 each group can be used as 8-bit input or output data bus and the remaining 4-bits are used as handshaking and interrupt control signals. Port A is used with port c upper three bits and port B is used with port c lower 3 bits. The remaining 2 bits of port C can be used as control signals.
- **Mode 2** − In this mode, Port A can be configured as the bidirectional port and Port B either in Mode 0 or Mode 1. Port A uses five signals from Port C as handshake signals for data transfer. The remaining three signals from Port C can be used either as simple I/O or as handshake for port B.

2. BIT SET/RESET (BSR) MODE

In this mode only port b can be used (as an output port). Each line of port C (PC0 - PC7) can be set/reset by suitably loading the command word register.no effect occurs in input-output mode. The individual bits of port c can be set or reset by sending the signal OUT instruction to the control register.

- The figure shows the control word format in BSR mode. This mode is selected by making D7='0'.
- D0 is used for bit set/reset. When D0= '1', the port C bit selected (selection of a port C bit is shown in the next point) is SET, when D0 = '0', the port C bit is RESET.
- D1, D2, D3 are used to select a particular port C bit whose value may be altered using D0 bit as mentioned above.



II. Programmable interval timer 8254 - Architecture and modes of operation

The Intel 8253 and 8254 are Programmable Interval Timers (PTIs) designed for microprocessors to perform timing and counting functions using three 16-bit registers. Each counter has 2 input pins, i.e. Clock & Gate, and 1 pin for "OUT" output. To operate a counter, a 16-bit count is loaded in its register. On command, it begins to decrement the count until it reaches 0, then it generates a pulse that can be used to interrupt the CPU.

Difference between 8253 and 8254

The following table differentiates the features of 8253 and 8254 –

8253	8254
• Its operating frequency is 0 - 2.6 MHz	Its operating frequency is 0 - 10 MHz
• It uses N-MOS technology	It uses H-MOS technology
• Read-Back command is not available	Read-Back command is available
• Reads and writes of the same counter cannot be interleaved.	Reads and writes of the same can be interleaved.

Features of 8253 / 54

The most prominent features of 8253/54 are as follows −

• It has three independent 16-bit down counters.

• It can handle inputs from DC to 10 MHz.

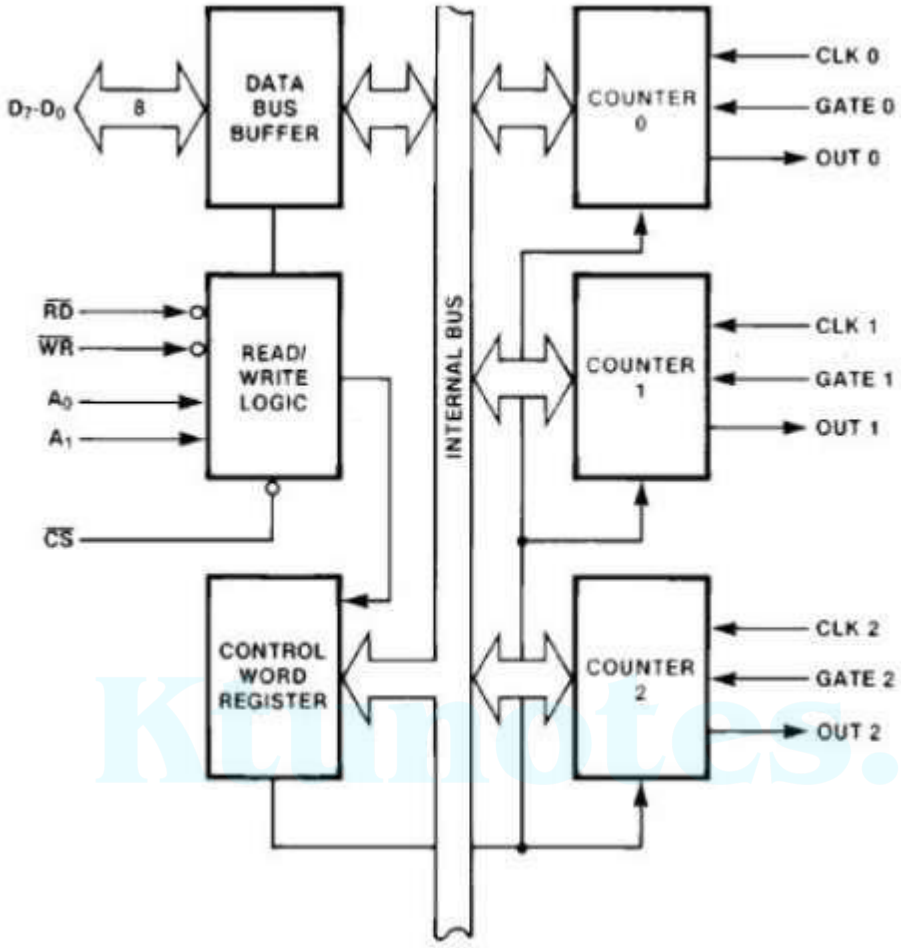
• These three counters can be programmed for either binary or BCD count.

• It is compatible with almost all microprocessors.

• 8254 has a powerful command called READ BACK command, which allows the user to check the count value, the programmed mode, the current mode, and the current status of the counter.

6.2.1 8254 Architecture

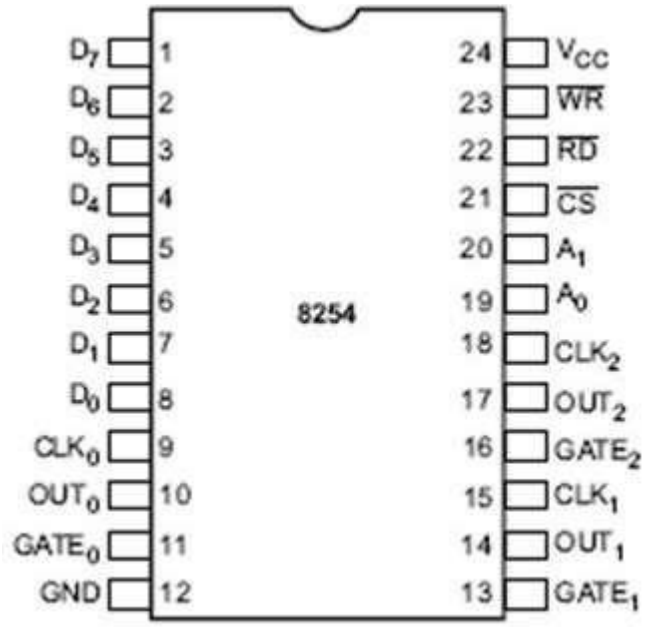
The architecture of 8254 looks as follows –



6.2.2 8254 Pin Description

Here is the pin diagram of 8254 –

In the above figure, there are three counters, a data bus buffer, Read/Write control logic, and a control register. Each counter has two input signals - CLOCK & GATE, and one output signal - OUT.



Data Bus Buffer

It is a tri-state, bi-directional, 8-bit buffer, which is used to interface the 8253/54 to the system data bus. It has three basic functions −

• Programming the modes of 8253/54.

• Loading the count registers.

• Reading the count values.

Read/Write Logic

It includes 5 signals, i.e. RD, WR, CS, and the address lines A0 & A1. In the peripheral I/O mode, the RD and WR signals are connected to IOR and IOW, respectively. In the memory mapped I/O mode, these are connected to MEMR and MEMW. Address lines A0 & A1 of the CPU are connected to lines A0 and A1 of the 8253/54, and CS is tied to a decoded address. The control word register and counters are selected according to the signals on lines A0 & A1.

A1	A0	Result
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control Word Register
X	X	No Selection

Control Word Register

This register is accessed when lines A0 & A1 are at logic 1. It is used to write a command word, which specifies the counter to be used, its mode, and either a read or write operation.

Following table shows the result for various control inputs.

A1	A0	RD	WR	CS	Result
0	0	1	0	0	Write Counter 0
0	1	1	0	0	Write Counter 1
1	0	1	0	0	Write Counter 2
1	1	1	0	0	Write Control Word
0	0	0	1	0	Read Counter 0
0	1	0	1	0	Read Counter 1
1	0	0	1	0	Read Counter 2
1	1	0	1	0	No operation
X	X	1	1	0	No operation
X	X	X	X	1	No operation

Counters

Each counter consists of a single, 16 bit-down counter, which can be operated in either binary or BCD. Its input and output are configured by the selection of modes stored in the control Word register. The programmer can read the contents of any of the three counters without disturbing the actual count in process.

6.2.3 MODES OF OPERATION

8253/54 can be operated in 6 different modes. In this chapter, we will discuss these operational modes.

i. Mode 0 ─ Interrupt on Terminal Count

It is used to generate an interrupt to the microprocessor after a certain interval. Initially the output is low after the mode is set. The output remains LOW after the count value is loaded into the counter.

The process of decrementing the counter continues till the terminal count is reached, i.e., the count become zero and the output goes HIGH and will remain high until it reloads a new count.

The GATE signal is high for normal counting. When GATE goes low, counting is terminated and the current count is latched till the GATE goes high again.

ii. Mode 1 – Programmable One Shot

It can be used as a mono stable multi-vibrator. The gate input is used as a trigger input in this mode. The output remains high until the count is loaded and a trigger is applied.

iii. Mode 2 – Rate Generator

The output is normally high after initialization. Whenever the count becomes zero, another low pulse is generated at the output and the counter will be reloaded.

iv. Mode 3 – Square Wave Generator

This mode is similar to Mode 2 except the output remains low for half of the timer period and high for the other half of the period.

v. Mode 4 − Software Triggered Mode

In this mode, the output will remain high until the timer has counted to zero, at which point the output will pulse low and then go high again. The count is latched when the GATE signal goes LOW. On the terminal count, the output goes low for one clock cycle then goes HIGH. This low pulse can be used as a strobe.

vi. Mode 5 – Hardware Triggered Mode

This mode generates a strobe in response to an externally generated signal. This mode is similar to mode 4 except that the counting is initiated by a signal at the gate input, which means it is hardware triggered instead of software triggered. After it is initialized, the output goes high. When the terminal count is reached, the output goes low for one clock cycle.

III. DMA controller 8257

Suppose any device which is connected to input-output port wants to transfer data to memory, first of all it will send input-output port address and control signal, input-output read to input-output port, then it will send memory address and memory write signal to memory where data has to be transferred. In normal input-output technique the processor becomes busy in checking whether any input-output operation is completed or not for next input-output operation, therefore this technique is slow.

DMA stands for Direct Memory Access. It is designed by Intel to transfer data at the fastest rate. It allows the device to transfer the data directly to/from memory without any interference of the CPU.

Using a DMA controller, the device requests the CPU to hold its data, address and control bus, so the device is free to transfer data directly to/from the memory. The DMA data transfer is initiated only after receiving HLDA signal from the CPU.

This problem of slow data transfer between input-output port and memory or between two memory is avoided by implementing Direct Memory Access (DMA) technique. This is faster as the microprocessor/computer is bypassed and the control of address bus and data bus is given to the DMA controller.

- HOLD – hold signal
- HLDA – hold acknowledgment
- DREQ – DMA request
- DACK – DMA acknowledgment

How DMA Operations are Performed?

Following is the sequence of operations performed by a DMA −

- Initially, when any device has to send data between the device and the memory, the device has to send DMA request (DRQ) to DMA controller.
- The DMA controller sends Hold request (HRQ) to the CPU and waits for the CPU to assert the HLDA.

- Then the microprocessor tri-states all the data bus, address bus, and control bus. The CPU leaves the control over bus and acknowledges the HOLD request through HLDA signal.
- Now the CPU is in HOLD state and the DMA controller has to manage the operations over buses between the CPU, memory, and I/O devices.

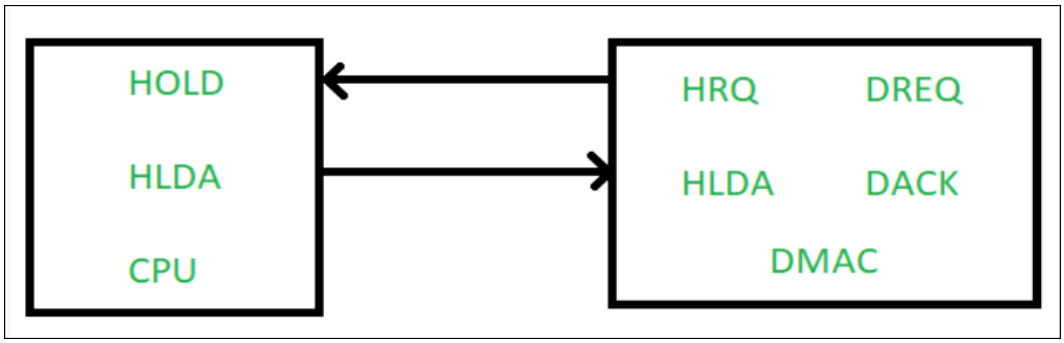
Features of 8257

Here is a list of some of the prominent features of 8257 −

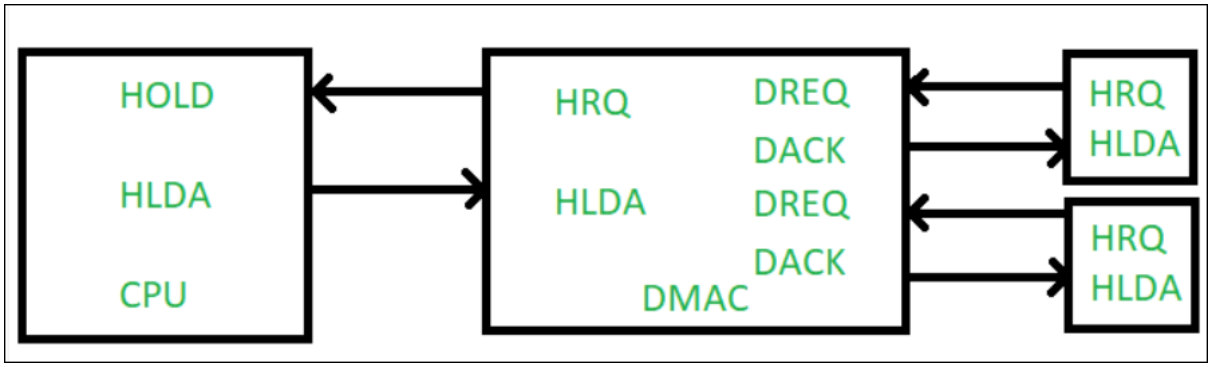
- It has four channels which can be used over four I/O devices.
- Each channel has 16-bit address and 14-bit counter.
- Each channel can transfer data up to 64kb.
- Each channel can be programmed independently.
- Each channel can perform read transfer, write transfer and verify transfer operations.
- It generates MARK signal to the peripheral device that 128 bytes have been transferred.
- It requires a single-phase clock.
- Its frequency ranges from 250Hz to 3MHz.
- It operates in 2 modes, i.e., Master mode and Slave mode.

Modes of DMAC:

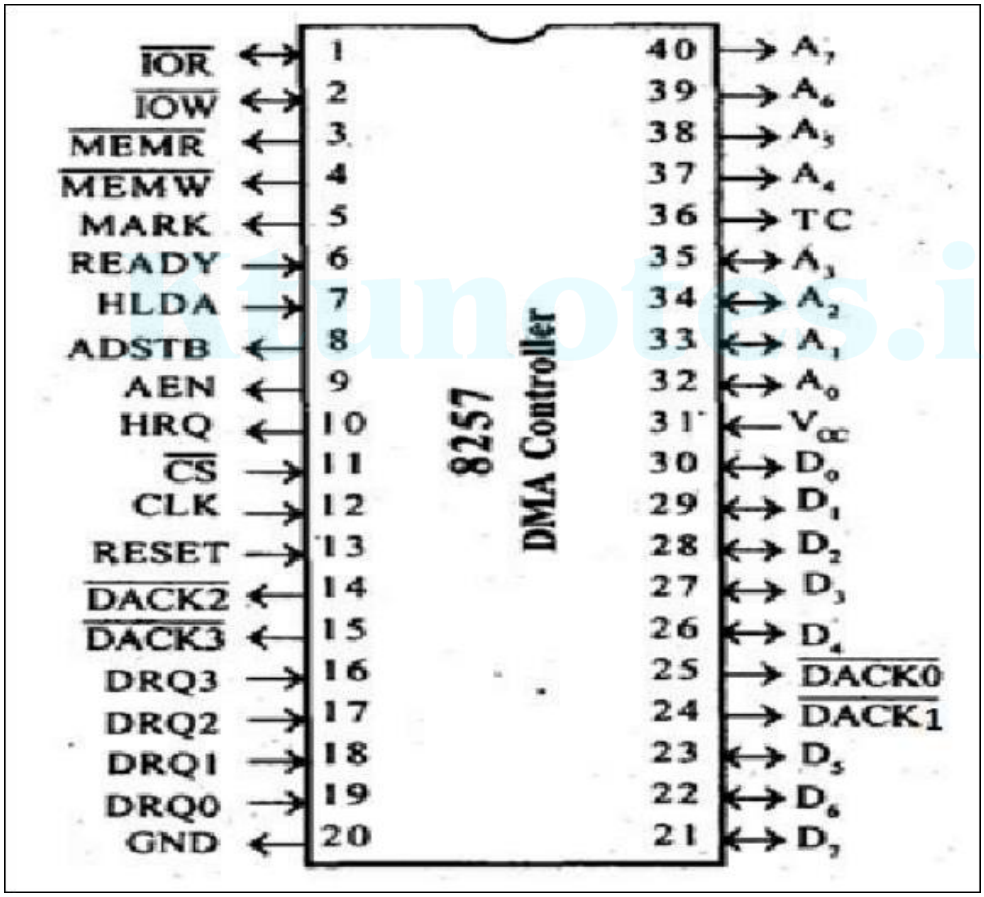
1. Single Mode – In this only one channel is used, means only a single DMAC is connected to the bus system.



2. **Cascade Mode –** In these multiple channels are used, we can further cascade more number of DMACs.



8257 Pin Description



DRQ0–DRQ3

These are the four individual channel DMA request inputs, which are used by the peripheral devices for using DMA services. When the fixed priority mode is selected, then DRQ_0 has the highest priority and DRQ_3 has the lowest priority among them.

DACKo − DACK3

These are the active-low DMA acknowledge lines, which updates the requesting peripheral about the status of their request by the CPU. These lines can also act as strobe lines for the requesting devices.

Do − D7

These are bidirectional, data lines which are used to interface the system bus with the internal data bus of DMA controller. In the Slave mode, it carries command words to 8257 and status word from 8257. In the master mode, these lines are used to send higher byte of the generated address to the latch. This address is further latched using ADSTB signal.

IOR

It is an active-low bidirectional tri-state input line, which is used by the CPU to read internal registers of 8257 in the Slave mode. In the master mode, it is used to read data from the peripheral devices during a memory write cycle.

IOW

It is an active low bi-direction tri-state line, which is used to load the contents of the data bus to the 8-bit mode register or upper/lower byte of a 16-bit DMA address register or terminal count register. In the master mode, it is used to load the data to the peripheral devices during DMA memory read cycle.

CLK

It is a clock frequency signal which is required for the internal operation of 8257.

RESET

This signal is used to RESET the DMA controller by disabling all the DMA channels.

Ao - A3

These are the four least significant address lines. In the slave mode, they act as an input, which selects one of the registers to be read or written. In the master mode, they are the four least significant memory address output lines generated by 8257.

CS

It is an active-low chip select line. In the Slave mode, it enables the read/write operations to/from 8257. In the master mode, it disables the read/write operations to/from 8257.

A4 - A7

These are the higher nibble of the lower byte address generated by DMA in the master mode.

READY

It is an active-high asynchronous input signal, which makes DMA ready by inserting wait states.

HRQ

This signal is used to receive the hold request signal from the output device. In the slave mode, it is connected with a DRQ input line 8257. In Master mode, it is connected with HOLD input of the CPU.

HLDA

It is the hold acknowledgement signal which indicates the DMA controller that the bus has been granted to the requesting peripheral by the CPU when it is set to 1.

MEMR

It is the low memory read signal, which is used to read the data from the addressed memory locations during DMA read cycles.

MEMW

It is the active-low three state signal which is used to write the data to the addressed memory location during DMA write operation.

ADST

This signal is used to convert the higher byte of the memory address generated by the DMA controller into the latches.

AEN

This signal is used to disable the address bus/data bus.

TC

It stands for ‘Terminal Count’, which indicates the present DMA cycle to the present peripheral devices.

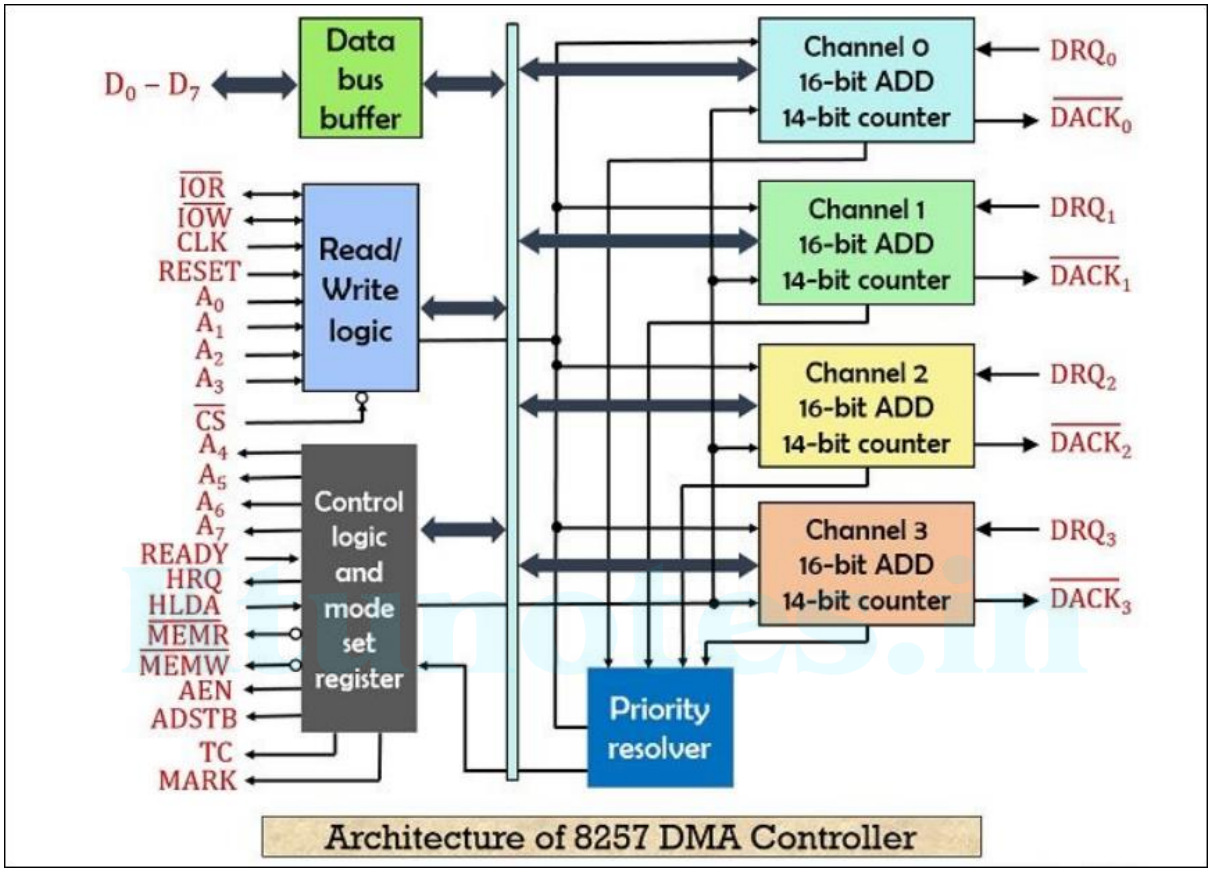
MARK

The mark will be activated after each 128 cycles or integral multiples of it from the beginning. It indicates the current DMA cycle is the 128th cycle since the previous MARK output to the selected peripheral device.

Vcc

It is the power signal which is required for the operation of the circuit.

8257 - Architecture



It consists of five functional blocks:

a) Data bus buffer
b) Control logic
c) Read/write logic
d) Priority Resolver
e) DMA channels

Data Bus Buffer:

8-bit Tristate, bidirectional buffer interfaces the internal bus of 8257 with the external system bus under the control of various control signals.

Read/Write Logic:

In the slave mode, the read/write logic accepts the I/O Read or I/O Write signals, decodes the Ao-A3 lines and either writes the contents of the data bus to the addressed internal register or reads the selected register depending upon whether IOW or IOR signal is activated.In master mode, the read/write logic generates the IOR and IOW signals to control the data flow to or from the selected peripheral.

Control Logic:

The control logic controls the sequences of operations and generates the required control signals like AEN, ADSTB, MEMR,MEMW, TC and MARK along with the address lines A4-A7, in master mode.

Priority Resolver:

The priority resolver resolves the priority of the four DMA channels depending upon whether normal priority or rotating priority is programmed.

Register Organisation of 8257:

The 8257 performs DMA operation over four independent DMA channels with the following Registers.

1. DMA Address Register

Each DMA channel has one DMA address register. The function of this register is to store the address of the starting memory location, which will be accessed by the DMA channel. The device that wants to transfer data over a DMA channel, will access the block of the memory with the starting address stored in the DMA Address Register.

2. Terminal Count Registers

Each of the four DMA channels of 8257 has one terminal count register (TC). This 16-bit register is used for ascertaining that the data transfer through a DMA channel cease or stops after the required number of DMA cycles.

After each DMA cycle, the terminal count register content will be decremented by one and finally it becomes zero after the required number of DMA cycles are over. The bits 14 and 15 of this register indicate the type of the DMA operation (transfer).

3. Mode Set Register

The mode set register is used for programming the 8257 as per the requirements of the system. The function of the mode set register is to enable the DMA channels individually and also to set the various modes of operation. The bits Do-D3 enable one of the four DMA channels of 8257.If the TC STOP bit is set, the selected channel is disabled after the terminal count condition is reached, and it further prevents any DMA cycle on the channel. If the TC STOP bit is programmed to be zero, the channel is not disabled, even after the count reaches zero and further request are allowed on the same channel. The auto load bit, if set, enables channel 2 for the repeat block chaining operations, without immediate software intervention between the two successive blocks. The extended write bit, if set to '1', extends the duration of MEMW and IOW signals by activating them earlier, which is useful in interfacing the peripherals with different access times.

4. Status register

The lower order 4-bits of this register contain the terminal count status for the four individual channels. If any of these bits is set, it indicates that the specific channel has reached the terminal count condition. The update flag is not affected by the read operation. This flag can only be cleared by resetting 8257. The update flag is set every time, the channel 2 registers are loaded with contents of the channel 3 registers. It is cleared by the completion of the first DMA cycle of the new block. This register can only read.

DMA TRANSFER & OPERATIONS

The 8257 is able to accomplish three types of operations such as

1.DMA operation

2. Write Operation

3. Read Operation

Operational sequence of 8257 is as follows

o The 8257 request any one of the 8257 DRQ inputs to transfer single byte.

o In response to the request, the 8257 sends HRQ signal to CPU at its HLD input and waits for acknowledgement at the HLDA input.

o If the DMA controller receives the HLDA signal it indicates that the bus is available for the transfer.

o The DMA controller generate the read and write commands to transfer the

byte from/to the I/O Device.

o The DACK line of the used channel is pulled down by the DMA controller to I/O device that requested for DMA transfers.

o The HRQ line is lowered by the DMA controller to indicate the CPU that it may regain the control of the bus.

o The DRQ must be high until acknowledged.

o In each s4 state, the DRQ lines are sampled and highest priority request is recognized during next transfer. The HRQ line is maintained active till all the DRQ line go low.

MODULE 4 INTERFACING CHIPS

PROGRAMABLE PERIPHRAL INPUT OUTPUT PORT 8255

The 8255A is a general purpose programmable I/O device designed to transfer the data from I/O to interrupt I/O under certain conditions as required. It can be used with almost any microprocessor. It consists of three 8-bit bidirectional I/O ports (24 I/O lines) which can be configured as per the requirement.
Features of 8255A

- It consists of 3 8-bit IO ports i.e. PA, PB, and PC.
- Address/data bus must be externally demultiplexed.
- It is TTL compatible.
- It has improved DC driving capability.

8255 ARCHITECTURE

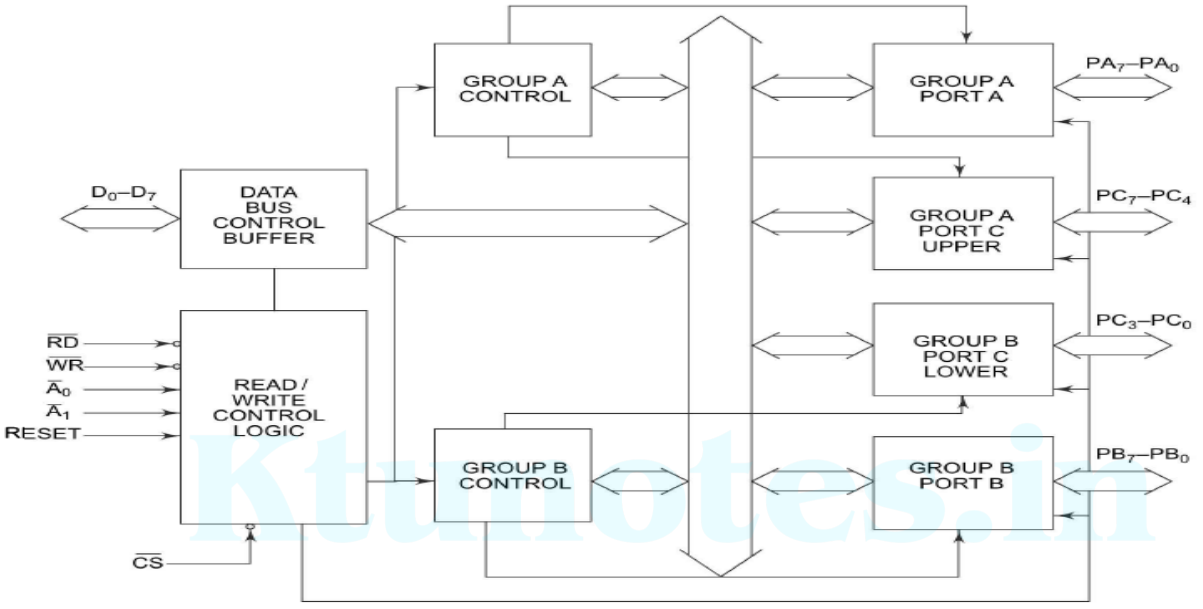


Fig. 5.17(a) *8255 Internal Architecture*

- It has 24 input/ output lines which may be individually programmed into two groups of 12 lines each or three groups with 8 lines of each.
- The two groups of I/O pin are named as Group A and Group B
- Each of these two groups contains a subgroup of 8 lines called 8 bit port and another 4 bit lines called port.
- Thus group A contains a 8 bit port along with a 4 bit port C upper. The port A lines are identified by PA_0 to PA_7 while port C lines are identified by PC_4 to PC_7.
- Similarly group B contains 8 bit port identified by PB_0 to PB_7 and 4 bit port C lower identified by PC_0 to PC_3.
- The port C upper and port C lower can be used in combination as 8 bit port C. both the port C are assigned same address.
- All these ports can function independently either as input or output port.
- This can be achieved by programming the bits of internal registers of 8255 called as Control Word Register (CWR).
- The 8 bit data buffer is controlled by read/write logic
- The read/write control logic manages all the internal and external transfers of both data and control words.
- The 8 bit 3 state bidirectional buffer is used to interface the internal data bus with external system data bus.

- This buffer receives or transmits data upon the execution of input or output instruction by the microprocessor. The control word or status information is also passed through the buffer.

SIGNAL DESCRIPTION OF 8255A

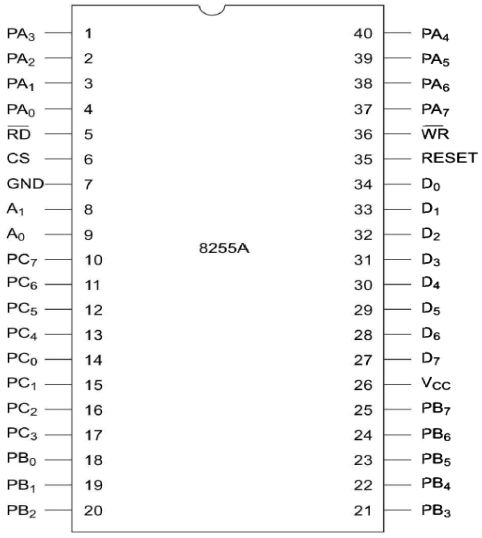


Fig. 5.17(b) *8255A Pin Configuration*

Pins	Description
$PA_7 – PA_0$	These are 8 port A lines that act as either latched output buffer or buffered input lines depending upon the control word loaded into CWR
$PC_7 – PC_4$	Upper nibble of port C. they might act as either output latches or input buffers. This port can also be used for generation of handshaking lines in mode 1 or 2
$PC_3 – PC_0$	Lower nibble of port C. same as above
$PB_0 – PB_7$	These are 8 port B lines which are used as latched output lines or buffered input lines same as port A
$\overline{RD}$	This input line is driven by the microprocessor and should be low to indicate read operation
$\overline{WR}$	For write operation it should be low
$\overline{CS}$	This is a chip select line. When it goes low it responds to RD/WR signals, otherwise neglected
$A_1 – A_0$	These are address lines driven by the microprocessor. These along with RD/ WR/CS forms the following operations. These address lines are used for addressing any of 4 registers as shown in below table.
$D_0 – D_7$	These are data bus lines which carry data or control word to/ from microprocessor .
RESET	A logic high on this line clears the control word register of 8255. All ports are set as input ports by default after reset.

Table 5.9(a)

$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	A_1	A_0	*Input (Read) cycle*
0	1	0	0	0	Port A to data bus
0	1	0	0	1	Port B to data bus
0	1	0	1	0	Port C to data bus
0	1	0	1	1	CWR to data bus

Table 5.9 (b)

$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	A_1	A_0	*Output (Write) cycle*
1	0	0	0	0	Data bus to Port A
1	0	0	0	1	Data bus to Port B
1	0	0	1	0	Data bus to Port C
1	0	0	1	1	Data bus to CWR

MODES OF OPERATION OF 8255

There are two basic modes of operation of 8255–I/O mode and Bit Set-Reset mode (BSR). In the I/O mode, the 8255 ports work as programmable I/O ports, while in BSR mode only port C(PC_0–PC_7) can be used to set or reset its individual port bits. Under the IO mode of operation, further there are three modes of operation of 8255, so as to support different types of applications, viz. *mode 0* , *mode 1* and *mode 2*. These modes of operation are discussed in significant details along with application problems in this section, so as to present a clear idea about 8255 operation and interfacing in different modes with 8086.

BSR Mode:

In this mode, any of the 8-bits of port C can be set or reset depending on B_0 of the control word. The bit to be set or reset is selected by bit select flags B_3, B_2 and B_1 of the CWR as given in Table 5.10. The CWR format is shown in Fig. 5.18(a).

Table 5.10

B_3	B_2	B_1	*Selected Bits of port C*
0	0	0	B_0
0	0	1	B_1
0	1	0	B_2
0	1	1	B_3
1	0	0	B_4
1	0	1	B_5
1	1	0	B_6
1	1	1	B_7

I/O Mode: 8255 has 3 input modes they are Mode 0, Mode 1 and Mode 2

MODE 0 (Basic I/O mode) This mode is also known as *basic input/output mode*. This mode provides simple input and output capability using each of the three ports. Data can be simply read from and written to the input and output ports respectively, after appropriate initialisation.

The salient features of this mode are as listed below:

(i) Two 8-bit ports (port A and port B) and two 4-bit ports (port C upper and lower) are available. The two 4-bit ports can be combinedly used as a third 8-bit port.
(ii) Any port can be used as an input or output port.
(iii) Output ports are latched. Input ports are not latched.
(iv) A maximum of four ports are available so that overall 16 I/O configurations are possible.

MODE 1 (Strobed I/O mode) This mode is also called as strobed input/output mode. In this mode the handshaking signals control the input or output action of the specified port. Port C lines PC_0–PC_2, provide strobe or handshake lines for port B. This group which includes port B and PC_0–PC_2 is called as group B for strobed data input/output. Port C lines PC_3–PC_5 provide strobe lines for port A. This group including port A and PC_3–PC_5 forms group A. Thus port C is utilized for generating handshake signals. The salient features of mode 1 are listed as follows:

(i) Two groups—group A and group B are available for strobed data transfer.
(ii) Each group contains one 8-bit data I/O port and one 4-bit control/data port.
(iii) The 8-bit data port can be either used as input or an output port. Both the inputs and outputs are latched.
(iv) Out of 8-bit port C, P C_0–PC_2 are used to generate control signals for port B and PC_3–PC_5 are used to generate control signals for port A. The lines PC_6, PC_7 may be used as independent data lines.

Input control signal definitions (mode 1)

$\overline{\text{STB}}$ (Strobe input)—If this line falls to logic low level, the data available at 8-bit input port is loaded into input latches.

IBF(Input buffer full)—If this signal rises to logic 1, it indicates that data has been loaded into the latches, i.e. it works as an acknowledgement. IBF is set by a low on **$\overline{\text{STB}}$** and is reset by the rising edge of **$\overline{\text{RD}}$** input.

INTR (Interrupt Request): this is active high input signal that can used to interrupt the CPU. Whenever an input devise request service. INTR is set by a high at STB pin and high at IBF pin.

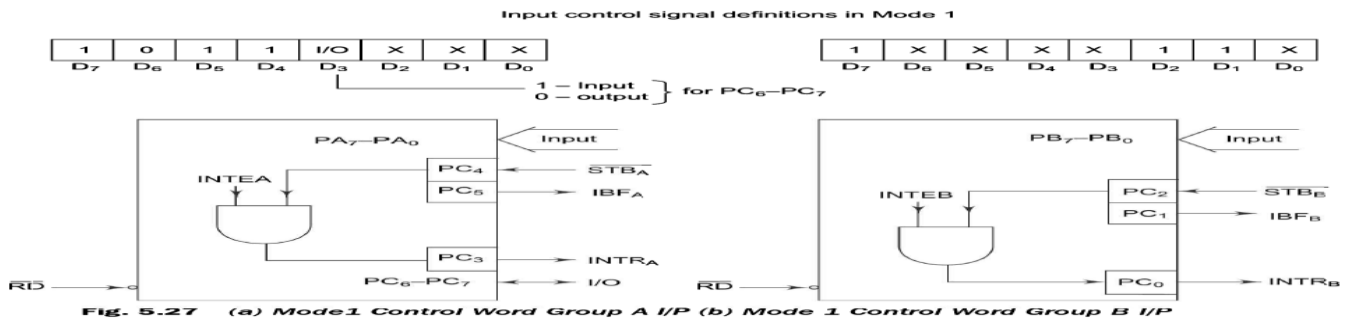


Fig. 5.27 (a) Mode1 Control Word Group A I/P (b) Mode 1 Control Word Group B I/P

Output control signal definitions (mode 1)

OBF (Output buffer full)—This status signal, whenever falls to logic low, indicates that the CPU has written data to the specified output port. The OBF flip-flop will be set by a rising edge of $\overline{WR}$ signal and reset by a low going edge at the $\overline{ACK}$ input.

$\overline{ACK}$ **(Acknowledge input)**— $\overline{ACK}$ signal acts as an acknowledgement to be given by an output device. $\overline{ACK}$ signal, whenever low, informs the CPU that the data transferred by the CPU to the output device through the port is received by the output device.

INTR (Interrupt Request): thus an output signal can be used to interrupt the CPU when an output device acknowledges the data received from the CPU. INTR is set when OBF, ACK and INTE is '1'. It is reset by a falling edge on WR input.

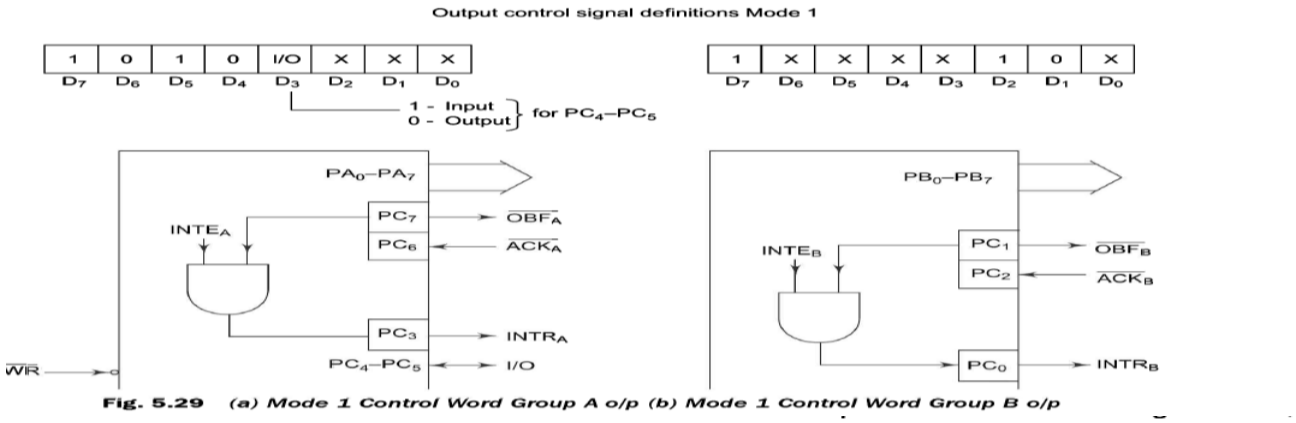


Fig. 5.29 *(a) Mode 1 Control Word Group A o/p (b) Mode 1 Control Word Group B o/p*

MODE 2 (Strobed bidirectional I/O) This mode of operation of 8255 is also known as *strobed bidirectional I/O* . This mode of operation provides 8255 with an additional feature for communicating with a peripheral device on an 8-bit data bus. Handshaking signals are provided to maintain proper data flow and synchronization between the data transmitter and receiver. The interrupt generation and other functions are similar to mode 1. Thus in this mode, 8255 is a bidirectional 8-bit port with handshake signals. The $\overline{RD}$ and $\overline{WR}$ signals decide whether the 8255 is going to operate as an input port or output port.

The salient features of mode 2 of 8255 are listed as follows:

1. The single 8-bit port in group A is available.
2. The 8-bit port is bidirectional and additionally a 5-bit control port is available.
3. Three I/O lines are available at port C,viz. PC_2–PC_0.
4. Inputs and outputs are both latched.
5. The 5-bit control port C (PC_3–PC_7) is used for generating/accepting handshake signals for the 8-bit data transfer on port A.

Control signal definitions in mode 2

INTR (Interrupt request) As in mode 1, this control signal is active high and is used to interrupt the microprocessor to ask for transfer of the next data byte to/from it. This signal is used for input (read) as well as output (write) operations.

Control signals for output operations

$\overline{OBF}$ **(Output buffer full)** This signal, when falls to logic low level, indicates that the CPU has written data to port A.

$\overline{ACK}$ **(Acknowledge)** This control input, when falls to logic low level, acknowledges that the previous data byte is received by the destination and the next byte may be sent by the processor. This signal enables the internal tristate buffers to send out the next data byte on port A.

INTE1 (A flag associated with $\overline{OBF}$) This can be controlled by bit set/reset mode with PC_6.

Control signals for input operations

$\overline{STB}$ **(Strobe input)** A low on this line is used to strobe in the data into the input latches of 8255.

IBF (Input buffer full) When the data is loaded into the input buffer, this signal rises to logic '1'. This can be used as an acknowledgement that the data has been received by the receiver.

PROGRAMABLE INTERVAL TIMER 8254

8254 facilitates the generation of accurate time delays. When 8254 is used as timing and delay generation peripherals, the microprocessor frees from the task of counting process and can executes the processes in memory, while timer may perform counting activities. This reduces the overhead of the microprocessor.

Features of 8253 / 54

The most prominent features of 8253/54 are as follows −

- It has three independent 16-bit down counters.
- It can handle inputs from DC to 10 MHz.
- These three counters can be programmed for either binary or BCD count.
- It is compatible with almost all microprocessors.
- 8254 has a powerful command called READ BACK command, which allows the user to check the count value, the programmed mode, the current mode, and the current status of the counter.

8254 ARCHITECTURE

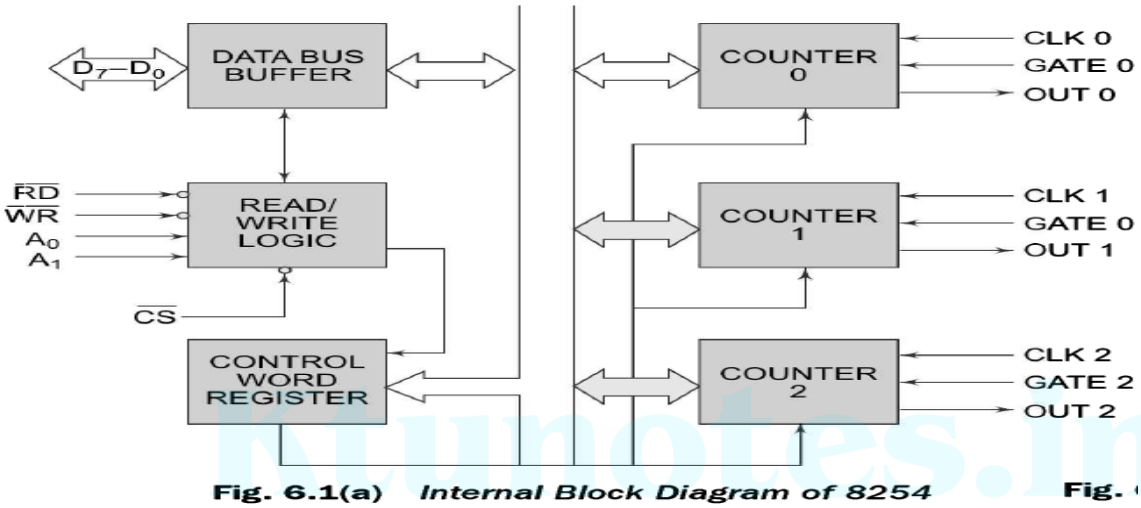


Fig. 6.1(a) *Internal Block Diagram of 8254* **Fig.**

- It contains 3 16 bit independent counters, each with a maximum count rate of 10 MHz.
- It is thus possible to generate three totally independent delays or maintain three independent counters simultaneously.
- All three counters may be independently controlled by programming three internal command word registers.
- Thie 8 bit bidirectional data bit buffer interfaces internal circuit of 8254 to external microprocessor system bus.
- Data is transmitted or received by the buffer depending upon the execution of IN or OUT instruction.
- The read/ wrote logic controls the direction of data buffer depending upon whether it is read or write operation.

- Three counters are independent of each other in operation but are identical to each other in organization. These are 16 bit presetable down counters able to operate either in BCD mode or hexadecimal mode.

- The mode control word register contains the information that can be used for writing or reading the count value into or from respective count register using IN or OUT instruction.

- The specialty of the counters is that they can be easily read on a line without disturbing the clock input to the counter.

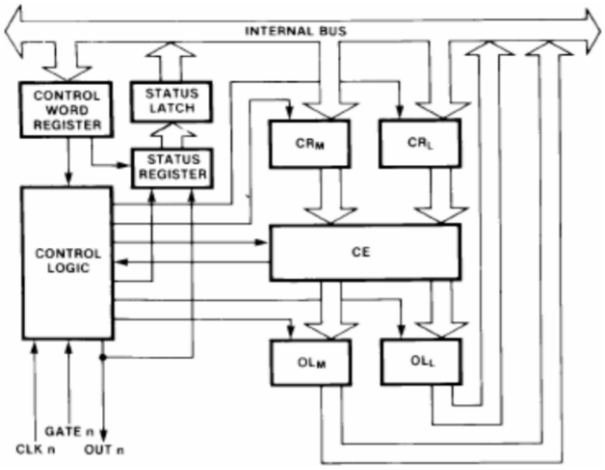
- A0, A1 are address pins and required internally for addressing the mode control word registers and three counter registers.

Table 6.1 *Selected Operations for Various Control Inputs of 8254*

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	*Selected Operation*
0	1	0	0	0	Write Counter 0
0	1	0	0	1	Write Counter 1
0	1	0	1	0	Write Counter 2
0	1	0	1	1	Write Control Word
0	0	1	0	0	Read Counter 0
0	0	1	0	1	Read Counter 1
0	0	1	1	0	Read Counter 2
0	0	1	1	1	No Operation (tristated)
0	1	1	×	×	No Operation (tristated)
1	×	×	×	×	Disabled (tristated)

- A control word register accept the 8 bit control word written by the microprocessor and stores it for controlling the complete operation of specific counter.

Internal block diagram of counters

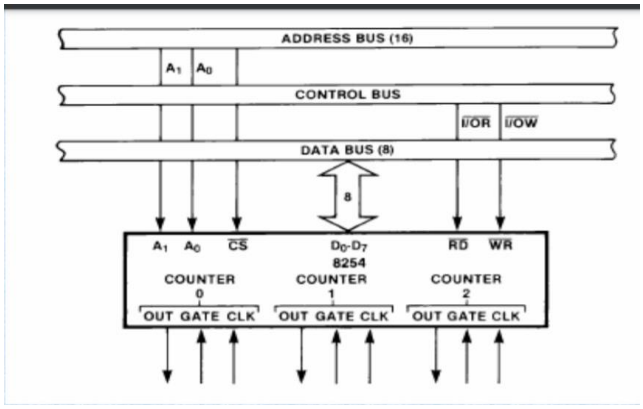


- The actual counter is labelled CE (for ``Counting Element''). It is a 16-bit presettable synchronous down counter. OLM and OLL are two 8-bit latches. OL stands for ``Output Latch''; the subscripts M and L stand for ``Most significant byte'' and ``Least significant byte'' respectively.

- Both are normally referred to as one unit and called just OL. These latches normally ``follow'' the CE, but if a suitable Counter Latch Command is sent to the 8254, the latches ``latch'' the present count until read by the CPU and then return to ``following'' the CE.
- One latch at a time is enabled by the counter's Control Logic to drive the internal bus. This is how the 16-bit Counter communicates over the 8-bit internal bus. Note that the CE itself cannot be read; whenever you read the count, it is the OL that is being read.
- Similarly, there are two 8-bit registers called CRM and CRL (for ``Count Register''). Both are normally referred to as one unit and called just CR.
- When a new count is written to the Counter, the count is stored in the CR and later transferred to the CE. The Control Logic allows one register at a time to be loaded from the internal bus. Both bytes are transferred to the CE simultaneously.
- CRM and CRL are cleared when the Counter is programmed. In this way, if the Counter has been programmed for one byte counts (either most significant byte only or least significant byte only) the other byte will be zero.

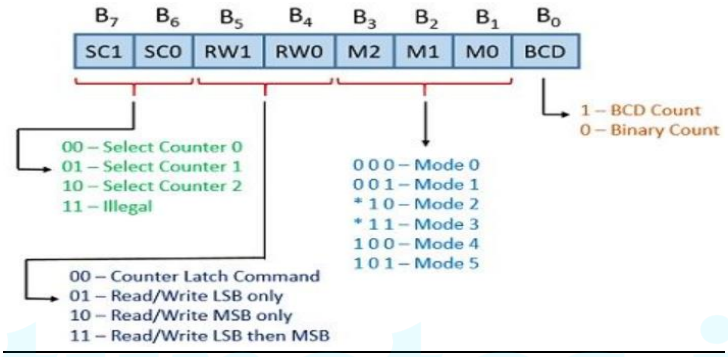
8254 System Interface

- It is treated by the system's software as an array of peripheral I/O ports; three are counters and the fourth is a control register for MODE programming

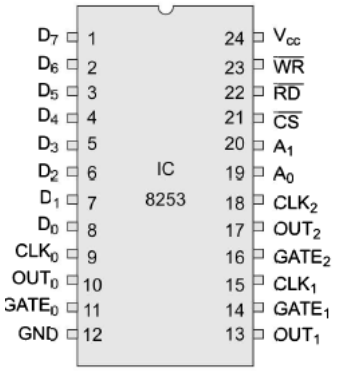


Programming of 8254

At the time of programming the timer it is necessary that each individual counter of 8254 is to be programmed separately using control word and count value.



PIN DESCRIPTION



1(b) ***Pin Configuration of 8254***

Pins	Description
A0, A1	The address input selects one of four counter registers within 8254
D0 – D7	Bidirectional three state data bus lines connected to system data bus
CLK	Clock input is timing source for each counters. This input is often connected with PCLK signal from the microprocessor system bus controller.
OUT	Counter output where the waveform generated by it is available.
RD	Read causes data to be read from 8254 and often connected to IORC signal
WR	Write causes data to be written to 8254 and often connected to IOWC signal

A1	A0	Function
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control word

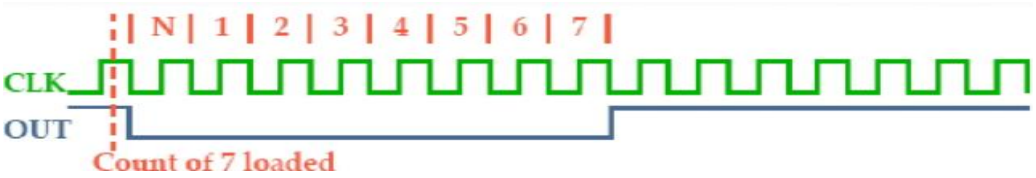
CS	Chip select enables 8254 for programming and for reading/writing a counter
VCC	Power supply to 8254 + 5V
GND	Ground connects to system ground bus
GATE	Gate input controls the operation of counter in some modes of operation.

MODES OF OPERATION OF 8254

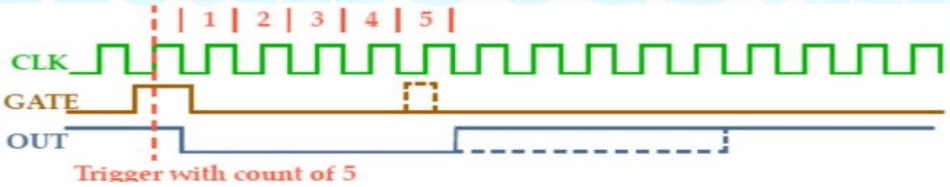
Each of the three counters of 8254 can be operated in one of the following six modes of operation:

1. **Mode 0 (Interrupt on terminal count)**
2. **Mode 1(Programmable monoshot)**
3. **Mode 2 (Rate generator)**
4. **Mode 3 (Square wave generator)**
5. **Mode 4 (Software triggered strobe)**
6. **Mode 5 (Hardware triggered strobe)**

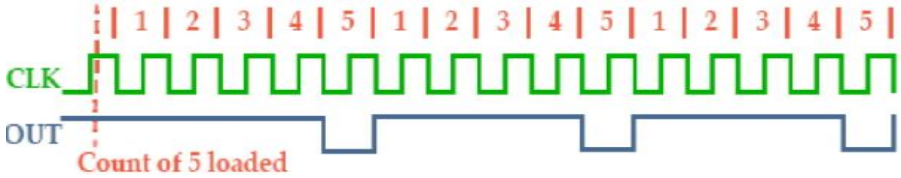
Mode 0: This is used for event counting. After writing the control word, OUT is low at first. It will remain low until the counter reaches 0, it is decremented by 1 after each clock cycle. Then the OUT goes high and remains high until a new count is there or a new Mode 0 control word is written into the counter. The GATE = 1 indicates enable counting, and 0 indicates disable counting



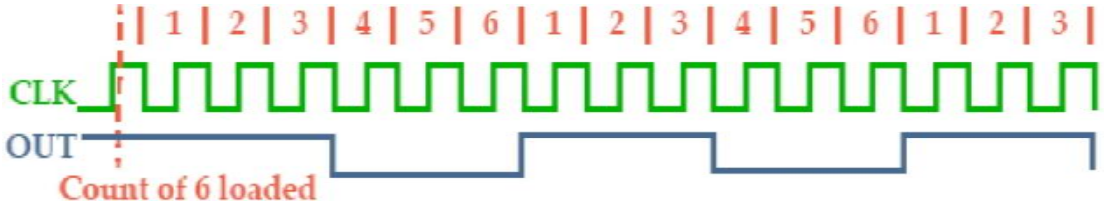
Mode 1: also called as programable one shot mode. This can be used as monostable vibrator. OUT will be high at first, it will go Low on the clock pulse following a trigger to begin the one-shot pulse. It will remain 0 until the counter reaches 0. If another count is loaded when the output is already low, it will not disturb the previous count till a new trigger pulse is applied at GATE input.



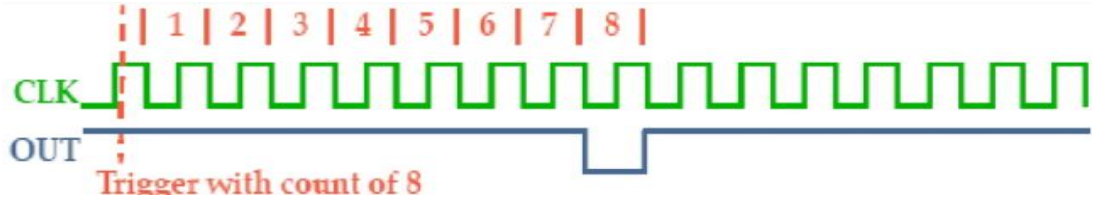
Mode 2: also called either rate generator or divide by N counter. In this the mode, if N is loaded as count value then after N – 1 cycle, the output becomes low only for one clock cycle. The count N is reloaded again and after N – 1 cycles output becomes high. The counter generates active low signals at output initially, after the count register is loaded with a count value. Then count down starts and whenever count becomes zero another active low pulse is generated at the output. The duration of these low pulses equal to one clock cycle.



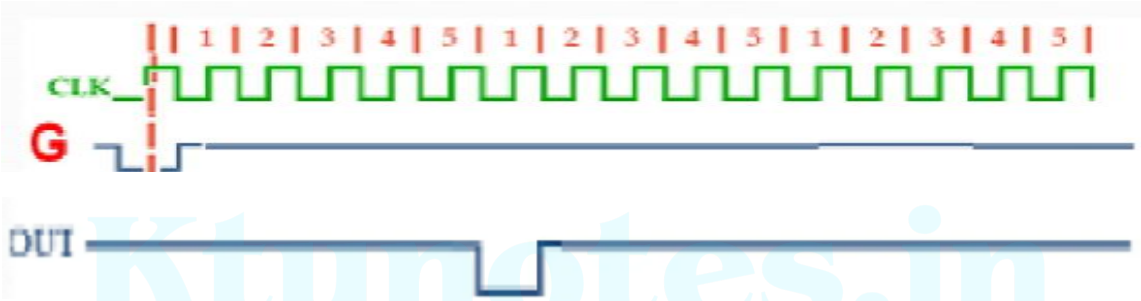
Mode 3: Also called square wave generator. When the count N is loaded is even, then for the half of the count the output remains high and rest of the half it remains low. If the count loaded is odd, first clock cycle decrements it by 1 resulting in even count. Then output remains high for first half and low for remaining half. The process is repeated continuously, resulting in generation of square wave. In case of odd count, the output is high for longer duration and low for shorter duration. In general, if loaded count value N is odd it remains high for (N +1)/2 pulses and low for (N -1)/2 pulses.



Mode 4: also called Software triggered strobe. In this mode counting is enabled by using GATE = 1 and disabled by GATE = 0. Initially value of OUT is high and becomes low when value of count is at last stage. Count is reloaded again for subsequent clock pulse.



Mode 5 (Hardware Triggered Strobe) – OUT will initially be high. Counting is triggered by a rising edge of GATE. When the initial count has expired, OUT will go low for one clock pulse and then go high again. After writing the Control Word and initial count, the counter will not be loaded until the clock pulse after a trigger.



DMA CONTROLLER 8257

DMA stands for Direct Memory Access. It is designed by Intel to transfer data at the fastest rate. It allows the device to transfer the data directly to/from memory without any interference of the CPU.

Using a DMA controller, the device requests the CPU to hold its data, address and control bus, so the device is free to transfer data directly to/from the memory. The DMA data transfer is initiated only after receiving HLDA signal from the CPU.

Following is the sequence of operations performed by a DMA controller 8257

- Initially, when any device has to send data between the device and the memory, the device has to send DMA request (DRQ) to DMA controller. There are four DRQ inputs namely DRQ0 – DRQ3 corresponding to each channel i.e. channel0 – channel3.
- Four devices can be connected to a single 8257.Prioroty resolver in 8257 select the any one of DRQ request based on the priority.
- The DMA controller sends Hold request (HRQ) to the CPU and waits for the CPU to assert the HLDA.
- Then the microprocessor tri-states all the data bus, address bus, and control bus. The CPU leaves the control over bus and acknowledges the HOLD request through HLDA signal.
- Now the CPU is in HOLD state and the DMA controller has to manage the operations over buses between the CPU, memory, and I/O devices.

Features of 8257: Some of the prominent features of 8257 −

- It has four channels which can be used over four I/O devices.
- Each channel has 16-bit address and 14-bit counter.
- Each channel can transfer data up to 64kb.
- Each channel can be programmed independently.

- Each channel can perform read transfer, write transfer and verify transfer operations.
- It generates MARK signal to the peripheral device that 128 bytes have been transferred.
- It requires a single-phase clock.
- Its frequency ranges from 250Hz to 3MHz.
- It operates in 2 modes, i.e., **Master mode** and **Slave mode.**

8257 ARCHITECTURE

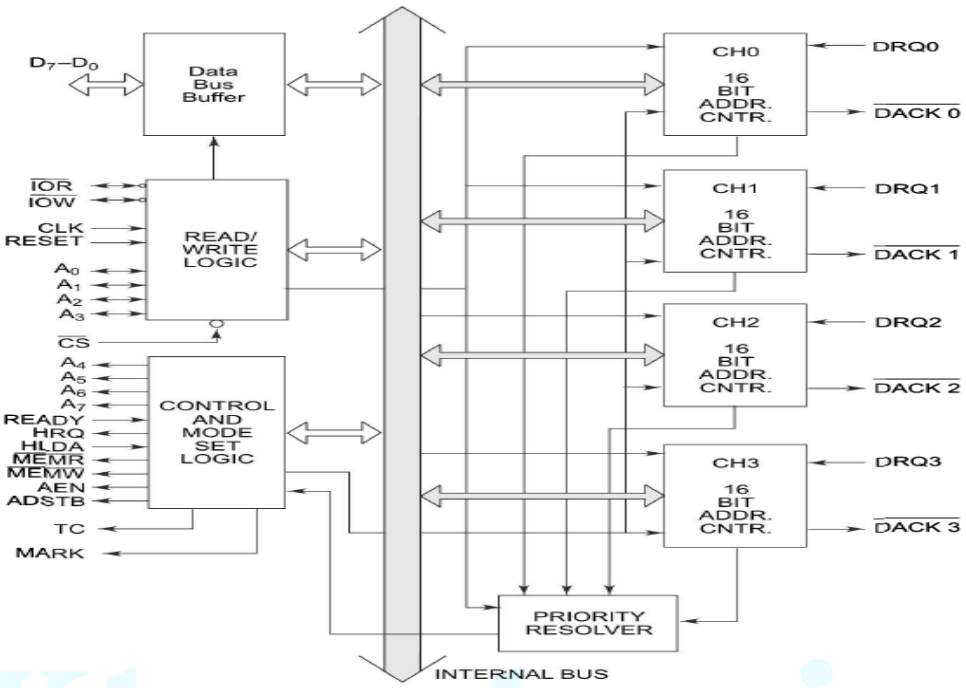


Fig. 7.1 *Internal Architecture of 8257*

- The chip support four DMA channels, i.e. four peripheral devices can independently request for DMA data transfer through these channels at a time.
- The DMA controller has 8-bit internal data buffer, a read/write unit, a control unit, a priority resolving unit along with a set of registers.
- The 8257 performs the DMA operation over four independent DMA channels.
- Each of four channels of 8257 has a pair of two 16-bit registers, viz. DMA address register and terminal count register.
- Also, there are two common registers for all channels namely mode set register and status register.
- Thus, there are total of 10 registers and CPU selects one of these using address lines A0 – A3.

DMA Address Register: Each DMA Channel has one DMA register. The function of these registers is to store the address of starting memory locations, which will be accessed by DMA channel. The device that wants to transfer data over a DMA channel, will access the block of the memory with the starting address stored in the DMA Address Register.

Terminal Count Register: Each of the four DMA channels of 8257 has one terminal count register (TC). This 16-bit register issued for ascertaining that the data transfer through a DMA channel ceases or stops after the required number of DMA cycles. The low order 14-bits of the terminal count register are initialized with the binary equivalent of the number of required DMA cycles minus one. After each DMA cycle, the terminal count register content will be decremented by one and finally it becomes zero after the required number of DMA cycles are over. The bits 14 and 15 of this register indicate the type of the DMA operation (transfer). If the device wants to write data into the memory, the DMA operation is called DMA write operation. Bit 14 of the register in this case will be set to one and bit 15 will be set to zero.

Mode Set Register: The mode set register is used for programming the 8257 as per the requirements of the system. The function of the mode set register is to enable the DMA channels individually and to set the various modes of operation. The DMA channel should not be enabled till the DMA address register and the

terminal count register contain valid information. The bits Do -D3 enable one of the four DMA channels of 8257. for example, if Do is '1', channel 0 is enabled. If bit 4 is set, rotating priority is enabled, otherwise, the normal, i.e. fixed priority is enabled. If the TC STOP bit is set, the selected channel is disabled after the terminal count condition is reached, and it further prevents any DMA cycle on the channel.

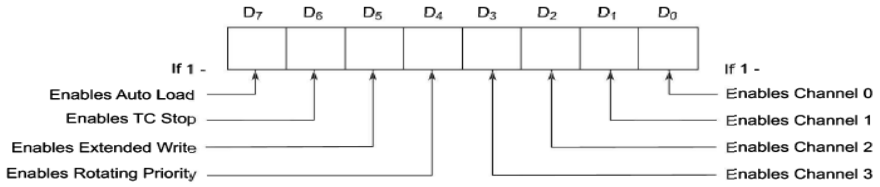


Fig. 7.2 *Bit Definitions of the Mode Set Register*

Status Register: The status register of 8257 is shown in figure. The lower order 4-bits of this register contain the terminal count status for the four individual channels. If any of these bits is set, it indicates that the specific channel has reached the terminal count condition. These bits remain set till either the status is read by the CPU or the 8257 is reset.

- The update flag is not affected by the read operation. This flag can only be cleared by resetting 8257 or by resetting the auto load bit of the mode set register.
- If the update flag is set, the contents of the channel 3 registers are reloaded to the corresponding registers of channel 2 whenever the channel 2 reaches a terminal count condition, after transferring one block and the next block is to be transferred using the auto load feature of 8257.
- The update flag is set every time; the channel 2 registers are loaded with contents of the channel 3 registers. It is cleared by the completion of the first DMA cycle of the new block. This register can only read.

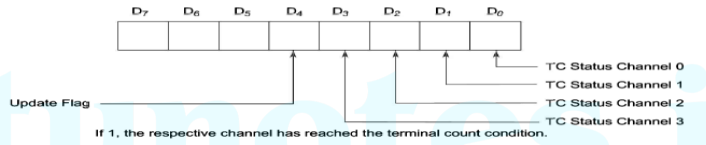


Fig. 7.3 *Bit Definitions of Status Register of 8257*

Data Bus Buffer, Read/ Write Logic, Control Unit and Priority Resolver

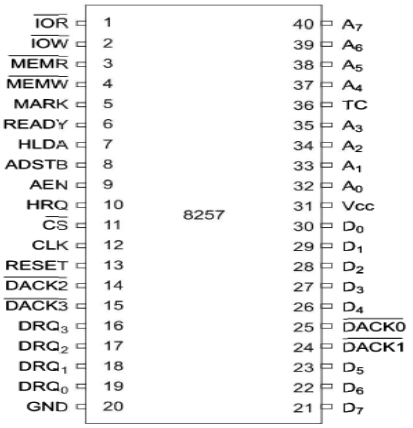
- The 8-bit. Tristate, bidirectional buffer interfaces the internal bus of 8257 with the external system bus under the control of various control signals.

- In the slave mode, the read/write logic accepts the I/O Read or I/O Write signals, decodes the Ao-A3 lines and either writes the contents of the data bus to the addressed internal register or reads the contents of the selected register depending upon whether IOW or IOR signal is activated.

- In master mode, the read/write logic generates the IOR and IOW signals to control the data flow to or from the selected peripheral. The control logic controls the sequences of operations and generates the required control signals like AEN, ADSTB, MEMR, MEMW, TC and MARK along with the address lines A4-A7, in master mode.

- The priority resolver resolves the priority of the four DMA channels depending upon whether normal priority or rotating priority is programmed.

PIN DESCRIPTION OF 8257



Pins	Description
DRQ0 – DRQ3	These are the 4 individual channel DMA requests used by peripheral device for requesting DMA services. DRQ0 has highest priority, while DRQ3 has lowest priority.
$\overline{DACK_0}$ – $\overline{DACK_3}$	These are the active-low DMA acknowledge lines, which updates the requesting peripheral about the status of their request by the CPU. These lines can also act as strobe lines for the requesting.
D0 – D7	These are bidirectional, data lines which are used to interface the system bus with the internal data bus of DMA controller. In the Slave mode, it carries command words to 8257 and status word from 8257. In the master mode, these lines are used to send higher byte of the generated address to the latch.
$\overline{IOR}$	It is an active-low bidirectional tri-state input line, which is used by the CPU to read internal registers of 8257 in the Slave mode. In the master mode, it is used to read data from the peripheral devices during a memory write cycle.
$\overline{IOW}$	It is an active low bi-direction tri-state line, which is used to load the contents of the data bus to the8-bit mode register or upper/lower byte of a 16-bit DMA address register or terminal count register. In the master mode, it is used to load the data to the peripheral devices during DMA memory read cycle.
CLK	Clock frequency signal is required for internal operations.
RESET	Asynchronous input which disables all DMA input channels by clearing the modes.
A0 – A3	These are the four least significant address lines. In the slave mode, they act as an input, which selects one of the registers to be read or written. In the master mode, they are the four least significant memory address output lines generated by 8257.
$\overline{CS}$	It is an active-low chip select line. In the Slave mode, it enables the read/write operations to/from 8257. In the master mode, it disables the read/write operations to/from 8257.
A4 – A7	Higher nibble of lower byte address generated during master mode.
READY	It is an active-high asynchronous input signal, which makes DMA ready by inserting wait states.
HRQ	This signal is used to receive the hold request signal from the output device. In the slave mode, it is connected with a DRQ input line 8257. In Master mode, it is connected with HOLD input of the CPU.
HLDA	It is the hold acknowledgement signal which indicates the DMA controller that the bus has been granted to the requesting peripheral by the CPU when it is set to 1.
$\overline{MEMR}$	It is the low memory read signal, which is used to read the data from the addressed memory locations during DMA read cycles.
$\overline{MEMW}$	It is the active-low three state signal which is used to write the data to the addressed memory location during DMA write operation.
ADSTB	This signal is used to convert the higher byte of the memory address generated by the DMA controller into the latches.
AEN	This signal is used to disable the address bus/data bus.
TC	It stands for ‘Terminal Count’, which indicates the present DMA cycle to the present peripheral devices.
MARK	The mark will be activated after each 128 cycles or integral multiples of it from the beginning. It indicates the current DMA cycle is the 128th cycle since the previous MARK output to the selected peripheral device.
V_{CC}	It is the power signal which is required for the operation of the circuit.
GND	This is a return line for the supply.