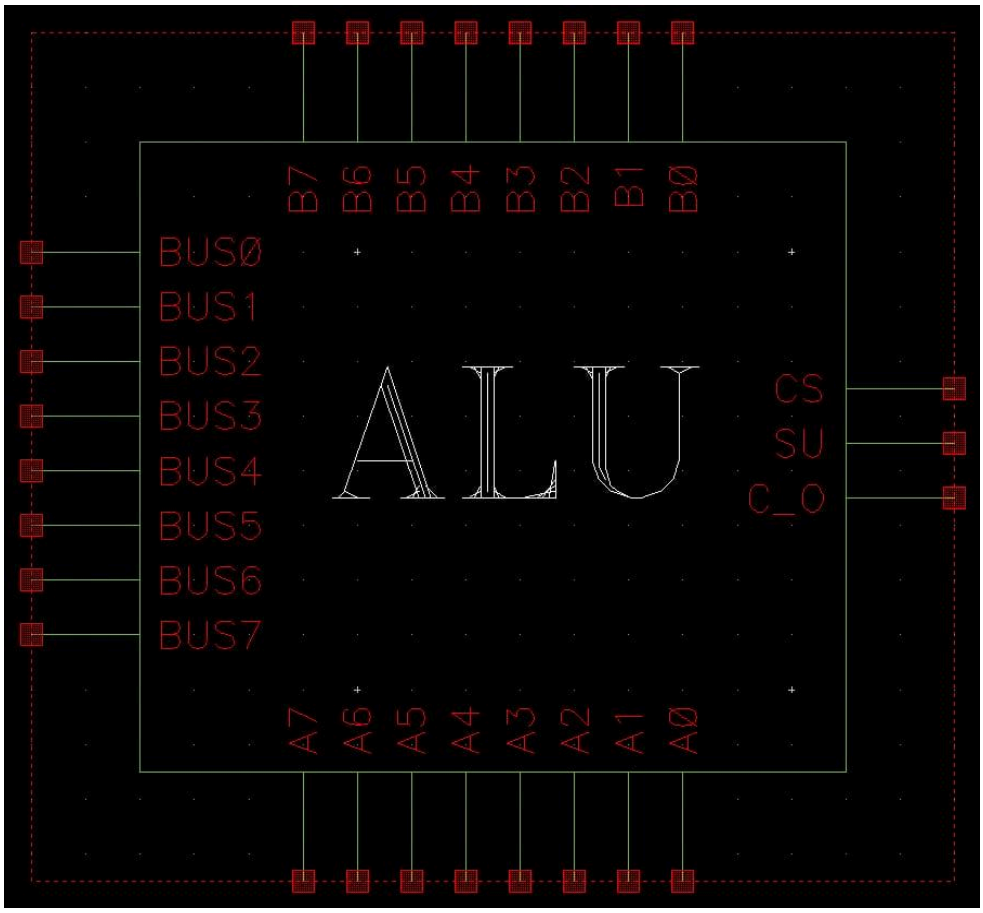
ED221

ALU Team 1



Team :

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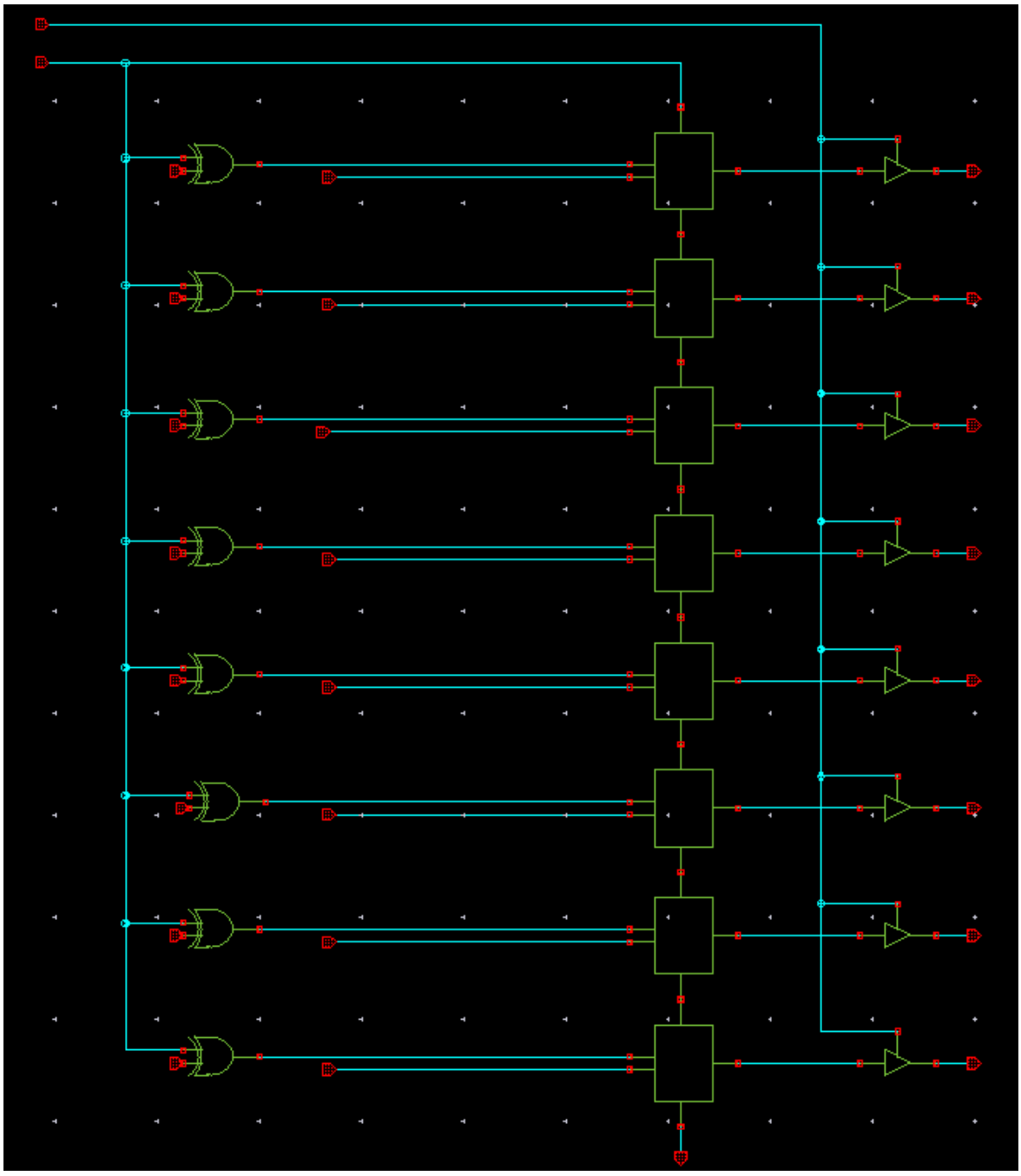
I/O:

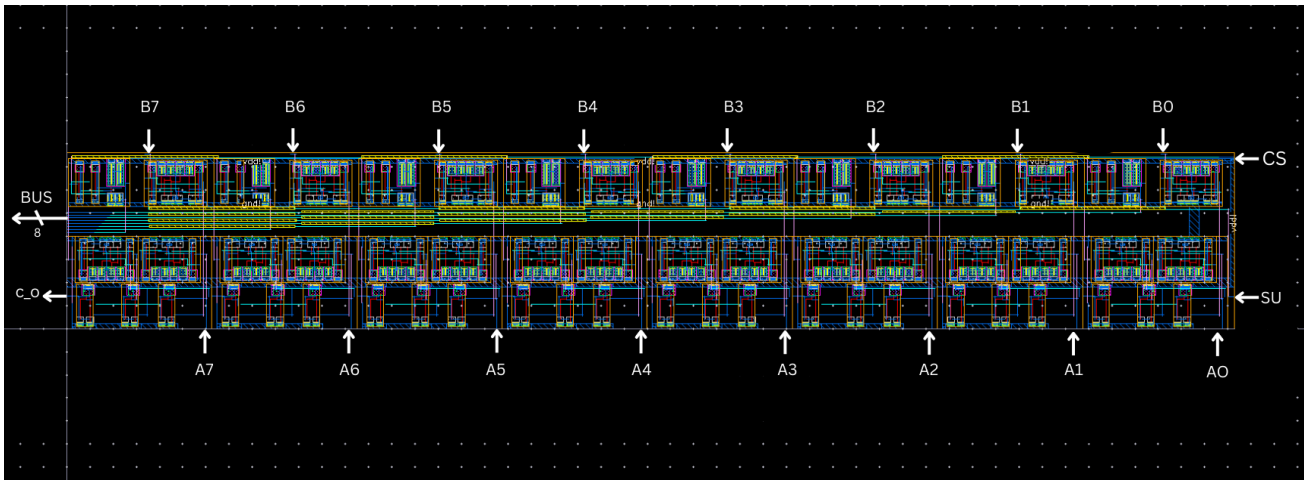
- **Inputs :** (A7 - A0), (B7 - B0), CS, SU
- **Outputs :** (BUS7 - BUS0), C_O

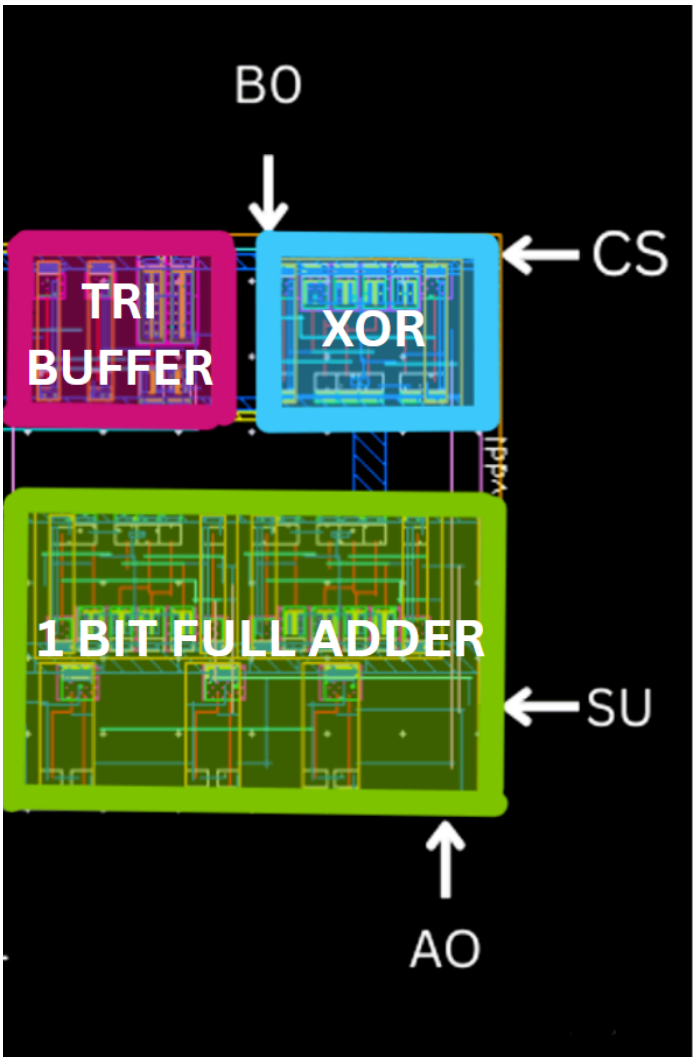
Schematic:



- Input from register A and register B is **hard wired** to the ALU.
- Input from register B and SU is connected to the XOR Gate, and the output of the XOR gate is inserted as 2nd input of the ALU.

Layout:


B7
B6
B5
B4
B3
B2
B1
B0
CS
BUS
8
C_O
SU
A7
A6
A5
A4
A3
A2
A1
AO


B0
CS
TRI
BUFFER
XOR
1 BIT FULL ADDER
SU
AO

Functionality :

- **A0 - A7** and **B0 - B7** are input pins hard wired to register A and register B, respectively.
- A0 & B0 are LSB and A7 & B7 are MSB.
- Pins (**BUS0 - BUS7**) contain the output of the ALU, which will be connected to the bus.
- **C_O** is the output carry.
- **The SU** pin is used to switch between addition and subtraction. It is also connected to the input carry.
    - **SU = 0**, Addition is performed by the ALU.
    - **SU = 1**, Subtraction is performed by the ALU.
- **CS** is the chip select pin in an active high configuration.
    - **CS = 1**, Output of ALU will be connected to the bus.
    - **CS = 0**, Output will be in high impedance state (i.e. ALU will be isolated).

Timings and Delay :

- After performing post-layout simulation, the **propagation delay of the ALU** was found to be **1.62 ns.**
- The maximum current ALU can provide is 535 µA, and it can charge a 50 pf capacitor in 0.2 µs.