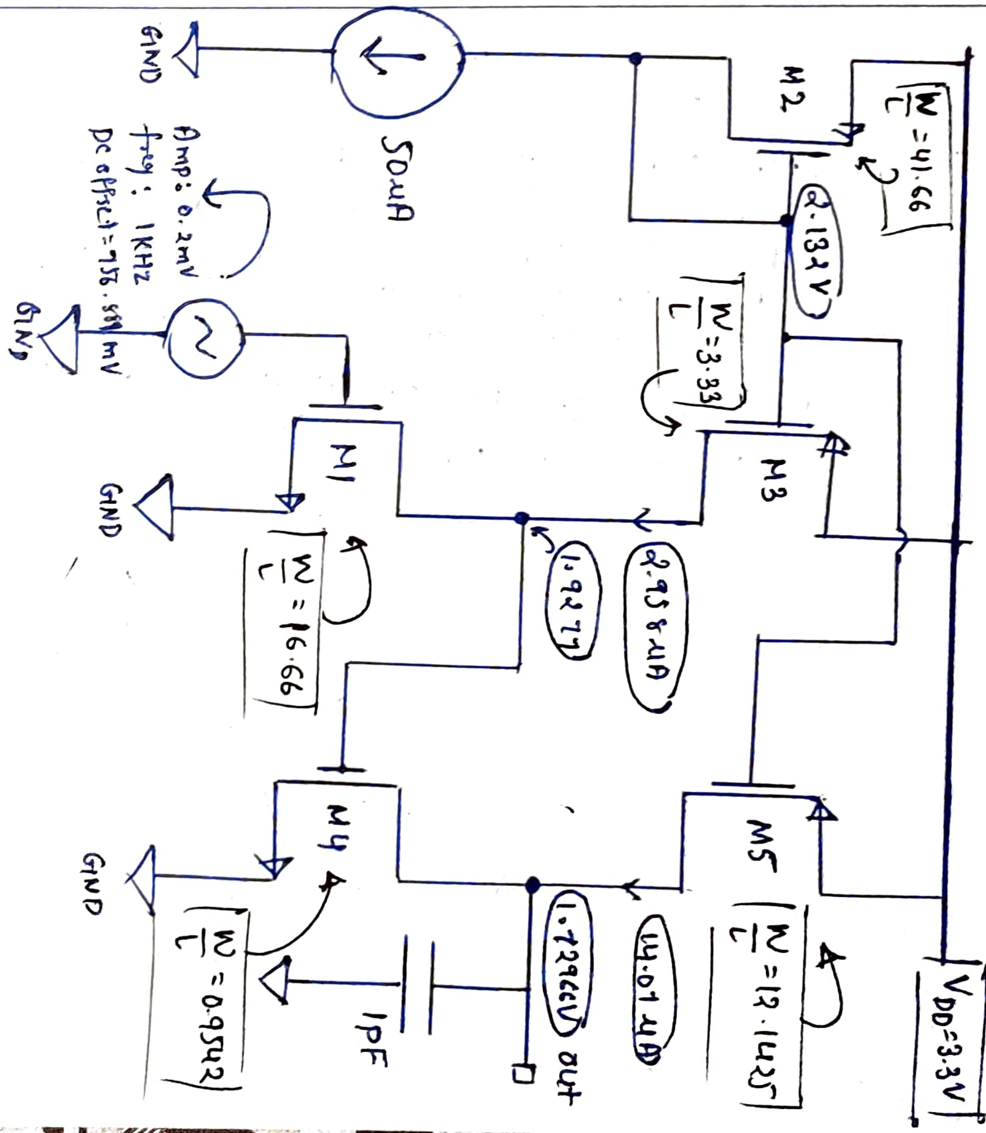
Devansh Tanna – 2019A3PS0158P | Prabhav Shah – 2019A3PS0200P

PROBLEM - 1

Common Source Amplifier

Note :- → Model used in this problem contains non-linear effects, which are simulated in LTSpice.
→ Hence its parameters such as G_m, G_{mb}, r_o are taken from results obtained in operating point simulation in LTSpice.

✱ Amplifier Configuration (Topology)



Note:- We have used simulation to find all the (W/L), for all MOSFETs because hand calculation may lead to wrong result, because given model is non-linear and it contains effects other than channel length modulation and Body-bias effect.

* Method for finding (W/L) of all the MOSFETs

[1.] First V_{tho} of PMOS is 0.927 V, and we want V_{ov} of 0.2 – 0.3V, so we decided to keep V_{ov} of M2 around 0.2–0.3 V, so its V_{SG1} will be 1.2 V, so its $V_{G1} = 2.1V$, from this we simulated (W/L) by doing Parameter sweep by keeping $L = 2L_{min} = 1.2\mu$.

→ We got $\boxed{W = 50\mu,\ V_{G1} = 2.132V}$

[2.] Now we have chosen value ~~by~~ $\left(\frac{W}{L}\right)$ of M3 by assuming some small current of 5μ-10μ, and ~~value~~ of $\left(\frac{W}{L}\right)$ of M1 ~~by~~ according to bias point like we need $V_{DS} = 1.6V$ for high output swing so for what given value of current we can get this V_{DS}, V_{GS}.

Note:- By Applying Second-stage, we have changed the values again because to control gain and V_{DS}.

[3.] Value of M5 is set for required gain, and value of M4 is ~~stack~~ set such that it operates at V_{DS} (bias) of first stage, so no new voltage is required

4. $\left(\frac{W}{L}\right)$ Values of M3 and M5 is chosen ~~and~~ tuned afterwards according to required gain (70dB).

5. Here accurate hand calculations can't be done because V_{DS} of both the NMOS ~~varies~~ is very sensitive to $\left(\frac{W}{L}\right)$ and bias point, that's how we can get such high gain.

→ So, at every point $\left(\frac{W}{L}\right)$ is simulated ~~after~~ but before that bias V_{GS} is set for M1 from VTC of first stage and $\left(\frac{W}{L}\right)$ of M5 is tuned for gain.

↦ Now, we got (W/L) of all the MOSFETs, so ~~we can~~ ~~now~~ we can generate small signal model of given amplifier.

⇒ Justification for all the MOSFETs are in active region

M1 : NMOS $V_{GS} = 0.757$ V $V_{th} = 0.674$ V $V_{DS} = 1.93$ V	M2 : PMOS $V_{SG} = 1.17$ V $V_{SD} = 1.17$ V $V_{th} = -0.926$ V	M3 : PMOS $V_{SG} = 1.17$ V $V_{SD} = 1.37$ $V_{th} = -0.945$ V
M4 : NMOS $V_{GS} = 1.93$ V $V_{DS} = 1.73$ V $V_{th} = 1.15$ V	M5 : $V_{SG} = 1.17$ V $V_{SD} = 1.57$ V $V_{th} = -0.930$ V	

From the Simulation :-

M1 : $g_m = \cancel{1.14 \times 10^{-4} \, A/V}$ 6.54×10^{-5} A/V

$g_{mb} = \cancel{3.36 \times 10^{-5} \, A/V}$ 2.25×10^{-5} A/V

$r_o = \cancel{1.087 \, M\Omega}$ 3.5714 MΩ

M4 : $g_m = 3.20 \times 10^{-5}$ A/V

$g_{mb} = 1.33 \times 10^{-5}$ A/V

$r_o = 2.4038$ MΩ

M5 : $r_o = 1.0869$ MΩ

M3 : $r_o = 4.7393$ MΩ

* Small Signal Model :-

Note :- → This small signal is based on what is taught in class. It does not contain parasitic capacitance, input Resistance of MOSFET, any non-linear effect other than channel length modulation

→ Purpose of this model to estimate

Av, Gm, Rout.

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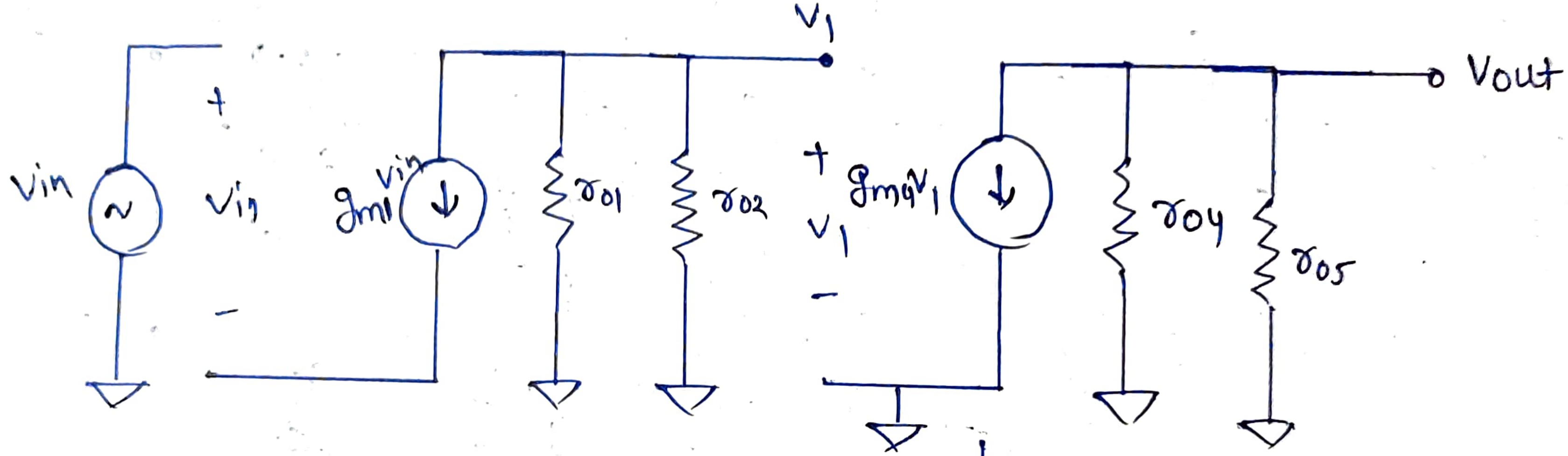
Devansh Tanna – 2019A3PS0158P



From stage-1,

$$V_1 = -g_{m1}\,(r_{o1} \,||\, r_{o2}) \cdot V_{in} \quad (1)$$

from stage-2,

$$V_{out} = -g_{m4}\,(r_{o4} \,||\, r_{o5}) \cdot V_1 \quad (2)$$

from (1) and (2)

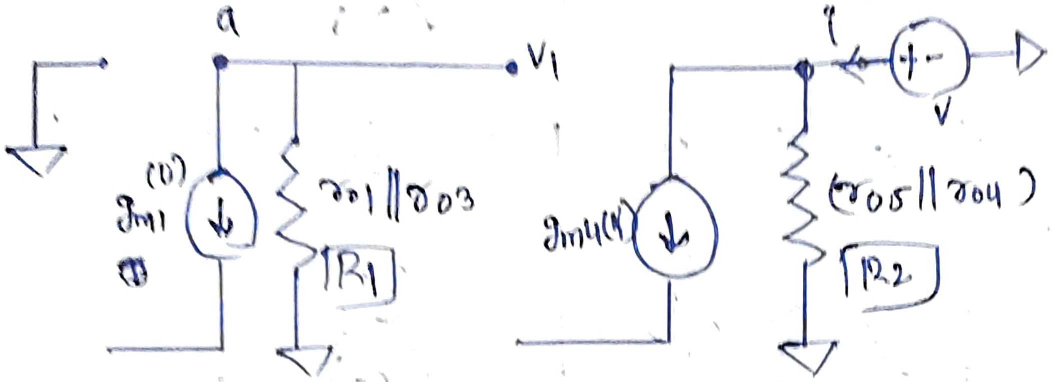
$$\frac{V_{out}}{V_{in}} = g_{m1} \cdot g_{m4}\,(r_{o1} \,||\, r_{o2}) \cdot (r_{o4} \,||\, r_{o5})$$

Substituting values,

$$\frac{V_{out}}{V_{in}} = (6.54 \times 10^{-5})(3.20 \times 10^{-5}) \times (3.5714 \times 10^{6} \,||\, 9.7393 \times 10^{6}) \times (1.0869 \times 10^{6} \,||\, 2.4038 \times 10^{6})$$

$$= 3190.2021 \text{ V/V} = \boxed{70.07 \text{ dB}}$$

Rout can be calculated by switching off input source and applying voltage source at output node.



Current through first stage is zero because no voltage at input so, current through R_1 is also zero.

$\Rightarrow$ so $V_1 = 0 \times (r_{o1} \| r_{o4})$

$$\boxed{V_1 = 0V}$$

Similarly current through R_2, will be i.

So $v = -i\,(r_{o5} \| r_{o4})$

$$\frac{v}{i} = r_{o5} \| r_{o4}$$

$$R_{out} = r_{o5} \| r_{o4}$$

In actual circuit there is one capacitance of 1pF. so it will be added in ~~series~~ parallel

so,

$$R_{out} = (r_{o5} \| r_{o4}) \| \frac{1}{j\omega C}$$

= putting all values which gives

$= 1.484 \times 10^5\ \Omega = \boxed{0.1484\ M\Omega}$

* Specifications Review :-

(1) Gain (Voltage)

Required → 70 dB
Obtained → 70.071 dB
Reason → Not required

(2) -3dB frequency

Required → 3 KHz
Obtained → 30 kHz
Reason → Already better response than required.

(3) Phase-margin :-

Required → 45°
Obtained → ≃ 0°
Reason → we need to change value of load capacitance to change the phase margin otherwise, we will have to change Rout to shift the pole, but this change will decrease gain so we have to trade-off between gain, 3dB freq and phase margin

(4) Power consuption

Required → 3mW
Obtained → 114.47 uW
Reason → already less than required, so no need.

(5) Output swing

Required → 2.64 V
Obtained → 2.3 V
Reason → little bit less ~~due to~~ because, we implemented Q-stages and bias (VGS) of secon ~~stage~~ is much higher so Vov is also much higher so output swing is limited at ~~positive~~ negative part.

→ $V_{DS} > V_{OV}$ ⇒ $V_{DS} > V_{GS} - V_{th}$

if $V_{GS} \uparrow$ ⇒ $V_{DS} \uparrow$

so swing will be limited at negative part.

(6) Input Swing

Obtained → 0.5 mV

---

* Small Signal Parameters of all the MOSFETs

M1

NMOS

$g_m = 6.54 \times 10^{-5}$ A/V

$g_{mb} = 2.25 \times 10^{-5}$ A/V

$r_o = 3.5714 \times 10^{6}\ \Omega$

$= 3.57\ M\Omega$

M2

PMOS

$g_m = 4.02 \times 10^{-4}$ A/V

$g_{mb} = 1.18 \times 10^{-4}$ A/V

$r_o = 0.265\ M\Omega$

M3

PMOS

$g_m = 2.58 \times 10^{-5}$ A/V

$g_{mb} = \cancel{1.1 \times 10^{-4}}\ 7.64 \times 10^{-6}$ A/V

$r_o = 4.7393\ M\Omega$

M4

NMOS

$g_m = 3.20 \times 10^{-5}$ A/V

$g_{mb} = 1.33 \times 10^{-5}$ A/V

$r_o = 2.403\ M\Omega$

M5

PMOS

$g_m = 1.14 \times 10^{-4}$ A/V

$g_{mb} = 3.36 \times 10^{-5}$ A/V

$r_o = 1.0869\ M\Omega$

V(out)/V(in)

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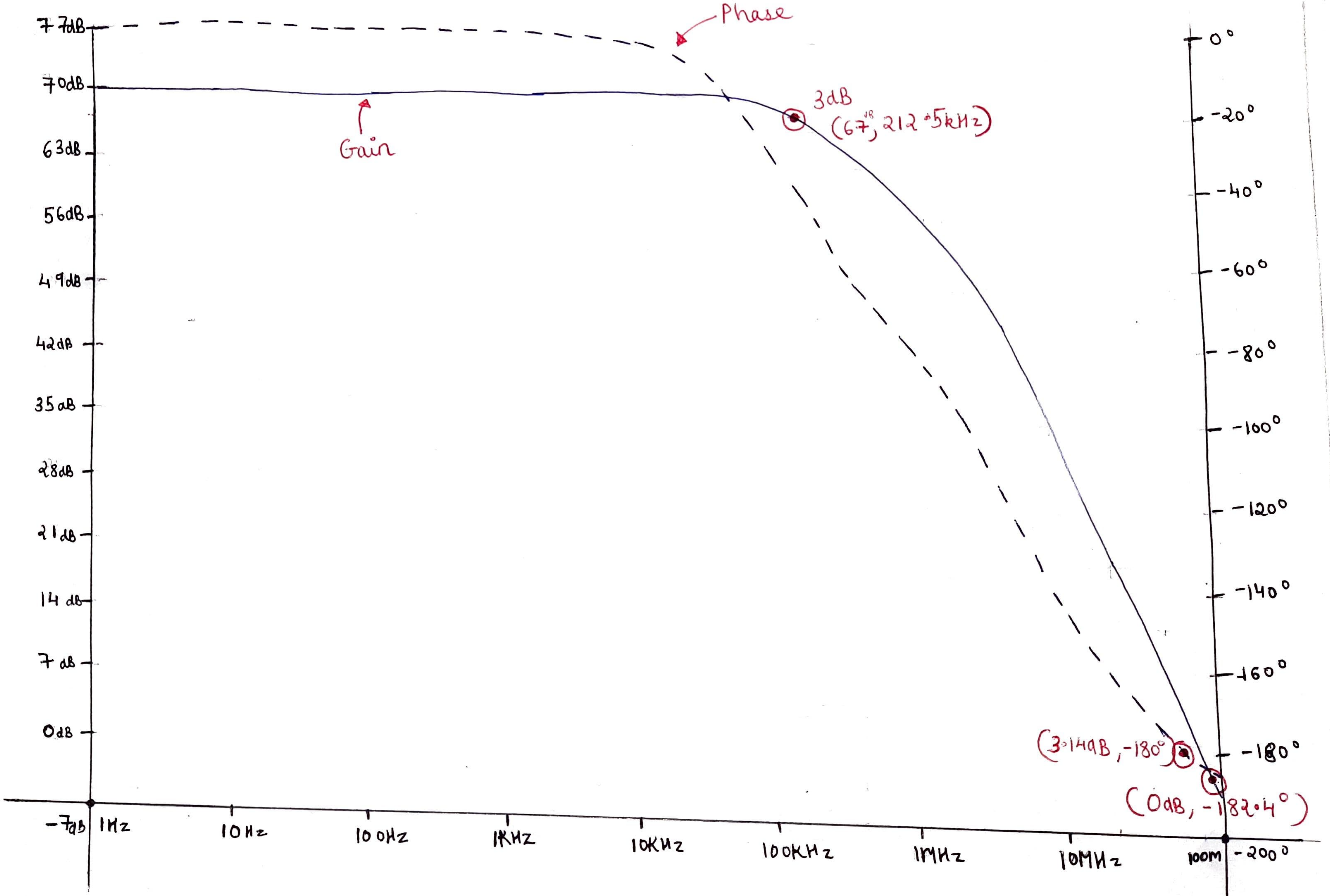

CSA .

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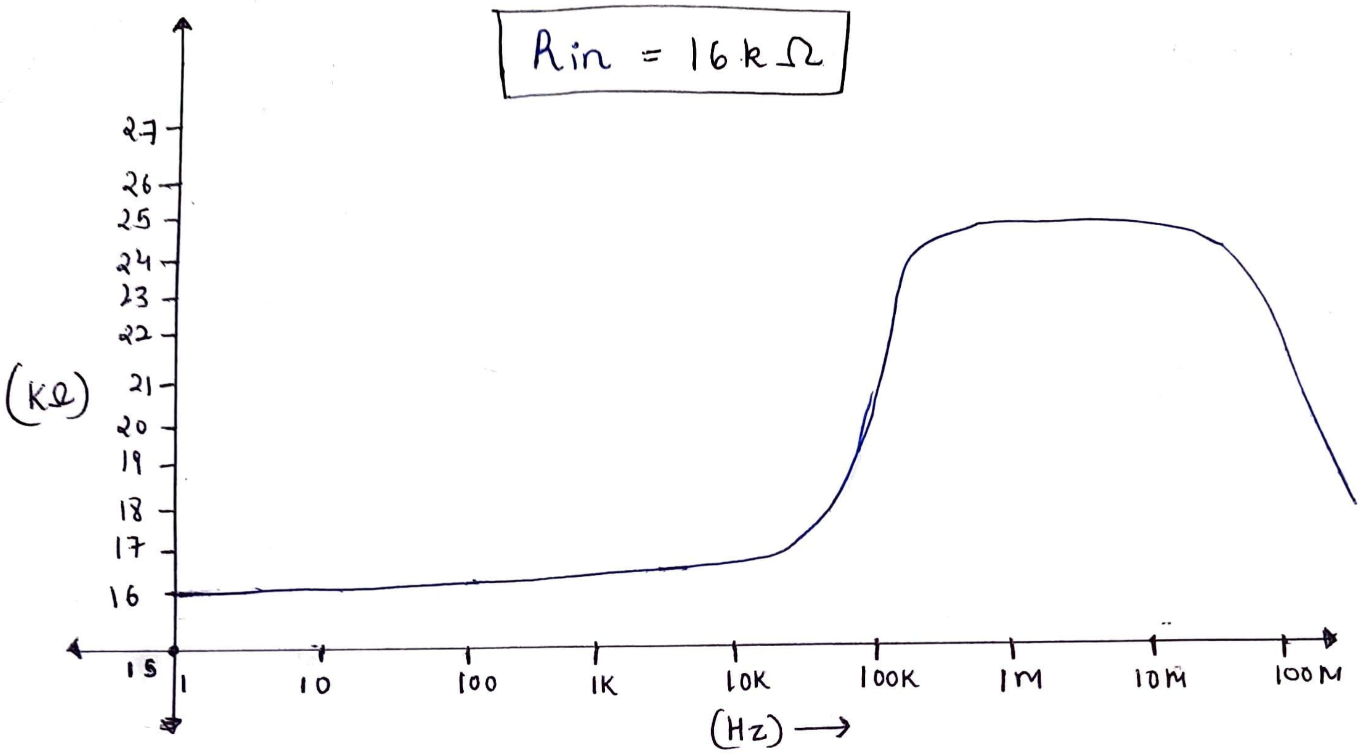
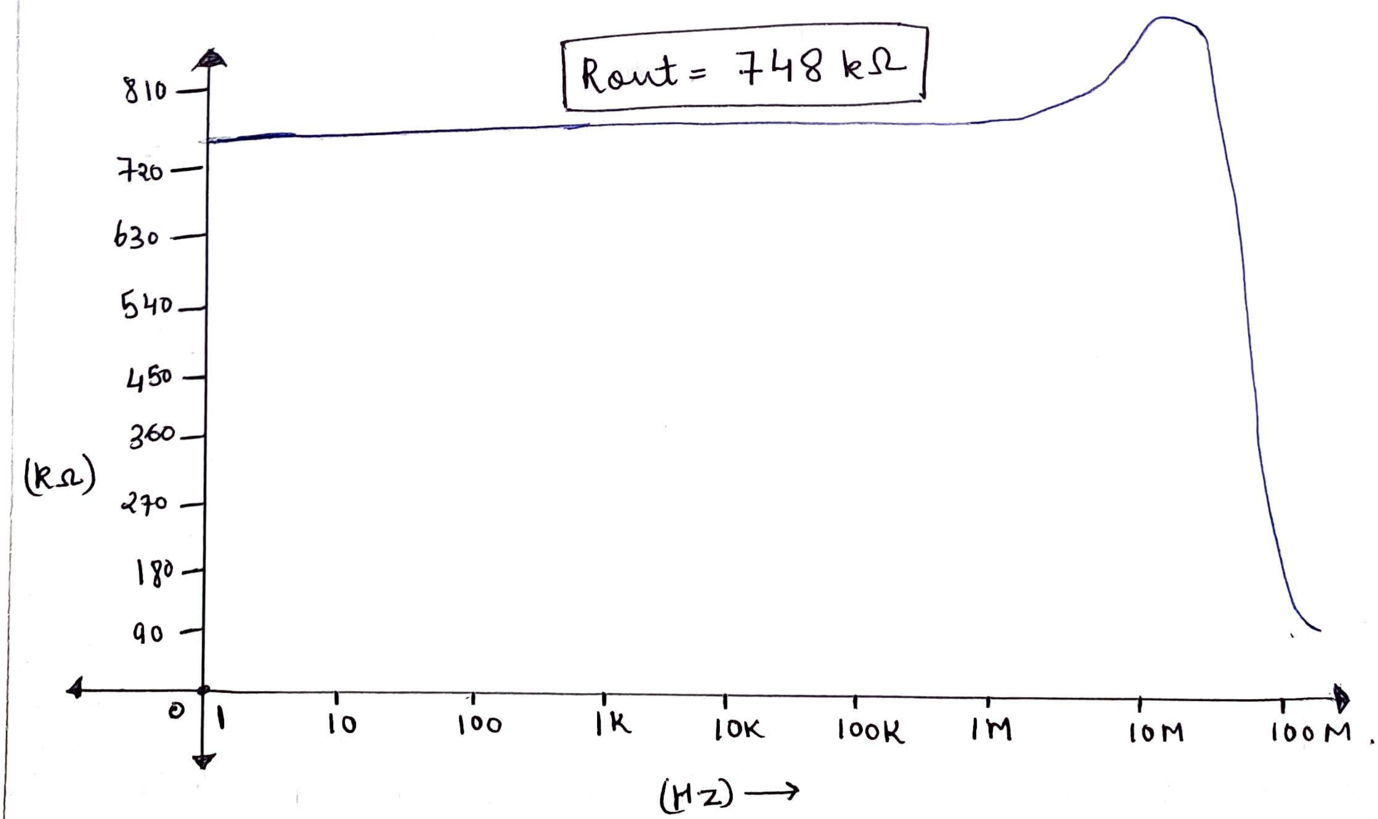




Problem-1

Code

```
* C:\Users\devan\Documents\assnmnt files(2)\final_1 - Copy.asc
M1 n2 in 0 0 NMOS l=1.2u w=20u
V1 in 0 SINE(756.88179m .2m 1k) AC 1
I1 n1 0 50µ
M2 n1 n1 N001 N001 PMOS l=1.2u w=50u
M3 n2 n1 N001 N001 PMOS l=1.2u w=4u
V2 N001 0 3.3
M4 out n2 0 0 NMOS l=1.2u w=1.145u
M5 out n1 N001 N001 PMOS l=1.2u w=14.571u
C1 out 0 7.2p
.model NMOS NMOS
.model PMOS PMOS
.lib C:\Users\devan\Documents\LTspiceXVII\lib\cmp\standard.mos
.op
;dc v1 0 5 0.0001
;tran 1
.opt plotwinsize=0
.include mue1.txt
;step param W 1.14u 1.15u 0.001u
;ac dec 1000 1 100Meg
.backanno
.end
```

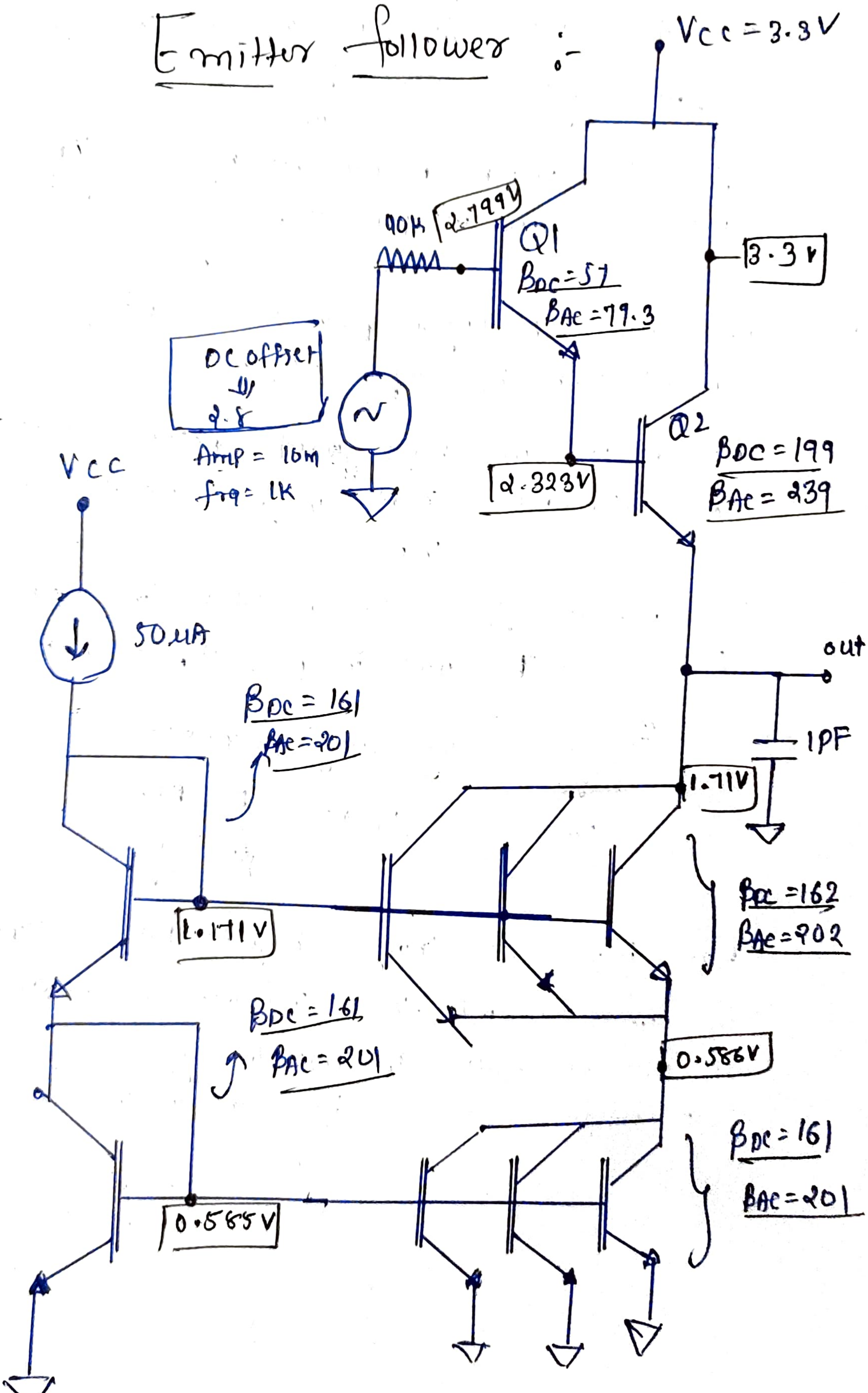
Error Log

```
Direct Newton iteration for .op point succeeded.
Semiconductor Device Operating Points:
                        --- BSIM3 MOSFETS ---
Name:        m5          m3          m2          m4          m1
Model:      pmos        pmos        pmos        nmos        nmos
Id:       -1.41e-05   -2.96e-06   -5.00e-05    1.41e-05    2.96e-06
Vgs:      -1.17e+00   -1.17e+00   -1.17e+00    1.93e+00    7.57e-01
Vds:      -1.57e+00   -1.37e+00   -1.17e+00    1.73e+00    1.93e+00
Vbs:       0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00
Vth:      -9.30e-01   -9.45e-01   -9.26e-01    1.15e+00    6.74e-01
Vdsat:    -2.22e-01   -2.08e-01   -2.27e-01    4.87e-01    6.74e-02
Gm:        1.14e-04    2.58e-05    4.02e-04    3.20e-05    6.54e-05
Gds:       9.20e-07    2.11e-07    3.77e-06    4.16e-07    2.80e-07
Gmb        3.36e-05    7.64e-06    1.18e-04    1.33e-05    2.25e-05
Cbd:       0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00
Cbs:       0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00
Cgsov:     4.06e-15    9.95e-16    1.43e-14    1.30e-16    3.90e-15
Cgdov:     4.06e-15    9.95e-16    1.43e-14    1.30e-16    3.90e-15
```

```
Cgbov:     1.09e-15    1.09e-15    1.09e-15    1.13e-15    1.13e-15
dQgdVgb:   3.88e-14    1.04e-14    1.34e-13    2.87e-15    4.98e-14
dQgdVdb:  -4.06e-15   -9.96e-16   -1.43e-14   -1.28e-16   -3.84e-15
dQgdVsb:  -3.14e-14   -7.73e-15   -1.11e-13   -1.52e-15   -3.61e-14
dQddVgb:  -1.67e-14   -4.08e-15   -5.89e-14   -7.38e-16   -2.03e-14
dQddVdb:   4.06e-15    9.96e-16    1.43e-14    1.29e-16    3.86e-15
dQddVsb:   1.65e-14    4.04e-15    5.82e-14    8.84e-16    2.24e-14
dQbdVgb:  -5.49e-15   -2.19e-15   -1.64e-14   -1.40e-15   -9.08e-15
dQbdVdb:  -4.24e-19   -1.64e-19   -4.71e-18    5.87e-19    2.24e-17
dQbdVsb:  -5.61e-15   -1.35e-15   -2.00e-14   -3.79e-16   -1.26e-14



Date: Sun Apr 11 17:45:44 2021
Total elapsed time: 0.097 seconds.

tnom = 27
temp = 27
method = trap
totiter = 13
traniter = 0
tranpoints = 0
accept = 0
rejected = 0
matrix size = 7
fillins = 0
solver = Normal
Matrix Compiler1: 312 bytes object code size
Matrix Compiler2: 555 bytes object code size
```

PROBLEM-2

Emitter follower :-



* Design Methodology :-

Note :- Here in case of BJTs, we can only change I_C to control g_m and r_π because of

$g_m = \frac{I_C}{V_t}$, $r_\pi = \frac{\beta}{g_m}$

So, to obtain proper biasing multiple BJTs are used in parallel.

[1] we used Darlington pair to amplify current gain by larger factor.

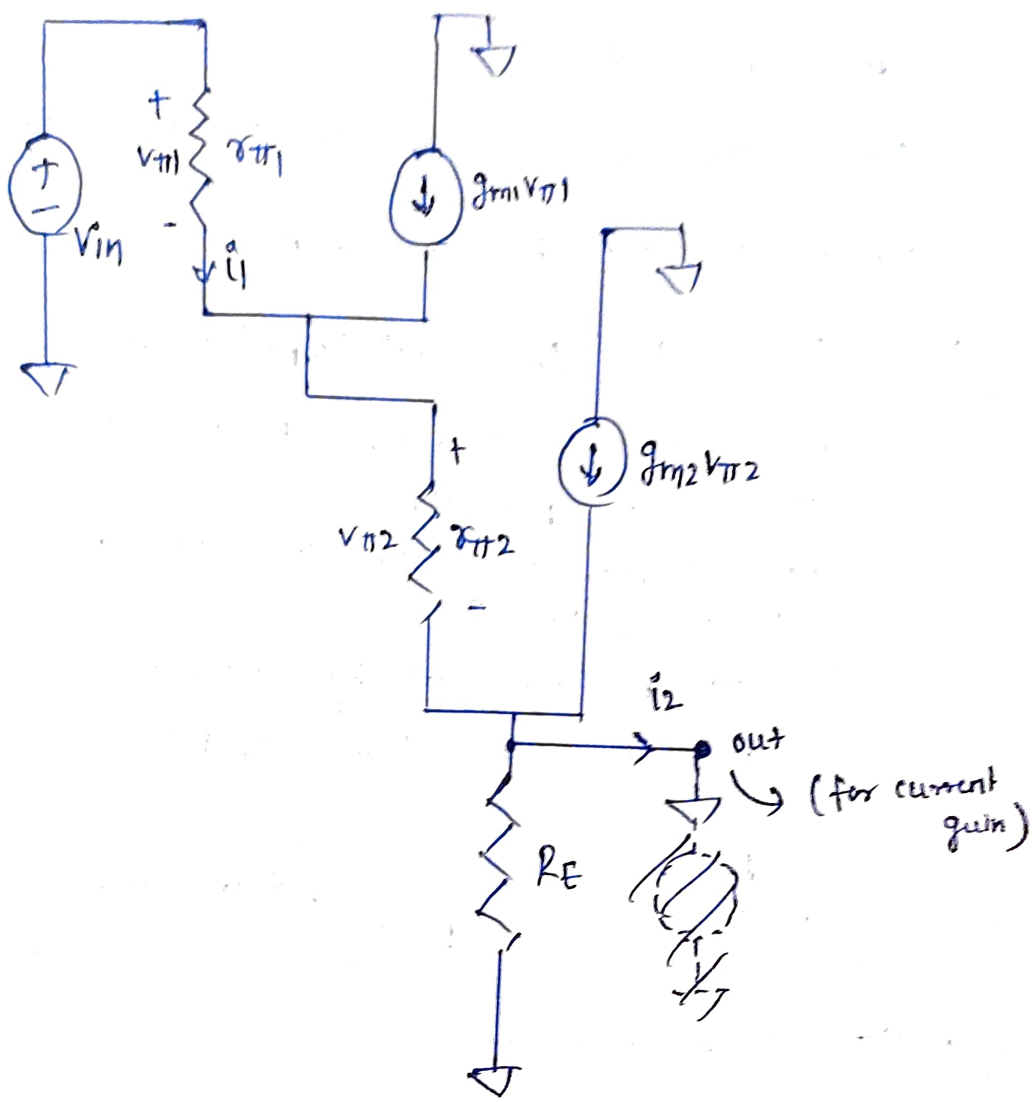
[2] ~~As~~ $\alpha < \alpha$ we have used Active Cascode load to get $\frac{V_{out}}{V_{in}}$ very close to unity.

[3] To increase g_m I_C should be increased so, 3 BJTs used in parallel, so net

$I_C = \frac{3 I_{REF}}{1 + \frac{4}{\beta_{AC}}}$, by using expression $I_{net} = \frac{N \cdot I_{REF}}{1 + \frac{(N+1)}{\beta}}$

[4] but here one thing should be ~~go~~ kept in ~~mid~~ mind that r_π decreases ~~drastically~~ as well as with increase in g_m, so current gain might decrease by further increase in I_C.

* Small signal model :-



* Current gain :-

i_2 can be simply calculated by following methods

$i_2 = i_1(\beta_1+1)(\beta_2+1)$, $\beta_1, \beta_2 \rightarrow$ Ac current gains.

$A_i = (\beta_1+1)(\beta_2+1)$

by putting values,

$\boxed{A_i = 19120 \ A/A}$

$= 85.48$ dB

And note that

A_i (simulated) $= 85.652$ dB

$$R_{out} = R_E \,\Big\|\, \left[\left(r_{e2} + \frac{r_{e1} + [R_{sig} / (\beta_2+1)]}{\beta_2+1} \right) \right]$$

Here note that,

$R_E \rightarrow$ active load of emitter degeneration.

it can be calculated by this expression.

$$R_E = (r_{o5}/3) + (g_{m5} \cdot r_{o5} + 1)(r_{\pi 5} \,\|\, (r_{o6}/3))$$

→ here we used $r_{o5}/3$ because 3 BJTs are in parallel,

→ And $3g_{m5}$ is used for equivalent current gain.

→ It can be understood by assuming 3 BJTs as one $(3g_m, \frac{r_o}{3})$ BJT.

$r_{e2} = \frac{r_{\pi 2}}{\beta_2+1}$, $r_{e1} = \frac{r_{\pi 1}}{\beta_1+1}$, $R_{sig} = 40\,k\Omega$

putting all the values,

$R_{out} = 341.4577\ \Omega$

while, R_{out}(simulated) $= 335\ \Omega$, which is quite close to hand-calculated.

Rin can be calculated by following expression

$$R_{in} = R_{sig} + (\beta_1+1)\left[r_{e1} + (\beta_2+1)(r_{e2} + R_E)\right]$$

Putting all the values,
we get

$R_{in} =$ ~~5.56 MΩ~~ $3.56 \times 10^{9}\,\Omega$

while ~~calculated~~ simulated $R_{in} = 3.6 \times 10^{9}\,\Omega$

* **Specification Review :-**

[1] Current gain :-

Required → 85 dB
Obtained → 85.41 dB
Justification → not required

[2] -3 dB frequency :-

Required → 50 KHz
Obtained → 2.322 KHz
Justification → Because of ~~output~~ ~~resistance~~ internal capacitance of BJT is too high so pole is shifted left, and note that current gain ~~of~~ will not depend on load capacitance because of we are grounding output terminal. ~~and~~

4.) output swing

Required → 2.64V
Obtained → 1.93V (0.717 – 2.64)
Justification → Because, we used darling ton pair, that's why output swing will be limited by $V_{CC} - (V_{CE_1} + V_{BE_2})$ in upper boud which is approx. 2.64 V and we have used Cascoded load so there also ~~Sam~~ swing is limited by $V_{BE} + V_{CE}$ in lower bound, so much higher part of Vcc is used in keeping all BJTs in active region.

5.) Phase - Margin

Required → 45°
Obtained → 126.168°
Justification → much better than required, but one thing must be noted that this configuration has high phase margin, and low 3dB frequency while in problem-1 configuration, which had higher 3dB frequency and lower phase margin, in that we can control by load capacitance but in this case we can not.

6.) Power Dissipation

Required → 3mW
Obtained → 501.6 μW
Justification → much less than required, so better performance.

* Small signal Parameters of all BJTs

Q1 (NPN)
$g_m = 2.71 \times 10^{-5}$ A/A
~~r_π~~ R_π : 4.92 MΩ
$r_o = 8.56 \times 10^{7}$ Ω
= 85.6 MΩ
$\beta_{DC} = 57$ $\beta_{AC} = 79.3$

Q2 (NPN)
$g_m = 5.49 \times 10^{-3}$ A/A
$r_\pi = 4.34 \times 10^{4}$ Ω
$r_o = 4.26 \times 10^{5}$ Ω
$\beta_{DC} = 199$
$\beta_{AC} = 239$

Q3 (~~PNP~~) NPN
$g_m = 1.89 \times 10^{-3}$ A/A
$r_\pi = 1.07 \times 10^{5}$ Ω
$r_o = 1.22 \times 10^{6}$ Ω
$\beta_{DC} = 161$
$\beta_{AC} = 201$

Q4 (~~PNP~~) NPN
$g_m = 1.85 \times 10^{-3}$ A/A
$r_\pi = 1.08 \times 10^{5}$ Ω
$r_o = 1.24 \times 10^{6}$ Ω
$\beta_{DC} = 161$
$\beta_{AC} = 201$

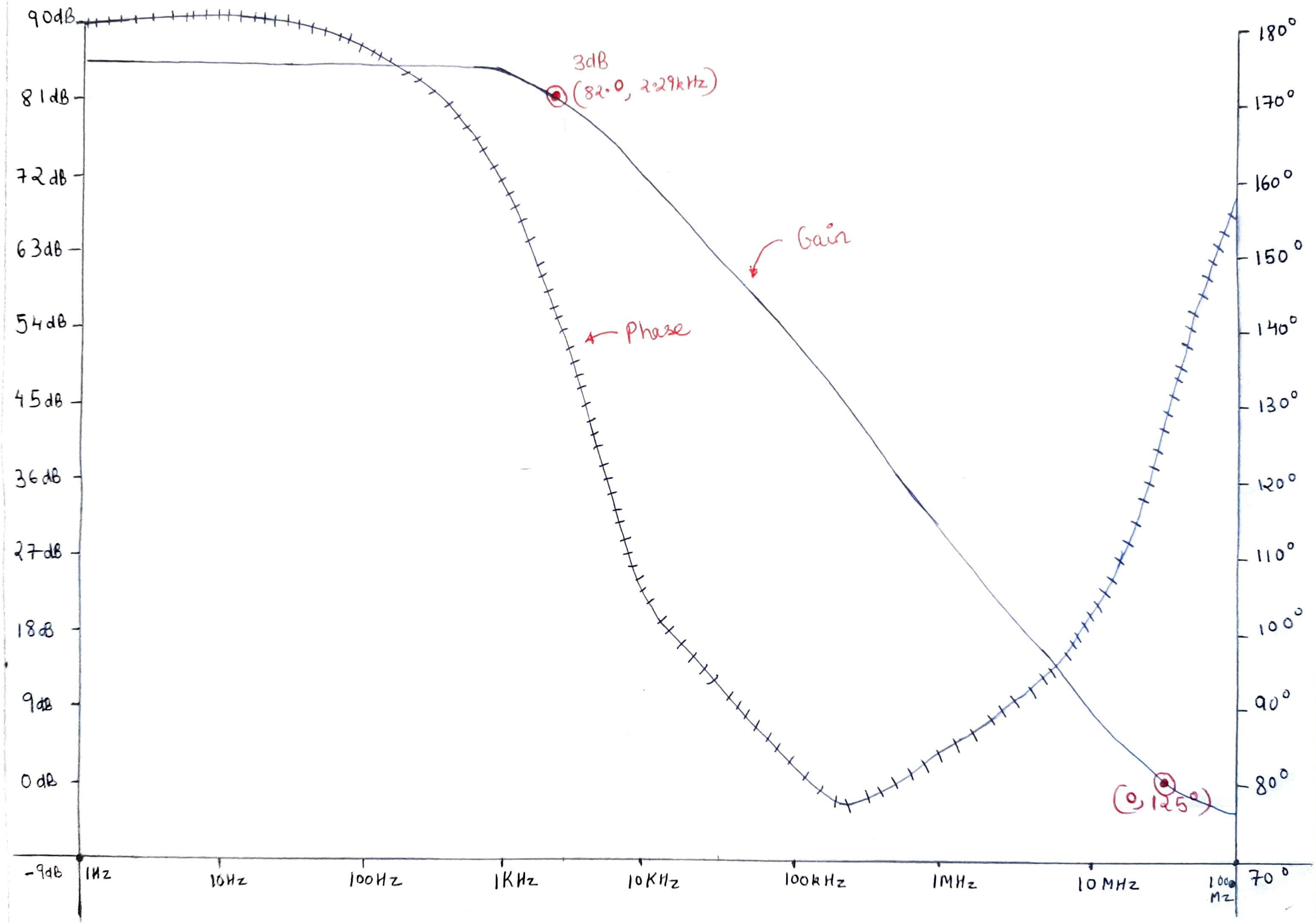
Q5, Q9, Q11
(NPN)
$g_m = 1.84 \times 10^{-3}$ A/A
$r_\pi = 1.10 \times 10^{5}$ Ω
$r_o = 1.26 \times 10^{6}$ Ω
$\beta_{DC} = \cancel{1.62 \times 10^{2}}$ 162
$\beta_{AC} = 202$

Q6, Q10, Q12
(NPN)
$g_m = 1.85 \times 10^{-3}$ A/A
$r_\pi = 1.08 \times 10^{5}$ Ω
$r_o = 1.24 \times 10^{6}$ Ω
$\beta_{DC} = 161$
$\beta_{AC} = 201$

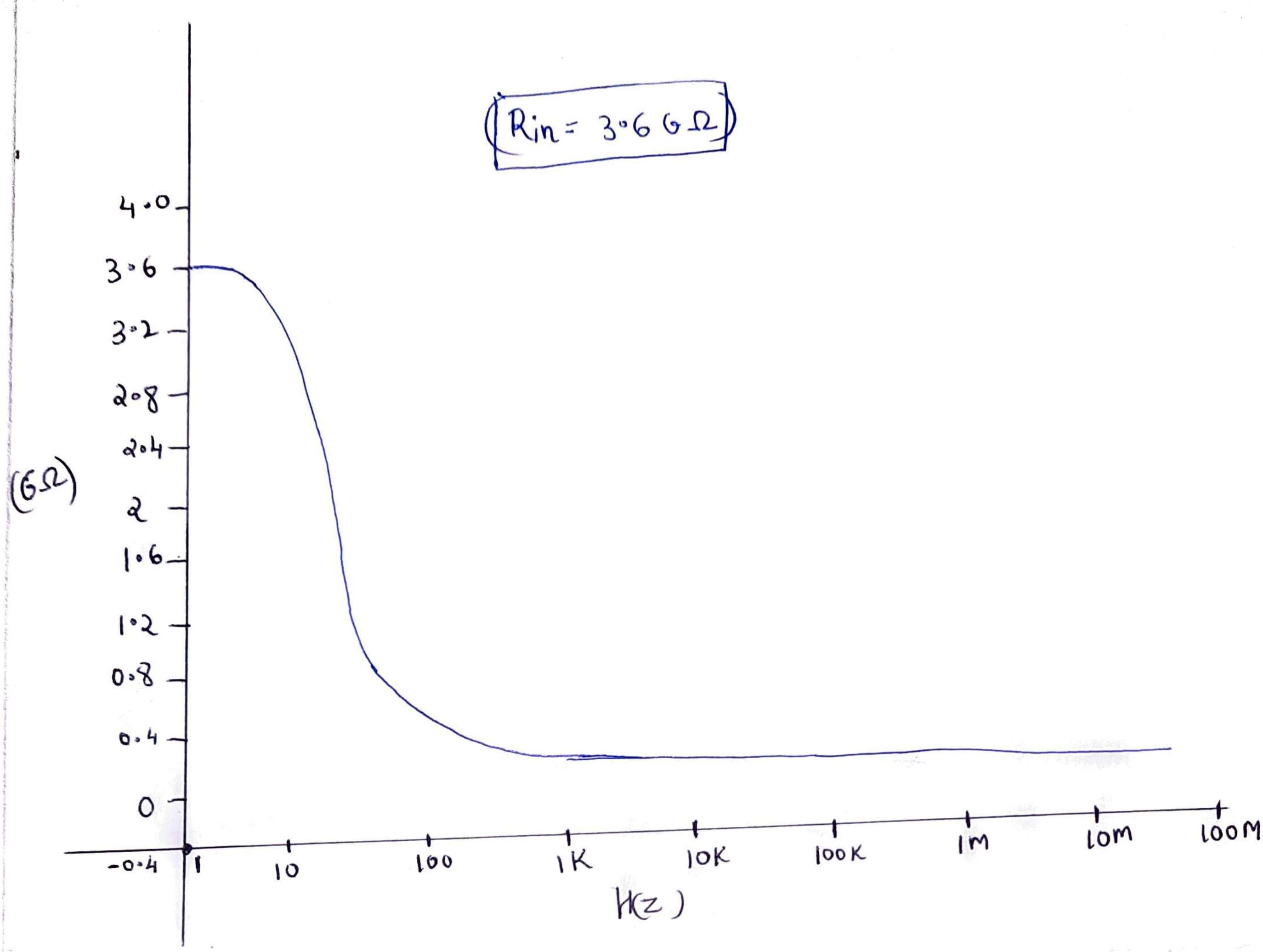
* AC analysis :-

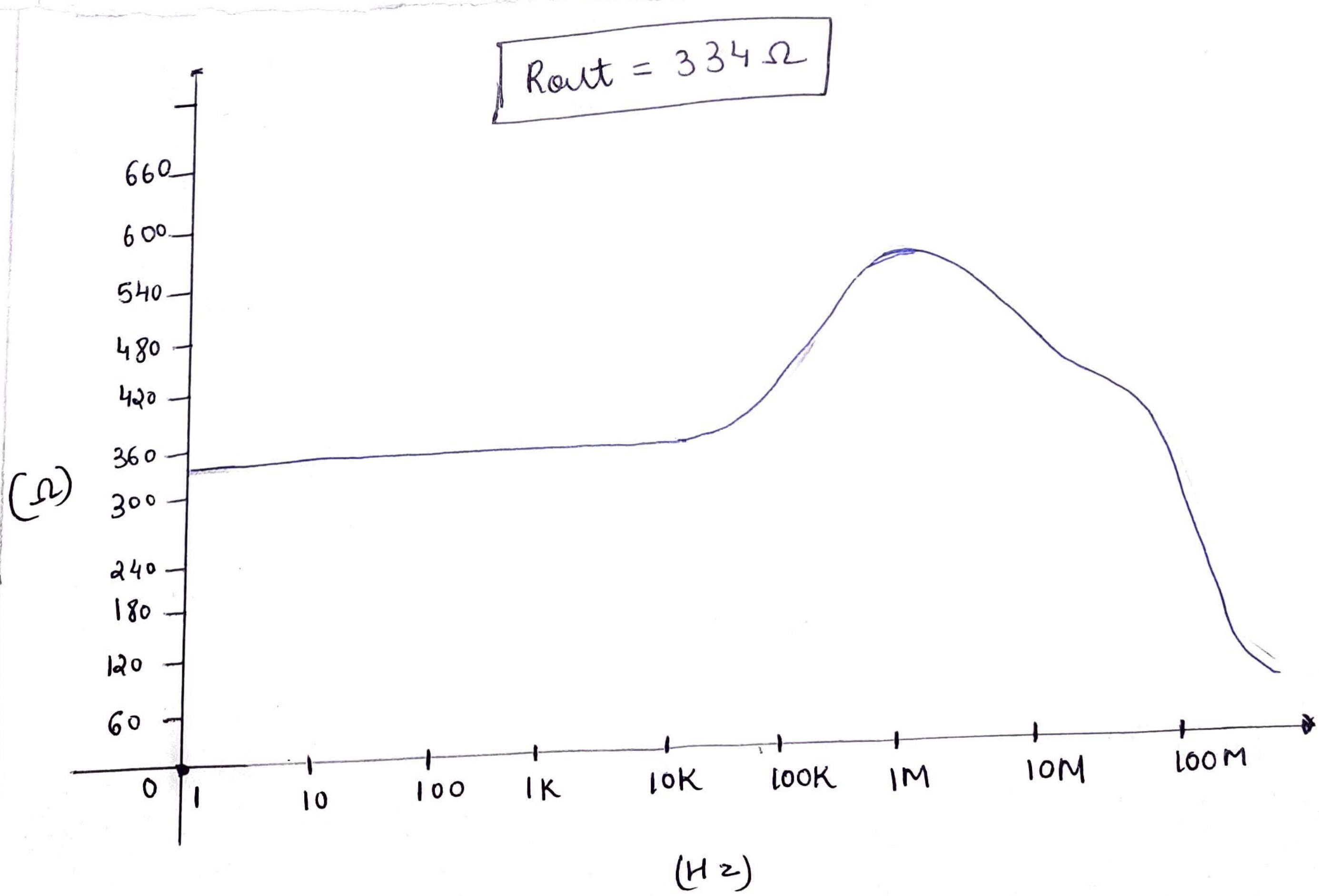
2019A3PS0200P | 2019A3PS0258P

Current Gain



2019A3PS0200P | 2019A3PS0158P





Problem-2

Code

```
* C:\Users\devan\Documents\assnmnt files(2)\final_q2 - Copy.asc
Q1 Vcc N001 N002 0 4
Q2 Vcc N002 out 0 4
Q3 N003 N003 N005 0 4
I1 Vcc N003 50µ
Vin in 0 SINE(2.8 10m 1k) AC 10m
V1 Vcc 0 3.3
Q4 N005 N005 0 0 4
Q5 out N003 N004 0 4
Q6 N004 N005 0 0 4
C2 out 0 1p
Q9 out N003 N004 0 4
Q10 N004 N005 0 0 4
Q11 out N003 N004 0 4
Q12 N004 N005 0 0 4
R1 N001 in 40k
V2 out 0 1.71008
.model NPN NPN
.model PNP PNP
.lib C:\Users\devan\Documents\LTspiceXVII\lib\cmp\standard.bjt
.include mue1.txt
;dc vin 1.3 10 0.0001
;ac dec 1000 1 100Meg
.MODEL 1 ako:BC107A
.MODEL 2 ako:BC107B
.MODEL 3 ako:BC108A
.op
.plot Ie(Q2)/Ib(Q1)
.MODEL 4 ako:BC108B
* 1700
* 1.71057
.backanno
.end
```

Error Log

```
Circuit: * C:\Users\devan\Documents\assnmnt files(2)\final_q2 - Copy.asc

Direct Newton iteration for .op point succeeded.
Semiconductor Device Operating Points:
                        --- Bipolar Transistors ---
Name:       q12         q11         q10         q9          q8
Model:       4           4           4           4           4
```

```
Ib:        2.98e-07    2.94e-07    2.98e-07    2.94e-07    3.72e-16
Ic:        4.79e-05    4.76e-05    4.79e-05    4.76e-05    1.74e-09
Vbe:       5.86e-01    5.85e-01    5.86e-01    5.85e-01    3.17e-01
Vbc:      -8.67e-04   -5.38e-01   -8.67e-04   -5.38e-01   -1.33e+00
Vce:       5.86e-01    1.12e+00    5.86e-01    1.12e+00    1.65e+00
BetaDC:    1.61e+02    1.62e+02    1.61e+02    1.62e+02    4.67e+06
Gm:        1.85e-03    1.84e-03    1.85e-03    1.84e-03    5.97e-08
Rpi:       1.08e+05    1.10e+05    1.08e+05    1.10e+05    2.01e+08
Rx:        0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00
Ro:        1.24e+06    1.26e+06    1.24e+06    1.26e+06    3.95e+10
Cbe:       1.98e-11    1.98e-11    1.98e-11    1.98e-11    1.49e-11
Cbc:       5.38e-12    4.38e-12    5.38e-12    4.38e-12    3.69e-12
Cjs:       0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00
BetaAC:    2.01e+02    2.02e+02    2.01e+02    2.02e+02    1.20e+01
Cbx:       0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00
Ft:        1.17e+07    1.21e+07    1.17e+07    1.21e+07    5.09e+02

Name:        q7          q6          q5          q4          q3
Model:        4           4           4           4           4
Ib:        3.72e-16    2.98e-07    2.94e-07    2.98e-07    3.02e-07
Ic:        1.74e-09    4.79e-05    4.76e-05    4.79e-05    4.88e-05
Vbe:       3.17e-01    5.86e-01    5.85e-01    5.86e-01    5.86e-01
Vbc:      -1.33e+00   -8.67e-04   -5.38e-01    0.00e+00    0.00e+00
Vce:       1.65e+00    5.86e-01    1.12e+00    5.86e-01    5.86e-01
BetaDC:    4.67e+06    1.61e+02    1.62e+02    1.61e+02    1.61e+02
Gm:        5.97e-08    1.85e-03    1.84e-03    1.85e-03    1.89e-03
Rpi:       2.01e+08    1.08e+05    1.10e+05    1.08e+05    1.07e+05
Rx:        0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00
Ro:        3.95e+10    1.24e+06    1.26e+06    1.24e+06    1.22e+06
Cbe:       1.49e-11    1.98e-11    1.98e-11    1.98e-11    1.98e-11
Cbc:       3.69e-12    5.38e-12    4.38e-12    5.38e-12    5.38e-12
Cjs:       0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00
BetaAC:    1.20e+01    2.01e+02    2.02e+02    2.01e+02    2.01e+02
Cbx:       0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00
Ft:        5.09e+02    1.17e+07    1.21e+07    1.17e+07    1.19e+07

Name:        q2          q1
Model:        4           4
Ib:        7.15e-07    1.23e-08
Ic:        1.42e-04    7.02e-07
Vbe:       6.13e-01    4.76e-01
Vbc:      -9.77e-01   -5.00e-01
Vce:       1.59e+00    9.77e-01
BetaDC:    1.99e+02    5.70e+01
Gm:        5.49e-03    2.71e-05
Rpi:       4.34e+04    2.92e+06
Rx:        0.00e+00    0.00e+00
Ro:        4.26e+05    8.56e+07
Cbe:       2.18e-11    1.73e-11
Cbc:       3.94e-12    4.43e-12
Cjs:       0.00e+00    0.00e+00
BetaAC:    2.39e+02    7.93e+01
Cbx:       0.00e+00    0.00e+00
Ft:        3.40e+07    1.99e+05



Date: Sun Apr 11 22:38:02 2021
```

```
Total elapsed time: 0.160 seconds.

tnom = 27
temp = 27
method = trap
totiter = 17
traniter = 0
tranpoints = 0
accept = 0
rejected = 0
matrix size = 26
fillins = 2
solver = Normal
Matrix Compiler1: 1.88 KB object code size
Matrix Compiler2: 2.25 KB object code size
```