Shri Vile Parle Kelavani Mandal's

DWARKADAS J. SANGHVI COLLEGE OF ENGINEERING

(Autonomous College Affiliated to the University of Mumbai)

NAAC Accredited with "A" Grade (CGPA : 3.18)

A.Y. 2022-2023

Subject: Process Organization and Architecture **SAP ID: 60004220253 – Devansh Mehta**

Experiment No: 05

Aim: Assembly program for 16-bit Addition / Subtraction using Direct, Immediate and Register Addressing Mode.

CODE:

Addition:

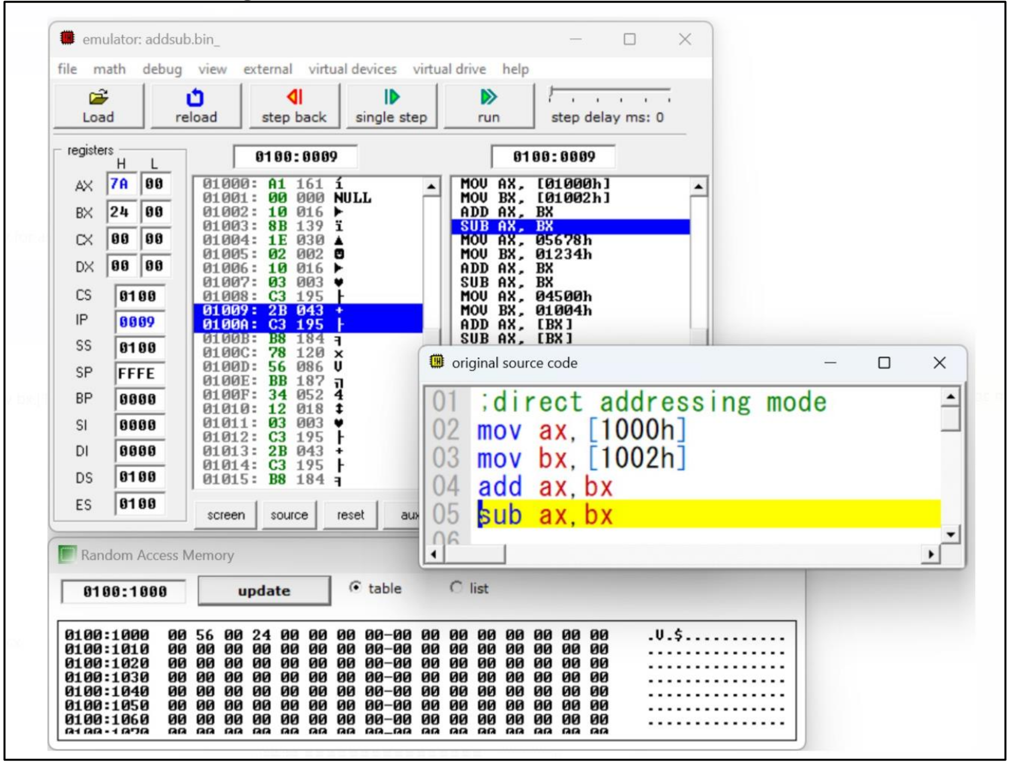
```
org 1000h

mov ax,[1000h]
mov bx,[1002h]
add ax,bx

mov ax,1234h
mov bx,0005h
add ax,bx

mov ax,1234h
mov bx,1000h
add ax,[bx]
Hlt
```

Subtraction:

```
org 1000h

mov ax,[1000h]
mov bx,[1002h]
sub ax,bx

mov ax,1234h
mov bx,0005h
sub ax,bx

mov ax,1234h
mov bx,1000h
sub ax,[bx]
Hlt
```

OUTPUT:

Direct addressing mode (Addition):



```
registers
     H    L
AX   7A   00
BX   24   00
CX   00   00
DX   00   00
CS   0100
IP   0009
SS   0100
SP   FFFE
BP   0000
SI   0000
DI   0000
DS   0100
ES   0100
```

```
0100:0009
01000: A1 161 í
01001: 00 000 NULL
01002: 10 016 ►
01003: 8B 139 ï
01004: 1E 030 ▲
01005: 02 002 ☻
01006: 10 016 ►
01007: 03 003 ♥
01008: C3 195 ├
01009: 2B 043 +
0100A: C3 195 ├
0100B: B8 184 ╕
0100C: 78 120 x
0100D: 56 086 V
0100E: BB 187 ╗
0100F: 34 052 4
01010: 12 018 ↕
01011: 03 003 ♥
01012: C3 195 ├
01013: 2B 043 +
01014: C3 195 ├
01015: B8 184 ╕
```

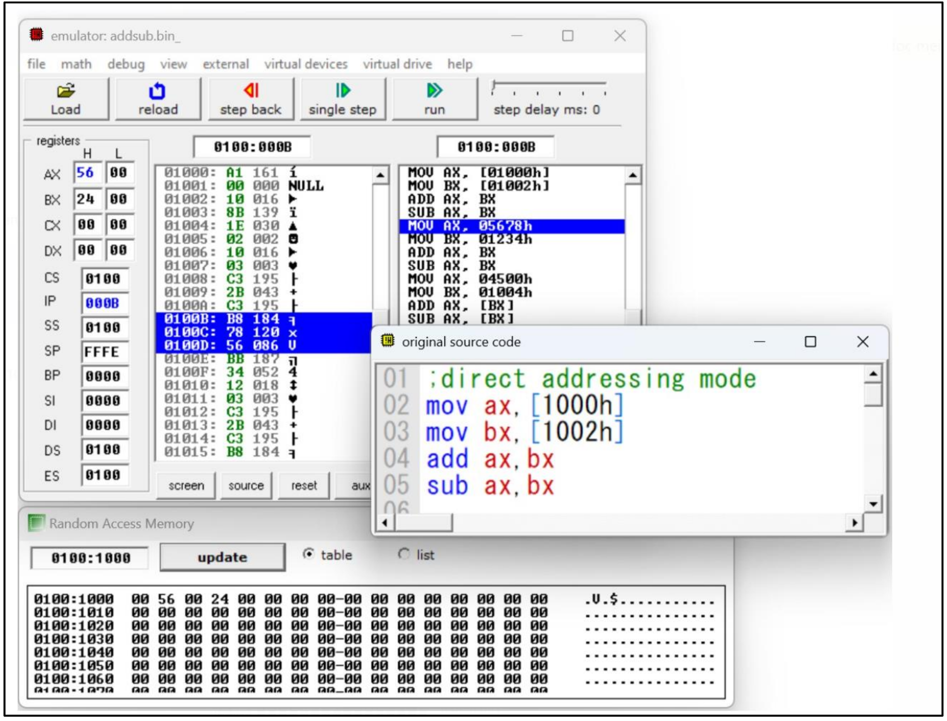
```
0100:0009
MOV AX, [01000h]
MOV BX, [01002h]
ADD AX, BX
SUB AX, BX
MOV AX, 05678h
MOV BX, 01234h
ADD AX, BX
SUB AX, BX
MOV AX, 04500h
MOV BX, 01004h
ADD AX, [BX]
SUB AX, [BX]
```

```
;direct addressing mode
mov ax, [1000h]
mov bx, [1002h]
add ax, bx
sub ax, bx
```

0100:1000 ● table ○ list

```
0100:1000  00 56 00 24 00 00 00 00-00 00 00 00 00 00 00 00   .V.$............
0100:1010  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00   ................
0100:1020  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00   ................
0100:1030  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00   ................
0100:1040  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00   ................
0100:1050  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00   ................
0100:1060  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00   ................
```

Direct addressing mode (Subtraction):



```
registers  H   L
AX        56  00
BX        24  00
CX        00  00
DX        00  00
CS   0100
IP   000B
SS   0100
SP   FFFE
BP   0000
SI   0000
DI   0000
DS   0100
ES   0100
```

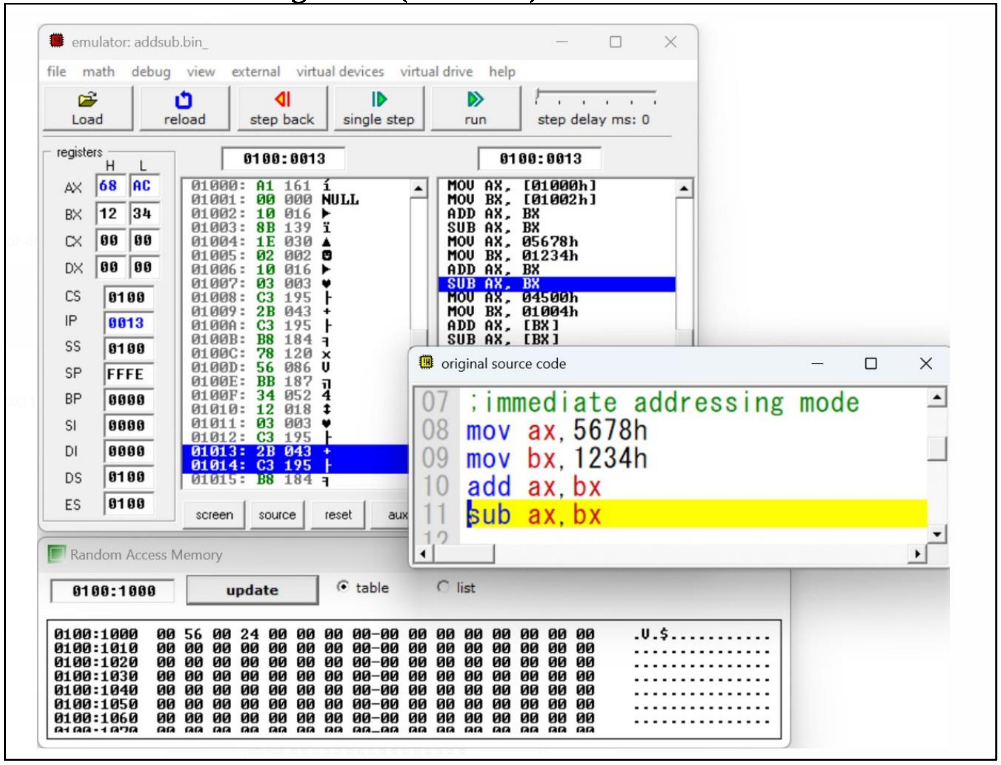
```
0100:000B
01000: A1 161 í
01001: 00 000 NULL
01002: 10 016 ►
01003: 8B 139 ï
01004: 1E 030 ▲
01005: 02 002 ☻
01006: 10 016 ►
01007: 03 003 ♥
01008: C3 195 ├
01009: 2B 043 +
0100A: C3 195 ├
0100B: B8 184 ╕
0100C: 78 120 x
0100D: 56 086 V
0100E: BB 187 ╗
0100F: 34 052 4
01010: 12 018 ↕
01011: 03 003 ♥
01012: C3 195 ├
01013: 2B 043 +
01014: C3 195 ├
01015: B8 184 ╕
```

```
0100:000B
MOV AX, [01000h]
MOV BX, [01002h]
ADD AX, BX
SUB AX, BX
MOV AX, 05678h
MOV BX, 01234h
ADD AX, BX
SUB AX, BX
MOV AX, 04500h
MOV BX, 01004h
ADD AX, [BX]
SUB AX, [BX]
```

```
;direct addressing mode
mov ax, [1000h]
mov bx, [1002h]
add ax, bx
sub ax, bx
```

```
0100:1000
0100:1000  00 56 00 24 00 00 00 00-00 00 00 00 00 00 00 00   .V.$............
0100:1010  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00   ................
0100:1020  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00   ................
0100:1030  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00   ................
0100:1040  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00   ................
0100:1050  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00   ................
0100:1060  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00   ................
```

Immediate addressing mode (Addition):



```
registers  H   L
AX        68  AC
BX        12  34
CX        00  00
DX        00  00
CS   0100
IP   0013
SS   0100
SP   FFFE
BP   0000
SI   0000
DI   0000
DS   0100
ES   0100
```

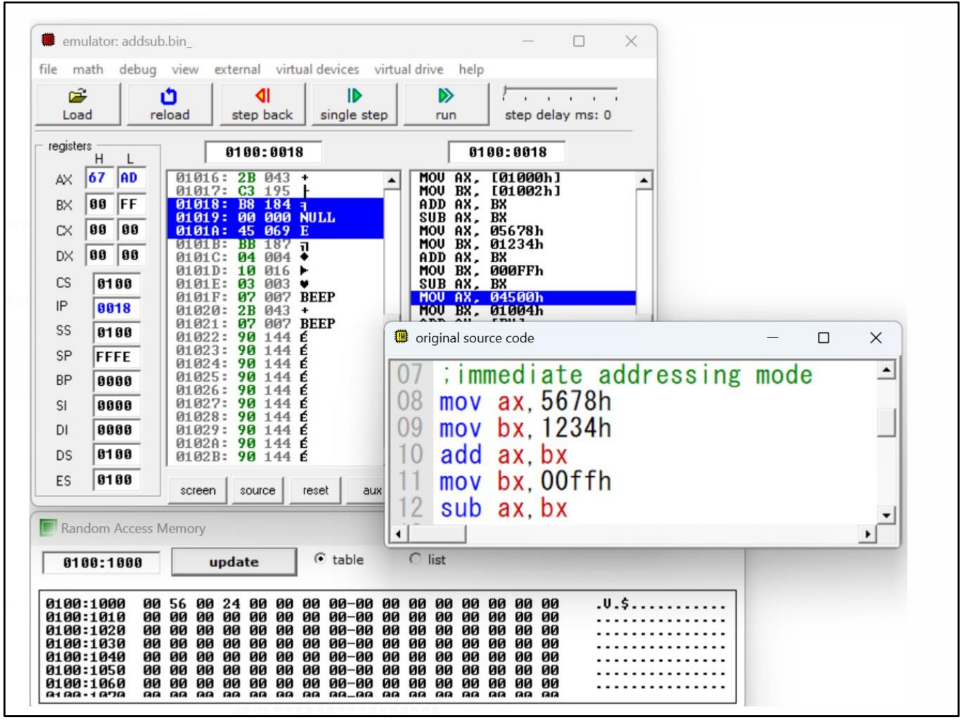
```
0100:0013
01000: A1 161 í
01001: 00 000 NULL
01002: 10 016 ►
01003: 8B 139 ï
01004: 1E 030 ▲
01005: 02 002 ☻
01006: 10 016 ►
01007: 03 003 ♥
01008: C3 195 ├
01009: 2B 043 +
0100A: C3 195 ├
0100B: B8 184 ╕
0100C: 78 120 x
0100D: 56 086 V
0100E: BB 187 ╗
0100F: 34 052 4
01010: 12 018 ↕
01011: 03 003 ♥
01012: C3 195 ├
01013: 2B 043 +
01014: C3 195 ├
01015: B8 184 ╕
```

```
0100:0013
MOV AX, [01000h]
MOV BX, [01002h]
ADD AX, BX
SUB AX, BX
MOV AX, 05678h
MOV BX, 01234h
ADD AX, BX
SUB AX, BX
MOV AX, 04500h
MOV BX, 01004h
ADD AX, [BX]
SUB AX, [BX]
```

```
;immediate addressing mode
mov ax, 5678h
mov bx, 1234h
add ax, bx
sub ax, bx
```

```
0100:1000
0100:1000  00 56 00 24 00 00 00 00-00 00 00 00 00 00 00 00   .V.$............
0100:1010  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00   ................
0100:1020  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00   ................
0100:1030  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00   ................
0100:1040  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00   ................
0100:1050  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00   ................
0100:1060  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00   ................
```

Immediate Addressing (Subtraction):

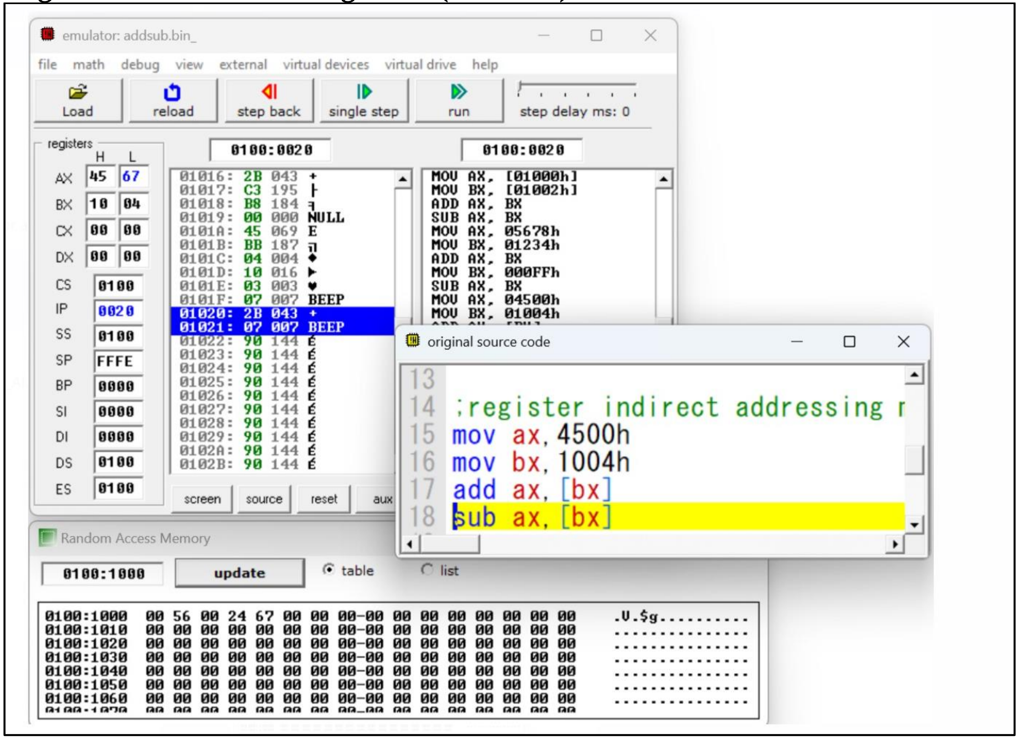

emulator: addsub.bin_
file math debug view external virtual devices virtual drive help
Load reload step back single step run step delay ms: 0
registers
screen source reset aux
original source code
Random Access Memory
update ● table ○ list

```
0100:0018                      0100:0018

     H   L
AX   67  AD     01016: 2B 043 +          MOV AX, [01000h]
BX   00  FF     01017: C3 195 ├          MOV BX, [01002h]
CX   00  00     01018: B8 184 ╕          ADD AX, BX
DX   00  00     01019: 00 000 NULL       SUB AX, BX
CS   0100       0101A: 45 069 E          MOV AX, 05678h
IP   0018       0101B: BB 187 ╗          MOV BX, 01234h
SS   0100       0101C: 04 004 ♦          ADD AX, BX
SP   FFFE       0101D: 10 016 ►          MOV BX, 000FFh
BP   0000       0101E: 03 003 ♥          SUB AX, BX
SI   0000       0101F: 07 007 BEEP       MOV AX, 04500h
DI   0000       01020: 2B 043 +          MOV BX, 01004h
DS   0100       01021: 07 007 BEEP
ES   0100       01022: 90 144 É
                01023: 90 144 É
                01024: 90 144 É
                01025: 90 144 É
                01026: 90 144 É
                01027: 90 144 É
                01028: 90 144 É
                01029: 90 144 É
                0102A: 90 144 É
                0102B: 90 144 É
```

```
;immediate addressing mode
mov ax,5678h
mov bx,1234h
add ax,bx
mov bx,00ffh
sub ax,bx
```

```
0100:1000

0100:1000  00 56 00 24 00 00 00 00-00 00 00 00 00 00 00 00  .V.$...........
0100:1010  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00  ...............
0100:1020  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00  ...............
0100:1030  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00  ...............
0100:1040  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00  ...............
0100:1050  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00  ...............
0100:1060  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00  ...............
```

Register indirect addressing mode (Addition):


emulator: addsub.bin_
file math debug view external virtual devices virtual drive help
Load reload step back single step run step delay ms: 0
registers
screen source reset aux
original source code
Random Access Memory
update ● table ○ list

```
0100:0020                      0100:0020

     H   L
AX   45  67     01016: 2B 043 +          MOV AX, [01000h]
BX   10  04     01017: C3 195 ├          MOV BX, [01002h]
CX   00  00     01018: B8 184 ╕          ADD AX, BX
DX   00  00     01019: 00 000 NULL       SUB AX, BX
CS   0100       0101A: 45 069 E          MOV AX, 05678h
IP   0020       0101B: BB 187 ╗          MOV BX, 01234h
SS   0100       0101C: 04 004 ♦          ADD AX, BX
SP   FFFE       0101D: 10 016 ►          MOV BX, 000FFh
BP   0000       0101E: 03 003 ♥          SUB AX, BX
SI   0000       0101F: 07 007 BEEP       MOV AX, 04500h
DI   0000       01020: 2B 043 +          MOV BX, 01004h
DS   0100       01021: 07 007 BEEP
ES   0100       01022: 90 144 É
                01023: 90 144 É
                01024: 90 144 É
                01025: 90 144 É
                01026: 90 144 É
                01027: 90 144 É
                01028: 90 144 É
                01029: 90 144 É
                0102A: 90 144 É
                0102B: 90 144 É
```

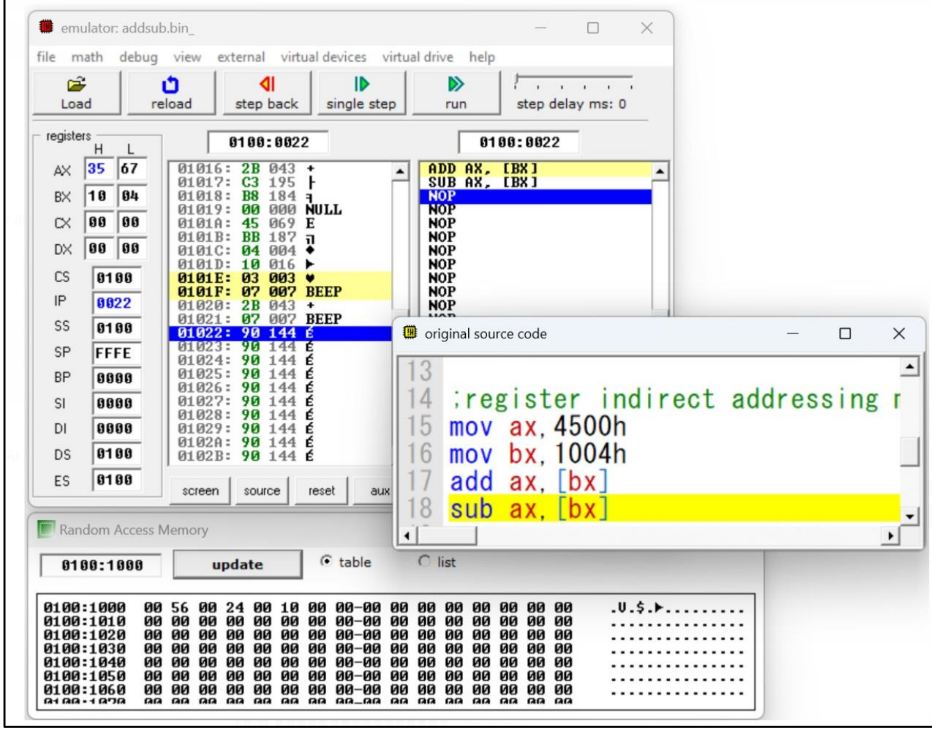
```

;register indirect addressing r
mov ax,4500h
mov bx,1004h
add ax,[bx]
sub ax,[bx]
```

```
0100:1000

0100:1000  00 56 00 24 67 00 00 00-00 00 00 00 00 00 00 00  .V.$g..........
0100:1010  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00  ...............
0100:1020  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00  ...............
0100:1030  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00  ...............
0100:1040  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00  ...............
0100:1050  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00  ...............
0100:1060  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00  ...............
```

A.Y. 2022-2023

Subject: Process Organization and Architecture SAP ID: 60004220253 – Devansh Mehta

Register indirect addressing mode (Subtraction):


emulator: addsub.bin_
file math debug view external virtual devices virtual drive help
Load reload step back single step run step delay ms: 0
screen source reset aux
original source code
Random Access Memory
update

registers

	H	L
AX	35	67
BX	10	04
CX	00	00
DX	00	00

CS	0100
IP	0022
SS	0100
SP	FFFE
BP	0000
SI	0000
DI	0000
DS	0100
ES	0100

```
0100:0022
01016: 2B 043 +
01017: C3 195 ├
01018: B8 184 ╕
01019: 00 000 NULL
0101A: 45 069 E
0101B: BB 187 ╗
0101C: 04 004 ♦
0101D: 10 016 ►
0101E: 03 003 ♥
0101F: 07 007 BEEP
01020: 2B 043 +
01021: 07 007 BEEP
01022: 90 144 É
01023: 90 144 É
01024: 90 144 É
01025: 90 144 É
01026: 90 144 É
01027: 90 144 É
01028: 90 144 É
01029: 90 144 É
0102A: 90 144 É
0102B: 90 144 É
```

```
0100:0022
ADD AX, [BX]
SUB AX, [BX]
NOP
NOP
NOP
NOP
NOP
NOP
NOP
NOP
NOP
NOP
```

```
;register indirect addressing r
mov ax, 4500h
mov bx, 1004h
add ax, [bx]
sub ax, [bx]
```

0100:1000 ● table ○ list

```
0100:1000  00 56 00 24 00 10 00 00-00 00 00 00 00 00 00 00   .V.$.►..........
0100:1010  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00   ................
0100:1020  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00   ................
0100:1030  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00   ................
0100:1040  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00   ................
0100:1050  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00   ................
0100:1060  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00   ................
0100:1070  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00
```