DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
B. E. SEM V INFORMATION TECHNOLOGY
THIRD SESSIONAL EXAMINATION
SUBJECT: ADVANCE MICROPROCESSOR ARCHITECTURE

Date: 15/10 /12 Seat No._____ Time: 11.15 to 12.30 Max. Marks: 36

Instruction: **No marks without justification.**
Calculator is not allowed.

Q-1 Answer the following.

[A] In data parallelism method, speedup is not directly proportional to the no. of processors. State True/False and justify. [2]

[B] Super scalar architecture uses both temporal and data parallelism. True/False and justify. [2]

[C] Difference between fine grained and coarse grained jobs. [2]

[D] If the percentage of unconditional branches is 10%, conditional branches is 18% and immediate instructions are 8% in programs executed in SMAC2P, calculate the average clock cycles required per instructions. [1]

[E] What is delay slot ? How it improves the delay due to control hazard ? [2]

[F] In one processor BTB size is 1024 and in other processor BTB size is 4096. Whose performance will be better ? Justify your answer (no marks without justification). [2]

[G] Pipelining increases the execution time of an individual instruction. State T/F and justify. [1]

Q-2 Answer Any Two. [12]

[A] An examination paper has 4 questions. The answer to these questions does not take equal time to correct. Answer to question 1 takes 4 min. to correct, question 2 takes 6 minutes, question 3 takes 5 minutes, and question 4 takes 8 minutes. Due to this speed mismatch storage should be provided between teachers. Answer the following questions assuming 2000 papers are to be corrected by 4 teachers. [6]

(i) What is the idle time of teachers?
(ii) What is the system efficiency?
(iii) How much tray space should be provided between teachers due to speed mismatch?
(iv) What will be efficiency if data parallel mode is given.

[B] i) In the pipeline mode of processing we assumed that there is no communication delay between stages of the pipeline . If there is a delay of y between pipeline stages derive a speed up formula. What condition should y satisfy to ensure a speedup of at least 0.8k where k is the no. of stages in the pipeline ? [4]

ii) Explain the differences between superscalar processors and multiscalar processors. [2]

[C] Draw the pipeline execution diagram for the following instructions of hypothetical processor SMAC2P : [6]

DIV R1, R5, R1
ADD R2, R1, R3
SUB R2, R5, R1

Draw the space-time diagram for above instructions by stalling the instruction for various hazards. Specify very clearly the cause of the stall. State the types of data dependency present in the above instructions set. Assuming register forwarding available, redraw the space-time diagram again.

Q-3 Answer the following. [12]

[A] The following expressions are to be evaluated. [6]

$a=g(p) + e^{-xf(y)} + h(x^2) + f(y)* g(p)$

$b= f(u^2) + \sin (g(p)) + \cos^2 h(y^2)$

1. Obtain task graph for calculating a and b.
2. Assuming 4 processors are available. Obtain task assignment to processors assuming the following timing for various operations.
   - Squaring=1, add=1,multiplication=1,
   - sin=cos=exponentiation=2 ,
   - g(x)=h(x)=f(x)=2

[B] (i) What is pipeline Hazards ? Explain various hazards due to non-ideal conditions present in pipelining processor. [3]

(ii) What is superscalar architecture ? Assuming ideal conditions. Draw the space-time diagram for 6 instructions. How many clock is saved compared to normal pipeline architecture ? [3]

OR

Q-3 [12]

[A] In the examination paper there are 4 questions and each will take on average 5 minutes to correct. 1000 candidates write examination. 4 teachers are employed to correct paper using pipeline mode. Every question is not answered by all candidates. 10% of candidates do not answer question 1, 15% question 2, 5% question 3, 25% question 4. [6]

i) How much time is taken to complete grading?
ii) What is the efficiency of pipeline processing?
iii) If data parallel method is used how much time will be taken to complete the grading?

[B] Explain the terms Pipeline stall and pipeline locking with the help of space-time diagram. What is the main advantage of pipeline locking over pipeline stall ? Explain how this will help to avoid WAW hazard. [6]