DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
THIRD SESSIONAL
SUBJECT NAME : (IT506) ADVANCED MICROPROCESSOR ARCHITECTURE

Examination	**: B.TECH - Semester - V**	**Seat No.**	**:**
Date	**: 07/10/2014**	**Day**	**: Tuesday**
Time	**: 11:15 TO 12:30**	**Max. Marks**	**: 36**

INSTRUCTIONS:
1. **Figures to the right indicate maximum marks for that question.**
2. **The symbols used carry their usual meanings.**
3. **Assume suitable data, if required & mention them clearly.**
4. **Draw neat sketches wherever necessary.**

Q.1 Answer the following.

(a) What do you mean by precise exception? Explain. **02**

(b) In data parallelism method, speedup is not directly proportional to the no. of processors. State True/False and justify. **02**

(c) The average number of instructions a thread executes before it suspends is 15, the delay when a thread suspends and switches to another one is 3 cycles and the average number of cycles it waits before it gets the resource it needs is 35.What is the number of threads the processor should support to hide the latency? What is the processor efficiency? (Assume 5 stage pipelining of SMAC2P) **02**

(d) Differentiate fine grained and coarse grained jobs. **02**

(e) Register scoreboarding and renaming technique will resolve anti and output dependency. How? **02**

(f) Differentiate data parallelism with dynamic assignment and data parallelism with quasi-dynamic scheduling. **02**

Q.2 Answer any *Two*.

(a) For the given sequence of instruction develop superscalar pipeline execution diagram (Assume two floating point and two integer execution unit). **06**

Instruction	Number of cycle needed	Arithmetic unit needed
R2←R2 * R6	2	Floating point
R3←R2+R1	1	Integer
R1←R6+8	1	Integer
R8←R2 – R9	1	Integer
R5←R4/R8	2	Floating point
R6←R2+4	1	Integer
R2←R1+2	1	Integer
R10←R9*R8	2	Floating point

Reschedule instructions (If possible) to reduce the no of cycles needed to execute given set of instructions. Show the appropriate execution diagram.

(b) The following expressions are to be evaluated: **06**

$a = \sin(x^2y) + \cos(xy^2) + \exp(-xy^2)$

$b = f(u^2) + \sin(g(p)) + \cos^2(h(y^2))$

(i) Obtain a task graph for calculating a, b.

(ii) Assuming 4 processors are available. Obtain a task assignment to processors assuming the following timings for various operations:

squaring= multiplication = negation= 1

sin = cos = exponentiation = 2

g(x) = h(x) = f(x)=3

(c)

1. Explain how branch instructions delay pipeline execution. If a program has 18% conditional branch instructions and 4% unconditional branch instructions and if 7% of conditional branches are taken branches, calculate the loss in speedup of a processor with 4 pipeline stages. **04**
2. Explain the terms Pipeline stall and pipeline locking with the help of space-time diagram. **02**

Q.3 **(a)** An examination paper has 5 questions. The answer to these questions does not take equal time to correct. Answer to question 1 takes 4 min. to correct, question 2 takes 6 minutes, question 3 takes 5 minutes, question 4 takes 5 minutes and question 5 takes 8 minutes. Due to this speed mismatch storage should be provided between teachers. Answer the following questions assuming 2000 papers are to be corrected by 5 teachers. **06**

1. What is the idle time of teachers?
2. What is the system efficiency?
3. What will be the efficiency of system if the data parallel mode is given?

(b) What is Multithreading? Briefly explain types of multithreaded processors. **06**

OR

Q.3 **(a)** In the pipeline mode of processing we assumed that there is no communication delay between stages of the pipeline . If there is a delay of **y** between pipeline stages derive a speed up formula. What condition should **y** satisfy to ensure a speedup of at least **0.8k** where k is the no. of stages in the pipeline ? **04**

(b) Following are the sequence of instructions: **04**

I1 ADD R1,R5,R1
I2 MUL R1,R2,R3
I3 SUB R2,R6,R2
I4 DIV R5,R1,R5
I5 ADD R2,1,R1

Classify the all data dependency present between above instructions and justify.

(c) Explain hardware modification techniques using BPB, BTB in details to reduce delay due to branches. **04**