DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
FIRST SESSIONAL
SUBJECT: (IT 403) Microprocessor Architecture Programming & Interfacing

Examination	**: B.TECH Semester – IV**	**Seat No.**	**:**
Date	**: 10 /01/2018**	**Day**	**: Wednesday**
Time	**: 10:00am To 11:15am**	**Max. Marks**	**: 36**

INSTRUCTIONS:
1. Figures to the right indicate maximum marks for that question.
2. The symbols used carry their usual meanings.
3. Specify your assumptions clearly. 4. No marks without justification for T/F.
5. Be precise, clear and to the point in answering the questions. 6. Calculator is not allowed.

Q.1 Do as directed. [12]

(a) What are the states of the Auxiliary Carry(AC), Zero(Z) and sign(S) flags after executing the following 8085 program? Justify your answer. What is the final answer in Acc. [2]

```
MVI L, 55h
MVI A, ABh
ADD L
```

(b) We can identify opcode fetch cycle looking at only *RD, *WR and IO/*M signals. State true/false and justify. [2]

(c) [2]

```
2100    LXI SP,3000h
2100    CALL 2400    ; Draw the stack frame when call instructions is executed.
```

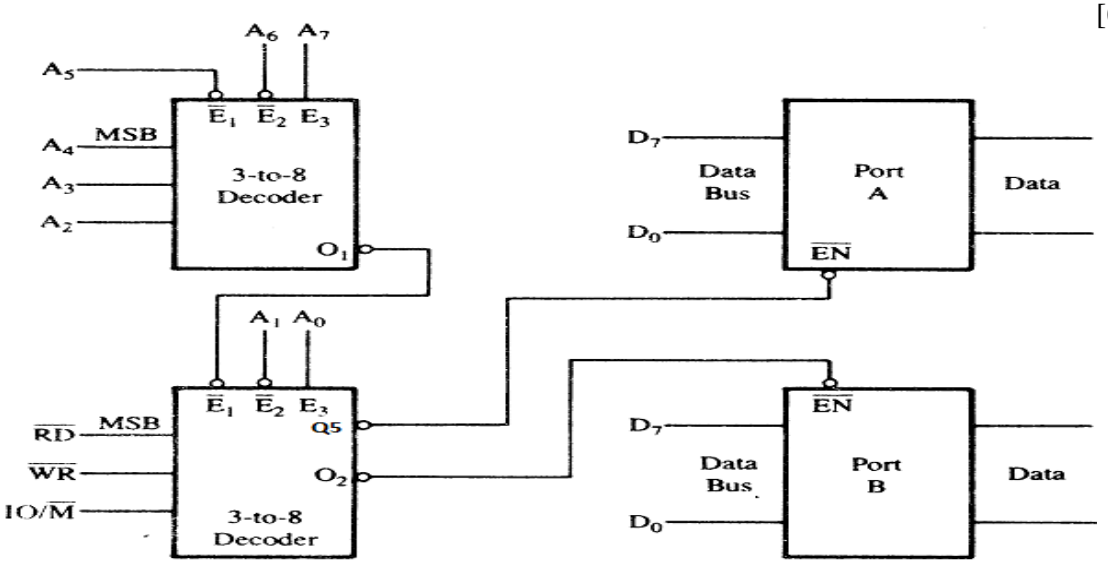
(d) What is the availability of the data on the data bus when read/write operation performed by 8085 ? State the type of devices used to interface simple Input/Output port and why? [2]

(e) In 8085 system, starting address of ROM is C000h and RAM is A000h. Size of the RAM and ROM devices are 4Kbytes. What address is most appropriate to initialize SP? Why? [2]

(f) What is the size of a RET instruction? Name the machine cycles required to complete the instruction. [2]

Q.2 [12]

(a) [6]



Identify ports A and B as input or output port. Justify your answer. Also specify ports are memory mapped or IO mapped IO. Identify the port address of port A and B. Write instructions to read input port and send the information to output port. Which port is partially decoded ?

(b) [6]

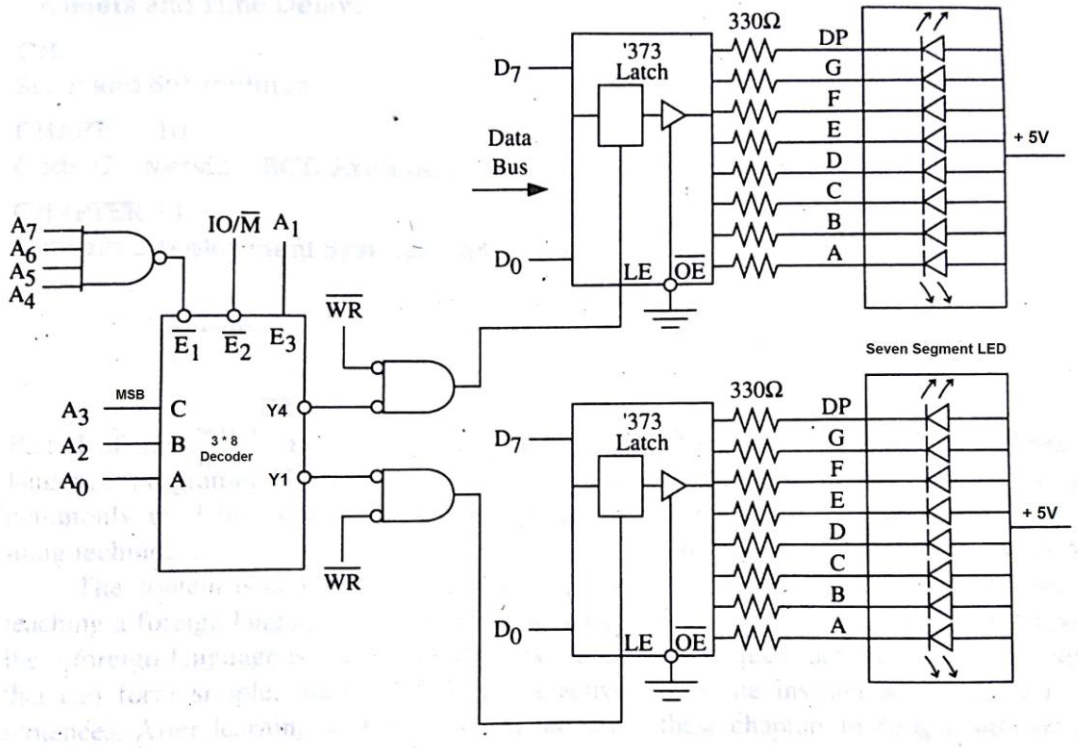
```
2100  LXI H, 1234h
      MVI A, 55h
      INR M
```

What is the size of INR M instruction. Specify the content of address bus, data bus and control signals *RD, *WR, IO/*M and ALE signals for every T states. Name the machine cycles also. Assume 4 T-states are required for op-code fetch cycle.

OR

(b) Write a program to move a memory block from memory locations 2300h - 230Fh to 2308h-2317h. Assume that data memory available is only 2300h to 2317h. Draw neat flow chart and explain your logic clearly. Specify your assumptions, if any, very clearly. [6]

Q.3 (a) [6]



Write Instructions to display the number "88" at the common Cathode Seven-segment LED port. Assume LE signal is active high pulse.

(b) What is the size of ANA M instruction? What is the size of ANA M instruction ? How many machine cycles required to complete this instruction? Name them. [3]

(c) Specify the addressing mode and function for following instructions : [3]

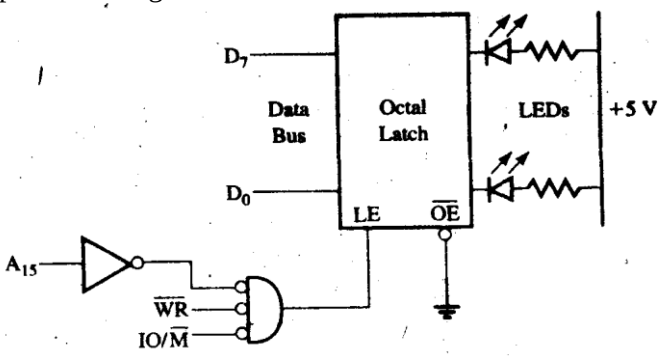
i) MOV B, M ii) CMA iii) SHLD

OR

Q.3 (a) In the subroutine, if you do not balance the stack, what will happen ? Explain. [2]

(b) Draw the neat circuit diagram to separate LSB address A0 to A7 from data bus AD0 to AD7. Explain working of the circuit. [4]

(c) [6]



Identify the port address of the output port in the above figure. Write a program to glow each LED one by one continuously.