DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
BLOCK EXAMINATION

SUBJECT CODE : (IT506) SUBJECT NAME : Advanced Microprocessor Architecture

Examination	: B.TECH - Semester - V	Seat No.	:
Date	: 27/10/2012	Day	:
Time	: 1.15 hr	Max. Marks	: 36

INSTRUCTIONS:
1. Figures to the right indicate maximum marks for that question.
2. The symbols used carry their usual meanings.
3. Assume suitable data, if required & mention them clearly.
4. Draw neat sketches wherever necessary.

Q.1 State true/false and justify your answer (no marks without justification).
(a) If string related instructions are not used in the program, 8086 will never access ES automatically. 02
(b) In protected mode of 80386, code segments are always write protected. 02
(c) Even though 8086 has 1 Mbytes of physical memory, it can access only 64 kbytes memory at a time. 02
(d) Two different logical addresses can point to the same physical address in 8086. 02
(e) An instruction MOV CS:[1234],AX will generate an exception in PM of 80386. 02
(f) What is delay slot ? How it improves the delay due to control hazard ? 02

Q.2 Answer the following Questions 06
(a) The 8086 system requires following memory map :
EPROM - 80000H TO 80FFFH
EPROM device available is of size 2 Kbytes. Use 3625 bipolar PROM as decoder to map above devices using absolute decoding. Write down the truth table and draw the complete circuit diagram. State your assumptions, if any, very clearly.
(b) In the examination paper there are 4 questions and each will take on average 5 minutes to correct. 06
1000 candidates write examination. 4 teachers are employed to correct paper using pipeline mode. Every question is not answered by all candidates. 10% of candidates do not answer question 1, 15% question 2, 5% question 3, 25% question 4.
i) How much time is taken to complete grading?
ii) What is the efficiency of pipeline processing?
iii) If data parallel method is used how much time will be taken to complete the grading?

Q.3 (a) The size of IVT and IDT tables are same. State T/F and justify (show your calculation also) 02
(b) State the addressing mode for the following instructions : 04
(i) Mov ax,[1234] (ii) mov ax,[bx] (iii) mov ax,[bx+si] (iv) mov ax,[bx+1234]
(c) Draw the pipeline execution diagram for the following instructions of hypothetical processor SMAC2P : 06

```
MUL R1, R2, R3
ADD R2, R3, R4
INC R4
SUB R6, R3, R7
```

Find out the delay in pipeline execution due to data dependency of the above instructions. State your assumptions clearly if any.

DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
B.TECH - Semester – V (CE/IT)
SUBJECT: DESIGN AND ANALYSIS OF ALGORITHMS

Examination	: [redacted] Session Back	**Seat No.**	:
Date	: 27/[redacted]/2012	**Day**	: Saturday
Time	: 12.00 to 1.15	**Max. Marks**	: 36

INSTRUCTIONS:
1. Figures to the right indicate maximum marks for that question.
2. The symbols used carry their usual meanings.
3. Assume suitable data, if required & mention them clearly.
4. Draw neat sketches wherever necessary.

Q.1 Do as Directed **[12]**

a. Give an example where choice of data structure affects algorithm

b. For which value of n, n-queen problem has no solution?

c. Define principle of Optimality.

d. Compare BruteForce, BackTracking and Branch and Bound techniques of combinatorial optimization

e. Find the Time Complexity of Code fragment, given below.

```
int x = 0;
for ( int j = 1; j <= n; j++ )
    for ( int k = 1; k < 3*j; k++ )
        x = x + j;
```

f. Explain following graph search methods in brief.
1. BFS 2. DFS 3. D-Search 4. Best First Search

Q.2 Answer the following **[12]**

a. Write Kruskal's algorithm for finding MST and explain it.

b. Solve following 0/1 Knapsack problem using branch and bound method. Where Capacity of knapsack is 20.

Item	Weight	Profit
A	10	10
B	8	40
C	12	30

OR

Q.2 Answer the following **[12]**

a. Write Dijkstra's algorithm to find single source shortest path and explain it.

b. Solve the following instance of 15-puzzle problem using Branch & bound. Explain your solution in depth.

i) An initial arrangement — Goal arrangement

Q.3 Answer the following **[12]**

a. Are the two sets A={1,2,3} and B= {2,1,3} equal ? Write suitable algorithm and find complexity of an algorithm

b. Write a Partition algorithm of Quick Sort.

OR

Q.3 Answer the following **[12]**

a. Find the Longest Common Subsequence of the two sequences: <1,0,0,1,0,1,0,1> and <0,1,0,1,1,0,1,1,0>

b. Write an algorithm for 0/1 knapsack problem using Dynamic programming

DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
B.TECH. SEMESTER V [IT]
SUBJECT: (IT-505) COMPUTER & COMMUNICATION NETWORK

Examination	**: Block Sessional**	**Seat No.**	**: ___**
Date	**: 29/10/2011**	**Day**	**:**
Time	**: 11:00 to 12:15**	**Max. Marks**	**: 36**

INSTRUCTIONS:
1. Figures to the right indicate maximum marks for that question.
2. The symbols used carry their usual meanings.
3. Assume suitable data, if required & mention them clearly.
4. Draw neat sketches wherever necessary.

Q.1 Do as directed. [12]

(a) Differentiate: Subnetting and supernetting. [2]

(b) If client and server are communicating using TCP protocol and the TCP segment contains only ACK then what is the size of packet for this segment at network layer? [2]

(c) Define: (a) Authentication. (b) Confidentiality. [2]

(d) Match the following [2]

(a)127.0.0.5	(p)Broadcast address
(b) 255.255.255.255	(q)Host address
(c) 192.168.36.0	(r)Network Address
(d)192.168.36.18	(s)Loop Back Address

(e) Is there any drawback of using piggybacking? [2]

(f) What is optimality principle? [1]

(g) Unit exchange at Datalink layer is called_____. [1]

Q.2 Attempt the following questions. [12]

(I) What is silly window syndrome problem explain with diagram? [3]

(II) Which problem you face to establish a bridge between 802.x to 802.y? [3]

(III) Differentiate: Virtual Circuit subnet and Datagram subnet. [3]

(IV) Give limitations of SMTP. [3]

Q.3 Attempt the following questions. [12]

(I) Consider a message D, presented by the following polynomial [6]
$x19 + x17 + x16 + x13 + x12 + x11 + x9 + x5 + x2 + 1$
Calculate the CRC code R for that message using a "generator-polynomial"
$x7 + x5 + x4 + x3 + x2 + 1$.
Represent in binary code the message to be sent (D and R)

(II) Explain IEEE 802.4 standard. [4]

(III) What is the subnetwork address for a host with IP address 165.100.5.68/28? [2]

DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
B.TECH. SEMESTER V [IT]
SUBJECT: DISCRETE MATHEMATICS
Block Exam (For Regular students)

Examination	**:Block Exam**	**Seat No.**	**: _____**
Date	**: 30/10/2012**	**Day**	**: Tuesday**
Time	**: 10.30 to 12.15**	**Max. Marks**	**: 36**

INSTRUCTIONS:
1. Figures to the right indicate maximum marks for that question.
2. The symbols used carry their usual meanings.
3. Assume suitable data, if required & mention them clearly.
4. Draw neat sketches wherever necessary.

Q.1 Do as directed.

(a) Let $(A, \leq)$ be distributive Lattice. Show that if $a \wedge x = a \wedge y$ and $a \vee x = a \vee y$ for some a, then $x = y$ **[2]**

(b) If A={a, b, c, d, e, f}, R_1 and R_2 are equivalent relations of A. R_1= {{a, b}, {c, d}, {e, f}}, R_2 = {{a, b, c}, {d}, {e, f}} then $R_1 \cap R_2$ = ... **[2]**

(c) What is the general form of particular solution of the difference equation $a_r - 2a_{r-1} + a_{r-2} = 7$ **[2]**

(d) In how many ways can the letters in the words MISSISSIPPI be arranged, if the two P's must be separated? **[2]**

(e) Find a deterministic finite state machine that recognizes the set of all binary Sequences that end with the digits 011 **[2]**

(f) Write grammar that specifies the language L= $\{a^{2i}b^{2j} / i \geq 1, j \geq 1\}$ **[2]**

Q.2 **[12]**

(a) Prove that every circuit has an even number of edges in common with every cut set.

(b) Prove that lower bound of the time complexity of the problem of finding largest among n numbers is proportional to n-1

(c) Prove that ker(f) is a normal subgroup of (G,*)

Q.3

(a) Let a*H and b*H be two cosets of H. Then prove that either a*H and b*H are disjoint or they are Identical. **[4]**

(b) Design a finite state machine with {0,1} as both its input and output alphabet such that output 1 will be produced beginning with the third 1 in any block of three or more 1s in the input sequence. **[4]**

(c) State and prove Euler's condition for the planar graph. **[4]**

DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
B.TECH. SEMESTER V [IT]
SUBJECT: (IT502) DATABASE MANAGEMENT SYSTEM

Examination	**: Block Exam(Repeater)**	**Seat No.**	**: _____**
Date	**: 30/10/2012**	**Day**	**: Tuesday**
Time	**: 3.00 to 4.15**	**Max. Marks**	**: 36**

INSTRUCTIONS:
1. Figures to the right indicate maximum marks for that question.
2. The symbols used carry their usual meanings.
3. Assume suitable data, if required & mention them clearly.
4. Draw neat sketches wherever necessary.

Q.1 **Do as directed.** **[12]**

(a) Difference between E-R diagram and schema diagram. **[2]**

(b) Define multivalued dependency and 4NF. **[2]**

(c) What are the advantages of having an index structure? **[2]**

(d) Two deadlock prevention techniques that use timestamps are _____ and _____. **[2]**

(e) What do you mean by a recovery system? Why do we need it? **[2]**

(f) "Each site requires a transaction manager." Justify this statement as true or false. **[2]**

Q.2 **Attempt *any two* from the following.** **[12]**

(a) What is the purpose of assertions and triggers? Explain with appropriate example. **[6]**

(b) Explain the shadow paging as the recovery system with diagrams. **[6]**

(c) Draw an E-R diagram for Online Airlines Reservation. (Min. 4 Entity Sets) **[6]**

Q.3 (a) Explain Graph based protocol with example. **[6]**

(b) Explain the concept of Conflict Serializability. **[6]**

Is below schedule is Conflict Serializable?

T1	T2
Read(A)	
Write(A)	
	Read(B)
	Write(B)
Read(B)	
Write(B)	
	Read(A)
	Write(A)

OR

Q.3 (a) What is Log based Recovery? Explain Differed Database Modification Technique. **[6]**

(b) Explain the constraints on generalization. **[4]**

(c) Give the name of two Deadlock free Concurrency Control Protocol with reason. **[2]**