**DHARMSINH DESAI UNIVERSITY, NADIAD**
**FACULTY OF TECHNOLOGY**
**FIRST SESSIONAL**
**SUBJECT CODE : (IT506) SUBJECT NAME : Advanced Microprocessor Architecture**

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| **Examination** | **: B.TECH - Semester - V** | **Seat No.** | **:** |
| **Date** | **: 02/09/2013** | **Day** | **: Monday** |
| **Time** | **: 9:30 to 10:45** | **Max. Marks** | **: 36** |

**INSTRUCTIONS:**

1. **Figures to the right indicate maximum marks for that question.**
2. **The symbols used carry their usual meanings.**
3. **Assume suitable data, if required & mention them clearly.**
4. **Draw neat sketches wherever necessary.**
5. **Calculator is not allowed.**

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|---|---|---|---|
| **Q.1** | **State true/false and justify your answer (no marks without justification).** | | |
| | **(a)** | **When task switching is done through FAR JMP instruction, 386 will set NT flag bit in Protected mode of 80386.** | **02** |
| | **(b)** | **If selector in SS pointing to descriptor in GDT whose LSB 5-bits of Access Right (AR) byte is 10101b, then PUSH AX instruction will generate the exception.** | **02** |
| | **(c)** | **A descriptor has defined a code segment as 'executable' only. Instruction MOV EAX,CS:[EBX] will generate an exception. (assume offset contained in EBX is within this code segment)** | **02** |
| | **(d)** | **An instruction MOV CS:[00001234],EAX will generate an exception in PM of 80386.** | **02** |
| | **(e)** | **'C' uses processor registers to pass parameters to the function.** | **02** |
| | **(f)** | **The restriction on starting address of memory segment in real address mode (ie must start with nibble zero) is removed in PVAM of 80386.** | **02** |
| **Q.2** | **Answer any two** | | |
| | **(a)** | **Describe the following descriptor in detail. If this descriptor is accessed by the program during execution, what kind of action will be performed by 80386 in PM?**<br>FFFFh \| 6<br>E009h \| FFh \| 4<br>000Ch \| 2<br>FFFFh \| 0<br>**Which are all the checks 80386 will do and will there be any exception(s) due to these checks ?** | **06** |
| | **(b)** | **(i) The following is valid data segment descriptor and already cached in invisible portion of the DS :**<br>00h \| CFh \| 6<br>91h \| 00h \| 4<br>0080h \| 2<br>FFFFh \| 0<br>**Now if following instruction is executed in PM of 80386 :**<br>**MOV [000FFFF0h],12345678h**<br>**Will there be any exception ? Justify your answer. If any exception, suggest the modification in the descriptor to avoid that exception.** | **04** |
| | | **(ii) In a Protected Mode system, system sets IOPL bits as '1','1' allowing all task to access complete I/O address space. In this scenario, describe the mechanism available in 80386 protected mode to restrict certain port addresses for specific task in detail.** | **02** |
| | **(c)** | **LDTR is loaded with LDT selector 000Ch. Will there be any exception ? Justify your answer. If yes, modify the content of LDTR to avoid exception. If GDTR contains 00008000003Fh, will there be any exception ? Justify your answer. If yes, modify the content of GDTR to avoid exception. The 5$^{th}$ byte of LDT descriptor pointed by LDT selector contains 82h. Will there be any exception ? Justify your answer. If yes, modify the content of 5$^{th}$ byte of the LDT descriptor to avoid exception.** | **06** |
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| **Q.3** | **(a)** | **Explain how 48-bit far pointer (virtual address in program) of 80386 in PM is translated into physical address space in detail and how 80386 manages the 32 Tbytes local virtual memory and 32 T bytes global virtual memory address space in detail.** | **06** |
| | **(b)** | **List the Protected mode registers and their function that are not the part of the real mode.** | **02** |
| | **(c)** | **If an interrupt comes on IR4 pin of 8259 and upper five bits of ICW2 contains $00000_b$ and IDTR=800000000027h, will there be any exception ? If exception, modify the content of IDTR to avoid exception.** | **02** |
| | **(d)** | **What is "TSR" ? How it differs compare to normal program?** | **02** |
| | | **OR** | |
| **Q.3** | **(a)** | **In multitasking system, OS should be protected from user program and user program should be isolated from each other. Explain in detail the support provided by 80386 in PM to implement the above requirements.** | **06** |
| | **(b)** | **What do the 20 most significant bits of a page directory or page table entry stand for ? How the 32-bit of starting address of page table or page frame is generated ?** | **02** |
| | **(c)** | **If the content of the GDTR is 000000280027h, what are the starting and ending addresses of the GDT table ? How many descriptors can be stored in the table ?** | **02** |
| | **(d)** | **Explain the mechanism available to run 8086 type program in Protected mode of 80386.** | **01** |
| | **(e)** | | **01** |