DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
B.TECH. SEMESTER IV [INFORMATION TECHNOLOGY]
SUBJECT: (IT-402) COMPUTER ORGANIZATION

Examination	**: Third Sessional**	**Seat No.**	**: _____**
Date	**: 27/03/2018**	**Day**	**: Tuesday**
Time	**: 10:00 to 11:15 AM**	**Max. Marks**	**: 36**

INSTRUCTIONS:
1. Figures to the right indicate maximum marks for that question.
2. The symbols used carry their usual meanings.
3. Assume suitable data, if required & mention them clearly.
4. Draw neat sketches wherever necessary.

Q.1 Do as directed.

(a) In which writing scheme does all the data writes go through to main memory and update the system cache? **[1]**
a) write-through b) write-back c) write buffering d) no caching of writing cycle

(b) In a virtual memory system, the address space specified by the address lines of the CPU must be _____than the physical memory size and _____than the secondary storage size. **[1]**

(c) Increasing the RAM of a computer typically improves performance because: **[1]**
a) Virtual Memory increases b) Larger RAMs are faster
c) Fewer page faults occur d) Fewer segmentation faults occur

(d) Consider the following steps: **[1]**
(S) In case of a miss, the block consisting of the requested word will be fetched from the main memory and then, the requested word will be forwarded to the processor.
(T) If word is in cache, there is a cache hit; otherwise, there is a cache miss.
(U) A check is made to determine if the word is in cache.
(V) In case of a hit, the requested word will be forwarded to the processor.
Arrange statements in correct sequence of steps when the processor attempts to read a memory word.

(e) If the memories chip size is 256×1 bits than how many chips are required to make up to 1 kB of memory? **[2]**

(f) If an 8-way set-associative cache is made up of 32-bit words, 4 words per line and 4096 sets, how big is the cache in bytes? **[2]**

(g) For Hypercube interconnection structure find number of edges, max internode distance, where n=16. **[2]**

(h) What is cache coherence? Explain with example. **[2]**

Q.2 Attempt ***Any Two*** from the following questions. **[12]**

(a) **(I)** A cache is having 60% hit ratio for read operation. Cache access time is 30 ns and main memory access time is 100 ns, 50% operations are read operation. What will be the average access time for read operation? **[3]**
(II) Consider a Direct Mapped Cache with 8 cache blocks (numbered 0-7). If the memory block requests are in the following order 3, 5, 2, 8, 0, 63, 9, 16, 20, 17, 25, 18, 30, 24, 2, 63, 5, 82, 17, 24. Which memory blocks will be in the cache at the end of the sequence? (show your calculation) **[3]**

(b) Explain and compare various bus arbitration techniques with diagram. **[6]**

(c) Suppose that a total of 64 MB RAM is available in a system this memory space is partitioned in to 8 fixed size slot of 8 MB each. Assume 8 processes are currently requesting memory usage with size indicated as follows [4 MB,3 MB,5 MB,1 MB,2 MB,9 MB,8 MB,4 MB]. Calculate the size of memory wasted due to External and Internal fragmentation. Assume exactly one slot can be given to each process. **[6]**

Q.3 (a) Consider a machine with a 2-way set associative data cache of size 64 Kbytes and block size 16 bytes. The cache is managed using 32-bit addresses and the page size is 4 Kbytes. A program to be run on this machine begins as follows: **[6]**

```
double ARR[1024][1024];
int i, j;

// Initialize array ARR to 0.0
for(i = 0; i < 1024; i++)
   for(j = 0; j < 1024; j++)
      ARR[i][j] = 0.0;
```

The size of double is 8 Bytes. Array ARR is located in memory starting at the beginning of virtual page 0xFF000 and stored in row major order. The cache is initially empty and no pre-fetching is done. The only data memory references made by the program are those to array ARR. What is total size of the tags in the cache directory?

(b) **(I)**What is IOP? Explain steps for CPU-IOP interaction. **[3]**
(II) Consider a paging hardware with a TLB. Assume that the entire page table and all the pages are in the physical memory. It takes 10 milliseconds to search the TLB and 80 milliseconds to access the physical memory. If the TLB hit ratio is 0.6.What is the effective memory access time (in milliseconds)? **[3]**

OR

Q.3 (a) Consider the virtual page reference string 1, 2, 3, 2, 4, 1, 3, 2, 4, 1. On a demand paged virtual memory system running on a computer system that main memory size of 3 pages frames which are initially empty. Let LRU, FIFO and OPTIMAL denote the number of page faults under the corresponding page replacements policy. What is relationship between all these three policies? **[6]**

(b) **(I)** Consider a system with byte-addressable memory, 32 bit logical addresses,4 kilobyte page size and page table entries of 4 bytes each. What is the size of the page table in the system in megabytes? **[3]**

(II) An application loads 100 libraries at startup. Loading each library requires exactly one disk access. The seek time of the disk to a random location is given as 10ms. Rotational speed of disk is 6000rpm. If all 100 libraries are loaded from random locations on the disk, how long does it take to load all libraries? (The time to transfer data from the disk block once the head has been positioned at the start of the block may be neglected) **[3]**