DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
B.TECH. SEMESTER V [INFORMATION TECHNOLOGY]
SUBJECT: (IT-506) ADVANCED MICROPROCESSOR ARCHITECTURE

Examination	**: First Sessional**	**Seat No.**	**: _____**
Date	**: 01/08/2018**	**Day**	**: Wednesday**
Time	**: 11:45 to 1:00**	**Max. Marks**	**: 36**

INSTRUCTIONS:
1. Figures to the right indicate maximum marks for that question.
2. The symbols used carry their usual meanings.
3. Assume suitable data, if required & mention them clearly.
4. Draw neat sketches wherever necessary.

Q.1 Do as directed.

(a) Give the values in the following table during the execution of following instructions for each bus cycle in 8086 with justification. **[2]**

Instruction	Logic on A0 pin	Logic on $\overline{BHE}$ pin	No. of bus Cycles required	Data path used D0-D7 or D8-D15 or D0-D15	justification
MOV AX,[00FB]					
MOV AL,[00FE]					

(b) Interrupt subroutine cannot be single stepped. State Tue/False and justify. **[2]**

(c) Assume SS=1000H, SP=FFEEH, AX=5678H. If PUSH AX instruction is executed, which physical memory locations AL and AH will be stored? **[2]**

(d) FAR CALL instruction will decrement the stack pointer by 2. State True/False and justify. **[2]**

(e) JMP [BX]; if this is a intersegment jump instruction, re-write the instruction with proper assembler directive. **[2]**

(f) If you want that after restart 8086 execute first instruction Mov AX,1234H then which segment base and offset address you use to write the instruction? Also write down the physical address for the same. **[2]**

Q.2 Attempt ***Any Two*** from the following questions. **[12]**

(a) Write down addressing mode and opcode(in hex) for the following instructions(Refer **Table-1** and take D=1 for all): **[6]**
(1) Mov CS:[BX],DL **(2)**Mov [SI+5689h],CH**(3)** MOV [3456H],DI

(b) **(I)**PUSHF **[4]**

```
MOV BP,SP
OR WORD PTR [BP+0],0100H
POPF
MOV AX,7FFEH
MOV BX,02H
ADD AX,BX
INTO
```

Describe the response of 8086 for all instructions after PUSHF instruction.

(II)MOV AX,7FFFH **[2]**

```
MOV BX,0001H
ADD AX,BX
INTO
```

During the execution of INTO instruction, NMI arrives. Explain the response of 8086.

(c) **(I)**What is the use of PTR and OFFSET directives? Explain by giving example. **[4]**
(II) What is reentrant procedure? Which methods of parameter passing are to be used for re-entrant procedure? **[2]**

Q.3 (a) **(I)**If DS=1000H, SS=2000H, SI=0000, DI=0000, BP=0000, BX=003DH, SP=0040H, CS=3000H **[4]**

```
MOV AX,11FFh
MOV WORD PTR[BX],AX
MOV WORD PTR[DI],AX
MOV AX,12FFh
PUSH AX
MOV AX,[BX]
MOV CX,[BX]
MOV BP,SP
MOV DX,[BP+0000]
```

Specify the content of AX, CX DX and SP registers after the execution of above program.

(II) Why you must use an IRET instruction rather than the regular RET instruction at the end of an ISR? **[2]**

(b) Write an assembly program which takes string and a character to be scan in string as input from keyboard, store both in a logical segment named DATA. The input messages "Enter a String "and "Enter a character to scan" should be printed on screen. If input character is found in entered string then display a message on screen "Character is found" else display "Character is not found". Also write down output and steps for compiling and running the program. **[6]**

OR

Q.3 (a) Write a multi module assembly program to divide 32bit number by 16bit number and return a 32bit quotient. Also write down output and steps for compiling and running the program. **[6]**

(b) **(I)**Which of the following instructions are invalid? Re write the invalid instructions with proper justification. **(i)** AND [BP],0001H **(ii)** MOV ES,5489H **[2]**

(II) Address 00090H in IVT contains 35A1H and address 00092H contains 457BH. To what interrupt type do these locations correspond? What is starting physical address for the interrupt service procedure? **[2]**

(III) How TSR is different from normal program? Give difference between active and passive TSR. **[2]**

operands	Memory operands			Register operands	
	No Displacement	Displacement 8 bits	Displacement 16 bits		
MOD	00	01	10	11	
R/M				w=0	w=1
0 0 0	[BX]+[SI]	[BX]+[SI]+DISP8	[BX]+[SI]+DISP16	*AL*	*AX*
0 0 1	[BX]+[DI]	[BX]+[DI] +DISP8	[BX]+[DI] +DISP16	*CL*	*CX*
0 1 0	[BP]+[SI]	[BP]+[SI]+DISP8	[BP]+[SI]+DISP16	*DL*	*DX*
0 1 1	[BP]+[DI]	[BP]+[DI]+DISP8	[BP]+[DI]+DISP16	*BL*	*BX*
1 0 0	[SI]	[SI]+DISP8	[SI]+DISP16	*AH*	*SP*
1 0 1	[DI]	[DI]+DISP8	[DI]+DISP16	*CH*	*BP*
1 1 0	DATA 16(DA)	[BP]+DISP8	[BP]+DISP16	*DH*	*SI*
1 1 1	[BX]	[BX]+DISP8	[BX]+DISP16	*BH*	*DI*

Table-1