FACULTY OF TECHNOLOGY
FIRST SESSIONAL
SUBJECT: (IT-402) Computer Organization

xamination	**: B.TECH - Semester - IV**	**Seat No.**	**:**
ate	**: 03/01/2012**	**Day**	**: Tuesday**
ime	**: 10 to 11**	**Max. Marks**	**: 36**

NSTRUCTIONS:

. Figures to the right indicate maximum marks for that question.
. The symbols used carry their usual meanings.
. Assume suitable data, if required & mention them clearly.
. Draw neat sketches wherever necessary.

Q.1 Do as directed. **[12]**

a Is there any difference between parallel processing and multiprocessing? Justify your answer **[2]**

b Why the communication between processor level components are asynchronous? **[2]**

c In IEEE-754 32-bit format type of number are infinites if fraction is_____and the type of numbers are NaNs if fraction is_____. **[1]**

d Consider indirect index addressing mode of format **opcode R a** the content of index register is **R** and the address part of the instruction is **a** the operand will be at _____. **[1]**

e What is the purpose of co-processor? **[1]**

f If a computer with 32-bit word size uses 2's complement representation for numbers that is range of integers that may be represented_____. **[1]**

g Give application of condition code. **[1]**

h What feature would you suggest adding to the IAS machine to support call and return operations? **[1]**

i **Match the following** **[2]**

(1)A[1]=B[j] (A)Indirect addressing
(2)while(*a++) (B)Indexed
(3)int temp=*x (C)Auto increment
(D)direct addressing
(E)Immediate addressing

Q.2 Attempt **Any TWO** of the following questions. **[12]**

a **(I)**Consider the following floating point format **[4]**

15	14 … 9	8 … 0
S	E	M

The floating point number is represent as,$=(-1)^{s}[1+M*2^{-9}]2^{E-31}$,if E≠0
=0 ,otherwise

Determine the difference between two successive smallest positive numbers representable in the above system.

(II) Differentiate: Macro and subroutine. **[2]**

b **(I)**Suppose that the hex contents of two CPU register in the 32-bit processor are as follows **[3]**
R0=01237654 R1=7654EDCB.The following store word instructions are executed to transfer the contents of these registers to main memory M.
STORE R0, ADR
STORE R1, ADR+4
Assuming that M is byte addressable,give the contents of all memory locations affected by the above code(A)if the computer is Big-endian (B)if the computer is Little-endian.

(II) For the 8-bit word 00111001, the check bits stored with it would be 0111.Suppose when the word is read from memory, the check bits are calculated to be 1101.What is the data word that was read from memory? **[3]**

c **(I)** How Register-Level design can solve the following function explain with diagram: **[3]**
Z=A+B; A=A+Z;A=-B; A=A-A.

(II) Implement 3 bit binary to excess-3 code converter using PLA. **[3]**

).3 Answer the following questions: **[12]**

a **(I)** Explian Architecture of IAS machine with diagram. **[4]**

(II) Suppose we have an instruction LDA 800.What would be loaded into the AC(accumulator)if the addressing mode for the operand is direct and indirect respectively? **[2]**

800	900