DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
B.TECH. SEMESTER V [IT]
SUBJECT : (IT506) ADVANCED MICROPROCESSOR ARCHITECTURE

Examination	**: Second Sessional**	**Seat No.**	**: _____**
Date	**: 31/08/2015**	**Day**	**: Monday**
Time	**: 12 to 1.15 pm**	**Max. Marks**	**: 36**

INSTRUCTIONS:
1. **Figures to the right indicate maximum marks for that question.**
2. **The symbols used carry their usual meanings.**
3. **Assume suitable data, if required & mention them clearly.**
4. **Draw neat sketches wherever necessary.**
5. **Zero marks, if justification is not given for T/F questions.**

Q.1 Do as directed.

(a) PM of 80386 supports segment size from 1 byte to 4 GB. Explain how? [2]

(b) An instruction MOV CS:[12345678],EAX will generate an exception in PM of 80386. State true/false and justify. [2]

(c) Parameters are pushed on the stack in the same order from the order they are written in the function call parentheses in 'C'. State true/false and justify. [2]

(d) Differentiate the terms Fault exception and Trap exception in PM of 80386. [2]

(e) IDT is not a memory segment, while LDT is a memory segment. Explain why? [2]

(f) State the major advantage/disadvantage of normalized pointer in Huge memory model. [1]

(g) Which mode supports to run 8086 type real address mode program once switched to Protected Virtual Address Mode in 80386. [1]

Q.2 Answer any two [12]

(a) What will be the minimum size of the IDT to avoid an exception when type 12_h interrupt arrives in 80386 in PM? Show your calculation. The following is the Interrupt Gate Descriptor whose content is as follows : [6]

		Byte
00	0F	6
FE	00	4
00	90	2
00	00	0

Is this a valid Interrupt Gate Descriptor ? Justify your answer and suggest necessary correction(s), if any.
Now if GDTR=000080000090_h and selector of this gate descriptor when loaded in CS register, will there be any exception ? If no, why? If yes, do the correction in the content of GDTR so that there would not be any exception.

(b) Logical address 1005_h:12345678_h is to be converted to 32-bit linear address by segmentation unit of 80386. Calculate the 16-bit offset generated by this selector. Also state to which descriptor table it will point. The content of the descriptor is as follows : [6]

		Byte
00	CF	6
F9	00	4
A2	90	2
FF	FF	0

Find out the 32-bit linear address generated by segmentation unit. Selector of the above logical address must be loaded into which segment register? If an instruction MOV EAX, CS:[12345678_h] is executed, will there be any exception? Justify your answer.

(c) The following is valid data segment descriptor and already cached into invisible portion of the **DS :** [6]

		Byte
00	CF	6
91	00	4
00	80	2

FF	FE	0

Now if following instruction is executed in PM of 80386 :
MOV [FFFFF0FFh],12345678h will there be any exception(s) ? Justify your answer. If any exception(s), suggest the modification in the descriptor to avoid that exception.

Q.3 (a) Explain the mechanism supported by 80386 to isolate and protect the tasks from each other in PM mode. [2]

(b) 80386 does not read every time 8 byte descriptor from the table to generate physical address once the selector is loaded in to segment register. State true/false and justify. [2]

(c) If IDTR= 1000000000FFh then state the range of interrupt types supported by the system. Show the calculation. If you want to accommodate all the interrupt types, modify the content of the IDTR. [2]

(d) Explain are the major advantages of CALL, interrupt and TRAP GATE descriptors. [2]

(e) What is the lifetime and scope of "Automatic" variable in 'C'? Explain which memory segment allocated for them in the system and how this will help to achieve above characteristics. [2]

(f) How translation look aside buffer (TLB) makes address conversion faster in PM of 80386? [2]

OR

Q.3 (a) If paging is enabled, how 32-bit linear address generated by segmentation unit is converted to 32-bit physical address by 80386. [2]

(b) Explain the advantages/disadvantages of segmented-paged model of 80386. [2]

(c) Assume that the base address of LDT is 00120000h and GDT base address is 00100000h. Value loaded into the CS register is 1007h. Is the segment descriptor in the GDT or LDT? What is the starting address of the segment descriptor? [2]

(d) TASK cannot be recursive in PM mode of Intel 80x86 family architecture. Explain how this can be ensured in PM of 80386. [2]

(e) Offset part of the far pointer of call/jmp instruction which points to CALL GATE Descriptor is ignored. State true/false & justify in detail. [2]

(f) What is true about the 386 TSS descriptor? [1]

a. It is a system segment descriptor.
b. If B=0, the TSS is available.
c. Minimum value of LIMIT is 00067h
d. All of the above.

(g) Which of the following is not true in 80386? [1]

a. The TSS descriptor is stored only in the LDT.
b. All the tasks must share the same page directory.
c. The minimum size of TSS is 104 bytes.
d. TSS is a not a memory segment.