DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
SECOND SESSIONAL
SUBJECT CODE : (IT506) SUBJECT NAME : Advanced Microprocessor Architecture

Examination	**: B.TECH - Semester - V**	**Seat No.**	**:**
Date	**: 08/09/2016**	**Day**	**: Thursday**
Time	**: 12:45 to 14:00**	**Max. Marks**	**: 36**

INSTRUCTIONS:
1. **Figures to the right indicate maximum marks for that question.**
2. **The symbols used carry their usual meanings.**
3. **Assume suitable data, if required & mention them clearly.**
4. **Draw neat sketches wherever necessary. 5. Calculator is not allowed.**

Q.1 State true/false and justify your answer (no marks without justification).

(a) When task switching is done through FAR JMP instruction, 386 will clear the Busy flag bit in current task's TSS descriptor. **02**

(b) If selector in SS pointing to descriptor in GDT whose LSB 5-bits of Access Right (AR) byte is 10111b, then 80386 will generate exception. **02**

(c) A descriptor has defined a segment whose LSB 5-bits of Access Right (AR) byte is 11001b. If Selector of this descriptor is loaded into DS register, exception will be generated. **02**

(d) An instruction MOV CS:[00001234],EAX will generate an exception in PM of 80386. **02**

(e) 'C' passes the arguments to function by pushing the arguments on the stack, in the order they are written in the function call parentheses. **02**

(f) IDT must be located at 0^{th} address of of 4 Gbytes of physical memory address space in PVAM of 80386. **02**

Q.2 Answer any two

(a) Describe the following descriptor in detail. If this descriptor is accessed by the program during execution, what kind of action will be performed by 80386 in PM? **06**

FFFFh		6
EBh	FFh	4
000Ch		2
FFFFh		0

Which are all the checks 80386 will do and will there be any exception(s) due to these checks ?

(b) (i) The following is valid data segment descriptor and already cached in invisible portion of the DS : **06**

		Byte
00h	4Fh	6
91h	00h	4
0080h		2
FFFFh		0

Now if following instruction is executed in PM of 80386 :
MOV 00100000h],12345678h
Will there be any exception(s) ? Justify your answer. If any exception(s), suggest the modification(s) in the descriptor to avoid that exception(s).

(c) If an interrupt type 16_d comes and IDTR=00001000008Fh, show that it will point to a valid interrupt gate descriptor in IDT. The following is the interrupt Gate descriptor whose content is as follows : **06**

		Byte
8000h		6
EEh	08h	4
0080h		2
0000h		0

Prove that it is a valid 80386 interrupt gate descriptor. Now if GDTR=00008000007Fh, selector of interrupt gate descriptor will generate any exception ? If yes, do the correction in the selector of the above descriptor such that there would not be any exception. If no, why?

Q.3 (a) Explain how 48-bit far pointer (virtual address in program) of 80386 in PM is translated by segmentation unit into 32-bit linear address space in detail. Also explain, how this 32-bit linear address is converted to 32-bit physical address by paging unit in detail. **06**

(b) Whenever exception occurs in the 80386, it always resumes from the next instruction after executing the exception handler. State True/False Justify **02**

(c) Explain the mechanism supported by 80386 in PVAM for protecting specific ports from unauthorized access by specific tasks. **01**

(d) What could be the size of IDT ? Show your calculation. **01**

(e) What is "TSR" ? How it differs compare to normal program execution? **01**

(f) Specify the main advantage and disadvantage of huge memory model in 'C'. **01**

OR

Q.3 (a) In multitasking system, OS should be protected from user program and user program should be isolated and protected from each other. Explain in detail the various support provided by 80386 in PM to implement the above requirements. **06**

(b) What is the lifetime and scope of "Automatic" variable in 'C'? Explain which memory segment allocated for them in the system and how this will help to achieve above characteristics. **02**

(c) Explain the extra two major hardware features provided in 80486 on chip. **02**

(d) How 80386 will know during task switching whether it is a normal task or virtual 8086 mode task during ? **01**

(e) Which memory model effectively nullify the segmentation in 80386 PM ? **01**