DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
B.TECH. SEMESTER IV [Information Technology]
SUBJECT: (IT-402) Computer Organization

Examination	**: Third Sessional**	**Seat No.**	**:**
Date	**: 20/03/2012**	**Day**	**:Tuesday**
Time	**: 10 to 11**	**Max. Marks**	**: 36**

INSTRUCTIONS:

1. Figures to the right indicate maximum marks for that question.
2. The symbols used carry their usual meanings.
3. Assume suitable data, if required & mention them clearly.
4. Draw neat sketches wherever necessary.

Q.1 Do as directed. **[12]**

a Give examples of non homogeneous interconnection network. **[1]**

b Why does the computer wait until the termination of the currently executing instruction, before checking and responding to an interrupt? What would happen if it tried earlier? **[2]**

c What is the average memory access time from the following options for a 3 level memory system where $T_2=2T_1$ and $T_3=3T_1$ and hit ratio's $H_1=H_2=0.9$[T_1 is effective access time].calculation necessary. **[2]**
(A)$1.11T_1$ (B)$1.22T_1$ (C)$1.09T_1$ (D)$1.01T_1$

d What is a page table used for? **[2]**

e Define: Packet switching. **[1]**

f Differtiate: Spatial and Temporal locality. **[2]**

g In an N*N omega switching network if N=64.How many stages and switches per stage are needed? **[2]**

Q.2 Attempt **Any TWO** of the following questions. **[12]**

a **(I)**Consider a memory hierarchy system consisting of two levels. The access time of level1 is 2ns.The miss penalty (The time to get data from level2, in case of miss) is 100ns.What is the average memory access time if the probability that valid data found in level1 is 0.97? **[4]**
(II) What is a drawback of segmentation compared to paging? **[2]**

b **(I)**A RAM is to be design with capacity 256 * 32 M bit and given IC's are 64MB.Design and draw the interface and also show required control signals. **[4]**
(II) Differentiate: Daisy chaining, polling & independent requesting. **[2]**

c **(I)**Explain how a logical memory address is transformed into a physical memory address in a paged memory system. **[4]**
(II) What are vectored interrupts? **[2]**

Q.3 (a) Given references to the following pages by a program 0 9 0 1 8 1 8 7 8 7 1 2 8 2 7 8 2 3 8 3.calculate the number of page fault if there are four page frames available to it using FIFO,LRU and OPTIMAL page replacement algorithm. **[6]**

Q.3 (b) On a non-pipelined sequential processor, a program segment, which is a part of the interrupt service routine, is given to transfer 500 bytes from an I/O device to memory. **[6]**

Initialize the address register
Initialize the count to 500
LOOP: Load a byte from device
Store in memory at address given by address register
Increment the address register
Decrement the count
If count != 0 go to LOOP

Assume that each statement in this program is equivalent to a machine instruction which takes one clock cycle to execute if it is a non-load/store instruction. The load-store instructions take two clock cycles to execute. The designer of the system also has an alternate approach of using the DMA controller to implement the same transfer. The DMA controller requires 20 clock cycles for initialization and other overheads. Each DMA transfer cycle takes two clock cycles to transfer one byte of data from the device to the memory. What is the approximate speedup when the DMA controller based design is used in place of the interrupt driven program based input-output?

-OR-

Q.3 (a) What are the two system organization for cache?What is cache coherance problem?Explain various techniques to solve cache coherence problem. **[6]**

Q.3 (b) **(I)**An application loads 100 libraries at startup. Loading each library requires exactly one disk access. The seek time of the disk to a random location is given as 10ms. Rotational speed of disk is 6000rpm. If all 100 libraries are loaded from random locations on the disk, how long does it take to load all libraries? (The time to transfer data from the disk block once the head has been positioned at the start of the block may be neglected) **[4]**
(II) Explain I/O instruction types. **[2]**