DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
B.TECH. - SEMESTER – V [INFORMATION TECHNOLOGY]
SUBJECT: (IT506) ADVANCED MICROPROCESSOR ARCHITECTURE

Examination	**: Third Sessional**	**Seat No.**	**:**
Date	**: 14/10/2016**	**Day**	**: Friday**
Time	**: 12:45 TO 2:00**	**Max. Marks**	**: 36**

INSTRUCTIONS:
1. **Figures to the right indicate maximum marks for that question.**
2. **The symbols used carry their usual meanings.**
3. **Assume suitable data, if required & mention them clearly.**
4. **Draw neat sketches wherever necessary.**

Q.1 Answer the following.

(a) One or more branch instructions addresses may point to the same entry in BPB. State True/False. Justify **02**

(b) In a data parallelism method efficiency is increased as the number of tasks is increasing. State True/False. Justify **02**

(c) Suppose the functions F and G can be computed in 5 and 3 nanoseconds by functional units U_F and U_G, respectively. Given two instances of U_F and two instances of U_G, it is required to implement the computation F (G(Xi)) for $1 \leq i \leq 10$. Ignoring all other delays, What is the minimum time required to complete this computation in nanoseconds? **02**

(d) Which of the following are NOT true in a pipe lined processor? **02**
1. Bypassing can handle all RAW hazards.
2. Register renaming can eliminate all register carried WAR hazards.
3. Control hazard penalties can be eliminated by dynamic branch prediction.

(A) 1 and 2 only (B) 1 and 3 only (C) 2 and 3 only (D) 1,2 and 3

(e) Register scoreboarding and renaming technique will resolve all types of dependency between instructions of a program. True/False. Justify **02**

(f) if a BTB is to be used in a 16-bit processor whose addressing capacity is 16Mbytes.What could be the word size(bit length) of BTB(assume only 1-bit predictor is used)? **02**

Q.2 Answer any *Two*.

(a) **(1)** Consider 6 execution stages of lengths 45 ns, 50 ns, 60 ns, 30 ns, 20 ns, and 40 ns. Find the time to execute 1000 instructions on both pipelined and non pipeline machine assuming overhead of 5ns in pipeline machine. Also calculate the speedup. **03**

(2) Consider the following code sequence having five instructions I1to I5. Each of these instruction has the following format. OP Ri, Rj, Rk. Where operation OP is performed on contents of registers Rj and Rk and the results are stored in register Ri. **03**

I1 : ADD R1, R2, R3
I 2: MUL R7, R1, R3
I 3:SUB R4, R1, R5
I 4: ADD R 3, R 2, R 4
I 5: MUL R7,R8, R9

Consider the following three statements.
S1: There is an anti-dependence between instructions I2 and I5
S2: There is an anti-dependence between instructions I2 and I4
S3: Within an instruction pipeline an anti-dependence always creates on or more stalls
Which one of above statements is/are correct? Justify your Answer.

(b) Consider a pipelined processor with the following four stages: **06**
IF: Instruction Fetch, ID: Instruction Decode and Operand Fetch, EX: Execute,
WB: Write Back. The IF, ID and WB stages take one clock cycle each to complete the operation. The number of clock cycles for the EX stage depends on the instruction. The ADD and SUB instructions need 1 clock cycle and the MUL instruction needs 3 clock cycles in the EX stage. Operand forwarding is used in the pipelined processor. What is the number of clock cycles taken to complete the following sequence of instructions?

ADD R2, R1, R0 R2 <- R0 + R1
MUL R4, R3, R2 R4 <- R3 * R2
SUB R6, R5, R4 R6 <- R5 - R4

(c) Consider an instruction pipeline with five stages without any branch prediction: Fetch Instruction (FI), Decode Instruction (DI), Fetch Operand (FO), Execute Instruction (EI) and Write Operand (WO). The stage delays for FI, DI, FO, EI and WO are 5 ns, 7 ns, 10 ns, 8 ns and 6 ns, respectively. There are intermediate storage buffers after each stage and the delay of each buffer is 1 ns. A program consisting of 15 instructions I1, I2, I3, …, I15 is executed in this pipelined processor. Instruction I5 is the only branch instruction and its branch target is I11. If the branch is taken during the execution of this program, What is the time (in ns) needed to complete the program? **06**

Q.3 (a) **(1)**Give the differences between Blocked, Interleaved and simultaneous Multi threading**.** **03**

(2) What is delay slot? How it is used to reduce the delay due to branches? **03**

(b) In the examination paper there are 5 questions and each will take on average 5 minutes to correct. 2000 candidates write examination. 5 teachers are employed to correct the papers using pipeline mode. Every question is not answered by all candidates. 20% of candidates do not answer question 1, 5% question 2, 15% question 3, 10% question 4, 12% question 5. **06**

1. How much time is taken to complete grading?
2. What is the efficiency of pipeline processing?
3. If data parallel method is used how much time will be taken to complete grading?

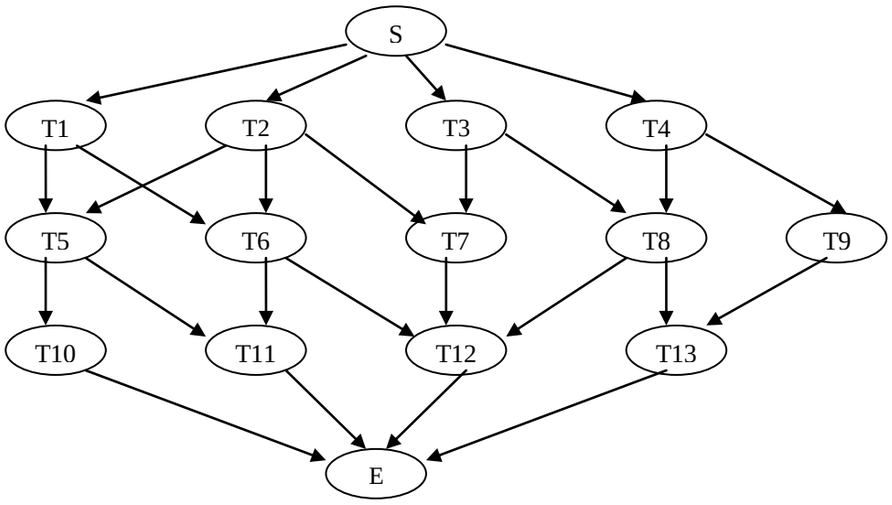
OR

Q.3 **(a)** For the given sequence of instruction develop superscalar pipeline execution diagram (Assume two floating point and two integer execution unit). **06**

Instruction	Number of cycle needed	Arithmetic unit needed
R2←R2 * R6	2	Floating point
R3←R2+R1	1	Integer
R1←R6+8	1	Integer
R8←R2 – R9	1	Integer
R5←R4/R8	2	Floating point
R6←R2+4	1	Integer
R2←R1+2	1	Integer
R10←R9*R8	2	Floating point

Reschedule instructions (If possible) to reduce the no of cycles needed to execute given set of instructions. Show the appropriate execution diagram.

(b) A Task graph with various tasks timing is given in Figure below. Assuming that 4 processors are available assign tasks to processors. **06**



T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13
3	4	5	4	6	7	6	5	6	8	9	10	9