DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
B.TECH. SEMESTER V [IT]
SUBJECT: (IT506) ADVANCED MICROPROCESSOR ARCHITECTURE

Examination	**: First Sessional**	**Seat No.**	**: _____**
Date	**: 02/08/2017**	**Day**	**: Wednesday**
Time	**: 11.30 to 12.45**	**Max. Marks**	**: 36**

INSTRUCTIONS:
1. ***Figures to the right indicate maximum marks for that question.***
2. ***The symbols used carry their usual meanings.***
3. ***Assume suitable data, if required & mention them clearly.***
4. ***Draw neat sketches wherever necessary.***
5. ***Calculator is not allowed.***

Q.1 State true/false and justify your answer. (No marks without justification) **12**

(a) If DI register is used to provide offset address, it will always refer ES to calculate 20-bit physical address. **02**

(b) The 8086 always needs two machine cycles to read or write the word. **02**

(c) Single stepping and maskable interrupt will be automatically disabled by 8086 as a part of an interrupt response. **02**

Do as directed.

(d) Which assembler directive is used to get offset address of a variable named DATA1 defined in a logical segment DATA? Explain by giving example. **02**

(e) If the 8086 DS contains 7000h,write the instruction that will copy the content of DL to physical address 4B2Ch. **02**

(f) Assume SS=1000H, SP=FFEEH, BX=6789H. If PUSH BX instruction is executed, which physical memory locations BL and BH will be stored? **02**

Q.2 (a) The 8086 system requires following memory map : **06**

EPROM - First 64 Kbytes of 1 Mbytes address space
RAM - Last 64 Kbytes of 1 Mbytes address space

EPROM and RAM devices available are of size 32 Kbytes. Use *3625* bipolar PROM as decoder to map above devices using absolute decoding. Write down the truth table and draw the complete circuit diagram. State your assumptions, if any, very clearly.

(b) **(I)**MOV AX,7FFFH **04**
MOV BX,0001H
ADD AX,BX
INTO

During the execution of INTO instruction, NMI arrives. Explain the response of 8086 in detail.

(II) Write a piece of code to set TRAP flag. **02**

OR

(b) Write a program to compare two strings STR1 And STR2 stored in same segment using string related instruction. If they are equal display "Strings are equal" and break the program, otherwise display "Strings are not equal" and break the program. Draw the neat flow chart. State your assumptions, if any, clearly. **06**

Q.3 (a) Explain the type of jump in detail for the following instructions: **04**

(a) JMP BX
(b) JMP DWORD PTR[SI[
(c) JMP 1234:5678
(d) JMP NEXT
:
NEXT:

(b) Address 00040h and 00041h in the interrupt vector table contains 4A24h and 0040h. **04**

(i) To what interrupt type do these locations correspond?
(ii) What is the starting address for interrupt service procedure?

(c) What is reentrant procedure? Which methods of parameter passing are to be used for re-entrant procedure? **02**

(d) Give differences between RET and IRET instructions. **02**

OR

Q.3 (a) Determine the addressing modes for following 8086 instructions. **04**

(i)ADD BX, 59H[DI] **(ii)**MOV AX, MULTIPLIER
(iii)MOV BX, OFFSET DATA1 **(iv)**SUB BYTE PTR [2048],DH

(b) Which of the following instructions are invalid? Modify the invalid instructions with proper justification for correction. **04**

(i)AND [BP],0001 **(ii)**MOV [SI], [BX]**(iii)**ADD CX,AL **(iv)**MOV DS,1234H

(c) Assume SS=1000H, DS=2000H and BP=1234H. If MOV AX, [BP+1234H] instruction is executed, content of which two physical memory locations will be transferred to AH and AL? **02**

(d) Why interrupt subroutine cannot be single stepped? How it can be done? **02**