DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
B.TECH - Semester - IV
SUBJECT: (IT-402) Computer Organization

Examination	**: First Sessional**	**Seat No.**	**:**
Date	**: 08/01/2012**	**Day**	**: Tuesday**
Time	**: 10 to 11**	**Max. Marks**	**: 36**

INSTRUCTIONS:

1. Figures to the right indicate maximum marks for that question.
2. The symbols used carry their usual meanings.
3. Assume suitable data, if required & mention them clearly.
4. Draw neat sketches wherever necessary.

Q.1 **Do as directed.** **[12]**

a Co-processor serves as an extension to microprocessor. Justify. **[2]**

b Define: loosely coupled and tightly coupled systems. **[2]**

c To obtain an operand value how many time memory access would take place in case of following addressing modes: i)Register, ii)Direct, iii)Immediate, iv)Indirect. **[2]**

d What is purpose of status register? **[1]**

e Consider indirect index addressing mode of format opcode R a content of index register is R and the address part of the instruction is a the operand will be at _____. **[1]**

f If a computer with 32-bit word size uses 2's complement representation for numbers that is range of integers that may be represented_____. **[1]**

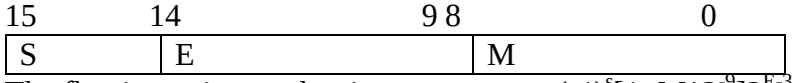
g "Branch instructions reduce the efficiency of instruction pipelining." Justify **[1]**

h What is the impact of the tagged storage architecture on overall program size? **[1]**

i Multitasking is logical extension of multiprogramming. Justify. **[1]**

Q.2 Attempt **Any TWO** of the following questions. **[12]**

a **(I)**Consider the following floating point format **[4]**



The floating point number is represent as,$=(-1)^{s}[1+M*2^{-9}]2^{E-31}$,if $E\neq 0$

$=0$,otherwise

Determine the difference between two successive smallest positive numbers representable in the above system.

(II) Differentiate: Macro and subroutine. **[2]**

b **(I)** The memory unit of a computer has 256K words of 32 bits each. The computer has an instruction format with four fields: an opcode field, a mode field to specify one of seven addressing modes, a register field to specify one of 60 processor registers, and a memory address field specify the instruction format and the number of bits in each field if the instruction is one memory word. **[3]**

II) For the 8-bit word 00111001, the check bits stored with it would be 0111.Suppose when the word is read from memory, the check bits are calculated to be 1101.What is the data word that was read from memory? **[3]**

c **(I)** Explain three speedup techniques. **[3]**

(II) Suppose that the hex contents of two CPU register in the 32-bit processor are as follows **[3]**
R0=01237654 R1=7654EDCB.The following store word instructions are executed to transfer the contents of these registers to main memory M.

STORE R0, ADR
STORE R1, ADR+4

Assuming that M is byte addressable,give the contents of all memory locations affected by the above code(A)if the computer is Big-endian (B)if the computer is Little-endian.

Q.3 **Answer the following questions:** **[12]**

a **(I)** Explian Architecture of IAS machine with diagram. **[3]**

(II) Implement 3 bit binary to excess-3 code converter using PLA. **[3]**

b **(I)**Determine the difference between two successive smallest negative numbers representable in the IEEE-754 32 bit format. **[3]**

(II)"communication between processor level components is asynchronous." Justify **[3]**

-OR-

Q.3 **Answer the following questions:** **[12]**

a **(I)** Differentiate: RISC and CISC machine. **[3]**

(II)A two-word instruction is stored in memory at an address designated by the symbol W.The address field of the instruction (stored at W+1) is designated by the symbol Y.The operand used during the execution of the instruction is stored at an address symbolized by Z.An index register contains the value X. State how Z is calculated from the other addresses if the addressing mode of the instruction is **[3]**

i) Relative, ii) Direct, iii) Index, iv) Indirect

b Consider the following set of Instructions I1,I2,I3,I4,I5,I6 and their respective probabilities are 0.12,0.03,0.07,0.34,0.20,0.24. Find the average opcode length using fixed and variable size. Comment which is better. **[6]**