DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
B.TECH - Semester - III
SUBJECT: (IT 301) Design of Digital Circuits

Examination	**: Second Sessional**	**Seat No.**	**:**
Date	**: 05/09/2014**	**Day**	**: Friday**
Time	**: 9:30 to 10:45**	**Max. Marks**	**: 36**

INSTRUCTIONS:
1. Figures to the right indicate maximum marks for that question.
2. The symbols used carry their usual meanings.
3. Assume suitable data, if required & mention them clearly.
4. Draw neat sketches wherever necessary.

Q.1 Do as directed. **[12]**

(a) How many don't care inputs are there in a BCD adder? Show your calculations. **[2]**

(b) PLA consists of 8 inputs, 8 product terms and 8 sum terms. It will have total ___ number of programmable links. Show your calculations. **[2]**

(c) How do look ahead carry adder speed up the addition process? **[2]**

(d) Determine ROM size to implement 6 Boolean functions of 6 variables each. **[2]**

(e) What is Priority Encoder. Explain giving example. **[2]**

(f) Define: Propagation Delay and Power Dissipation **[2]**

Q.2 Attempt following questions. **[12]**

(a) Determine the equations: greater than, less than and equal to for 4-bit magnitude comparator. **[3]**

(b) Implement the following function using only NAND gates.
F = A(B+CD) + BC' **[3]**

(c) Obtain sum of minterms (in canonical form) of output functions for a combinational circuit that converts a decimal digit from the 8,4,-2,-1 code to BCD code and implement it with decoder and NAND gates **[6]**

OR

(c) Obtain sum of minterms (in canonical form) of output function for a 4 bit odd parity checker and implement it with a multiplexer. Variables given are A,B,C,C' and D **[6]**

Q.3 Attempt following questions **[12]**

(a) Show the derivation table and block diagram of a BCD Adder. **[4]**

(b) List the PLA program table for BCD to Excess-3 coder convertor circuit. **[8]**

OR

Q.3 Attempt following questions **[12]**

(a) Design a combinational circuit using ROM. The circuit accepts 4-bit binary number and generates 4-bit reflected code at the output **[4]**

(b) List the PLA program table for BCD to 9's complement code convertor circuit. **[8]**