DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
B.TECH. SEMESTER V [INFORMATION TECHNOLOGY]
SUBJECT: (IT-506) ADVANCE MICROPROCESSOR ARCHITECTURE

Examination	**: Block Exam (Repeater)**	**Seat No.**	**: _____**
Date	**: 20/10/2018**	**Day**	**: Saturday**
Time	**: 11:00 to 12:15**	**Max. Marks**	**: 36**

INSTRUCTIONS:

1. Figures to the right indicate maximum marks for that question.
2. The symbols used carry their usual meanings.
3. Assume suitable data, if required & mention them clearly.
4. Draw neat sketches wherever necessary.

Q.1 Do as directed.

(a) If DS=10000, SS=20000, BP=0001 and SI=FFFF, IF MOV AX,[BP+SI] is executed, from which physical memory locations, content will be transferred to AX register ? **[2]**

(b) The size of IVT and IDT tables are same. State True/False and justify (show your calculation also) **[2]**

(c) If string related instructions are not used in the program, 8086 will never access ES automatically. State true/false and justify your answer **[2]**

(d) What is the lifetime and scope of "Automatic" variable in „C"? Explain which memory segment allocated for them in the system and how this will help to achieve above characteristics. **[2]**

(e) State the addressing mode for the following instructions :(i) Mov ax,[1234] (ii) Mov ax,[bx] **[2]**

(f) If the variable TEMP is defined as TEMP DW 1234h.Write the Instruction to move a MSB byte of variable TEMP into AL register such that assembler should not give any error. **[2]**

Q.2 Attempt Any Two from the following questions. **[12]**

(a) **(I)**Why interrupt subroutine cannot be interrupted by maskable interrupt INTR? **[2]**

(II) An instruction MOV CS:[00001234],EAX will generate an exception in PM of 80386. State True/False and justify **[2]**

(II) What is "TSR"? How it differs compare to normal program execution? **[2]**

(b) Write an assembly language program (for the assembler) to add ten 8 bit numbers which are stored at Memory location defined as NUMBER. Draw neat flow chart and state your assumptions if any. **[6]**

(c) Explain how 48-bit far pointer (virtual address in program) of 80386 in PM is translated into physical address space in detail and how 80386 manages the 32 Tbytes local virtual memory and 32 T bytes global virtual memory address space in detail. **[6]**

Q.3 (a) Distinguish between anti- dependency and output dependency with appropriate example. **[6]**

(b) The following is valid data segment descriptor : **[6]**

		byte
00h	C0h	6
91h	80h	4
0080h		2
FFFFh		0

Now if following instructions are executed :
MOV EBX,10000000H
MOV [EBX],11111111H

Explain, before executing MOV[EBX],11111111h instruction, what are all the checks processor will do and mention if any exception(s) can be generated due to above checks. If any exception(s), modify the content of the above descriptor, such that above instruction can execute properly.

OR

Q.3 (a) Draw the pipeline execution diagram for the following instructions of hypothetical processor SMAC2P : **[6]**

```
DIV  R1, R5, R1
ADD R2, R1, R3
SUB R2, R5, R1
```

Draw the space-time diagram for above instructions by stalling the instruction for various hazards. Specify very clearly the cause of the stall. State the types of data dependency present in the above instructions set. Assuming register forwarding available, redraw the space-time diagram again.

(b) In multitasking system, OS should be protected from user program and one user program should be protected from other user programs. Explain the support provided by 80x86 family processor in Protected mode to implement the above requirements. **[6]**