

DHARMSINH DESAI UNIVERSITY, NADIAD FACULTY OF TECHNOLOGY

FIRST SESSIONAL

SUBJECT NAME: Advanced Microprocessor Architecture (IT506)

Examination: B.TECH - Semester - V Seat No.:

Time : 11:30 to 12:45 Max. Marks : 36

INSTRUCTIONS:

1. Figures to the right indicate maximum marks for that question.

- 2. The symbols used carry their usual meanings.
- 3. Assume suitable data, if required & mention them clearly.
- 4. No marks without justification in T/F questions.
- 5. Draw neat sketches wherever necessary. 6. Calculator is not allowed.

0.1	-	
0.1	Do as	directed.

(a)	MOVE AX,[1234H]	02
	For above instruction, offset will be added to which segment register? Modify the instruction if	
	offeet is to be added to CS register	

- b) After reset, CS and IP will have values _____ and ____ respectively in 8086. 02
- (c) How many segments are active at a time in 8086? State the names.
- (d) Two different logical addresses can point to the same physical address in 8086. State, in which 02 condition this is possible.
- (e) Why interrupt subroutine cannot be interrupted by maskable interrupt INTR?
- (f) Indirect FAR jump instruction will always use one of the memory addressing mode to get new address. State true/false and justify

Q.2 Answer any two

(a) The 8086 system requires following memory map:

06

03

02

EPROM - First 16 Kbytes of 1 Mbytes address space RAM - Last 16 Kbytes of 1 Mbytes address space

EPROM and RAM devices available are of size 8 Kbytes. Use <u>3625</u> bipolar PROM as decoder to map above devices using absolute decoding. Write down the truth table and draw the complete circuit diagram. State your assumptions, if any, very clearly.

(b) The 8086 system requires following memory map:

RAM - Last 32 Kbytes of 1 Mbytes address space

RAM device available is of size 8 Kbytes. Use 3625 bipolar PROM as decoder to map above devices using absolute decoding. Connect A0 and *BHE as input to the decoder. Write down the truth table and draw the complete circuit diagram. State your assumptions, if any, very clearly.

(c) Write an assembly program for assembler to find number of times letter 'R' exist in the string 'MICROPROCESSOR'. Store the count at memory Location COUNT in Data segment. Draw neat flow chart and state your assumptions very clearly.

Q.3 (a) IRET instruction modifies 01 (i)CS only (iii)IP only (iii)CS and IP (iv)CS, IP and flag register

(b) The BP register is typically used for accessing
(i)extra segment (ii)code segment (iii)stack segment (iv) data segment

(c) Which of the following is an illegal 8086 instruction and why?

(i)MOV ax,[bx] (b)INC [bx] (c)ADD bx,[bx] (d)ADD [si],[bx]

(d) Calculate the displacement for jump.

MOV CX,5 ; size 3 bytes

NEXT: ADD AX,BX ; size 2 bytes

NOP ; size 1 byte

NOP ; size 1 byte

NOP ; size 1 byte

JMP NEXT ; size 2 bytes

e) MOV AX,201H 06

MOV BL,02H

DIV BL

If INTR interrupt is already enabled and arrives at the beginning of the DIV instruction. Describe the response of 8086 after the execution of DIV BL instruction for the following conditions:

Type 0 isr takes 70 microsec and INTR pulse width is 140 microsec. INTR isr takes 40 Microsec.

OR

Q.3 (a) Variable TEMP is defined as TEMP DB 34H, 12H. Write an instruction to move a word from variable TEMP into AX register such that assembler should not give any error.

Address 00080H in IVT contains 4A24H and address 00082H contains 0040H. To what interrupt type do these locations correspond? What is starting physical address for the interrupt service procedure?

(b) State two main advantages of memory segmentation in 8086 system.

(c) If DS=1000H, SS=1000H, SI=0000, DI=0000, BP=0000, BX=003DH, SP=0040H, CS=3000H MOV AX.1234H

MOV WORD PTR[003DH],AX

MOV WORD PTR[0000],AX

MOV AX,5678H

PUSH AX

MOV AX,[003DH]

MOV CX,[BX]

MOV BP,SP

MOV DX,[BP+0000]

Specify the memory addressing modes for MOV AX,[003DH), MOV CX,[BX] and MOV DX,[BP+0000] instructions. Also specify the content of AX, CX and DX registers after the execution of above program.