DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
THIRD SESSIONAL
SUBJECT: (IT 403) Microprocessor Architecture Programming & Interfacing

Examination	: B.TECH Semester – IV	Seat No.	:
Date	: 28 /03/2018	Day	: Wednesday
Time	: 10:00am To 11:15 am	Max. Marks	: 36

INSTRUCTIONS:
1. Figures to the right indicate maximum marks for that question.
2. The symbols used carry their usual meanings.
3. Assume any necessary data but giving proper justifications.
4. Be precise, clear and to the point in answering the questions. Unnecessary elaborations will not fetch more marks.

Q.1 **Do as directed.** [12]

(a) Why only 10 registers are available at a time even though 4 banks of 8 registers are available in 8051 ? [1]

(b) 8051 will generate *PSEN signal to access _____ memory. [1]

(c) Instructions MOV R0,R1((if RS0=0 and RS1=0) and MOV 00,01 will perform the same operation. Say advantage and disadvantage of both the instruction with reason. [2]

(d) Explain term "Re-locatable code". Explain how relative addressing can help to write re-locatable code. [2]

(e) State the two major differences between microprocessor and microcontroller in terms of [2]
1. its Architecture
2. components required to build the computer systems

(f) Write 4 different instructions which will perform the same job of moving a content of memory location 00 to 01(using register addressing and direct addressing). Assume Bank 0 is selected. [2]

(g) What is the main difference between Harvard architecture and Van Neumann architecture in terms of memory organization ? [2]

Q.2 Attempt *Any TWO* of the following questions. [12]

(a) Write a program to transmit 10 bytes using asynchronous mode of 8251. Program 8251 for 8 data bits, no parity, 1 stop bits and baud factor X16. Assume suitable port addresses. State your assumptions very clearly, if any and draw neat flow chart. [6]

(b) Write a subroutine to transfer 1 byte data on SOD pin of 8085 asynchronously assuming data is passed in B register of 8085.State your assumptions very clearly, if any and draw neat flow chart. Assume bit delay routine is available and does not destroy any registers. [6]

(c) How many interrupts are there in 8051? Name them. Explain the characteristics in terms of maskability, vectoring and priority. Name the SFRs used for these purpose. [6]

Q.3 (a) During the execution of Instruction _____ , *PSEN will be generated. [1]

(b) During the execution of Instruction _____ , *RD will be generated. [1]

(c) During the execution of Instruction _____ , *WR will be generated. [1]

(d) Sketch the serial output waveform for the ASCII character "A" when it is transmitted with 1200 baud and even parity asynchronously. [2]

(e) Why we require to add wait state ? Which signal of 8085 is used to add wait state ? Draw the one wait state generator circuit which will add one wait state only for memory address space for 8085. [3]

(f) Explain the internal (data and program) memory organization of 8051. [4]

OR

Q.3 (a) Which control signal is to be connected to DIR pin of 74LS245 while buffering the data bus. [1]

(b) Why system bus is to be buffered ? Explain. [1]

(c) Which instructions are used to access external program memory ? [1]

(d) Which instructions are used to access external data memory ? [1]

(e) Identify addressing modes for following instruction: [2]
1. MOVC A,@DPTR+A
2. SJMP NEXT
3. MOV 00,01
4. MOVX A, @DPTR

(f) Draw the neat circuit diagram to interface 8Kbytes external data memory whose starting address is 2000H which could be used for both running the program as well as storing the data. Do the absolute decoding. [6]