DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
B.TECH - IT - Semester - III
SUBJECT: (IT 301) Design of Digital Circuits

Examination	**: Second Sessional**	**Seat No.**	**:**
Date	**: 09/09/2016**	**Day**	**: Friday**
Time	**: 11:00 to 12:15**	**Max. Marks**	**: 36**

INSTRUCTIONS:
1. Figures to the right indicate maximum marks for that question.
2. The symbols used carry their usual meanings.
3. Assume suitable data, if required & mention them clearly.
4. Draw neat sketches wherever necessary.

Q.1 Do as directed. **[12]**

(a) "When the number of variables in Ex-OR function is odd, the minterms with an even number of 0's are same as minterms with odd number of 1's." State T/F with justification. **[2]**

(b) Show that $A \oplus B \oplus C \oplus D = \Sigma (1, 2, 4, 7, 8, 11, 13, 14)$. **[2]**

(c) PLA consists of 6 inputs, 6 outputs and 5 product terms. Calculate total no. of links. **[1]**

(d) What is the number of inputs and outputs of a decoder that accepts 256 different input combinations? **[1]**

(e) "The circuit for a DEMUX is basically the same as that for a decoder". State T/F with justification. **[1]**

(f) What do you mean by noise margin and propagation delay of gate? **[2]**

(g) How does look-ahead carry concept speed up the addition process in parallel adder? Explain in detail. **[3]**

Q.2 Attempt following questions. **[12]**

(a) Design and implement the BCD adder which adds two BCD digits in parallel and produce a sum digit also in BCD. **[5]**

(b) (i) Signals **A, B, C, C', D** are available. Using a single 8 X 1 MUX and no other gate, implement the Boolean function **F=∑ (0,1,2,6,9,10,12,13,15).** **[4]**

(ii) Implement the function **F= AB'CD' + A'BCD' + AB'C'D + A'BC'D** with 2 Ex-OR and one AND gates. **[3]**

OR

(b) (i) Derive the PLA program table for a combinational circuit that squares 2-bit number. Minimize the number of product terms. **[4]**

(ii) Implement BCD to Excess-3 convertor using 4-bit parallel adder MSI circuit. (draw block diagram for parallel adder) **[3]**

Q.3 Attempt following questions **[12]**

(a) Implement the function **F=(X+Z')(WX+Y')(Y+Z)** with multilevel NAND gates. **[4]**

(b) Design a combination circuit using ROM which accepts 3-bit binary input and generates an output binary number equal to cube of the input number.(Show block diagram for ROM) **[4]**

(c) Design & implement 4 bit even parity generator circuit. **[4]**

OR

Q.3 Attempt following questions **[12]**

(a) Implement the function **F=AB(C+CD)+BC'** with multilevel NOR gates. **[4]**

(b) Determine the high level output voltage of the RTL gate for a fan-out of 6.Also determine the minimum input voltage required to drive an RTL transistor to saturation when hfe = 20. From the results obtained, determine the noise margin of the RTL gate when the input is high and the fan-out is 6. **[4]**

(c) Design a combinational circuit that converts a decimal digit from **5,2,1,1 to 2,4,2,1** code. **[4]**