DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
B.TECH. SEMESTER V [INFORMATION TECHNOLOGY]
SUBJECT: (IT-506) ADVANCED MICROPROCESSOR ARCHITECTURE

Examination	**: Third Sessional**	**Seat No.**	**: _____**
Date	**: 10/10/2018**	**Day**	**: Wednesday**
Time	**: 11:45 to 1:00**	**Max. Marks**	**: 36**

INSTRUCTIONS:
1. Figures to the right indicate maximum marks for that question.
2. The symbols used carry their usual meanings.
3. Assume suitable data, if required & mention them clearly.
4. Draw neat sketches wherever necessary.

Q.1 Do as directed.

(a) The average number of instructions a thread executes before it suspends is 15, the delay when a thread suspends and switches to another one is 3 cycles and the average number of cycles it waits before it gets the resource it needs is 35.What is the number of threads the processor should support to hide the latency? What is the processor efficiency? (Assume 5 stage pipelining of SMAC2P) **[2]**

(b) Superscalar architecture uses both temporal and data parallelism. State True/False and justify. **[2]**

(c) What is the main advantage of pipeline locking over pipeline stall? Explain how this will help to avoid WAW hazard. **[2]**

(d) Can delay slot be used to improve the delay due to all types of branch instructions while rearranging code in a loop? Justify your answer. **[2]**

(e) If a BTB is to be used in a 16-bit processor whose addressing capacity is 16Mbytes.What could be the word size(bit length) of BTB(assume only 2-bit predictor is used)? **[2]**

(f) Give differences between Temporal and Data parallelism. **[2]**

Q.2 Attempt ***Any Two*** from the following questions. **[12]**

(a) If a program has 18% conditional branch instructions and 4% unconditional branch instructions and if 30% of conditional branches are taken branches. The probability of branch instructions found in BTB is 0.85 and 70% cases the branch prediction base on BTB is correct calculate the % loss in speedup for SMAC2P. **[6]**

(b) Instruction execution in processor is divided into 5 stages. Instruction fetch(IF), Instruction Decode(ID), Operand Fetch(OF), Execute(Ex), and Write Back(WB). These stages take 5, 4, 20, 10 and 3 nanoseconds respectively. A pipelined implementation of the processor requires buffering between each pair of consecutive stages with a delay of 2ns. Two pipelined implementations of the processors are contemplated: **[6]**
(1)A naïve pipeline implementation(NP) with 5 stages and
(2) An Efficient pipeline (EP) where the OF stage is divided into stages OF1 and OF2 with execution times of 12ns and 8ns respectively.
What is the speedup achieved by EP over NP in executing 20 independent instructions with no hazards?

(c) The instruction pipeline of a RISC processor has the following stages: Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Perform Operation (PO) and Writeback (WB).The IF, ID, OF and WB stages take 1 clock cycle each for every instruction. Consider a sequence of 100 instructions. In the PO stage, 40 instructions take 3 clock cycles each, 35 instructions take 2 clock cycles each, and the remaining 25 instructions take 1 clock cycle each. Assume that there are no data hazards and no control hazards. How many number of clock cycles required for completion of execution of the sequence of instructions? **[6]**

Q.3 (a) An examination paper has 8 questions to be answered and there are 1000 answer books. Each answer takes 3 minutes to correct. If 4 teachers are employed to correct the papers in a pipelined mode, how much time will be taken to complete the job of correcting 1000 answer papers? What is the efficiency of processing? If 8 teachers are employed instead of 4, what is the efficiency? Repeat with 32 teachers and 4 pipeline. **[6]**

(b) The following expressions are to be evaluated. **[6]**

$a=g(p) + e^{-xf(y)} + h(x^2) + f(y)* g(p)$

$b= f(u^2) + \sin (g(p)) + \cos^2 h(y^2)$

Obtain task graph for calculating a and b.

OR

Q.3 (a) For the given sequence of instruction develop superscalar pipeline execution diagram (Assume 2 floating point and 2 integer execution unit and two instructions fetch at a time). **[6]**

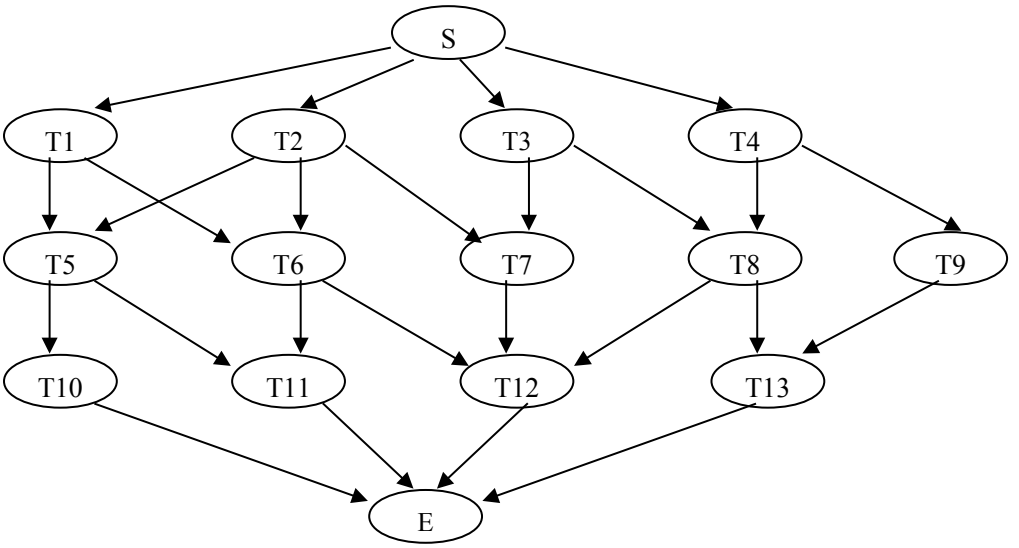
Instruction	Number of cycle needed	Arithmetic unit needed
R2←R2 * R6	2	Floating point
R3←R2+R1	1	Integer
R1←R6+8	1	Integer
R8←R2 – R9	1	Integer
R5←R4/R8	2	Floating point
R6←R2+4	1	Integer
R2←R1+2	1	Integer
R10←R9*R8	2	Floating point

(I) Develop superscalar pipeline execution diagram.

(II) Is it possible to rename registers to reduce the number of execution cycles?

(III) Reschedule instructions (If possible) to reduce the no of cycles needed to execute given set of instructions. Show the appropriate execution diagram.

(b) A Task graph with various tasks timing is given in Figure below. Assuming that 4 processors are available assign tasks to processors and also calculate time. **[6]**



T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13
3	4	5	4	6	7	6	5	6	8	9	10	9