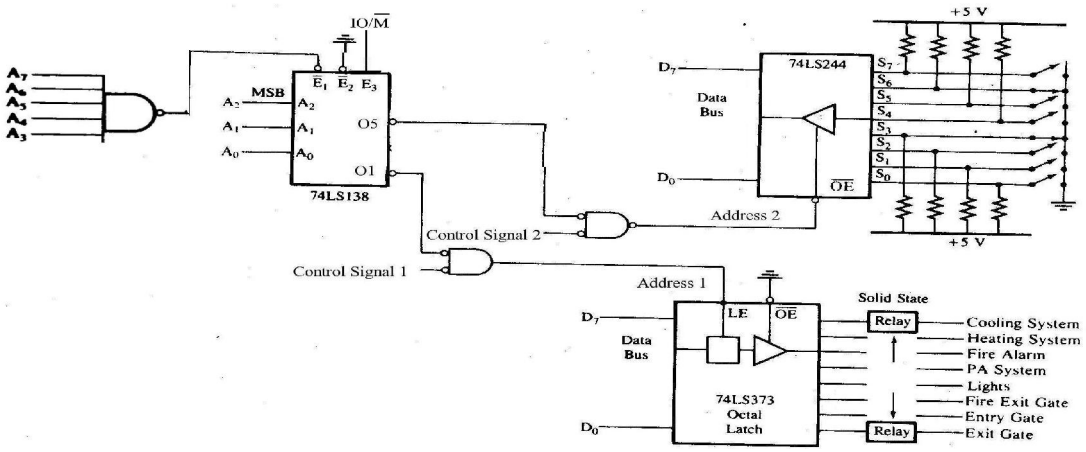
DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
FIRST SESSIONAL

SUBJECT CODE : (IT403) SUBJECT NAME : Microprocessor Architecture Programming & Interfacing

Examination	**: B.TECH - Semester - IV**	**Seat No.**	**:**
Date	**: 20/01/2016**	**Day**	**: Wednesday**
Time	**: 11 to 12:15**	**Max. Marks**	**: 36**

INSTRUCTIONS:

1. **Figures to the right indicate maximum marks for that question.**
2. **The symbols used carry their usual meanings. Calculator is not allowed.**
3. **Assume suitable data, if required & mention them clearly. No marks without justification in case T/F.**
4. **Draw neat sketches wherever necessary.**

Q.1	**Do as directed.**		
	(a)	**Why ALE is generated during the first T state of every machine cycle?**	**[2]**
	(b)	**"Instructions which use direct addressing mode run faster than the instructions which use indirect addressing mode". State T/F with justification.**	**[2]**
	(c)	**"During third machine cycle of STA instruction, transfer of data take place". State T/F with justification.**	**[2]**
	(d)	**2100 CALL 2300 ; Draw the stack frame when CALL instruction is executed.**	**[2]**
	(e)	**State the differences between opcode fetch and memory read cycle.**	**[2]**
	(f)	**After Reset, 8085 will send _____ on A8-A15 and _____ on AD0-AD7.**	**[2]**
Q.2			
	(a)	 **Identify the port addresses and control signals of the input and output port in the above figure. Write instructions to read the input port and output the same on output port.**	**[6]**
	(b)	**8085 system requires following memory map in the system :** **EPROM : 16 Kbytes at processor address space 8000H.** **RAM : last 16 Kbytes of processor address space.** **16 Kbytes EPROM and 16 Kbytes RAM devices are available.** **Use one 74LS138 three to eight line decoder to fully decode the above address map. Draw the neat circuit diagram. Also specify the processor address space mapped to RAM and EPROM.**	**[6]**
		OR	
	(b)	**2100 LXI D, 3E3EH** **MVI A, 3EH** **LDAX D** **How many machine cycle(s) require to complete the LDAX D instruction? Name them. Show the content of AD0-AD7, A0-A7 & A8-A15 for each T-state for *"LDAX D" instruction only* along with the control and status signals. LDAX D requires 4 T-sates for opcode fetch cycle.**	**[6]**
Q.3	**(a)**	**Write an assembly language program to count number of odd numbers from 100 unsigned binary numbers. Explain your logic very clearly. Draw neat flow chart. State your assumptions, if any, clearly.**	**[4]**
	(b)	**State the function of the CALL instruction and explain with example. Also state the number of machine cycles require to complete the instruction and name them.**	**[4]**
	(c)	**State addressing mode for instructions: 1. LXI H 2500H 2. LHLD ABCDH 3. ADD M 4. ADD A**	**[4]**
		OR	
Q.3	**(a)**	**Show schematic of Latching Low-Order Address Bus (Demultiplexing the BUS AD7 to AD0) and generation of control signals (*IOR,*IOW,*MEMR,*MEMW) using *RD, *WR, and IO/*M control signals.**	**[4]**
	(b)	**Calculate the count value needed to generate 1ms delay for microprocessor operating at 1Mhz clock freq.**	**[4]**
	(c)	**Show content of registers and memory locations after execution of each of the following instructions.** **2100 LXI H , 29FFH 29FF: ABH** **INR L 2A00: CDH** **INX H 2A01: EFH** **INR M**	**[4]**