DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
B.TECH Semester – IV
SUBJECT: (IT 403) Microprocessor Architecture Programming & Interfacing

Examination	**: BLOCK Sessional**	**Seat No.**	**:**
Date	**: 06 /04/2018**	**Day**	**: Friday**
Time	**: 11.00am to 12.15pm**	**Max. Marks**	**: 36**

INSTRUCTIONS:
1. Figures to the right indicate maximum marks for that question.
2. The symbols used carry their usual meanings.
3. Assume any necessary data but giving proper justifications.
4. Be precise, clear and to the point in answering the questions. Unnecessary elaborations will not fetch more marks.

Q.1 Do as directed. **[12]**

(a) Can we interface input and output device with same port number? State True/False and Justify your answer. **[2]**

(b) Specify function of ADI instruction. How many machine cycles will be require to execute this instruction ? Name Them. **[2]**

(c) What will be the analog voltages corresponding to MSB, LSB and FS for 4 bit DAC for 0 to 10 volt range. **[2]**

(d) Instructions MOV R0,R1((if RS0=0 and RS1=0) and MOV 00,01 will perform the same operation. Say advantage and disadvantage of both the instruction with reason. **[2]**

(e) After reset, is it necessary to initialize SP if we want to use only register bank-0 in the system? Justify your answer. **[2]**

(e) State 2 advantages of using USART (8251) over SID and SOD pin of 8085 for serial communication. **[2]**

Q.2 Attempt following questions. **[12]**

(a) 8085 system requires following memory map in the system: **[6]**

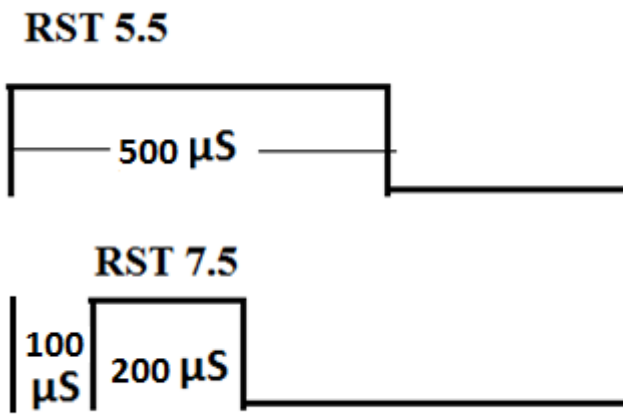
RAM: Last 8 Kbytes of processor address space.
EPROM: First 8 Kbytes of processor address space.

4 Kbytes RAM and EPROM devices are available. Use only one 74138 3 to 8 line Decoder to fully decode the above address map. Draw the neat circuit diagram. Specify processor address space mapped to RAM and EPROM devices.

(b) **[6]**

In 8085 system, as shown in above figure, RST 7.5 arrives after 100 µS of RST 5.5. Assume maskable interrupt system is already enabled, RST 5.5 & RST 7.5 are unmasked and RST 7.5 & RST 5.5 interrupt service routines take 300 µS each. Also assume that EI is written at the end of the RST 5.5 interrupt service routine. Describe the response of 8085 and execution of program for following 2 cases:

Case 1: If EI is written at middle of the RST 7.5 interrupt service routine.
Case 2: If EI is written at the end of the RST 7.5 interrupt service routine.



Q.3 (a) 8 bit DAC is interfaced with 8085 using port number 18H. Write programs to generate following wave forms: **[6]**

1. Triangular Waveform
2. 1 KHz square wave

Draw neat flow chart and state your assumption clearly, if any.

(b) 2100 XTHL **[6]**

What is size of XTHL instruction ? How many machine cycles required to complete the instruction ? Show the content of data bus, address bus for every T-state.