DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
B.TECH. - SEMESTER – IV [INFORMATION TECHNOLOGY]
SUBJECT: (IT-402) COMPUTER ORGANIZATION

Examination	**: Third Sessional**	**Seat No.**	**:**
Date	**: 08/04/2016**	**Day**	**: Friday**
Time	**: 11 to 12:15**	**Max. Marks**	**: 36**

INSTRUCTIONS:
1. Figures to the right indicate maximum marks for that question.
2. The symbols used carry their usual meanings.
3. Assume suitable data, if required & mention them clearly.
4. Draw neat sketches wherever necessary.

Q.1 Do as directed.

(a) Consider a disk pack with 16 surfaces, 128 tracks per surface and 256 sectors per track. 512 bytes of data are stored in a bit serial manner in a sector. The capacity of the disk pack and the number of bits required to specify a particular sector in the disk are respectively: **[2]**
(A) 256 Mbyte, 19 bits (B) 256 Mbyte, 28 bits
(C) 512 Mbyte, 20 bits (D) 64 Gbyte, 28 bits

(b) Consider a machine with a byte addressable main memory of 1MB, block size of 16bytes and a direct mapped cache with size 64KB. Let the addresses of two consecutive bytes in main memory be $(E201F)_{16}$ and $(E2020)_{16}$.What are the tag, cache line address and displacement (in hex) for main memory address $(E201F)_{16}$? **[2]**

(c) Consider a 4-way set associative cache consisting of 128 lines with a line size of 64 words. The CPU generates a 20-bit address of a word in main memory. What are the numbers of bits in the TAG, LINE and WORD fields are respectively? **[2]**

(d) Consider a machine with 64 MB physical memory and a 32-bit virtual address space. If the page size is 4KB, each page table entry size is 2 bytes then what is the approximate size of the page table? **[2]**

(e) Why DRAM cells required periodic refreshing? **[2]**

(f) For complete interconnection structure find number of edges, max node degree, where n=64. **[2]**

Q.2 Attempt ***Any TWO*** of the following questions. **[12]**

(a) **(I)**In a two level memory, the average access time without level 1 is 180 ns and with level 1 the average access time is 60 ns. Calculate the miss ratio if level 1 access time is 45 ns. **[3]**
(II) If page frames are initially empty and a process is allowed 3 page frames in real memory and reference string of pages is 1 2 3 4 1 2 5 1 2 3 4 5 and the page replacement is FIFO then the total number of page fault caused is x. If we increase the number of frames in main memory i.e., Now main memory has 4 frames. So, if total number of page fault for the same reference string is y then what is the relation between x and y? **[3]**

(b) Consider a computer system with ten physical page frames. The system is provided with an access sequence (a1; a2;:::; a20; a1; a2;:::; a20), where each ai is a distinct virtual page number. What is the difference in the number of page faults between the last-in-first-out page replacement policy and the optimal page replacement policy? **[6]**

(c) Given memory portions of 100KB,500KB,200KB,300KB,and 600KB(in order),how would each of the first fit, best fit algorithms place processes of 212KB,417KB,112KB,and 426KB(in order)? Which algorithm makes most efficient use of memory? **[6]**

Q.3 (a) Discuss the steps involve in DMA transfer process with diagram. **[6]**

(b) Design 8K × 16 RAM from 1K × 8 RAM IC. Draw interface using given IC'S .Also show required control lines. **[6]**

OR

Q.3 (a) Explain and compare various bus arbitration techniques with diagram. **[6]**

(b) What is cache coherence? Discuss various solutions of it with neat diagram. **[6]**