DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
FIRST SESSIONAL
SUBJECT CODE : (IT506) SUBJECT NAME : Advanced Microprocessor Architecture

Examination	**: B.TECH - Semester - V**	**Seat No.**	**:**
Date	**: 10/09/2012**	**Day**	**: Wednesday**
Time	**: 10:45 to 12.00**	**Max. Marks**	**: 36**

INSTRUCTIONS:

1. **Figures to the right indicate maximum marks for that question.**
2. **The symbols used carry their usual meanings.**
3. **Assume suitable data, if required & mention them clearly.**
4. **Draw neat sketches wherever necessary.**

Q.1 State true/false and justify your answer (no marks without justification).

(a) **All memory segment must start with nibble zero in Protected mode of 80386.** **02**

(b) **If Selector in SS pointing to descriptor in GDT whose LSB 5-bits of Access Right (AR) byte is 10101b, then PUSH AX instruction will generate the exception.** **02**

(c) **If you load the selector of a code segment which is 'marked' as readable into DS segment register, there will be an exception.** **02**

(d) **An instruction MOV CS:[1234],AX will generate an exception in PM of 80386.** **02**

(e) **User programs are running at the same privilege level, so one user can easily access the memory segments of other user.** **02**

(f) **Parameters which are passed in parentheses to function in 'C', pushed in the left to right order on stack when the function is called.** **02**

Q.2

(a) **Describe the following descriptor in detail. Selector of this descriptor must be loaded into which register of 80386 in PM?** **06**

0040h		6
9Bh	80h	4
0000h		2
0020h		0

Which are all the checks 80386 will do and will there be exception(s) due to this checks ?

(b) **The following program is executed in 8086 system :** **04**

```
MOV AX,03ffH
    MOV BL,02h
    DIV BL
```

In the middle of DIV instruction, NMI occurs. Explain the response of processor after DIV BL instruction in detail.

(c) **In a Protected Mode system, system sets IOPL bits as '1','1' allowing all task to access complete I/O address space. In this scenario, describe the mechanism available in 80386 protected mode to restrict certain port addresses for specific task in detail.** **02**

OR

Q.2 (a) **Explain how 48-bit far pointer (virtual address in program) of 80386 is translated into physical address space and how 80386 manages the virtual memory address space of 4 Gbytes in detail.** **06**

(b) **If an interrupt comes on IR2 pin of 8259 and upper five bits of ICW2 contains 00010_b and IDTR=000000000060h, will there be any exception ? If exception, what is the remedial action ?** **03**

(c) **If the content of the GDTR is 0021000001FFH, what are the starting and ending addresses of the GDT table ? How many descriptors can be stored in the table ?** **03**

Q.3 (a) **What do the 20 most significant bits of a page directory or page table entry stand for ? How the 32-bit of starting address of page table or page frame is generated ?** **03**

(b) **What does the D bit in a page table entry stand for ? Explain in detail.** **03**

(c) **List the Protected mode registers and their function that are not the part of the real mode.** **02**

(d) **What is stored in the IDT ?** **02**

(e) **Offset part of the far pointer of call/jmp instruction to point CALL GATE Descriptor is ignored. State true/false & justify in detail.** **02**

OR

Q.3 (a) **The size of IVT and IDT tables are same. State T/F and justify (show your calculation also)** **02**

(b) **In 'C', when the function is called, whose responsibility to balance the stack ?** **02**

(c) **The addressing capacity decides the maximum size of memory segment in Intel Architecture processor. State T/F & justify.** **02**

(d) **IDT is not a memory segment, while LDT is a memory segment. Explain why?** **02**

(e) **Near pointers are used for all code and data references in huge memory model for turbo C. State T/F & justify.** **02**

(f) **Explain the mechanism available to run 8086 type program in Protected mode of 80386.** **02**