DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
B.TECH. SEMESTER V [IT]
SUBJECT : (IT506) ADVANCED MICROPROCESSOR ARCHITECTURE

Examination	**: Second Sessional**	**Seat No.**	**: _____**
Date	**: 01/09/2014**	**Day**	**: Monday**
Time	**:**	**Max. Marks**	**: 36**

INSTRUCTIONS:
1. **Figures to the right indicate maximum marks for that question.**
2. **The symbols used carry their usual meanings.**
3. **Assume suitable data, if required & mention them clearly.**
4. **Draw neat sketches wherever necessary.**

Q.1 State true/false and justify.

(a) **In protected mode of 80386, restriction on starting address of memory segment with nibble 0 in real address mode is still present.** **[2]**

(b) **An instruction MOV CS:[1234],EAX will generate an exception in PM of 80386.** **[2]**

(c) **Parameters are pushed on the stack in the same order from the order they are written in the function call parentheses in 'C'.** **[2]**

(d) **The size of page directory table in paging mode is 16 Kbytes where as page table is 4Kbytes.** **[2]**

(e) **To enter into virtual 8086 mode the VM bit in EFLAGS is not directly switched to 1 by software.** **[2]**

(f) **There is no difference in gate structure of interrupt and trap gates. But there is a difference when the processor executes the interrupt or trap procedure in 80386 PM.** **[2]**

Q.2 **[12]**

(a) **If an interrupt comes on IR4 pin of 8259 and upper five bits of ICW2 contains 00000b and IDTR=00000000000Fh, will it generate any exception to load interrupt gate descriptor from IDT? If yes then modify the value of IDTR The following is the interrupt Gate descriptor whose content is as follows :** **[6]**

		byte
000Fh		6
E2h	00h	4
0014h		2
0000h		0

State the validity of this interrupt gate descriptor. If it is not valid, modify the content at appropriate location. What will be the starting address of the Interrupt subroutine? Will this interrupt procedure be global or local ? Why ?

(b) **Explain how 48-bit far pointer (virtual logical address in program) of protected mode of 80386 is translated into physical address space if paging is also enabled.. Assuming PDBR=23455XXXh, the Page table address in the PDE5= 45345XXXh, The page Frame address in the PTE32=67345XXXh. Calculate The Physical address of the Linear address 014202CAh.** **[6]**

OR

(b) **In multiuser / multitasking system, OS should be protected from user program and user program should be isolated from each other and they should be protected from each other. Explain in detail the support provided by 80386 in PM to implement the above requirements.** **[6]**

Q.3 **(a)** **What is the lifetime and scope of "Automatic" variable in 'C'? Explain which memory segment allocated for them in the system and how this will help to achieve above characteristics.** **[2]**

(b) **Explain how semaphore helps to protect critical region code in "mutual exclusion" technique with the help of an assembly language code example.** **[2]**

(c) **G bit in descriptor defines the maximum size of the memory segment in protected mode of 80386. State true/false and justify.** **[2]**

	(d)	In protected mode, task can not be recursive. This is the requirement of the Intel. How system software developer can take care of this requirement ?	[2]
	(e)	What is the maximum value that should assign to LIMIT in the IDTR? What is the address range of last descriptor in descriptor table defined by IDTR= 0001100001FFh ?	[2]
	(f)	To switch the task through interrupt, interrupt type must point to _____ in _____.	[2]
		OR	
Q.3	(a)	Specify from the following, which one is memory segment and which one is not a memory segment in the Intel 80x86 architecture with reason : 1. IDT 2. LDT 3. TSS 4. GDT	[2]
	(b)	Assume that the base address of LDT is 00120000h and GDT base address is 00100000h. If value loaded into the CS register is 1007h, what is the RPL? Is the segment descriptor in the GDT or LDT? What is the starting address of the segment descriptor?	[2]
	(c)	Explain how IOs are protected in protected mode of 80386. Also specify the mechanism which allows ports to be associated only with specific tasks.	[2]
	(d)	Offset part of the far pointer of call/jmp instruction to point CALL GATE Descriptor is ignored. State true/false & justify in detail.	[2]
	(e)	Explain the terms hardware interrupt, software interrupt, Trap and Fault in 80386 protected mode.	[4]