DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
B.TECH. SEMESTER V [INFORMATION TECHNOLOGY]
SUBJECT: ADVANCE MICROPROCESSOR ARCHITECTURE (IT506)

Examination	**: Third Sessional**	**Seat No.**	**: _____**
Date	**: 11/10/2017**	**Day**	**: Wednesday**
Time	**: 11:30 to 12:45**	**Max. Marks**	**: 36**

INSTRUCTIONS:
1. Figures to the right indicate maximum marks for that question.
2. The symbols used carry their usual meanings.
3. Assume suitable data, if required & mention them clearly.
4. Draw neat sketches wherever necessary.
5. Calculator is not allowed.

Q.1 Do as directed.

(a) Register scoreboarding and renaming techniques will resolve all types of data dependency between instructions of a program. State True/False. Justify **[2]**

(b) What are the major differences between superscalar processor and VLIW processor? **[2]**

(c) Differentiate data parallelism with dynamic assignment and data parallelism with quasi-dynamic scheduling. **[2]**

(d) What is delay slot? How it improves the delay due to control hazard? **[2]**

(e) The size of BTB memory is niether very small nor very large.Justify **[2]**

(f) The average number of instructions a thread executes before it suspends is 15, the delay when a thread suspends and switches to another one is 3 cycles and the average number of cycles it waits before it gets the resource it needs is 35.What is the number of threads the processor should support to hide the latency? What is the processor efficiency? (Assume 5 stage pipelining of SMAC2P) **[2]**

Q.2 Attempt Any Two from the following questions. **[12]**

(a) A 5-stage pipelined processor has Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Perform Operation (PO) and Write Operand (WO) stages. The IF, ID, OF and WO stages take 1 clock cycle each for any instruction. The PO stage takes 1 clock cycle for ADD and SUB instructions, 3 clock cycles for MUL instruction, and 6 clock cycles for DIV instruction respectively. Operand forwarding is used in the pipeline. What is the number of clock cycles needed to execute the following sequence of instructions? **[6]**

Instruction	**Meaning of instruction**
I0 :MUL R2 ,R0 ,R1	R2 ← R0 *R1
I1 :DIV R5 ,R3 ,R4	R5 ← R3 /R4
I2 : ADD R2 ,R5 ,R2	R2 ← R5 + R2
I3 :SUB R5 ,R2 ,R6	R5 ← R2 - R6

(b) **(1)** Explain how branch instructions delay pipeline execution. If a program has 18% conditional branch instructions and 4% unconditional branch instructions and if 7% of conditional branches are taken branches, calculate the loss in speedup in SMAC2P. **[4]**

(2) Explain the terms Pipeline stall and pipeline locking with the help of space-time diagram. **[2]**

(c) What is Multithreading? Briefly explain types of multithreaded processors. **[6]**

Q.3 (a) **(1)** In the pipeline mode of processing we assumed that there is no communication delay between stages of the pipeline. If there is a delay of y between pipeline stages derive a speed up formula. What condition should **y** satisfy to ensure a speedup of at least **0.8k** where k is the no. of stages in the pipeline? **[3]**

(2) Following are the sequence of instructions:

	Instruction	**Meaning of Instruction**
I1	ADD R1,R5,R1	R1=R5+R1
I2	MUL R1,R2,R3	R1=R2*R3
I3	SUB R2,R6,R2	R2=R6-R2
I4	DIV R5,R1,R5	R5=R1/R5
I5	ADD R2,1,R1	R2=R1+1

[3]

Classify all the data dependency present between above instructions and justify.

(b) An examination paper has 8 questions to be answered and there are 1000 answer books. Each answer takes 3 minutes to correct. If 4 teachers are employed to correct the papers in a pipelined mode, how much time will be taken to complete the job of correcting 1000 answer papers? What is the efficiency of processing? If 8 teachers are employed instead of 4, what is the efficiency? Repeat with 32 teachers and 4 pipeline. **[6]**

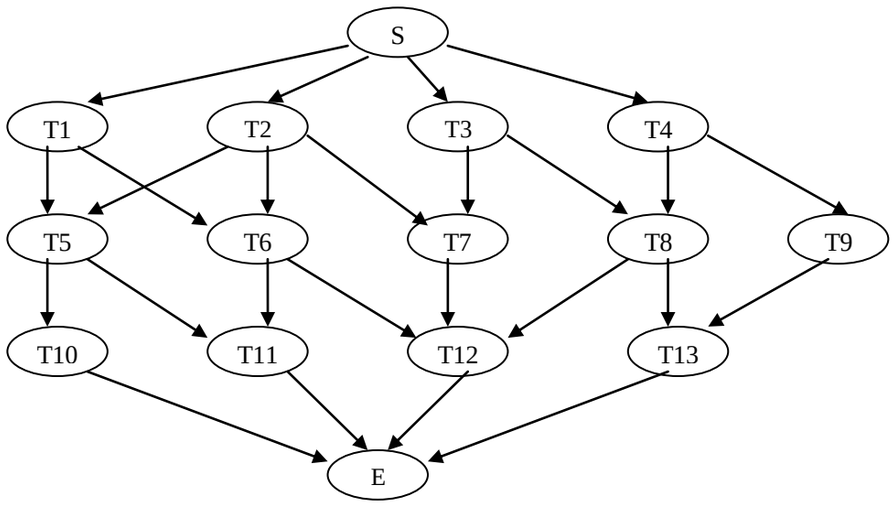
OR

Q.3 **(a)** For the given sequence of instruction develop superscalar pipeline execution diagram (Assume two floating point and two integer execution unit). **[6]**

Instruction	Number of cycle needed	Arithmetic unit needed
R2←R2 * R6	2	Floating point
R3←R2+R1	1	Integer
R1←R6+8	1	Integer
R8←R2 – R9	1	Integer
R5←R4/R8	2	Floating point
R6←R2+4	1	Integer
R2←R1+2	1	Integer
R10←R9*R8	2	Floating point

Reschedule instructions (If possible) to reduce the no of cycles needed to execute given set of instructions. Show the appropriate execution diagram.

(b) A Task graph with various tasks timing is given in Figure below. Assuming that 4 processors are available assign tasks to processors. **[6]**



T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13
3	4	5	4	6	7	6	5	6	8	9	10	9