DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
B.TECH. SEMESTER IV [Information Technology]
SUBJECT: (IT-402) Computer Organization

Examination	**: Second Sessional**	**Seat No.**	**:**
Date	**: 08/02/2012**	**Day**	**: Wednesday**
Time	**: 10 to 11**	**Max. Marks**	**: 36**

INSTRUCTIONS:

1. Figures to the right indicate maximum marks for that question.
2. The symbols used carry their usual meanings.
3. Assume suitable data, if required & mention them clearly.
4. Draw neat sketches wherever necessary.

Q.1 Do as directed. **[12]**

a State True/False with justification: **[3]**
(I) In moore type machine output is shown on each state.
(II) Hardwired is used in Pentium microprocessor.
(III) Classical method minimizes the control unit memory element.

b Identify the overflow from following by adding two 4-bit two's complement number **[2]**
(1)0101+1100(2)0100+0101(3)1110+1011(4)0111+0101

c For a four stage pipeline out of 40 T-state 12 T-state are busy, find out the speedup of pipeline. **[2]**

d Explain two technique of ALU expansion **[2]**

e When computer is said to dynamic programmable? **[1]**

f A pipeline has a speedup factor 8.5 and has efficiency 70%, how many stages do the pipelining has? **[1]**

g Can you multiply floating point number using Booths algorithm? Justify your answer **[1]**

Q.2 Attempt **Any TWO** of the following questions. **[12]**

a **(I)** Differentiate combinational and sequential ALU with reference to their working. **[4]**
(II) How does read and write operation can be implemented in a single clock cycle in any register also give its logic diagram? **[2]**

b **(I)** What is the principle working of carry look ahead adder? Explain it in detail. **[4]**
(II)"Microprogramming techniques is an innovative approach" Discuss its merits and demerits **[2]**

c **(I)**Explain the difference between hardwired control and microprogrammed control and define following terms (I) Micro-operation (II) Micro-instruction (III) Microprogram. **[3]**
(II) Given that pipeline's performance to cost ratio PCR is defined as PCR=f/k where f-pipeline clock frequency, k-is its hardware cost. Derive the equation of optimum no. of stages to maximize PCR. **[3]**

Q.3 Answer the following questions: **[12]**

a Consider the following assembly-language program for a hypothetical RISC **[6]**

```
LD    r4,#A       Load constant A into general register  r4
LD    r5,#B       Load constant B into general register  r5
LD    r6,#C       Load constant c into general register  r6
LD    r9,#0       Clear general register r9
BEQ   r4,r5,adr1  If r4=r5 then go to adr1
ADD   r9,r4,r5    Add the sum of r4 and r5 to r9
MUL   r9,r9,r9    Square the content of r9
MUL   r9,r9,#1    Increment r9 by 1
adr1:st  M(r1),r9 Store r9 in the memory location addressed by r1
```

Identify all possible RAW, WAR and WAW hazards that are present if nothing known about the structure of the RISC`s instruction pipeline.

b Find the product of two numbers X and Y where X=11 and Y= -89 using booths algorithm. Why this method is more preferred than other method? **[6]**

-OR-

Q.3 Answer the following questions: **[12]**

a **(I)**Explain the stages involved in floating point arithmetic. Explain block diagram of floating point unit of IBM system/360 Model. **[3]**
(II) Derive equations of one hot method for Fig-1 **[3]**

b Time t **[6]**

Stage	1	2	3	4	5	6	7
S1	×			×			
S2		×					×
S3			×				
S4					×		
S5						×	

For the pipeline reservation table shown above calculate forbidden set F, minimum average latency (Lmin), minimum constant latency (Lcmin) and also construct task initiation diagram