DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
THIRD SESSIONAL
SUBJECT NAME : (IT506) ADVANCED MICROPROCESSOR ARCHITECTURE

Examination	**: B.TECH - Semester - V**	**Seat No.**	**:**
Date	**: 07/10/2013**	**Day**	**: Monday**
Time	**: 11:15 TO 12:30**	**Max. Marks**	**: 36**

INSTRUCTIONS:
1. **Figures to the right indicate maximum marks for that question.**
2. **The symbols used carry their usual meanings.**
3. **Assume suitable data, if required & mention them clearly.**
4. **Draw neat sketches wherever necessary.**

Q.1 Answer the following.

(a) Superscalar architecture uses both temporal and data parallelism. State true/false and justify. **02**

(b) In pipeline the maximum speedup is 5.The percentage of unconditional branches in program is 10% and conditional branches be 18%. Assume that 85% of the conditional branches are taken in the programs. Find out loss of speedup due to branches.(Assume 5 stage pipelining of SMAC2P) **02**

(c) What is locking of pipeline & when it is required? **02**

(d) "Memory Protection violation "exception can occur during which Stages of SMAC2P processor and why? **02**

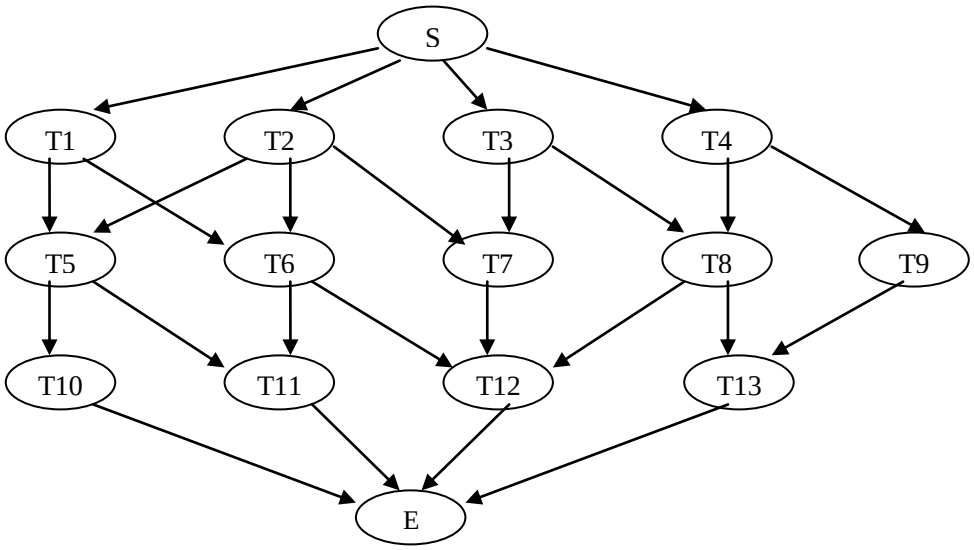
(e) What is the difference between superscalar and superpipelining? **02**

(f) Register scoreboarding and renaming technique will resolve anti dependency and output dependency. How? **02**

Q.2 Answer any *Two*.

(a) What is Multithreading? Name 3 types of Multithreaded Processors. Briefly explain the techniques employed to schedule the threads for each type. **06**

(b) A Task graph with various tasks timing is given in Figure below. Assuming that 4 processors are available assign tasks to processors. **06**



T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13
3	4	5	4	6	7	6	5	6	8	9	10	9

(c)

1. The average number of instructions a thread executes before it suspends is 15, the delay when a thread suspends and switches to another one is 3 cycles and the average number of cycles it waits before it gets the resource it needs is 35.What is the number of threads the processor should support to hide the latency? What is the processor efficiency? (Assume 5 stage pipelining of SMAC2P) **02**
2. Explain hardware modification techniques using BPB, BTB in details to reduce delay due to branches. **04**

Q.3 **(a)** In the examination paper there are 5 questions and each will take on average 5 minutes to correct. 2000 candidates write examination. 5 teachers are employed to correct the papers using pipeline mode. Every question is not answered by all candidates. 20% of candidates do not answer question 1, 5% question 2, 15% question 3, 10% question 4, 12% question 5. **06**

1. How much time is taken to complete grading?
2. What is the efficiency of pipeline processing?
3. If data parallel method is used how much time will be taken to complete grading?

(b) For the given sequence of instruction develop superscalar pipeline execution (Assume one floating point and two integer execution unit and register forwarding is applied). **06**

Instruction	Number of cycle needed	Arithmetic unit needed
R2←R2 * R6	2	Floating point
R3←R2+R1	1	Integer
R1←R6+8	1	Integer
R8←R2 – R9	1	Integer
R5←R4/R8	2	Floating point
R6←R2+4	1	Integer
R2←R1+2	1	Integer
R10←R9*R8	2	Floating point

State the various type of data dependencies between the instructions in the above program .

OR

Q.3 **(a)** An examination paper has 5 questions. The answer to these questions does not take equal time to correct. Answer to question 1 takes 4 min. to correct, question 2 takes 6 minutes, question 3 takes 5 minutes, question 4 takes 5 minutes and question 5 takes 8 minutes. Due to this speed mismatch storage should be provided between teachers. Answer the following questions assuming 2000 papers are to be corrected by 5 teachers. **06**

1. What is the idle time of teachers?
2. What is the system efficiency?
3. What will be the efficiency of system if the data parallel mode is given?

(b)

1. Explain basic difference of instruction scheduling between superscalar and VLIW architecture. **03**
2. Explain various hazards in Pipelining. **03**