



DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
B.TECH. SEMESTER IV [Information Technology]
SUBJECT: (IT-402) Computer Organization

Examination : Block Sessional
Date : 29/03/2012
Time : 10 to 11

Seat No. :
Day :Thursday
Max. Marks : 36

INSTRUCTIONS:

1. Figures to the right indicate maximum marks for that question.
 2. The symbols used carry their usual meanings.
 3. Assume suitable data, if required & mention them clearly.
 4. Draw neat sketches wherever necessary.
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Q.1 Do as directed.

- a** For mesh interconnection structure find number of edges, max node degree, max inter node distance, where $n=32$. [2]
- b** What is age register? [2]
- c** Convert the following 32 bit IEEE-754 format to decimal: 3F800000H. [2]
- d** What are the step involved in addition of two floating point numbers X and Y $X=2.61200111 \times 10^{17}$ and $Y=1.04799245 \times 10^{21}$. [2]
- e** What are the difference between hardwired and microprogramming? [2]
- f** Explain CAD with flow chart for design process. [2]

Q.2 Answer the following questions.

- a** (I) Find the product of two numbers X and Y where $X = -11$ and $Y = -6$ using Booth's algorithm. [4]
(II) Define: (I) Truncation (II) Rounding. [2]
- b** (I) Explain the technique by using that we can reduce the size of control memory. [4]
(II) TLB is sometimes referred to as an address cache. Justify. [2]

Q.3 (I) An instruction is stored at location 300 with its address field at location 301. the address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is [4]

- (a) register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is

(a) Direct; (b) Immediate; (c) relative; (d) register indirect; (e) index with R1 as the index Register.

(II) Define (I) Page (II) Page Frames [2]

Q.3 (I) Explain 2901 bit slice ALU with diagram [4]

- (b) (II) Give the names of register level components. [2]