**DHARMSINH DESAI UNIVERSITY, NADIAD**
**FACULTY OF TECHNOLOGY**
**B.TECH. SEMESTER IV [INFORMATION TECHNOLOGY]**
**SUBJECT: (IT-402) COMPUTER ORGANIZATION**

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|---|---|---|---|
| **Examination** | **: Second Sessional** | **Seat No.** | **: _____** |
| **Date** | **: 14/02/2018** | **Day** | **: Wednesday** |
| **Time** | **: 10:00 to 11:15 AM** | **Max. Marks** | **: 36** |

**INSTRUCTIONS:**
1. Figures to the right indicate maximum marks for that question.
2. The symbols used carry their usual meanings.
3. Assume suitable data, if required & mention them clearly.
4. Draw neat sketches wherever necessary.

**Q.1 Do as directed.**

(a) Given the values of two multiplier M1=0111110 M2=0101010.Which of these multiplier gives best performance in booths multiplication algorithm? Why? **[2]**

(b) A microprocessor provides an instruction capable of moving a string of bytes from one area of memory to another. The fetching and initial decoding of the instruction takes 10 clock cycles. Thereafter, it takes 15 clock cycles to transfer each byte. The microprocessor is clocked at a rate of 10 GHz. Determine the length of the instruction cycle for the case of a string of 64 bytes. **[2]**

(c) For a pipelined CPU with a single ALU, consider the following situations **[2]**
1. The j + 1 thinstruction uses the result of j thinstruction as an operand
2. The execution of a conditional jump instruction
3. The jth and j + 1 thinstructions require the ALU at the same time
Which of the above can cause a hazard?
(A) 1 and 2 only (B) 2 and 3 only(C) 3 only (D) All the three

(d) n instruction set of a processor has 125 signals which can be divided into 5 groups of mutually exclusive signals as follows: Group1: 20 signals, Group2: 70 signals, Group3: 2 signals, Group4 : 10 signals, Group5 : 23 signals. How many bits of the control words can be saved by using vertical microprogramming over horizontal microprogramming? **[2]**

(e) Give differences between hardwired and microprogrammimig. **[2]**

(f) Register File (RF) is also called multiport RAM. Justify the statement. **[2]**

**Q.2** Attempt ***Any Two*** from the following questions. **[12]**

(a) **(I)** A non pipelined single cycle processor operating at 100 MHz is converted into a synchro-nous pipelined processor with five stages requiring 2.5 nsec, 1.5 nsec, 2 nsec, 1.5 nsec and 2.5 nsec, respectively. The delay of the buffer is 0.5 nsec. What is the speedup of the pipeline processor for a large number of instructions? What is the new frequency of the processor using the pipiline design? **[4]**
**(II)** How combinatinal ALU is different from sequential ALU? **[2]**

(b) Consider a 3 GHz (gigahertz) processor with a three-stage pipeline and stage latencies t1, t2, and t3 such that t1 = 3t2/4 = 2t3. If the longest pipeline stage is split into two pipeline stages of equal latency, What is the new frequency in GHz? Ignore buffer registers delays in the pipeline. **[6]**

(c) **(I)**The stage delays in a 4-stage pipeline are 800, 500, 400 and 300 picoseconds. The first stage (with delay 800 picoseconds) is replaced with a functionally equivalent design involving two stages with respective delays 600 and 350 picoseconds. How many percent throughput of the pipeline increase? **[4]**
**(II)** Define: spatial and temporal expansion of ALU. **[2]**

**Q.3** (a) A 5-stage pipelined processor has Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Perform Operation (PO) and Write Operand (WO) stages. The IF, ID, OF and WO stages take 1 clock cycle each for any instruction. The PO stage takes 1 clock cycle for ADD and SUB instructions, 3 clock cycles for MUL instruction, and 6 clock cycles for DIV instruction respectively. Operand forwarding is used in the pipeline. What is the number of clock cycles needed to execute the following sequence of instructions? Also classify all the data dependency present between instructions. **[6]**

| | **Instruction** | **Meaning of Instruction** |
|---|---|---|
| I1 | ADD R1,R5,R1 | R1=R5+R1 |
| I2 | MUL R1,R2,R3 | R1=R2*R3 |
| I3 | SUB R2,R6,R2 | R2=R6-R2 |
| I4 | DIV R5,R1,R5 | R5=R1/R5 |
| I5 | ADD R2,1,R1 | R2=R1+1 |

(b) For the pipeline reservation table shown below calculate forbidden set F, minimum latency (Lmin), minimum constant latency (Lcmin) and also construct task initiation diagram. **[6]**

| Stage | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| S1 | × | | | | | × | | × |
| S2 | | × | | × | | | | × |
| S3 | | | × | | × | | × | |

**OR**

**Q.3** (a) Write down steps of 2`s complement division (restore) algorithm and perform division using Dividend=21 Divisor=4. **[6]**

(b) **(I)**A hardwired CPU uses 10 control signals S1 to S10, in various time steps T1 to T5, to implement 4 instructions I1 to I4as shown below: **[4]**

| | T1 | T2 | T3 | T4 | T5 |
|---|---|---|---|---|---|
| I1 | S1,S3,S5 | S2,S4,S6 | S1,S7 | S10 | S3,S8 |
| I2 | S1,S3,S5 | S8,S9,S10 | S5,S6,S7 | S6 | S10 |
| I3 | S1,S3,S5 | S7,S8,S10 | S2,S6,S9 | S10 | S1,S3 |
| I4 | S1,S3,S5 | S2,S6,S7 | S5,S10 | S6,S9 | S10 |

What are the expressions for generating control signals S5 and S10 respectively?
$(I_j+I_k)T_n$ indicates that the control signal should be generated in time step $T_n$ if the instruction being executed is $I_j$or $I_k$.

**(II)** For 2909 microprogram sequencer wrtie condition of microinstruction control field for the following: **[2]**

**(a)** RETURN **(b)** GOTO ZERO.