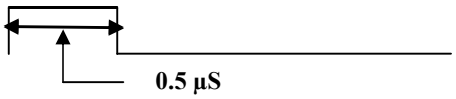
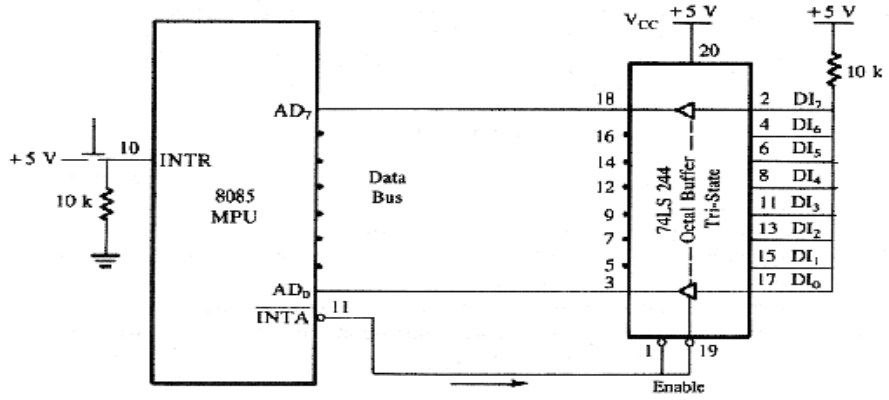
DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
SECOND SESSIONAL

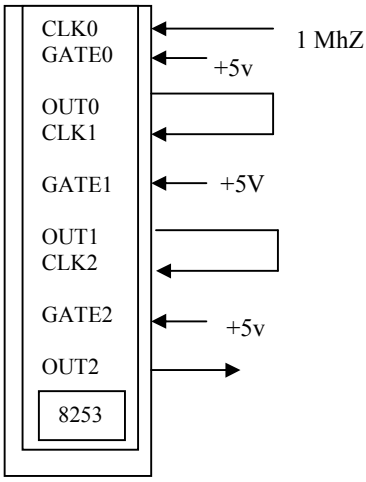
SUBJECT CODE : (IT403) SUBJECT NAME : Microprocessor Architecture Programming & Interfacing

Examination	**: B.TECH - Semester - IV**	**Seat No.**	**:**
Date	**: 17/02/2016**	**Day**	**: Wednesday**
Time	**: 11.15 to 12:30**	**Max. Marks**	**: 36**

INSTRUCTIONS:

1. **Figures to the right indicate maximum marks for that question.**
2. **The symbols used carry their usual meanings.**
3. **Assume suitable data, if required & mention them clearly. 4. No marks without justification.**
5. **Draw neat sketches wherever necessary**

Q.1	**Do as directed.**		
	(a)	**As a part of a INTR interrupt response, 8085 reads a opcode during the first machine cycle of interrupt acknowledge machine cycle. How is it different from normal opcode read cycle ? Explain in detail.**	**[2]**
	(b)	**If you want to transfer data bi-directionally using port A, which mode of 8255 will be used ?**	**[2]**
	(c)	**If ICW1is initialized with D2h and ICW2 is initialized with 80h and interrupt arrives on IR2 pin of 8259. Show how 8259 will form the ISR address from the information provided in the ICW1 and ICW2.**	**[2]**
	(d)	**If TRAP arrives during 1st machine cycle and HOLD arrives during 3rd machine cycle of an instruction. Instruction takes 4 machine cycles to complete the operation. 8085 will respond to HOLD first even it has arrived during 3rd machine cycle. State True/false and justify.**	**[2]**
	(e)	**During the execution of 4 machine cycle instruction, INTR arrived during 1st machine cycle and RST5.5 arrived during 3rd machine cycle. 8085 would first respond to RST5.5. State T/F and justify.**	**[2]**
	(f)	**If you forget to write EI instruction in TRAP subroutine, 8085 will never respond to all maskable interrupt. State T/F and justify.**	**[2]**
Q.2			
	(a)	 **The above signal is connected to RST7.5 and TRAP pins of the 8085 and 8085 is operating at 4 MHz clock. Assuming RST 7.5 is already enabled, describe the response of 8085 for following two cases :** **1. RST 7.5 interrupt subroutine takes 100 µS and EI is written just before the RET instruction in RST 7.5 interrupt subroutine. TRAP interrupt subroutine takes 50 µS.** **2. If RST 7.5 interrupt subroutine takes 50 µS and EI is written in the beginning of the RST 7.5 interrupt subroutine. TRAP interrupt subroutine takes 100 µS.**	**[6]**
	(b)	 **Write the response of 8085 (assuming maskable interrupt system is enabled) in detail when the key is pressed (assuming there is no key bounce).**	**[6]**
		OR	
	(b)	**Write a program to generate approximate 1 KHz square wave on PC5 pin of 8255 using BSR mode whose control port is 83H. Assume 8085 is operating at 1 Mhz clock.**	**[6]**
Q.3	**(a)**	**Initialise the 8279 for 8-bit 8 character left entry, 2 key lock out encoded key matrix mode. Write a program to read a 8-bit key code from the FIFO using polled mode of 8279. Assume control port is 81H and data port is 80H. Assume 8 seven segment LEDs are connected and the 8-bit seven segment code for numerals 0 to 9 are 00 to 09. Write a program to display 0 to 8 in 8 seven segment display. Draw neat flow chart.**	**[6]**
	(b)	**Write a code to unmask RST7.5, RST5.5 and mask RST6.5.**	**[2]**
	(c)	**2100 LXI SP,4000h** **MOV A,B** **If 8085 responds to interrupt after the execution of MOV A,B instruction, draw the stack frame.**	**[2]**

		OR	
	(d)	**RST is a one byte CALL instruction. Justify the statement.**	**[2]**
Q.3	**(a)**	**Why DMA data technique is faster than interrupt or polled mode data transfer techniques ? Explain.**	**[2]**
	(b)	**Without resetting the 8085, how 8085 can comes out from Halt state ? After coming out from the Halt state, from which address it will start fetching the opcode of a new instruction ?**	**[2]**
	(c)	**List advantages/disadvantages of time multiplexed display technique using simple output port in microprocessor based system.**	**[2]**
	(d)	 Initialise and load the counts in three counters such a way to get 1 Hz square wave frequency at OUT2 of counter2 of 8253 shown in figure. Assume control port as 83H. Show how the control words and counts have been decided.	**[6]**