DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
B.TECH. SEMESTER IV [Information Technology]
SUBJECT: (IT-402) Computer Organization

Examination	**: Block Sessional**	**Seat No.**	**:**
Date	**: 08/04/2013**	**Day**	**: MONDAY**
Time	**: 2 to 3:15**	**Max. Marks**	**: 36**

INSTRUCTIONS:

1. Figures to the right indicate maximum marks for that question.
2. The symbols used carry their usual meanings.
3. Assume suitable data, if required & mention them clearly.
4. Draw neat sketches wherever necessary.

Q.1 **Do as directed.** **[12]**

a What is age register? **[2]**

b The DMA breakpoint is at the end of the machine cycle and Interrupt breakpoint is at the end of instruction cycle. True/False. Justify **[2]**

c Differentiate: RISC and CISC. **[2]**

d Explain user and supervisor mode programs. **[2]**

e Justify: Block Diagram conveys Structure rather than Behavior. **[2]**

f Write steps involved in execution of CLEAR instruction. **[2]**

Q.2 Attempt the following questions. **[12]**

(A) **(I)**An instruction is stored at location 300 with its address field at location 301.the address field has the value 400.A processor register R1 contains the number 200.Evalute the effective address if the addressing mode of the instruction is **[4]**
(a)Direct; (b) Immediate ;(c) relative ;(d) register indirect; (e) index with R1 as the index Register

(II)A pipeline has a speedup factor 8.5 and has efficiency 70%, how many stages do the pipelining has? **[2]**

(B) **(I)** Explain DMA transfer process with diagram. **[4]**

(II) What is the average memory access time from the following options for a 3 level memory system where T2=2T1 and T3=3T1 and hit ratio's H1=H2=0.9[T1 is effective access time].calculation necessary. **[2]**
(A)1.11T1 (B)1.22T1 (C)1.09T1 (D)1.01T1

Q.3 **(A)** **(I)** Assume that the unpipelined machine has 10ns clock cycles and that it uses 4 cycles for ALU operations and 3cycle for branches and 5 cycles for memory operations. Assume that the relative frequencies of these operations are 40%, 20% and 40% respectively. Suppose that due to clock skew and set up, pipelining the machine adds 1 ns of overhead to the clock. Ignore any latency impact. What is the average instruction execution time on unpipelined machine? What is the average instruction execution time on pipeline machine? What is the speedup? **[4]**

(II) Write a short note on co-processsor. **[2]**

Q.3 **(B)** **(I)** Write code to implement the expression: **A= (B + C) * (D + E)**on 3-, 2-, 1- and 0-address machines. In accordance with programming language practice,computing the expression should not change the values of its operands. **[4]**

(II) Give the difference between hardwired and microprogramming. **[2]**