**DHARMSINH DESAI UNIVERSITY, NADIAD**
**FACULTY OF TECHNOLOGY**
**B.TECH. SEMESTER IV [INFORMATION TECHNOLOGY]**
**SUBJECT: (IT-402) COMPUTER ORGANIZATION**

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| **Examination** | **: First Sessional** | **Seat No.** | **: _____** |
| **Date** | **: 09/01/2018** | **Day** | **: Tuesday** |
| **Time** | **: 10:00 to 11:15 AM** | **Max. Marks** | **: 36** |

**INSTRUCTIONS:**
1. Figures to the right indicate maximum marks for that question.
2. The symbols used carry their usual meanings.
3. Assume suitable data, if required & mention them clearly.
4. Draw neat sketches wherever necessary.

**Q.1 Do as directed.**

(a) What must the address field of an indexed addressing mode instruction (with XR being the index registers) be to make it the same as a register indirect mode instruction (with XR being the used register for indirect address generation)? **[2]**

(b) Match the following: **[2]**

| | |
|---|---|
| **(1)**Constant | (**P)**Indirect addressing |
| **(2)** Pointer | (**Q)** Direct addressing |
| **(3)** Array Implementation | (**R)**Auto increment addressing |
| **(4)** Loops | (**S)**Index addressing |
| | (**T)**Immediate addressing |

(c) To obtain an operand value how many time memory access would take place in case of following addressing mode: ( (I) Direct, (II) Indirect. **[2]**

(d) Differentiate: loosely coupled and tightly coupled systems. **[2]**

(e) Differentiate: RISC and CISC machine. **[2]**

(f) How multitasking is different from multiprogramming? **[2]**

**Q.2** Attempt ***Any Two*** from the following questions. **[12]**

(a) **(I)** A hypothetical computer stores floationg point numbers in 7 bits.The first bit is used for sign of number,the next three for the biased exponent and the next three for the magnitude of the mantissa.What is the decimal number equivalent to$(0010110)_2$? **[4]**

**(II)** What are processor level componenets? Why communication between processor level componenets is asynchronous? **[2]**

(b) A machine has a 32-bit architecture, with 1-word long instructions. It has 64 registers, each of which is 32 bits long. It needs to support 45 instructions, which have an immediate operand in addition to two register operands. Assuming that the immediate operand is an unsigned integer, What is the maximum value of the immediate operand? **[6]**

(c) A message is made up entirely of characters from the set X={P,Q,R,S,T},whose probabilities are 0.22, 0.34, 0.17, 0.19, 0.08 respectively. If a message of 100 characters over X is encoded using Huffman coding, what is the expected length of the encoded message in bits? **[6]**

**Q.3** (a) Consider a set of four processors P0, P1, P2, and P3, where Pi is an i-address machine. P0 is a zero-address stack machine, while P1, P2, P3 are conventional computers each with 16 general-purpose registers R0:R15 for data and address storage. All four processors have instructions with the opcodes ADD, SUB, MUL and DIV to implement the operations +,-,* and / respectively. Write a program for each of the four machines to evaluate the following arithmetic expression:X := ( ( A / ( B+C ) ) + ( D*E ) – ( A*C ) **[6]**

(b) **(I)** Let the address stored in the program counter be designated by the symbol X1. The one byte instruction stored in X1 has an address part (operand reference) X2. The operand needed to execute the instruction is stored in the memory word with address X3. An index register contains the value X4.What is the relationship between these various quantities if the addressing mode of the instruction is (a)indirect;(b)relative;(c)indexed? **[3]**

**(II)** Assume an instruction set that uses a fixed 16-bit instruction length. Operand specifiers are 6 bits in length. There are K two-operand instructions and L zero operand instructions. What is the maximum number of one-operand instructions that can be supported? **[3]**

**OR**

**Q.3** (a) Devlop SECSED code for a 16-bit data.Generate the code for the data 0101000000111001.Show the code will correctly identify an error in the data bit 5. **[6]**

(b) Explain the organization of IAS machine with diagram. **[6]**