DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
THIRD SESSIONAL
SUBJECT NAME : (IT506) ADVANCED MICROPROCESSOR ARCHITECTURE

Examination	**: B.TECH - Semester - V**	**Seat No.**	**:**
Date	**: 05/10/2015**	**Day**	**: MONDAY**
Time	**: 12.00 TO 1.15**	**Max. Marks**	**: 36**

INSTRUCTIONS:
1. **Figures to the right indicate maximum marks for that question.**
2. **The symbols used carry their usual meanings.**
3. **Assume suitable data, if required & mention them clearly.**
4. **Draw neat sketches wherever necessary.**

Q.1 Answer the following.

(a) Assume that the following pair of instructions of SMAC2P cause a data page fault and an arithmetic exception at the same time, since LD is in the MEM stage while the ADD is in the EX stage. How this ***multiple exceptions occuring in the same clock cycle*** can be handled by the processor? **02**

Instructions	1	2	3	4	5	6
LD	FI	DE	EX	**MEM**	SR	
ADD		FI	DE	**EX**	MEM	SR

(b) What is delay slot? How it improves the delay due to control hazard? **02**

(c) What is difference between superscalar processing and superpipelining? Can one combine the two? If yes then explain how? **02**

(d) Differentiate fine grained and coarse grained jobs with example. **02**

(e) If a program has 18% conditional branch instructions and 4% unconditional branch instructions and if 7% of conditional branches are taken branches, calculate the loss in speedup of a processor with 4 pipeline stages. **02**

(f) The size Prediction bits field of BPB is 2 bits. Explain why? **02**

Q.2 Answer any *Two*.

(a) Design a scoreboard for following sequences of instructions. Show Instruction status, Functional unit status, Register result status using tables. State the assumptions if any. Explain all steps. **06**

I1:	MULT	R1	R3	R5
I2:	SUB	R2	R4	R3
I3:	DIV	R6	R1	R4
I4:	ADD	R4	R2	R3

Functional Unit (FU)	***No. of FUs***	***Latencies (in cycles)***
Multiply	1	4
Add	1	1
Divide	1	4

(b) An examination paper has 5 questions. The answer to these questions does not take equal time to correct. Answer to question 1 takes 4 min. to correct, question 2 takes 6 minutes, question 3 takes 5 minutes, question 4 takes 5 minutes and question 5 takes 8 minutes. Due to this speed mismatch storage should be provided between teachers. Answer the following questions assuming 2000 papers are to be corrected by 5 teachers. **06**

1. What is the idle time of teachers?
2. What is the system efficiency?
3. What will be the efficiency of system if the data parallel mode is given?

OR

(b)
1. In the pipeline mode of processing we assumed that there is no communication delay between stages of the pipeline . If there is a delay of **y** between pipeline stages derive a speed up formula. What condition should **y** satisfy to ensure a speedup of at least **0.8k** where k is the no. of stages in the pipeline ? **04**
2. The average number of instructions a thread executes before it suspends is 15, the delay when a thread suspends and switches to another one is 3 cycles and the average number of cycles it waits before it gets the resource it needs is 35.What is the number of threads the processor should support to hide the latency? What is the processor efficiency? (Assume 5 stage pipelining of SMAC2P) **02**

Q.3 **(a)** The following expressions are to be evaluated: **06**

$a = \sin(x^2y) + \cos(xy^2) + \exp(-xy^2)$

$b = f(u^2) + \sin(g(p)) + \cos^2(h(y^2))$

(i) Obtain a task graph for calculating a, b.

(ii) Assuming 4 processors are available. Obtain a task assignment to processors assuming the following timings for various operations:

squaring= multiplication = negation= 1

sin = cos = exponentiation = 2

g(x) = h(x) = f(x)=3

(b) What is Multithreading? Name 3 types of Multithreaded Processors. Briefly explain the techniques employed to schedule the threads for each type. **06**

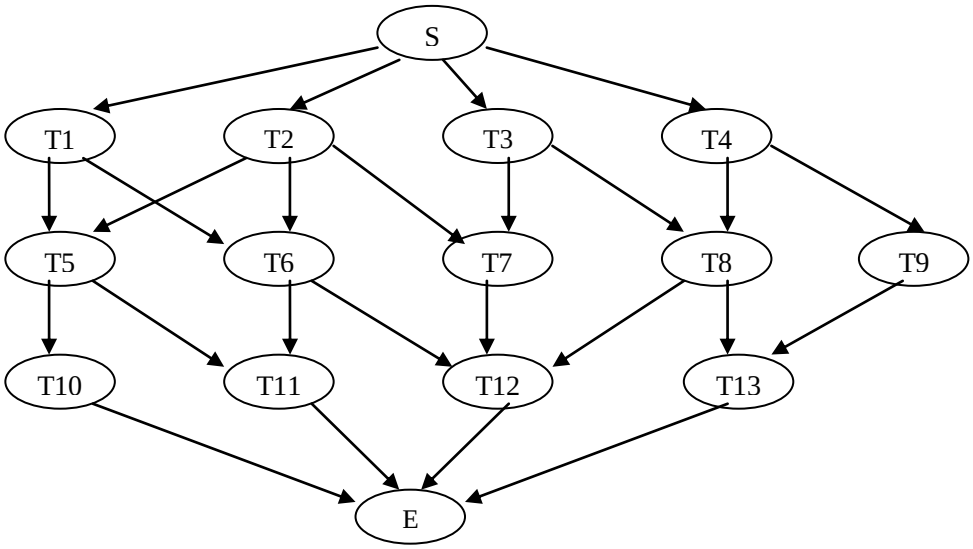
OR

Q.3 **(a)** For the given sequence of instruction develop superscalar pipeline execution diagram (Assume two floating point and two integer execution unit). **06**

Instruction	Number of cycle needed	Arithmetic unit needed
R2←R2 * R6	2	Floating point
R3←R2+R1	1	Integer
R1←R6+8	1	Integer
R8←R2 – R9	1	Integer
R5←R4/R8	2	Floating point
R6←R2+4	1	Integer
R2←R1+2	1	Integer
R10←R9*R8	2	Floating point

Reschedule instructions (If possible) to reduce the no of cycles needed to execute given set of instructions. Assume that instruction window size is 3 instructions. Show the appropriate execution diagram.

(b) A Task graph with various tasks timing is given in Figure below. Assuming that 4 processors are available assign tasks to processors. **06**



T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13
3	4	5	4	6	7	6	5	6	8	9	10	9