DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
B.TECH. - SEMESTER – V [INFORMATION TECHNOLOGY]
SUBJECT: (IT506) ADVANCED MICROPROCESSOR ARCHITECTURE

Examination	**: BLOCK(Repeater)**	**Seat No.**	**:**
Date	**: 10/11/2017**	**Day**	**: Friday**
Time	**: 11:00 TO 12:15**	**Max. Marks**	**: 36**

INSTRUCTIONS:
1. **Figures to the right indicate maximum marks for that question.**
2. **The symbols used carry their usual meanings.**
3. **Assume suitable data, if required & mention them clearly.**
4. **Draw neat sketches wherever necessary.**

Q.1 Answer the following.

(a) What is difference between superscalar processing and super pipelining? Can one combine the two? If yes then explain how? **02**

(b) Even though 8086 has 1 Mbytes of physical memory, it can access only 64 kbytes memory at a time. Justify **02**

(c) 'C' uses processor registers to pass parameters to the function. State True/False Justify **02**

(d) If DS=2000H, SS=1000H, BP=E000H, SI=E000H, the instruction MOV AL,[BP+SI] will move the data from physical memory location 2C000H. State True/False Justify **02**

(e) Register scoreboarding and renaming technique will resolve all types of dependency between instructions of a program. True/False. Justify **02**

(f) if a BTB is to be used in a 16-bit processor whose addressing capacity is 32Mbytes.What could be the word size(bit length) of BTB(assume only 1-bit predictor is used)? **02**

Q.2 Answer any *Two*.

(a) Write an assembly program to move a string 'ADVANCED MICROPROCESSOR' which is defined in a logical segment named DATA1 to another logical segment named DATA2. Use a MACRO to copy a string from source to destination. The macro has 3 parameters: length of a string, offset of source string and offset of a destination string. **06**

(b) Consider 6 execution stages of lengths 45 ns, 50 ns, 60 ns, 30 ns, 20 ns, and 40 ns. Find the time to execute 1000 instructions on both pipelined and non pipeline machine assuming overhead of 5ns in pipeline machine. Also calculate the speedup. **06**

(c) Describe the following descriptor in detail. If this descriptor is accessed by the program during execution, what kind of action will be performed by 80386 in PM? **06**

FFFFh		**6**
E9h	**FFh**	**4**
000Ch		**2**
FFFFh		**0**

Which are all the checks 80386 will do and will there be any exception(s) due to these checks ?

Q.3 (a) **(1)** Calculate the displacement for jump. **03**

```
        MOV CX,5      ; size 3 bytes
NEXT:   ADD AX,BX     ; size 2 bytes
        NOP           ; size 1 byte
        NOP           ; size 1 byte
        NOP           ; size 1 byte
        JMP NEXT      ; size 2 bytes
```

03

(2) Assume that the base address of LDT is 00120000h and GDT base address is 00100000h. Value loaded into the CS register is 1007h. Is the segment descriptor in the GDT or LDT? What is the starting address of the segment descriptor?

(b) In the examination paper there are 5 questions and each will take on average 5 minutes to correct. 2000 candidates write examination. 5 teachers are employed to correct the papers using pipeline mode. Every question is not answered by all candidates. 20% of candidates do not answer question 1, 5% question 2, 15% question 3, 10% question 4, 12% question 5. **06**

1. How much time is taken to complete grading?
2. What is the efficiency of pipeline processing?
3. If data parallel method is used how much time will be taken to complete grading?

OR

Q.3 (a) In multitasking system, OS should be protected from user program and user program should be isolated from each other. Explain in detail the support provided by 80386 in PM to implement the above requirements. **06**

(b) Explain how 48-bit far pointer (virtual address in program) of 80386 in PM is translated into physical address space in detail and how 80386 manages the 32 Tbytes local virtual memory and 32 T bytes global virtual memory address space in detail. **06**