DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
B.TECH. SEMESTER IV [INFORMATION TECHNOLOGY]
SUBJECT: (IT-402) COMPUTER ORGANIZATION

Examination	**:** BLOCK (Repeater)	**Seat No.**	**: _____**
Date	**:** 5/4/2018	**Day**	**: Thursday**
Time	**:** 3:00 to 4:15	**Max. Marks**	**: 36**

INSTRUCTIONS:
1. Figures to the right indicate maximum marks for that question.
2. The symbols used carry their usual meanings.
3. Assume suitable data, if required & mention them clearly.
4. Draw neat sketches wherever necessary.

Q.1 Do as directed. **[12]**

(a) Convert the following 32 bit IEEE-754 format to decimal: 3F800000H. **[2]**

(b) Explain user and supervisor mode programs. **[2]**

(c) Differentiate: Macro and subroutine. **[2]**

(d) The DMA breakpoint is at the end of the machine cycle and Interrupt breakpoint is at the end of instruction cycle. True/False. Justify **[2]**

(e) "Branch instructions reduce the efficiency of instruction pipelining." Justify **[2]**

(f) Differentiate: RISC and CISC machine.. **[2]**

Q.2 Attempt ***Any Two*** from the following questions. **[12]**

(a) **(I)** Find the product of two numbers X= 4 and Y= -3 using booth's algorithm. **[4]**
(II) A pipeline has a speedup factor 8.5 and has efficiency 70%, how many stages do the pipelining has? **[2]**

(b) Given references to the following pages by a program 0 9 0 1 8 1 8 7 8 7 1 2 8 2 7 8 2 3 8 3.calculate the hit ratio if there are four page frames available to it using FIFO,LRU and OPTIMAL page replacement algorithm **[6]**

(c) **(I)** The memory unit of a computer has 256K words of 32 bits each. The computer has an instruction format with four fields: an opcode field, a mode field to specify one of seven addressing modes, a register field to specify one of 60 processor registers, and a memory address field specify the instruction format and the number of bits in each field if the instruction is one memory word. **[3]**
(II) Explain three speedup techniques. **[3]**

Q.3 (a) Explain Architecture of IAS machine with diagram. **[6]**

(b) **(I)**Write code to implement the expression: A= (B + C) * (D + E) on 3-, 2-, 1- address machines. In accordance with programming language practice, computing the expression should not change the values of its operands. **[4]**
(II) What do you mean by co-processor trap? Explain the format of co-processor instruction. **[2]**

OR

Q.3 (a) Consider the following assembly-language program for a hypothetical RISC **[6]**

```
LD r4,#A          Load constant A into general register r4
LD r5,#B          Load constant B into general register r5
LD r6,#C          Load constant c into general register r6
LD r9,#0          Clear general register r9
BEQ r4,r5,adr1    If r4=r5 then go to adr1
ADD r9,r4,r5      Add the sum of r4 and r5 to r9
MUL r9,r9,r9      Square the content of r9
MUL r9,r9,#1      Increment r9 by 1
adr1:st M(r1),r9  Store r9 in the memory location addressed by r1
```

Identify all possible RAW, WAR and WAW hazards that are present if nothing known about the structure of the RISC`s instruction pipeline.

(b) Discuss the steps involve in DMA transfer process with diagram. **[6]**