DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
B.TECH. SEMESTER IV [IT]
SUBJECT: (IT402) COMPUTER ORGANIZATION

Examination	**: Second Sessional**	**Seat No.**	**: _____**
Date	**: 11/02/2014**	**Day**	**: Tuesday**
Time	**: 11:00 to 12:15**	**Max. Marks**	**: 36**

INSTRUCTIONS:
1. Figures to the right indicate maximum marks for that question.
2. The symbols used carry their usual meanings.
3. Assume suitable data, if required & mention them clearly.
4. Draw neat sketches wherever necessary.

Q.1 Do as directed.

(a) Define following terms (I) Micro instruction (II) Microprogram. **[2]**

(b) How does read and write operation can be implemented in a single clock cycle in any register also give its logic diagram? **[2]**

(c) A pipeline has a speedup factor 8.5 and has efficiency 97%, how many stages do the pipelining has? **[2]**

(d) What do you mean by co-processor trap? Explain the format of co-processor instruction. **[2]**

(e) Why microprogramming is not use in RISC and other high speed processors? **[2]**

(f) Vertical micro instructions have high degree of encoding with limited parallelismTrue/False.Justify **[2]**

Q.2 Attempt Any Two from the following questions. **[12]**

(a) **(I)**Draw and explain 16-bit 4-slice array of 2901s employing carry look ahead adder. **[6]**

(b) **(I)**Consider a floating point pipeline with four stages (S1, S2, S3 and S4) each with combinational circuit only whose delays are 5,6,11,8 ns, respectively. The pipeline registers are required between each stage and at the end of the last stage whose delays are 1ns for each. What is the approximate speed up of the pipeline in steady state under ideal conditions when compared to the corresponding non-pipeline implementation? **[4]**

(II) Differentiate: Combinational ALU and sequential ALU. **[2]**

(c) Consider the following pipeline reservation table of five stage pipeline **[6]**

	Time t						
Stage	1	2	3	4	5	6	7
S1	×			×			
S2		×					×
S3			×				
S4					×		
S5						×	

Find optimal pipeline scheduling strategies for the above pipeline reservation table.

Q.3 **(a)** Identify all possible hazards in the following instructions and show clearly which instructions are involved in what type of hazard (WAW, WAR, RAW and control) and why? **[6]**

Inst 1: LD R1 700(R0)
Inst 2: LD R2 800(R1)
Inst 3: LD R3 900(R1)
Inst 4: ADDI R3,R3, #3
Inst 5: ADDI R4,R2, #3
Inst 6: MUL R2, R2, R3
Inst 7: ADD R5,R4,R2
Inst 8: ADD R6,R6,R5
Inst 9: ADDI R1,R1,#-1
Inst 10: BGTZ R1, #-32
Inst 11: SD R6 1000(R0)
Inst 12: BREAK

(b) Find the product of two numbers X and Y where X=5 and Y= -8 using booths algorithm. Why this method is more preferred than other method? Can you multiply floating point number using this algorithm? Justify your answer **[6]**

OR

(a) **(I)**Derive equations for GCD processor using one-hot method. **[4]**

(II) Draw control unit organization for typical microprogrammed controller. **[2]**

(b) **(I)**In accumulator based CPU instruction fetching takes three cycles, while instruction executing takes from one to three cycles. Explain with diagram. **[4]**

(II) When computer c1 is said to emulate computer c2? **[2]**