DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
FIRST SESSIONAL

SUBJECT CODE : (IT506) SUBJECT NAME : Advanced Microprocessor Architecture

Examination	**: B.TECH - Semester - V**	**Seat No.**	**:**
Date	**: 03/08/2012**	**Day**	**: Wednesday**
Time	**: 10 to 11**	**Max. Marks**	**: 36**

INSTRUCTIONS:

1. **Figures to the right indicate maximum marks for that question.**
2. **The symbols used carry their usual meanings.**
3. **Assume suitable data, if required & mention them clearly.**
4. **Draw neat sketches wherever necessary.**

Q.1 **State true/false and justify your answer (no marks without justification).**

(a) **If string related instructions are not used in the program, 8086 will never access ES automatically.** **02**

(b) **After reset, 8086 fetches it first instruction from physical address 00000H.** **02**

(c) **Even though 8086 has 1 Mbytes of physical memory, it can access only 64 kbytes memory at a time.** **02**

(d) **Two different logical addresses can point to the same physical address in 8086.** **02**

(e) **Interrupt subroutine can not be single stepped.** **02**

(f) **MOV AX,7FFFEH** **02**
MOV BX,02H
ADD AX,BX
INTO
When INTO instruction is executed, type 4 response will be generated.

Q.2

(a) **The 8086 system requires following memory map :** **06**
EPROM - 80000H TO 80FFFH
EPROM device available is of size 2 Kbytes. Use *3625* bipolar PROM as decoder to map above devices using absolute decoding. Write down the truth table and draw the complete circuit diagram. State your assumptions, if any, very clearly.

(b) **Write a program to move a string 'DDIT' which is defined in a logical segment named DATA1 to another logical segment named DATA2 using MOVS instruction. Draw neat flow chart and state your assumptions, if any, very clearly.** **06**

OR

Q.2 **(a)** **MOV AX,FFFH** **06**
MOV BL,02H
DIV BL
Describe the response of 8086 after the execution of DIV BL instruction.

(b) **The 8086 system requires following memory map :** **06**
EPROM - 40000H TO 43FFFH
EPROM device available is of size 8 Kbytes. Use *3625* bipolar PROM as decoder to map above devices using absolute decoding. Write down the truth table and draw the complete circuit diagram. State your assumptions, if any, very clearly.

Q.3 **(a)** **The instruction "JE LABEL" is an example of** **01**
(i) Short jump (ii) near jump (iii) far jump (iv) intersegment jump

(b) **(e) The BP register is typically used for accessing** **01**
(i)extra segment (ii)code segment (iii)stack segment (iv) data segment

(c) **Which of the following is an illegal 8086 instruction** **01**
(i)mov ax,[bx] (b)INC [bx] (c)ADD bx,[bx] (d)ADD ax,[cx]

(d) **IRET instruction modifies** **01**
(i)CS only (iii)IP only (iii)CS and IP (iv)CS, IP and flag register

(e) **If you align your word array to odd address boundary, it will take less time to read the word from this array compared to the array aligned to even boundary address. State true/false and justify.** **02**

(f) **Far CALL instruction will push first IP and then CS on stack. State true/false and justify.** **02**

(g) **If the variable TEMP is defined as TEMP DW 1234h.Write the Instruction to move a MSB byte of variable TEMP into AL register such that assembler should not give any error.** **02**

(e) **Address 00010H in IVT contains 0000H and address 00012H contains 1000H. To what interrupt type do these locations correspond ? What is starting physical address for the interrupt service procedure ?** **02**

OR

Q.3 **(a)** **Which addressing mode allows to have two different machine codes to a instruction ?** **02**

(b) **State the addressing mode for the following instructions :** **04**
(i) Mov ax,[1234] (ii) mov ax,[bx] (iii) mov ax,[bx+si] (iv) mov ax,[bx+1234]

(c) **When processor is executing DIV instruction, a low to high going edge has occurred on NMI pin. Divide by zero error has occurred at the end of the DIV instruction. Describe the response of 8086 for this situation.** **06**