

## DHARMSINH DESAI UNIVERSITY, NADIAD

# FACULTY OF TECHNOLOGY

B.TECH - IT - Semester - III SUBJECT: (IT 301) Design of Digital Circuits

Examination: Third Sessional Seat No.

#### **INSTRUCTIONS:**

- 1. Figures to the right indicate maximum marks for that question.
- 2. The symbols used carry their usual meanings.
- 3. Assume suitable data, if required & mention them clearly.
- 4. Draw neat sketches wherever necessary.

Q.1	<ul> <li>Do as directed.</li> <li>(a) Obtain Characteristic Table and Excitation table of RS flip-flop.</li> <li>(b) What is the difference between serial and parallel transfer? What type of register is used in each case?</li> <li>(c) The memory unit has capacity of 8192 words of 32 bits/word. What is the length of a</li> </ul>						
	(c)	memory address (input bits)? What are decade counters? Show the block diagram of a BCD counter which counts from 0	[2] [3]				
	(e)	to 999. Explain the working of Ring-counter with logic diagram.	[3]				
Q.2	Atte (a) (b)	flops. Draw the logic diagram.	[12] [6] [4] [2] [6]				
	OR						
	<b>(b)</b>	Design a sequential circuit described by the following state equations. Use JK flip-flops.	[6]				

(b) Design a sequential circuit described by the following state equations. Use JK flip-flops.
 A(t+1) = xAB+yA'C+xy
 B(t+1) = xAC+y'BC'

B(t+1) = xAC+y'BC' C(t+1) = x'B+yAB'

#### Q.3 Attempt following questions

[12]

- (a) Reduce the no of states in the following state table **fig-1** & tabulate the reduced state table. [4] State no of flip flop required before and after reduction.
- (b) A sequential circuit has the flip-flops (**X & Y**), two inputs (**a & b**), and one output (**c**). The flip-flop input function and the circuit output function are as follow:

JX = aY+b'Y' JY = aX' c = abX+a'b'Y KX = ab'+X

Obtain the state table and state diagram.

OR

### Q.3 Attempt following questions

[12]

(a) Construct a mod 08-counter using MSI circuit. Give two alternatives

[4]

**Next State** 

0

1

0

0

0

1

[8]

(b) Design a sequential circuit whose state table is given below (**fig-2**) using a 2-bit register and combinational gates. (draw the logic diagram).

Present	Next state		Output	
state	X=0	X=1	X=0	X=1
a	f	b	0	0
b	d	С	0	0
С	f	e	0	0
d	g	a	1	0
e	d	С	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

U	1	1	U	1
1	0	0	1	0
1	0	1	1	1
1	1	0	1	0
1	1	1	0	1

**Present State** 

0

0

1

0

0

0

(Fig-1)

Input

0

1

0