DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
BLOCK EXAMINATION
SUBJECT CODE : (IT506) SUBJECT NAME : Advanced Microprocessor Architecture

Examination	**: B.TECH - Semester - V**	**Seat No.**	**:**
Date	**: 15/10/2015**	**Day**	**: Thursday**
Time	**: 11 to 12.15**	**Max. Marks**	**: 36**

INSTRUCTIONS:

1. **Figures to the right indicate maximum marks for that question.**
2. **The symbols used carry their usual meanings.**
3. **Assume suitable data, if required & mention them clearly.**
4. **Draw neat sketches wherever necessary.**

Q.1 State true/false and justify your answer (no marks without justification).

(a) If string related instructions are not used in the program, 8086 will never access ES automatically. 02

(b) If you load the selector of a code segment which is 'marked' as readable into DS segment register, there will be an exception. 02

(c) Even though 8086 has 1 Mbytes of physical memory, it can access only 64 kbytes memory at a time. 02

(d) Two different logical addresses can point to the same physical address in 8086. 02

(e) An instruction MOV CS:[1234],AX will generate an exception in PM of 80386. 02

(f) What is delay slot ? How it improves the delay due to control hazard ? 02

Q.2 Answer Any Two

(a) The 8086 system requires following memory map : 06

EPROM - 80000H TO 80FFFH

EPROM device available is of size 2 Kbytes. Use *3625* bipolar PROM as decoder to map above devices using absolute decoding. Write down the truth table and draw the complete circuit diagram. State your assumptions, if any, very clearly.

(b) In the examination paper there are 4 questions and each will take on average 5 minutes to correct. 1000 candidates write examination. 4 teachers are employed to correct paper using pipeline mode. Every question is not answered by all candidates. 10% of candidates do not answer question 1, 15% question 2, 5% question 3, 25% question 4. 06

i) How much time is taken to complete grading?
ii) What is the efficiency of pipeline processing?
iii) If data parallel method is used how much time will be taken to complete the grading?

(c) Write a program to move a string 'DDIT' which is defined in a logical segment named DATA1 to another logical segment named DATA2 using MOVS instruction. Draw neat flow chart and state your assumptions, if any, very clearly. 06

Q.3 (a) Pipelining increases the execution time of an individual instruction. State T/F and justify. 02

(b) In 8086, 00000H to 003FFH memory must me RAM (read & write memory).State true/false and justify. 02

(c) If you align your word array to odd address boundary, it will take less time to read the word from this array compared to the array aligned to even boundary address. State true/false and justify. 02

(d) Offset part of the far pointer of call/jmp instruction to point CALL GATE Descriptor is ignored. State true/false & justify in detail 02

(e) IDT is not a memory segment, while LDT is a memory segment. Explain why? 02

(f) What is pipeline hazards ? Classify them. 02

OR

Q.3 (a) The size of IVT and IDT tables are same. State T/F and justify (show your calculation also) 02

(b) State the addressing mode for the following instructions : 04
(i) Mov ax,[1234] (ii) mov ax,[bx] (iii) mov ax,[bx+si] (iv) mov ax,[bx+1234]

(c) Draw the pipeline execution diagram for the following instructions of hypothetical processor SMAC2P : 06

```
MUL R1, R2, R3
ADD R2, R3, R4
INC R4
SUB R6, R3, R7
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Find out the delay in pipeline execution due to data dependency of the above instructions. State your assumptions clearly if any.