DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
B.TECH. - SEMESTER – V [INFORMATION TECHNOLOGY]
SUBJECT: (IT506) ADVANCED MICROPROCESSOR ARCHITECTURE

Examination	**: Block Sessional(Repeater)**	**Seat No.**	**:**
Date	**: 21/10/2016**	**Day**	**: Friday**
Time	**: 11 to 12.15**	**Max. Marks**	**: 36**

INSTRUCTIONS:
1. **Figures to the right indicate maximum marks for that question.**
2. **The symbols used carry their usual meanings.**
3. **Assume suitable data, if required & mention them clearly.**
4. **Draw neat sketches wherever necessary.**

Q.1 Do as directed.

(a) What is difference between superscalar processing and superpipelining? Can one combine the two? If yes then explain how? **[2]**

(b) Differentiate data parallelism with dynamic assignment and data parallelism with quasi-dynamic scheduling. **[2]**

(c) Interrupt subroutine cannot be single stepped. State true/false and justify **[2]**

(d) Even though 8086 has 1 Mbytes of physical memory, it can access only 64 kbytes memory at a time. Justify **[2]**

(e) If the content of the GDTR is 000000280027h, what are the starting and ending addresses of the GDT table? How many descriptors can be stored in the table? **[2]**

(f) G bit in descriptor defines the maximum size of the memory segment in protected mode of 80386. State true/false and justify. **[2]**

Q.2 Attempt ***Any Two*** from the following questions. **[12]**

(a) The 8086 system requires following memory map : **[6]**
EPROM - FC000H TO FDFFFH
EPROM device available is of size 4 Kbytes. Use 3625 bipolar PROM as decoder to map above devices using absolute decoding. Write down the truth table and draw the complete circuit diagram. State your assumptions, if any, very clearly.

(b) Write an assembly program to move a string 'ADVANCED MICROPROCESSOR' which is defined in a logical segment named DATA1 to another logical segment named DATA2. Use a ***MACRO*** to copy a string from source to destination. The macro has 3 parameters: length of a string, offset of source string and offset of a destination string. **[6]**

(c) **(I)**Specify the addressing mode for the following instruction: **[3]**
(1)MOV AX,1234H
(2)MOV AX,[1234H]
(3)MOV AX,[BX+SI]
(II) Explain the salient features of trace processors. Is branch prediction essential in trace processors **[3]**

Q.3 (a) Explain how 48-bit far pointer (virtual logical address in program) of protected mode of 80386 is translated into physical address space if paging is also enabled.. Assuming PDBR=23455XXXh, the Page table address in the PDE5= 45345XXXh, The page Frame address in the PTE32=67345XXXh. Calculate The Physical address of the Linear address 014202CAh **[6]**

(b) Describe the following descriptor in detail. If this descriptor is accessed by the program during execution, what kind of action will be performed by 80386 in PM? **[6]**

FFFFh		6
E9h	FFh	4
000Ch		2
FFFFh		0

Which are all the checks 80386 will do and will there be any exception(s) due to these checks?

OR

Q.3 (a) The following expressions are to be evaluated: **[6]**

$a = \sin(x^2y) + \cos(xy^2) + \exp(-xy^2)$

$b = f(u^2) + \sin(g(p)) + \cos^2(h(y^2))$

(i) Obtain a task graph for calculating a, b.

(ii) Assuming 4 processors are available. Obtain a task assignment to processors assuming the following timings for various operations:

squaring= multiplication = negation= 1

sin = cos = exponentiation = 2

g(x) = h(x) = f(x)=3

(b) Draw the pipeline execution diagram for the following instructions of hypothetical processor SMAC2P : **[6]**

MUL R1, R2, R3

ADD R2, R3, R4

INC R4

SUB R6, R3, R7

Find out the delay in pipeline execution due to data dependency of the above instructions. State your assumptions clearly if any.