DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
B.TECH. - SEMESTER – IV [INFORMATION TECHNOLOGY]
SUBJECT: (IT-402) COMPUTER ORGANIZATION

Examination	**: First Sessional**	**Seat No.**	**:**
Date	**: 19/01/2016**	**Day**	**: Tuesday**
Time	**: 11 to 12:15**	**Max. Marks**	**: 36**

INSTRUCTIONS:
1. Figures to the right indicate maximum marks for that question.
2. The symbols used carry their usual meanings.
3. Assume suitable data, if required & mention them clearly.
4. Draw neat sketches wherever necessary.

Q.1 Do as directed.

(a) **(I)**What is the smallest integer that can be represented by an 8-bit number in 2's complement? **[2]**

(II) The 2's complement representation of the number 43 from the following options is
(a) 01010101(b) 11010101(c) 00101011(d) 10101011

(b) **(I)**_____addressing mode is most suitable to change the normal sequence of execution of instructions **[2]**

(II) The addressing mode, where you directly specify the operand value is_____

(c) "Multitasking is logical extension of multiprogramming "True/False. Justify. **[2]**

(d) What are processor level components? Why the communication between processor level components is asynchronous? **[2]**

(e) What are speedup techniques? How they are useful to improve speedup? **[2]**

(f) What must the address field of an indexed addressing mode instruction (with XR being the index register) be to make it the same as a register indirect mode instruction (with XR being the used register for indirect address generation)? **[2]**

Q.2 Attempt ***Any TWO*** of the following questions. **[12]**

(a) The format of a double-operand instruction of a CPU is: **[6]**

4-bits	4-bits	4-bits
OP Code	Source Data	Destination Data

If 12 double-operand instructions and 32 single-operand instructions must be implemented, and if the op-code field must identify the three groups of n operand instructions, calculate the total number of no-operand instructions that can be implemented.

(b) The frequency of different types of instruction by a machine is tabulated below **[6]**

Addressing Modes	Frequencies
Register	30
Immediate	20
Direct	22
Indirect	17
Index	11

Assuming 2 clock cycle are consumed for an operand to be read from the memory, 1 clock cycle for index arithmetic computation 0 clock cycle if operand available in register or within instruction itself. What is average operand fetch rate of machine?

(c) Consider the following set of Instructions I1,I2,I3,I4,I5,I6 and their respective probabilities are 0.12,0.03,0.07,0.34,0.20,0.24. What will be the compressed sequence of the instructions using Huffman coding corresponding to binary sequence 00011110111001010? From the given options. Calculation necessary. **[6]**
(A) I4,I2,I1,I2,I4,I1 (B) I4,I6,I3,I2,I4,I1 (C) I4,I6,I1,I5,I4,I1 (D) I4,I6,I5,I2,I1,I3

Q.3 (a) **(I)**A 12-bit Hamming code whose hexadecimal value is 0XE4F read from memory. What were the original data bits in hexadecimal? Assume that not more than one bit is in error. Number the bits from left to right. **[3]**

(II) Design multifunction circuit using register-level design which can solve the following function: **[3]**

Z=A+B; A=A-B;Z=A;A=0;A=-A;A=Z+A;Z=Z+A.

(b) Show how the following values would be stored by byte-addressable machines with32-bit words, using little endian and then big endian format. Assume each value starts at address 10_{16}. Draw a diagram of memory for each, placing the appropriate values in the correct (and labeled) memory locations. **[6]**

(I) 456789A116 **(II)** 0000058A16 **(III)** 1414888816

OR

Q.3 (a) The following is a scheme for floating point number representation using 16 bits. **[6]**

15Sign 14 Exponent 9 8 Mantissa 0

S	E	M

Let S, E and M be the numbers represented in binary in the sign, exponent, and mantissa fields respectively. Then the floating point number represented is

$$\begin{cases} (-1)^S \left(1 + m \times 2^{-9}\right) 2^{e-31}, & \text{if the exponent } \neq 111111 \\ 0, & \text{otherwise} \end{cases}$$

What is the maximum difference between two successive real numbers representable in this system?

(b) Explain the architecture of IAS computer with neat diagram. **[6]**