DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
B.TECH. - SEMESTER – IV [INFORMATION TECHNOLOGY]
SUBJECT: (IT-402) COMPUTER ORGANIZATION

Examination	**: BLOCK**	**Seat No.**	**:**
Date	**: 18/04/2016**	**Day**	**: Friday**
Time	**: 3:00 to 4:15**	**Max. Marks**	**: 36**

INSTRUCTIONS:
1. Figures to the right indicate maximum marks for that question.
2. The symbols used carry their usual meanings.
3. Assume suitable data, if required & mention them clearly.
4. Draw neat sketches wherever necessary.

Q.1 Do as directed.

(a) Justify: Block Diagram conveys Structure rather than Behavior. **[2]**

(b) "TLB and Page table both have same content." State True/False with Justification. **[2]**

(c) Explain three speedup techniques. **[2]**

(d) Differentiate: RISC and CISC machine. **[2]**

(e) Why DRAM cells required periodic refreshing? **[2]**

(f) For complete interconnection structure find number of edges, max node degree, where n=64. **[2]**

Q.2 Attempt the following questions. **[12]**

(a) Explain with diagram organization of IAS computer. **[6]**

(b) Given references to the following pages by a program 0 9 0 1 8 1 8 7 8 7 1 2 8 2 7 8 2 3 8 3.calculate the hit ratio if there are four page frames available to it using FIFO,LRU and OPTIMAL page replacement algorithm **[6]**

Q.3 (a) Discuss the steps involve in DMA transfer process with diagram. **[6]**

(b) Consider the following assembly-language program for a hypothetical RISC **[6]**

```
LD    r4,#A        Load constant A into general register r4
LD    r5,#B        Load constant B into general register r5
LD    r6,#C        Load constant c into general register r6
LD    r9,#0        Clear general register r9
BEQ   r4,r5,adr1   If r4=r5 then go to adr1
ADD   r9,r4,r5     Add the sum of r4 and r5 to r9
MUL   r9,r9,r9     Square the content of r9
MUL   r9,r9,#1     Increment r9 by 1
adr1:st  M(r1),r9  Store r9 in the memory location addressed by r1
```

Identify all possible RAW, WAR and WAW hazards that are present if nothing known about the structure of the RISC`s instruction pipeline.