DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
B.TECH. - SEMESTER – IV [INFORMATION TECHNOLOGY]
SUBJECT: (IT-402) COMPUTER ORGANIZATION

Examination	**: Second Sessional**	**Seat No.**	**:**
Date	**: 16/02/2016**	**Day**	**: Tuesday**
Time	**: 11 to 12:15**	**Max. Marks**	**: 36**

INSTRUCTIONS:
1. Figures to the right indicate maximum marks for that question.
2. The symbols used carry their usual meanings.
3. Assume suitable data, if required & mention them clearly.
4. Draw neat sketches wherever necessary.

Q.1 Do as directed.(No Marks Without Justification for Q-1 (a) to Q-1(c))

(a) Consider the following pattern of multiplier: **[2]**
(a) 010101010101 (b) 11111111111111 (c) 1111100111000
Which of the above string will give best performance for Booth's multiplication algorithm? (A) Only (a) (B) Only (b) (C) Only (c) (D) Both (b) & (c)

(b) The performance of a pipelined processor suffers if **[2]**
(A) The pipelined stages have different delays
(B) Consecutive instructions are dependent on each other
(C) The pipeline stages share hardware resources
(D) All the above

(c) For a pipelined CPU with a single ALU, consider the following situations **[2]**
1. The j + 1 th instruction uses the result of j th instruction as an operand
2. The execution of a conditional jump instruction
3. The j th and j + 1 th instructions require the ALU at the same time
Which of the above can cause a hazard?
(A) 1 and 2 only (B) 2 and 3 only(C) 3 only (D) All the three

(d) We have two designs D1 and D2 for a synchronous pipeline processor. D1 has 5 pipeline stages with execution times of 3 nsec, 2 nsec, 4 nsec, 2 nsec and 3 nsec while the design D2 has 8 pipeline stages each with 2 nsec execution time How much time can be saved using design D2 over design D1 for executing 100 instructions? **[2]**

(e) n instruction set of a processor has 125 signals which can be divided into 5 groups of mutually exclusive signals as follows: Group 1 : 20 signals, Group 2 : 70 signals, Group 3 : 2 signals, Group 4 : 10 signals, Group 5 : 23 signals. How many bits of the control words can be saved by using vertical microprogramming over horizontal microprogramming? **[2]**

(f) Give differences between hardwired and microprogramming. **[2]**

Q.2 Attempt ***Any TWO*** of the following questions. **[12]**

(a) Consider a 4 stage pipeline processor. The number of cycles needed by the four instructions I1, I2, I3, I4 in stages S1, S2, S3, S4 is shown below: **[6]**

	S1	S2	S3	S4
I1	2	1	1	1
I2	1	3	2	2
I3	2	1	1	3
I4	1	2	2	2

What is the number of cycles needed to execute the following loop?
for (i=1 to 2) {I1; I2; I3; I4;}

(b) Consider following Mealy machine. Machine M1 reads i/p in little endian form. Now output of M1 is used as a input for machine M2. M2reads input in big endian form. If input for machine M1is 101101 then what is output produced by M2? **[6]**
Machines are as shown in figure-1:-

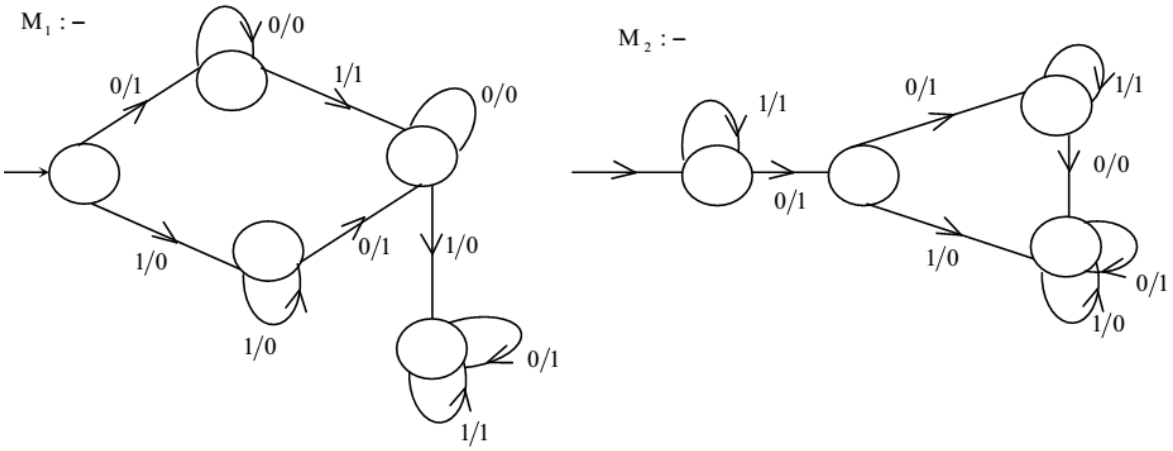

Figure-1

(c) **(I)** Consider the sequence of machine instructions given below: **[3]**

MUL R5, R0, R1
DIV R6, R2, R3
ADD R7, R5, R6
SUB R8, R7, R4

In the above sequence, R0 to R8 are general purpose registers. In the instructions shown, the first register stores the result of the operation performed on the second and the third registers. This sequence of instructions is to be executed in a pipelined instruction processor with the following 4 stages: (1) Instruction Fetch and Decode (IF), (2) Operand Fetch (OF), (3) Perform Operation (PO) and (4) Write back the Result (WB). The IF, OF and WB stages take 1 clock cycle each for any instruction. The PO stage takes 1 clock cycle for ADD or SUB instruction, 3 clock cycles for MUL instruction and 5 clock cycles for DIV instruction. The pipelined processor uses operand forwarding from the PO stage to the OF stage. What is the number of clock cycles taken for the execution of the above sequence of instructions?

(II) A CPU has a five-stage pipeline and runs at 1 GHz frequency. Instruction fetch happens in the first stage of the pipeline. A conditional branch instruction computes the target address and evaluates the condition in the third stage of the pipeline. The processor stops fetching new instructions following a conditional branch until the branch outcome is known. A program executes 10^9 instructions out of which 20% are conditional branches. If each instruction takes one cycle to complete on average, What is the total execution time of the program (in second)? **[3]**

Q.3 (a) What are the advantages of booth's algorithm? Can you multiply floating point numbers using booth's algorithm? Find the product of two numbers X and Y where X=14 and Y= -4 using booth's algorithm. **[6]**

(b) What is the purpose of control unit? What do you mean by control signals? Explain organization of microprogram based control unit. **[6]**

OR

Q.3 (a) **(I)** Define following terms (1) Micro operation (2) Micro instruction (3) Micro program. **[3]**

(II) Design the n-bit two's complement adder-subtracter so that it can compute any of the three operations X+Y, X-Y, or Y-X, as specified by a two bit MODE control input. **[3]**

(b) Design the control unit for gcd processor using classical method. **[6]**