FACULTY OF TECHNOLOGY
B.TECH - Semester - IV
SUBJECT: (IT-402) Computer Organization

Examination	**: Third Sessional**	**Seat No.**	**:**
Date	**: 26/03/2013**	**Day**	**: Tuesday**
Time	**: 9:30 to 10:45**	**Max. Marks**	**: 36**

INSTRUCTIONS:

1. Figures to the right indicate maximum marks for that question.
2. The symbols used carry their usual meanings.
3. Assume suitable data, if required & mention them clearly.
4. Draw neat sketches wherever necessary.

Q.1 Do as directed. **[12]**

a How many 32K x 1 RAM chips are needed to provide a memory capacity of 256K-bytes? **[2]**

b A system uses OPTIMAL policy for page replacement. It has 3 page frames with no pages loaded to begin with. The system first accesses 100 distinct pages in some order and then accesses the same 100 pages but now in the reverse order. How many page faults will occur? **[2]**

c Differentiate: Message Switching and Packet Switching **[2]**

d For Hypercube interconnection structure find number of edges, max node degree, max internode distance, where n=16. **[2]**

e If we let S^R be the reverse of a reference string S, the page fault rate for the FIFO algorithm on S is the same as the page fault rate for the optimal algorithm on S^R. True/False. Justify **[2]**

f Why dynamic memory required periodic refreshing? **[2]**

Q.2 Attempt **Any TWO** of the following questions. **[12]**

a **(I)**Let the page fault service time be 10ms in a computer with average memory access time being 20ns. If one page fault is generated for every 10^6memory accesses, what is the effective access time for the memory? **[3]**

(II) A nine-track magnetic tape has a fixed block & inter block gap sizes. The gap length is 0.6 inch storage density is 1600 b/inch if space utilization is 70% what is block size in bytes? **[3]**

b **(I)**An 8KB 2-way set associative write-back cache is organized as multiple blocks, each of size 32-bytes. The processor generates 32-bit addresses. The cache controller maintains the tag information for each cache block. What is the total size of memory needed at the cache controller to store meta-data (tags) for the cache? **[4]**

(II) Explain Flynn's classification with example. **[2]**

c **(I)** Suppose that a total of 64 MB RAM is available in a system this memory space is partitioned in to 8 fixed size slot of 8 MB each. Assume 8 processes are currently requesting memory usage with size indicated as follows[2 MB,4 MB,3 MB,7 MB,6 MB,9 MB,1 MB,8 MB].calulate the size of memory wasted due to External and Internal fragmentation. Assume exactly one slot can be given to each process. **[4]**

(II) Consider a memory hierarchy system consisting of two levels. The access time of level1 is 2ns.The miss penalty (The time to get data from level2, in case of miss) is 100ns.What is the hit ratio in order to get average access time 5ns? **[2]**

Q.3 Answer the following questions: **[12]**

a Given references to the following pages by a program 0 9 0 1 8 1 8 7 8 7 1 2 8 2 7 8 2 3 8 3.calculate the number of page faults if there are four page frames available to it using FIFO,LRU and OPTIMAL page replacement algorithm. **[6]**

b On a non-pipelined sequential processor, a program segment, which is a part of the interrupt service routine, is given to transfer 512 bytes from an I/O device to memory. **[6]**

Initialize the address register
Initialize the count to 512
LOOP: Load a byte from device
Store in memory at address given by address register
Increment the address register
Decrement the count
If count != 0 go to LOOP

Assume that each statement in this program is equivalent to a machine instruction which takes one clock cycle to execute if it is a non-load/store instruction. The load-store instructions take two clock cycles to execute. The designer of the system also has an alternate approach of using the DMA controller to implement the same transfer. The DMA controller requires 30 clock cycles for initialization and other overheads. Each DMA transfer cycle takes two clock cycles to transfer one byte of data from the device to the memory. What is the approximate speedup when the DMA controller based design is used in place of the interrupt driven program based input-output?

-OR-

Q.3 Answer the following questions: **[12]**

a The available space list of a 19KB memory has the following entries at some time t: **[6]**

Region Address(hex)	**Size(byte)**