DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
B.TECH - IT - Semester - III
SUBJECT: (IT 301) Design of Digital Circuits

Examination	**: Block Exam**	**Seat No.**	**:**
Date	**: 18/10/2014**	**Day**	**: Saturday**
Time	**: 11:00 to 12:15**	**Max. Marks**	**: 36**

INSTRUCTIONS:
1. Figures to the right indicate maximum marks for that question.
2. The symbols used carry their usual meanings.
3. Assume suitable data, if required & mention them clearly.
4. Draw neat sketches wherever necessary.

Q.1 Do as directed. **[12]**

(a) Represent the Decimal number, 620 in **[2]**
i) BCD Code ii) Excess-3 Code iii) 2421 Code iv) Binary

(b) Find complement of: F = X(Y'Z' + YZ) **[2]**

(c) State T/F with Justification: "The NAND operator is Associative" **[2]**

(d) Why Flip-Flop is called a single-bit register? **[2]**

(e) How do the look-ahead carry adder speed up the addition process? **[2]**

(f) Obtain Gray Code for decimal 12 and decimal 15. **[2]**

Q.2 Attempt following questions. **[12]**

(a) Determine the Prime Implicants of the function: **[6]**
$F(A,B,C,D) = \sum (0,4,6,7,8,9,10,11,15)$

(b) Design the sequential Circuit using JK Flip-Flop for given State Stable **[6]**

Present State		Next State			
		X=0		X=1	
A	B	A	B	A	B
0	0	0	0	0	1
0	1	1	0	0	1
1	0	1	0	1	1
1	1	1	1	0	0

OR

(b) Simplify $F(A,B,C,D) = \sum (0,1,2,8,10,11,14,15)$ using Tabulation Method **[6]**

Q.3 Attempt following questions **[12]**

(a) Design and implement SOP that will generate an odd parity bit for a 4-bit input. **[6]**

(b) Design a serial adder using sequential logic procedure. **[6]**

OR

Q.3 Attempt following questions **[12]**

(a) Signal A,B,C,D and D' are available. Using a single 8 x 1 Mux and no other gate implement the Boolean function. **[6]**
$F=\sum(0,1,3,4,8,9,15)$

(b) Derive PLA program table for full subtractor. **[6]**