DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
SECOND SESSIONAL
SUBJECT: (IT 403) Microprocessor Architecture Programming & Interfacing

Examination	**: B.TECH Semester – IV**	**Seat No.**	**:**
Date	**: 15 /02/2018**	**Day**	**: Thursday**
Time	**: 10:00am To 11:15 am**	**Max. Marks**	**: 36**

INSTRUCTIONS:
1. Figures to the right indicate maximum marks for that question.
2. The symbols used carry their usual meanings.
3. Assume any necessary data but giving proper justifications.
4. Be precise, clear and to the point in answering the questions. Unnecessary elaborations will not fetch more marks.

Q.1 Do as directed. **[12]**

(a) System requires 8 seven segment display. How many 8-bit ports are required, if scanned multiplexed display technique is not used. If scanned multiplex display technique is used, how many 8-bit ports are required ? What is the major disadvantage of scanned multiplexed display technique ? [2]

(b) First machine cycle of Auto vector interrupt is Bus Idle machine cycle, State true/false and justify. [1]

(c) With respect to 8085 match column X with column Y : [1]

Column X	Column Y
1. RST 5.5	1. Edge-triggered
2. RST 6	2. Level-triggered
3. RST 7.5	3. Edge and level triggered
4. RST 4.5	4. Software

(d) With respect to 8085 match column X with column Y : [1]

Column X	Column Y
1. INTR	1. Non-maskable
2. RST 5.5	2. Maskable
3. TRAP	3. Software
4. RST 1	4. Non-vectored

(e) Interrupt Auto vector table of 8085 ranges over : [1]
0010H - 0100H
0000H - FFFFH
0000H - 00FFH
0100H - 01FFH

(f) RST7.5 to be recognized, it must be high for minimum number of T-states equal to : [1]
1. 17.5
2. 18.5
3. 19.5
4. none of the above

(g) Before RET instruction in ISR, SP contains 3000H. What will be the value of SP, when it returns to main line program ? [2]

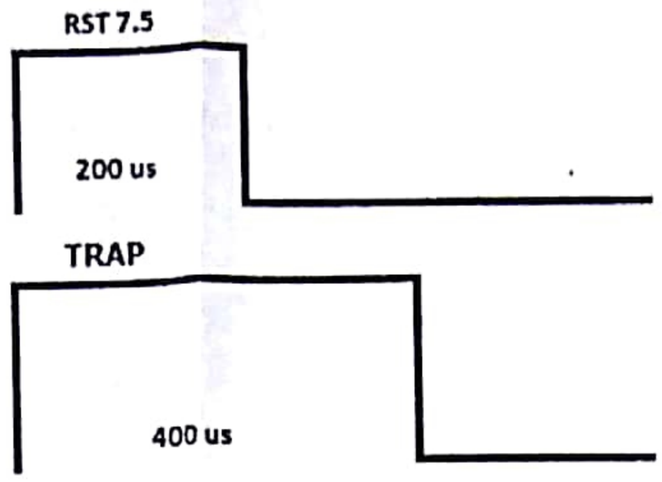
(h) The instruction TST 7 is a : [1]
1. Restart instruction that begins the execution of a program.
2. One-byte call to the memory address 0038H.
3. One-byte call to the memory address 0007H
4. Hardware interrupt.

(i) Through which pin external DMA controller sends a control signal to an 8085 microprocessor? [1]
1. HOLD
2. HLDA
3. INTR
4. INTA

(j) The opcode of the instruction RST 6 in an 8085 microprocessor is: [1]
1. F7
2. EF
3. FE
4. None of above

Q.2 Attempt *Any TWO* of the following questions. [12]

(a) [6]



In 8085 system, as shown in above figure, both RST 7.5 and TRAP arrive at the same time. Pulse width of RST 7.5 is 200 Microsecond and TRAp is 400 microsecond. Assume maskable interrupt system is already enabled and RST 7.5 are unmasked. RST 7.5 & TRAP interrupt service routines take 250 µS each. Also assume that EI is written at the end of the interrupt service routines. Describe the response of 8085.

(b) [6]

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2100   LXI SP,8000h
       STA 2300h
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TRAP interrupt arrives during STA instruction. How many machine cycles required by interrupt acknowledge machine cycle ? Name them. Also state the content of data bus and address bus during T2 and T3 states of every machine cycle. Draw the stack frame.

(c) Write a program to generate 1 KHz square wave on PC5 pin of 8255 using BSR mode whose control port is 83H. Assume 8085 is operating at 1 MHz clock frequency. [6]

Q.3 (a) (i) Initialise the 8279 for 8-bit 8 character right entry, N key Roll over encoded scan keyboard mode. Write a program to read a key code from the FIFO (assuming 8279 is connected in polled mode). Assume control port is 83H. [6]

(ii) If 12 bit ADC is to be connected with 8085, how many input and output lines are required ? Draw the diagram.

(b) (i) Write a piece of code to read counter 1 of 8253 whose control port is 83h. Assume Counter 1 is programmed for 16-bit count. [6]

(iii) Write a program to generate full scale triangular waveform at the output of DAC, which is connected on a simple 8-bit port whose address is 80h.

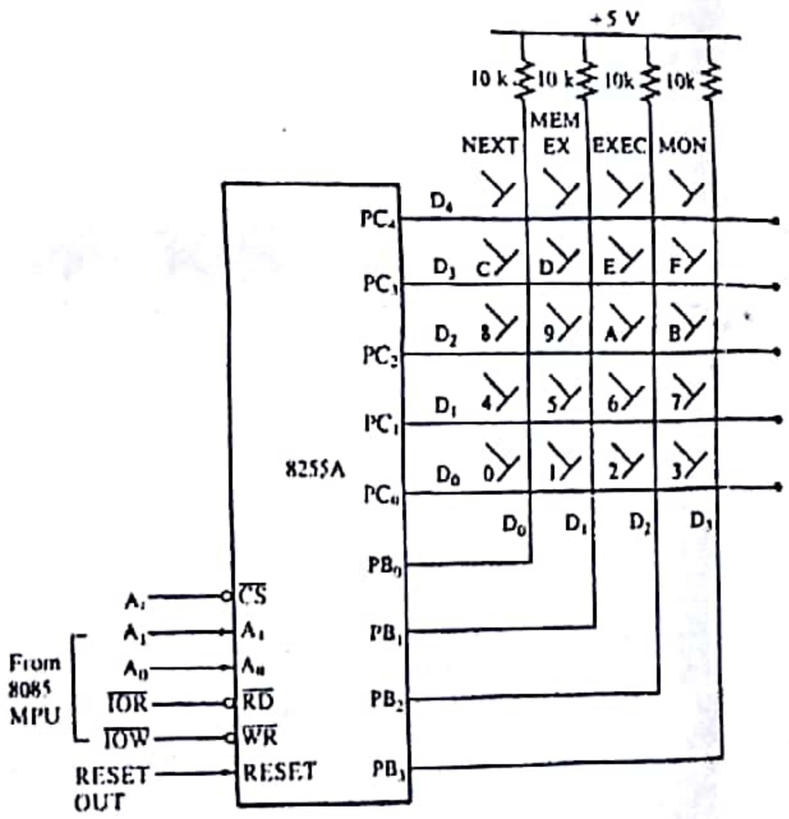
OR

Q.3 (a) (i) If ICW1=FAh and interrupt arrives on IR3 pin of 8259, what will be the LSB byte generated by 8259 for interrupt sub-routine address ? Show how 8259 will calculate this from the information provided in ICW1. [6]

(ii) After the execution of instruction RIM, the accumulator contained 49H. Which of the following statement is TRUE in this case :

1. RST 5.5 is enabled and is pending.
2. RST 6.5 is enabled and is pending.
3. RST 7.5 is enabled and is pending.
4. None of the given options.

(b) [6]



20 keys matrix keyboard is interfaced with 8085 processor through 8255 as shown in figure. Identify port addresses and initialize 8255 in appropriate mode. Write down assembly language program to identify key closure and generate its key code. State your assumptions, if any clearly.