	Page No.
	Date
	Devanshy Surana
	PC-23, Batch Cl
	1032210755
	MAIOT Lab Assignment 9
	The Car was January and Car was a second of the Car wa
	Problem statement:
	Write an ALP to display the contents of GDTR, IDTR, LDTR,
	TRand MSW.
	the state of the s
	Objectives
	1. Understand the concept of protected mode.
	2. Understand the values of GOTR, LOTR, IDTR, TR and
:	MSW Registers.
1	Theory:
1.	Theory: Explain the following instructions used to read the content
	of respective registers.
a.	SADT. Kmem>:
	The contents of the global descriptor table register is
	copied by OCOT to the six butes of memory specified by
	operand. The first word at the Effective address is assigne
	I the limit field of register 890T is not used in
	application programs, they are used in os.
b.	SIDT <mem>:</mem>
	The contents of the interrupt descriptor table register is upied to SIDT. The instruction stores 8-byte base and
	copied to SIDT. The instruction stoles or byle buse win
	2-byte limit values.
,	
	183 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

.

Page No.
Date
The second secon
1. 1
able register (LDTR)
cation indicated by the
istor is a selector
table SLD.T. is only
ive.
, , , , , , , , , , , , , , , , , , , ,
egisters value into
gisters value into
1
itch to protected
nto destination operand.
in operating system
' J, O
egisters. Write use of

c SLDT Kmem >:

SLDY stores the local descriptor table register. CLDTR in 2-byte Register or memory location indicated by the effective address operand. The registor is a selector that points into Global Descriptor table. SLDT is only used in operating system software.

di STR Lmem >:

STR instruction store the task registers value into a memory. The memory address to load from or store to is at an offset from the register.

e. SMSW. Kmem'>:

This instruction can be used to switch to protected mode stores machine status word into destination operand. The SMSW instruction is only useful in operating system software.

2. Draw the structure of the each registers. Write use of the registers GDTR, IDTR, LDTR and TR.

-> System Table Registers.

aptr 32-bit linear Base Address 16-bit Table limit 1DTR 32-bit linear Base Address 16-bit Table limit

Task Register Seg Sel LDTR seg sel

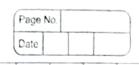
Uses:

Holds the Base Address and loads new Base Address as parts of processor initialization process for protected mode operation.

Page No.		
Date		Latigation of the Control

				Page No.		
3.	Draw dig diagramm pointed to.	aticaly the	tables	where !	these regis	sters
	Task Register		GDT		1,	
	1. 1663 A M MC		1			
Interrupt			Seg. 1	Desc	Segment	set
vector	TOT	100		11 11		
	2.111.1	yell tribals	TSS	Desc	TR.	
	Interrupt gate -	>	seq	Desc	.1.	
•	Interrupt gate	1>	 કલ્વ	Desc	1.: -	
	> Trap gate -	· : J.		-1 .0	e Vic	
			IL LOST	Desc	તં	
		,) · .	16	7-1	\
	LIDTR			GOTR		
	Lī	T		÷., † ;. ` .		
	Leave trial and and and	the pregna	1.07.60.	. rolyini,	1.1.	
	Seg	· Desc			`.	
	selector Cal	1.1	· · · · ·	.1"		
6	selector Cal	gate				
					. 1 .	
A			<u> </u>	4 11 72		,
	LDTR			15 7 1		
,	0) 11					
3	Algorithm	: 1 · 1 · 1			1	11.
1.	Initialize the golf I a	nd left v	variable	by 6 by	re and 10	ITIC
11/2 17/2	Initialize the golt 1 and the variable by Store the MSW or	2 byte an	d Msu	11 by 2	byte.	
2.	Store the MSW or	CKID conten	TINT	re accur	MUIQIOI ·	
	Check the Bito of			rt-011-	TYOTELTO	11
					•	
	A CONTRACTOR AND A CONT		1 1		L'i	

	Page No.
4.	if it is set (i) then processor mode lese it is
1	reset (0) then processor is in real mode!
5.	If processor is in protected made then stored the contents
	of memory management register in to assigned variable
	using special instruction i.e. SGDT, SIDT, SLDT, STR.
6.	Display the contents of memory management register
	Display the contents of memory management register one by one byte using unpacking logic
7.	End.
	Platform: OS-Ubuntu 16,64-bit
	System Calls Used: -
	* SYS write call
	* 848 exit call
	Conclusion:
	Thus implemented the program in assembly language to
	Thus, implemented the program in assembly language to display the contents of system register used in protected
	mode memory management and MSW.
	FAQ's
1	
-) What is protected mode? How is processor switched from
	real to protected mode? Using which register and which
	real to protected mode? Using which register and which flag?
	real to protected mode? Using which register and which flag? Protected mode is a mode of operation in modern
	real to protected mode? Using which register and which flag? Protected mode is a mode of operation in modern X86 processors that provides hardware - enforced mem-
	real to protected mode? Using which register and which flag? Protected mode is a mode of operation in modern X86 processors that provides hardware - enforced mem- ony protection, virtual memory, and advanced fearetures
	real to protected mode? Using which register and which flag? Protected mode is a mode of operation in modern X86 processors that provides hardware - enforced mem- ony protection, virtual memory, and advanced fearltures The processor is switched from real to protected
	real to protected mode? Using which register and which flag? Protected mode is a mode of operation in modern X86 processors that provides hardware - enforced mem- ory protection, virtual memory, and advanced fearetures The processor is switched from real to protected mode by loading the GDT address into the GDTR.
	real to protected mode? Using which register and which flag? Protected mode is a mode of operation in modern X86 processors that provides hardware - enforced mem- ony protection, virtual memory, and advanced feartures The processor is switched from real to protected



- 2) What is MSWI Explain Bits present in MSW in brief.
- The machine status word is stored by smsw in the two-byte register of memory location pointed to by the Effective Address operand

8086 machines should use MOV --- , CRO

Store the machine status word in the Effective Address SMSW 5 (ebx).

The machine status word consists of 4 flags - PE,MP, EM and TS of four lower order Bits. D19 to D16 of the upper word of the flag register.

PE - Protection Enable, switches processor between protected and real mode.

MP- Math present, Gontrols functions of wait.

EN - Emulation indicates whether co-processor function are emulated

TS - Task switched Intrepreting co-processor instructions. ET- Extension Type.

Next Bits are perserved and the PG-Paging indicate whether processor uses page tables to translate linear addresses to physical Addresses.

- 3) Explain difference between Real Address mode and protected mode.
- Real mode program uses BIOS subroutines along with as subroutines whereas a 'protected mode' program uses only as subroutines.

 Instruction code differs since opcodes for registers

Instruction code differs since opcodes for register are different and offset addresses of different teg length.

Name: Devasnhu Surana Roll No.: 23

Panel: C Batch: C1

MAIoT Assignment 09

write real, real len imp end

CODE:

%macro write 2 mov rax,1 mov rdi,1 mov rsi,%1 mov rdx,%2 syscall %endmacro section .data gmsg db 10,10,"The contents of GDTR are: "gmsg len equ \$-gmsg lmsg db 10,10,"The contents of LDTR are: " lmsg len equ \$-lmsg imsg db 10,10,"The contents of IDTR are: "imsg len equ \$-imsg tmsg db 10,10,"The contents of TR are: "tmsg len equ \$-tmsg mmsg db 10,10,"The contents of MSW/CR0 are: " mmsg len equ \$-mmsg pro db 10,10,"The processor is in protected mode "pro len equ \$-pro real db 10,10,"The processor is in protected mode "real len equ \\$-real col db ":" col len equ \$-col nline db 10,10 nlen equ \$-nline section .bss buff resb 4 gdt1 resb 6 idt1 resb 6 ldt1 resw 1 t1 resb 2 msw1 resb 4 section .text global start start: smsw eax mov [msw1],eax bt eax,0 ic protected

```
protected:
write pro, pro len sgdt [gdt1]
sldt [ldt1]
sidt [idt1]
str [t1]
write gmsg,gmsg len mov bx,[gdt1+4]
call original ascii mov bx,[gdt1+2]
call original ascii write col,col len mov bx,[gdt1] call original ascii
write lmsg,lmsg len mov bx,[ldt1]
call original ascii
write lmsg,lmsg len mov bx,[idt1+4] call original ascii mov bx,[idt1+2]
call original ascii write col,col len mov bx,[idt1]
call original ascii
write tmsg,tmsg len mov bx,[t1]
call original ascii
write mmsg,mmsg len mov bx,[idt1+4]
call original ascii
mov bx, [idt1+2]
call original ascii
end:
write nline, nlen mov rax, 60 mov rdi, 0
mov rsi.0
mov rdx,0 syscall
original ascii: mov rax,0 mov rex,4
mov rdi,buff up2: rol bx,4 mov dl,bl
and dl,0fh cmp dl,09h jbe down2 add dl,07h
down2: add dl,30h mov [rdi],dl
inc rdi
loop up2 write buff,4
```

OUTPUT:

