DK-303

Dr. Vishwanath Karad
MIT WORLD PEACE UNIVERSITY | PUNE
MIT-WPU

PRN: 1032210755

End Semester Examination

May-June 2023

CET3014B - Microprocessor Architectures and Internet of Things

Schedule ID: 19075

Faculty/School	Faculty of Engineering & Technology	**Term**	IV
Program	Second Year B. Tech	**Duration**	**1 Hours 30 Minutes**
Specialization		**Max. Marks**	**40**

Read the instructions provided for every question properly before attempting the answer.

Section - 1 : contain(s) **10** question(s) and each question carries 5 mark(s).You can answer any **8** questions out of **10.**

Click **Finish** only after completion of the Exam.

Section - 1 (8 X 5 Marks)
Answer any 8 questions

1	Draw and explain architecture of embedded system. List any 4 types of embedded system.	**5 marks**	CO1	Understanding
2	List any five features of Pentium processor and clearly explain their role in increasing performance of the processor.	**5 marks**	CO3	Remembering
3	Explain the structure of GDT. Which register holds the base address of GDT? Draw the related register and describe it.	**5 marks**	CO5	Understanding
4	Describe the segment selector. What is its purpose? Analyze the content of the CS register 0017H to find the following values. 1. Table Indicator 2. Requested Privilege Level 3. Descriptor Index	**5 marks**	CO5	Applying
5	5 For a given instruction MOV AH, [EDI], assume that EDI=00001114H, the base address of the LDT is 00151012H and the GDT base address is 00220024H. If the value of the selector loaded into the DS register is 0021H, then what is the Requested Privilege Level? Is the segment descriptor located in the GDT or LDT? Calculate the address of the segment descriptor?	**5 marks**	CO5	Applying

620

6	Explain the terms DPL, RPL, CPL. What are the rules to transfer the control to a. other data segment b. Non-conforming code segment c. Conforming code segment	**5 marks**	CO5	Applying
7	Describe the significance of following fields in segment descriptor. 1. S Bit 2. Type field 3. G Bit, Limit Field 4. P Bit	**5 marks**	CO5	Understanding
8	Describe Call Gate Mechanism in detail with the help of a diagram.	**5 marks**	CO5	Understanding
9	Describe the structure of a task. List the registers and data structures that support task management.	**5 marks**	CO6	Understanding
10	List the various types of interrupts and exceptions. Provide three distinctions between exceptions and interrupts.	**5 marks**	CO6	Understanding

END OF QUESTION PAPER