Roll No. 1032210755

Department of Computer Engineering & Technology
T.Y.B.Tech.(CSE) (Academic Year 2023-24)
Mid Term Exam - Semester VI

Course Name:- High Performance Computing **Course Code:- CET3007B**

Maximum Marks: 15 **Time: 45 Minutes** **Date: 04/04/24**

Instructions:-

1. *Solve Q1 or Q2 and Q3 or Q4.*
2. *Figure to the right indicates full marks.*
3. *Use of cell phone is prohibited in the examination hall.*
4. *Neat diagrams must be drawn wherever necessary.*
5. *Assume suitable data, if necessary and clearly state.*
6. *Use of scientific calculator is allowed*

Q. 1 a. Explain Moore`s Law. Discuss the motivating factors for parallelism. **[4 Marks]**

b. With neat diagrams explain the typical SIMD and MIMD architectures **[4 Marks]**

OR

Q. 2 a. Define Speedup, Efficiency with equations. **[4 Marks]**

b. Write a note on Very Long Instruction Word processors with suitable example. **[4 Marks]**

Q. 3 a. Describe the following terms with respect to parallel algorithm design: **[4 Marks]**

(i) Decomposition
(ii) Dependency Graphs
(iii) Granularity
(iv) Concurrency

b Define **[3 Marks]**

(i) Critical Path Length
(ii) maximum degree of concurrency
(iii) average degree of concurrency.

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OR

Q. 4 a Discuss briefly following Parallel Algorithm Models: **[4 Marks]**

(i) The Data- Parallel Model

(ii) The Task Graph Model

(iii) The Work Pool Model

(iv) The Pipeline or Producer-Consumer Model

b What are mapping techniques for load balancing? **[3 Marks]**
Explain at least two mapping techniques.

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