Lab 4: BJT as a Voltage Amplifier: Common Emitter 60

Prerequisite:

You must have a working simulation and physical implementation of a waveform Function Generator that swings to both positive and negative voltages, as worked out in Lab 1 + 2. We call this the FG for short throughout the rest of this lab.
The official standardized design is published on moodle – use those component values to get a reliable output and test that your FG works as expected.
Settings for LTSpice: Use the following timing parameters in LTSpice simulation command

```
Stop time = 101m
Time to start saving data = 100m
Maximum time step = 0.01m
```

This skips the initial transients in the first 10ms of simulation caused by calculation artefacts, capacitive charging etc and gives you a stable picture of one full cycle of V_{in} @ $f \sim 1kHz$

Grand goal:

Design a BJT based circuit that is able to amplify a small AC input voltage to a large output Voltage. Current requirements are not very precisely defined, but the output must be able to function as a reasonably good AC voltage source (we will test in the end, how good is "reasonably" good)
By now, you must be familiar with the terms DC voltages and currents (constant in time, with capitals V,I); AC voltages and currents (v, i) and the concept of "sourcing" v/s "sinking" current at a circuit node.

Part 1) Circuit Design and Simulation

Fig 1 shows the basic structure of a voltage amplifier circuit. In principle, since $I_c = \beta I_B \rightarrow V_{out} = V_{CC} - I_c R_C$
But Fig 1 is just a 'conceptual skeleton circuit'.
Some important extra components are needed to put Q1 in the proper operating mode as in earlier Lab, AND ensure non-linear effects at B-E junction are suppressed .

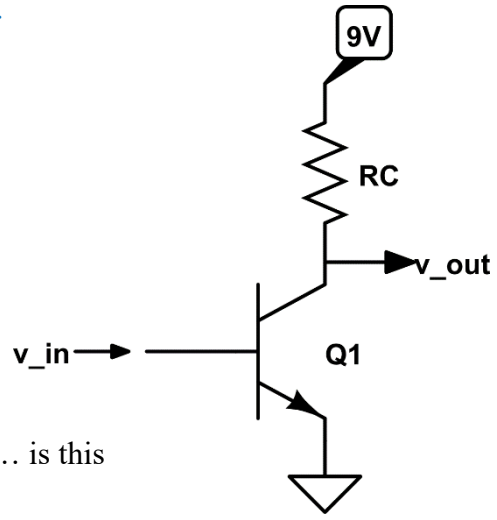


Fig 1:
The BJT voltage amplifier… is this all there is to it?

Level 0: The "crack"

If v_{in} is an AC voltage whose value can be both positive and negative,

0.1 What are the assumed conditions required for $i_c = \beta i_b$?
What are the necessary absolute and relative voltage conditions required at the C, B, E terminals of Q1 to use it as a voltage amplifier? **5**

PLEASE NOTE: A significant part of lab 1+2 was devoted to making a stable 8.3V (V_{CC}), So all further calculations are done taking $V_{CC} = 8.3V$ which is what is used for hardware.

1) Functional requirement: BJT must be forward biased for $i_c = \beta i_b$.

2) Safety requirements: I_{CE} must not exceed safety limit given in the data sheet. Also V_{EB} must not exceed the maximum reverse bias voltage limit. The absolute maximum safety ratings given below must not be exceeded. (we need not worry about V_{CE} and V_{CB} much because well beyond our power supply range.)

$$V_{\mathrm{CE}} < V_{\mathrm{CE|max}} = 45V$$
$$V_{\mathrm{CB}} < V_{\mathrm{CB|max}} = 50V$$
$$V_{\mathrm{EB}} < V_{\mathrm{EB|max}} = 6V\ (reverse\ bias\ breakdown)$$
$$I_c < I_{\mathrm{C\,|max}} = 200mA$$

3) The terminals of Q1 must satisfy the following voltages conditions:
General inequality: $V_C(= V_{\mathrm{CC}}) > V_B(V_{\mathrm{in}}) > V_E$
In active region $I_E \simeq I_C \gg I_B$
Thus, $V_{\mathrm{BE}} > 0.7V$ to maintain CB forward bias.
Thus, $V_{\mathrm{CB}} > 0.7V \rightarrow V_B < 7.6V$ to maintain CB reverse bias. (C is N and B is P)

0.2 Input side: Our input signal is a voltage: v_{in}, It is NOT a current i_{in}.
Is it OK to send v_{in} directly into the base of Q1? Explain with equations why it's not OK to apply v_{in} directly to Q1-B. This will guide you to figuring out what set of components have to put in between v_{in} and Q1-base terminal **5**

No v_{in} should not be directly applied to the base of the transistor because:
1) When v_{in} drops below 0.7V, $V_{\mathrm{BE}} < 0.7V$ hence the BE terminal is reverse biased and the transistor is no more in the active region.
2) Thus, amplification doesn't occur for the negative half cycle and the positive voltages below 0.7V.

3) Even for positive values of v_{in} the Q-point is unstable and the transistor is on the verge of saturation whenever $v_{in} > 0.7V$. This would drive huge collector current which might damage the transistor.
4) Hence, for majority of the time the transistor is not doing any amplification.
5) For the grounded emitter configuration:
$V_E = 0 \rightarrow V_{BE} = v_{in}$. $V_{CC} - I_C R_C = V_C$.

Also, the absence of an emitter resistor and base biasing resistors means that the I_C is highly unstable due to temperature effects on the diode junction.

Level 1: Basic Design

After cracking the concepts in Level 0, and with experience from previous circuit design, you should already have a rough idea how to proceed:

The design parameters we wish to achieve in this lab's circuit design are:

1. Assume V_{CC} = 9V constant, and Q1 β = 300
2. Use I_Q = 1mA
3. Circuit gain = **–10** (note '–' due to overall design)
4. Amplifier has a high-pass f_{3dB} = 100 Hz
5. Test amplifier with v_{in} = ± 0.3V @ 1.17 kHz (our standard FG output)

Here is the step-by-step design procedure:

BJT terminal voltages must be setup such that it always remains in the forward-active operation mode. Here are ways in which this can be accomplished, without too much complexity:

PLEASE NOTE: A significant part of lab 1+2 was devoted to making a stable 8.3V (V_{CC}), So all further calculations are done taking $V_{CC} = 8.3V$ which is what is used for hardware.

DC Design:

1) Choice of I_Q = 1mA [given]

Note that we have chosen I_Q much lower than the Q point of the emitter follower current amplifier – we are mostly interested here in voltage amplification and not too bothered about delivering large current to the load. In the first approximation, we don't deliver *any* current to the DSO probe load. So a choice of low I_Q is OK as long as we can ensure the BJT remains forward-active at all times.

2) **Calculation of R_C** – we would like to allow v_{out} to have maximum possible

range from 0 – V_{CC}. So, we would like to set V_C at about ½ V_{CC}. Fixing V_C and I_Q immediately determines R_C. What value of R_C do you choose? **2**

$$V_C = \frac{V_{CC}}{2} = (V_{CC} - I_C R_C) \rightarrow R_C = \frac{4.15V}{1mA} = 4.15k\Omega$$

In practice we can use $2k\Omega + 2.2k\Omega$.

3) Is it OK to connect Q1-E terminal directly to GND as shown in Fig 1? Why not? Explain what type of non-linearity is expected if Q1-E is at GND. **2**

No, it is not OK to do so because of the following reasons:

1) Non-Linearity: The emitter voltage oscillates (about $V_{EQ} + v_{in}$) due to the AC input at base, thus generating the AC output current required.

The effective voltage gain is $G_v = -\frac{R_C}{r_e} = -\frac{R_C I_C(mA)}{25mV}$

which is dependent on the collector current. So, for a quiescent current of 1mA the gain is -400 but I_C isn't constant and it varies as the output signal varies, so the gain is not at all stable. The amplifier has a lot of distortion or poor linearity. Given below is a graph from the book "The Art of Electronics" showing the non-linearities observed:

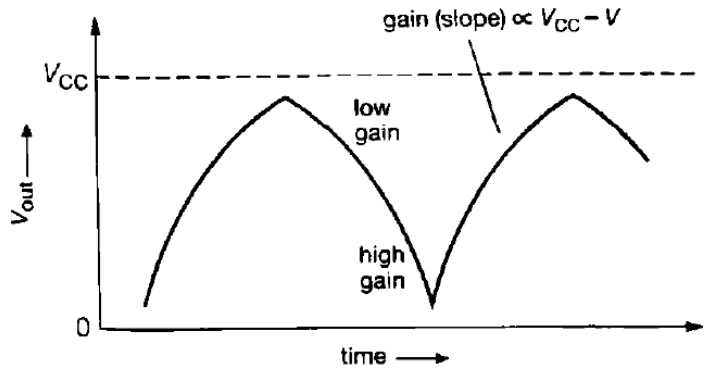


Figure 2.45. Nonlinear output waveform from grounded-emitter amplifier.

The non-linearity is estimation is as follows:

$$G_v = -\frac{R_C}{r_e} = \frac{-I_C R_C}{V_T} = -\frac{V_{drop}}{V_T}$$

Then non-linearity $\frac{\Delta G_v}{G_v} \simeq \left(\frac{\Delta V_{out}}{V_{drop}}\right)\left(\frac{V_T}{V_T + I_E R_E}\right)$

4) 2) V_{BE} is ~ 0.7V in forward active mode. So V_E should be at least of comparable value at the Q-point to ensure thermal stability.
Explain what is the Q-point value of V_E required, and what is the component value required at E? [ref: Horowitz, Chap. 2] **2**

The goal is to set a stable DC emitter voltage and to reduce the dependence of the voltage gain on collector current. This is done using an emitter resistor whose value is set according to the desired current value and voltage gain value.

With R_E the voltage gain is: $G_v = -\frac{R_C}{r_e+R_E}$. The non-linearities due to $r_e = \frac{25mV}{I_C(mA)}$ are reduced by $\frac{r_e}{R_E+r_e}$.

Given: expected $A_v = -10 \rightarrow R_E = \frac{R_C}{10} - r_e = \frac{4150\Omega}{10} - \frac{25mV}{1mA} = 390\Omega$

$$\therefore V_{EQ} = I_C R_C = 0.39V$$

In practice we can use $330\Omega + 68\Omega$

Finer points of choosing V_{EQ}: **2**

Setting V_E to be $0.1V_{CC}$ directly, you will find that you don't get to gain G= – 10 in step 5 below. So you can come back here to re-do the V_{EQ} setting to lower than $0.1V_{CC}$ (while still having $\frac{V_E}{I_E}$ dominate over r_e) – Design is an iterative process!

Let, $V_E = fV_{CC}$ where $0 < f < 0.5$. For such a setting we would have: $(I_C \simeq I_E)$

$$G_v = \frac{-R_C}{\frac{V_E}{I_E} + r_e} = -\frac{R_C I_C}{fV_{CC} + 25mV}$$

The above expression helps set up an iterative process to adjust f such that we preserve the gain G_v.

5) Setting V_B: Once DC values of V_C and V_E are decided in steps above, choose the simplest method of setting V_B (similar considerations as used in earlier current amplifier lab apply, to make sure the biasing network provides a much lower impedance path to ground than R_B.

List the values of components used to set V_B here: **2**

The V_{EQ} calculated is 0.39V. Hence the DC base voltage V_{BQ} should be $V_{EQ} + 0.7V$=1.09V.

To achieve this, we set up a voltage divider using resistors R_{B1} and R_{B2} as follows: $V_{BQ} = V_{CC}\left(\frac{R_{B2}}{R_{B1}+R_{B2}}\right) \rightarrow \frac{R_{B1}}{R_{B2}} = \frac{8.3V}{1.09V} - 1 = 6.61$

Choice of resistors: $R_{B1} = 68k\Omega \; and \; R_{B2} = 10k\Omega$

6) What AC voltage gain do you get?

Combining the answers to questions 2 & 3 calculate the AC voltage gain of the circuit designed thus far.

Note: Though we are technically in the DC design phase, we are looking ahead and interested in the AC voltage gain. So turn all the capital letter quantities V…, I… into small case and do a little bit of math with the AC terms $v_{in}=v_B$, $v_C=v_{out}$, i_C, i_E, i_B.

The main steps involve using the fact that

$v_{out} = v_C = -i_C R_C$ (V_{CC} is DC value drops out) and $r_e \ll R_E$ by design

$v_B = v_E$ since $V_{BE} = 0.7V$ is fixed by the DC design.

You may find, surprisingly, that β is not involved in the final voltage gain of this circuit! **5**

r_e varies but here we consider the mean value $r_e = \frac{25mV}{<I_C>} = \frac{25mV}{1mA} = 25\Omega$

$$v_{out} = -i_c R_C$$
$$v_{in} = i_e(R_E + r_e) \simeq i_c(R_E + r_e)$$
$$\therefore G_v = \frac{v_{out}}{v_{in}} = -\frac{R_C}{R_E + r_e} \rightarrow A_v = -\frac{4150}{390 + 25} = -10$$

G_v is independent of β and also has reduced dependance on I_C

AC Design:

1) Input side: In general $V_{in} = V_{in|dc} + v_{in}$. We want to strictly reject $V_{in|dc}$ hence the 100Hz f_{3dB} high pass filter at the input is required. Calculate the value of the required component. The calculation is similar to the way we used R_{inp} of the amplifier as part of the CR high-pass filter in earlier lab **2**

Similar to the method followed in the previous lab, we add a capacitor to make a high pass filter with $f_{3dB} = 100Hz$ at the input side.

$$f_{3dB} = 100Hz = \frac{1}{2\pi R_{inp} C_I} \rightarrow C_I = \frac{1}{2\pi R_{inp} \cdot 100Hz}$$

Where the total input impedance:

$$R_{inp} = R_{B1}||R_{B2}||\beta(R_E + r_e) = 10k\Omega||68k\Omega||300(415\Omega) = 8.15k\Omega$$
$$\therefore C_I = \frac{1}{2\pi \cdot 8.15k\Omega \cdot 100\text{Hz}} = 195.4nF$$

We can use $200nF = 100nF||100nF$ during circuit design.

2) Output side: $V_{out} = V_{CC} - I_C R_C$ we are interested in only amplifying the AC component of $I_C = I_Q + i_C$ In fact, we want to *block* any DC share of the current flowing through R_C getting diverted to the load – this will disturb our DC calculations above!

Calculate the filter components required at the output before connecting to v_{out} What is the corresponding R required for this filter calculation? Recall from the reading notes that looking back Q1's C, the CB junction is effectively open circuit (MΩ) and there is only one other resistor at that junction! **2**

A high pass filter at the output does the job since the DC voltages can be considered to be a 0Hz waveform. The same $f_{3dB} = 100Hz$ which was used for the input can be used here since it would block DC. The high pass capacitor would be C_O(output side capacitor) parallel to the collector resistor. Note: R_{out} is only the collector resistor because the reverse biased CB terminal offers infinite resistance.

$$\therefore C_O = \frac{1}{2\pi R_C \cdot 100Hz} = \frac{1}{2\pi \cdot 4150\Omega \cdot 100Hz} \simeq 384nF$$

Here, 330nF from the kit can be used.

Go back and check: you may now realize that as long as you keep Q1 in forward-active mode, some I_Q and hence a DC $I_B = I_Q/\beta$ is required. Since I_Q has been set very low, corresponding DC I_B must be really small indeed! This means you must obey the constraint $(R_{B1}||R_{B2}) \ll R_B$ much more strictly to make sure most of the DC current in the biasing path is preferentially sent into the biasing network and *not* into the base of Q1. Re-check your answers to question 4) in the DC design above for the biasing network to set V_B to make sure your design is self-consistent in terms of all the DC values and the design gain G is achieved.

1

We have worked out $R_{B2} = 10k\Omega \; and \; R_{B1} = 68k\Omega. \rightarrow R_{B1}||R_{B2} = 8.72k\Omega.$

$$R_B = \beta(r_e + R_E) = 300(415)\Omega = 124.5k\Omega \gg R_{B1}||R_{B2}$$

Thus, the expected inequality holds.

Level 3: Advanced Design check **5**

Is the gain constant over the full span of $v_{in} = \pm 0.3V$?

We have designed for a gain of G= –10 at the Q-point. But as v_{in} varies i_C varies around I_{CQ} *and hence* r_e *also changes.* Have you chosen your component values conservatively enough that for the given design parameters, $G = -10$ is constant?

What we need for a stable enough voltage gain $G_v = -10$:
1) Small enough i_b. Nearly all AC input current must flow through $R_{B1}||R_{B2}$.
2) Changes in $r_e \ll R_E$. This will keep G_v relatively stable.

Given v_{in} oscillates between $\pm 0.3V$. We know that $i_b = \frac{v_{in}}{R_B}$

$$\therefore |i_b| \leq \frac{0.3V}{R_B} = \frac{0.3V}{124.5k\Omega} = 2.4\mu A$$

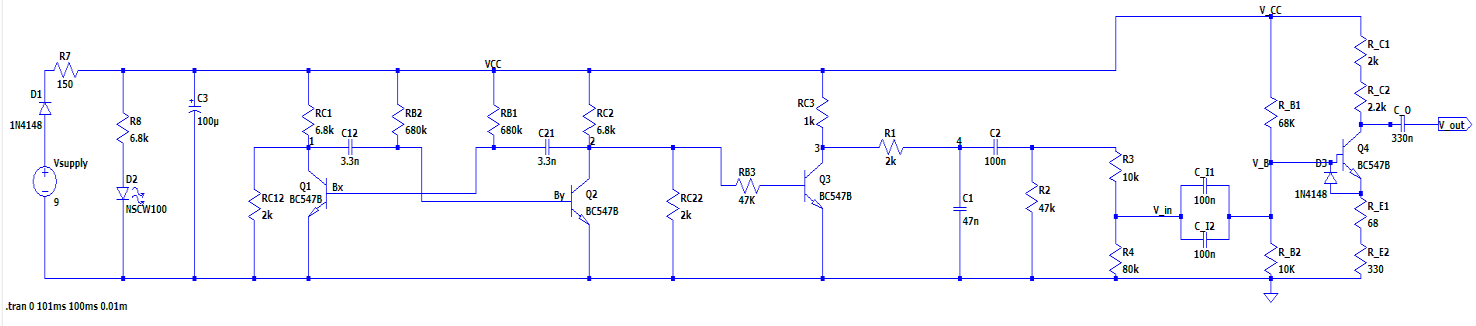
Thus, for the AC collector current: $|i_c| = \beta|i_b| \leq 300 \cdot 2.4\mu A = 0.72mA$.
The total collector current varies between $1 - 0.72 = 0.28mA$ *and* $1 + 0.72 = 1.72mA$.
Which means $R_E + r_e = R_E + \frac{25mV}{I_C}$ varies from $\simeq 405\Omega$ *to* $\simeq 470\Omega$
Thus $G_v = -\frac{R_C}{R_E + r_e}$ varies between -8.82 to -10.24 which is within acceptable bounds.

Level 4: Simulate in LTSpice and plot 30

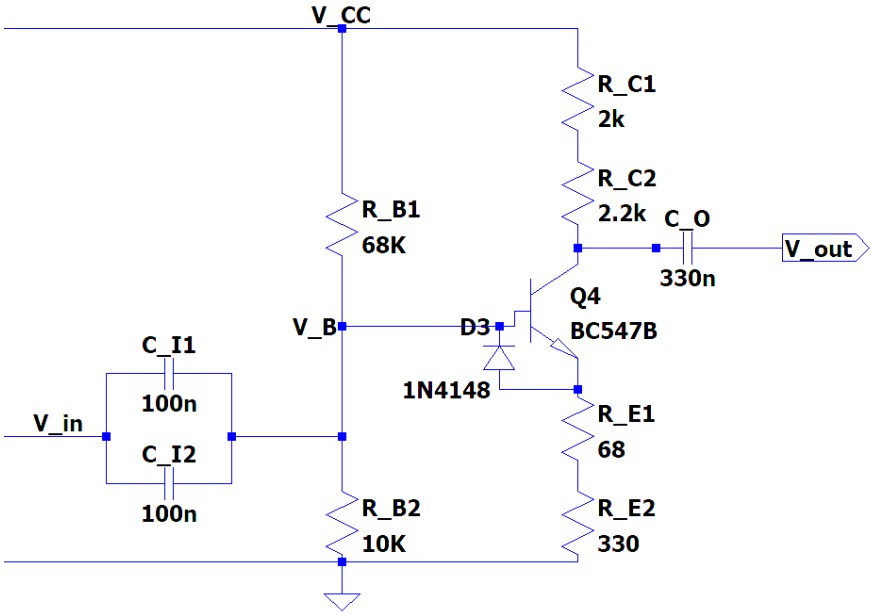
Simulate the complete circuit as designed above in LTSpice and check its performance as per the design parameters
(*v_{in} = ±0.3V, f=1.17kHz, Gain = –10*)
Put your LTSpice circuit diagram and simulation result plots below.
Make sure to plot voltages as a function of time (as you will check them after building the circuit). Also, plot voltages *v_{out} v/s v_{in}* to check the Gain linearity and any peculiar features.

LTSpice design **5 marks**
Voltage amplification as function of time **10 marks**
V_{out} v/s V_{in} to check for linear gain, and explain any peculiar features observed with your choice of circuit component values **15 marks**

LTSpice design:

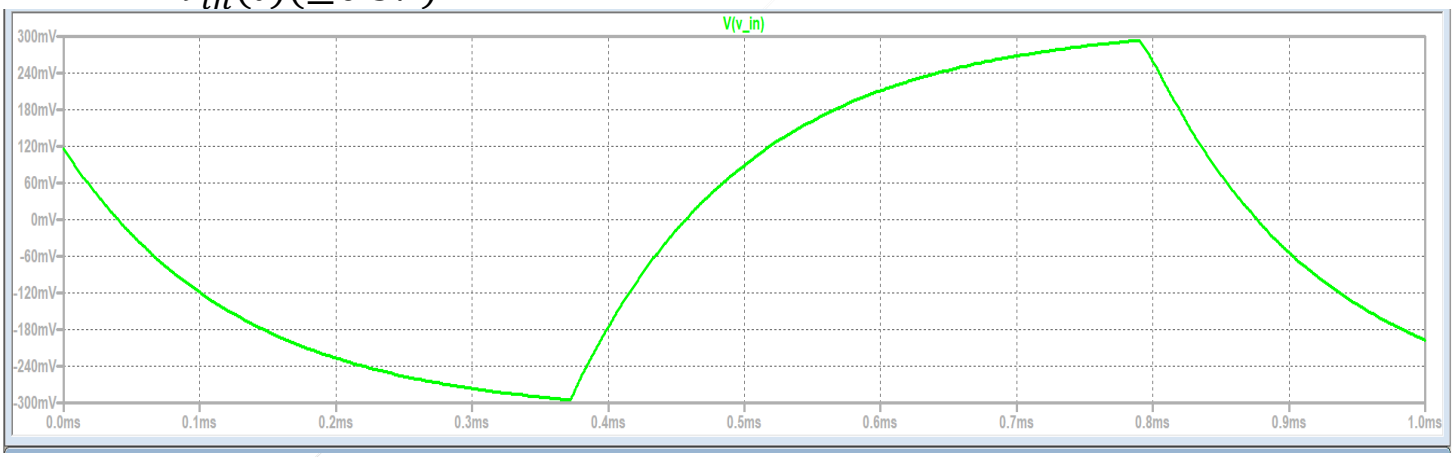


CE Amplifier: (voltage amplification)

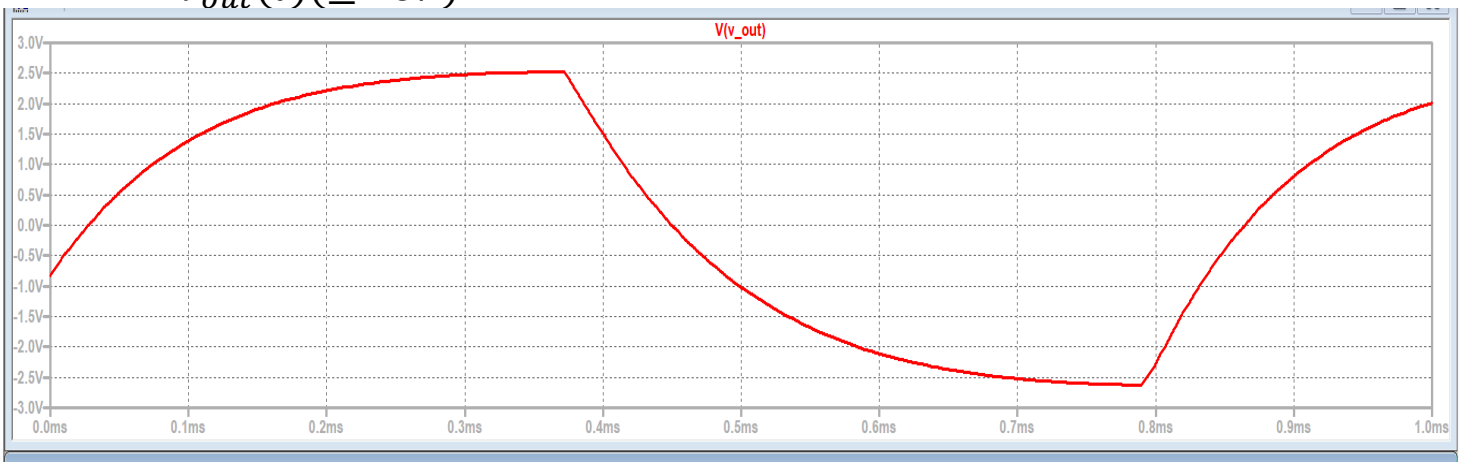


v_{in} *and* v_{out} plots in LTSpice:

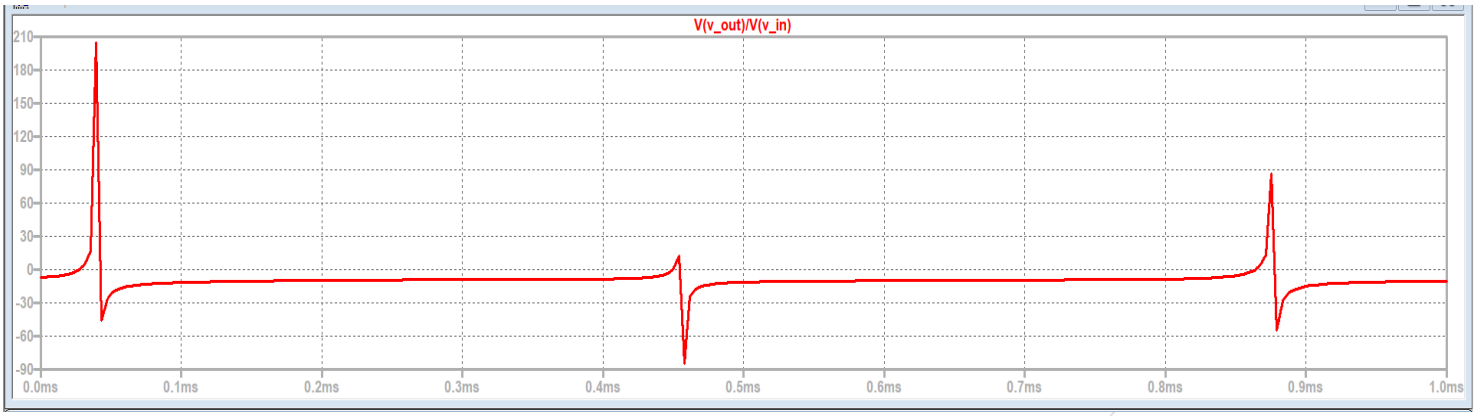
Observed $v_{in}(t)(\pm 0.3V)$



Observed $v_{out}(t)(\pm 2.6V)$

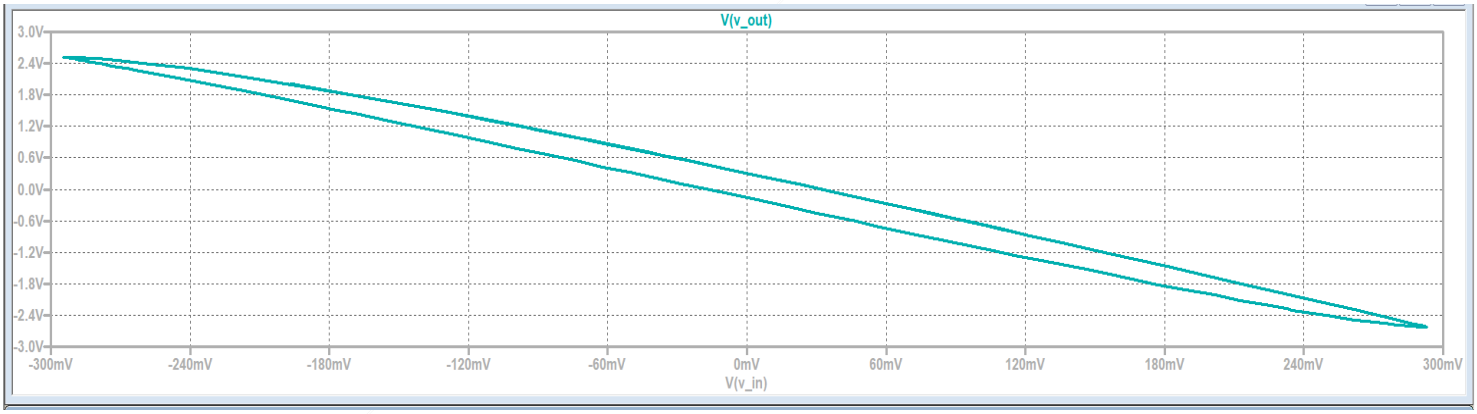


$G_v(t) = \frac{v_{out}}{v_{in}}$ (value attained in steady region$\simeq -10$)



The sudden peaks/valleys observed in the above graph occur when $v_{in} \to 0V$. The phase difference between v_{in} *and* v_{out} is not exactly 180˚ (apart from this slight phse lag is there due to filters) and the relationship is also not exactly linear. (External noise ensures that v_{in} is never exactly 0V)

v_{out} vs v_{in}



The above graph shows hysteresis i.e., as we increase/decrease v_{in} the decrease/increase (out of phase) in v_{out} is not instantaneous. This lag is due to capacitive effects of the diode depletion region. The ideal approximation assumes an abrupt depletion layer which in not the case in reality thus the lag (hysteresis effect) is observed.