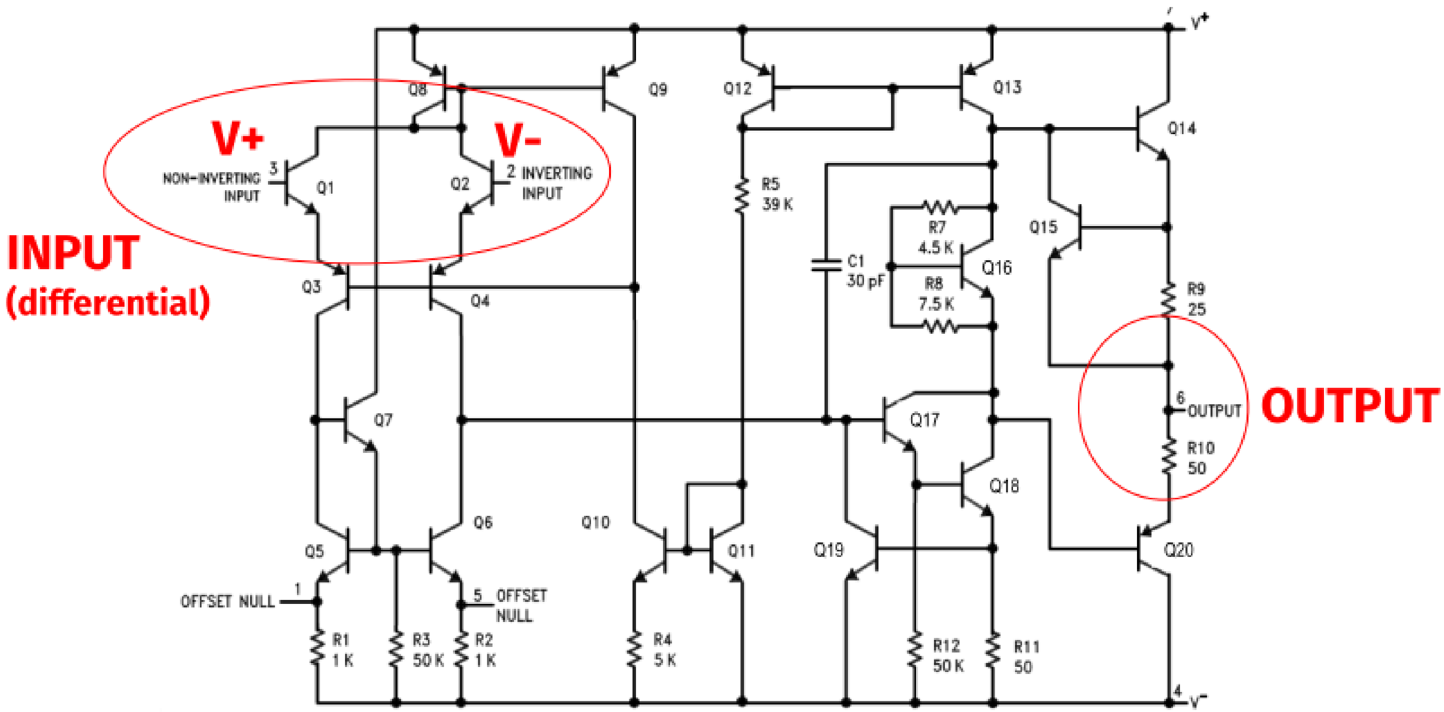
Lab Assignment 1: Reverse engineer the design of an opamp LM741

All question material is in blue. Please put your answers in black color font



The above diagram, taken from the datasheet of the LM741 opamp IC shows the internal functional block diagram of the IC as discussed in Session 1

An opamp is a three terminal device – the generic LTSpice symbol for an opamp, and its basic governing equation is shown in Fig 2

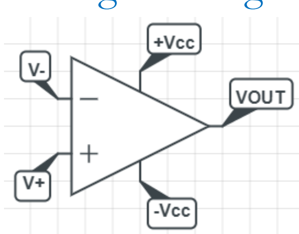


Fig 2: The opamp abstract model

$$VOUT = A_0 * (V_+ - V_-) \quad with\ open\ loop\ gain\ A_o \to \infty$$

At this point, we *don't* want to think of any feedback connections. Our objective is to figure what the integrated circuit of Fig 1 is doing, when packed into the tiny triangle of Fig 2

Answer the following questions:

Question 1: Identify the function of transistors Q1 – Q20 20

There are 20 transistors shown in Fig 1. Some are NPN, some PNP. Many seem to be configured in pairs.

Identify the function performed by each of these transistors. Many of the transistors are connected to work in pairs. For each transistor or pair of transistors, you must identify:

a) What is its functional role?
b) What is the use of that function in the overall circuit?

For example, it was discussed briefly in the session that Q10+Q11 function as a current mirror: your answer must indicate what is the use of the current set by this current mirror?

Merge row-wise cells in the following table as required for pairs of transistors (select the table cells, right-click and 'merge cells' as has been done already for Q10+Q11 below) You may need to re-order some of the cells (for example Q14+Q20 seem to go together!

<table>
<tr><th>BJT</th><th colspan="2">… is a</th><th>… this is the use</th></tr>
<tr><td>Q1</td><td rowspan="4">High input impedance Differential amplifier.</td><td rowspan="2">NPN transistors, connected as Emitter Followers.</td><td rowspan="2">Provides high input impedance, with virtually 0 current input to the Op-Amp.</td></tr>
<tr><td>Q2</td></tr>
<tr><td>Q3</td><td rowspan="2">Form common base PNP Differential pair.</td><td rowspan="2">Eliminate Miller effect.
Provide DC level shifting and prevent EB junction breakdown in Q1 and Q2.</td></tr>
<tr><td>Q4</td></tr>
<tr><td>Q5</td><td colspan="2" rowspan="3">Active load to the Input stage Diff-Amp. They form a modified 3-terminal Wilson current mirror.</td><td rowspan="3">High impedance active load (Q7, Q6, Q5, R1, R2, R3).
Its role is to convert the (differential) input current signal to a single-ended signal without the attendant 50% losses (increasing the op amp's open-loop gain by 3 dB).</td></tr>
<tr><td>Q6</td></tr>
<tr><td>Q7</td></tr>
<tr><td>Q8</td><td rowspan="2">Current Mirror.</td><td rowspan="6">The network of the current mirrors across the 3 stages {1) input, 2) high gain stage, 3) output} plays a crucial role in maintaining stable Q-point biasing currents across these stages.</td><td rowspan="2">Sets the Q-point base currents for the common base pair Q3, Q4.</td></tr>
<tr><td>Q9</td></tr>
<tr><td>Q10</td><td rowspan="2">Current Mirror. (Widlar current mirror)</td><td rowspan="2">The output part (Q10) of Q10-Q11 current mirror keeps up the common current through Q9/Q8 constant in spite of varying voltage</td></tr>
<tr><td>Q11</td></tr>
<tr><td>Q12</td><td rowspan="2">Current Mirror.</td><td rowspan="2">Current source, active load to Q17.
This acts as a high impedance collector load the Q17, Q18 Darlington pair.
This helps provide high gain.</td></tr>
<tr><td>Q13</td></tr>
<tr><td>Q19</td><td colspan="2">Current regulator (/limiter).</td><td>The transistor Q19 prevents this stage from delivering excessive current to Q20 and thus limits the output sink</td></tr>
</table>

<table>
<tr><td></td><td colspan="2"></td><td>current.
Q19 senses the voltage across Q18's emitter resistor (R11-50 Ω); as it turns on, it diminishes the drive current to Q17 base.</td></tr>
<tr><td>Q15</td><td colspan="2">Current Regulator (/limiter).</td><td>The 25 Ω resistor at the Q14 emitter, along with Q15, acts to limit Q14 current to about 25 mA; otherwise, Q15 conducts no current.</td></tr>
<tr><td>Q16</td><td colspan="2">Voltage level shifter</td><td>Is a high input impedance current Amp whose output is delivered to Q17. It provides the quiescent current for the output transistors Q14 and Q20.</td></tr>
<tr><td>Q17</td><td rowspan="2">Darlington pair.
High gain class-A voltage amp.</td><td>Emitter Follower.</td><td rowspan="2">Amplifier with high gain. The output from the differential stage (collector of Q6) is amplified. The amplified voltage of this stage is the input to the final class-AB buffer.</td></tr>
<tr><td>Q18</td><td>Common Emitter voltage amp.</td></tr>
<tr><td>Q14</td><td rowspan="2" colspan="2">Class AB type buffer. (Push-Pull Amp) Each of them is connected as emitter follower.</td><td rowspan="2">This stage acts like a buffer:
Provides low output impedance and good current driving capabilities. High efficiency with low distortion.</td></tr>
<tr><td>Q20</td></tr>
</table>

Question 2: Voltage or Current output? 1

Is the output from the opamp a Voltage or Current output?

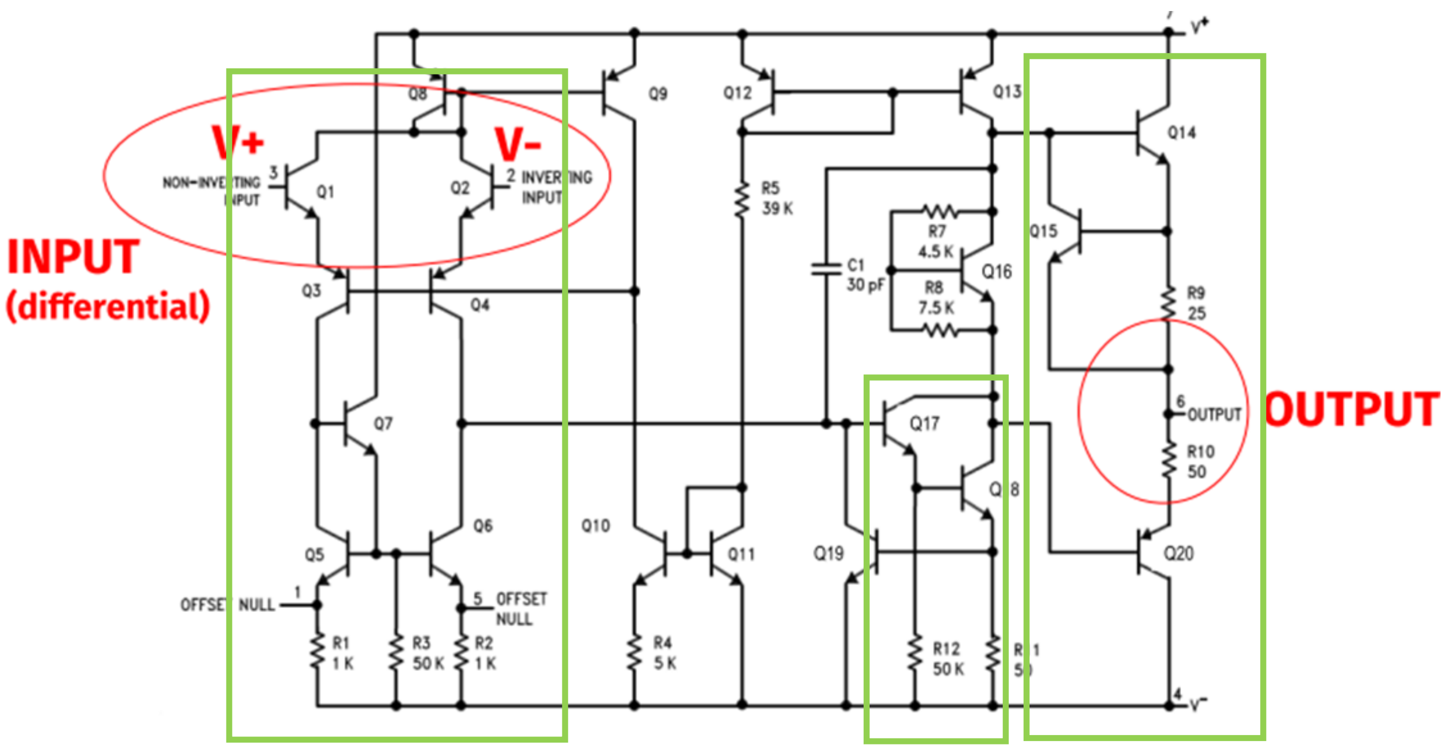
A good answer to this question would evaluate (qualitatively, if not exactly) the output impedance of the circuit and accordingly match it to the properties of a voltage source or a current source.

Answer: The output from the op-amp is a voltage output. Qualitatively one can reason why this should be the case by looking at the working of the three main stages: 1) Input stage, 2) Intermediate high gain stage and 3) Class-AB output buffer. The input stage and the high gain stage combined lead to extremely high input impedance (of the net circuit) and **the output stage has a low output impedance. This is the characteristic of a Voltage source.** Here, one can consider the whole circuit as black box where effective R_{in} is very large and R_{out} is tiny. Looking at the circuit stage-3 R_{out} is 50Ω in parallel to other larger resistors, thus $\boldsymbol{R_{out} \sim 50\Omega}$.

Question 3: How does $VOUT = A_0 * (V_+ - V_-)$ happen? 5

Following the signal flow from left to right in the circuit of Fig 1, explain qualitatively, how the circuit design ensures the open loop gain A_O is essentially infinite.
Don't take into account any of the passive resistor values or try to get a numerical estimate of A_O - the amazing thing about opamps is that *by definition*, $VOUT = A_0 * (V_+ - V_-)$ for *all* opamps

Answer:



The net open-loop small-signal voltage gain of the op amp involves the product of the current gain h_{fe} of some 4 transistors. In practice, the voltage gain for a typical 741-style op amp is of order 200,000, and the current gain, the ratio of input impedance (~2−6 MΩ) to output impedance (~50 Ω) provides yet more (power) gain.
To get a qualitative idea about why this is so one can look at the three main stages individually:

1) Stage-1 (input): This stage amplifies the differential input $(v_+ - v_-)$. The gain $\sim \frac{R_C}{R_E}$ but here, both the collector resistor and the emitter resistors are active loads. Even then the current mirror provides very high input impedance and hence $v_{out1} = A_1(v_+ - v_-) \sim \frac{R_C}{R_E}(v_+ - v_-) \sim 10^2(v_+ - v_-)$
2) Stage-2 (high gain intermediate stage): Amplified voltage of the diff-amp: $A_1(v_+ - v_-)$ is further amplified here. The gain is very high, of the order of β^2, thus $A_2 \sim 10^4$.
3) Stage-3 (buffer): This stage has unity voltage gain.

Thus, a very rough estimate of $A_o \sim A_1 A_2 \sim 10^6$. With $v_{out} = A_o(v_+ - v_-)$