Lab 3: BJT Emitter Follower : Part 2 [100]

Prerequisite:

You must have a working simulation and physical implementation of a waveform **F**unction **G**enerator that swings to both positive and negative voltages, as worked out in Lab 1 + 2. We call this the FG for short throughout the rest of this lab.
The official standardized design is published on moodle – use those component values to get a reliable output and test that your FG works as expected.
Settings for LTSpice: Use the following timing parameters in LTSpice simulation command

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Stop time = 101m
Time to start saving data = 100m
Maximum time step = 0.01m
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This skips the initial transients in the first 10ms of simulation caused by calculation artefacts, capacitive charging etc and gives you a stable picture of one full cycle of V_{in} @ $f \sim 1kHz$

Grand goal:

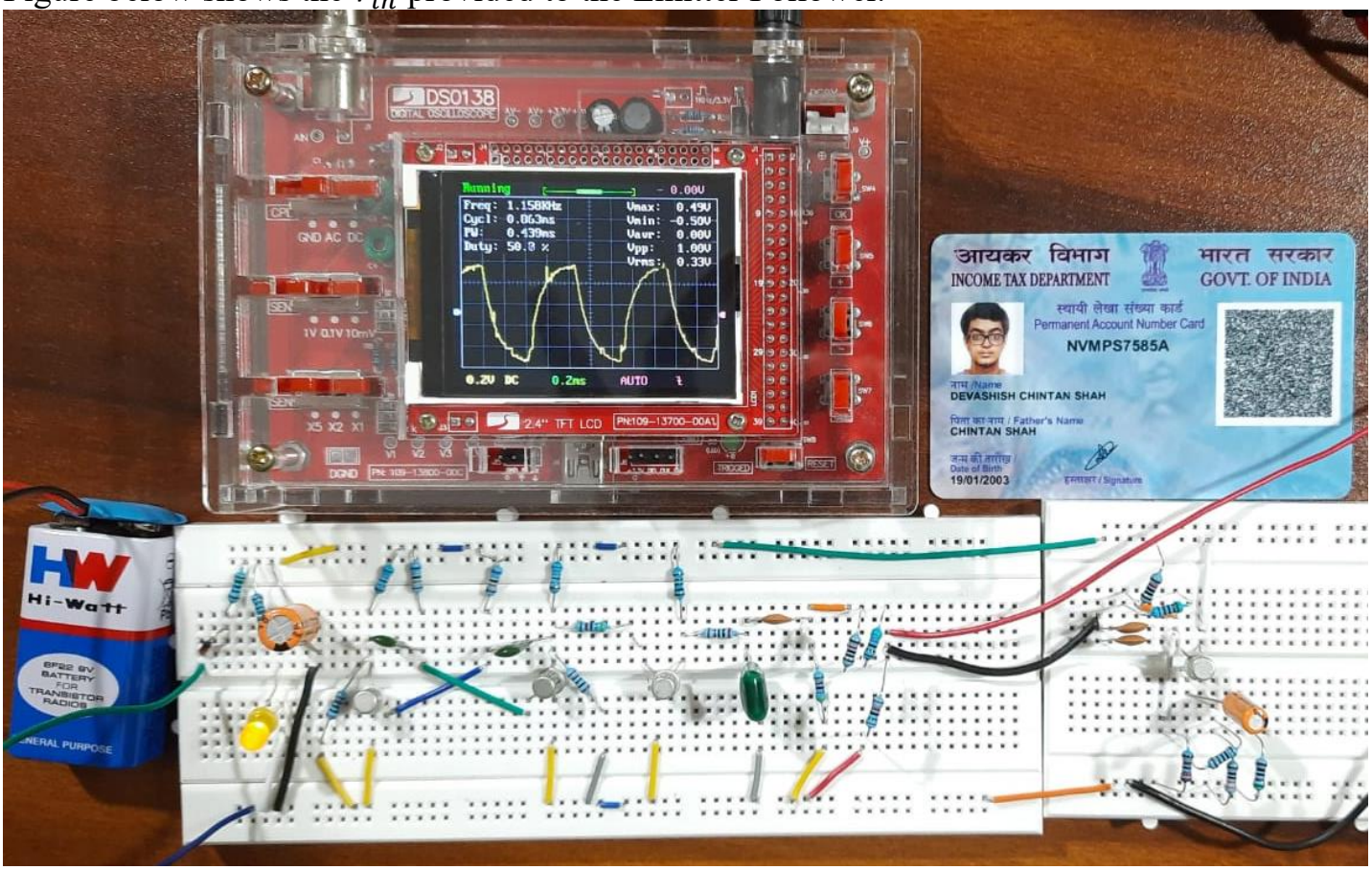
Design a BJT based circuit that has no voltage gain, but is able to amplify a small input current to a large output current. In terms of impedance, it means that the final circuit design must have very high input impedance and very low output impedance. This is very attractive for practical applications, since most electro-mechanical devices are driven by current.
Note about terminology of 'current' used in this assignment:

1) We consider the traditional Kirchoff's Law current *I* in the circuit design and analysis. This current can be flowing in either direction across two nodes in a circuit. Though as explained in the introduction session, inside an NPN/PNP transistor, the current *I* flows exclusively from the Collector to the Emitter.
2) The term AC current used here refers to a time-varying current, and is denoted in small case *i*. In contrast, a DC current denoted by capital letter *I* is one whose value remains constant with time. Generalizing, a DC voltage is one which is constant in time (like the 9V supply to your circuit), and an AC voltage is one which varies as a function of time, like the output of your FG.
3) If V_{out} is supplying current to the load, we say the circuit is 'sourcing current'. Vice-versa, if current is being pulled *into* the circuit from the load, we say the circuit is 'sinking current'

Level 2.A: Circuit Demo 30

Build the circuit as designed and simulated in Level 1.
Use the FG as per standard design built earlier to provide V_{in} to your amplifier circuit..
Before connecting V_{in} and poking around with the DSO, follow the usual debugging steps: check DC voltage values at each significant node of the circuit to make sure they match the simulation and your circuit is wired up correctly. It's a good idea to explicitly write them down, since variations caused by component value tolerances may affect performance.
Connect V_{in} and probe the voltage across R_L. Provide photos of your full setup with ID card in the frame as usual.
Show by numerical calculation that measured voltage across R_L divided by R_L gives the current $I(R_L)$. Does it match the simulations done in Part 1?

Figure below shows the V_{in} provided to the Emitter Follower.



The observation matches the simulation with $V_{in|peak-peak} = 1V(\pm 0.5V)$.

The nature of the waveform also matches the simulation with symmetrical 50% duty cycle ($V_{avg} = 0$)

The frequency is as expected $\simeq 1.16kHz$

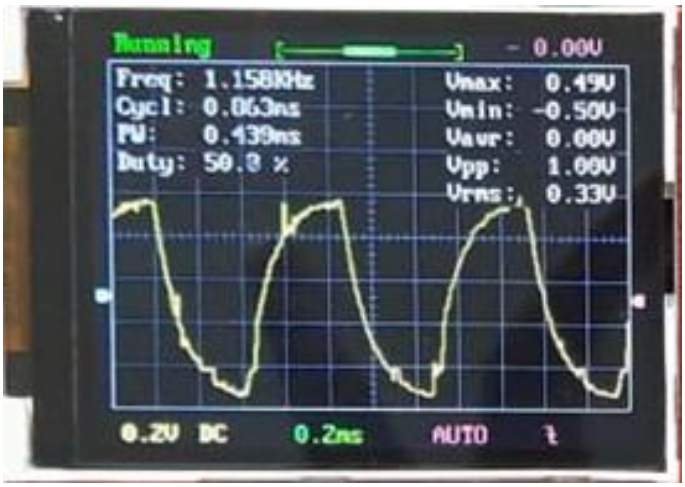
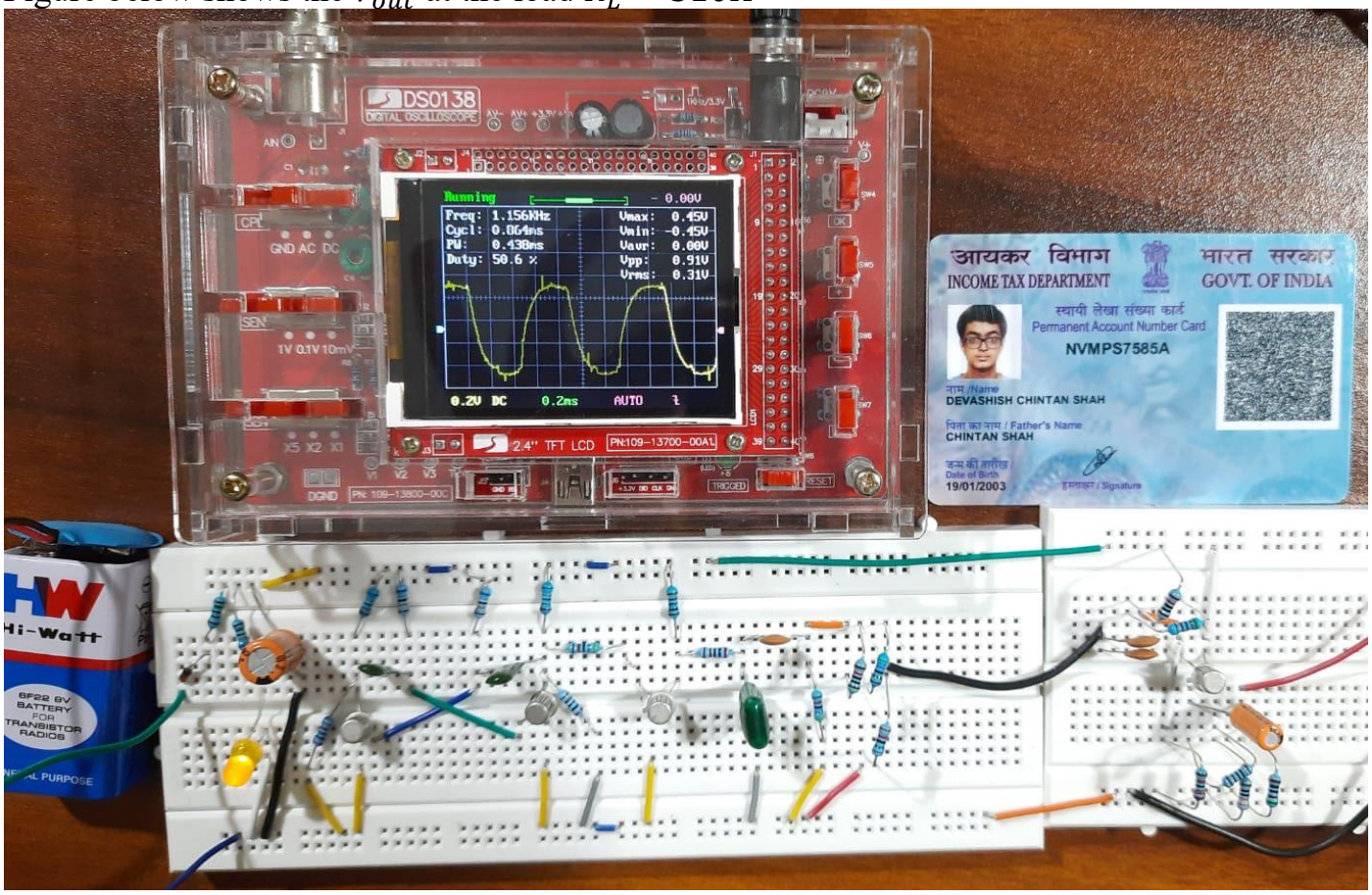
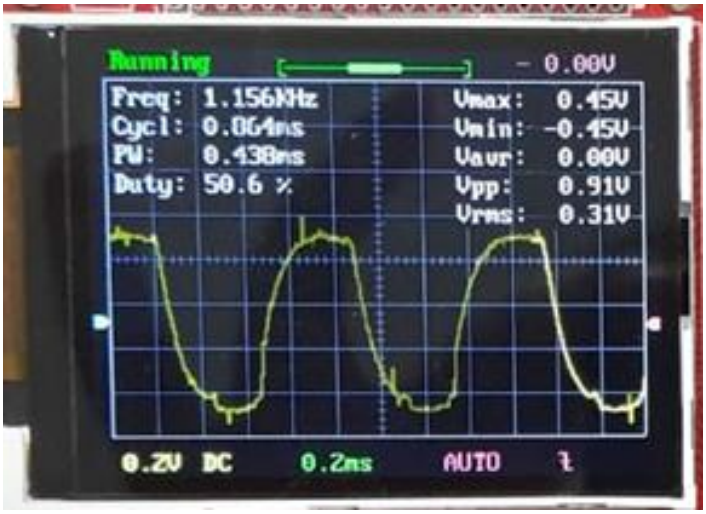


Figure below shows the V_{out} at the load $R_L = 510\Omega$



The peak value is nearly the same as that obtained through simulations. $V_{out|peak-peak} = 900mV(\pm 0.450mV)$.



The nature of the waveform is also as expected with rather rounded peaks compared to V_{in} due to the non-linearities discussed earlier.

$$I_{out|peak-peak} = \frac{V_{out|peak-peak}}{R_L} = \frac{900mV}{500\Omega}$$

$\therefore I_{L|peak-peak} = 1.8mA\ (\pm 0.9mA)$. This is in close agreement with the simulated result of 1.72mA peak-peak value.

Based on your measurements, determine the current gain $\frac{I_L}{I_{in}}$ actually achieved in your circuit. Is it symmetrical for both polarities of V_{in}?

We have the following peak-peak values for the input and output currents:
$(R_{inp} = 7.88k\Omega\ as\ calculated\ in\ part-1)$

$$I_{in|peak-peak} = \frac{V_{in|peak-peak}}{R_{inp}} = \frac{1V}{7.88k\Omega} = 127\mu A$$

$$I_{L|peak-peak} = \frac{V_{out|peak-peak}}{R_L} = \frac{900mV}{500\Omega} = 1.8mA$$

Current Gain: $\frac{I_{L|peak-peak}}{I_{in|peak-peak}} = 14.2$

This is in very close agreement with the simulated result of 14.82 from part-1
Yes, $I_L \propto V_{out}$ is symmetrical for both polarities of V_{in}.

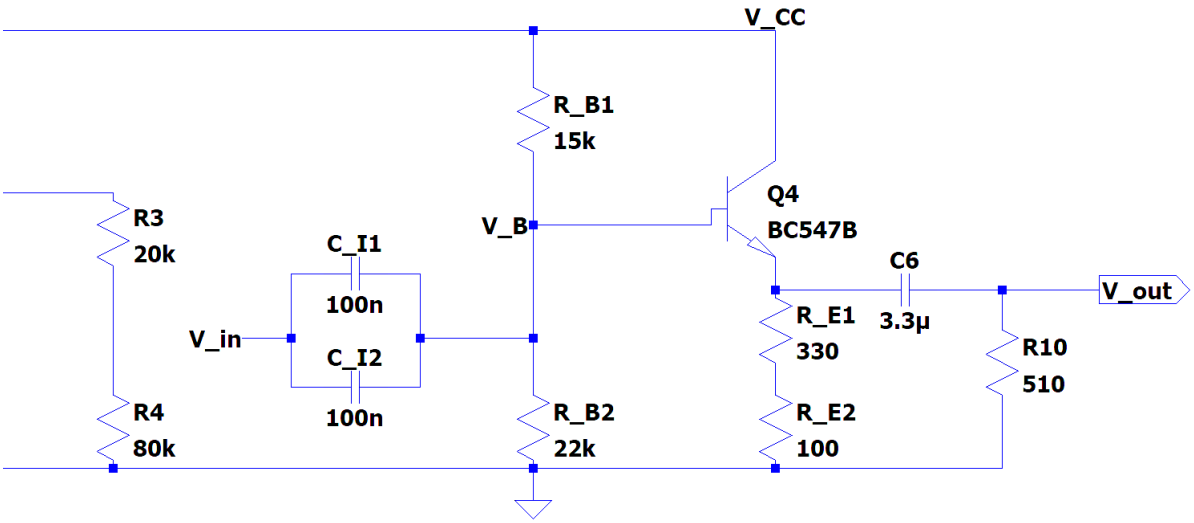
Level 2.B: Power analysis 30

For the following analysis, it is adequate to consider the peak power consumption. RMS power formulae are applied for sinusoidal waveforms, but our test waveform is *not* a sinusoid. So, you may simply take V*I products at the peak values.

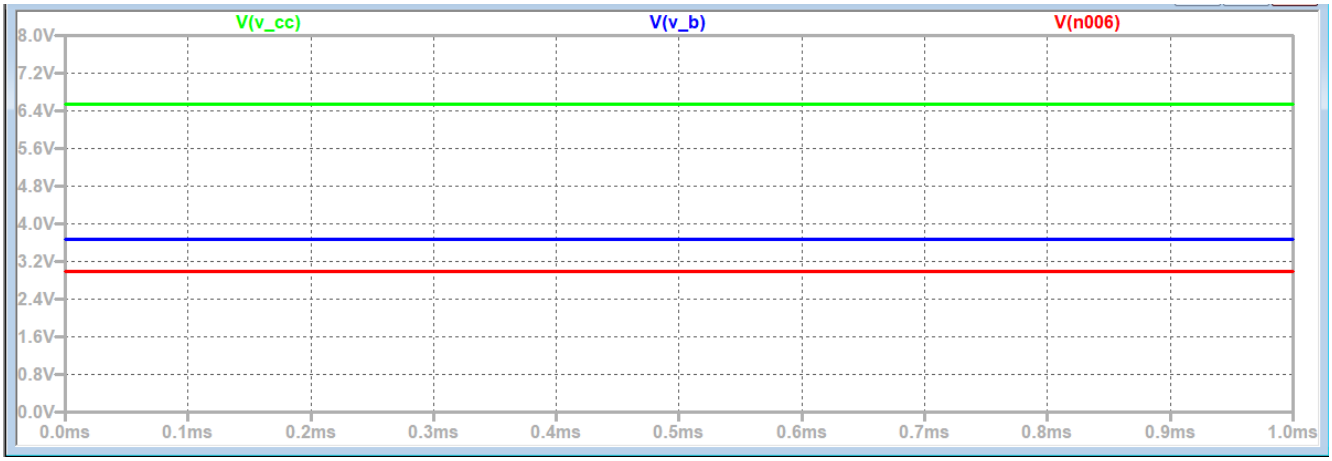
1) DC power consumption at idle. Disconnect V_{in} and V_{out}: Now your amplifier is ON and idling at DC. It is ready to amplify current, but there is no input to be amplified.

Measure the power consumed by the amplifier circuit from V_{CC} in idle condition at the Q-point

Find a clever method to do this without disturbing the circuit operation **5**



The trick would be to simply disconnect V_{in}. We don't have to worry about disconnecting V_{out} since once the circuit reaches steady state R_L doesn't draw any current.
The above method allows us to easily measure stable Q-point power dissipation of the amplifier components.



Simulation results:
$V_{CC} = 6.56V, V_B = 3.7V, V_E = 3V$
Quiescent DC Power consumption:

$$P_{R_{B1}} = \frac{(V_{CC}-V_B)^2}{R_{B1}} = \frac{2.86V^2}{15K\Omega} = 0.545mW$$

$$P_{R_{B2}} = \frac{(V_B)^2}{R_{B2}} = \frac{3.7V^2}{22K\Omega} = 0.622mW$$

$$P_{R_E} = \frac{(V_E)^2}{R_E} = \frac{3V^2}{430\Omega} = 20.9mW$$

$$P_{Transistor} = (V_{CC} - V_E) * I_C = 3.56V * 6.9mA = 24.56mW$$

Total DC power dissipation is: $P_{DC} = 46.631\text{mW}$

2) AC power consumption during amplification. Now apply a bipolar V_{in} input as earlier, and again measure the peak power consumed from V_{CC} (a suitable modification of the method used in 1.a) might be useful)

Keep the power consumed by the FG circuit and the load R_L as separate quantities. Power consumed by the FG can be measured independently and subtracted, *before* connecting it to the amplifier to get AC power measurement during amplification. Power delivered to the load is measured separately below.

What is the power consumed by the amplifier circuit itself during AC operation? **10**

The AC power can be measured by finding the max amplitude of swing about the DC values.
$\delta V_E = 0.4V\ (peak - peak \equiv 3.4V - 2.6V)$
$\delta V_B = 0.4V\ (peak - peak \equiv 4.1V - 3.3V)$
$\delta V_{CC} = 0V$

$P_{R_{B1}} = \frac{(\delta V_{CC} - \delta V_B)^2}{R_{B1}} = \frac{0.4V^2}{15K\Omega} = 0.0107mW$

$P_{R_{B2}} = \frac{(\delta V_B)^2}{R_{B2}} = \frac{0.4V^2}{22K\Omega} = 0.0073mW$

$P_{R_E} = \frac{(\delta V_E)^2}{R_E} = \frac{0.4V^2}{430\Omega} = 0.372mW$

$P_{Transistor} = |(\delta V_{CC} - \delta V_E) * \delta I_C| = 0.4V * 1.9mA = 0.76mW$

Total AC power dissipation is: $P_{AC} = 1.15\text{mW}$

3) What is the power delivered to the load? (re-verify the Level 2 result) Accordingly what is the ratio of power delivered to the load to the power consumed within the amplifier circuit itself?

5

Only AC power is supplied to the load, the DC power used is the expense for maintaining the conditions for active region transistor action.

$P_L = \delta I_L * \delta V_{out} = \frac{\delta V_{out}^2}{R_L} = \frac{(430mV)^2}{500\Omega} = 0.369mW$

$\frac{P_L}{P_{AC}} = 0.322$, thus, we can deliver about 24% to the load and the rest is used up in operating the amplifier.

4) Provide a detailed analysis of why the current amplifier is unable to deliver the peak power specification to R_L.
> Did you go wrong somewhere in the step-by-step calculations?
> Was some operation assumption violated?
> Is there a fundamental limitation to this circuit design that will never let it the desired peak power delivery specification?

10

The apparent inefficiency of the circuit in terms of power usage is inevitable because:

- The biasing resistors R_{B1} *and* R_{B1} are required for maintaining a stable DC quiescent voltage V_B.
- The Emitter resistor is also crucial in maintaining the quiescent value of V_E.
- Thus, the overall DC and AC power loss of the CC amplifier circuit can only be optimized keeping in mind the constraints required for operation.

The simple CC-amplifier has the above limitations, thus changing parameter values is not a solution.
So, in order to decrease the power loss further one must redesign the circuit such that it allows for lesser constraints while preserving the current amplification.

Level 3: Optimize design to reduce power consumption 20 [Advanced question]

3.1 Provide a rough circuit idea along the lines of Fig 1, to solve the main problem with power dissipation in amplifier v/s poor efficiency in delivering power to the load 5

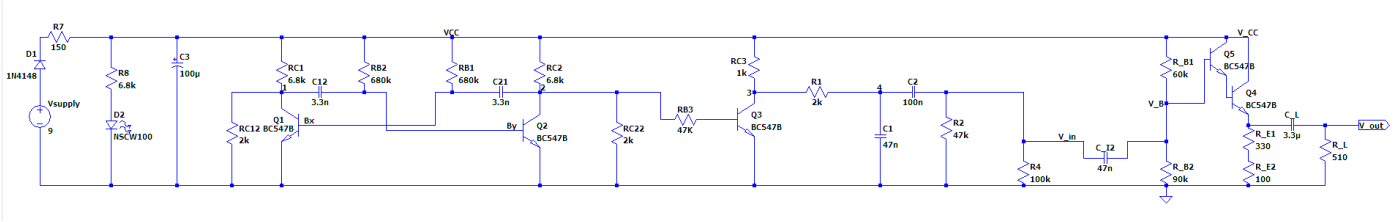
Using a Darlington Pair of transistors. Combination of transistors that allows us to increase the effective current gain $\beta_{net} = \beta_1\beta_2$

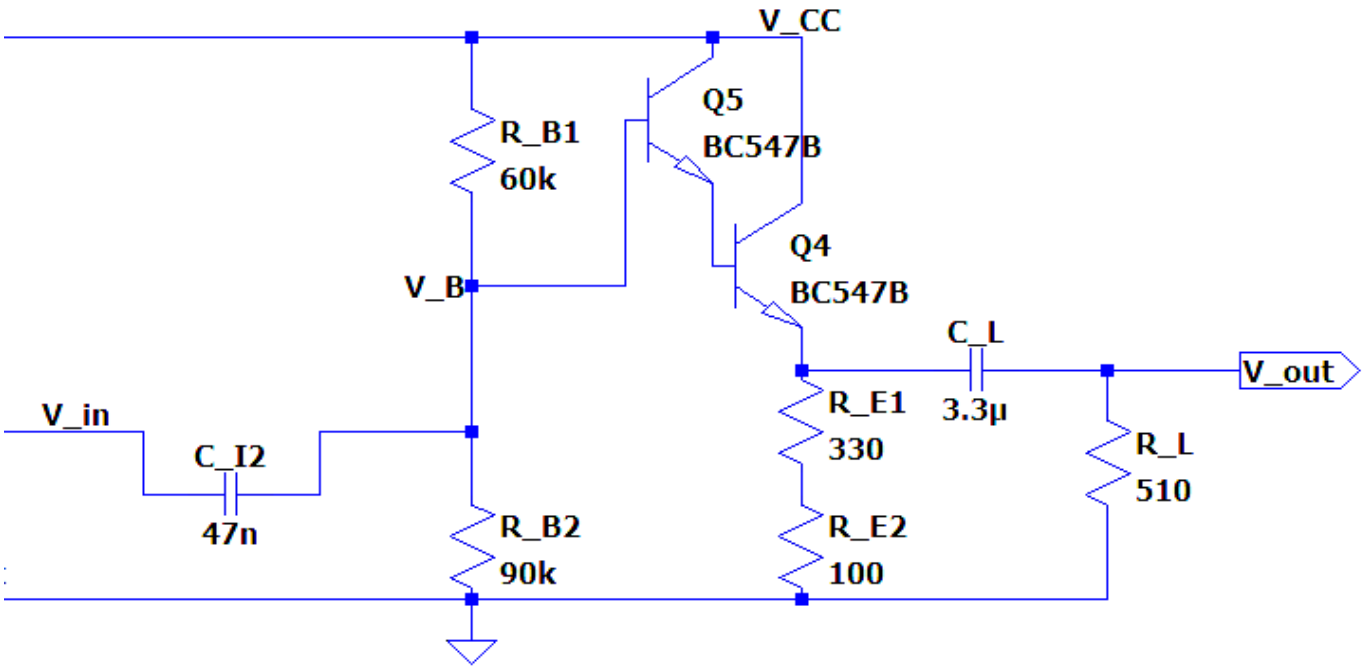
How they allow us to improve the power distribution:

- Power consumption through R_{B1} and R_{B2} can be reduced drastically since now the condition $(R_{B1}||R_{B2}) \ll R_B$ allows large R_{B1} and R_{B2} values. This is because $R_B = \beta(r_e + R_E)$ is modified to $R_B = \beta^2(r_e + R_E)$.
- All other conditions will still be achieved for optimal active region action. With the very beneficial increase of the input impedance R_{inp} and the decrease in output impedance bringing the circuit closer to an ideal current source.

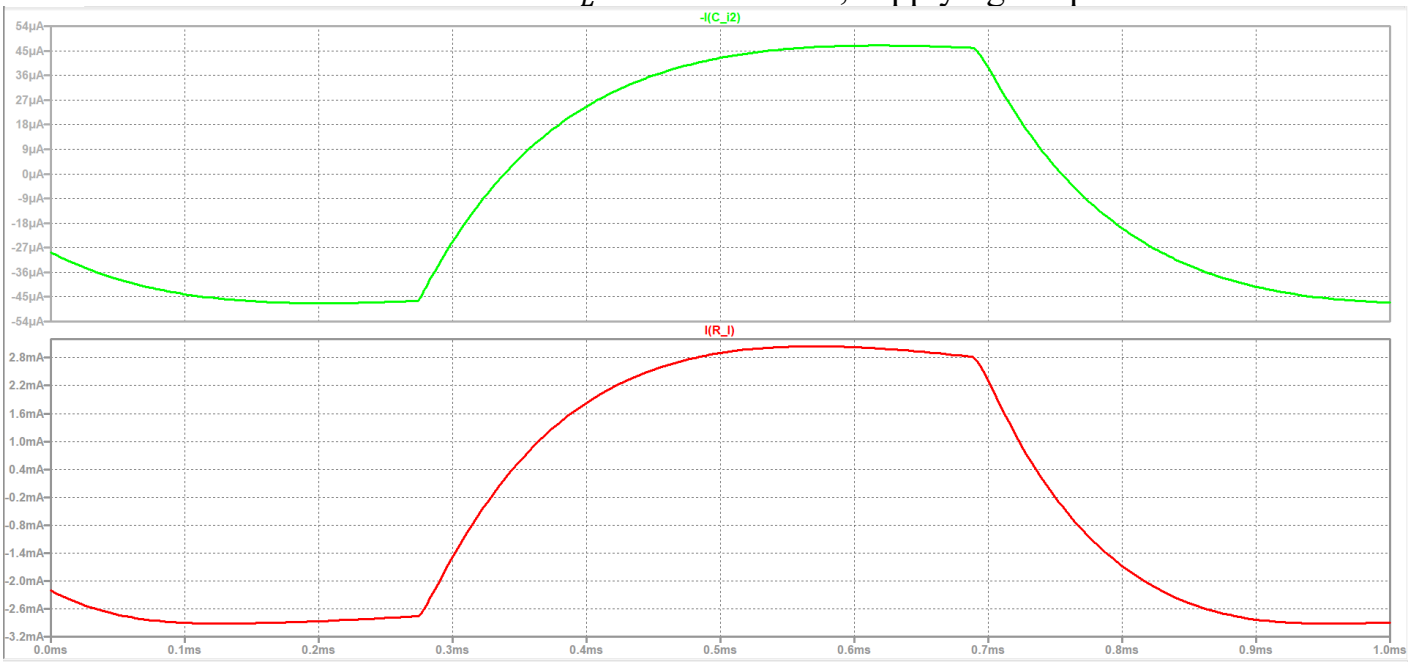
3.2 Fill out your circuit idea of (3.1) as a full-fledged LTSpice simulation. Use the same design parameters as Level 1. 5

Insert your circuit design image and the LTSpice simulation results here.





With this circuit we can achieve the δI_L we wanted thus, supplying the power needed.

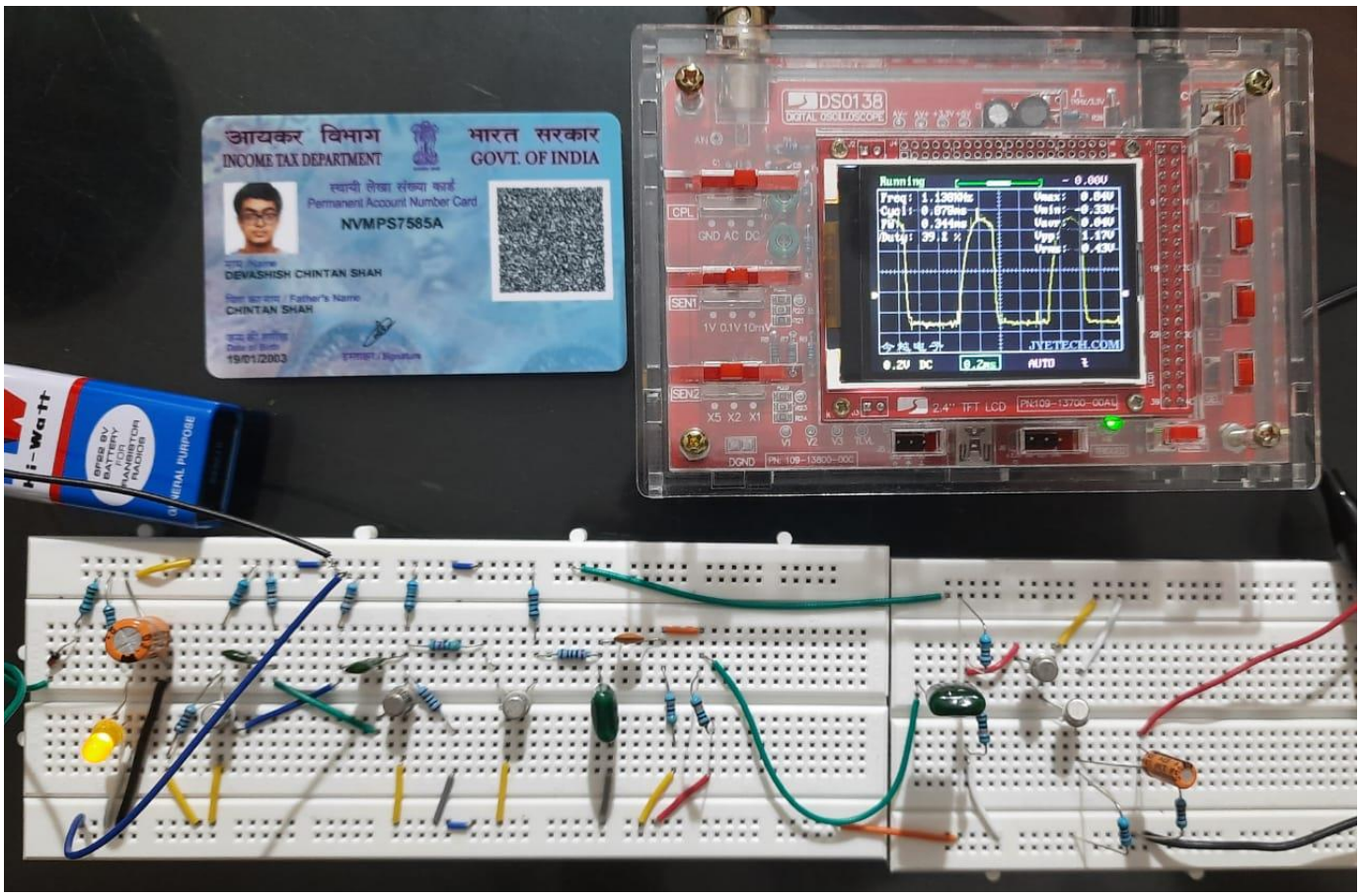


The input voltage is miniscule compared to the output, with current gain of about 64. This is what helps decrease the unnecessary power dissipation in the CC amplifier.

3.3 Build a working circuit as per your full design of (3.2) and demonstrate that it achieves close to the desired power delivery to the load **10**

As usual, provide a photo of your working circuit with your ID card and the measured DSO waveforms highlighting what is better about your Level 3 design

The goal of optimal power distribution has been achieved but there are certain distortions which need to be analyzed.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