Lab 3.2: Putting opamps to 'gainful' use [Negative Feedback]

Note: This assignment contains hardware demo questions corresponding to the design + simulation problems in Lab 3.1 **[40]**

Before starting on building the opamp circuits, see the demo video posted on Moodle to check that your 741 opamp is in good working condition

Part A: Simple Negative Feedback

A.1) Simple negative feedback to set finite voltage gain G_f

Non-inverting negative feedback

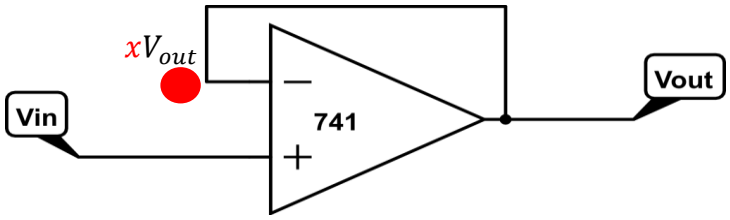


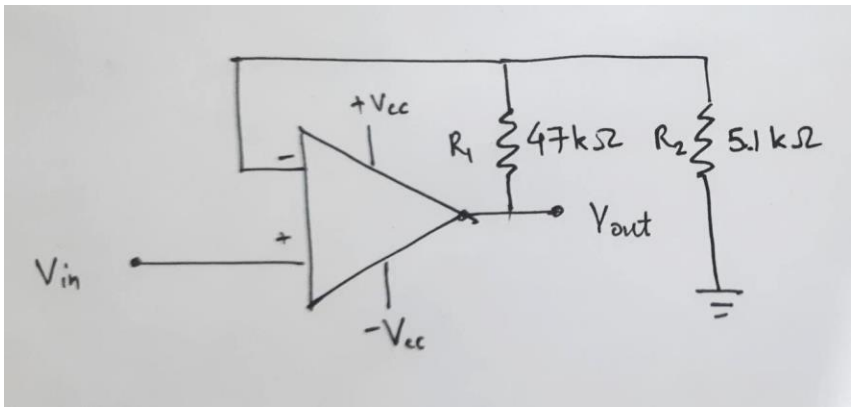
Fig 1: Basic scheme for opamp negative feedback, preserving the sign of V_{in}

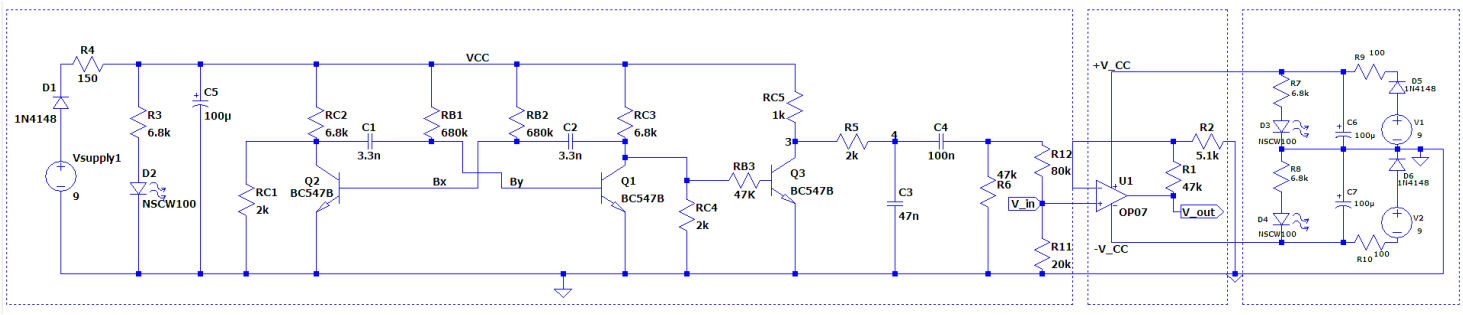
NOTE: As discussed by sir in the live session, the resistor values of the order of ~ $100k\Omega$ or more must be avoided because of non-zero tolerances. Keeping this in mind, the resistor values in some parts of lab 3.1 have simply been scaled down keeping the ratio same.

Demo of negative feedback with $G_f = +10$

For reference, put a copy here of the LTSpice circuit and time domain simulation output as you have solved for this exercise in Lab 3.1

Resistor values used: $R_1 = 47k\Omega \; and \; R_2 = 5.1k\Omega$ (shown in diagram below)





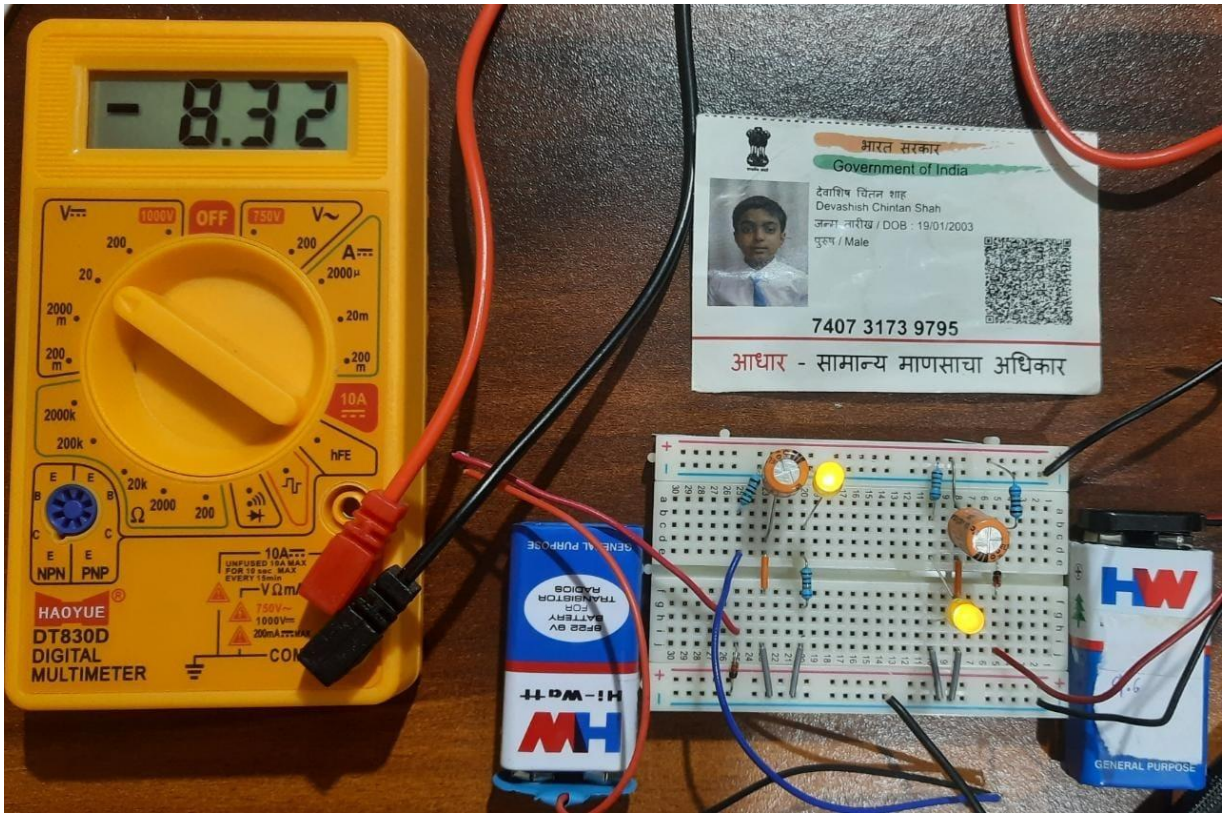
Demo of V_{in} $G_f = +10$ [5]

Setup your breadboard circuit with dual power supply $\pm V_{CC}$. The AFG from PH231 is to be setup again to produce a sawtooth waveform.

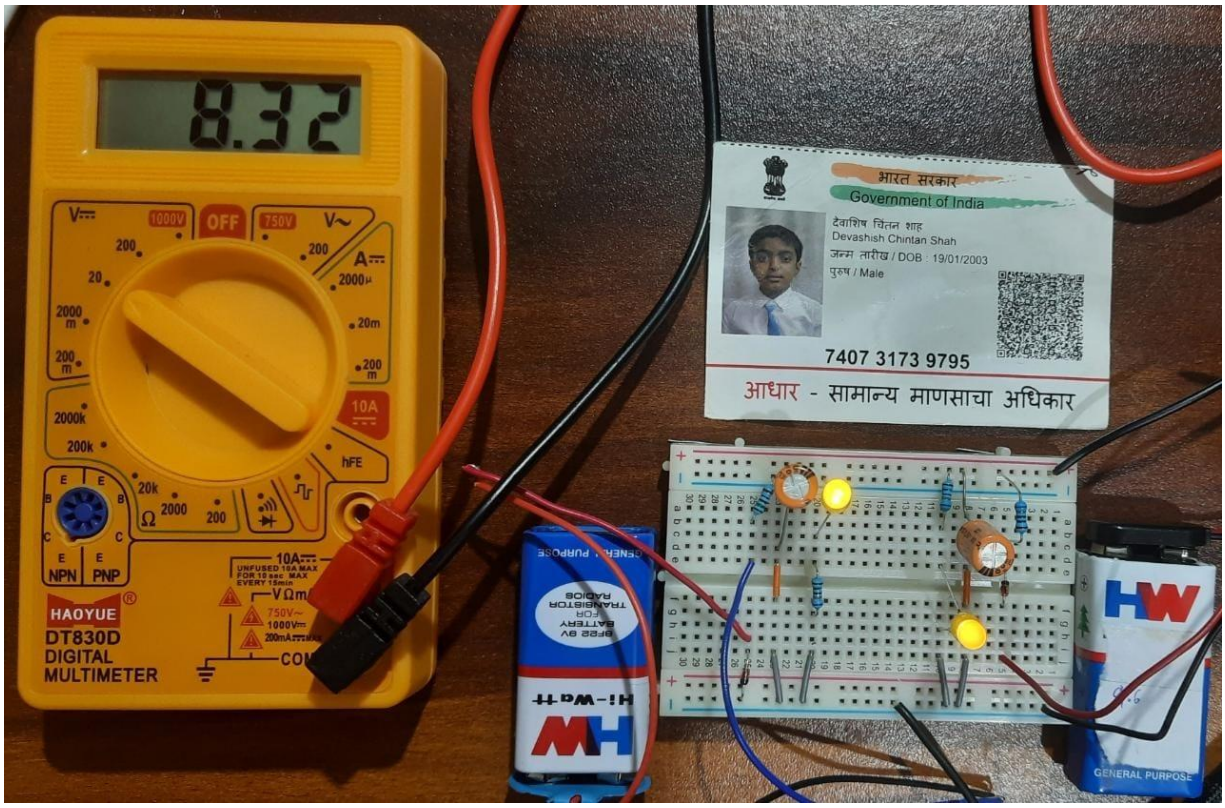
Put photos here showing clearly:

1) Your $\pm V_{CC}$. Make sure that your individual battery voltages are close to 9V, and the component values chosen for the protection resistors are equal so that you get a symmetrical $|\pm V_{CC}|$ ~ 8.12V (an asymmetry up to ~ 0.15V is acceptable)
   PHOTO 1: $+V_{CC}$ 1 mark
   PHOTO 2: $-V_{CC}$ 1 mark

$-V_{cc}$:


- 8.32
HAOYUE
DT830D
DIGITAL
MULTIMETER
भारत सरकार
Government of India
देवाशिष चिंतन शाह
Devashish Chintan Shah
जन्म तारीख / DOB : 19/01/2003
पुरुष / Male
7407 3173 9795
आधार - सामान्य माणसाचा अधिकार
GENERAL PURPOSE

$+V_{cc}$:



The two battery voltages were such that symmetrical protection resistors yielded $\sim 0.5V$ difference in the magnitudes of supply voltages, so I tinkered a little and selected a slightly larger protection resistor for one branch and obtained the desired values.

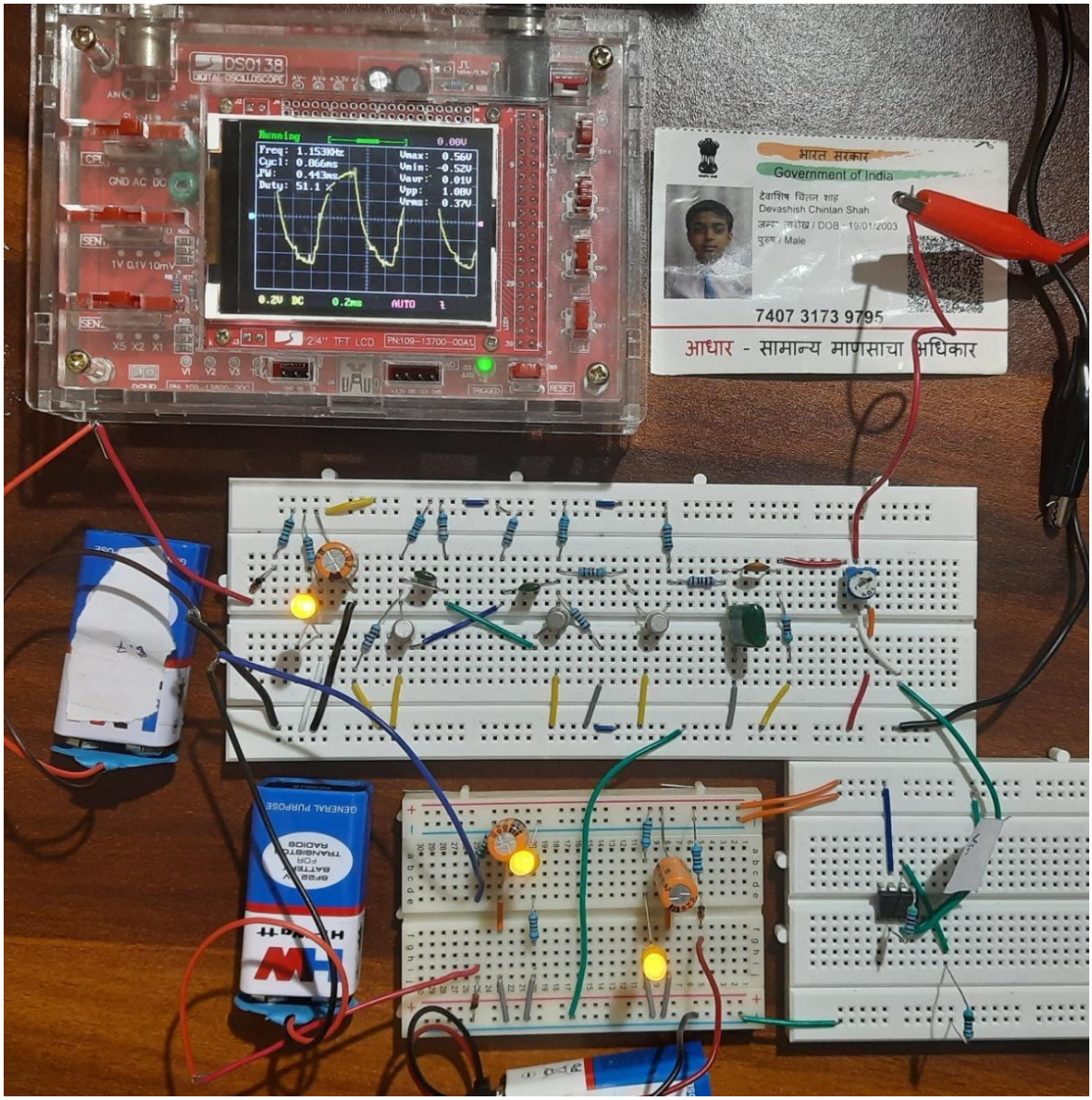
Since the circuit had to be on for quite some time, I kept checking if discharging of either battery more had caused any asymmetries (because asymmetric resistors meant slightly different power consumption) along the way and fortunately nothing of this sort had occurred.

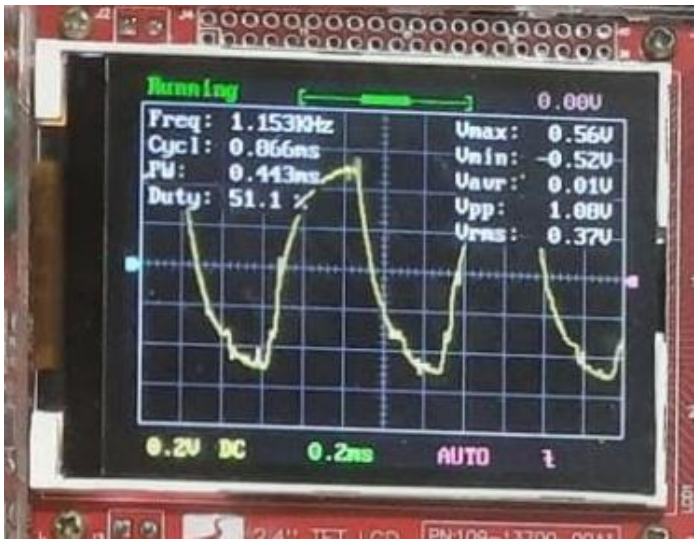
2) PHOTO 3: Output of AFG: 3 marks

Obviously you will need to supply only $+V_{CC}$ to the AFG circuit blocks. Make sure to use a hefty 100µF capacitor to bypass the power supply rails to the AFG

Note: looking ahead, if you expect to get a gain of $G_f = +10$ from the following opamp, choose a suitable value of the output amplitude of the AFG (using potentiometer at its output) so as to not saturate the opamp! Your V_{in} photo should clearly indicate its amplitude

V_{in} from the FG: $\pm 0.52V$





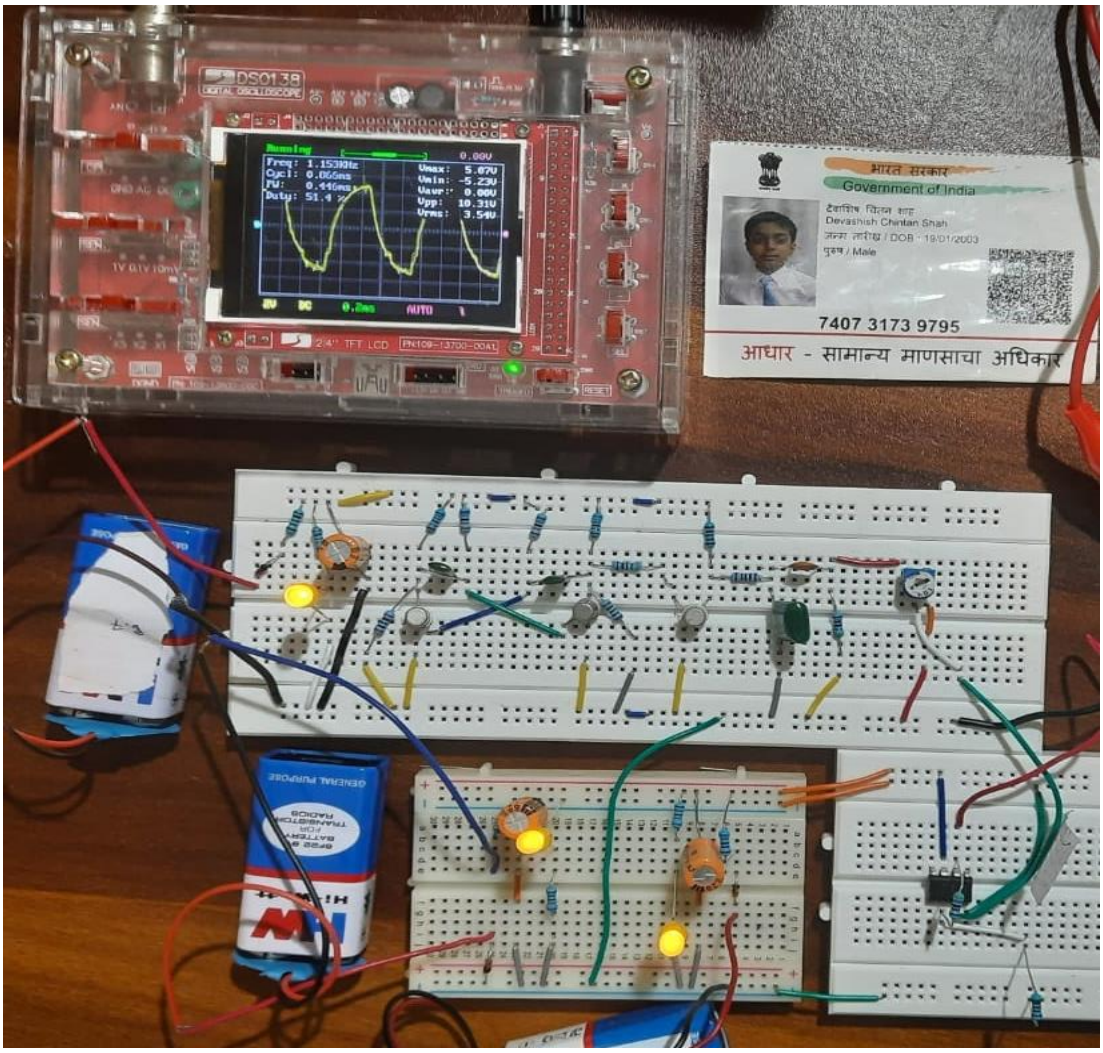
Demo of V_{out} [5]

Connect V_{in} demonstrated above to the input of your opamp circuit as designed and built on your breadboard.

Note that here too, you should use hefty 100μf capacitors to bypass both $+V_{CC}$ and $-V_{CC}$. Be careful of the polarity of the electrolytic capacitor connections! Electrolytic capacitors have a polarity indicated by a (–) sign on one terminal. The (–) terminal must always be at a lower potential.

Provide a photo here of your end-to-end connected circuit, demonstrating a gain $G_f = +10$ times the V_{in} shown above.

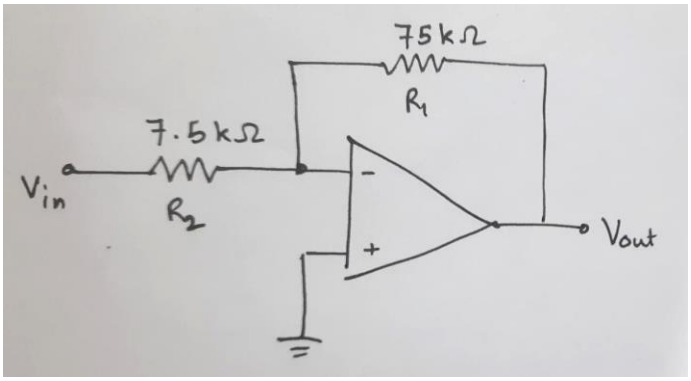
V_{out} from Amplifier: $\pm 5.15V$

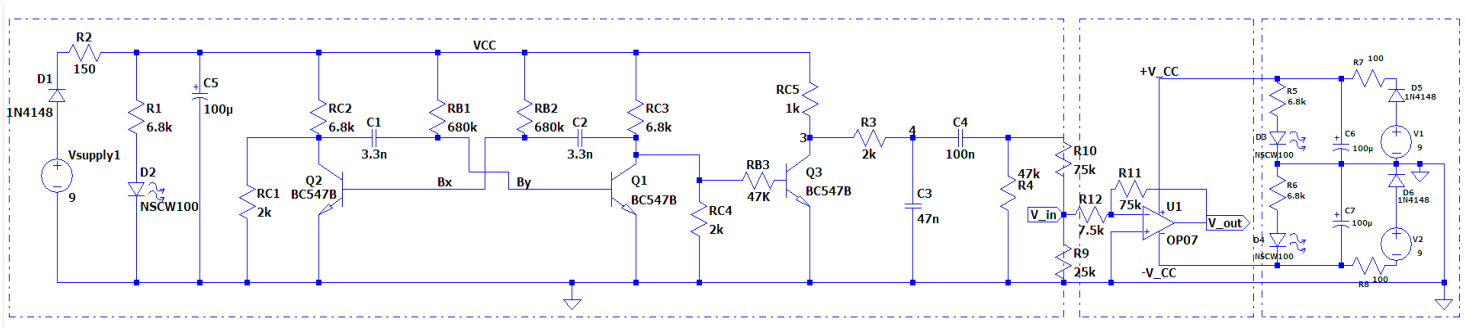


Indeed, we see that $V_{out} = G_f V_{in}$. ($G_f = +10$)
Zoomed in DSO on next pg.

A.2) DEMO: Negative feedback, inverting the sign of V_{in} : $G_f = -10$

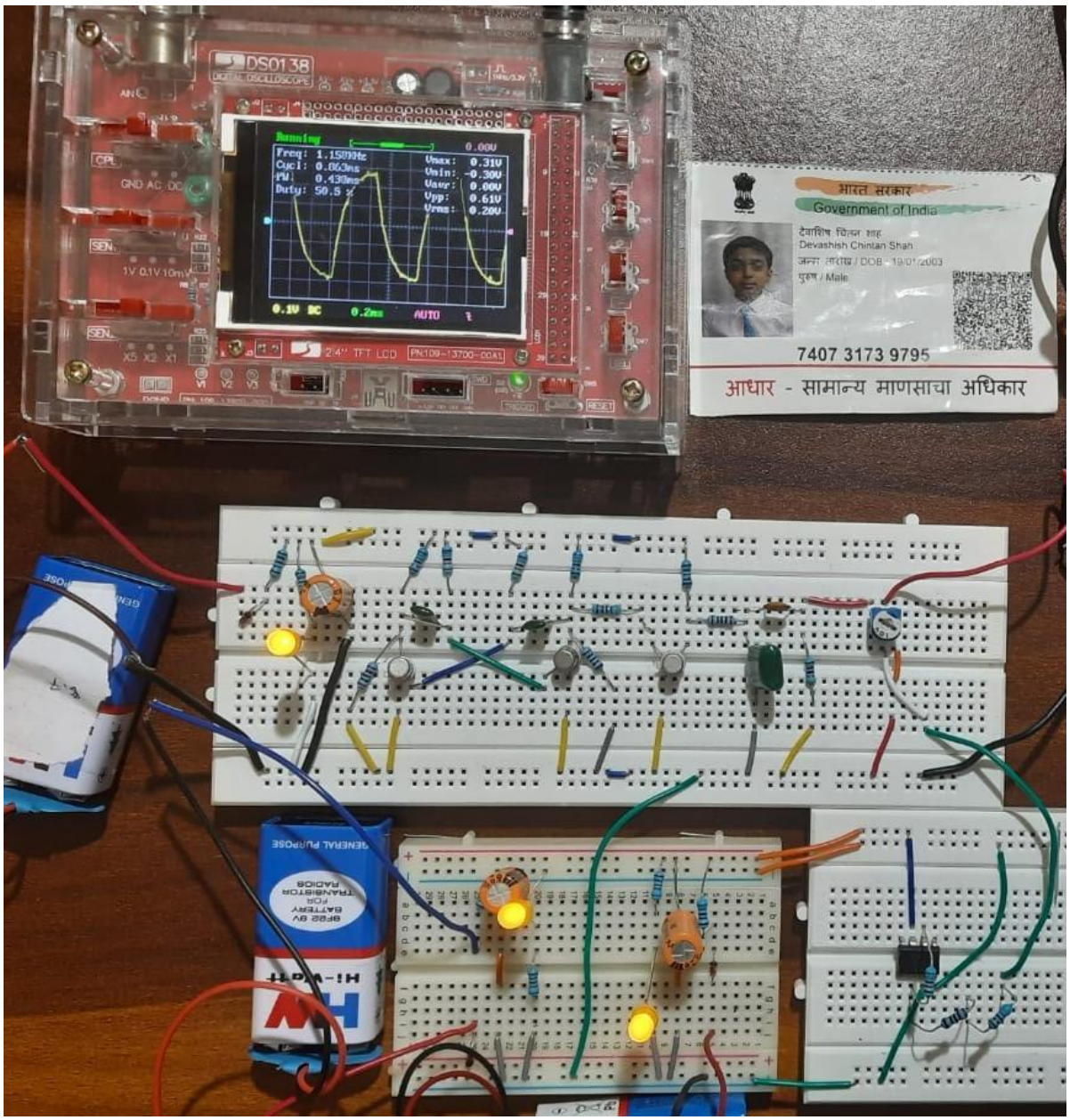
Put here a copy of your circuit design for this exercise from Lab 3.1 for the negative feedback amplifier that provides a gain $G_f = -10$:

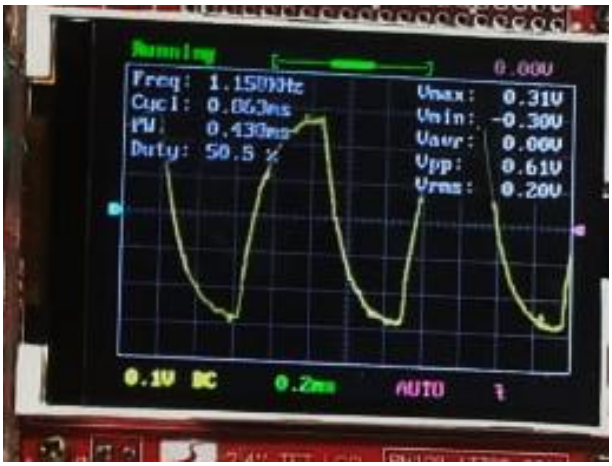




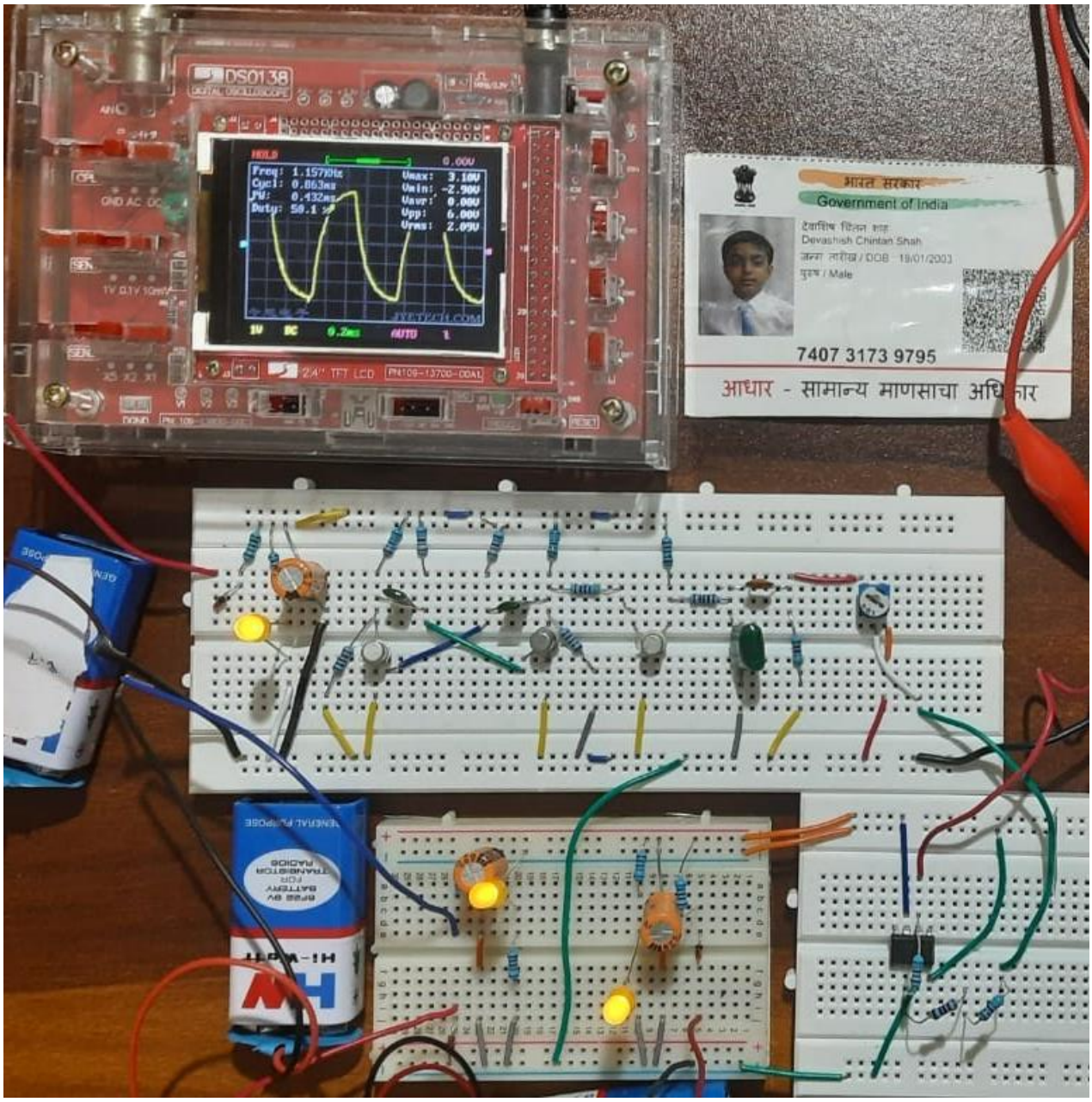
A.2.1) PHOTO 1: Provide a photo of V_{out} from your circuit as built, that demonstrates in practice a gain of $G_f = -10$ **[5]**

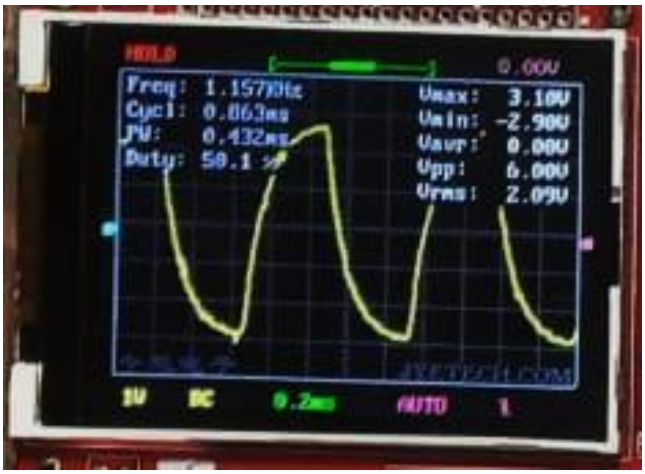
V_{in} fed from the FG: $\pm 0.3V$


DS0138
Running
Freq: 1.150kHz
Cycl: 0.863ms
PW: 0.430ms
Duty: 50.5 %
Vmax: 0.31V
Vmin: -0.30V
Vavr: 0.00V
Vpp: 0.61V
Vrms: 0.20V
0.1V DC 0.2ms AUTO
भारत सरकार
Government of India
Devashish Chintan Shah
7407 3173 9795
आधार - सामान्य माणसाचा अधिकार


Running
Freq: 1.150kHz
Cycl: 0.863ms
PW: 0.430ms
Duty: 50.5 %
Vmax: 0.31V
Vmin: -0.30V
Vavr: 0.00V
Vpp: 0.61V
Vrms: 0.20V
0.1V DC 0.2ms AUTO

V_{out} from the Amplifier: $\pm 3V$





A.2.2) [Thought experiment → Real experiment] [5]

Provide photo proof here of whatever clever method you have devised to prove that the output is indeed inverted in sign w.r.t. the input. Else measuring just the output V_{out} waveforms on your DSO would look identical for both $G_f = +10$ and $G_f = -10$!

Now we measure V_{out} relative to V_{in}.

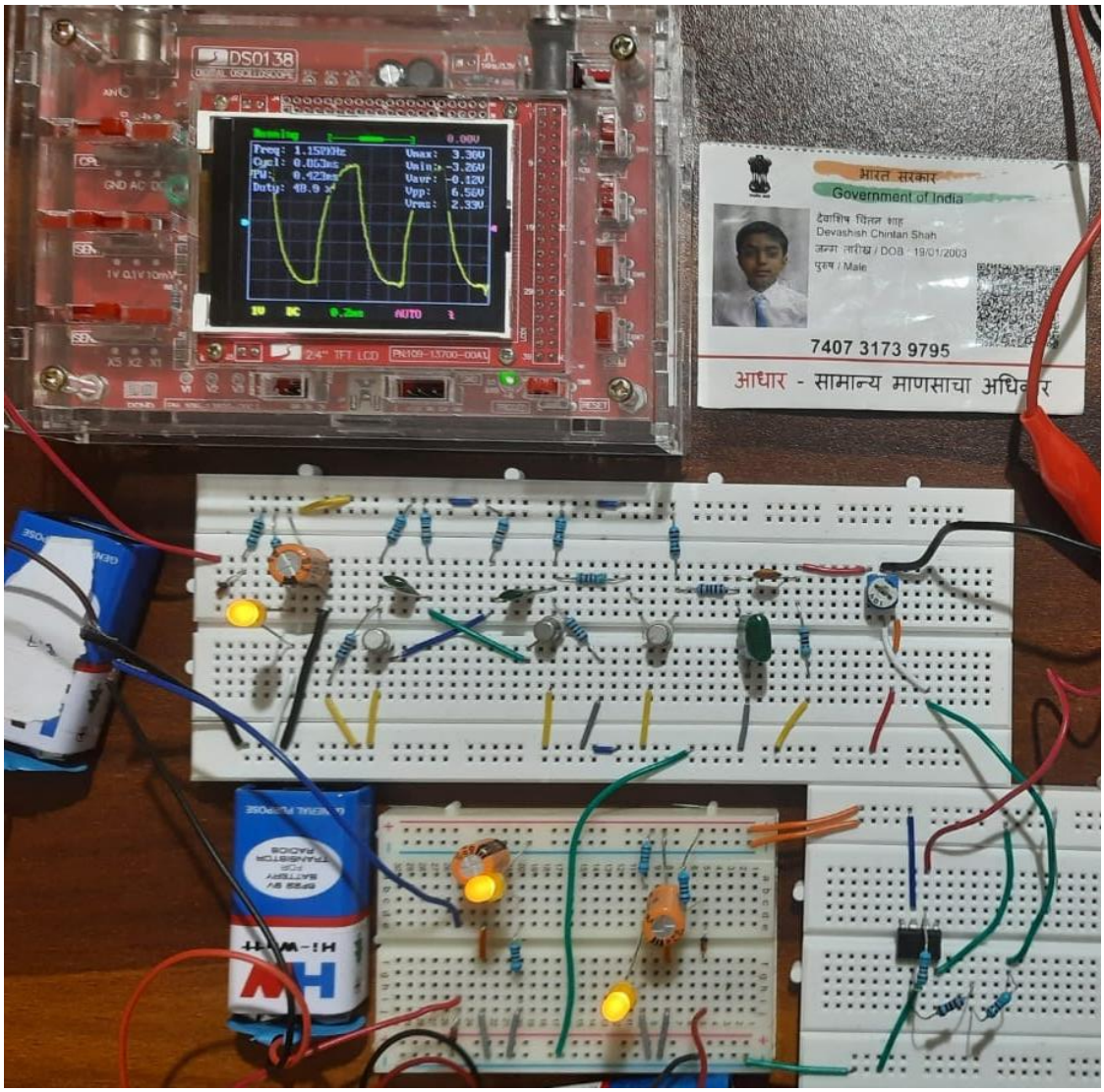
$$V_{DSO} = V_{red} - V_{black} = V_{out} - V_{in}$$

If V_{out} *and* V_{in} are out of phase V_{DSO} will have amplitude

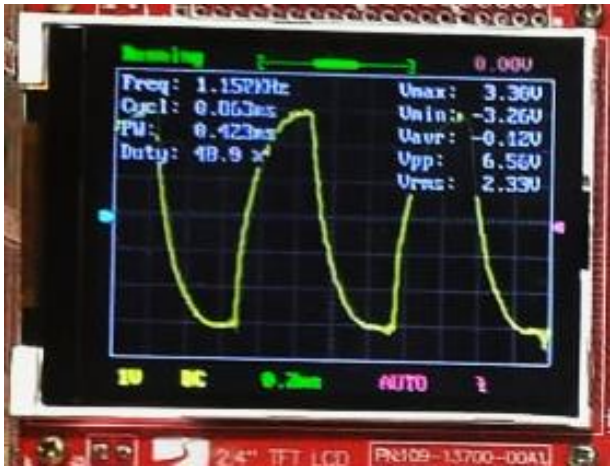
$$V_{DSO} = |(-10 - 1)V_{in}| > |V_{out} - 0|$$

Thus, for our values we must observe $V_{DSO} = \pm 3V - \mp 0.3V = \pm 3.3V$

And this is indeed what is observed practically. Thus, phase difference is $180°$.



Zoomed in DSO



Part B) "Complex" negative feedback

B.1) Integrator / low pass filter

For reference, put a copy of your LTSpice circuit diagram for this exercise in Lab 3.1

Here V_{in} will be fed from the FG and the $\pm V_{CC}$ will be fed from the DC source built earlier.

$$C_1 = 2.2\mu F - in\ series - 3.3\mu F$$

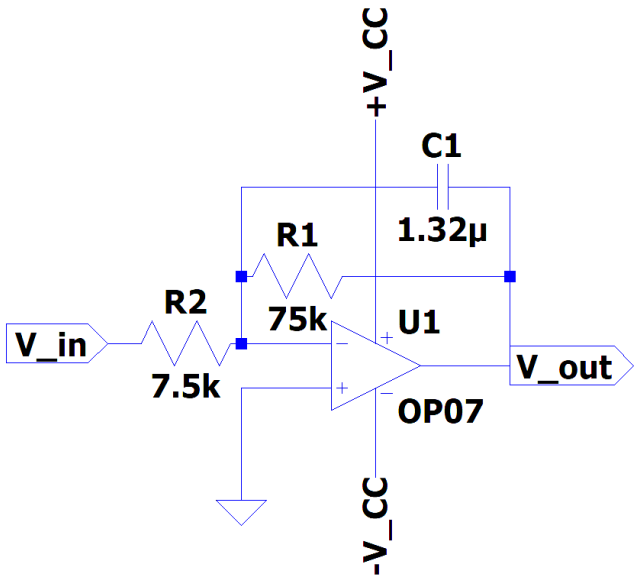


PHOTO of DEMO: [10]

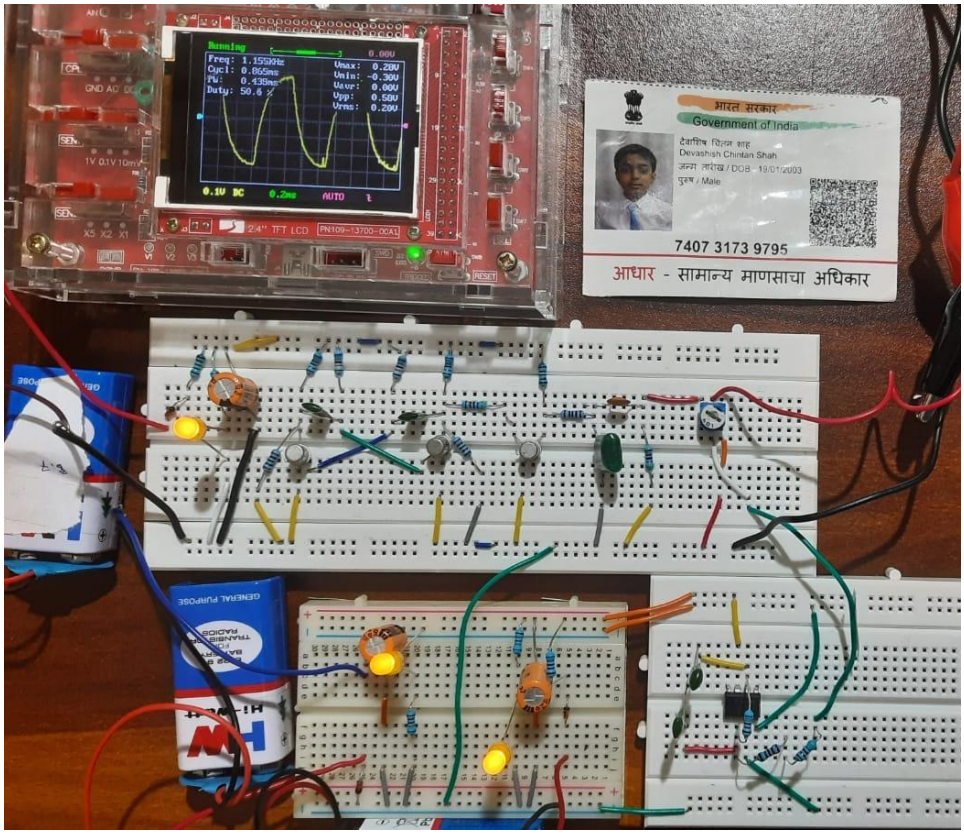
Build the circuit as per above design. Since it produces a single frequency output, doing a frequency sweep is not possible to demonstrate the low-pass filter characteristics. Use a straightforward hack to demonstrate the equivalent circuit behavior of a low-pass filter in the time domain.

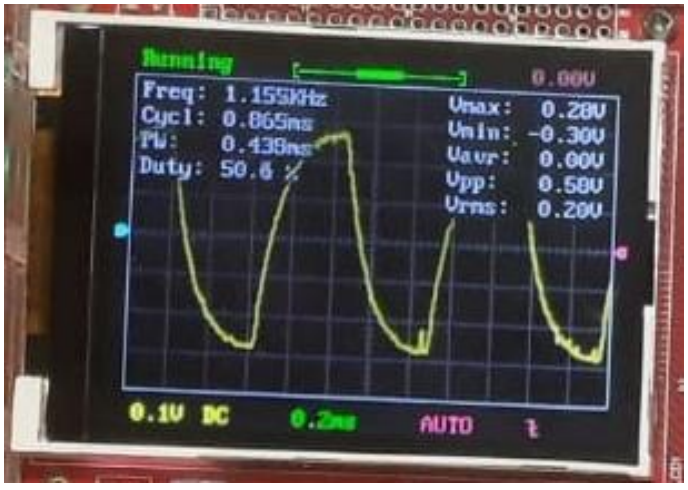
Put a photo of your DSO waveform V_{out} from your op-amp circuit. Use graphic arrows and text boxes to clearly indicate where V_{in} is connected

Since we have built a low pass filter with $f_{3dB} = 160Hz$, we must observe reduced amplification ($|G_f| < 10$) for the FG frequency of 1.1kHz, whereas if we connect a DC input it should be amplified by a factor of -10.

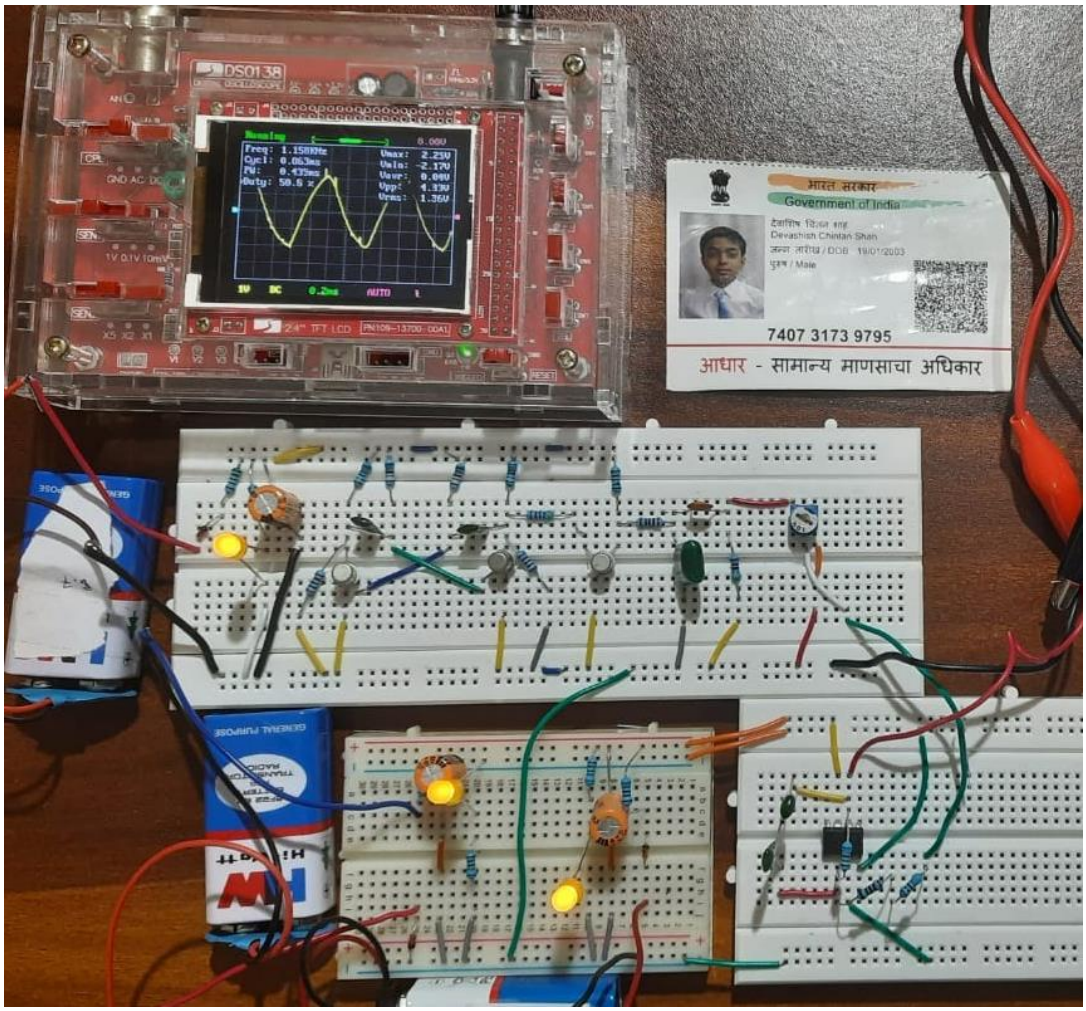
1) AC input from FG:

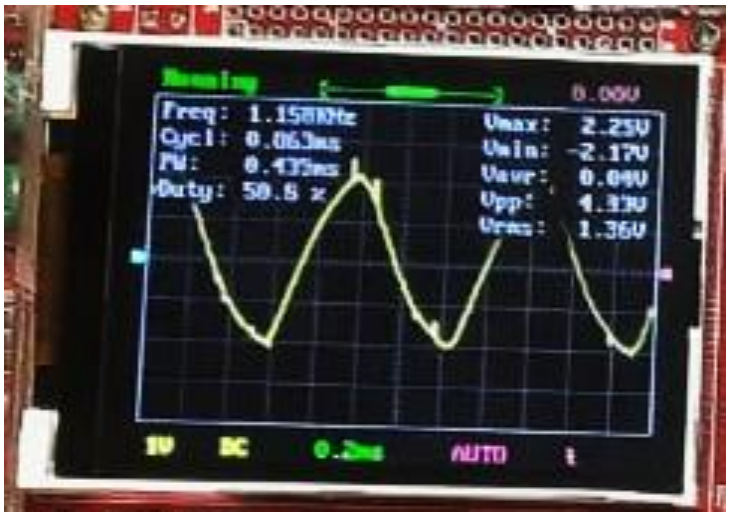
$$V_{in} = \pm 0.29V$$





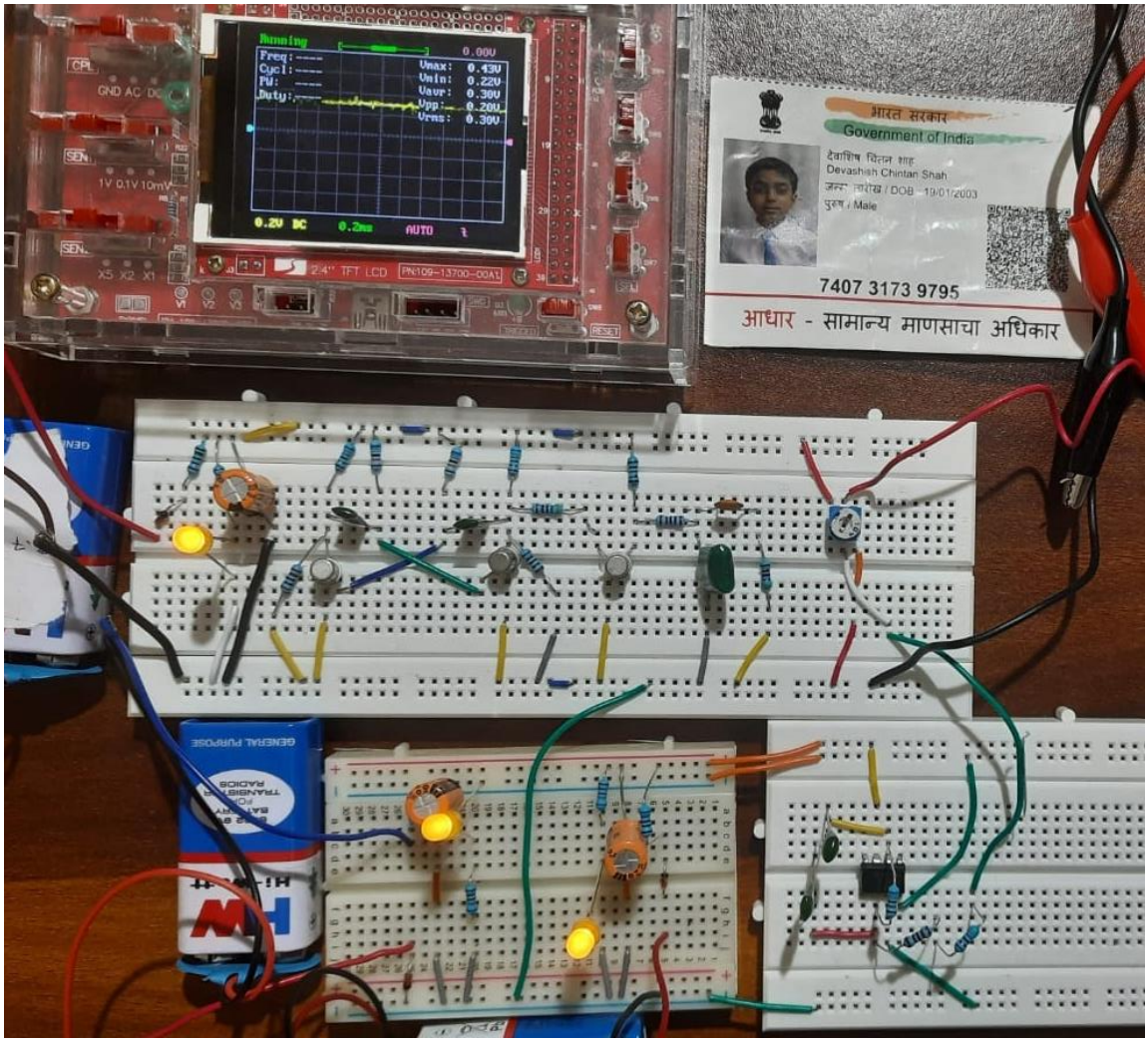
$$V_{out} = \pm 2.17V (< \pm |G_f|\, V_{in})$$

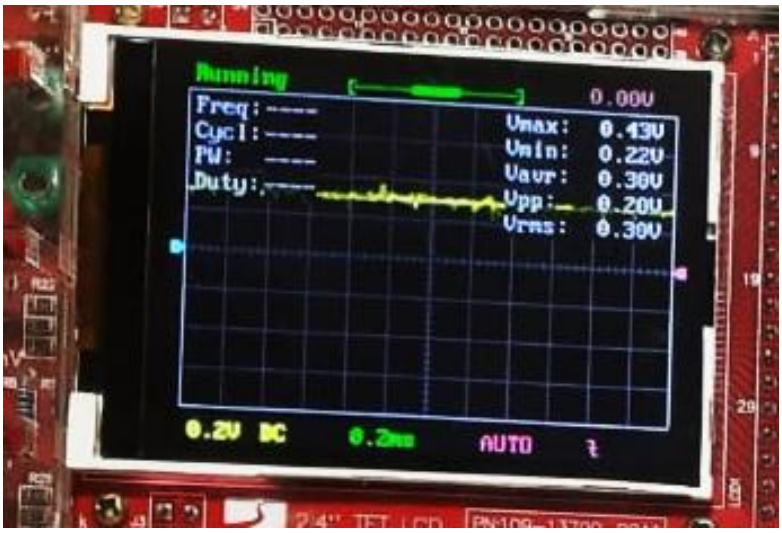

DS0138
भारत सरकार
Government of India
Devashish Chintan Shah
7407 3173 9795
आधार - सामान्य माणसाचा अधिकार


Freq: 1.158KHz
Cycl: 0.863ms
PW: 0.439ms
Duty: 50.8 %
Vmax: 2.25V
Vmin: -2.17V
Vavr: 0.04V
Vpp: 4.33V
Vrms: 1.36V
1V
DC
0.2ms
AUTO

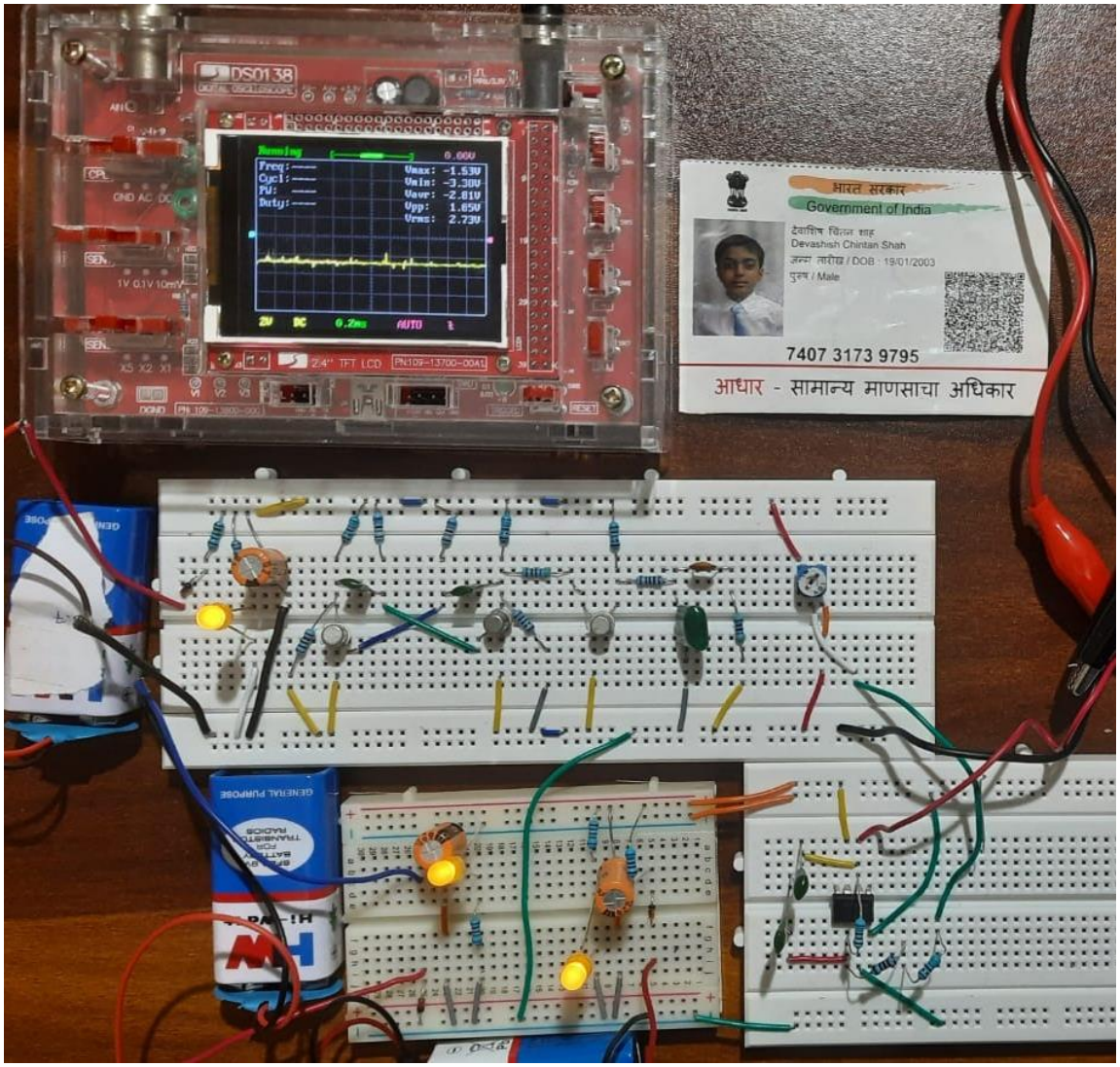
2) DC input from FG:

$$V_{in} = 0.3V\ DC$$





$$V_{out} = -2.81V\ DC \Rightarrow amplification \simeq G_f$$



B.2) Differentiator/ high pass filter

For reference, put a copy of your LTSpice circuit diagram for this exercise in Lab 3.1

Here V_{in} will be fed from the FG and the $\pm V_{CC}$ will be fed from the DC source built earlier.

$$C_1 = 2.2nF - in\ series - 3.3nF$$

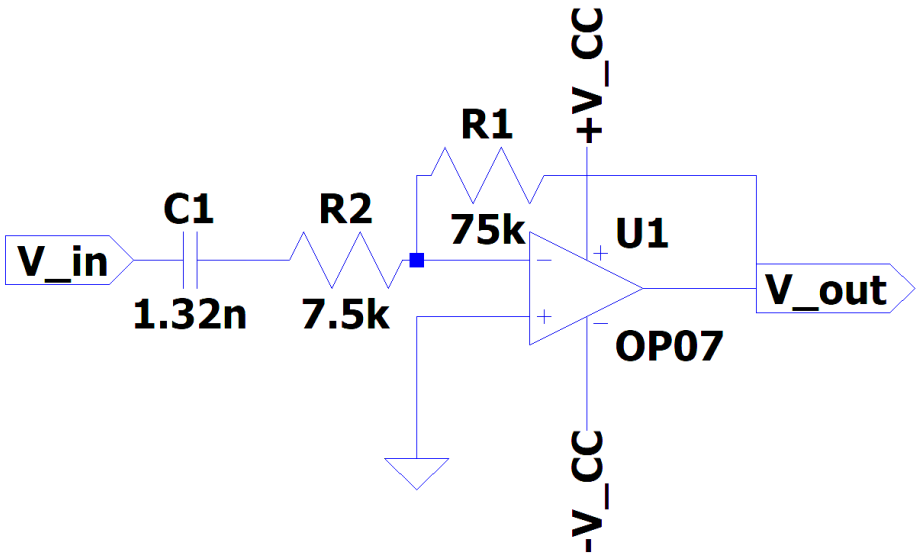


PHOTO of DEMO: [10]

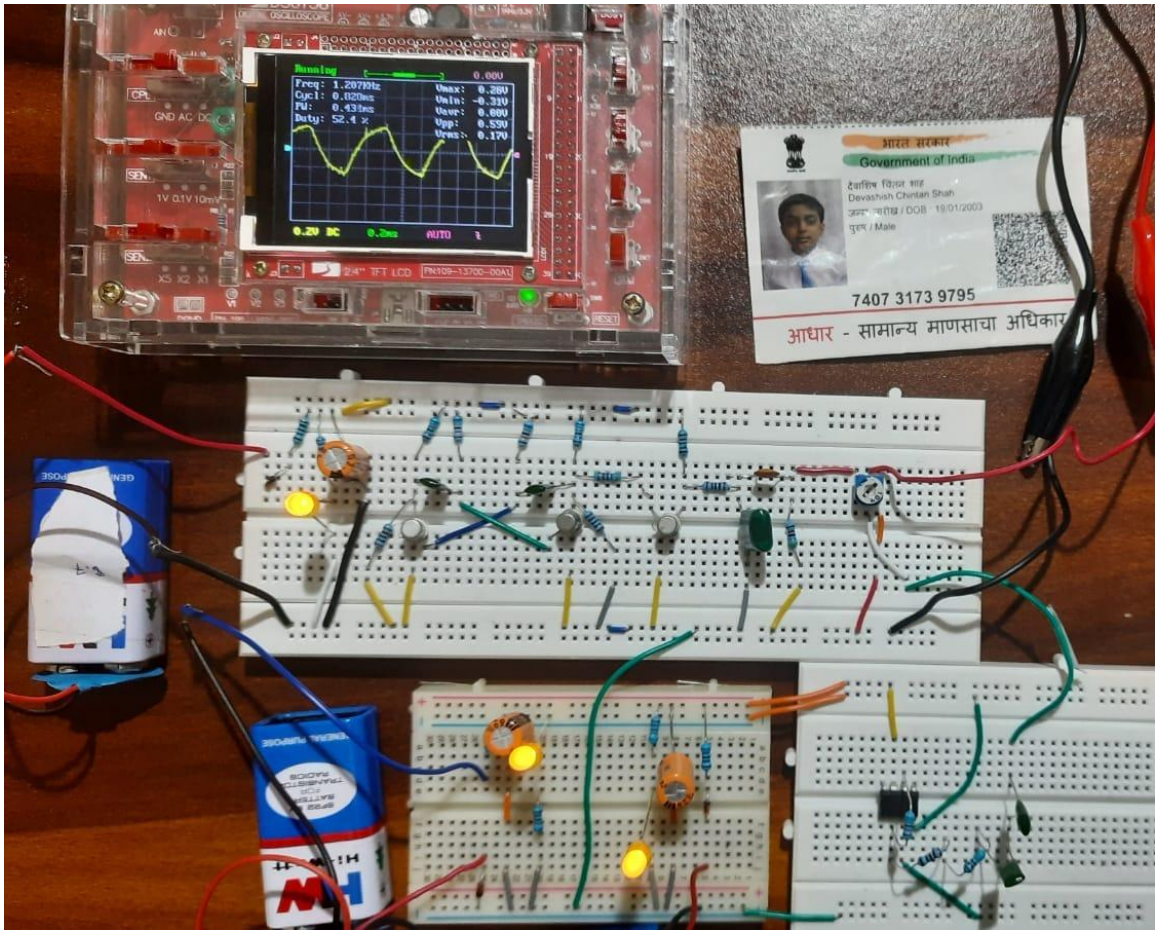
Build the circuit as per above design. Since it produces a single frequency output, doing a frequency sweep is not possible to demonstrate the low-pass filter characteristics. Use a straightforward hack to demonstrate the equivalent circuit behavior of a high pass filter in the time domain.

Put a photo of your DSO waveform V_{out} from your opamp circuit. Use graphic arrows and text boxes to clearly indicate where V_{in} is connected

Since we have built a high pass filter with $f_{3dB} = 16kHz$, we must observe reduced amplification ($|G_f| < 10$) for the FG frequency of 1.1kHz, whereas if we connect a DC input it should be blocked altogether.

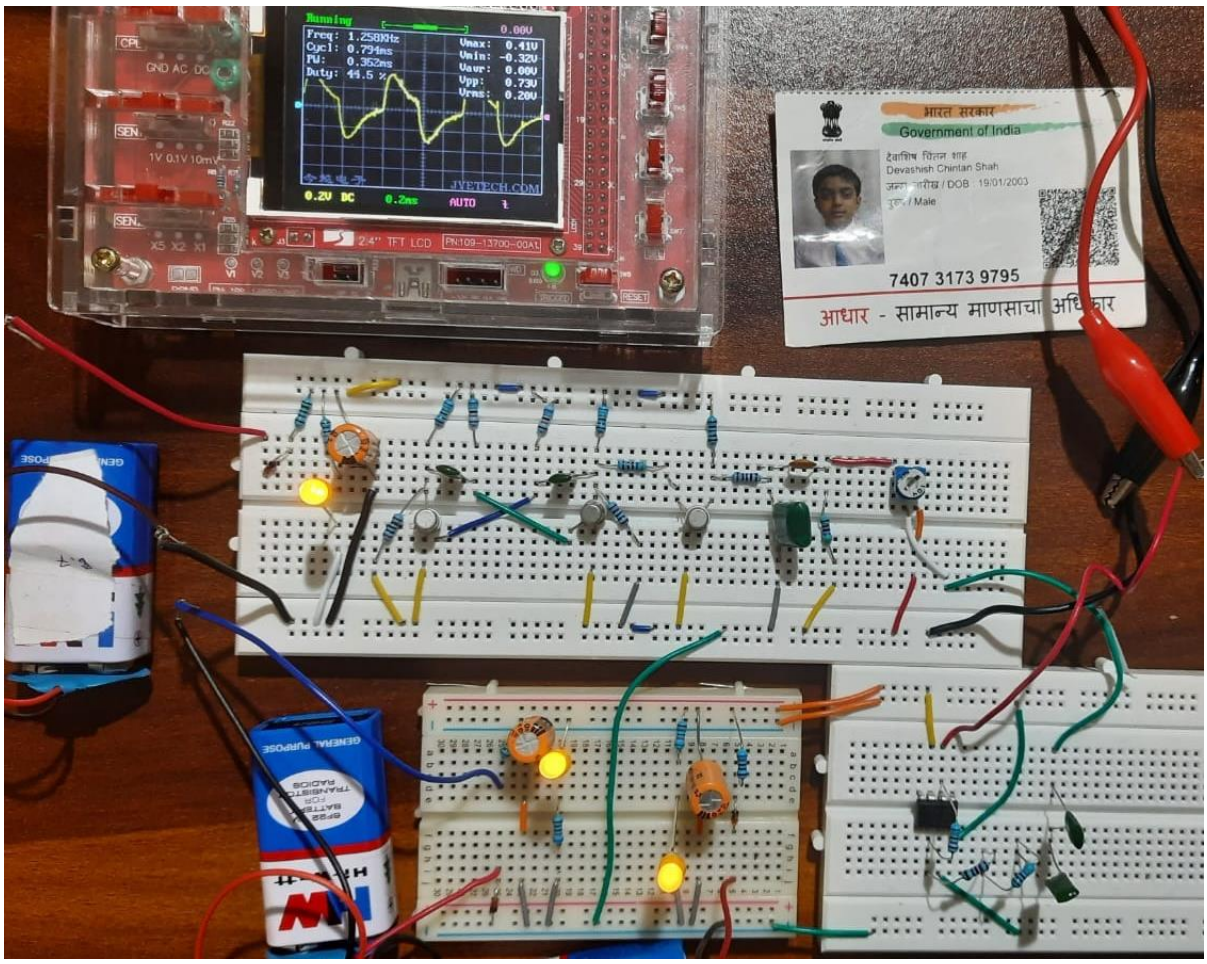
1) AC input from FG:

$$V_{in} = \pm 0.29V$$



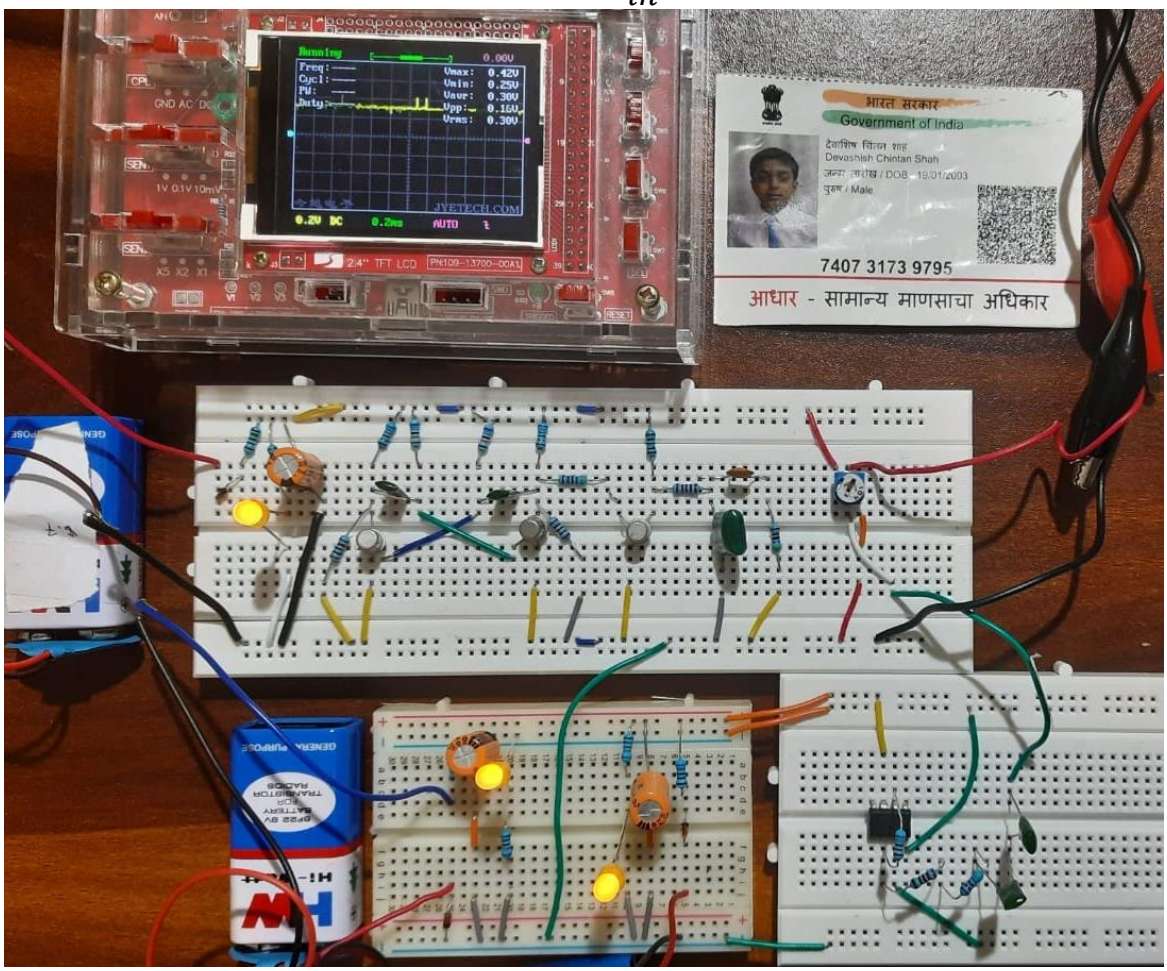
$$V_{out} \simeq \pm 0.36V (< \pm |G_f|\, V_{in})$$

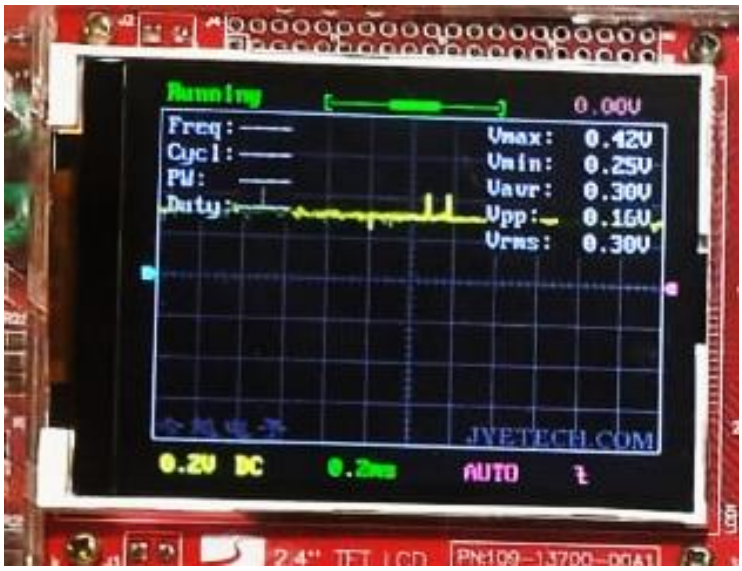
As expected, the circuit behaves as a differentiator and a high pass filter. Since $1.1kHz < f_{3dB} = 16kHz$ the frequency is mostly blocked and $|Gain| < |G_f|$.



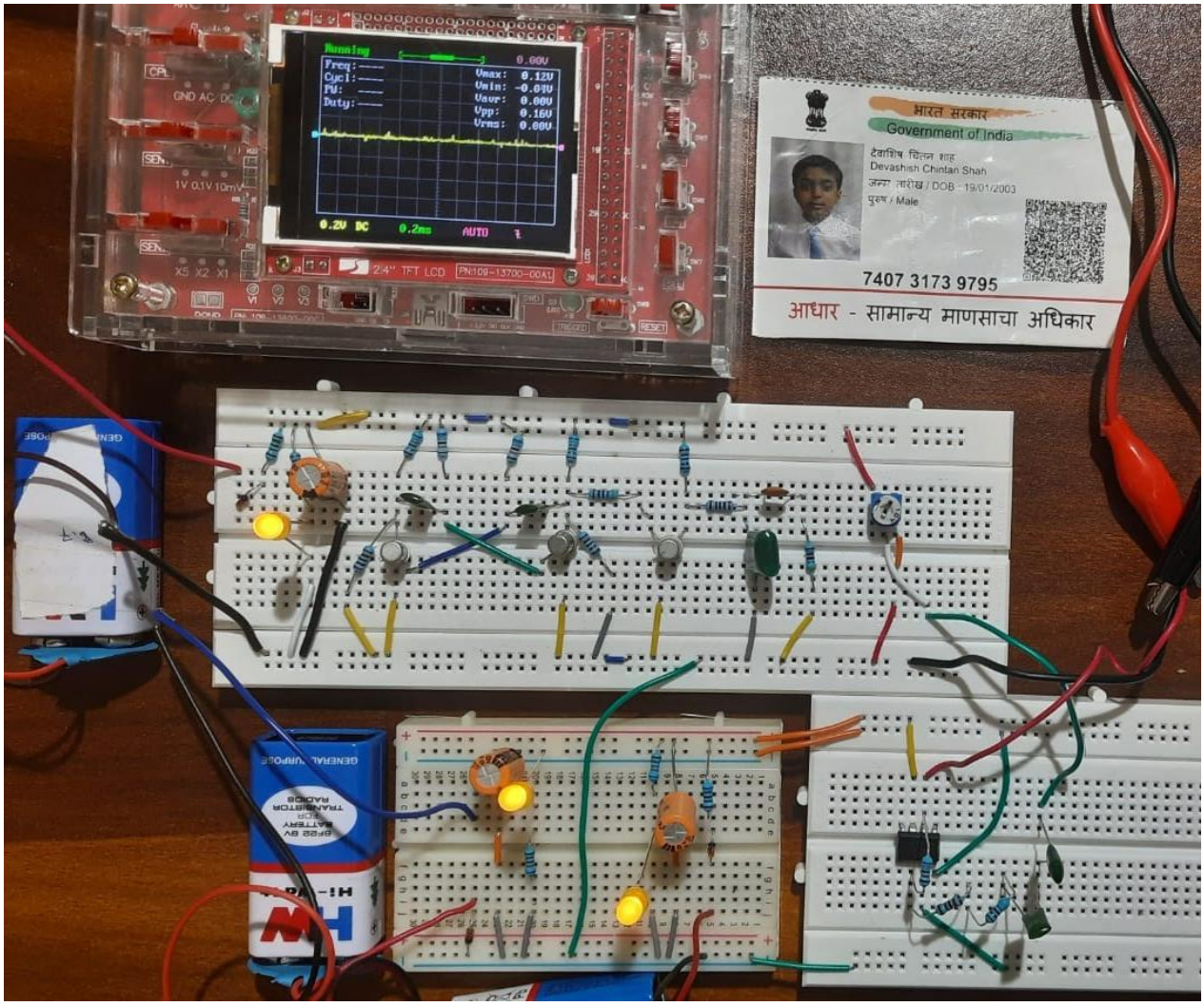
2) DC input from FG:

$$V_{in} = 0.3V\ DC$$





$$V_{out} = 0V\ DC\ blocked$$




Running
0.00V
Freq: ----
Cycl: ----
PW: ----
Duty: ----
Vmax: 0.12V
Vmin: -0.04V
Vavr: 0.00V
Vpp: 0.16V
Vrms: 0.00V
0.2V DC
0.2ms
AUTO