Lab 4: BJT as a Voltage Amplifier: Common Emitter Mode Part 2: the Demo 60

Prerequisite:

You must have a working simulation and physical implementation of a waveform **F**unction **G**enerator that swings to both positive and negative voltages, as worked out in Lab 1 + 2. We call this the FG for short throughout the rest of this lab.

You must have solved Part 1 of this lab assignment – design of a BJT in Common Emitter mode as a voltage amplifier of Gain = –10 and other design specifications as per Part 1. A working LTSpice simulation of the full circuit will be used in matching your measurements of the built-up circuit to the ones predicted from LTSpice.

In case you are not confident of your design from Part 1, the official standardized design is published on moodle – use those component values to get a reliable output and test that your FG works as expected.

Grand goal: Part 2

Demonstrate a working circuit of a BJT configured as a voltage amplifier.

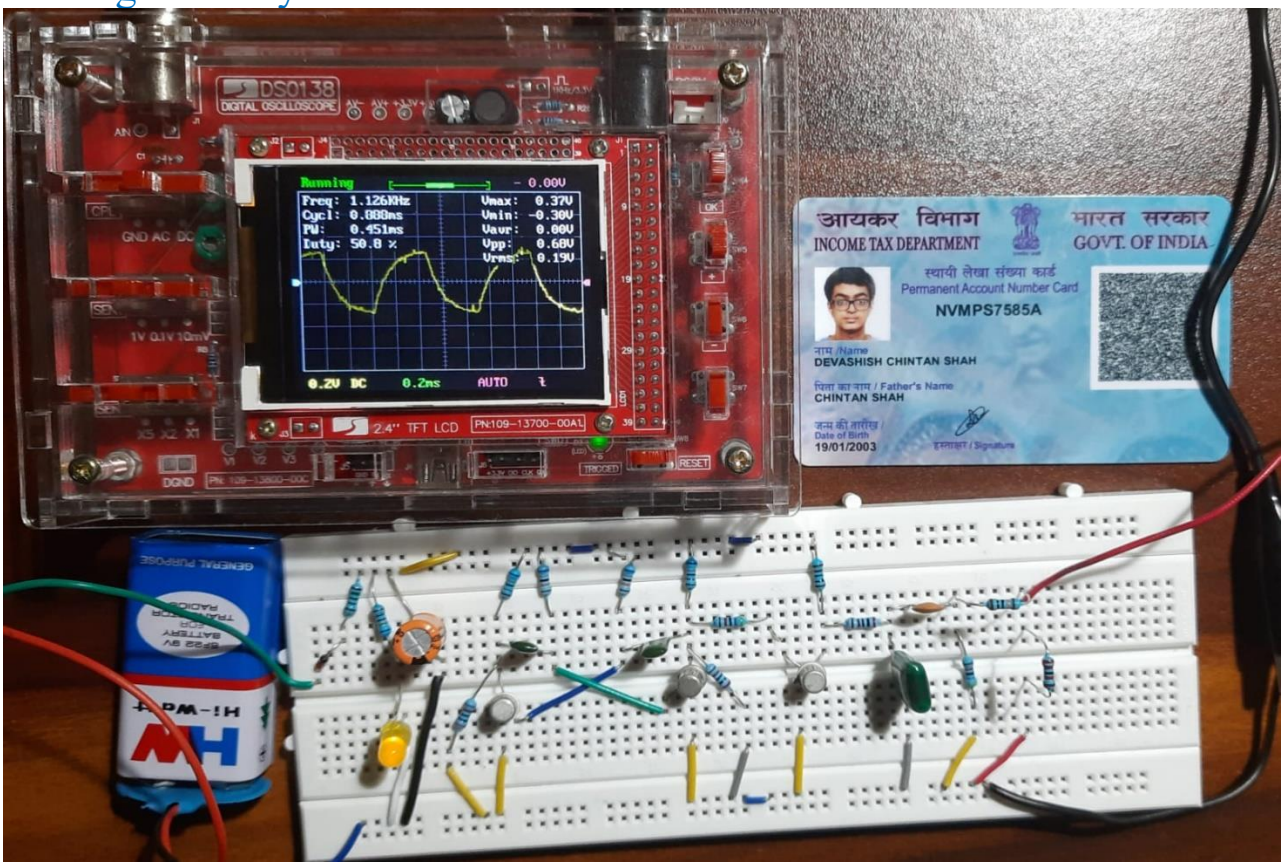
Input provided must be ±0.3V @ f=1.17kHz. With the design specification of Gain = –10 , we expect to see an output voltage swing of ∓3V (negative sign is implicit in the design!)

To help you demonstrate your circuit building expertise and earn piece-wise marks, we have split up the circuit demo into separate parts

Level 0: Function generator (FG) is it still working?) 10

Demonstrate that the FG built earlier and used several times in the past labs is still working! Include a photo of your built-up FG with **no load** connected at the output except the DSO probes. Set the output potentiometer to produce a sawtooth waveform of ±0.3V @ *f*~1.17kHz

This will be your input for subsequent testing, so we make sure that FG is functioning correctly.



Level 1: Voltage amplifier circuit build Sanity check 10

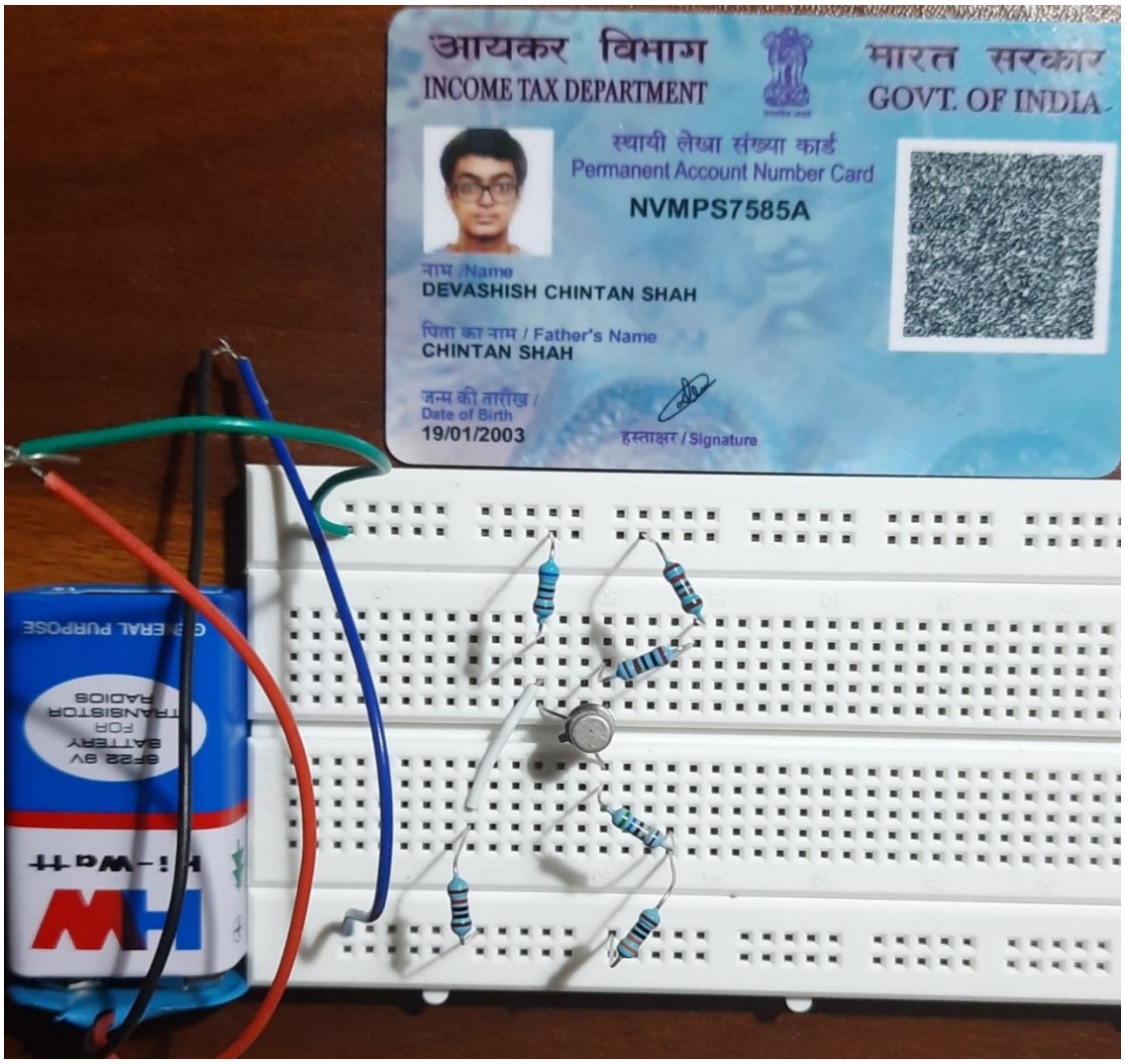
From LTSpice simulation of circuit as designed in Part 1, you should have a clear prediction of the node voltages at various points in your amplifier circuit with no v_{in} applied.

Build your amplifier with 1 BJT. Keep the FG disconnected completely from V_{CC} (since that seems to cause issues with V_{CC} fluctuation as the Q_i in the FG itself slam back and forth from saturation to cutoff). Also don't connect the output of the FG to the input of your amplifier yet.

Using a DMM, check the DC voltages at various nodes in your circuit: V_{CC}, and the BJT terminals C,B,E. Match the measured values to your expectations from design calculations and LTSpice simulation and list them here

This will give you confidence that your BJT voltage amplifier circuit is built correctly and BJT is biased into forward-active mode

The DC Voltage Divider Bias:



V_C

Measured: $V_C = 3.96V$, Calculated: $V_C = 4.15V$

V_B

Measured: $V_B = 1080mV$, Calculated: $V_B = 1090mV$

V_E

Measured: $V_E = 390mV$, Calculated: $V_E = 390mV$

Level 2: Voltage amplifier working with $v_{in} = 0.3V$ 20

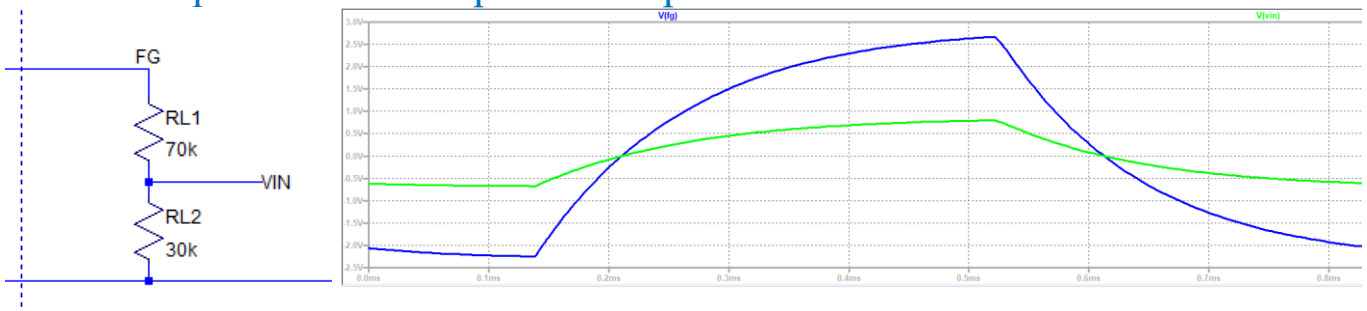
Connect the full end-to-end circuit together: FG → RC-CR shaper → newly built BJT voltage amplifier as per the full LTSpice simulation design of Lab 4, Part 1

Turn power ON and double check the power indicator light, that V_{CC} is indeed reaching your breadboard!

Now your FG *should* be putting out a ±0.3V sawtooth voltage waveform (checked in Level 0) and the newly built BJT common-emitter voltage amplifier should be ready to amplify that voltage (checked in Level 1)

Proceed to test the combination by connect output of your FG to v_{in} of your BJT amplifier. Answer the following questions by performing the hardware checks sequentially – this will help you characterize and understand the built circuit.

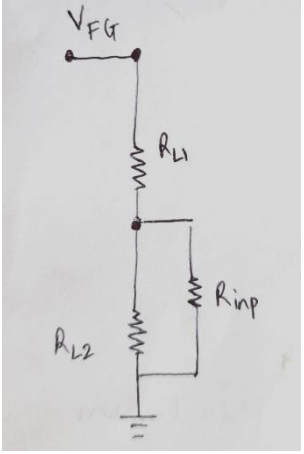
2.1) Does the input impedance R_{inp} of your BJT amplifier cause loading on your FG output, pulling down v_{in} amplitude? For example, V(FG) driving a 100k potentiometer load should be putting out a ±2.5V output. A 30k:70k split of the potentiometer should give you ±0.75V as v_{in} to your newly built BJT amplifier circuit as per the LTspice simulation:



After connecting output of your FG to v_{in} of your BJT amplifier with a 30:70 split ratio of your potentiometer, do you in fact get ±0.75V swing of v_{in}?

Explain quantitatively why not?

No, we don't not get $\pm 0.75V$ swing this is because the equivalent R_{inp} of the CE amplifier is now in parallel to R_{L2}. $V_{FG}(\pm 2.5V)$



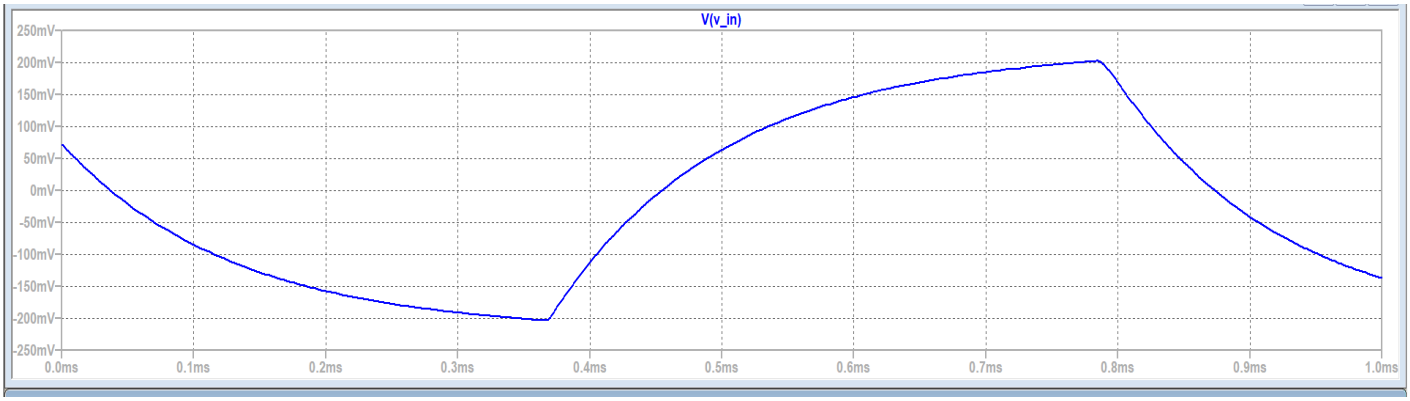
Here, $v_{in} = \frac{R_{inp}||R_{L2}}{R_{inp}||R_{L2}+R_{L2}} V_{FG}$

Thus, a 30:70 split ratio would give:

$$v_{in|peak-peak} = \frac{8.15k\Omega||30k\Omega}{8.15k\Omega||30k\Omega + 70\text{k}\Omega} 5V = 0.42V$$

$v_{in}(\pm 0.21)$

This is exactly the value of v_{in} obtained when this voltage divider is chosen in LTSpice:



2.1.A) Amplifier input R_{inp} loads the FG output. Explain how? 4

Use equations, calculate the effective impedance loading the FG. There is the resistor divider in the 100kΩ potentiometer and R_{inp} of the amplifier to be taken into account!

Thus, using simple voltage divider for $(R_{inp}||R_{L2})$ with R_{L1} gives the value of v_{in} delivered to the FG.

$$v_{in} = \frac{R_{inp}||R_{L2}}{R_{inp}||R_{L2} + R_{L1}} V_{FG}$$

Here, $R_{inp} = 8.15k\Omega$ had been calculated in part-1 and we are free to choose $R_{L1} and\ R_{L2}$ to select desired v_{in}.

2.1.B) INPUT DEMO 5

Instead of re-designing and re-building the whole circuit (big headache when you are likely within a few hours of the submission deadline!), simply adjust the potentiometer setting – you should be able to find some ratio of RL1:RL2 that gets you $v_{in} \sim \pm 0.3V$ at $f \sim 1$kHz

Put a photo of your setup here with DSO measurement of v_{in}

Instead of random trial and error, we can use the formula derived above to estimate the values of $R_{L1}\ and\ R_{L2}$ required for $v_{in} \sim \pm 0.3V$.

$$v_{in} = \frac{R_{inp}||R_{L2}}{R_{inp}||R_{L2} + R_{L1}} V_{FG} \rightarrow \frac{8.15k\Omega||R_{L2}}{8.15k\Omega||R_{L2} + R_{L1}} = \frac{0.3}{2.5}$$

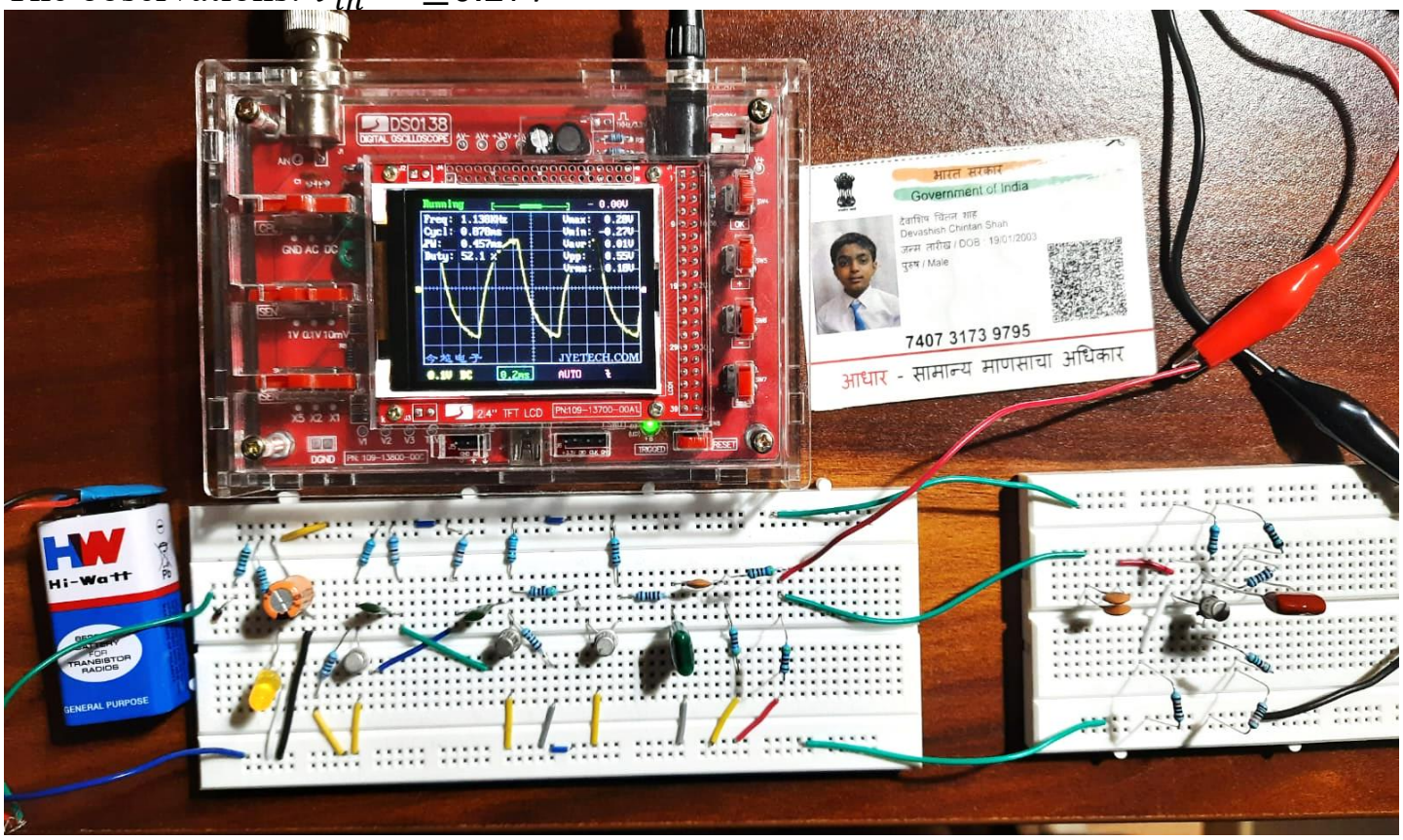
$$\frac{R_{L1}}{8.15k\Omega||R_{L2}} = \frac{25}{3} - 1 = 7.33$$

Set $R_{L1} = 100k\Omega - R_{L2}$. We get $\frac{R_{L1}}{R_{L2}} \simeq 1$.

I used two $47k\Omega$ resistors as my voltage divider.

For this value the predicted $v_{in} = \pm 2.5 \left(\frac{6.94}{6.94+47}\right) = \pm 0.31$

The observations: $v_{in} = \pm 0.27V$



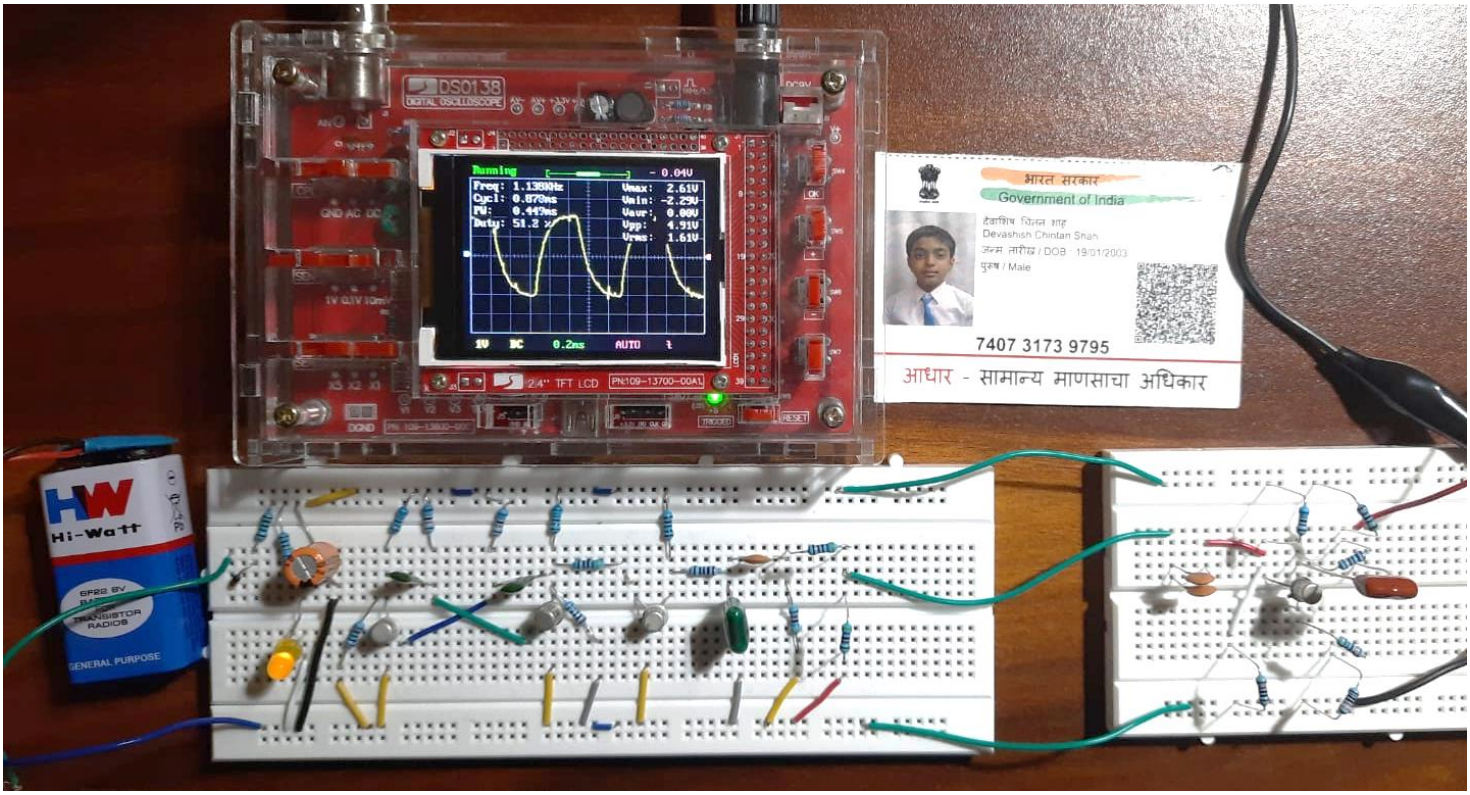
What is the value of RL1:RL2 you ended up using to get $\pm 0.3 v_{in}$ swing? Does it match your calculation of Part 2.1.A? **1**

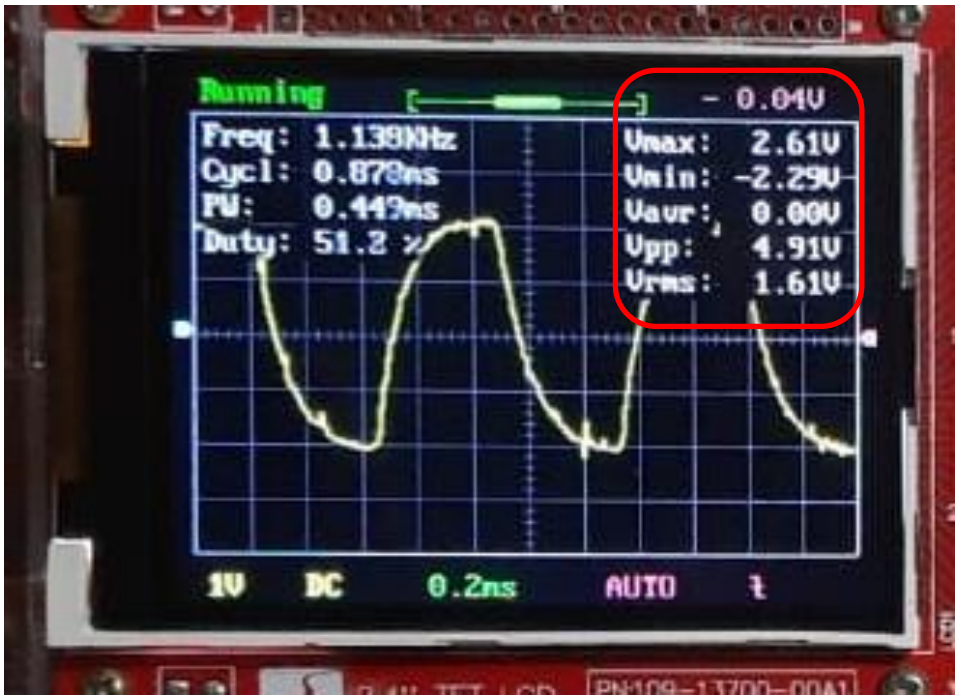
I used two $47k\Omega$ resistors as my voltage divider as calculated in 2.1.B. The observations are in great agreement with the calculations!
(note: the calculations are shown in 2.1.B)

Note that it is incorrect to measure these resistors *while they are connected in the circuit.* You will have to apply some skill to take the potentiometer out of the circuit. Safest is to plug it into another blank area of your breadboard and use little probe wires to measure the resistor divider values. Of course, don't forget to put it back correctly in the circuit without changing the value!
This is a general principle of practical electronics – if you try to measure values of components like resistors with a DMM while they are connected in the circuit, you will end up measuring the value in parallel with all the other nearby (and sometimes far away) circuit nodes. You may find out later in life that this makes it very difficult to debug fully assembled complex PCB's with many components of which one or two may have malfunctioned.

2.1.C) OUTPUT DEMO **10**

Probe v_{out} of your amplifier circuit. With effectively infinite impedance of your DSO probe, you should get close to the simulated voltage gain from $v_{in} = \pm 0.3$V
Put a photo of your circuit (with ID) and a DSO measurement of v_{out} highlighting the measured amplitude of v_{out} and hence the measured voltage gain





The DSO readings give
This means $v_{out} \sim \pm 2.5V$
The input measured $v_{in} \sim \pm 0.27V$

$$\therefore G_v = -9.25$$

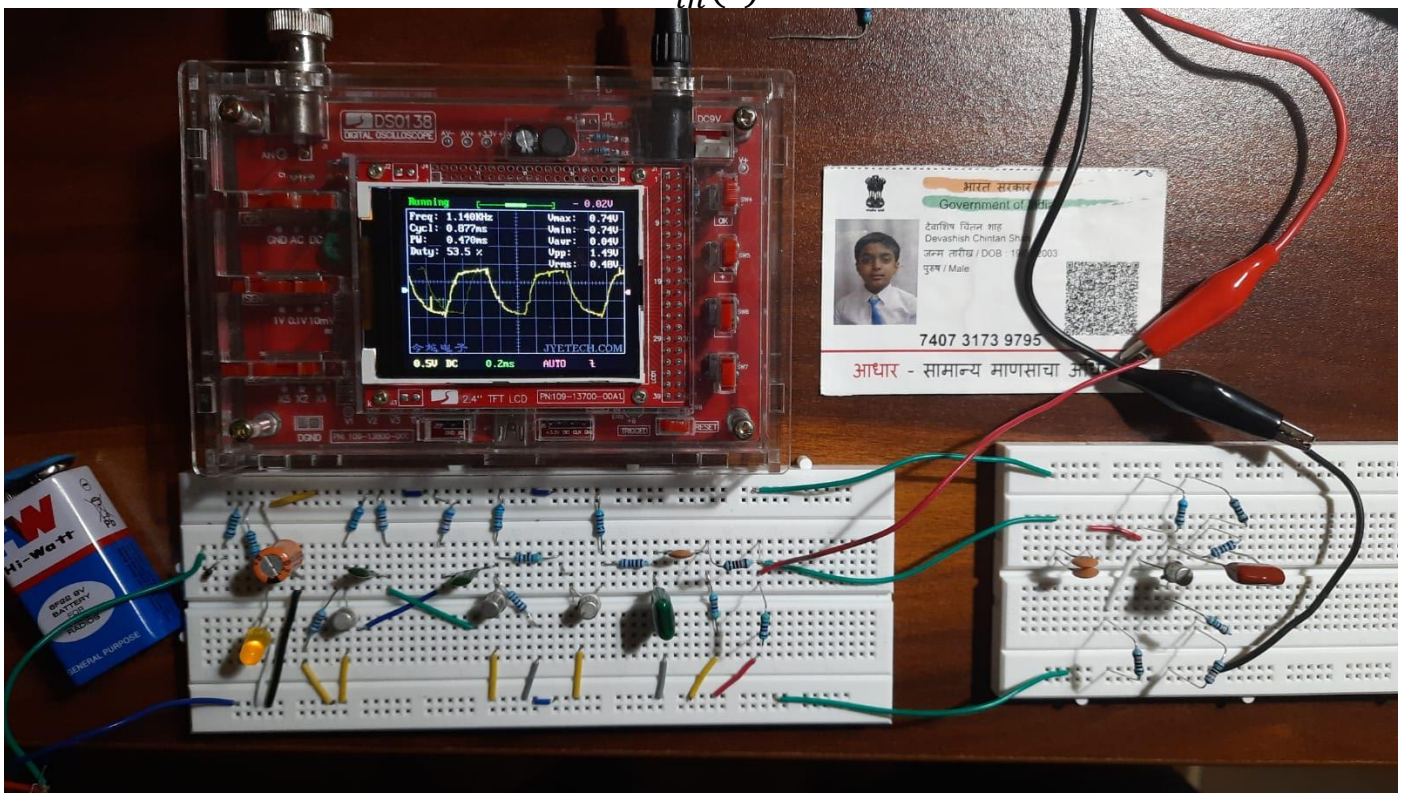
Level 3: Explore limits of voltage amplification 10

With v_{in}=±0.3V swing, you can see that the amplification is (mostly) linear and fixed except for some artifacts near the extremes. Thus the amplifier is able to amplify any v_{in} in the range 0 – ±0.3V

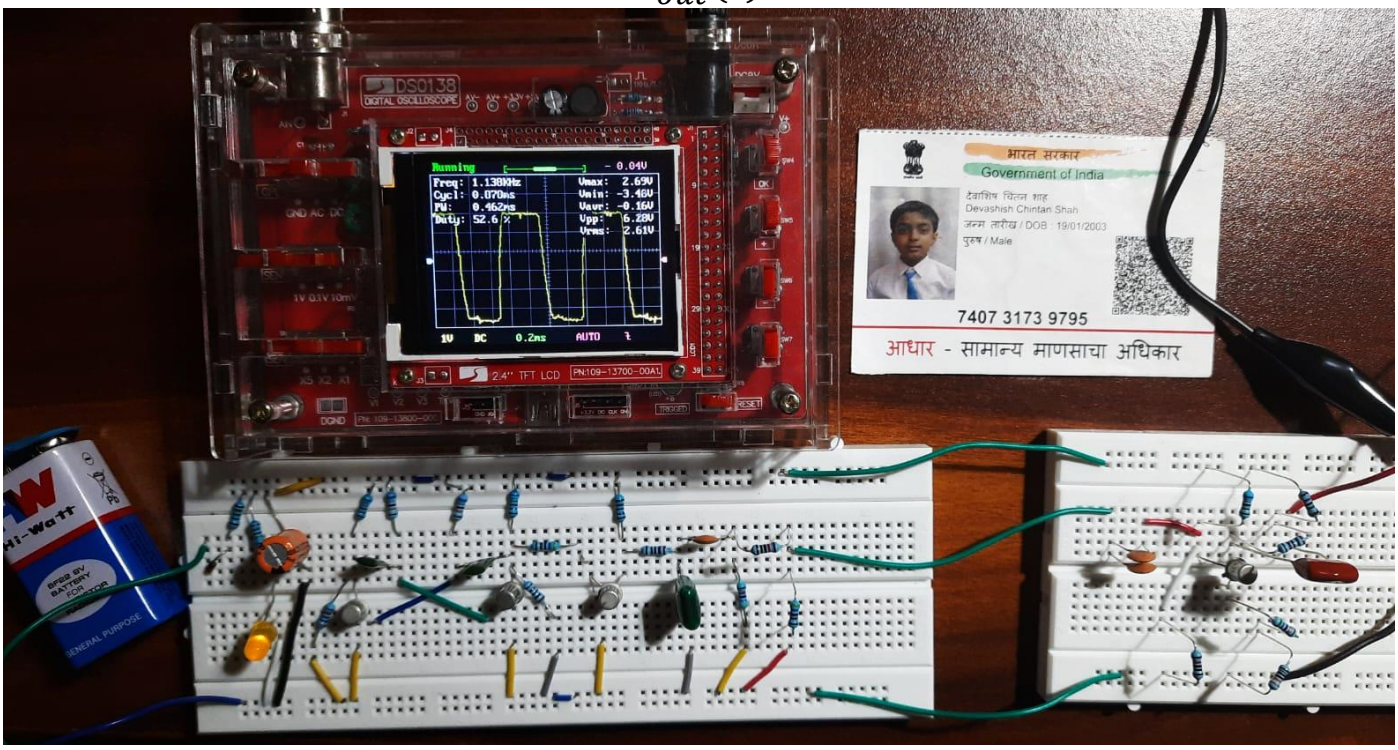
Increase v_{in} to higher values by adjusting the potentiometer of the FG.
Put a photo of your measurements here when you see deviation from linear gain.
Make a note of what is the value of v_{in} swing when v_{out} does not show a smooth amplified sawtooth waveform, but flattened edges near the extremities. Is the flattening present at both positive and negative extremities of v_{out}? **5**

For $v_{in} \sim \pm 0.74V$ there are prominent non-linearities observed in v_{out}.
The flattening is present for both, positive and negative extremes of v_{out}.
The sawtooth waveform which we obtained earlier now seems to be clipped at the extremities of v_{out}.

$v_{in}(t)$

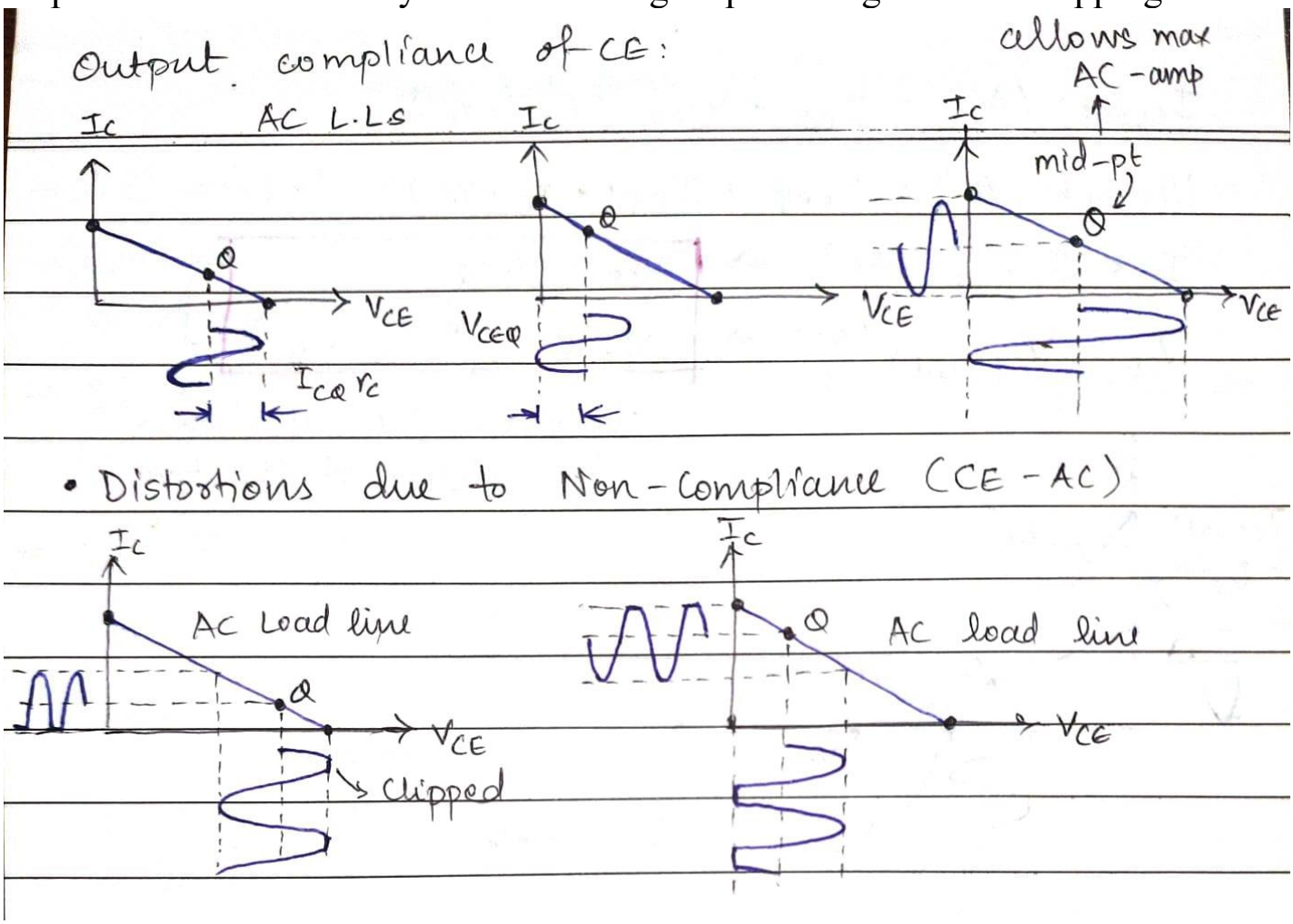

DS0138
DIGITAL OSCILLOSCOPE
Running
Freq: 1.140KHz
Cycl: 0.877ms
PW: 0.470ms
Duty: 53.5 %
Vmax: 0.74V
Vmin: -0.74V
Vavr: 0.04V
Vpp: 1.49V
Vrms: 0.48V
0.5V DC 0.2ms AUTO
2.4" TFT LCD
JYETECH.COM
भारत सरकार
Government of India
Devashish Chintan Shah
जन्म तारीख / DOB : 19/01/2003
पुरुष / Male
7407 3173 9795
आधार - सामान्य माणसाचा अधिकार

$v_{out}(t)$:


DS0138
DIGITAL OSCILLOSCOPE
Running
Freq: 1.138KHz
Cycl: 0.070ms
PW: 0.462ms
Duty: 52.6 %
Vmax: 2.69V
Vmin: -3.48V
Vavr: -0.16V
Vpp: 6.28V
Vrms: 2.61V
1V DC 0.2ms AUTO
2.4" TFT LCD
भारत सरकार
Government of India
Devashish Chintan Shah
जन्म तारीख / DOB : 19/01/2003
पुरुष / Male
7407 3173 9795
आधार - सामान्य माणसाचा अधिकार

Provide quantitative explanation of why you see a deviation from linear gain **5**

The clipping occurs because the transistor is driven out of the forward active region. Given below is a simple graphical analysis of the AC load line for a CE amplifier which intuitively shows how large input voltages lead to clipping.



Quantitatively the compliance is calculated as follows:
(notation: for any quantity X; $X_Q \equiv DC\ value, x \equiv AC\ value, X \equiv X_Q + x$)

AC loal line (by Kirchhoff's law): $I_C = I_{CQ} + \frac{V_{CEQ} - V_{CE}}{R_C}$

$$I_{C|sat} = I_{CQ} + \frac{V_{CEQ}}{R_C}\ and\ V_{CE|cutoff} = V_{CEQ} + I_{CQ}R_C$$

For active amplification without clipping, we require:

$$V_{CE} < V_{CE|cut} \Rightarrow v_{ce} < I_{CQ}R_C$$

And

$$I_C < I_{C|sat} \Rightarrow i_c < \frac{V_{CEQ}}{R_C}$$

The stronger of the two constraints must be satisfied at all times.