Lab 2.1: Analysis of NPN Astable Multivibrator

100 marks

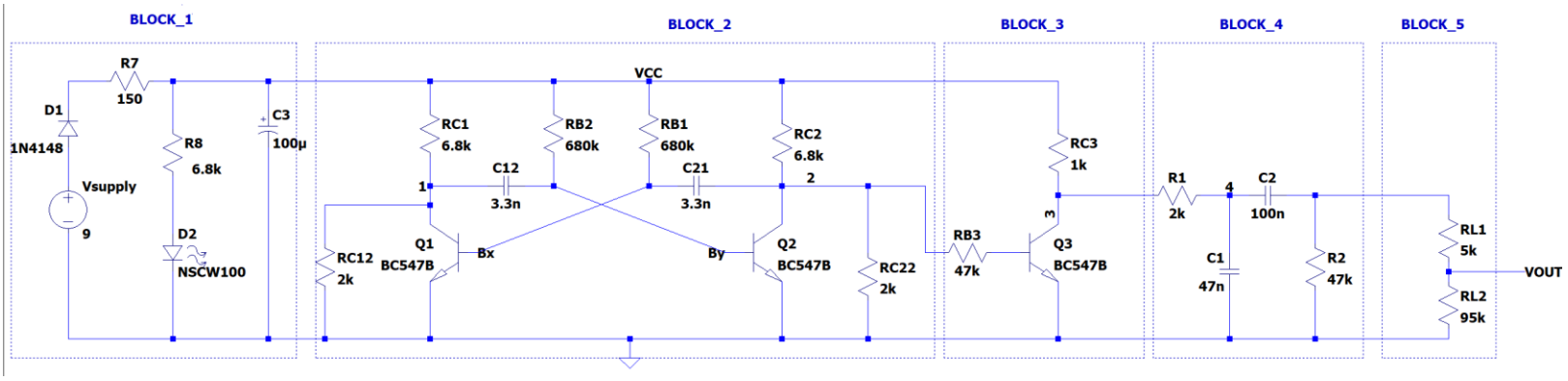
Edit the header above to insert your Rollnumber and Name.
Solution must be submitted on Moodle as a PDF file. Use 'File→Export'
All the questions in this file are in blue font. Please type in your answers in BLACK font to make your submission easy to grade

Objective: At the end of this lab assignment, you will:
Analyze all circuit blocks and limitations of the Astable Multivibrator square wave generator circuit built in Lab 1. You will thus be ready to build it on breadboard with supplied components.

CONTEXT:

Combining best aspects of all the solutions submitted for Lab 1, we have made the 'reference' design shown in Fig 1 for a function generator.
'Function' in circuit jargon usually means a Voltage that is changing as a function of time. A desktop instrument called '**A**rbitrary **F**unction **G**enerator' (AFG) produces a function of any desired shape (square, sine, triangle, sawtooth etc) by pressing a few control panel buttons. The following circuit design provides some of that functionality – enough to allow us to do future experiments in PH231+PH233.

Fig 1: "Reference" design for a function generator. LTSpice `.asc` file is given



In the following questions we ask you to analyze the function and limitations of each of the 'blocks' enclosed within the rectangles in Fig 1

Question 0: Block level functions **10**

Study the diagram of Fig 1 and explain in one sentence the function of each of the blocks labelled in the diagram. We are just looking for an overview explanation in this question – detailed questions on each block follow.

[2 marks each]

BLOCK 1:

Answer: Block-1 acts as a stable DC-Voltage source, like an adapter with ON/OFF indication LED. It ensures that a unidirectional, stable DC voltage is fed to block-2. This block reduces any fluctuations or distortions in the input.

BLOCK 2:

Answer: The second block is an Astable Multivibrator which generates feeds a square wave biasing voltage to the base of Q-3. The various parameter values can be tweaked in order to get desired duty cycle and frequency of the square wave.

BLOCK 3:

Answer: The third block is like a buffer which reduces distortions due to block-4 on the square wave output of block-2. It essentially disconnects block-2 and block-4. It also amplifies the signal fed at the base of Q-3 and changes its phase by 180°.

BLOCK 4:

Answer: The fourth block is a passive band pass filter. It allows a certain band (band values depend on the R and C values) of frequencies to pass and reduces amplitude of all others. It sets the average value of output voltage to 0V.

BLOCK 5:

Answer: The block 5 is a voltage divider. It is just an easy practical way of reducing the effect of loading by adding a large resistor in series with the load thus increasing effective output resistance with minimal loss in amplitude of $V_{out|max}$ and giving the desired fraction of this as output V_{out}.

Question 1: BLOCK_1 Detailed analysis **20**

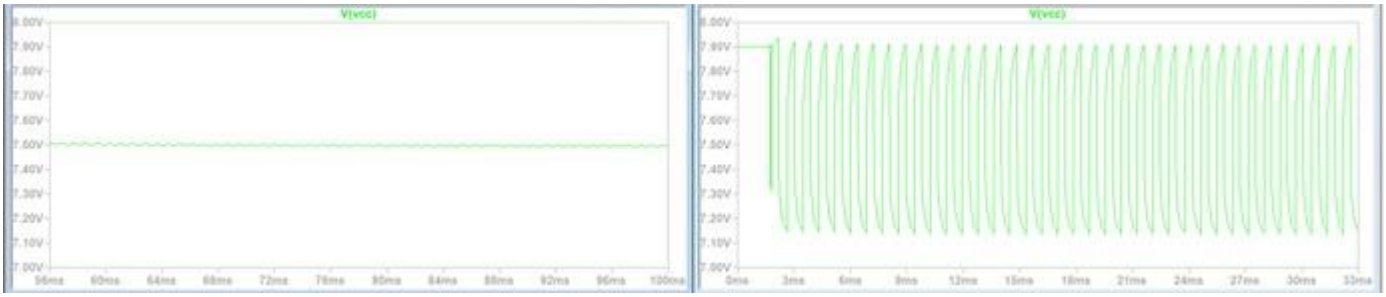
Block 1 obviously provides power to the rest of the circuit.
A power source is a unit which provides a specified voltage and current to the load.
In this case, Block 1 provides 9V to the load. Whether it acts as voltage source, or a current source depends on its internal series resistance.

2.1) Identify component functions.

What is the function of the following components included in Block 1?

D1: Block-1 is a DC source which means that any reverse flow of current is undesirable. D1 is acts like a one-way DC valve, preventing any damage by reverse voltages to the rest of the circuit. Diode acts nearly like a open switch if reverse biased.
R7: R7 prevents excess flow of current thus keeping capacitor C3 from shorting on connecting the voltage source.
R8: R8 serves the purpose of restricting current flow through the LED.
D2 (LED): LED acts as an ON/OFF indicator. If the source circuit is connected properly it lights up.
C3: The capacitor stabilizes by suppressing any fluctuations due to the external block or the source itself the DC output of block-1. In absence of C3 the output of voltage undergoes oscillations of significant magnitude about the mean value of 7.51V due to effects of block-2,3,4. The magnitude of fluctuations observed with C3 are $\simeq$0.02V whereas it is of the order $\simeq$0.4V if C3 is removed.
Below is a simple LTSpice simulation with the whole circuit unchanged except removal of C3 in the image on the right.

With C3 v/s Without C3

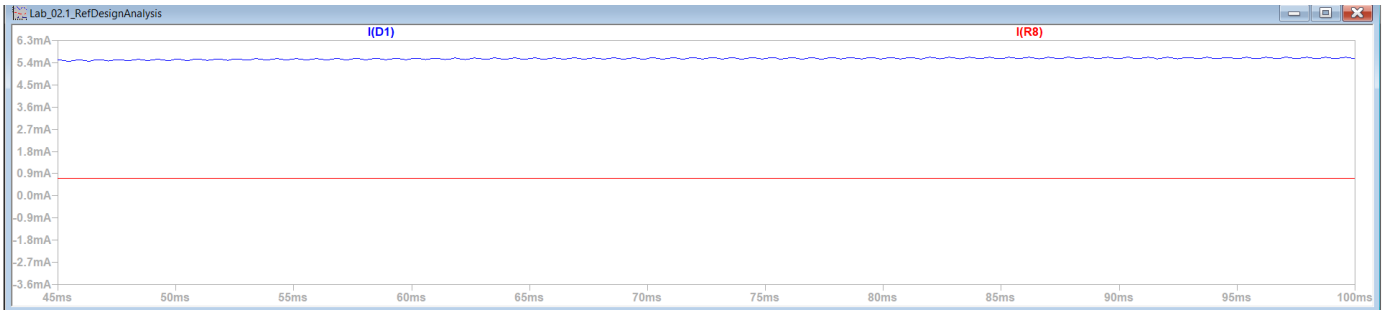


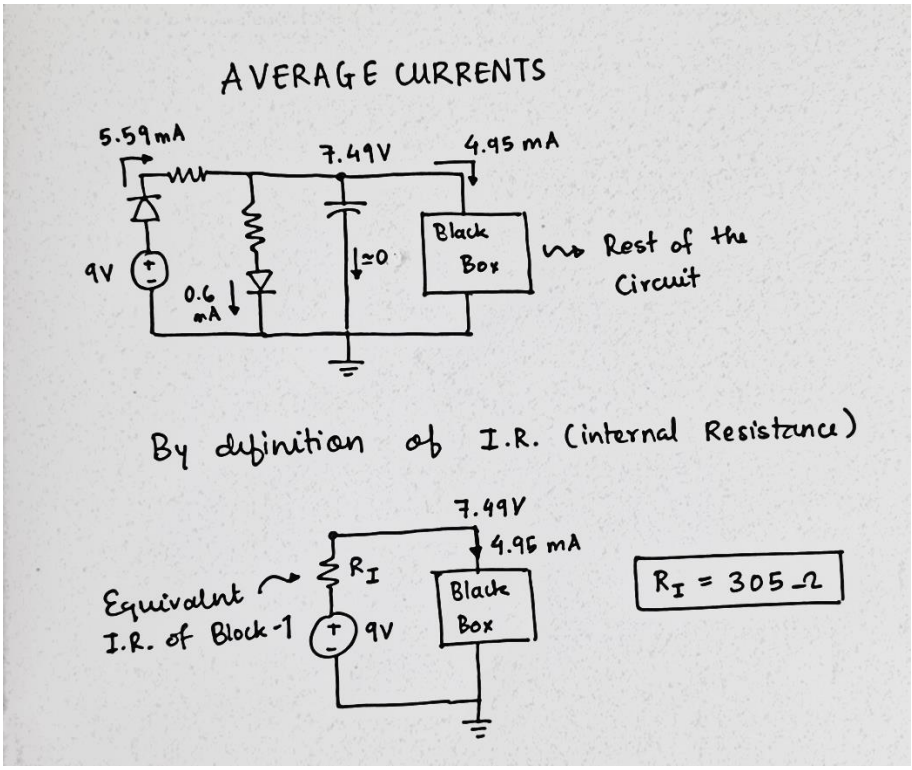
2.2) What is the effective internal series resistance of Block 1? Does this make Block 1 a voltage source or a current source?

One could simply isolate block-1 and as it reaches steady state the capacitor can be thought of as an open switch. Block-1 is a Voltage source with relatively small internal resistance and output current is small since the other blocks have large effective resistance compared to block-1. The above assumptions are wrong, they might simplify the matter but give highly inaccurate answers.

This is because diode resistances depend on the current flowing through them which in turn depends on the output blocks. Also, the assumption that the output current is small is observed to be wrong. We use simulations from LTSpice to find average values of currents through branches of block-1 and the average output current and apply the definition of internal resistance.

Average current through C3=0. From the simulation it is clear that I_{out}=I(D1)-I(R8) is significant.



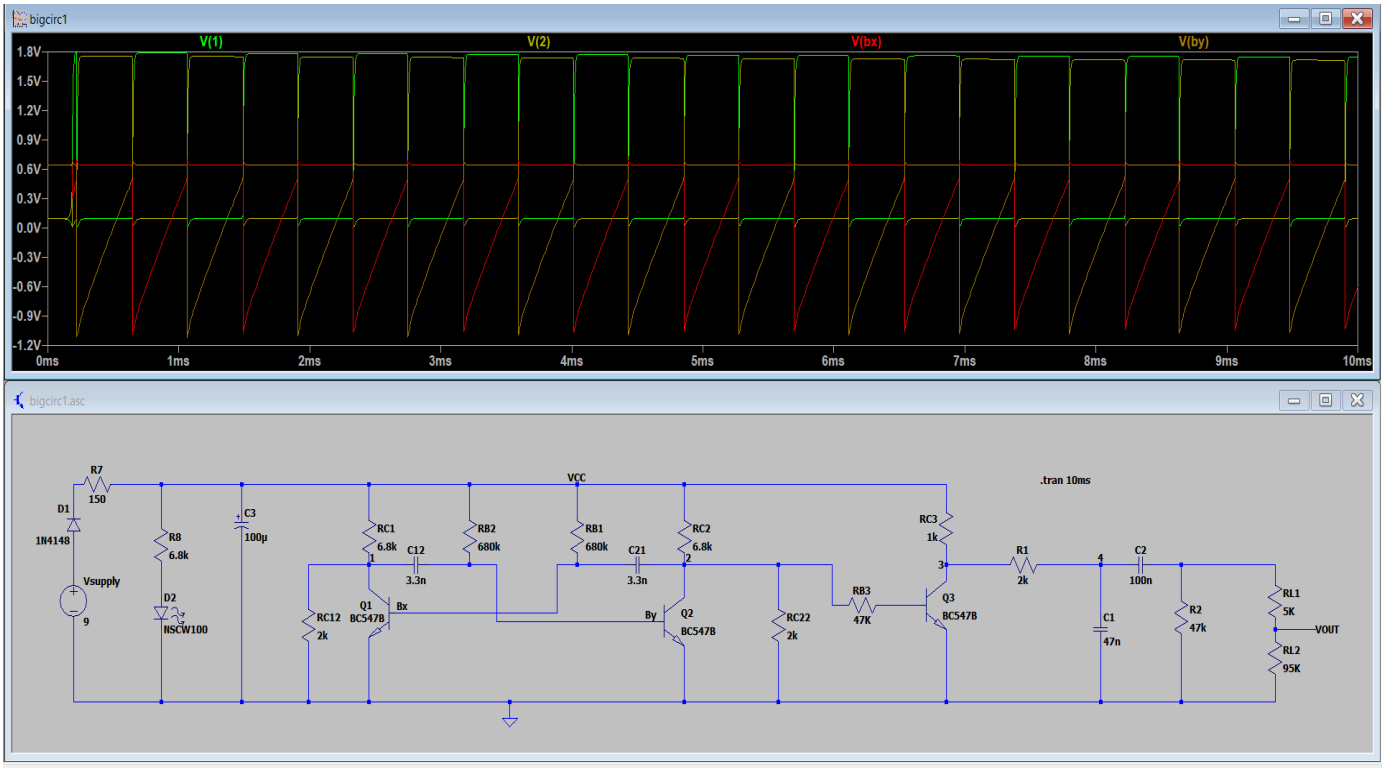


Question 2: BLOCK_2 Detailed analysis **10**

Block 2 is the Astable multivibrator function generator with two NPN BJT's we have worked out in Lab 1. It is expected to produce a 1kHz square wave form switching between 0V and 9V.

But look carefully! Two resistors RC12 and RC22 of 2kΩ have been added in Fig 1.

Explain with equations, what is the function of RC12 and RC22 in BLOCK_2 – why have they been added to this design?



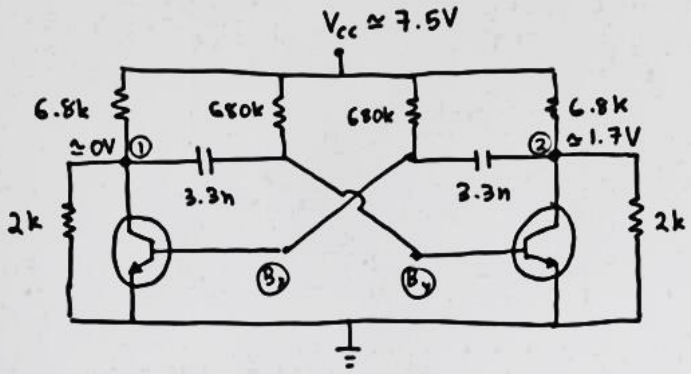
Here in Green-V(1)-Collector of Q-1, Yellow-V(2)-Collector of Q-2, Red-V(Bx)-Base of Q-1 and Brown-V(By)-Base of Q-2.

The Astable Multivibrator toggles between two states (State-1 being Q-2 in cutoff, Q-1 in saturation and State-2 being the other way round) as discussed in lab 1. Here, due to the near perfect symmetry in the values of various components and the very high resistance R_{B3} compared to R_{C22} and R_{C12} analysis of one of the states is enough. Since $R_{B3}>>R_{C22}$ we don't have to worry about excess current being drawn by block-4.

We first analyze state-1.

We analyze loaded circuit state by state.

State - ① Output is High :



Note: Ideal Calculated $V_{out} = 1.7V$, which is acceptable since the real $V_{out(obs)} \simeq 1.75V$.

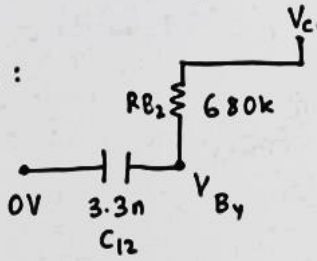
⇒ We can Go ahead with the Calculations.

$$V_{out(max)} = V_{cc} * \frac{R_L}{R_{c_2} + R_L} = \boxed{1.7V}$$

When Q-2 is Cut-off B_y drops down to $-V_{out(max)} + 0.7$ This is because when Q-2 was in saturation $V_{①}$ was $V_{out(max)}$ and V_{B_y} was 0.7V. (discussed in Lab-1 in detail)

∴ Time period of state 1 T_1 = time taken by V_{B_y} to rise from $(-V_{out(max)} + 0.7 \simeq -1V)$ to $(+0.7V)$.

We need to analyze:



$$q(0) = (-V_{out(max)} + 0.7) \times C_{12}$$

$$q(T_1) = (0.7) \times C_{12}$$

$$V_{cc} - \frac{dq}{dt} R_{B_2} - \frac{q}{C_{12}} = 0$$

$$\Rightarrow \int_0^{T_1} \frac{dt}{C_{12} R_{B_2}} = \int_{q(0)}^{q(T_1)} \frac{dq}{(7.5 C_{12} - q)} = -\ln\left[\frac{7.5 C_{12} - q(T_1)}{7.5 C_{12} - q(0)}\right] = -\ln\left[\frac{6.8}{8.5}\right]$$

$$\boxed{T_1 = 0.223 R_{B_2} C_{12}}$$

$$T_1 \simeq -\ln\left[\frac{V_{cc} - V_{BE}}{V_{cc} - V_{BE} + V_{out\,(max)}}\right] R_{B2} C_{12}$$

$$T_1 = \ln\left[1 + \frac{V_{cc}}{V_{cc} - V_{BE}}\left(\frac{R_{C12}}{R_{C1} + R_{C12}}\right)\right]$$

The above analysis gives $T_1 = 0.223\, R_{B2}C_{12} = 0.5\, ms$ which is within acceptable bounds of the observed value of $T_1 \simeq 0.46\, ms$.
As stated earlier we need not analyze much further because symmetry demands that the time period in state-2 be, $T_2 = 0.223\, R_{B1}C_{21} = 0.5\, ms$.

Need of R_{C12} and R_{C22}:

- The time periods T_1 and T_2 depend on $V_{out(max)}$ which depends on these resistors. These resistors, thus play a role in setting the desired frequency of oscillation.
- When Q-3 operates in the active region the potential difference across the base resistor is $R_{B3} = V_{out(max)} - 0.7V$. In absence of these resistors the $V_{out(max)}$ fed to the base of resistor of transistor Q-3 (block-4) is $V_{CC} \simeq 7.5V$ itself, this high base voltage would drive it to saturation.
- Thus, the function of this resistor is to prevent Q-3 from reaching saturation, allowing it to perform its function of disconnecting blocks 2 and 4 in the active region.

Question 3: BLOCK_3 Detailed analysis **20**

Block 3 is connected as the load to Block 2. Notice that Block 3 is an **active** circuit. By **active** circuit we mean the block consumes power from the source, and has its own input-output relationship.
So in principle, Block 3 can function as an independent unit irrespective of the presence of the other blocks. It has an input signal applied to RB3. Let's name it's input signal $V_{in|block3}$. The output $V_{out|block3}$ is the voltage at the Collector terminal of Q3

3.1) DC analysis: If $V_{in|block3}$ and $V_{out|block3}$ are unconnected, what are junction bias voltages C-B and B-E of Q3?

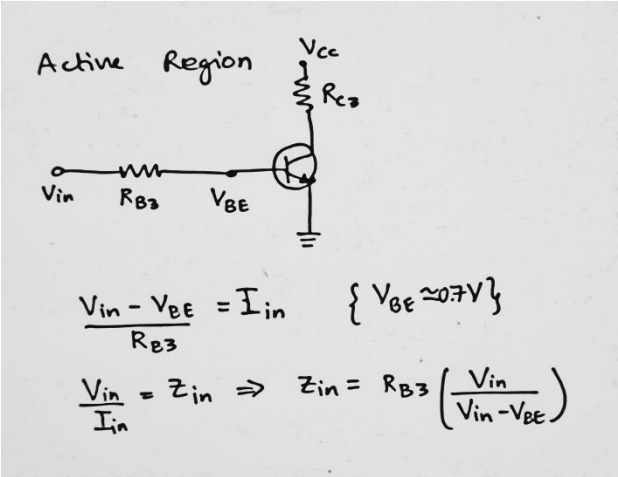
Disconnecting $V_{in|block3}$ and $V_{out|block3}$ the DC operating point on LTSpice gives C-B bias voltage to be equal to 7.9V and B-E is approximately 0.2V.

3.2) Operation point of Q3: Accordingly, is Q3 in saturation/active/cut-off mode?

Q3 is in cutoff.

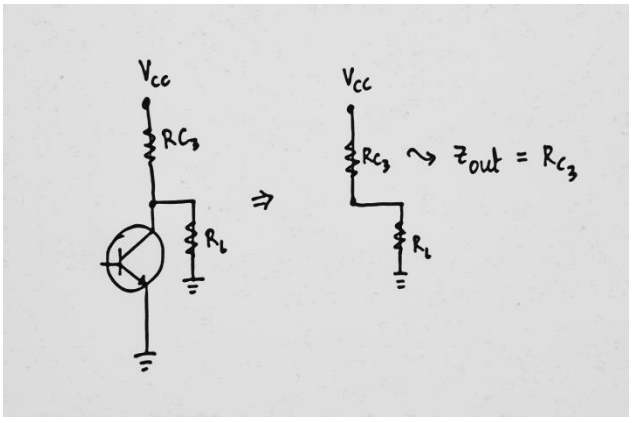
3.3) Input impedance: When $V_{in|block3}$ is connected, use KVL, KCL to determine what is the input impedance of Block 3?

$$Z_{in} = R_{B3}\left(\frac{V_{in}}{V_{in} - V_{BE}}\right)$$



3.4) Output impedance: Similarly, when $V_{out|block3}$ is connected, for simplicity, to some fixed load R_L what is the output impedance of Block 3? Detailed analysis of its connection to Block 4 is analyzed in the next question.

$Z_{out}=R_{C3.}$



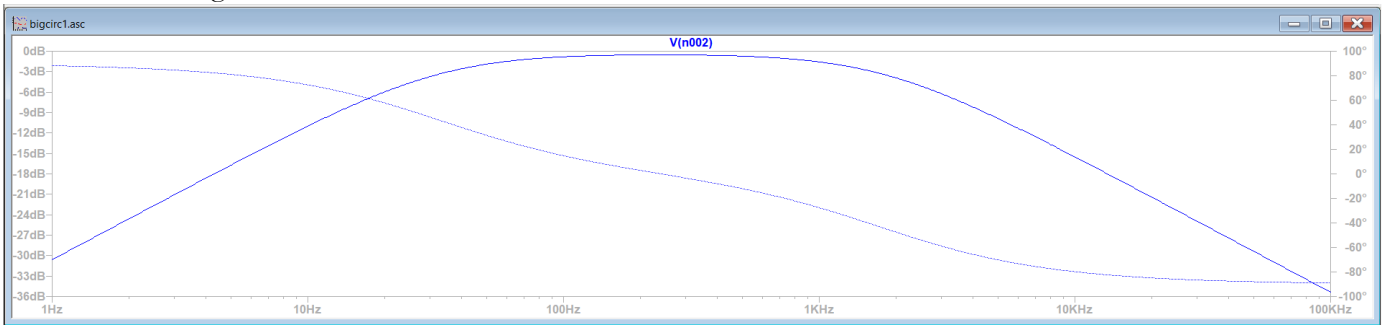
Question 4: BLOCK_4 **20**

Block 4 seems to have a very familiar circuit arrangement, resistor capacitor pair of R1, C1 and C2,R1 are cascaded together.

4.1) Frequency domain analysis: **5**

Perform a frequency domain analysis of Block 4. Put a plot of your LTSpice simulation result for magnitude and phase relationship between $V_{out|block4}$ and $V_{in|block4}$

Note: axes are logarithmic scales



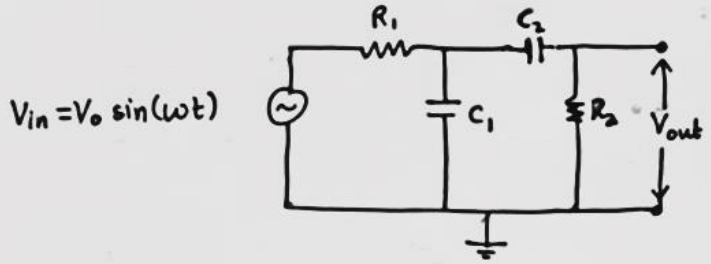
Here, the solid blue line is the Voltage gain $A_v = \frac{V_{out}}{V_{in}}$ in decibel scale. The dotted line is the phase offset of the output w.r.t. the input. For very small frequencies phase difference is $\phi \sim 90\dot{}$ (output leads) which falls to $\phi \sim -90\dot{}$ (output lags) for very large frequencies.

We now analyze Block-4 for a single sinusoidal input of angular frequency $\omega = 2\pi f$.

The reactance of a capacitor then becomes $X_C = \frac{1}{i\omega C}$ where $i = \sqrt{-1}$.

The complex Voltage gain accounts for the magnitude as well as the phase offset between input and output.

for Sinusoidal Input of one freq



$$X_1 = \frac{1}{i\omega C_1}, \quad i = \sqrt{-1}$$

$$X_2 = \frac{1}{i\omega C_2}$$

$$Z = \left[(R_2 + X_2) \,||\, X_1\right] + R_1$$

$$= \left[\frac{i\omega C_2 R_2 + 1}{i\omega C_2} \,||\, \frac{1}{i\omega C_1}\right] + R_1$$

$$= \frac{\left[\frac{1}{\omega^2 C_1 C_2}(i\omega C_2 R_2 + 1)\right]}{\left[\frac{-1\omega^2 C_1 C_2 R_2 + i\omega C_1 + i\omega C_2}{i \cdot i\omega^2 C_1 C_2}\right]} + R_1$$

$$Z(\omega) = \frac{i\omega(C_2R_2 + C_1R_1 + C_2R_1) + (1 - \omega^2 C_1 C_2 R_1 R_2)}{i\omega(C_1 + C_2) - \omega^2 C_1 C_2 R_2}$$

$$\therefore \frac{V_{out}}{V_{in}} = \left(\frac{R_2}{X_2 + R_2}\right) \cdot \frac{\left((X_2 + R_2) \,||\, X_1\right)}{\left(R_1 + (X_2 + R_2) \,||\, X_1\right)}$$

$$A_v = \frac{i\omega R_2 C_2}{(1 - \omega^2 C_1 C_2 R_1 R_2) + i\omega(C_2 R_2 + C_1 R_1 + C_2 R_1)}$$

4.2) Time domain analysis: 5

From earlier Block 3, if a 1kHz square voltage waveform is fed in as $V_{in|block4}$, what is the expected $V_{out|block4}$? Note carefully any change in the magnitude and phase between $V_{out|block4}$ and $V_{in|block4}$

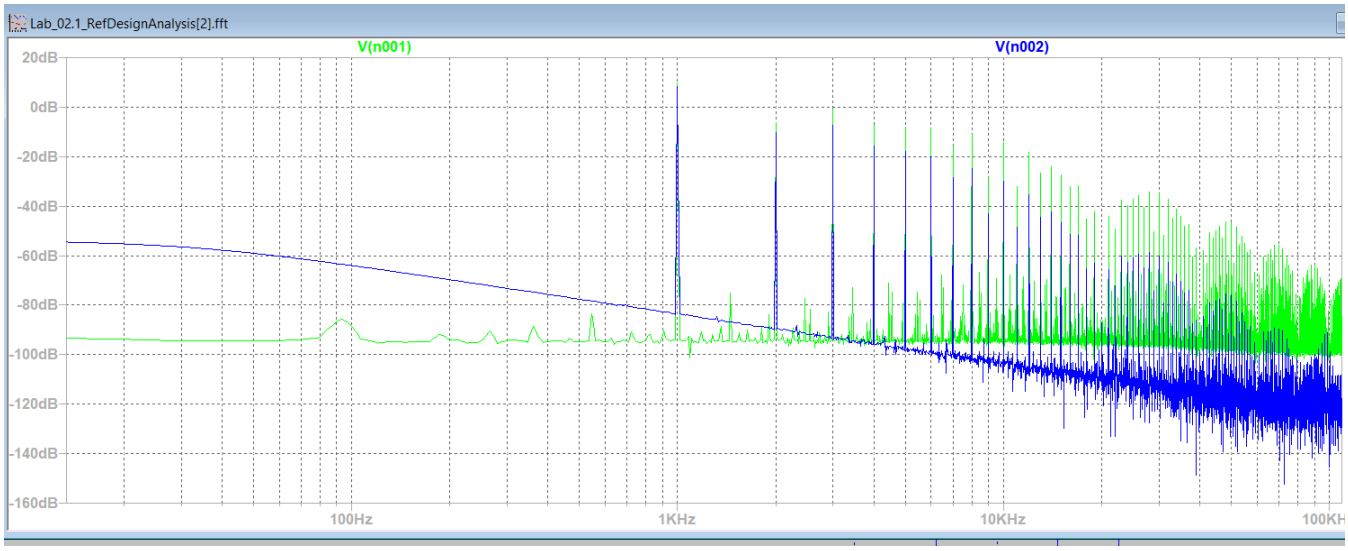
The analysis done so far was for sinusoidal input of a single frequency. To understand the behavior for a square wave input we need to use Fourier's theorem. The square wave input can be formed by superposition of infinite sinusoids with respective amplitude functions. Taking into account the Voltage gain and the phase offset worked out in Q.4.1 one can perform brute force numerical integration using formulae derived in Q.4.1 to get the output voltage.

$$V_{in} = \int_0^\infty B_{in}(f)\,\sin(2\pi f t)\,df$$

$$V_{out} = \int_0^\infty B_{out}(f)\,\sin\big(2\pi f t + \phi(f)\big)\,df$$

Here, $B(f)$ is the amplitude (contribution) of sinusoidal wave of frequency f.
Since the filter attenuates frequencies outside the pass band significantly the final output has lesser peak-to-peak voltage value as expected. Also, the square wave input is smoothened out due to this and the phase offsets.

But there are several more insightful and practical methods to study the nature of the output voltage. FTT feature of LTSpice being one of them. It plots the contribution of various frequency components of the input (green) and the output (blue) wave using a logarithmic scale. The highest peak is at 1kHz as expected (since that is the frequency of the voltages), peaks get much lower for higher frequencies because the band pass filter attenuates these higher values.



4.3) Impedance matching:

For good power transfer between blocks, it is desirable that the output impedance of the sending block matches the input impedance of the receiving block.

Evaluate the input impedance of Block 4. **5**

The receiving impedance of block-4 for a sinusoid of particular frequency f has been derived in Q.4.1. But since our input wave is a superposition of such sinusoids, we apply Fourier transform to obtain the effective impedance Z with amplitude C(f).

$$Z = \int_0^\infty C(f)\, \mathrm{Z(f)} df$$

Numerical integration is one way. Another reasonable method is to calculate the lower bound for the total impedance as being equal to the impedance for the highest contributing peak frequency which is 1kHz. The impedance comes out to be of the order $\sim 10k\Omega$.

Does it match the output impedance of Block 3 calculated earlier? What parameters will you tweak to achieve good impedance matching? **5**

It doesn't match the output impedance of block-3. One way is to tweak the capacitor and resistor values of block-4 such that the frequency response is unaltered but impedance decreases. The output impedance of block-3 can be increased by simply adding resistors between the two blocks.

Question 5: BLOCK 5 **20**

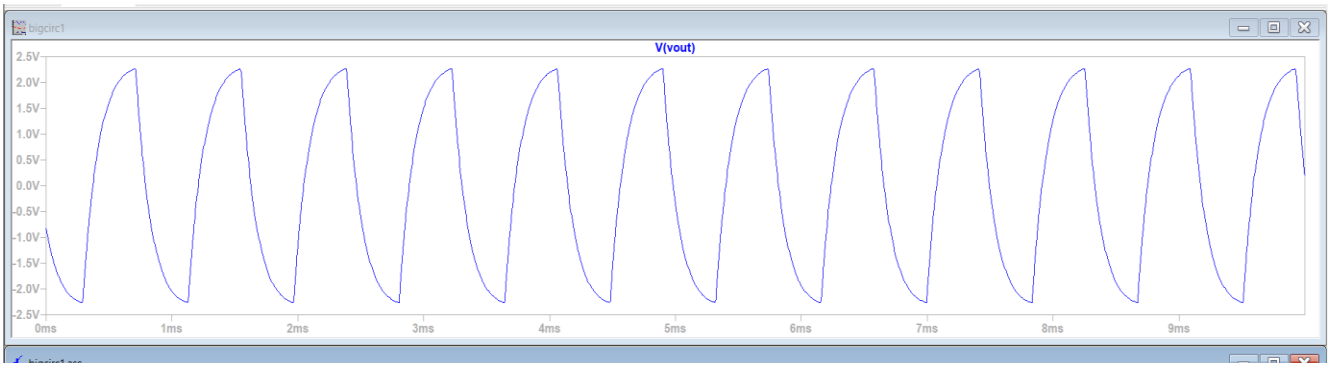
5.1) Block 5 is a simple resistor divider interfacing Block 4 to the final load on the function generator, and provides the final VOUT of the function generator.
We have shown the total resistance of this resistor divider to be 100kΩ.

Why have we chosen the value RL1+RL2 = 100kΩ so large? **2**

Large resistor values ensure near ideal behavior. Small load resistor values drastically impact the magnitude as well as the nature of the output of block-4. If we had used small resistors the frequency and time domain analysis in Q4 would have been rendered useless since the loaded circuit would have large deviations from the ideal-unloaded case.

5.2) Range of VOUT practically obtained: Perform the end-to-end simulation connecting all the blocks sequentially. What is the magnitude of VOUT(t) obtained for the shown divider ratio 5kΩ:95kΩ? Put your LTSpice result here. Try a few different values. If the maximum amplitude of VOUT that can be obtained is $V_{OUT|max}$, calculate 3 values of the ratio RL1:RL2 such that you are able to obtain VOUT of magnitudes $0.75V_{OUT|max}$, $0.5V_{OUT|max}$, $0.25V_{OUT|max}$ Verify that your calculation matches the simulation result. **4** Save these values for future reference. We will be using this circuit as the function generator voltage input for all future experiments.

The peak-to-peak value of V_{out} for the voltage divider $5k\Omega: 95k\Omega$ is measured to be 4.53V.



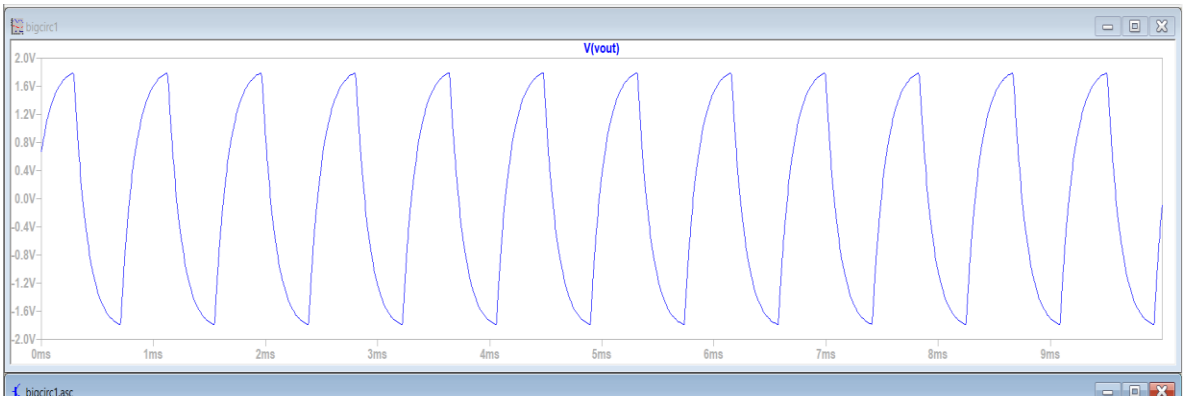
$V_{out|max}=V_{out}((R_{L2}+R_{L1})/R_{L2})$

Thus, $V_{out} = V_{out|max}\left(\frac{R_{L2}}{R_{L2}+R_{L1}}\right) = V_{out|max}\left(\frac{1}{1+\frac{R_{L1}}{R_{L2}}}\right)$

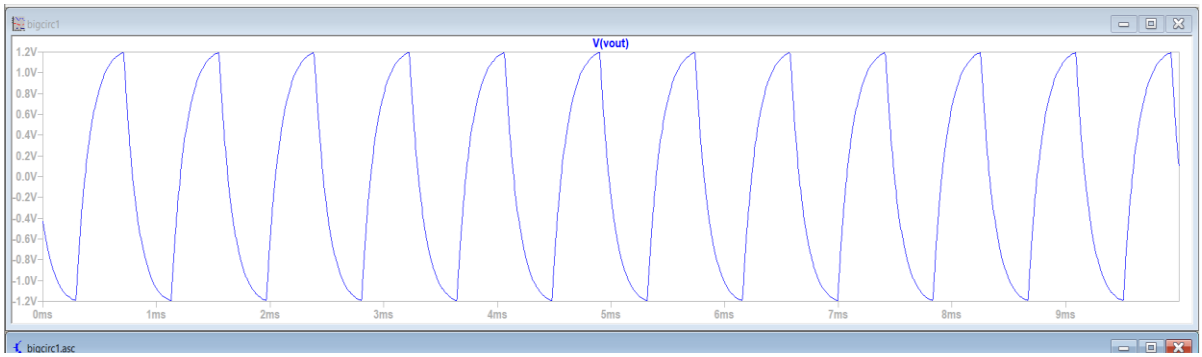
Here $V_{out|max}$ works out to be 4.78V.

For obtaining the V_{out} as different fractions of $V_{out|max}$ we adjust the ration of $\frac{R_{L1}}{R_{L2}}$.

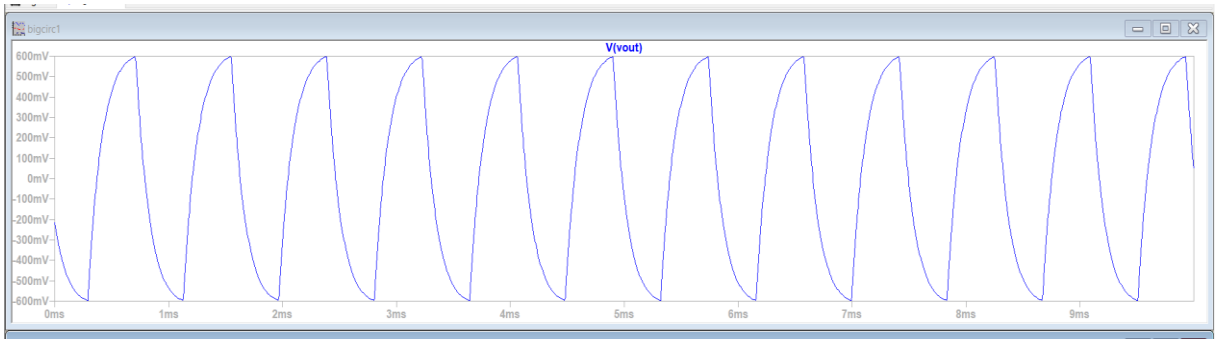
1. For $V_{out} = 0.75\, V_{out|max}$ we need $\frac{R_{L1}}{R_{L2}} = \frac{1}{3}$, $V_{peak-to-peak} = 3.65V$



2. For $V_{out} = 0.5\, V_{out|max}$ we need $\frac{R_{L1}}{R_{L2}} = \frac{1}{1}$, $V_{peak-to-peak} = 2.4V$



3. For $V_{out} = 0.25\, V_{out|max}$ we need $\frac{R_{L1}}{R_{L2}} = \frac{3}{1}$, $V_{peak-to-peak} = 1.2V$

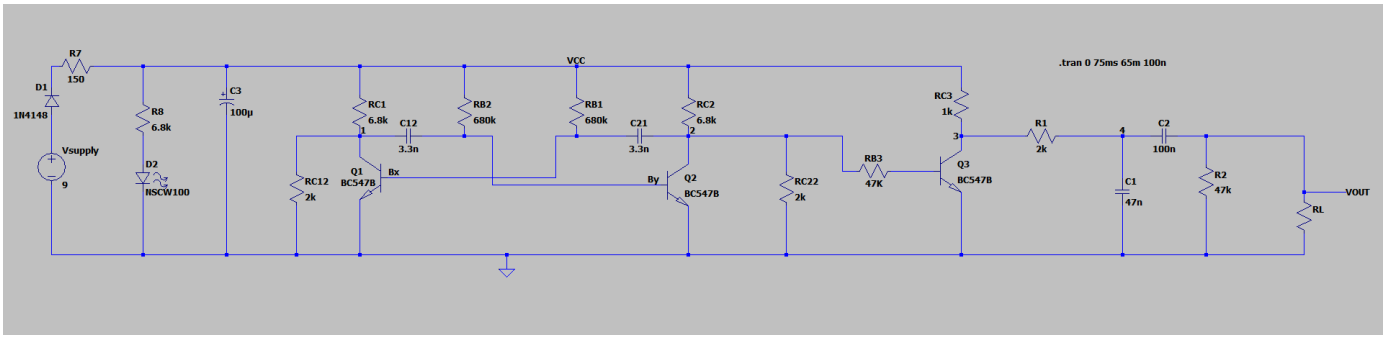


5.3) FINAL DEPENDENCE ON R_L 4

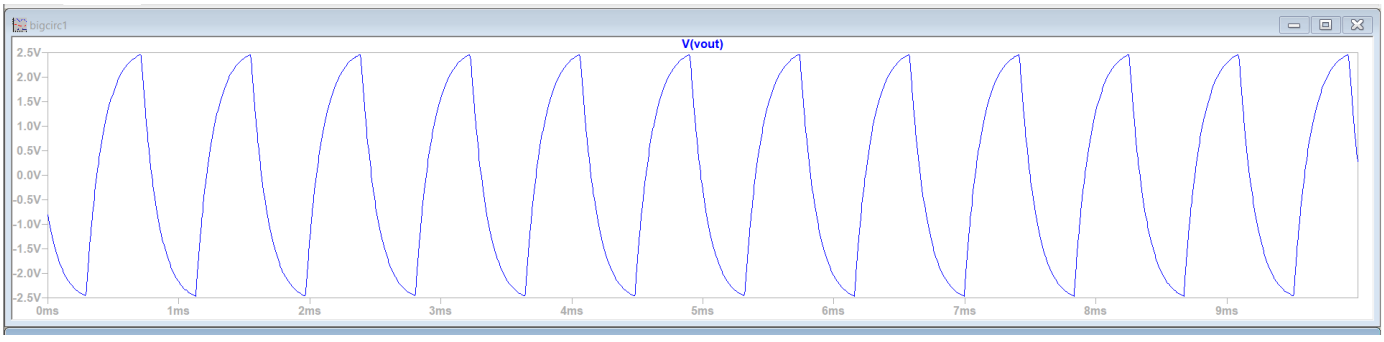
Now we have a detailed analysis of the circuit of Fig 1 consisting of 5 blocks, which should be able to robustly drive a reasonable load R_L.
Perform a simulation and show the difference in VOUT measured with no load (effectively $R_L=\infty$), load R_L = 1kΩ and R_L = 10kΩ [like we did in Lab 1]
What has improved?

QUESTION: What are the limitations on acceptable R_L values that can be reliably driven by this function generator circuit?

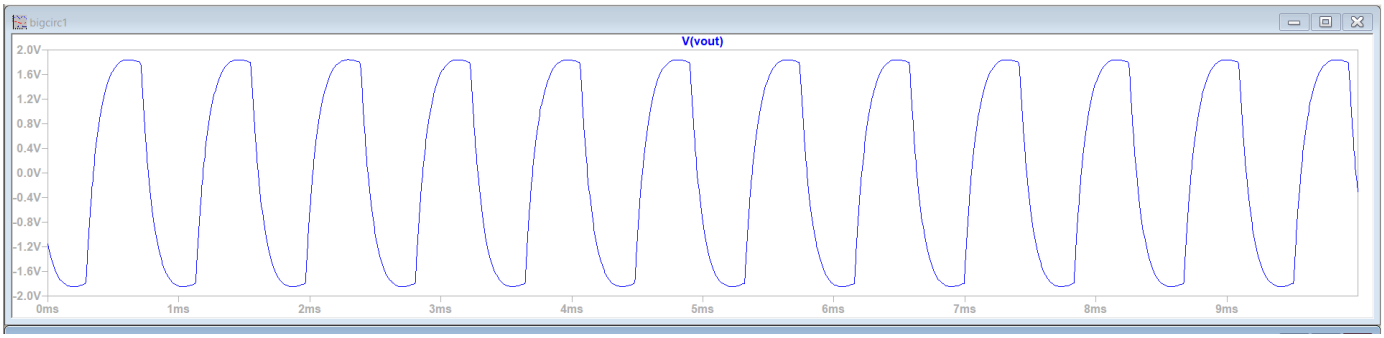
Essentially this question relates to back to analysis of the very first Block 1 in this assignment – what are the desirable characteristics of a voltage/current source? Our grand objective all along has been to design a voltage source whose output VOUT changes as a function of time as per internal circuit settings, without much dependence on the load R_L to which VOUT is connected.



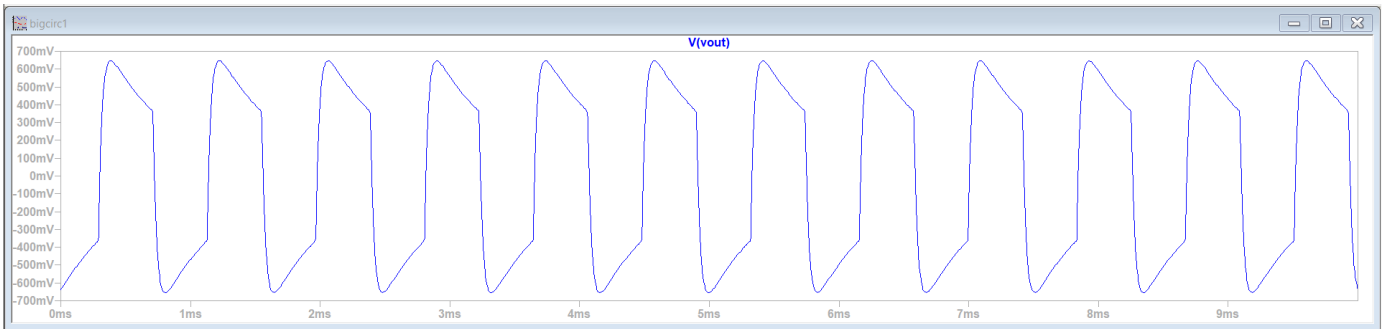
For an unloaded circuit ($R_L \to \infty$) the $V_{peak-to-peak} = 5V$



For a loaded circuit with $R_L = 10k\Omega$ the $V_{peak-to-peak} = 3.6V$ and the output waveform is much more curved.



For a loaded circuit with $R_L = 1k\Omega$ the $V_{peak-to-peak} = 1.35V$ and the output waveform is highly deformed as expected for low load resistances.



An ideal voltage source must provide a constant voltage irrespective of the loading; thus, it must have zero internal resistance. Whereas an ideal current source must have an infinite resistance which would mean that it supplies the same current value irrespective of loading.

The aim of this lab was to build a voltage source. We can define a certain minimum load required in order for the circuit to produce a significant percent of the max output. For load resistor values higher than this the circuit behaves sufficiently close to a being an ideal source. For example let's say one wants the output to be greater than 85% the max value of 5V then any load above $\simeq 21.5k\Omega$ works.

Compared to the circuit in lab-1 one prominent change in behavior upon loading is the frequency being constant. For the Astable Multivibrator built in lab-1 the load resistor dependence of frequency was high. This is certainly a very advantageous of the function generator.

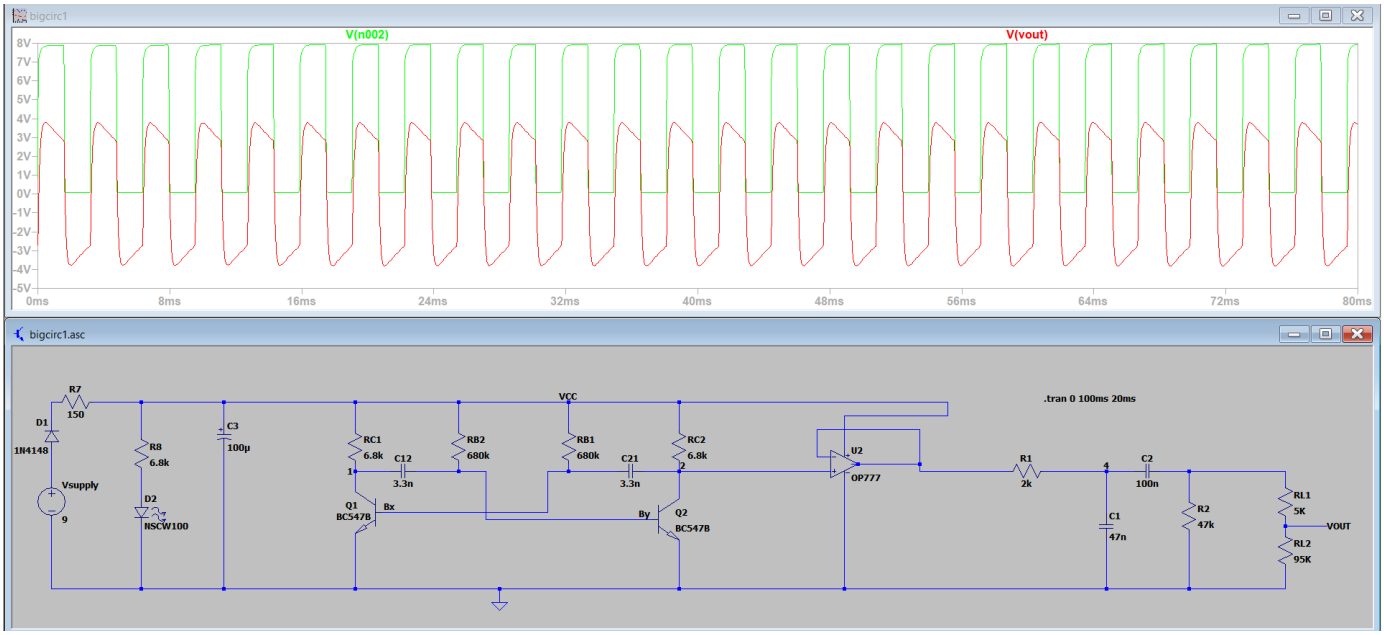
5.4) Going BEYOND the reference design **10**

We have by now fully analyzed and found the limitations of the 'reference design' of Fig 1, which we evolved starting from ideas explored in Lab 1. But this is obviously not good enough. Suggest alternative design ideas that will improve the voltage source characteristics of this function generator. You must use the same 2-BJT astable multivibrator circuit as the starting point.

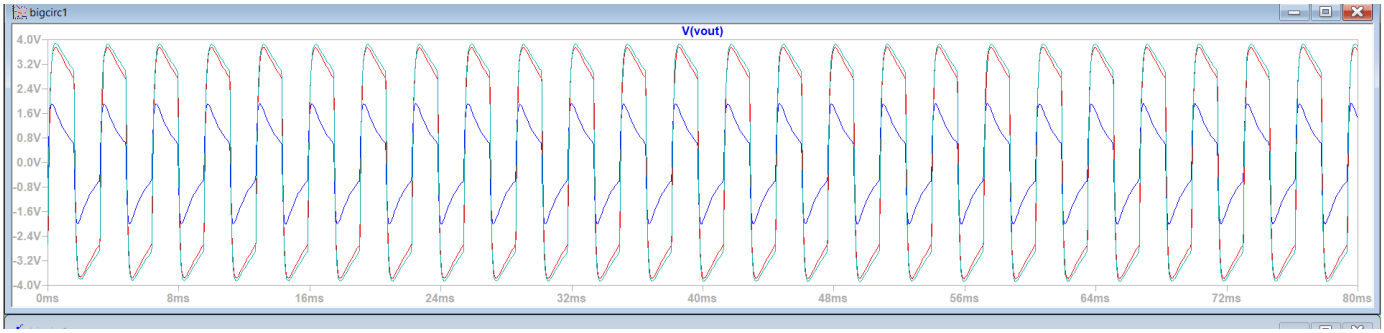
– use as much space as necessary below to explain details of your creative ideas – simply stating keywords based on looking up textbook/internet is not adequate to earn the 10 marks for this question.

An Op-Amp forms a much better buffer than a transistor. We replace block 3 by an Op-Amp unit gain buffer as shown below. Since we do not need to worry about preventing Q-3 from undergoing saturation we can remove R_{C12} and R_{C22}. We can now adjust the frequency of the square wave generated using the analysis done in lab-1.

The wave generated using this circuit is much more stable in terms of amplitude than the original circuit and is as stable in terms of operating frequency. The circuit now uses almost the complete range of voltage available (0-8V) unlike the earlier circuit which only gave maximum 5V peak-to-peak.



A simple .STEP simulation reveals the above facts about the reduced effect of loading:



The above simulation plots the output for three R_{L2} values: $5k\Omega, 80k\Omega, 155k\Omega$.

Another way to improve the circuit is to modify the block-4 circuit and cascade active high and low pass filters. This will lead to a better frequency response.