Lab 1: Design, simulate and analyze NPN transistor based oscillator 100 marks + 50 bonus

Objective: At the end of this lab assignment, you will:

1. Have a well-designed, ready to build square wave voltage waveform generator using two NPN transistors and a few selected R, C values
2. You will know what DC voltage values you must check after building the circuit to ensure that your circuit is correctly built and working
3. Know what to expect when you measure the square wave output of the oscillator with load set to:
    a. Infinity (open circuit direct probe)
    b. Terminated by a finite load resistor R_L
4. In case of discrepancies in your measurements of 3.a, have a clear idea of what component values could be the cause of discrepancies. Figure out some ideas to get around potential problems caused by 3.b

Questions are given in the following pages. Put your answers in the space provided below each question. Be careful to adjust pagination while inserting circuit diagrams exported from LTSpice.

Edit the header above to insert your Rollnumber and Name.
Solution must be submitted on Moodle as a PDF file. Use 'File→Export'
All the questions in this file are in blue font. Please type in your answers in BLACK font to make your submission easy to grade

CONTEXT:

In the introductory session for this lab, we discussed the operation principles of a Bipolar Junction Transistor (BJT). For this assignment, we focus on the saturation and cut-off modes of operation. Effectively, in these modes the transistor acts as a switch with the Collector (C) and the Emitter (E) as two terminals of the switch. The switch is controlled by voltage V_B applied to the base terminal (B). When V_B is low, the CE switch is ON, when V_B is high, the CE switch is OFF. Revise the notes to figure out the voltage values in these two configurations. Design and simulate the required circuit in LTSpice as per the questions given below.

Question 1: Design a circuit using two NPN transistors that produces a square wave output 0-9V, frequency 1kHz and 50% duty cycle

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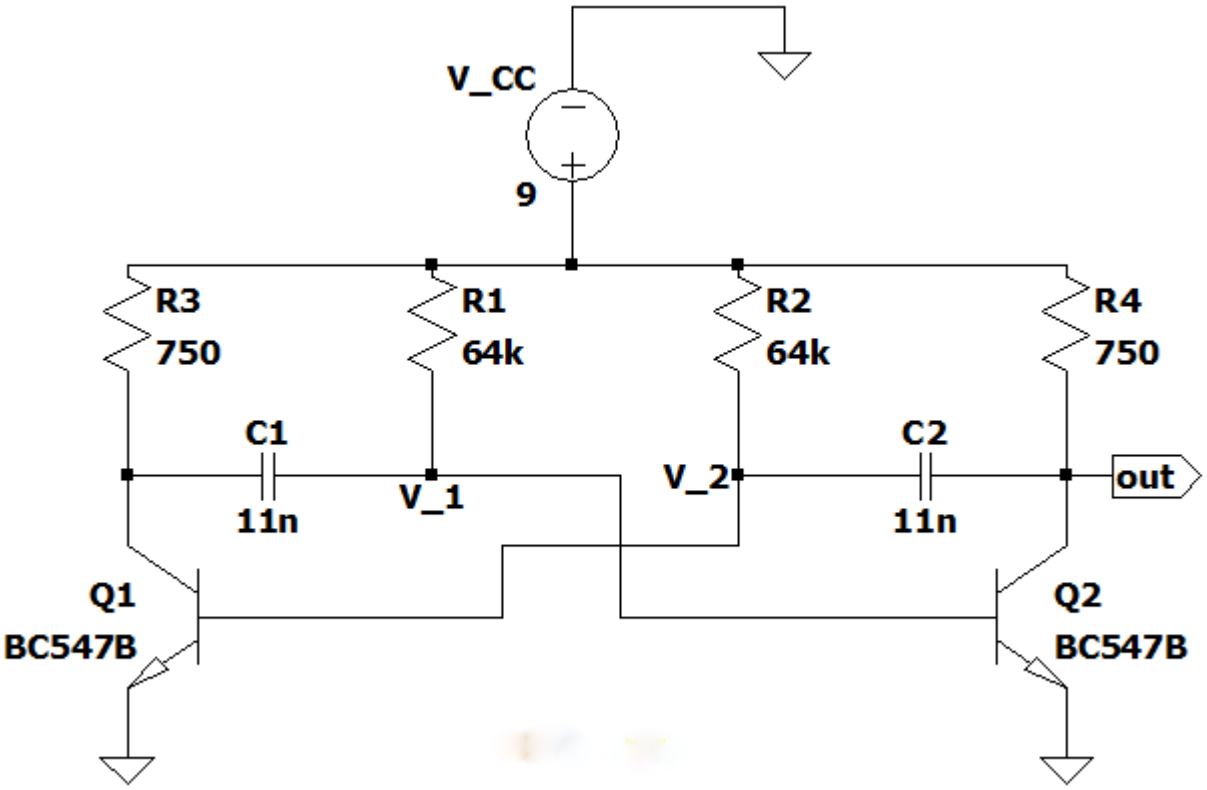
Your circuit design must obey the following design constraints:

1. It must use two NPN BJT's. You can assume initially that the BJT's are identical and use the ideal circuit model in LTSpice for the BJT BC547B
2. Work with a supply voltage V_{CC} = 9V and consume minimal current (few mA)
3. Use R, C as the only passive components.
4. The R values must set the BJT operating points. In conjunction with C, the circuit must produce the desired output voltage square waveform
5. Minimize the number of *different* values of R, C required – you may assume that each R and C is ideal

Space for Answer 1 (use 'Insert → picture' to insert your circuit design here)



Question 2: What values to check after building the circuit? **20**

You have made a clever circuit design in Answer 1 – now suppose you build it on your breadboard using the actual transistors, resistors, capacitors and some wire. After turning on V_{cc} what, and where are the values of DC voltages you should check on your circuit as built, to ensure that all the connections are made properly and the circuit should be working?

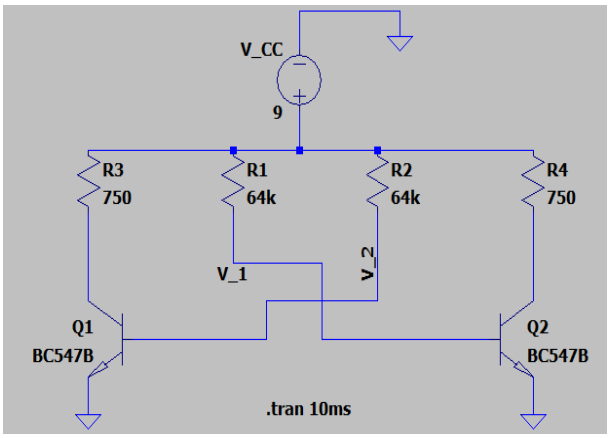
Note that the designed circuit is expected to start oscillating when powered up – so ideally, there should be no stable DC voltages in the circuit! Yet, we usually build circuits a few components at a time. After the first few components are connected and V_{cc} is turned on, the circuit should demonstrate stable DC voltages at certain nodes. What are these nodes and what are values of their DC voltages?

Make a list of the voltages to be checked here:

Space for Answer 2:

The circuit oscillations are caused by the combination of the transistors and the capacitors. So, in order to examine connections part by part using theoretical stable DC voltages one must follow the process:

1. Measure the voltages on both terminals of the voltage source V_{CC}. The positive terminal must read +9V and the Grounded terminal must read 0V.
2. Now, make connections of the resistors with the voltage source. We measure voltages across each resistor. Since the circuit is open the potential difference across all the resistors should be 0V, because both terminals should be at 9V. Different readings will imply that that resistor doesn't work.
3. We now connect the transistors with the resistors. In absence of the capacitors the partial circuit made so far has no open connections thus, it reaches a stable DC state. We calculate the theoretical expectations of stable state DC voltages at the base and collector terminals of the transistors and then compare these with actual observed values. Check that the emitter terminals should be grounded at 0V. Analysis gives that he following circuit is driven to saturation with voltages:
   - $V_{base} = 712mV$
   - $V_{collector} = 105\text{mV}$
4. The uncharged capacitors must read 0V across their terminals.
5. Now the circuit can be completed.



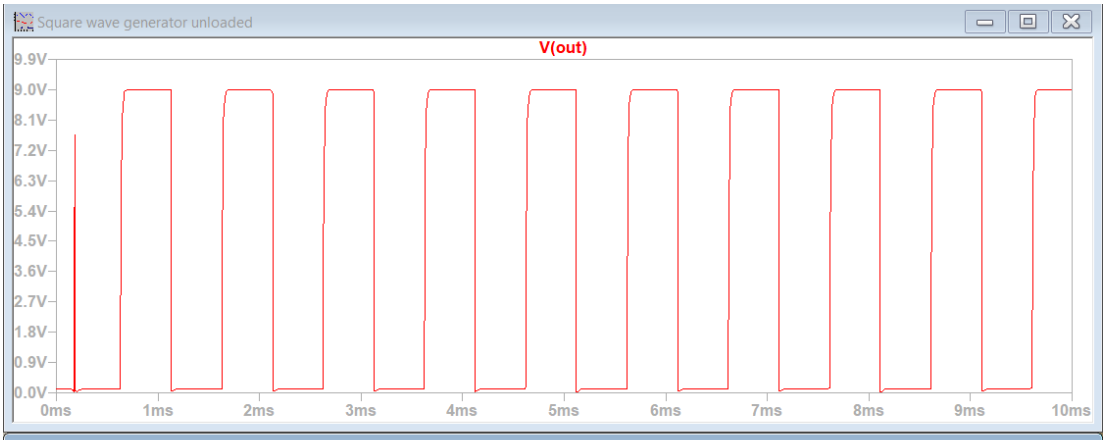
Question 3: What voltage waveform do you expect at the circuit output?

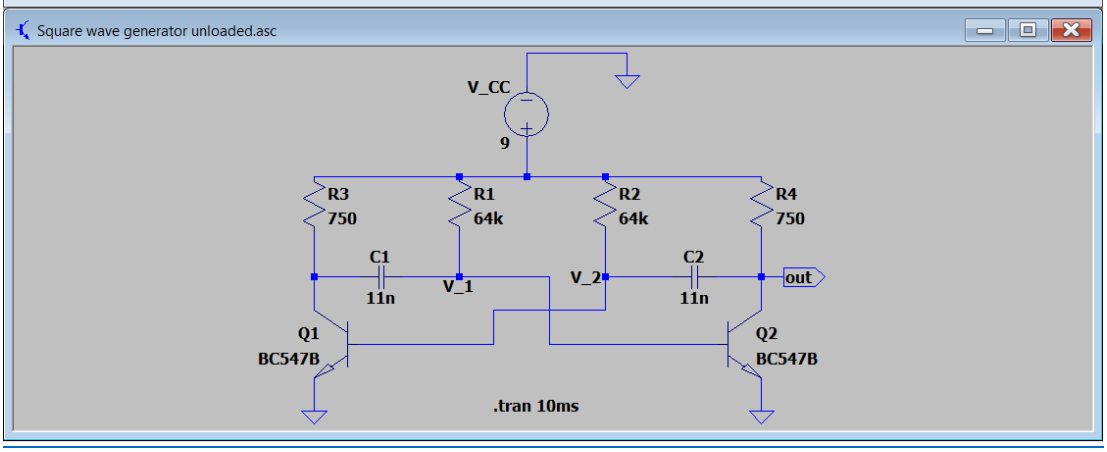
You are given a Digital Storage Oscilloscope (DSO) that allows you to probe the time-dependent voltage waveforms at various points in your circuit.

3.a) The DSO probe has effectively infinite impedance (like the LTSpice simulation "software probe") – what waveform do you expect to observe at the output of the circuit?
Run the circuit simulation completed in Question 1 and Insert a picture of your expected square wave output waveform here:

Answer 3.a **10**

With infinite load resistance the expected waveform is a square wave with minimum output (low state) $\simeq 0V$ and maximum output (high state)$\simeq V_{CC} = 9V$.





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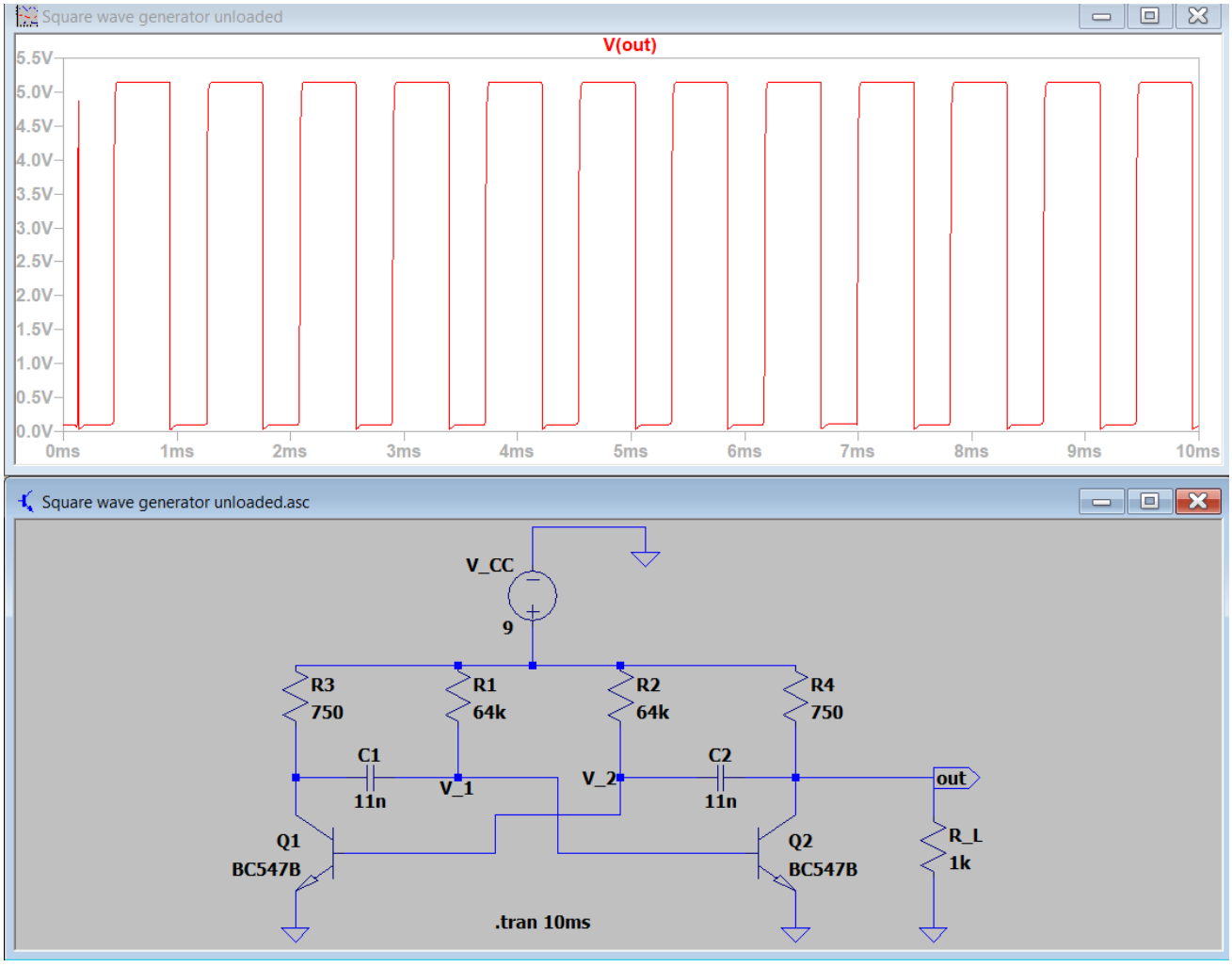
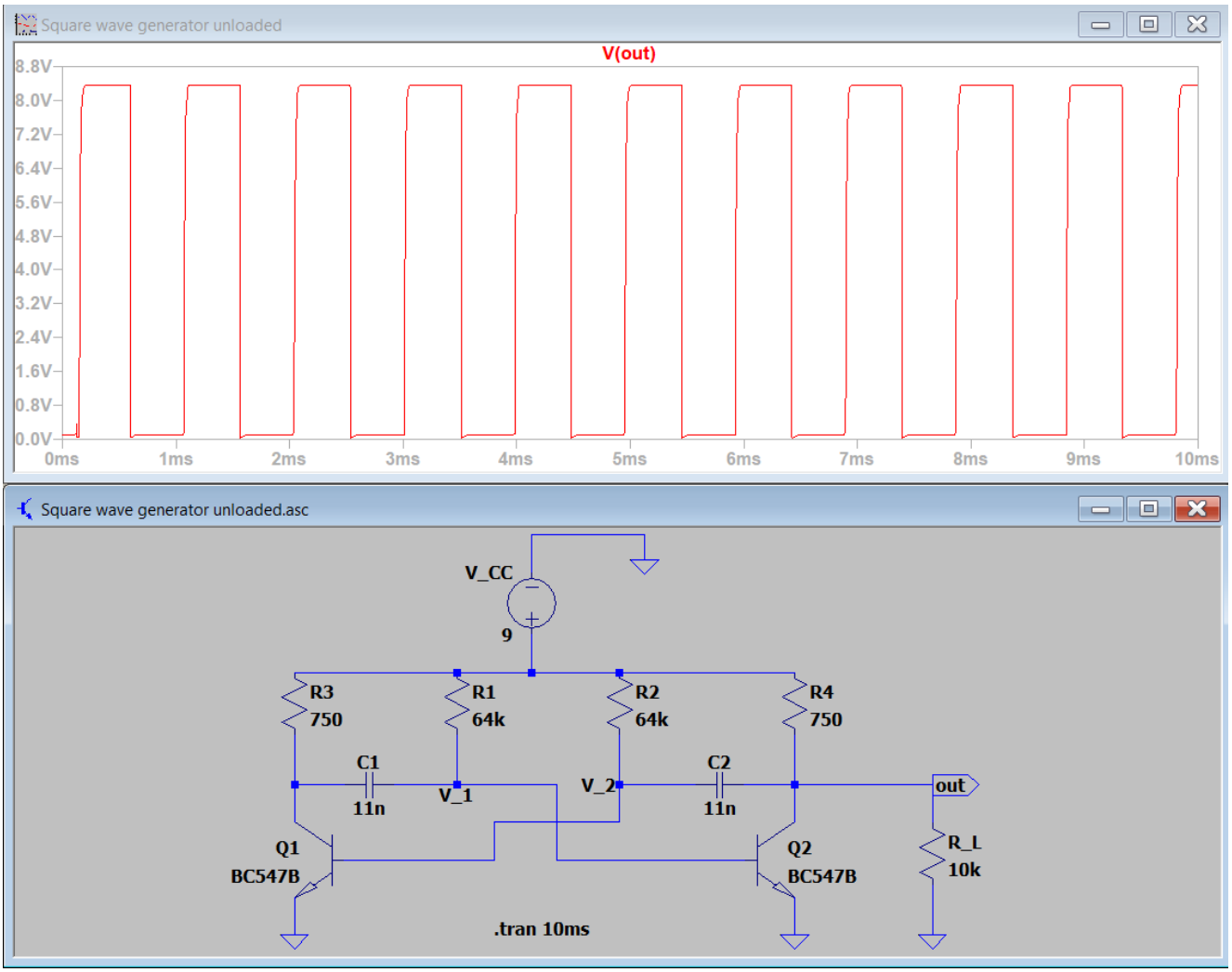
3.b) Suppose your oscillator circuit's output is sent to another circuit whose input is purely resistive. What waveform do you expect to observe at your oscillator's output if it is connected to ground through such a resistor load R_L?

The expected waveform is still a square wave to a high degree of approximation with lower value of maximum output and deviations from 0 for minimum values of output.

3.b.1) Simulation and analysis **10**

a) Run the simulation with output connected to a load resistance R_L=1kΩ /10kΩ and put a picture of your results here.

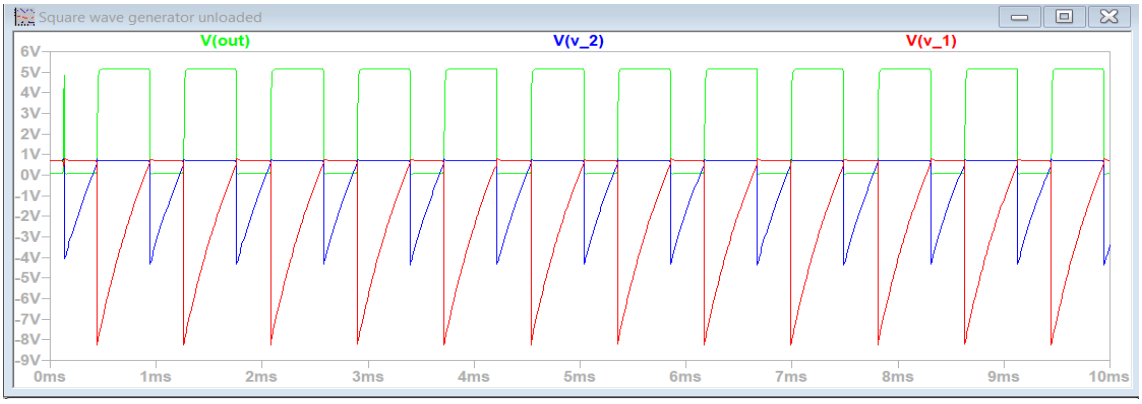



Square wave generator unloaded
V(out)
8.8V
8.0V
7.2V
6.4V
5.6V
4.8V
4.0V
3.2V
2.4V
1.6V
0.8V
0.0V
0ms
1ms
2ms
3ms
4ms
5ms
6ms
7ms
8ms
9ms
10ms
Square wave generator unloaded.asc
V_CC
9
R3
750
R1
64k
R2
64k
R4
750
C1
11n
V_1
V_2
C2
11n
out
Q1
BC547B
Q2
BC547B
R_L
10k
.tran 10ms

b) Work out the circuit formulae and justify the adverse effect of connecting a finite load resistance to the circuit output

Note: see Q.4 for notation, reference and theory. This is a continuation.

We consider the circuit with 1kΩ load. The graphs below denote V_{out}(green), V_1(red) and V_2(blue).



The analysis below (next pg.) doesn't down for very small load resistors when the max V_{out} is very low and the minimum output rises above 0V. The output graph shows severe distortion. Roughly put the waveform distortion is low when T_1 *and* T_2 are of the same order (of course $T_2 < T_1$ for any finite R_L), in other words the waveform distortion is low when the duty cycle is not very large.

One assumption is that we have a sufficiently large load-resistor (which can allow Q-2 to be driven to saturation and cutoff),

$$(V_{out})_{max} = \frac{V_{CC}R_L}{R_L+R_4},\ T_1 = 0.73\ R_1C_1,\ T_2 = R_2C_2 \ln\left(\frac{(V_{out})_{max}-0.7}{2(V_{out})_{max}-0.7}\right)$$

The Rise time can also be calculated it comes out to be:

$$\delta t_1 = 0.846\ C_2R_4$$

Having calculated T_1 and T_2 we have also found the duty cycle:

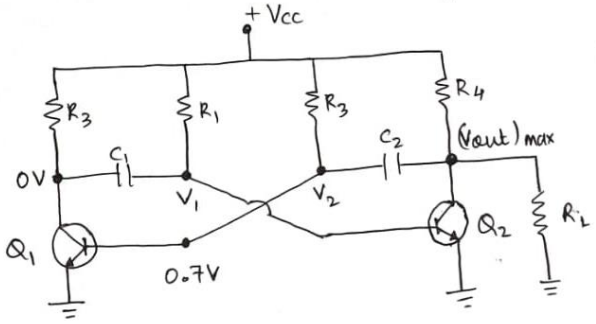
$$D = \frac{T_1}{T_1 + T_2}$$

Loaded Circuit.

We analyze state by state (Assuming oscillations have been set up)

① State - 1 V_{out} is high $\Rightarrow$ Q-2 in Cut-off

(I Derive and simultaneously work out values for $R_L = 1k\Omega$)



$$(V_{out})_{max} = \left(\frac{R_L}{R_L + R_4}\right) \cdot V$$

for $R_L = 1k\Omega$ & circuit given,

$$V_{out} = \frac{1}{1+0.75} \cdot 9 \simeq \boxed{5.14V}$$

Matches observation.

T_1: time taken by V_1 to rise from (−Vcc + 0.7) to 0.7., remains the same because Cutoff and Saturation voltages of Q-1 are unchanged. (unaffected by R_L)

$\Rightarrow \boxed{T_1 \simeq 0.73\, R_1 C_1}$

Though, Rise time changes since it involves $(V_{out})_{max}$

$\delta t_1 \equiv$ time taken for V_{out} to rise from 0V to $(V_{out})_{max}$ given that V_2 is at 0.7V.

The diffrential equation is still of the same for (Q.4.3)

$$\frac{\delta t_1}{C_2 R_4} = \ln\left[\frac{9 - V_{out}(t=0)}{9 - V_{out}(t=\delta t_1)}\right] = \ln\left[\frac{9}{9 - 5.14}\right]$$

$$\boxed{\delta t_1 = 0.846\, C_2 R_4}$$

.

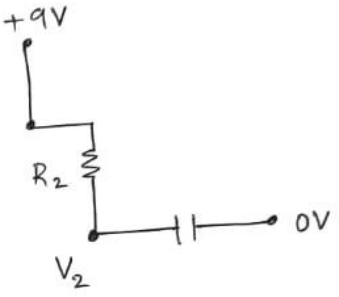
(2) V_{out} is Low - Q-2 is saturated $\Rightarrow V_{out} = 0V$

Sudden drop of V_{out} from $5.14\,V \equiv (V_{out})_{max}$ to 0V causes:

V_2 to drop to $\left(-(V_{out})_{max} + 0.7\right) = -5.14 + 0.7$
$= -4.44\,V$ for our case

$T_2 \equiv$ time taken by V_2 to rise from $-(V_{out})_{max} + 0.7$ to $+0.7\,V$

The form of differential eqn remains the same as in Q.4)



$$\int_0^{T_2} \frac{dt}{C_2 R_2} = \int_{q(0)}^{q(T_2)} \frac{dq}{qC_1 - q}$$

$$\Rightarrow \frac{T_2}{C_2 R_2} = -\ln\left[\frac{q - V(t=2)}{q - V(t=0)}\right]$$

$$\frac{T_2}{C_2 R_2} = -\ln\left[\frac{q - 0.7}{q - \left[(-V_{out})_{max} + 0.7\right]}\right]$$

$$\boxed{T_2 = + \ln\left[\frac{8.3 + (V_{out})_{max}}{8.3}\right] C_2 R_2}$$

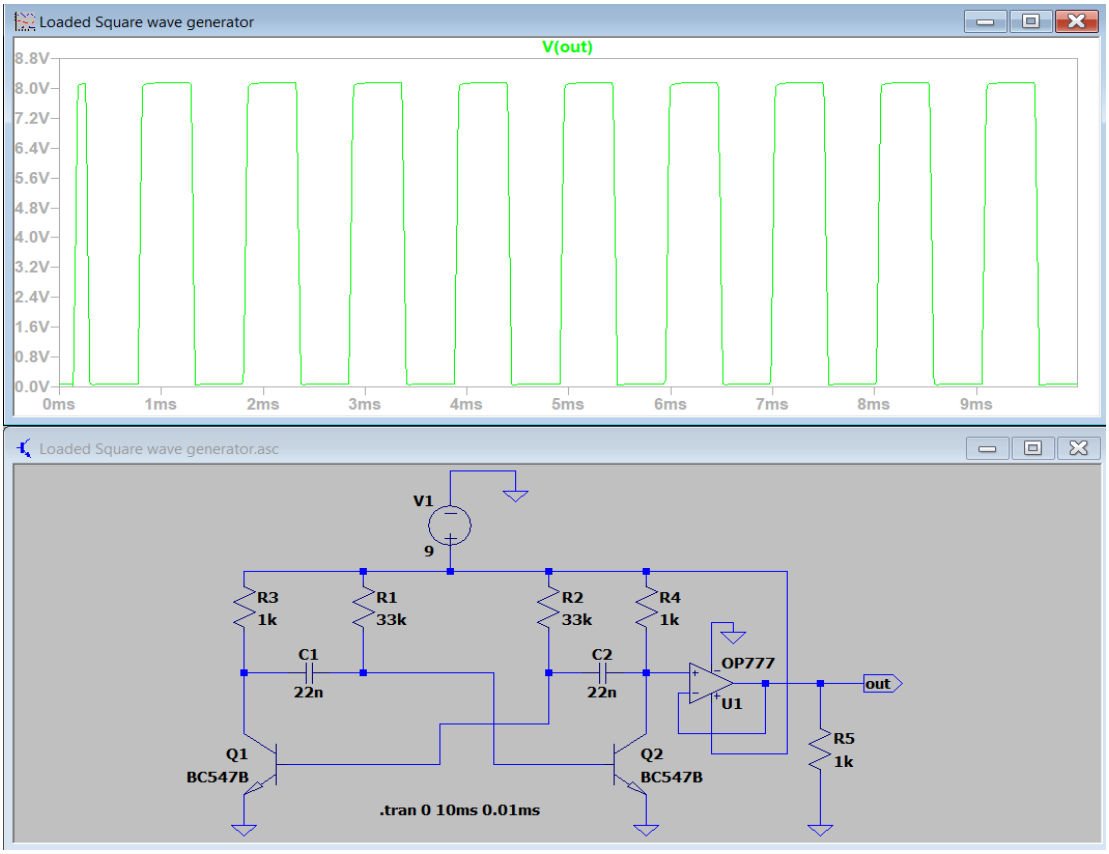
Working out these values for $R_L = 1k\Omega$ and rest of our circuit:

$T_1 = 0.5ms$
$T_2 = 0.33ms$ $\longrightarrow$ $T = 0.83\,ms$

Exactly what is observed!

$\delta t_1 \simeq 7\mu s$

3.b.2) Think of ideas that reduce the effect of "loading" on your circuit output voltage. Your ideas can include adding a passive or active component to the circuit **20**



An Op-Amp has a very high input impedance and hence a unit gain Op-Amp buffer decreases effect of small load. The effectiveness of this is evident from the above simulation.

For the same value of load connected directly the output peak was merely 5.14V but now it is 8.21V which is a significant fraction of the ideal infinite load output of 9V.

Another alternative that can be considered is using a third BJT which would increase the effective load resistance by a factor of β as seen from the base side which would be connected to the circuit at. Only, optimizations must be done to ensure that this apparatus doesn't draw high currents from the voltage source.

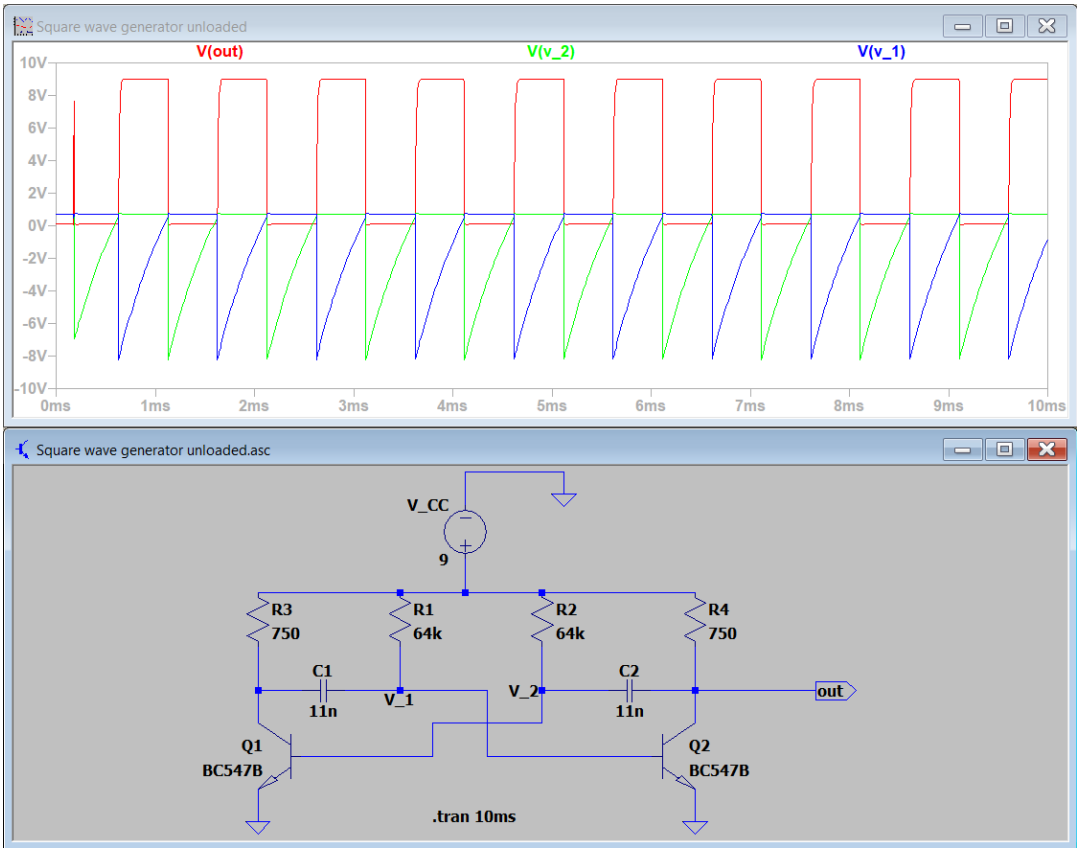
Question 4: Unexpected, non-ideal measurements

Even with the effectively infinite input impedance of the DSO probe, suppose the measured output of your circuit is not as expected

a) The frequency of the output is not exactly 1kHz as designed
b) The rise/fall times of each square pulse is rather large, i.e. the square pulse looks like it has 'rounded' edges

Give a summary of your understanding by answering the following questions:

4.1) Derive the formula that determines the frequency of oscillation of the circuit in terms of the values of the resistors and capacitors used (assume the two BJT's are identical) **20**



The above graphs and circuit diagram will come in handy for analyzing the circuit. In the Voltage charts below, Red is the output voltage, Blue is the voltage V_1 and Green is the voltage V_2.

Notation: For the passive elements notation is as used in the circuit diagram. The three terminals of the two transistors Q-i (i={1,2}), are denoted as C-i for collector, B-i for base and E-i for the emitter. Voltages of these terminals use the above symbols as subscript. The voltages at the inner terminals of the two capacitors are as labelled V_1 *and* V_2.

The Process: For deriving the formulae that describe the frequency of oscillation one must understand the working of the circuit. When the circuit is powered up one of the two transistors reaches saturation first due to the increase of the base voltage to a positive value (>0.7V). This asymmetry in the cycle is due any minute asymmetries in the circuit like the tolerances of various components, residual charge on the capacitor, etc.

The saturation of one of the transistors, say Q-1 causes it to short, suddenly dropping the collector voltage to zero $(V_{C-1} = 0)$ (This is an approximation, see Q.4.3 for the reasoning). This causes the second terminal of the capacitor (C_1) connected to base: B-2 to drop down to a negative voltage $(V_1 = -V_{CC} + 0.7V)$ which causes transistor Q-2 to cut off.

This is State-1 of the Astable Multivibrator. Here transistor Q-1 operates as a closed switch (ON, in Saturation) with transistor Q-2 operating as an open switch (OFF, in cutoff). In State-1: $V_{C-1} \simeq 0 \; and \; V_{C-2} \simeq \mathrm{V_{CC}}$

State-2 is when Q-1 operates in the cut-off region and Q-2 operates in the saturation region.

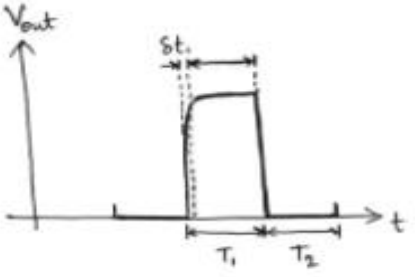
In the circuit the output is taken at the collector of Q-2 which means in State-1 output is high and in State-2 it is low. The output toggles in between these two states.

Due to the nature of the circuit (unloaded), it is enough to derive expressions for state-1 and the expressions for state-2 will follow.

Q4.1)

Derivation

State 1: Q-2 in cut-off mode - Output is high.

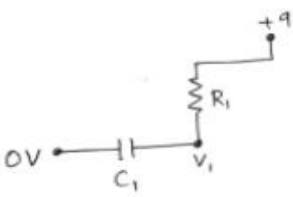


St_1 = Rise time from $V_{out} = 0$ to $V_{out} \simeq 0.99 V_{cc}$

T_1 = Time period of state-1, T_1 is the time taken for V_1 to rise from $(-V_{cc} + 0.7)V$ to $(0.7V)$

Given $V_{cc} = 9V$;

① Calculating T_1 : Q-1 is saturated $\Rightarrow$ C_1 charges through Source $\longrightarrow$ R_1 $\longrightarrow$ C_1 $\longrightarrow$ Ground path



Apply Kirchhoff's Law :

$$* \quad 9 - \frac{dq}{dt} R_1 - \frac{q}{C_1} = 0$$

$$\Rightarrow \quad 9C_1 - q = C_1 R_1 \frac{dq}{dt}$$

$$\Rightarrow \int_0^{T_1} \frac{dt}{C_1 R_1} = \int_{q(0)}^{q(T_1)} \frac{dq}{(9C_1 - q)} = -\ln\left[\frac{9C_1 - q(t_1)}{9C_1 - q(0)}\right]$$

$$q(t_1) = 0.7V \times C_1 \quad ; \quad q(0) = (-V_{cc} + 0.7) \times C_1$$

$$\therefore \quad \frac{T_1}{C_1 R_1} = -\ln\left[\frac{9 - 0.7}{18 - 0.7}\right] = -\ln[0.48]$$

$$\boxed{T_1 \simeq 0.73 R_1 C_1}$$

Sloppy approximation of the above expression by taking $V_{cc} >> 0.7$ gives $T_1 = \ln 2 \, R_1 C_1$.

Similarly $\boxed{T_2 \simeq 0.73 R_2 C_2}$

Hence if T is the total period then $\boxed{T = T_1 + T_2} = 0.73 (R_2 C_2 + R_1 C_1)$

Duty Cycle ≡ % of output in high state

Here, $D = \dfrac{T_1}{T_1 + T_2}$

for $D = 50\%$ we choose $R_1 = R_2 = R$, $C_1 = C_2 = R$

$$\Rightarrow \quad T = 0.73 \times 2 \times RC$$

$$f \simeq \frac{1}{1.46 RC} \quad , \text{ for } f = 1\,kHz$$

$R = 64\,k\Omega$ and $C = 11\,nF$ is a possible combination

$f \simeq 1\,kHz$, $T = 1\,ms$

4.2) If one of the resistor values used while building the circuit is different from the specified value by 5%, what is the effect of this error on the frequency of oscillation? Evaluate the error δf in the frequency, if there is an error $\delta R = 0.05 \cdot R$ of the resistor value.

5

Q 4.2) f, T depends on R_1 and R_2.
effects due to R_3 and R_4 are negligible on f.

Thus if R_3 or R_4 are off by 0.05 factor or 5% the change in f is zero.

If R_1 or R_2 change by 5%, let $R' = 2R + \delta R$

$$f' = \frac{1}{0.73\,C\,(R')} = \frac{1}{0.73\,C \cdot 2R\left[1 + \frac{\delta R}{2R}\right]}$$

$$f' \simeq \frac{1}{1.46\,RC}\left[1 - \frac{\delta R}{2R}\right] \Rightarrow f' - f = -f\frac{\delta R}{2R}.$$

$$\frac{\delta f}{f} = -\frac{\delta R}{2R} \quad \therefore \text{ if } \frac{\delta R}{R} = \pm 0.05$$

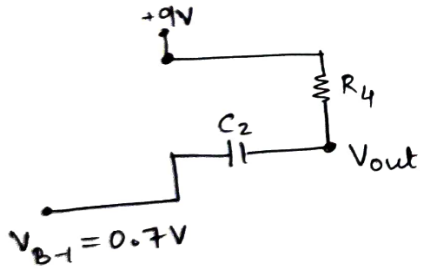
$$\boxed{\frac{\delta f}{f} = \mp 0.025}$$

4.3) If the observed oscillatory waveform is not a perfect square wave, but instead has 'rounded edges', what component value would you suspect as the culprit?
Evaluate how an error δX where X is the value of the suspected component affects the shape of the waveform (it may be easier to use `.STEP` feature of LTSpice to answer this question). In particular if δX is 0.05·X, what is the change in rise time of the output?

5

The round edges are due to the finite rise time dependent on C_2 *and* R_4 for our circuit ($C_1 = C_2$ *and* $R_3 = R_4$). The simulation reveals the dependence of the rise time on the variation in parameter R_4 keeping C_2 constant.

Q 4.3)
In fig of Q 4.1) $S_t \equiv$ Rise time from $V_{out} = 0$ to $V_{out} \simeq V_{cc}$
We want to find S_t to go from $V_{out} = 0$ to $V_{out} = 99\%$ of V_{cc}
The rise is due to charging of capacitor as follows:



Kirchhoff's Law gives:

$$q - V_{out} = \frac{dq}{dt} R_4$$

$$\{q = (V_{out} - 0.7) \cdot C_2\}$$

$$\Rightarrow \quad q - V_{out} = \frac{d}{dt}(V_{out} - 0.7)\, C_2 R_4$$

Solving,

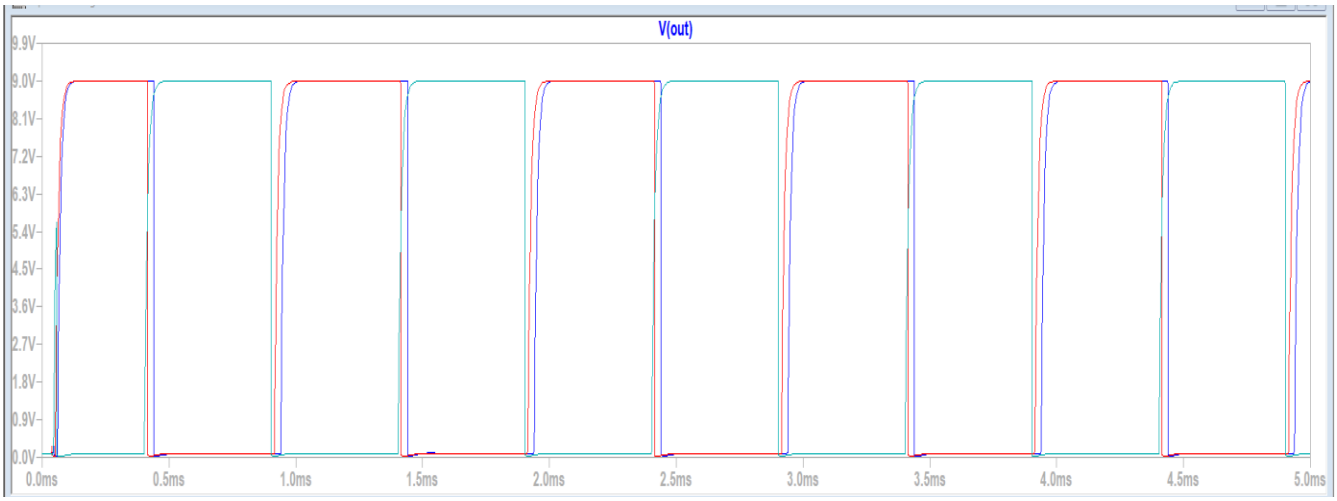
$$\frac{S_{t_1}}{C_2 R_4} = \ln\left[\frac{9 - V_{out}(0)}{9 - V_{out}(S_{t_1})}\right] = \ln\left[\frac{9}{0.01 \times 9}\right]$$

$$\boxed{S_{t_1} = C_2 R_4 \times 4.6}$$

For 5% change in $R_4(with\ R_3)$ value the rise time changes by nearly 5%. Here we have considered only change in $R_4(with\ R_3)$ because changing $R_4(with\ R_3)$ values will also change the time period. Note that $R_4(with\ R_3)$

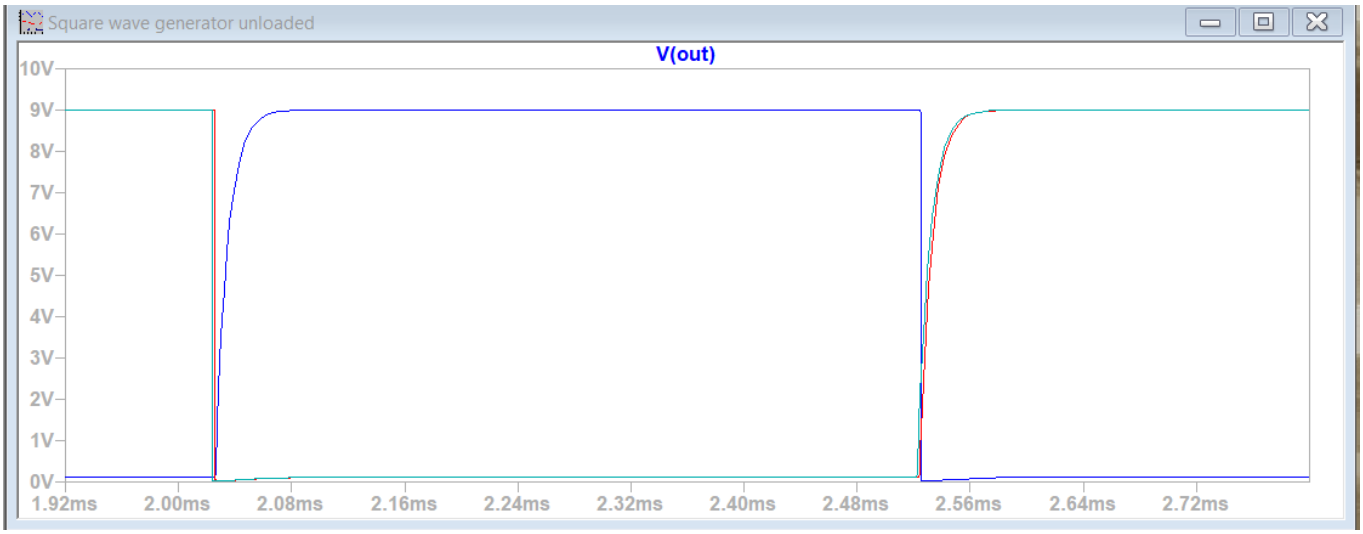
The .STEP feature is used in the simulation below in order to see a comparative picture of the rise times for different R_4(and R_3) values.

1) The simulation below is for values 950Ω, 1000Ω and 1050Ω. (step size 5% around 1000Ω)



Observed difference in rise time is minute but zooming in onto the curved part reveals that rise time increases as R_4 value increases as derived.

2) The simulation below is for values 748Ω, 750Ω and 752Ω. (step size ≃ 2% around 750Ω). The variation in rise time is insignificant compared to the time period.



Question 5: (Advanced, BONUS questions)

1) What are the circuit modifications required to change the duty cycle of the waveform to less than or more than 50%? **20**

a. How does the waveform performance change (with reference to non-idealities analyzed in question 4) as you change the parameters? It appears to be a large parameter space, but upon understanding the circuit's behavior you may find that only a few parameters really decide both the duty cycle and the waveform rise/fall times

b. As an example, give circuit component values required for a 25% and 75% duty cycle waveform of 1kHz

Note: see Q.4.1 for the derivation.

As derived in Q.4.1 the duty cycle depends on the time periods $T_1 = 0.73\ R_1C_1$ and $T_2 = 0.73\ R_2C_2$.

$$D = \frac{T_1}{T_1 + T_2} = \frac{R_1C_1}{R_1C_1 + R_2C_2}$$

Thus, the duty cycle depends on 4 circuit components, in fact even varying one of these changes the duty cycle accordingly. We avoid changing the capacitor values since that will also change the rise time as analyzed in Q.4.

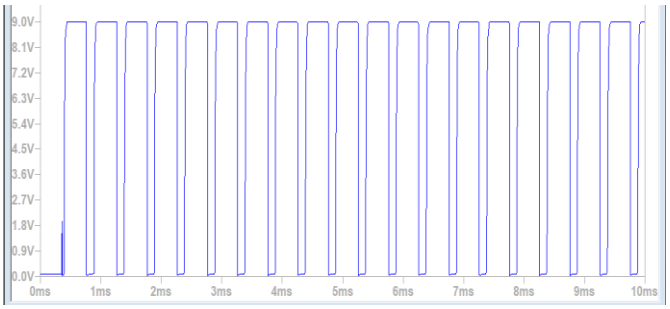
We can choose these component values to get the desired duty cycle.

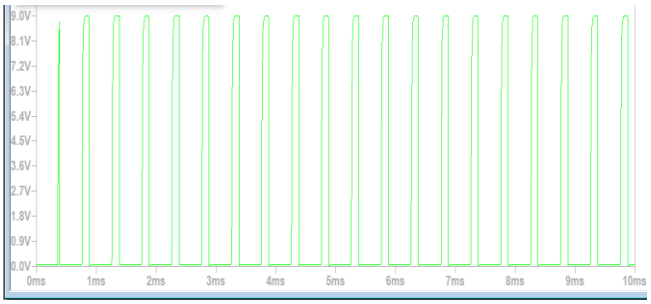
Duty cycle 75%: for T=1ms, $T_1 = 0.75ms$ and $T_2 = 0.25ms$

$R_1 = 48\Omega, R_2 = 15.6\Omega, C_1 = C_2 = 11nF.$ (f=1kHz)

Duty cycle 25%: for T=1ms, $T_1 = 0.75ms$ and $T_2 = 0.25ms$

$R_1 = 15.6\Omega, R_2 = 48\Omega, C_1 = C_2 = 11nF.$ (f=1kHz)





Above are the simulations for the specifications calculated with D=0.75 and D=0.25 respectively.

2) It is, in principle, with a quick internet search, possible to make an oscillator circuit with a single BJT circuit. Analyze that circuit and determine what are its drawbacks. Why did we steer you away from a deceptively simpler single BJT oscillator??

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