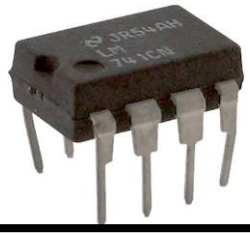
Lab 2: First experiments with the LM741 opamp IC 25

All question material is in blue. Please put your answers in black color font

In this assignment we will introduce you to the LM741 opamp IC. You will learn how to reliably make connections and build circuits around this IC. We will use the LM741 for many experiments during the rest of the semester, so make sure that at the end of this lab, you are thoroughly familiar with the procedure for making circuit connections to the LM741



"Golden" rules of opamp:

1) $V_o = G(V_+ - V_-); G \sim 10^6$
2) Negligible current into V_+ *and* V_-

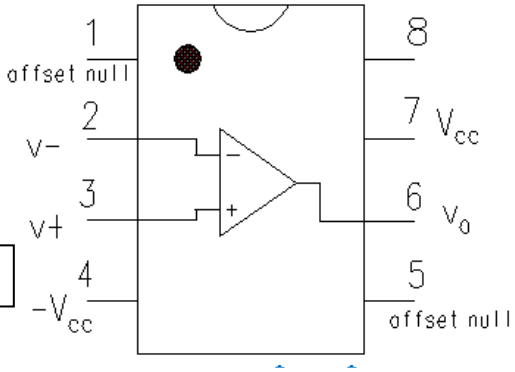


Fig 1: Picture and pinout of LM741

Fig 1 shows a picture and the pin diagran

Note the numbering of pins as viewed from the top, with the semicircular notch facing up. You must always remember this when connecting the IC on a breadboard as shown in Fig 2

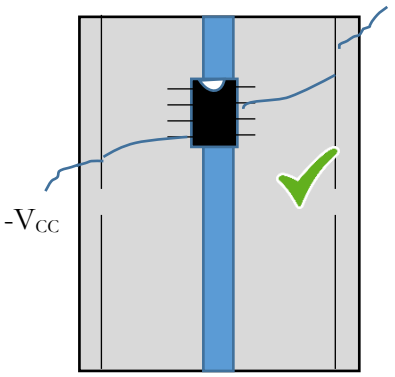
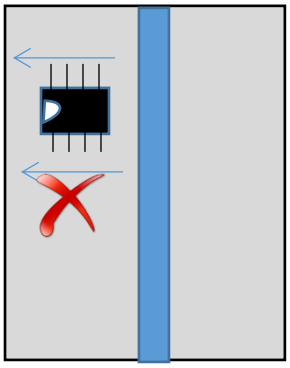


Fig 2: Connecting the LM741 on a breadboard



CORRECT: Each pin has a separate horizontal breadboard trace. $+V_{CC}$ and $-V_{CC}$ are connected along the edge traces

WRONG! Pins 1-4 and 5-8 of the IC will be shorted to each other!

Question 1: "Dual" supply voltage Setup 3

741 opamp requires a dual voltage supply $+V_{cc}$ and $-V_{cc}$ (Fig 1)

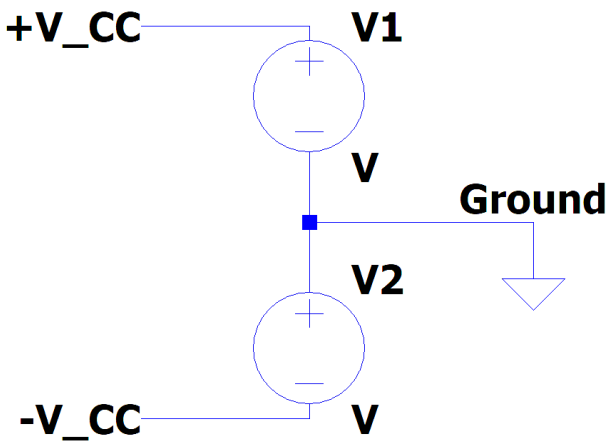
1.1) BASIC SETUP: 1

You have two 9V batteries. How should you connect them so as to obtain such a dual supply $+V_{CC}$ and $-V_{CC}$? Is +9V and -9V adequate power supply voltage for the op-amp? (look up the LM741 datasheet!).

Make a circuit diagram here of your connection scheme: $\pm V_{CC}$

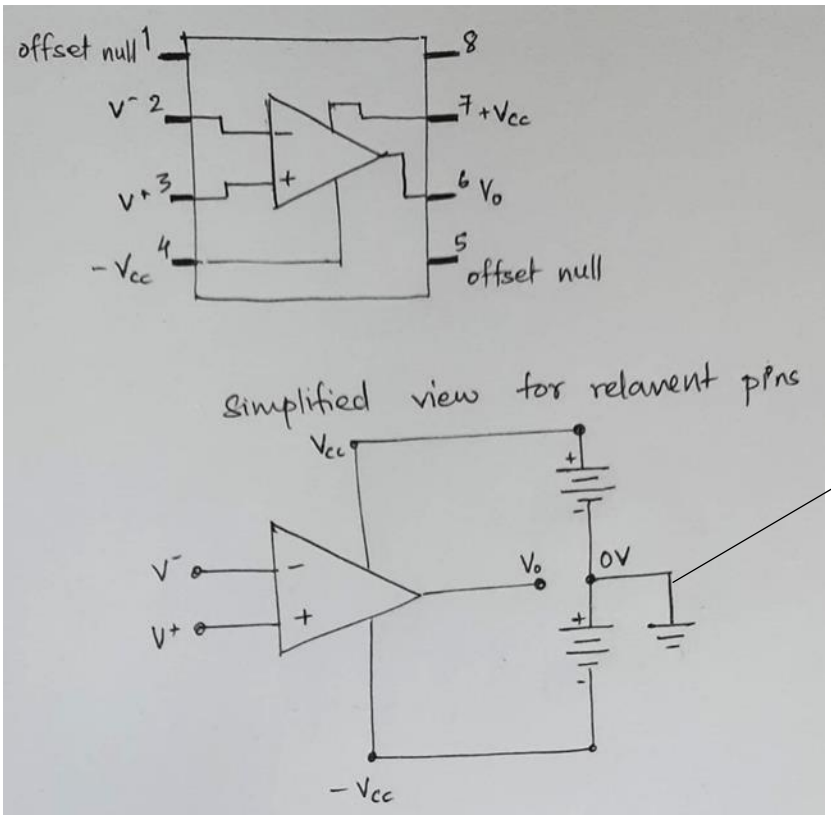
Note that the op-amp in the kit is **UA741CN.** The datasheet gives the operating supply voltage rating as: min $\pm 2.5V$ and max $\pm 20V$. So, a $\pm 9V$ would be within safe limits.

We have two $V_{CC}(\simeq 9V)$ batteries so we can connect them in series with their common terminal as the reference ground as shown:



1.2) GROUND: 1

As discussed extensively in PH231, every circuit must have a 0V GND reference node. In your $\pm V_{CC}$ connection scheme of Question 1.1 above, which node should you take as the GND node?

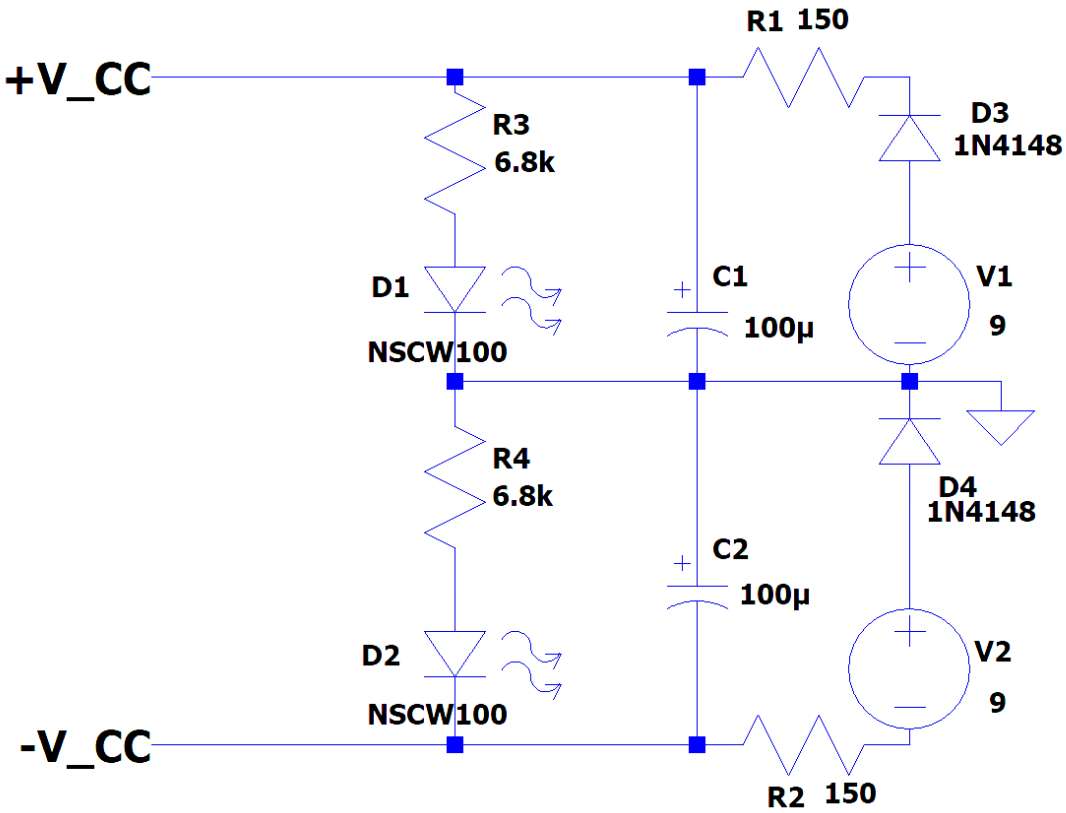


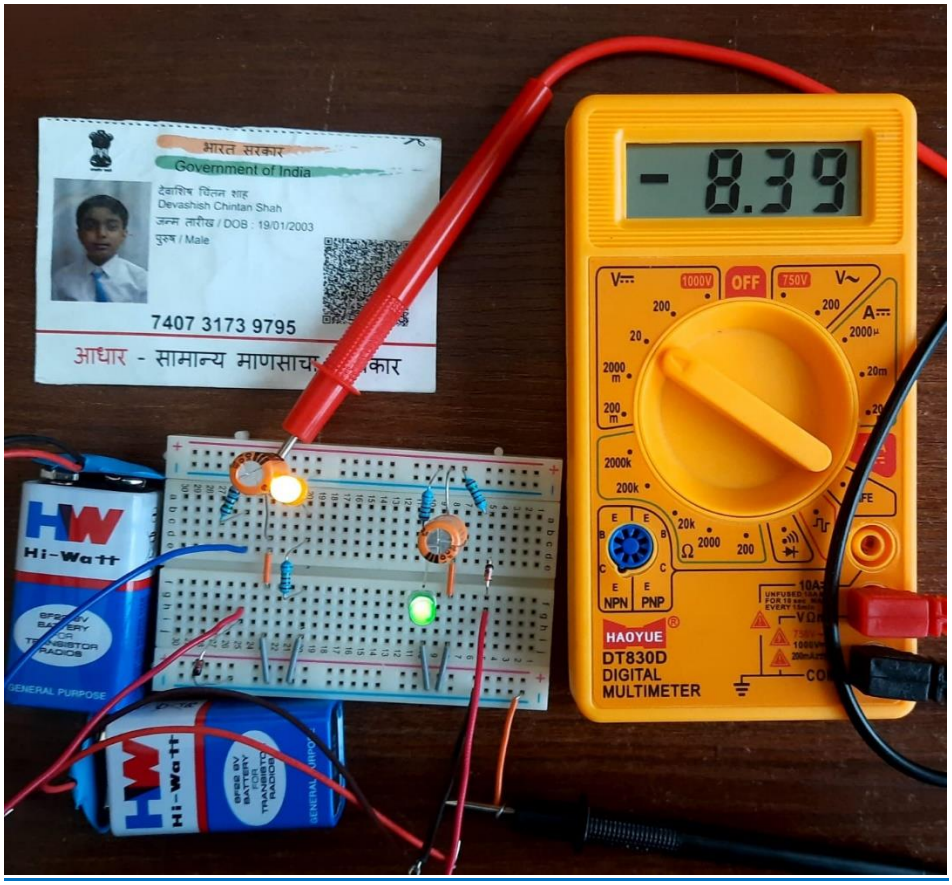
The above diagram clearly shows the node to be taken as the GND node. It is the common node between the two batteries.

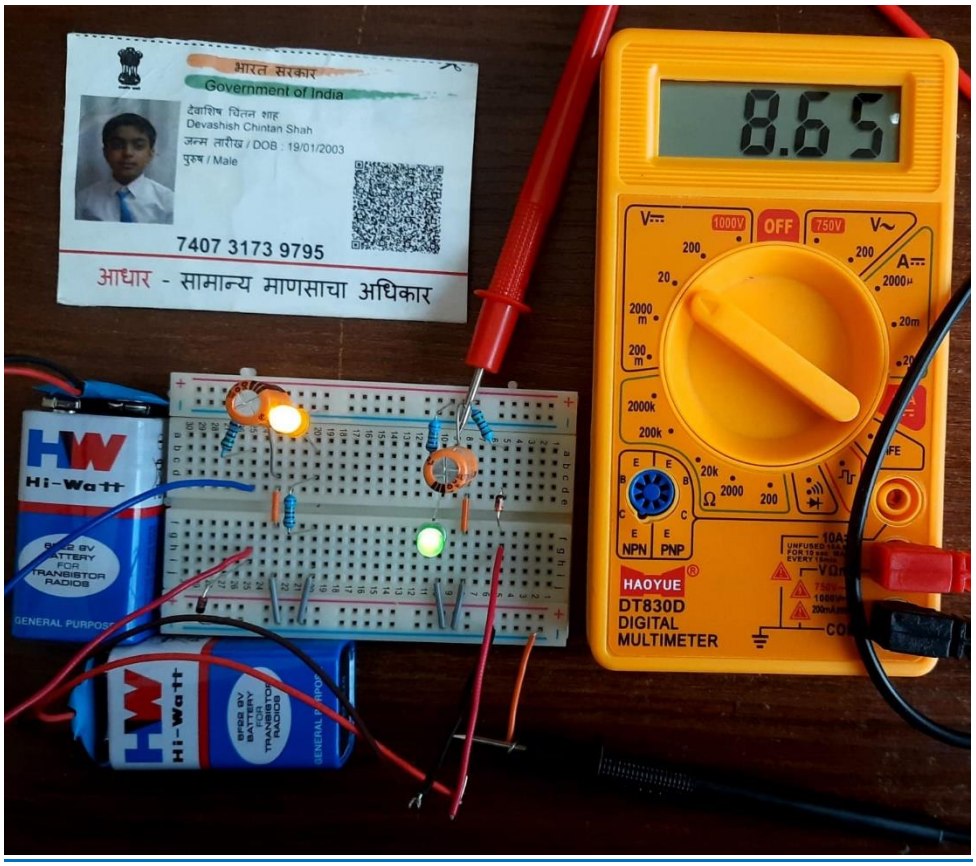
1.3) PROTECTION/INDICATOR CIRCUIT 1

Similar to the 9V V_{CC} circuit used in PH231, it would be nice to have a power on indicator, and a protection circuit to guard against instant discharge of the battery in case of bread-board short-circuits. Expand the design of which, power indicator and protection circuit of PH231 for dual supply $\pm V_{CC}$. Draw your circuit here and implement it on your breadboard. **Now on your breadboard side rails, you will have 3 power lines, one each for +9V, –9V and GND. Check with DMM that you are getting the correct voltages at these power lines and label them for yourself clearly: you don't want to *ever* reverse the ±9V connections to the op-amp and blow it up!**

NOTE: A smaller is used since it had printed labelling for the +/- power lines which helps.


+V_CC
-V_CC
R1 150
R2 150
R3
6.8k
R4
6.8k
D1
NSCW100
D2
NSCW100
D3
1N4148
D4
1N4148
C1
100µ
C2
100µ
V1
9
V2
9

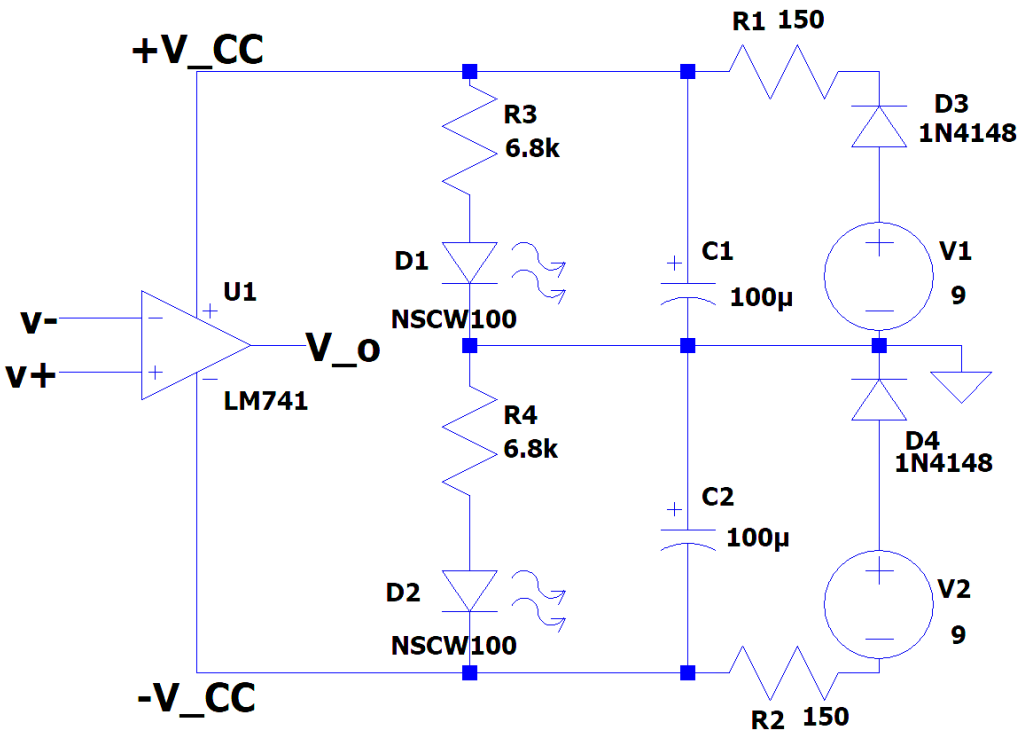

भारत सरकार
Government of India
Devashish Chintan Shah
7407 3173 9795
- 8.39
HAOYUE
DT830D
DIGITAL
MULTIMETER
Hi-Watt



Question 2: Op-amp POWER ON and Open Loop Test 7

2.1) Mount the 741 op-amp on your breadboard in the correct orientation as shown in Fig 2. Leave the inputs **disconnected** and the power **OFF.**
Connect the red (signal) probe of the DSO to V_{out} from the op-amp, black (GND) probe should be connected to your breadboard GND
Set the DSO trigger mode to AUTO and choose a longtime axis ~ 10ms/div.
Record here (with a photo) the steady state voltage observed at V_{out} and how **V_{out} changes when you turn the power ON:** **1**

Given below are the pictures of the LTSpice circuit (for reference) and the Breadboard circuit:

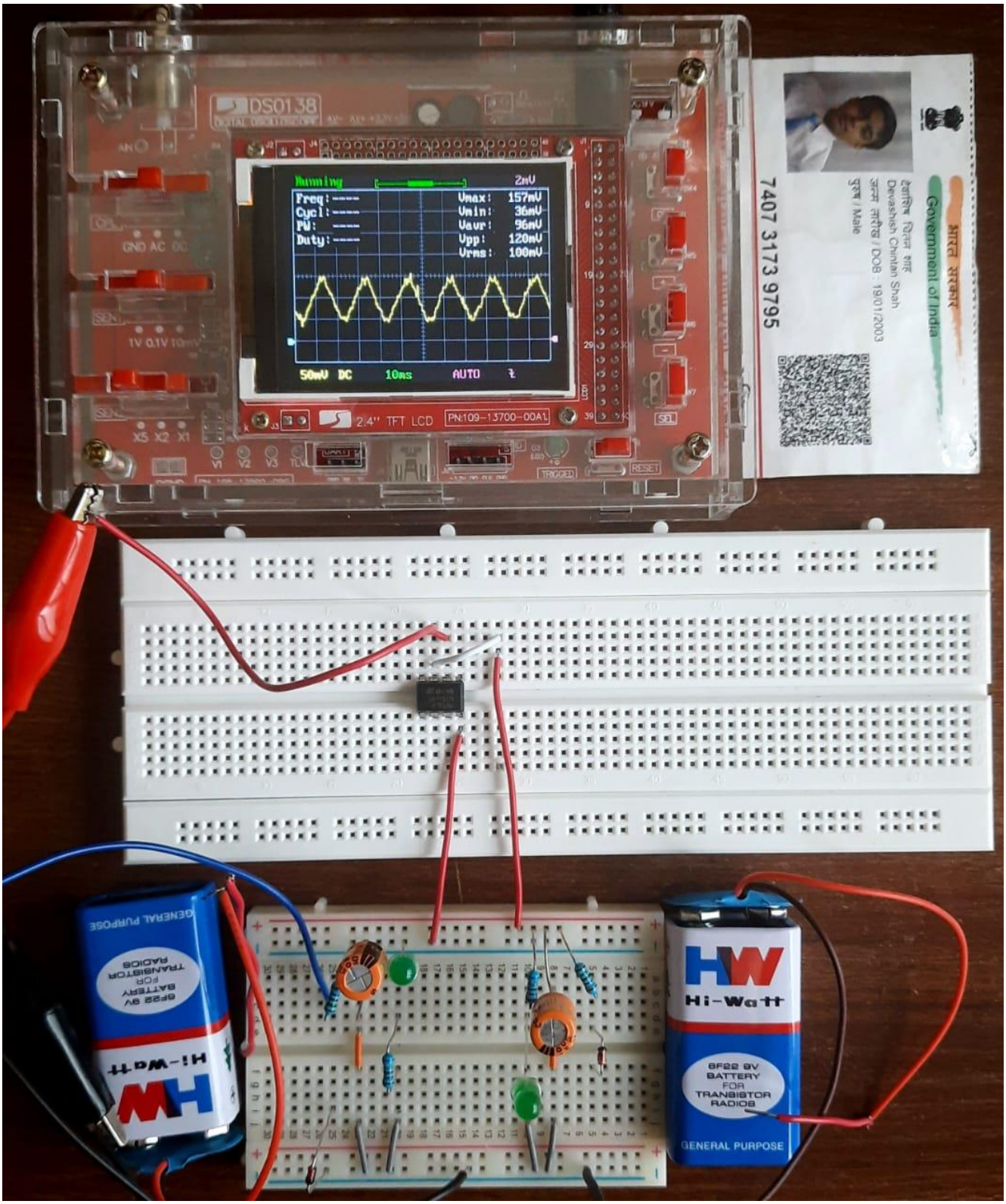


Observations:

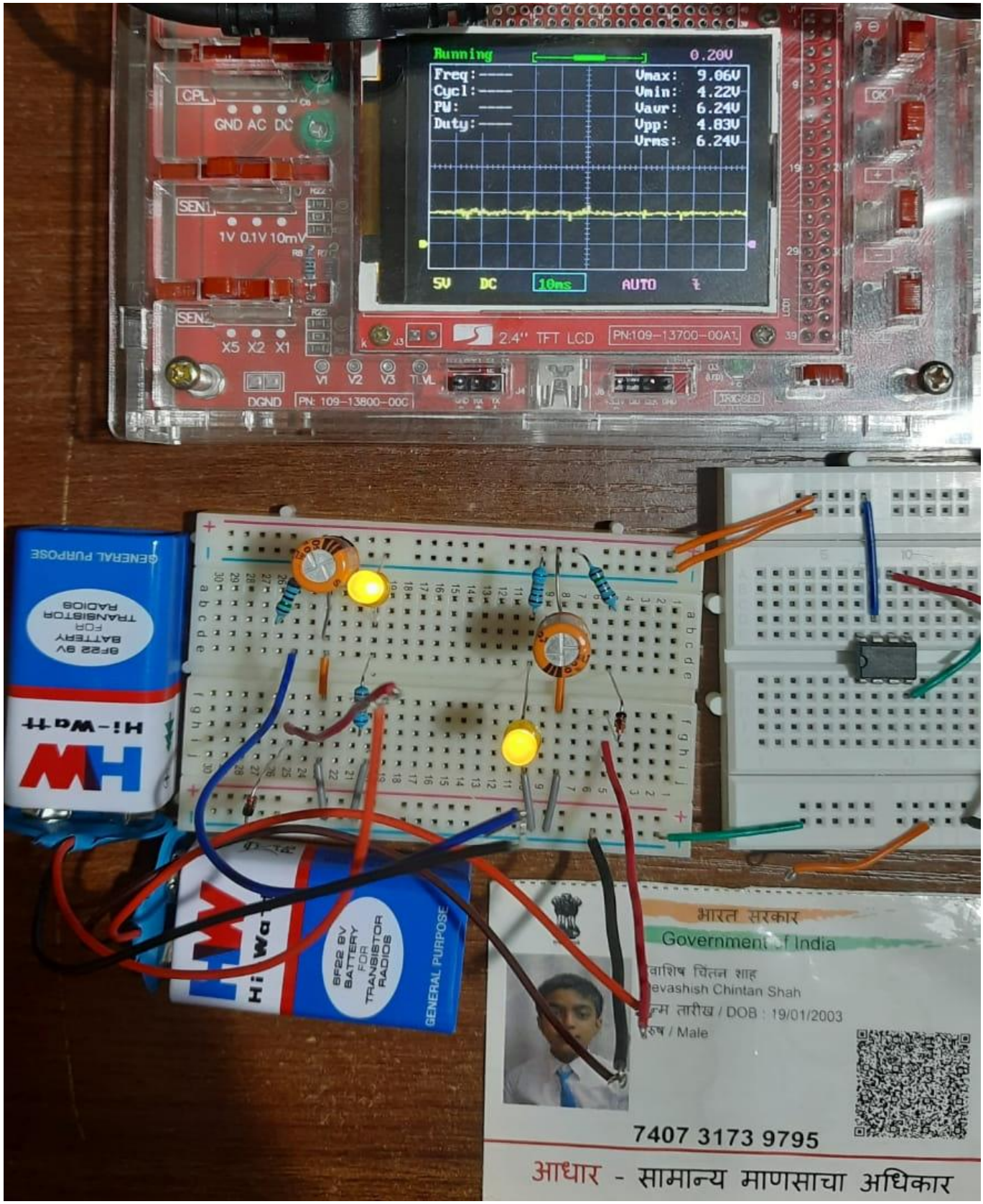
1) DSO screen registers small amplitude noise when supply isn't connected.

2) DSO screen shows an average voltage of $\sim 6.24V$ because even small fluctuations or noise are magnified by $\sim 10^6$ to a maximum of about V_{cc}.

$\pm V_{CC}$ disconnected:



Supply voltage connected:



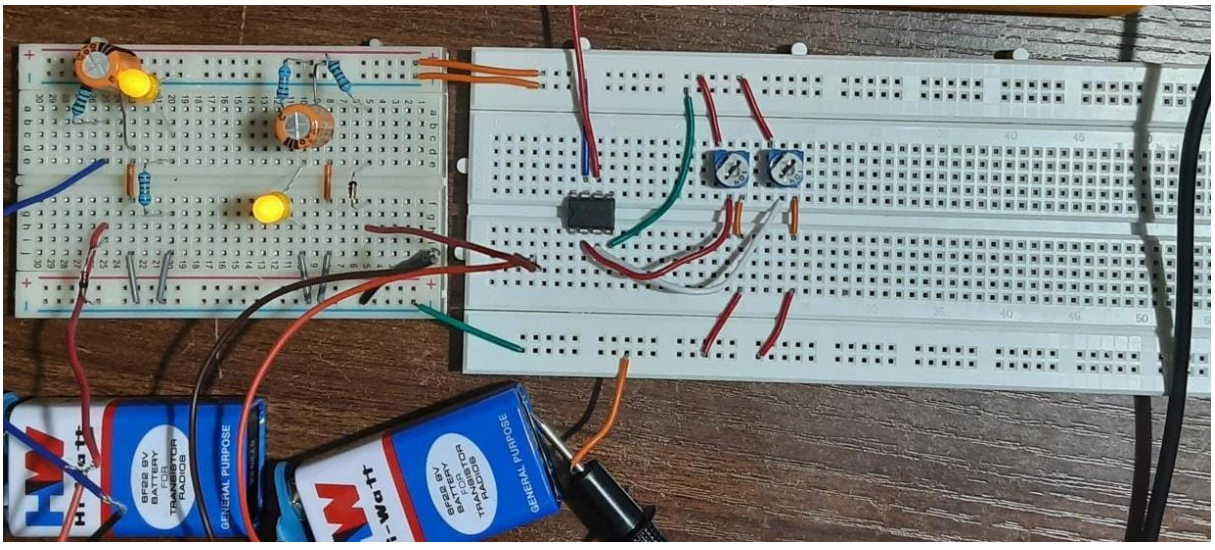
Explain your observation using the governing equation of op-amp operation:
$V_{out} = G \times (V_+ - V_-)$ where $G \sim 10^6$ is the "open loop gain". **2**
It may be useful to try this power ON/OFF test multiple times to check if your result is repeatable.

Repeated power ON/OFF test reveals the fact that the output voltage is highly unstable when it comes to max/min values because after all it is a result of the magnification of small amplitude noise from the mains, external environment. The average value of the output voltage observed is about $\sim 6.5V$, which is due to the small positive average value of noise.

2.2) To understand the measurements made in question 2.1 perform the following experiment to set voltages at two inputs V_+ and V_- to definite values:
a) $\mathbf{V_-}$: Using a simple resister divider set voltage at V_- terminal to 1V
b) $\mathbf{V_+}$: Use a potentiometer as a variable resistor divider to set a variable voltage at V_+ terminal
Verify these voltages independently with the DMM as you connect them to the $\mathbf{V_+}$ and $\mathbf{V_-}$ terminals.

What do you observe at V_{out} using the DMM as you vary V_+ from below 1V to above 1V? Record your observations here: **2**

$V_- = 1000mV = 1.000V$ is kept constant.
V_+ is slightly varied about 1V.
The circuit used for this purpose:



Observations: (maximum precision of V^+ is mV, even at max precision of DMM it is hard to make very fine variations using potentiometer.)

The Op-Amp saturates at $\simeq +7.28V$ or $\simeq -7.50V$ depending on sign of differential input.

V_+	$\Delta V = (V_+ - V_-)$	V_{out}
1022mV	22mV	7.28V
1008mV	8mV	7.28V
1001mV	1mV	7.21V
994mV	6mV	-7.49V
980mV	20mV	-7.50V
920mV	80mV	-7.54

Using a graphic arrow, indicate where V_+ (as measured with DMM) rises from below 1V to above 1V. Are you able to accurately correlate your V_+ setting to the observed transition in V_{out}? Why not? **2**

(You'd have to be a brave and patient experimenter to record in steps of μV!)

No, it is nearly impossible to make adjustments fine enough- of the order of μV using a potentiometer. The open loop Gain $G \sim 10^6$ implies that change in the differential input $(V_+ - V_-)$ of the order of μV leads to a change in the output of the order of Volts! With the assistance of the DMM it is possible to make changes of the order of mV in the V^+ value at best.

Maximum value of output voltage is reached when the transistors of the buffer stage saturate, thus giving $|V_{out|max}| \simeq V_{CC}$. This means that even a small differential input of the order of mV drives the V_{out} to $\simeq \pm V_{CC}$ $(sign\ depends\ on\ sign\ of\ V_+ - V_-)$, explaining the values obtained above.
(the approximate sign is used above taking into account the minute asymmetries in the supply voltages)

Question 3: Op-amp with feedback 10

From the experiments in question 2 it should be clear that an opamp running in "open loop" is a nearly useless device.

3.1: Reconfigure your circuit connections of question 2 as per the following diagram (not all wiring to $\pm V_{CC}$ and DSO probes is shown).
Note that the op-amp being a complex active IC requires it's $\pm V_{CC}$ power inputs to be bypassed by large electrolytic capacitors (choose 10 - 47µF) depending on availability. Make sure to connect each capacitor with its negative to a node that is at a *lesser* potential always than it's positive terminal – else you are liable to suffer a little 'poof' event on your breadboard!

Now the fixed resistor divider at V_- is no longer required.

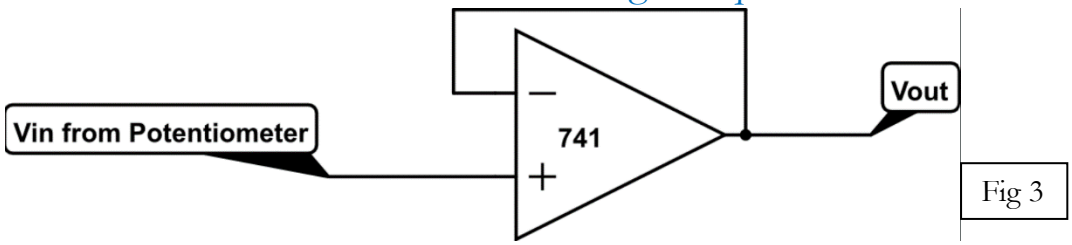


Fig 3

Note that by convention, the op-amp schematic symbol is drawn with V_- ("inverting" input) above and V_+ ("non-inverting" input) below.

3.1.1) Apply the governing equation of op-amp operation with $G \gg 1$ $(\sim 10^6)$ to work out the relation between V_{out} and V_{in} in the above circuit **2**

$$V_{out} = G(V^+ - V^-) = G(V_{in} - V_{out})$$

$$\Rightarrow V_{out} = \frac{G}{G+1} V_{in} \simeq V_{in} \quad (\because G \gg 1)$$

$$V_{out} \simeq V_{in}$$

3.1.2) Try the above circuit with four different values of potentiometer setting for different values of V_{in} and observe the corresponding V_{out}. Measure both V_{in} and V_{out} with your DMM. **2**

Do your readings match your expectations from 3.1.1 above?

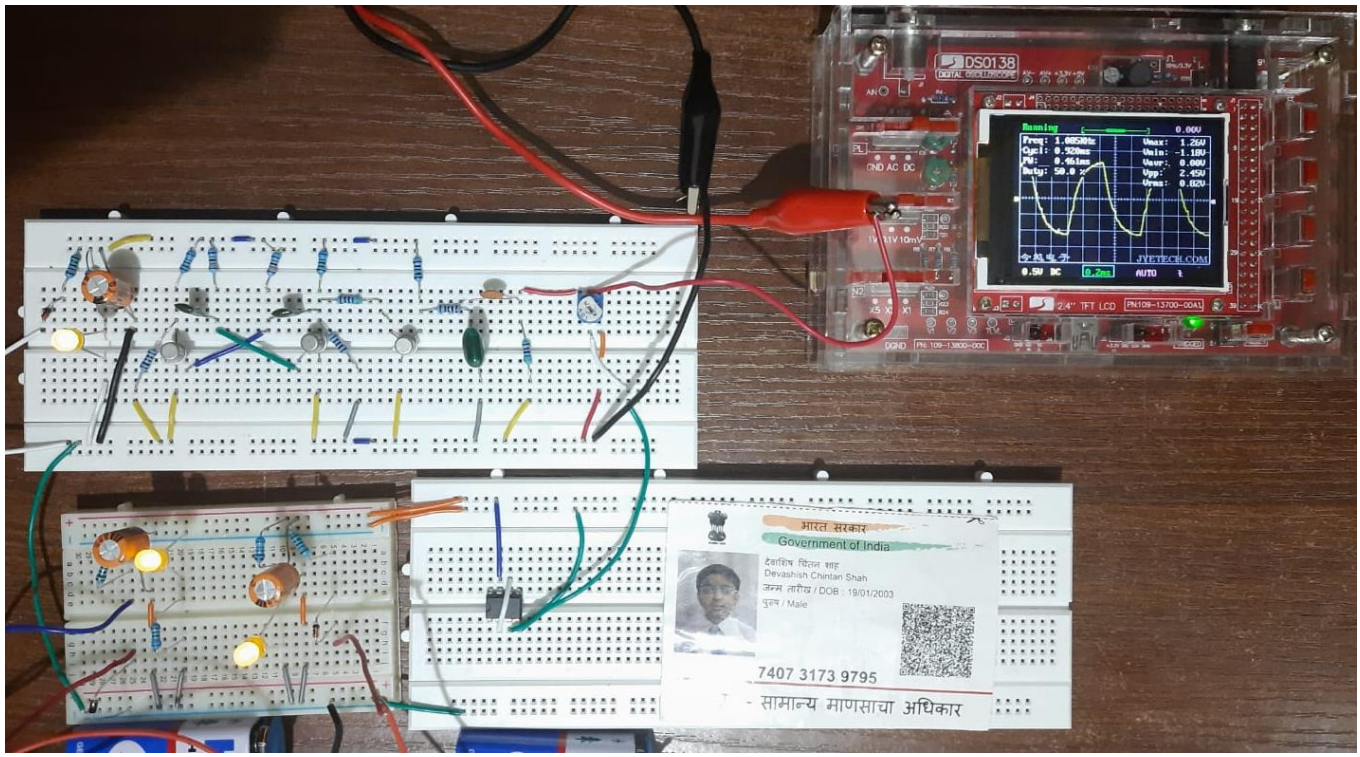
Yes, the observations agree with the theoretical expectations to a very high degree.

V_{in}	V_{out}
2.52V	2.49V
2.02V	2.01V
1.59V	1.54V
1.00V	1.01V

3.1.3) This would be a good time to dust off the astable multivibrator circuit built as a Function Generator (FG) from PH231 lab. Set the peak-to-peak output of the FG to some reasonable value, Replace the DC voltage V_{in} from potentiometer of 3.1.2 and connect output of the FG to V_{in} of the op-amp for a smoothly time-varying voltage waveform input. **6**

Record your photo readings of V_{in} (output of FG) and V_{out} from op-amp here (two side-side-side) photos expected, indicating which photo shows input V_{in} and which one shows V_{out}

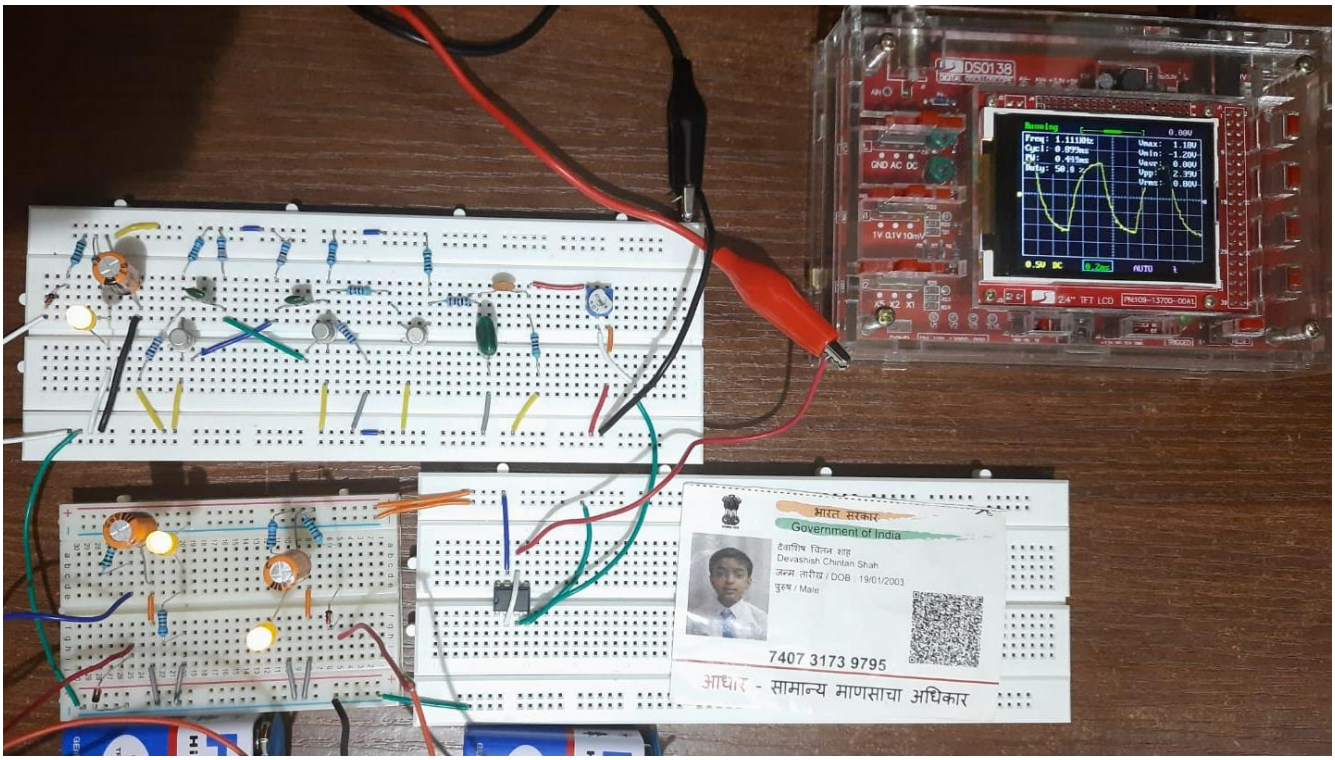
$$V_{in}: from\ potentiometer\ of\ FG$$



$$V_{in}: from\ potentiometer\ of\ FG, DSO\ zoomed\ in$$

$$V_{in|peak-peak} = 2.42V\ (read\ using\ grid)$$

$$V_{out}: from\ the\ OpAmp$$



$$V_{out}: from\ OpAmp, zoomed\ in\ DSO$$

$$V_{out|peak-peak} = 2.39V$$

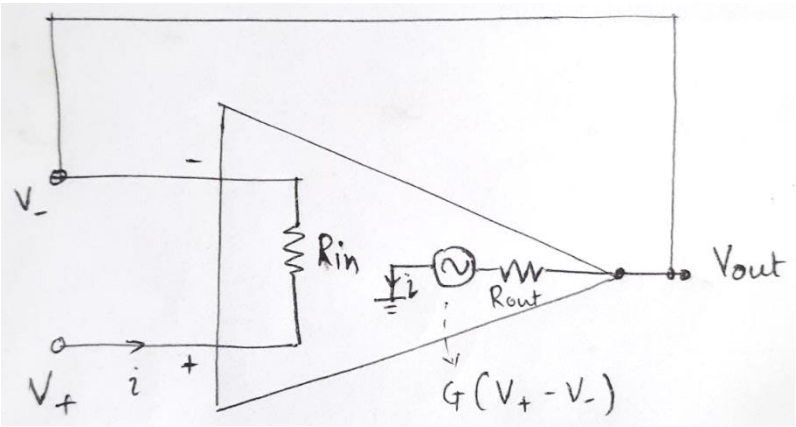
Indeed, the observations agree with the theoretical expressions, $V_{out} \simeq V_{in}$.

Question 4: Analysis of Op-Amp with feedback 5

Recall from our use of the Function Generator in PH231 that we often struggled with "loading" of its output by the input impedance of the circuit it was driving. The LTSpice simulation told us that for some value of the output 100kΩ potentiometer setting (say 30kΩ :70kΩ) the output amplitude should swing 0.3*3V = ±0.9V. But the experiments done in PH231 required a different potentiometer setting in practice due to impedance matching.

Analysis: 3

Calculate, with steps, the input impedance of the circuit of Fig 3 (Question 3)



$$Z_{in} = \frac{V_{in}}{i}$$

$$V_{in} - V_{out} = V_+ - V_- = iR_{in}$$

$$(eliminating\ i)$$

$$\Rightarrow Z_{in} = \frac{V_{in}R_{in}}{V_{in}-V_{out}}$$

$$V_{out} = G(V_{in} - V_{out}) \Rightarrow V_{in} = \frac{G+1}{G} V_{out}$$

$$\Rightarrow \boldsymbol{Z_{in} = (G+1)R_{in}}$$

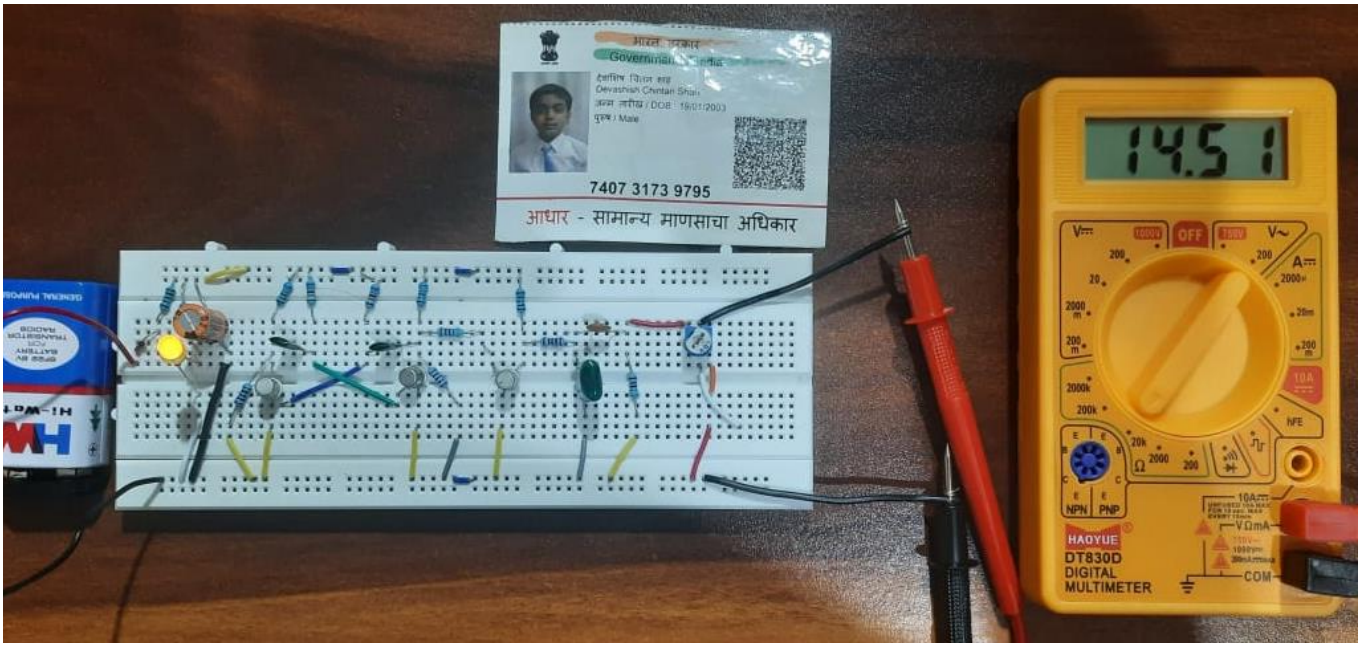
$R_{in} \sim 2M\Omega - 6\text{M}\Omega$ for an UA741 IC. Thus, Z_{in} is effectively infinite!

Demo: 2

Set the output potentiometer of the FG to a precise value (as measured by DMM) and check its value with DMM *before* connecting it to opamp circuit of Fig 3 (i.e. V_{in} of Question 3). Then measure the potentiometer value *after* connecting it to the opamp circuit, whose output V_{out} you have already measured in Question 3

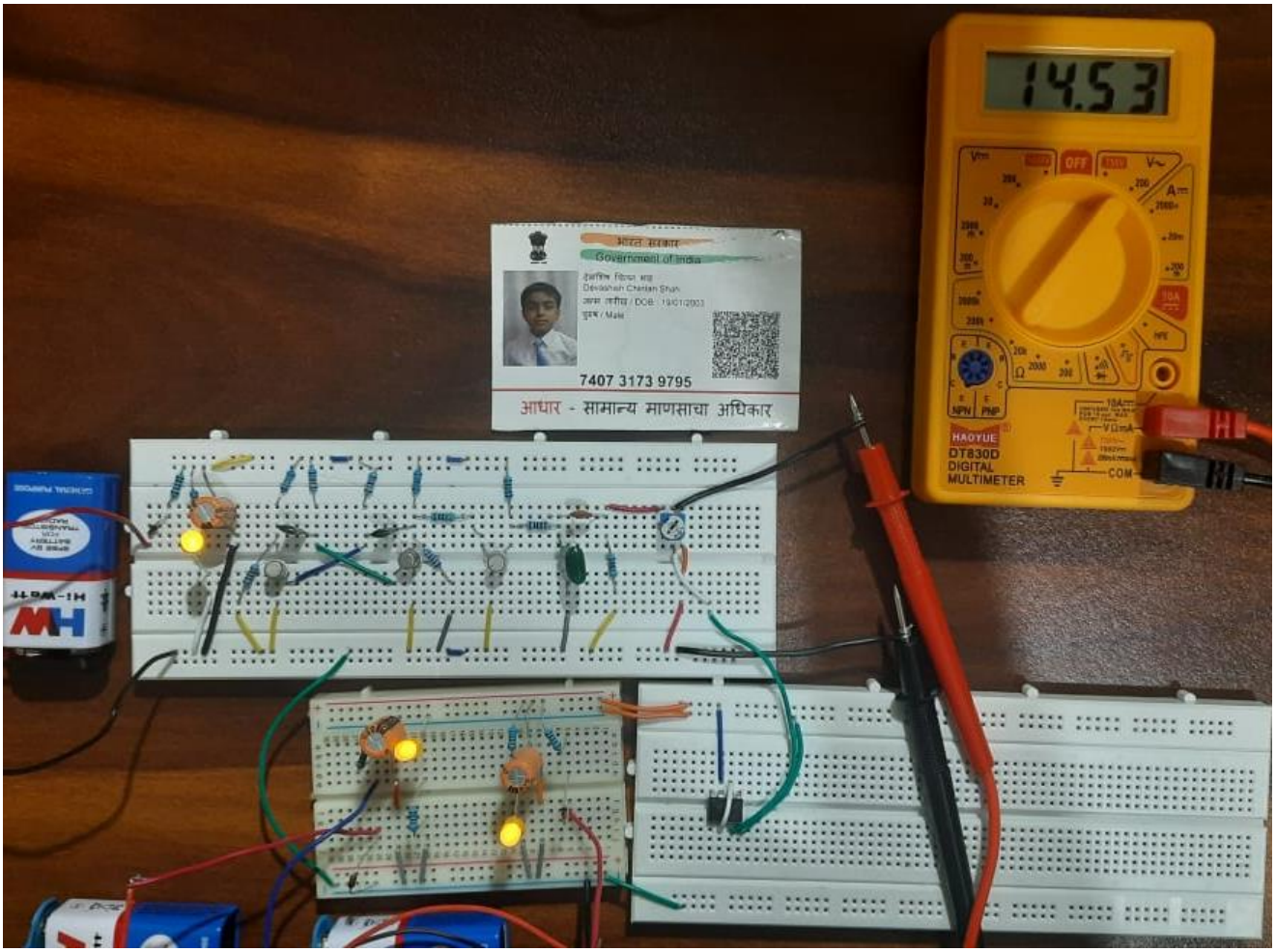
a) For this question, two photos of DMM measurement of potentiometer value are expected: labelled photos of the DMM measuring potentiometer values *before* and *after* connecting FG to the opamp circuit. These photos correspond to the DSO photos already put in Question 3 **(1 mark)**

R_2: Before connecting the potentiometer to the Op-Amp circuit: ($14.51k\Omega$)



R_2: The resistance value $R_2||Z_{in|opamp}$ is now measured, which is practically no different from R_2. R_2 in parallel to the Op-Amp input impedance which can be considered infinite for all practical purposes.

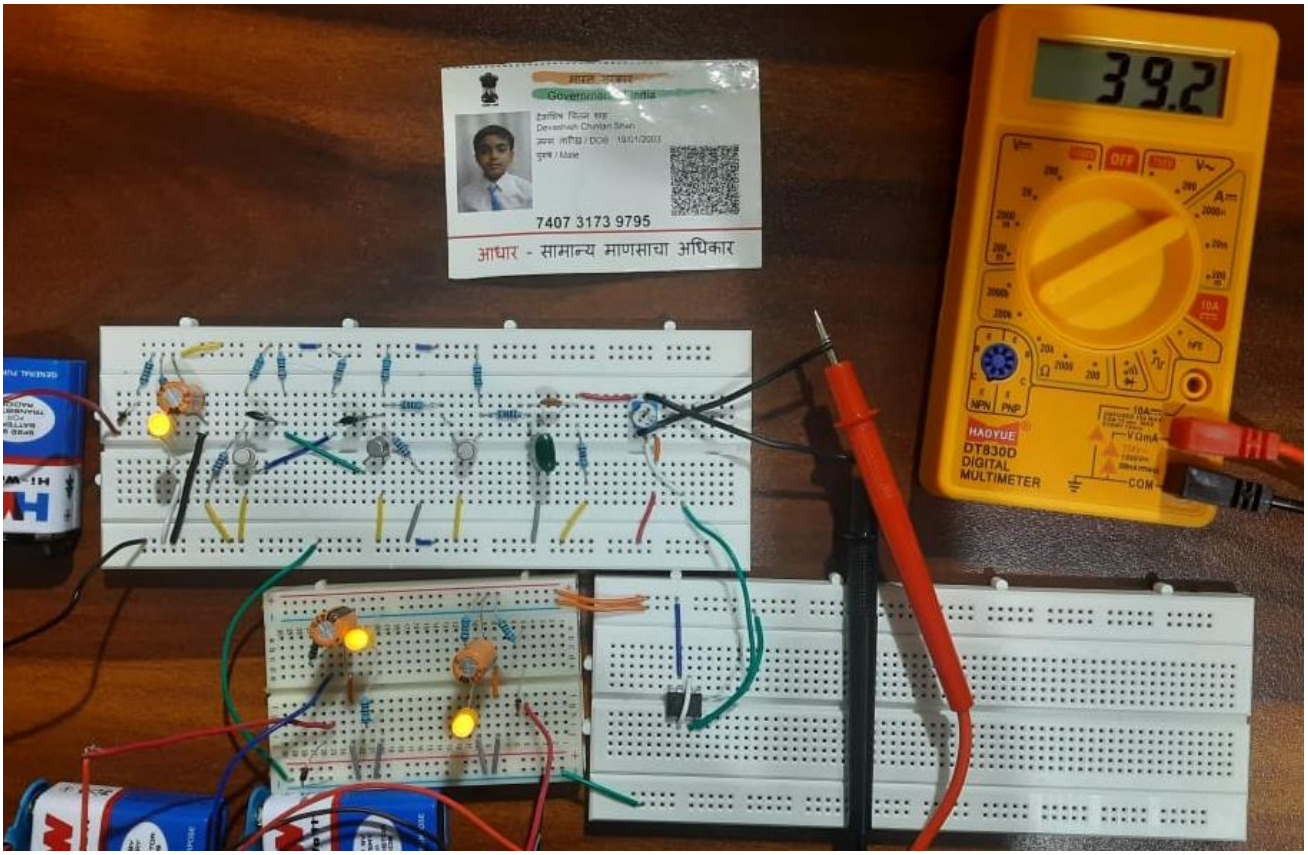
After connecting to the Op-Amp circuit: ($14.53k\Omega$)



$R_1||Z_{out|FG}$: Before connecting the potentiometer to the Op-Amp circuit: ($39.2k\Omega$)

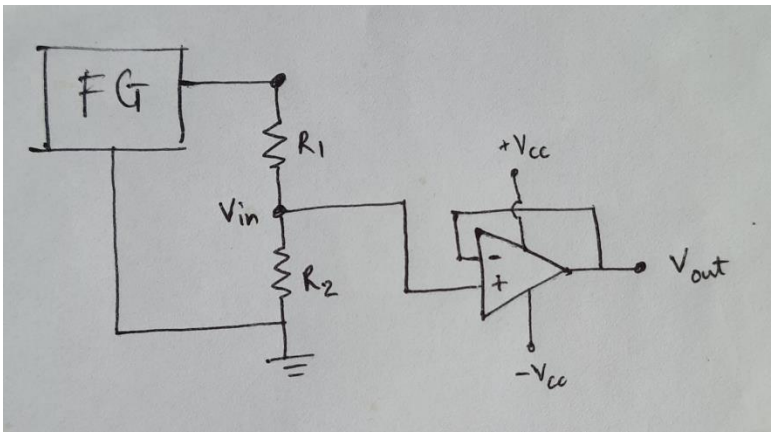
$R_1||Z_{out|FG}$: After connecting the potentiometer to the Op-Amp circuit: (39.2kΩ)

Unchanged as expected.



b) It has been pointed out in PH231 earlier that usually it is not recommended to measure passive component values while they are connected in a circuit – you end up measuring the value of the component in parallel with whatever other complex circuit it is embedded in. Then why is it OK to make the measurement in this question against standard recommended practice? What could go wrong?

(1 mark)



In this case we don't face any issues if we measure the resistance R_2 when connected in the circuit because it is in parallel to the Op-Amp.

The Op-Amp's input impedance is huge compared to the $\sim 15k\Omega$ value of the potentiometer's R_2.

One must make sure that the Op-Amp unity gain buffer (fig.3) is set up perfectly, else feeding the potentiometer output can not only drastically alter the DMM measurement but also damage the op-amp in some cases.