Lab 3: BJT as a current source: Emitter Follower Part 1 100

Prerequisite:

You must have a working simulation and physical implementation of a waveform **F**unction **G**enerator that swings to both positive and negative voltages, as worked out in Lab 1 + 2. We call this the FG for short throughout the rest of this lab.

The official standardized design is published on moodle – use those component values to get a reliable output and test that your FG works as expected.

Settings for LTSpice: Use the following timing parameters in LTSpice simulation command

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Stop time = 101m
Time to start saving data = 100m
Maximum time step = 0.01m
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This skips the initial transients in the first 10ms of simulation caused by calculation artefacts, capacitive charging etc and gives you a stable picture of one full cycle (1ms from 100ms to 101ms) of V_{in} @ $f \sim 1kHz$

Grand goal:

Design a BJT based circuit that has no voltage gain, but is able to amplify a small input current to a large output current. In terms of impedance, it means that the final circuit design must have very high input impedance and very low output impedance. This is very attractive for practical applications, since most electro-mechanical devices are driven by current.

Note about terminology of 'current' used in this assignment:

1) We consider the traditional Kirchoff's Law current I in the circuit design and analysis. This current can be flowing in either direction across two nodes in a circuit. Though as explained in the introduction session, inside an NPN/PNP transistor, the current I flows exclusively from the Collector to the Emitter.
2) The term AC current used here refers to a time-varying current, and is denoted in small case i. In contrast, a DC current denoted by capital letter I is one whose value remains constant with time. Generalizing, a DC voltage is one which is constant in time (like the 9V supply to your circuit), and an AC voltage is one which varies as a function of time, like the output of your FG.
3) If V_{out} is supplying current to the load, we say the circuit is 'sourcing current'. Vice-versa, if current is being pulled *into* the circuit from the load, we say the circuit is 'sinking current'

Part (A) Circuit Design

Fig 1 shows the basic structure of a current amplifier circuit. Since $I_C = \beta I_B$ this is a 'skeleton' of the circuit. Solve questions below at Level 0 and Level 1 to 'flesh' out the circuit with all the other required components

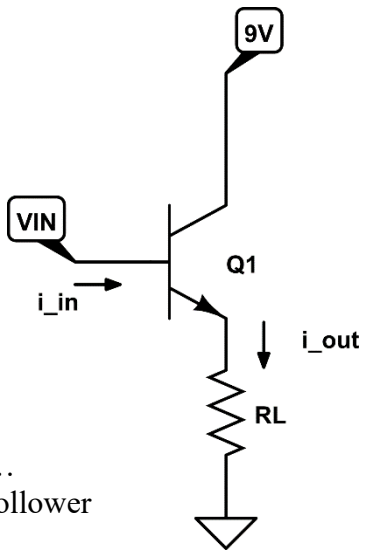


Fig 1:
The BJT current amplifier…
Basic principle of emitter follower

Level 0: The "crack" 5

If V_{in} is an AC voltage whose value can be both positive and negative,

0.1 What are the assumed conditions required for $i_{out} = \beta i_{in}$? **1**

List constraints on the operating mode of Q1, and safety limits on the currents and voltage differences (refer datasheet for BC107)

1) For the circuit to operate as a current amplifier, first of all it must operate in the Active region i.e., the BE junction must be forward biased and the CB junction reverse biased.
2) The optimal value for the operating point will be in the center of the active region i.e., $V_E \simeq \frac{V_{CC}}{2}$. Thus, the emitter resistor must be chosen taking this into consideration.
3) The current I_C must not exceed the safe limit.

The absolute max ratings as per datasheet for BC107:

$$V_{\mathrm{CE}} < V_{\mathrm{CE|max}} = 45V$$
$$V_{\mathrm{CB}} < V_{\mathrm{CB|max}} = 50V$$
$$V_{\mathrm{EB}} < V_{\mathrm{EB|max}} = 6V\ (reverse\ bias\ breakdown)$$
$$I_c < I_{\mathrm{C\,|max}} = 200mA$$

0.2 What are the necessary absolute and relative voltage conditions required at the C, B, E terminals of Q1 to use it as a current amplifier? **1**

General inequality: $V_C(= V_{\mathrm{CC}}) > V_B(V_{\mathrm{in}}) > V_E > 0$.
In active region $I_E \simeq I_C \gg I_B$
Thus, $V_{\mathrm{BE}} > 0.7V$ to maintain CB forward bias.
Thus, $V_{\mathrm{CB}} > 0.7V$ to maintain CB reverse bias. (C is N and B is P)

0.3 Including the load R_L as a part of your circuit is always a recipe for disaster. Will the circuit still work as a current amplifier as per design specifications if the following things happen? (explain your answers with full detail)

a) if R_L burns out? In electrical terms, $R_L \to \infty$? **1**
Are conditions 0.1 and 0.2 above fulfilled? What is power delivered to load?

No, the conditions aren't met. The load acts as an open switch $I_E = 0$, thus the amplifier doesn't function.
Relevant biasing requirements are also not met.

Or

b) R_L short-circuits due to Q1-E accidently touching GND? **1**
Which conditions in 0.1 and 0.2 above violated?

The voltage of the emitter terminal drops down to 0V, thus the transistor is no more in the middle of the active region and is easily driven to saturation (if $V_{\mathrm{B}} > 0.7V$) and cutoff (if $V_{\mathrm{B}} < 0.7V$).
Also, I_C might exceed the safety limit (damaging the transistor) if the base voltage exceeds a small positive value.

Or

R_L is frequency dependent, i.e., the corresponding impedance $Z_L =$

$f(\omega)$ where $f(\omega) \sim \frac{1}{\omega}$ or $f(\omega) \sim \omega$? **1**

The R_L plays a major role in setting the value of V_E. If R_L is frequency dependent the optimal Collector-Emitter voltage drop will be obtained only for a particular frequency, any frequency change will change $R_L(\omega)$ which will drive the Q-point to one of the two extreme cases. In short this will result in an unstable Q-point leading to unstable I_E.

Level 1: Basic Design **15**

After having understood the limitations of the skeleton circuit of Fig 1 in Level 0 design a practical current amplifier using 1 NPN transistor with the following design parameters:

1. deliver PEAK power to load_____ = 5mW
2. Assume purely resistive load R_L_____ = 500Ω
3. V_{CC} _____ = 9V
4. Amplifier has a high-pass f_{3dB}_____ = 100 Hz
   (i.e. noise in V_{in} below 100Hz will be rejected)
5. Transistor β_____ = 300

Typical application scenario: an audio amplifier for headphones. The coil driving the speaker diaphragm in your headphones has $\mathcal{O}(100\Omega)$ resistance. Given the small size of the speaker in the headphone, 5mW peak power should drive it up to ear-splitting volume.

You will find that with the basic design, the amplifier circuit itself consumes power from V_{CC} *even if there is no* V_{in} applied. We will calculate this idle power dissipation, and ways to avoid it in Level 2 and Level 3

Here is the step-by-step design procedure:

From cracking Level 0, it is obvious that the BJT terminal voltages must be setup such that it always remains in the forward-active operation mode. Here are ways in which this can be accomplished, without too much complexity:

DC Design: Give your calculation steps for each of the questions

below

PLEASE NOTE: The FG built in the first two labs has a stable $V_{CC} = 8.3V$ which is what will be used in the Hardware part. Thus, keeping this in mind the calculations are done using this value.

1) Pick a value of I_C that must flow at the 'quiet' operating point. This is called the quiescent current I_{CQ}. Even when V_{in} is 0, the transistor must be ready to supply a range $I_{CQ} \pm \delta I$.

Choose I_{CQ} = 10mA

Since PEAK power delivery is specified, What δI do you expect to deliver to the load *if* the load were directly connected to E as in Fig 1? **1**

Peak power above the stable quiescent supply: $P_{max} = \delta I^2 R$

$\delta I = \sqrt{\frac{5mW}{500\Omega}}$ =3.2mA

2) You *don't* want to include R_L in the core circuit of your amplifier! Yet you must use a resistor at the emitter to fix a DC value of V_E. Call this resistor R_E and calculate its value to set the DC value of V_E to be approximately half of V_{CC}. What is R_E? **1**

The function generator built has a stable $V_{CC} = 8.3V$.

For 10mA quiescent collector current and DC voltage $V_E = \frac{8.3}{2}V = 4.15V$.

$$R_E = \frac{V_E}{I_{CQ}} = 415\Omega \; (used \; 430k\Omega)$$

The kit provided for hardware has resistors of value $330\Omega \; and \; 100\Omega$ which are the combination of resistor values required in series!

3) Use a resistor divider with resistors R_{B1} & R_{B2} to set the bias voltage V_B such that BE junction is always forward biased. There are three competing considerations in choosing suitable values of R_{B1} & R_{B2}

a. Base current I_B at DC must be kept very small ~ $\frac{I_Q}{\beta}$ When the BE junction is forward biased, it has an equivalent resistance of $r_e = \frac{25mV}{I_Q}$

The effective resistance 'looking into' the base is thus $R_B = \beta(r_e + R_E)$

R_{B1} in series with R_{B2} must provide a preferred current path to ground from V_{CC} than R_B. i.e. $(R_{B1}||R_{B2}) \ll R_B$

b. R_{B1} and R_{B2} are in series from V_{CC} to ground, hence this path will *always* pass DC current and contribute to the amplifier's idle power dissipation.

c. R_{B1} & R_{B2} will play a role in the f_{3dB} = 100Hz filter so you might have to iterate with the AC design below:

What is your choice of R_{B1} & R_{B2} ? **1**

$r_e = \frac{25mV}{I_Q} = 2.5\Omega$. $R_{B1}||R_{B2} \ll 300(R_E + 2.5\Omega) \simeq 124.5k\Omega$.

We need to consider tradeoff between a) and b). For optimal power consumption as well as for small I_B.
First of all: $V_{BQ} = 4.85V$ which means that the voltage divider must be designed such that:

$$8.3V\left(\frac{R_{B2}}{R_{B2}+R_{B1}}\right) = 4.85V \rightarrow \frac{R_{B1}}{R_{B2}} = 0.711$$

$R_{B1} = 15k\Omega \; and \; R_{B2} = 22k\Omega$

AC Design:

We want the amplifier to have a high-pass filter at f_{3dB} = 100Hz. Keeping the core DC amplifier design as finalized above, we can add on high pass filters at the input and output.

4) It is easier to start at the output side. Add a single component high pass filter before R_L. What is the value of this component? **1**

$f_{3dB} = 100Hz = \frac{1}{2\pi R_L C_L}$. Thus, the capacitor to be added will be $C_L = 3.2\mu F \simeq 3.3\mu F$ $(3.3\mu F \; given \; in \; kit)$

5) Now at the input side, we must take into account the entire input impedance of the amplifier circuit (*including R_L reflected through the amplifier)*
Take this input impedance to be $R_{inp} = (R_{B1}||R_{B2})||\beta(r_e + R_E||R_L)$
Calculate R_{inp} with the previously chosen component values

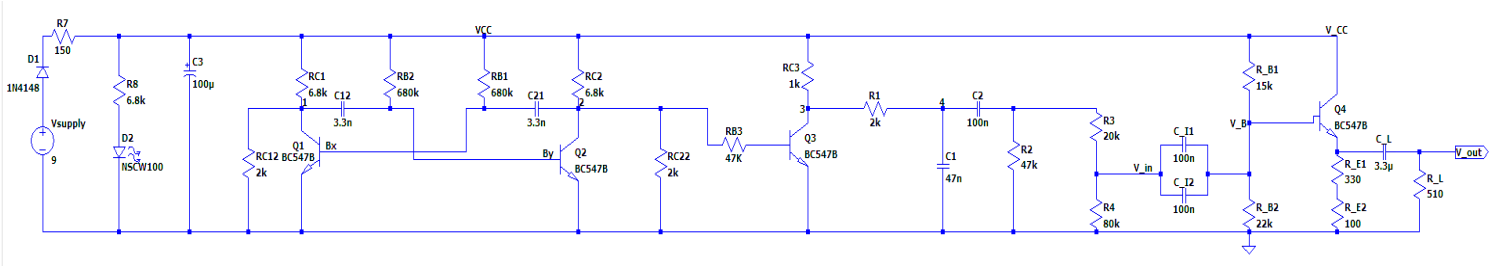
$$R_{inp} = (R_{B1}||R_{B2})||\beta(r_e + R_E||R_L) = (8.9k\Omega)||(68.8k\Omega) = 7.88k\Omega$$

Accordingly add a single component series high pass filter for f_{3dB}=100Hz. What is the value of this component? **1**

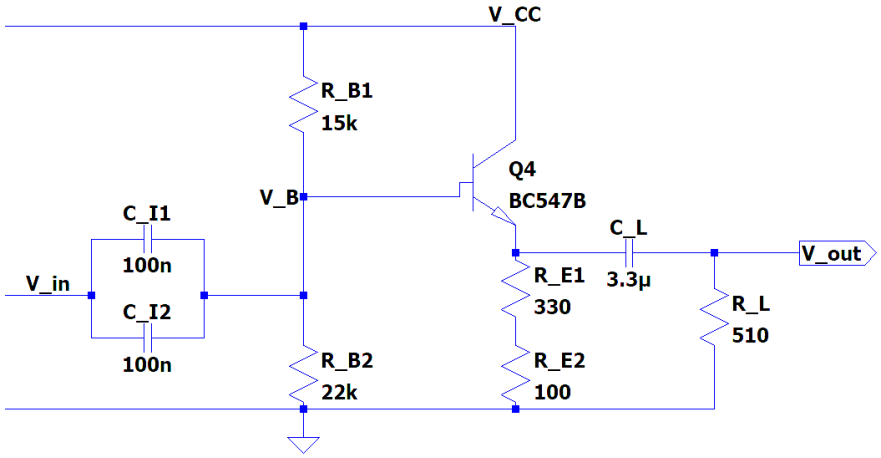
$f_{3dB} = \frac{1}{2\pi R_{inp} C_I} \rightarrow C_I = \frac{1}{2\pi R_{inp} f_{3dB}} = 202nF (\simeq 100nF \; in \; parallel \; with \; 100nF)$

Paste a circuit diagram of the current amplifier created in LTSpice as per the

above design calculations here. Provide the simulated test results: **10**



The Emitter Follower part added to the FG:



The potential divider (block-5) is selected so as to provide a +/-0.5V peak-peak V_{in}.

Simulations:

Use the FG simulation done earlier to provide V_{in} to your amplifier circuit. This will be a frequency $f \sim 1.17kHz$ so it should sail through the 100Hz high-pass cutoff frequency of your amplifier.

Specify V_{in} to have a pk-pk signal of 1V, centered around 0V. i.e. V_{in} should swing between +0.5V and –0.5V. Measure current delivered to the load R_L both as a current probe in LTSpice, and the voltage across R_L which you will measure in the circuit demo

Put your simulation output plots here:

Expected plots:

1) For V_{in} = 1V pk-pk (i.e. ±0.5V)

a. Plot Voltage gain **10**

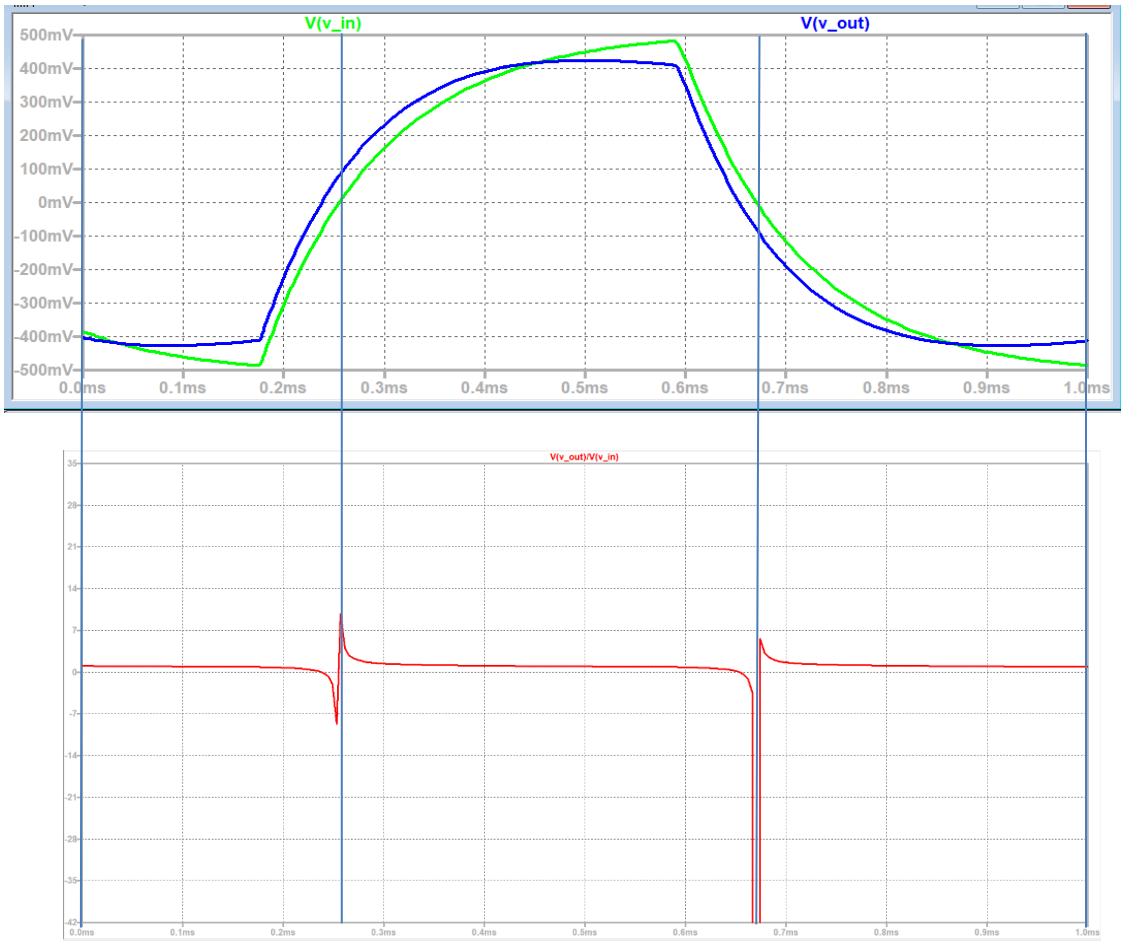
For $V_{in|peak-peak} = 1V$ (±500mV)

the $V_{out|peak-peak} = 860mV$(±430mV)

Note: here A_V should not be taken to be the ratio between peak values, rather we consider the stable values obtained from the voltage gain plot. This is because the output waveform is not linearly dependent on the input rather some minute nonlinearities alter the shape of the curve.

Voltage gain (ignoring distortions in the waveform itself)

$$A_V = 0.95$$



The voltage gain plotted above is as expected with stable value of ≃ 1 with peaks and valleys at instants when V_{in} is 0V. This is because of the minute phase difference introduced in V_{out} *and* V_{in} due to the two high pass filters.

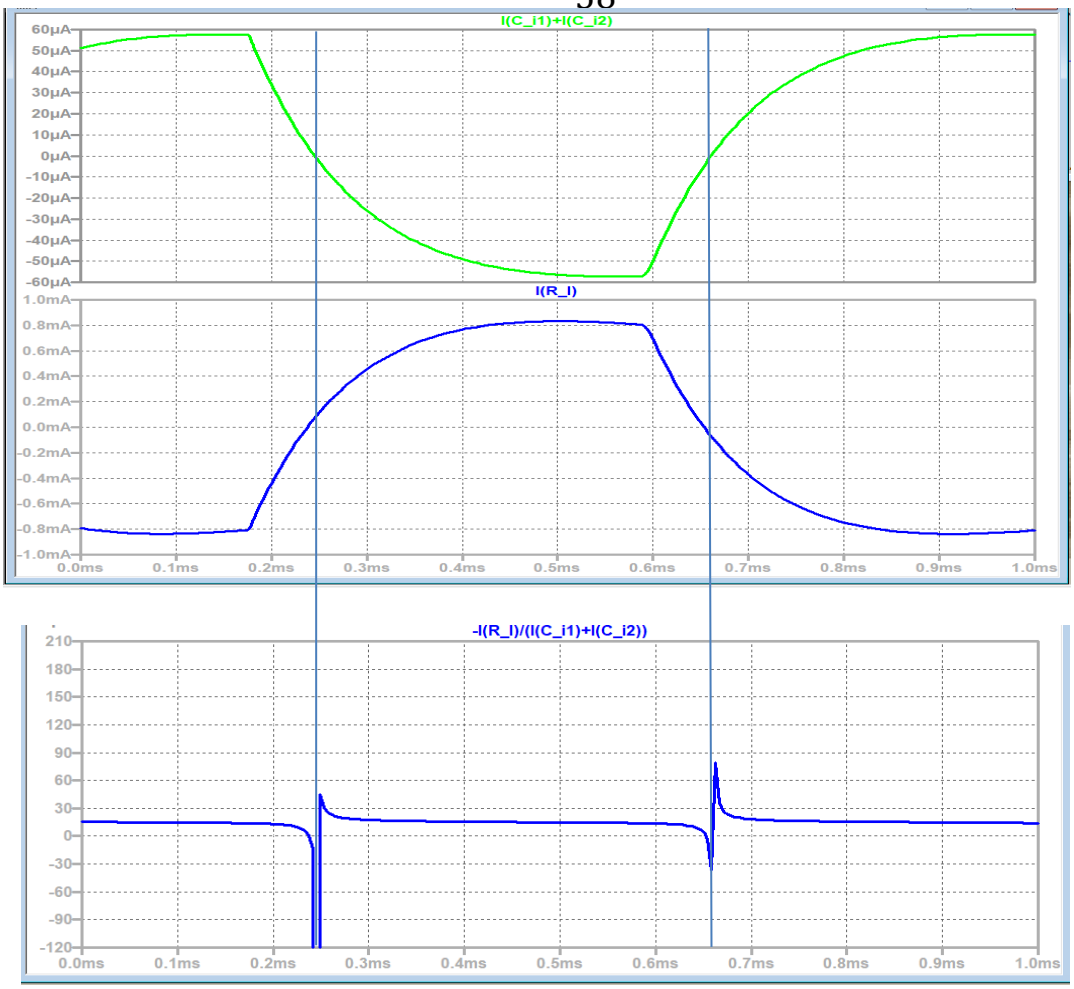
Phase shift $\phi = tan^{-1}\left(\frac{1}{2\pi RCf}\right)$ where f is 1.1kHz of our FG.

Net phase shift $\phi = \phi_I + \phi_L$

b. Plot Current gain **10**

For $I_{in|peak-peak} = I_{C_{I1}|peak-peak} + I_{C_{I2}|peak-peak} \simeq 116\mu A$ (±58μA) the $I_{L|peak-peak} = 1.720mA$ (±0.860mA)
Current gain is:

$$A_I = \frac{860}{58} = 14.82$$



The steady current gain is as mentioned (14.82) with sudden spikes at points when I_{in} becomes 0. This is again as expected because of the minute phase difference between the two.
The LTSpice probe measures the input current through the capacitor in the opposite direction giving the apparent out of phase simulations. In reality the currents are also phase shifted only by a small phase as the voltages.

Do these match the calculated values? If not, why not? **10**

They don't match the calculated values exactly but are acceptable within experimental bounds. These minor deviations are due to certain idealizations assumed combined with the non-linearities observed in practice.

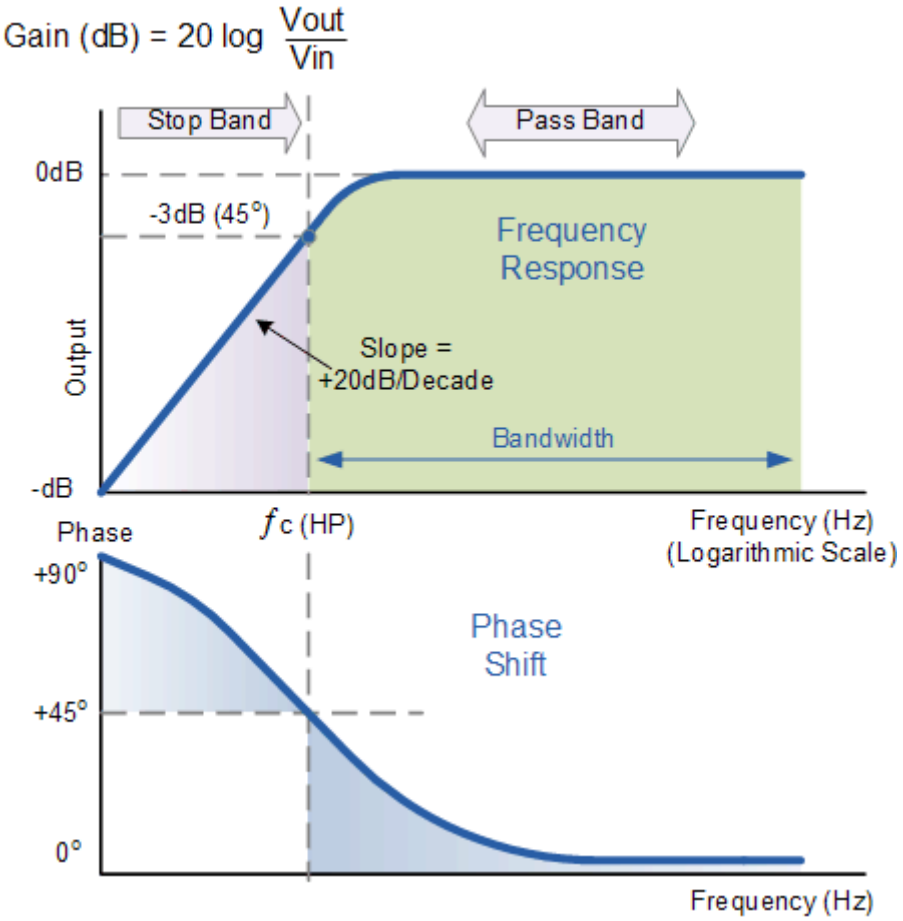
Calculated Values:

Voltage gain: $A_V = \frac{V_{out}}{V_{in}} = \frac{(R_E||R_L)}{r_e+(R_E||R_L)} \simeq 1$

Current: $A_I = \frac{i_{out}}{i_{in}} = \frac{V_{out}R_{in}}{R_L V_{in}} = \frac{R_{in}}{R_E||\left(r_e+\frac{(R_{B1}||R_{B2})}{\beta}\right)} A_V \simeq \frac{7880}{500} = 15.76$

c. Explain the relative phase between input and output voltage & current **10**

A small phase shift is observed between the input and the output voltage and current. This is because of the phase shift introduced by the two high pass filters. Phase shift for a passive high pass filter with resistor R and capacitor C is $\phi = tan^{-1}\left(\frac{1}{2\pi RCf}\right)$ where f is 1.1kHz of our FG. The figure below shows how his phase shift varies with frequency.



Net phase shift $\phi = \phi_I + \phi_L = tan^{-1}\left(\frac{1}{2\pi R_{in} C_I f}\right) + tan^{-1}\left(\frac{1}{2\pi R_L C_L f}\right) \simeq 10^{\circ}$

2) Keep increasing V_{in} by adjusting the potentiometer until you achieve the design goal of delivering 5mW. What is the V_{in} required to achieve this goal?

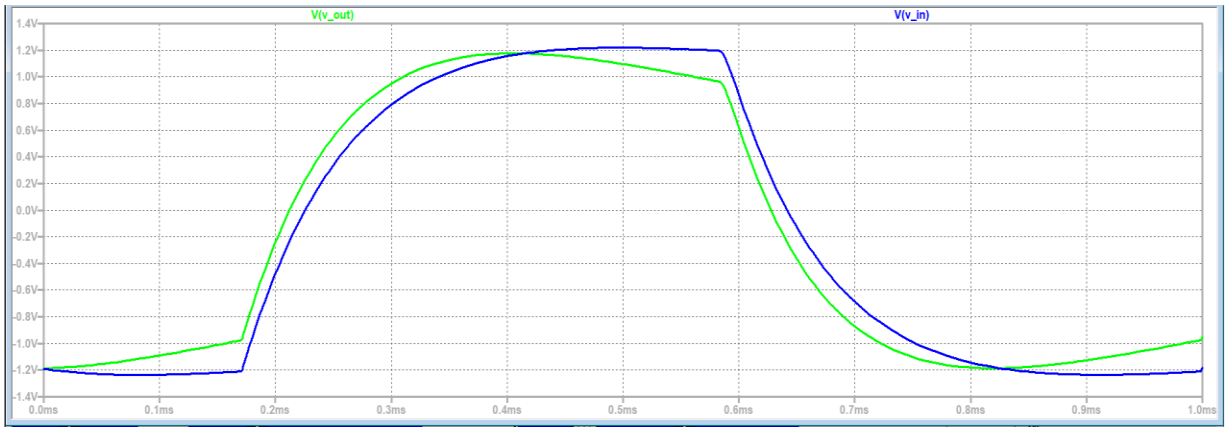
At V_{in} set to achieve peak power delivery condition:

For the design goal of 5mW power delivery δI=3.2mA, which means 6.4mA peak to peak. The closest peak-peak variation we can get to this maximum is the value of I_L when the CC amplifier is connected to the $100k\Omega$.

a. Plot Voltage Gain **5**

For $V_{out|peak-peak} = 2.352V$ (±1.176V)
the $V_{in|peak-peak} = 2.450V$ (±1.225V)
Voltage gain (ignoring distortions in the waveform itself)

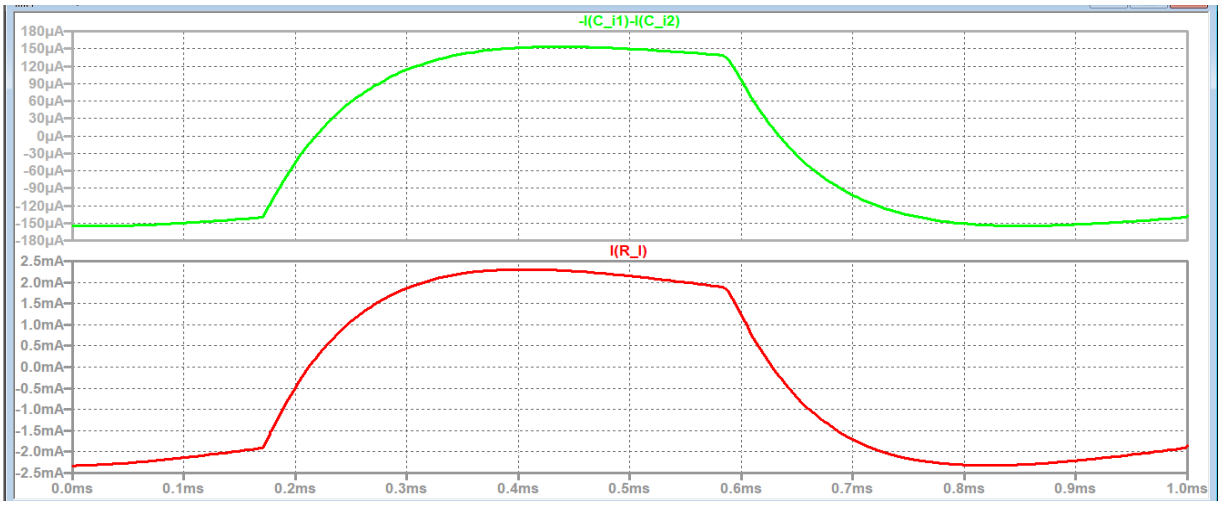
$$A_V = \frac{1.176}{1.225} = 0.96$$



b. Plot Current Gain **5**

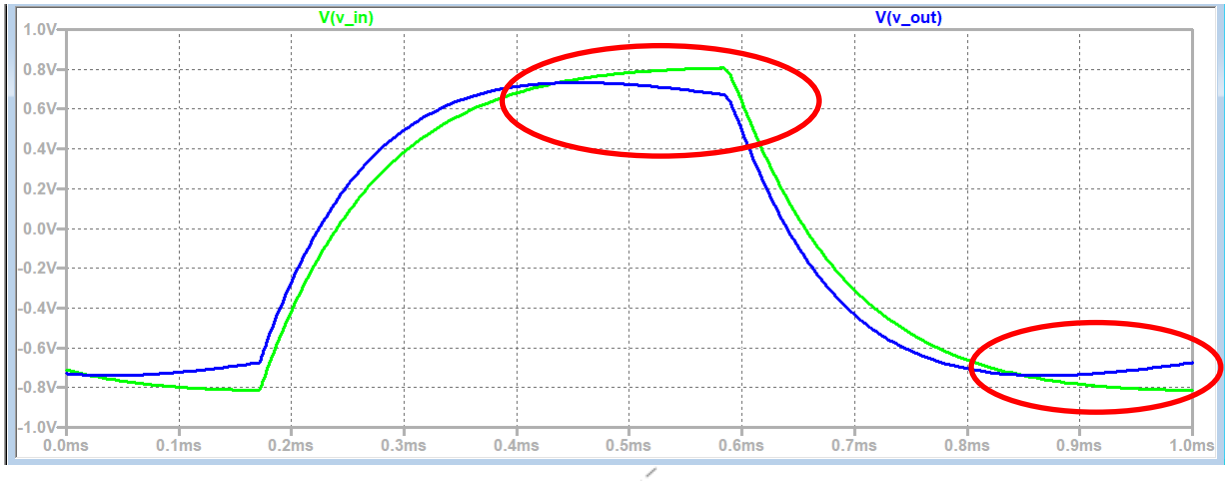
For $I_{in|peak-peak} = I_{C_{I1}|peak-peak} + I_{C_{I2}|peak-peak} \simeq 310\mu A$ (±155μA) the $I_{L|peak-peak} = 4.62mA$ (±2.31mA)
Current gain (ignoring distortions in the waveform itself)

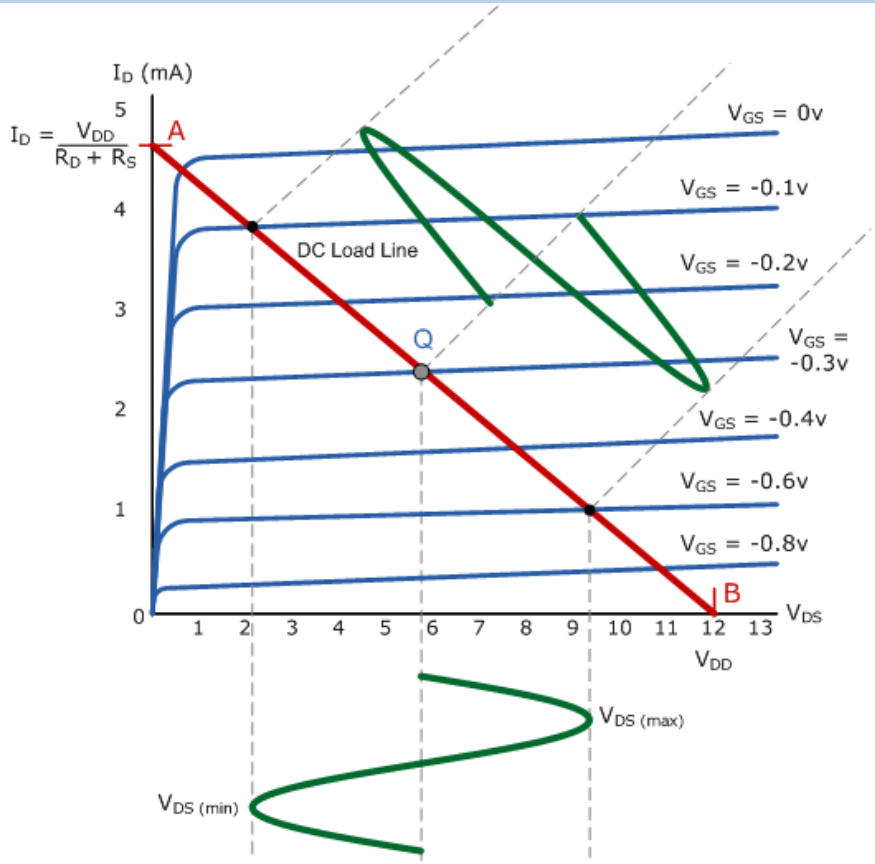
$$A_I = \frac{4620}{310} = 14.9$$



c. Is there any non-linearity in (a) and (b)? If so, explain when and why the non-linearity occurs (refer to the constraints of operation we specified back in Level 0!) **10**
– what is the region of the $I_{C|Q1}/V_{CE|Q1}$) characteristic your circuit is approaching when the non-linearity occurs?

It is clear from the graph of V_{out} *and* V_{in} that the non-linearities occur when these voltages are near their negative or positive peak values.





For ideal amplifier action the swing must be as small as possible so that total voltage (AC+DC) across the CE junction doesn't vary much about the Q-point value of $\frac{V_{CC}}{2}$. Thus, the non-linear behavior is observed because of the fact that the transistor approaches the edges of the active region when the voltage swing is maximum. That is when I_C /V_{CE} approaches the cutoff or saturation regions of the I/V characteristic.