University of Glasgow

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ENG5092 – VLSI Design

Lab report

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INTRODUCTION:

In the past, analogue filters were designed using OPAMPs whose bandwidth (BW) was limited by the gain-bandwidth product which limited the ability to get the ideal filter response. This technology process also consumed more power. Therefore, OTAs are used in place of OPAMPs. OTA's are also used as Low Noise Amplifiers (LNA) which have high gain and less noise (good Singal to Noise Ratio (SNR)). Therefore, OTA's play an integral role in the analogue front end of low-power systems.

An OTA is a Differential Voltage Controlled Current Source (DVCCS) which converts the differential input voltage to an output current.

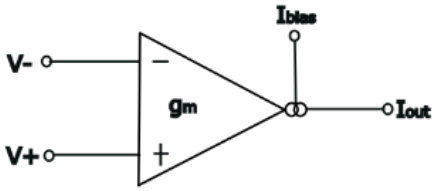

Figure 1: Symbol of an OTA

BACKGROUND AND SCHEMATIC ANALYSIS-

An Integrated Circuit (IC) contains analogue and digital cells which operate on the same supply voltage range. To make the analogue circuits work in this range it is operated in the subthreshold region or weak inversion region.

- The input stage of the schematic is similar to a PMOS differential pair circuit consisting of a PMOS current mirror which sets the I_{bias} (MP5 and MP6) and 2 PMOS differential inputs V- and V+ (MP1 and MP2) with an amplification stage formed by MP4 and MN4.
- The V+ and V- are converted into a differential current signal I_1 and I_2.
- MOSFET's MN1 and MN2 are active load transistors for the differential current signals I_1 and I_2 which results in lower operating current resulting in lower g_m and increased linearity.
- Therefore, the gain of the OTA is given by:

$$\boldsymbol{Av = \frac{\beta . gm, MP1}{gds, MP4 + gds, MN4}}$$

- Where g_{ds} is the conductance between the drain and source. From the above equation we can see that the high gain requirement leads to a multistage design with long channel MOSFETS biased at low current levels this degrades the frequency of operation but can be easily avoided using partial feedback between MP1 and MP2 (not done in this design) to enhance the output impedance of the amplifier.
- As shown in Figure 2, MP1 and MP2 operate in the subthreshold voltage region, the differential current output is given as:

$$\boldsymbol{I_{out} = \beta\left(I_{D,MP2} - I_{D,MP1}\right) = \beta(I_2 - I_1) = \beta I_{BIAS}\left(\frac{\frac{I_2}{I_1} - 1}{\frac{I_2}{I_1} + 1}\right)}$$

OR

$$\boldsymbol{I_{out} = g_m V_{in}}$$

Where $\boldsymbol{\frac{I_2}{I_1} = e^{\frac{-V_{in}}{nV_T}}}$ and $\boldsymbol{V_{in} = (V+) - (V-)}$

- Based on the above equations we can define the transconductance of the OTA as:

$$\boldsymbol{g_m = \frac{\partial I_{out}}{\partial V_{in}} = \frac{\beta I_{BIAS}}{2nV_T}}$$

- We can conclude that the **transconductance (g_m)** of the OTA is controlled by the setup current I_{BIAS} which means the **output current I_{out}** is proportional to the **input voltage V_{in}** .
- MP5 and MP6 make up the I_{bias} circuit (current mirror) having the same (W/L) ratio. Thus, the current set at MP5 is mirrored and outputted at the drain of MP6. They have the largest (W/L) ratio as the mobility of PMOS (μ_p) is lesser than that of NMOS and a sufficient amount of current needs to flow through for the entire circuit to operate.
- The differential input PMOS (MP1 and MP2) have twice the width of the NMOS active loads (MN1 and MN2) as the mobility of charge carriers of PMOS (μ_p) is lower than that of NMOS charge carriers(μ_n). PMOS is preferred as it has better noise performance.
- The number of fingers for each of the MOSFETs is discussed later in the layout section.
- We can divide the OTA schematic into 3 main sections:
    1. I_{bias} current mirror circuit (MP5 and MP6).
    2. Differential input stage with NMOS active loads (MP1 and MP2, MN1 and MN2).
    3. NMOS Common Source Amplification Stage (MN4 (Amplifying MOS), MP4 and MP3(PMOS current mirror active load)).

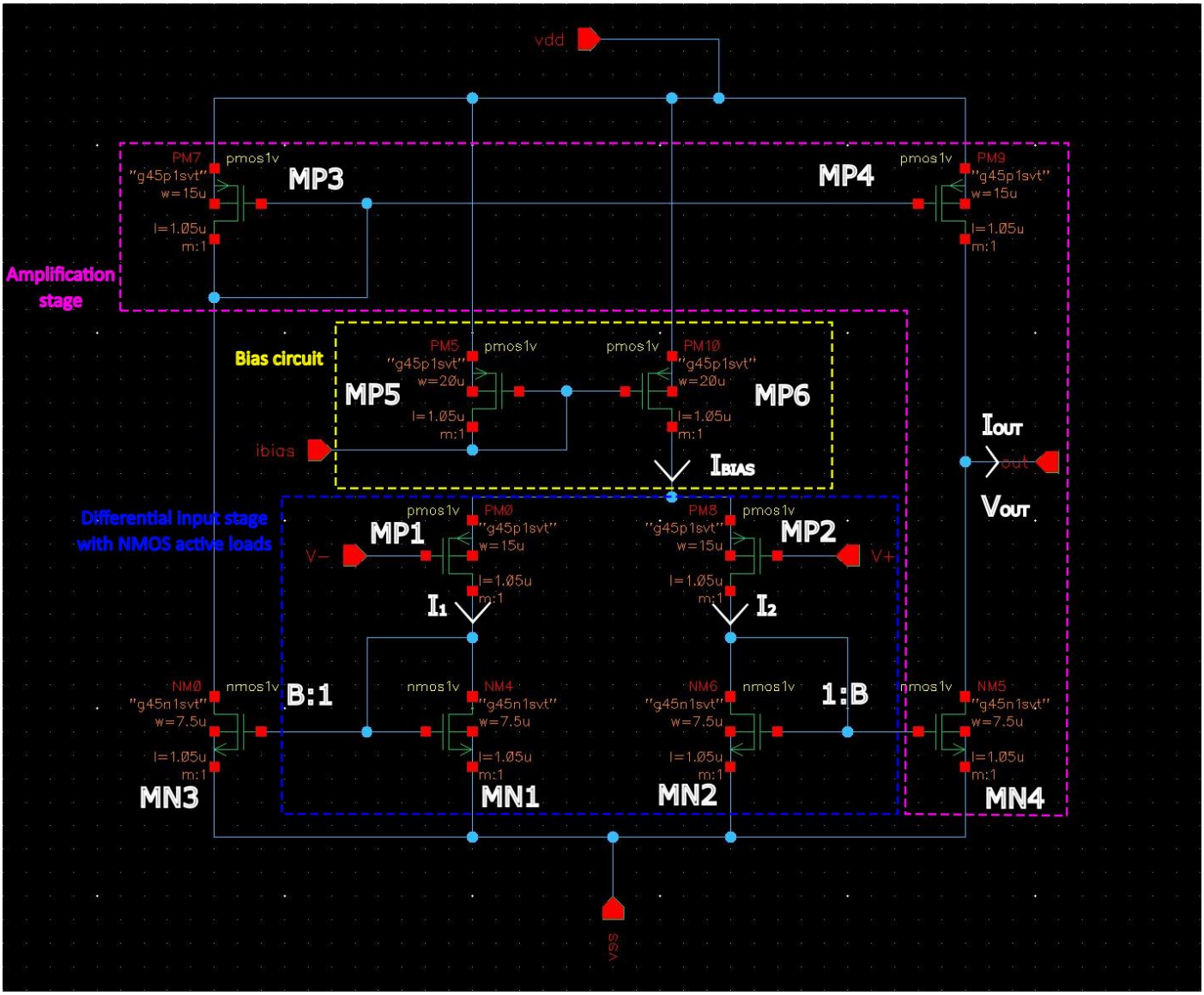

Figure 2: Schematic of OTA

SIMULATION CIRCUIT-

- I_{BIAS}(Also called amplifier bias current) set to 10uA which is such that it would result in a low gm and unity gain (A_v=1). The small transconductance means the output impedance must be high so that the output current I_{out} can be read as a voltage across the resistor.
- The output impedance at 1000Hz for the parallel RC is:|Z| = 79.577kΩ
- OTA's drive-only capacitive loads (connected to the gate terminal) therefore a capacitor is connected to emulate a gate connection of the next stage.
- The differential input of the OTA as discussed before needs to operate in the subthreshold or weak inversion region. The MOSFET can be kept in the weak inversion region by having the gate-to-source voltage slightly lower than the threshold voltage. In this region, the transistor saturates when V_{ds} > 3 to 4V_T. In general, the saturation voltage of the MOS is lower than that of a MOS working in strong inversion.

$$|V_{gs}| < |V_{th}|$$

- The input voltage is offset by 500mv with peak V_a=200mV. The peak-to-peak V_{peak}=400mV. Therefore, the input swings between 700mV to 300mV.
- The OTA is operated in closed feedback (voltage follower) rather than an open feedback loop (amplification application). That is why the V- is connected to the output similar to an OPAMP.
- This configuration of the OTA acts as a Source follower or Voltage follower circuit, where the output voltage follows the input voltage in both magnitude and phase as the gain stage is set to unity gain.

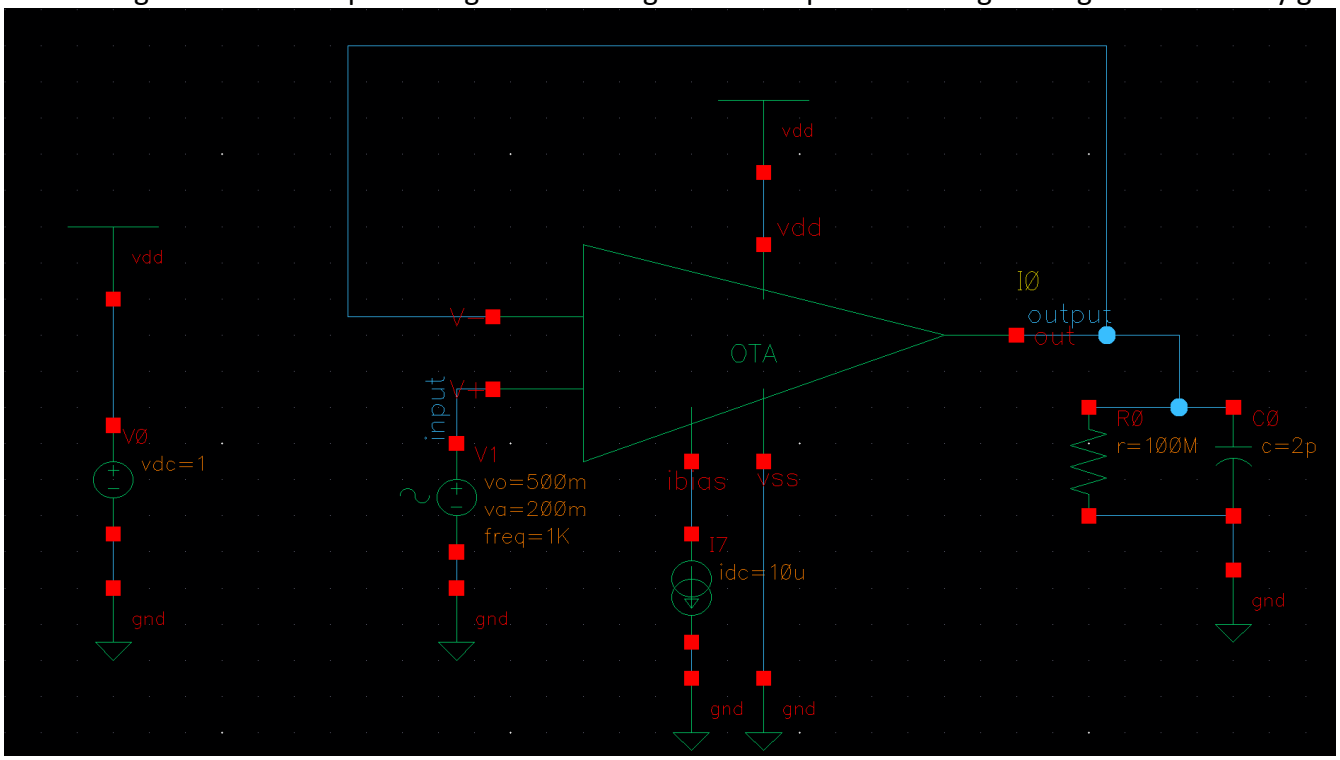

Figure 3: Test circuit for the OTA

LAYOUT AND AV EXTRACTED LAYOUT-

- During layout design, certain rules are followed for making connections between the MOSFETs. Some of the most important are that no two connections of different nets but of the same type can be overlapped. The metal connections need to be wide enough to prevent electromigration and a minimum distance maintained between two metal wires to avoid crosstalk. The minimum distance between various wires (lambda rules) must be satisfied with proper via sizes.
- The lengths of all the MOSFETs are set to 1.05um which is dependent on the manufacturing capabilities. Therefore it remains a fixed parameter and the designer can only vary the width.

- We notice that the 2 bigger PMOS (I_{bias} current mirror) and 4 smaller PMOS have their fingers set to 2. This is a configuration where a large MOSFET is split into 2 MOSFETs and connected in parallel with overlapping drains resulting in multi-fingered gate terminals (i.e., 2 gate terminals).
- Therefore, each MOS (having width W/2) connected in parallel will have an effective width of W, with the same current carrying capacity as a MOSFET with one finger.
- Therefore, the source capacitance remains the same as there are two source terminals (as seen in the layout) and the junction capacitance at the drain is halved (as there is effectively only one drain). The **resistance** seen at the gate (the gate terminal is made of polysilicon which has resistance) is reduced as they are split and connected in parallel.
- This improves the matching (common centroid matching) as the MOS can be arranged in rows to form squares, it reduces the parasitic capacitance and the overall area in the layout design.
- The size of the via is important as it defines how much current flows between two contacts. As seen in Figure 5 there is a voltage drop across the via as it has some resistance. If the resistance is too high, then enough current will not flow through resulting in a failure. This can be avoided by adding more via contacts which are connected in parallel thus reducing the effective resistance and allows more current to flow through compared to the prior option.
- Inherently the bulk in the layout is of p-type. This suits well for an NMOS but for a PMOS we need to incorporate N-Wells. The gap between the PMOS devices at the top is filled with a VDD_Nwell to prevent cross-talk between the two devices. Since two conductor lines (VDD) are close to each other, it leads to capacitive effects and degradation of the device's performance.
- During layout design it is important to keep the area as small as possible this can be achieved with other benefits by using multi-fingered MOSFETs.
- As discussed earlier the PMOS is multi-fingered. The finger(gate) is made of polysilicon which has resistance. If the MOSFET is not multi-fingered, then the resistance seen at the gate will be very large resulting in noise in analogue circuits. The junction capacitance is also reduced and allows them to be placed in rows for better matching. This is useful for making current mirrors. Due to oxide encroachment during production if 2 MOSFETs of different widths are connected in parallel to form a current mirror the exact ratio of current I_1/I_2 will not be as expected. This can be solved by using multiple fingers and then the 2 MOSFETs are matched.
- Fingering will help with matching and the common centroid layout method, where the centroid of the matched devices should coincide at least approximately. Ideally producing a square shape.
- The VDD and VSS bus is large to allow proper sourcing and sinking of the current drawn by the MOSFETs avoiding electromigration.
- As discussed earlier two metal wires of different wires cannot overlap, to avoid long metal wires another metal layer (RED) is used to bridge the gap with M1_M2 vias to make the connection.
- AV extraction shows the parasitic capacitances and resistances in the layout which we would otherwise not be able to notice directly.
- The parasitics seen include the series gate resistance, drain-to-source resistance, drain-to-source capacitance, gate-to-source capacitance, gate-to-drain capacitance and the capacitance and resistance offered by the metal strips.

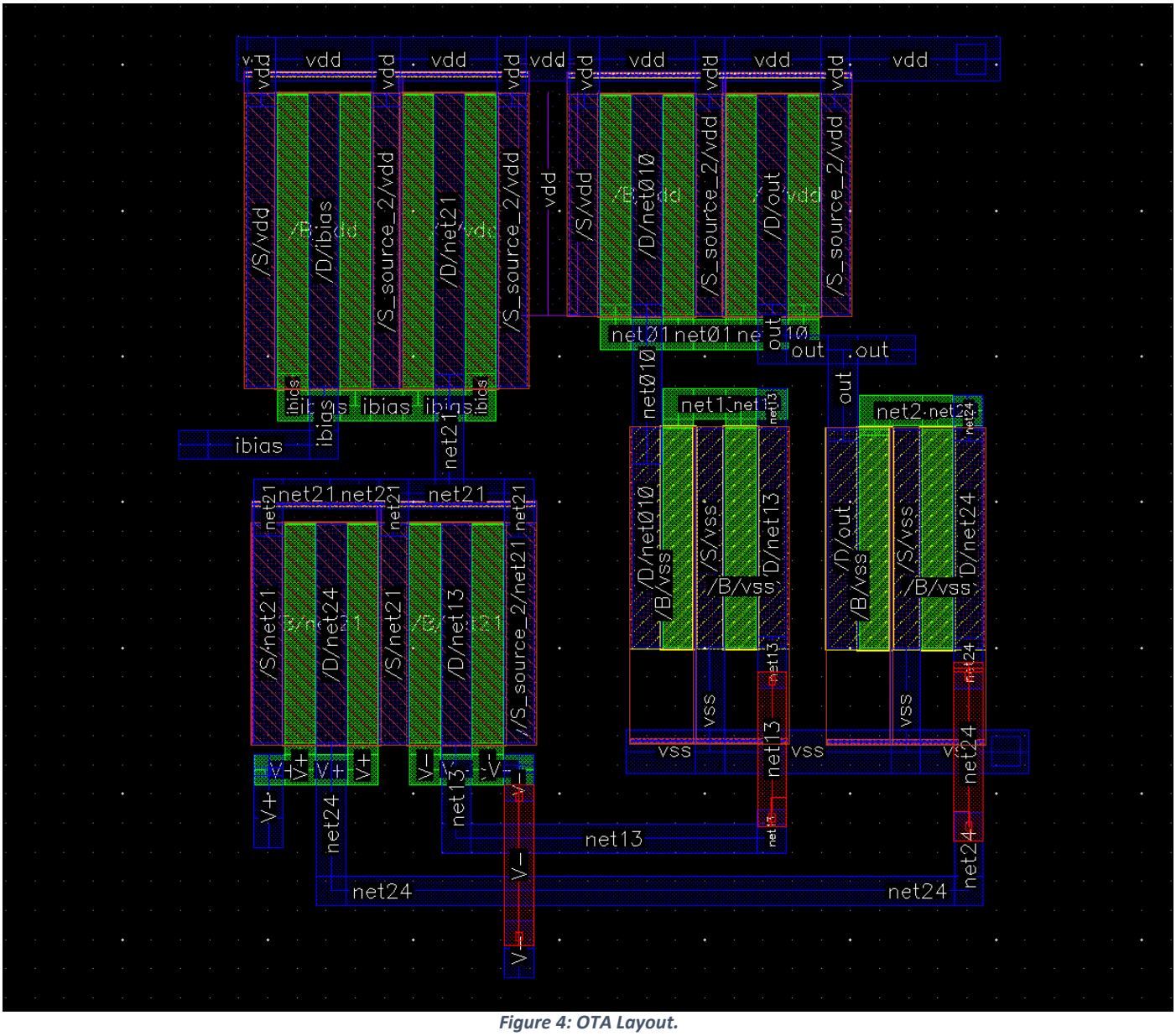

Figure 4: OTA Layout.

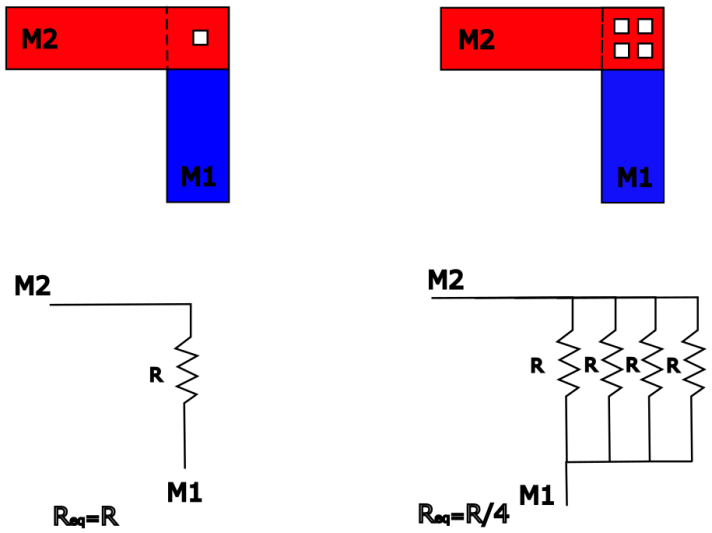

Figure 5: Layout vs schematic of the contact resistance of one via vs four vias.

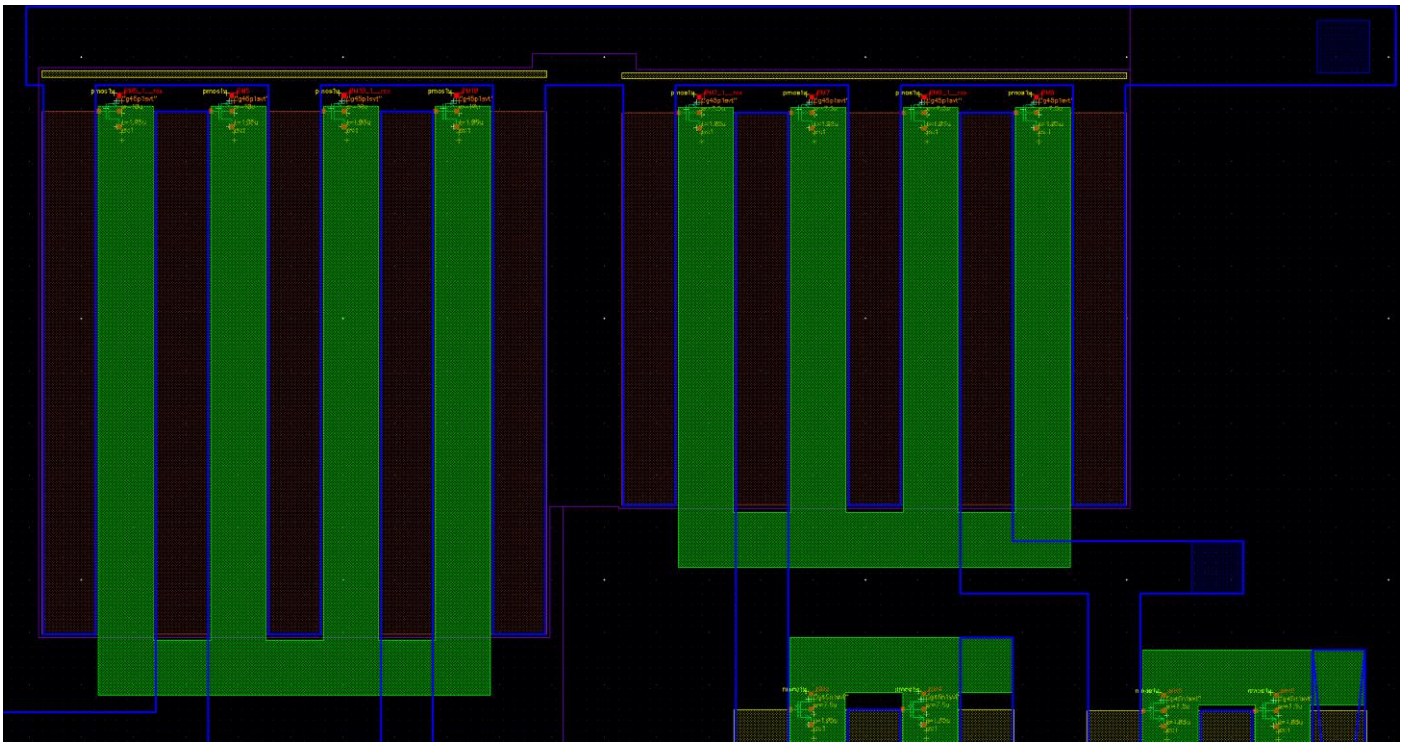

Figure 6: AV Extracted layout view of the top half.

SIMULATION OUTPUTS-

- The transient response of the OTA can be seen in Figures 7 and 8 done using ADE (Analogue Design Environment).
- The output (red) follows the input (green), therefore acting as a source follower.
- We can see that the output of the simulated circuit and the AV extracted output match. Thus, the layout works as we intended.
- The simulations are done only after the Design Rule Check (DRC) followed by LVS (Layout Versus Schematic) check for the layout and QRC to extract the parasitic capacitance and resistance to give the AV extracted layout.
- LVS compares the netlist generated from the layout to the original netlist and checks if they match.
- DRC verifies as to whether a specific design meets the constraints imposed by the process technology to be used for manufacturing.
- If the parasitics were more then the output would have deviated from the input resulting in a large voltage drop.

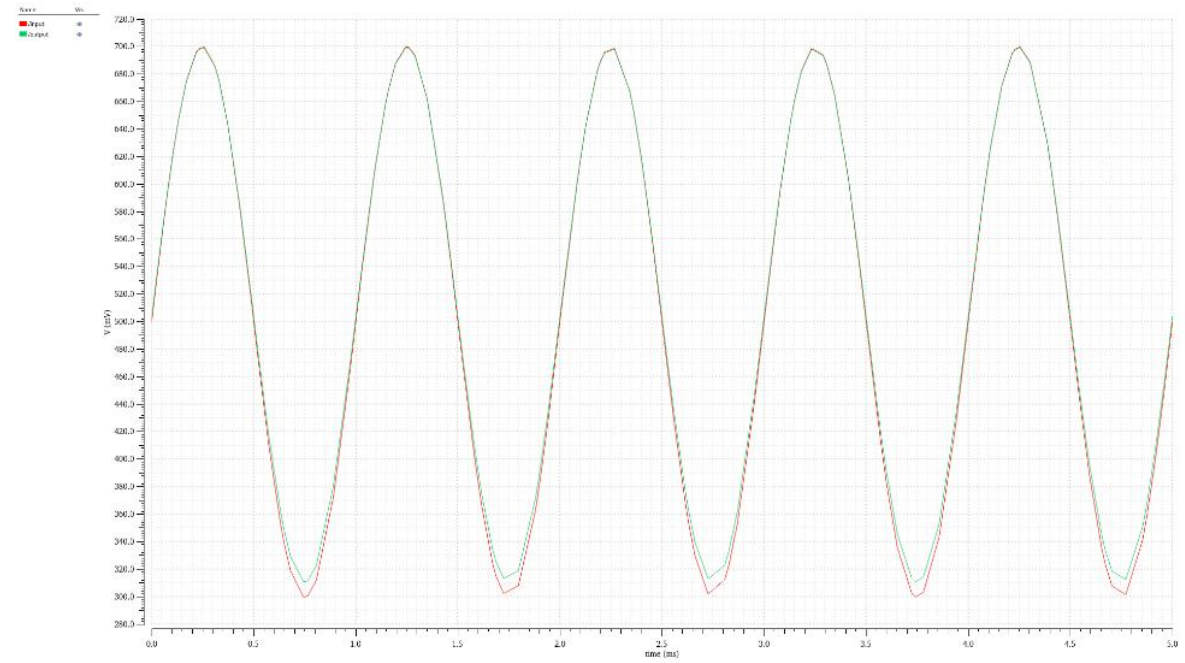

Figure 7: Output voltage following the input voltage from the test circuit.

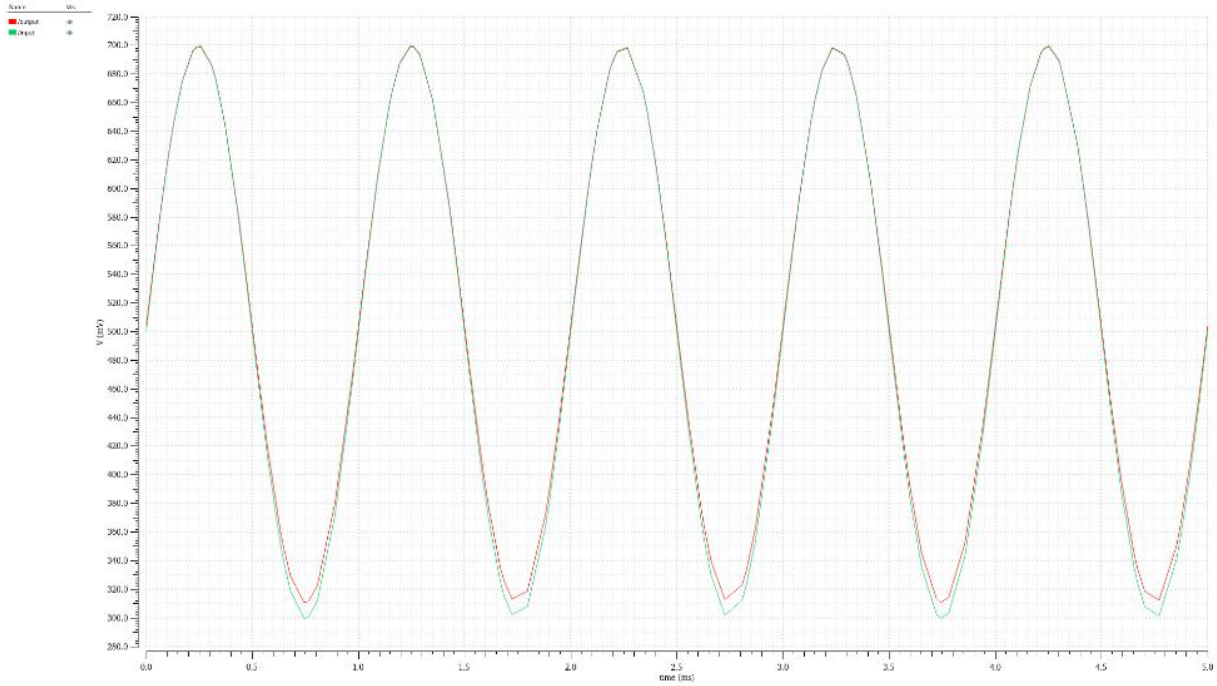

Figure 8: Output voltage following the input voltage from the AV extracted layout