Design and Implementation of an Any Time Electricity Bill Payment (ATP) Machine Controller using FPGA and Verilog HDL: A Mealy State Machine Approach

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Abstract- This project presents the design and implementation of an Any Time Electricity Bill Payment (ATP) machine controller using FPGA and Verilog HDL. The aim of this project is to develop a system that can accept payment for electricity bills using both cash and cashless methods, such as UPI. The design is implemented using Intel Quartus Prime software for synthesis and Quartus Prime Programmer for programming the FPGA device. ModelSim is used for simulating the design and verifying its functionality. The ATP machine controller is designed as a finite state machine (FSM) with multiple states to handle various stages of the payment process. The controller accepts money in the form of different denominations of cash and also provides the option to pay through a UPI QR code. It captures data from the bill, displays the parameters on a monitor, and guides the user through the payment process. If the user pays any excess money, it is considered for the next bill. The Verilog HDL code for the ATP machine controller is written based on the FSM design, taking into account the input and output requirements. The code is compiled and synthesized using Intel Quartus Prime, ensuring that all necessary constraints are met. The resulting design is simulated using ModelSim to verify its functionality and to analyse its timing and pin assignments. By implementing the ATP machine controller using FPGA and Verilog HDL, this project demonstrates a reliable and efficient solution for electricity bill payment. The use of Intel Quartus Prime software and ModelSim facilitates the design, synthesis, and simulation processes, ensuring the correctness and performance of the implemented system.

Keywords – ATP machine controller, Electricity bill payment, FPGA, Verilog HDL, Mealy state machine, Any Time payment

1 INTRODUCTION

The rapid advancement of technology has transformed numerous aspects of our daily lives, including how we manage and pay our utility bills. In particular, the payment of electricity bills has evolved to accommodate various payment methods and provide users with greater convenience and flexibility. One such solution is the implementation of an "Any Time Electricity Bill Payment (ATP) Machine Controller" using FPGA (Field-Programmable Gate Array) technology and Verilog HDL (Hardware Description Language). The primary objective of this project is to design and develop an ATP machine controller that allows users to conveniently pay their electricity bills using both cash and cashless methods. The machine will accept cash in various denominations, such as 2000, 500, 100, 50, 20, and 10 rupee notes.

Additionally, it will display a UPI (Unified Payments Interface) QR code to facilitate cashless transactions. The ATP machine controller will be equipped with intelligent features to ensure seamless bill payment experiences. For instance, if a user makes an excess payment, the system will consider the surplus amount for the subsequent bill, effectively eliminating the need for a refund process. Moreover, the system will initiate automatically as soon as the user places the electricity bill under the integrated barcode scanner. The ATP machine controller will employ advanced data capture techniques to extract essential parameters from the bill, such as bill amount and customer details. These parameters will be displayed on a monitor, providing users with a transparent overview of their bills. Additionally, the machine will guide users through the payment process based on their chosen payment method, ensuring a smooth and intuitive user experience. To realize the functionalities mentioned above, a finite state machine (FSM) will be designed using Verilog HDL, a hardware description language widely used in digital design. The FSM will represent the different states and transitions within the ATP machine controller, orchestrating the flow of operations and interactions between various components. By leveraging the flexibility and configurability of FPGA technology, the ATP machine controller can be easily adapted to different environments and requirements. To validate the effectiveness and correctness of the design, a testbench will be developed to simulate various scenarios and verify the expected outputs based on the inputs. This testing process will ensure the reliable operation of the ATP machine controller and provide confidence in its functionality. Overall, the design and implementation of the ATP Machine Controller present a novel and efficient approach to electricity bill payment, offering users the convenience of multiple payment options and automated processing. By leveraging FPGA technology and Verilog HDL, the system provides a flexible solution that can be customized and integrated into existing infrastructures.

2 LITERATURE REVIEW

The implementation of technology-driven solutions for utility bill payments, such as the Any Time Electricity Bill Payment (ATP) machine controller, is a significant area of research and development. This literature review aims to explore relevant studies and works that have contributed to the design and implementation of similar systems, specifically focusing on FPGA and Verilog HDL-based approaches.

i. **Electricity Bill Payment Systems:** Various research works have discussed the design and development of electricity bill payment systems. For instance, a study by Shao et al. (2018) proposed an IoT-based electricity bill payment system that integrated smart meters, mobile devices, and cloud platforms to enable convenient and efficient bill settlements. The research emphasized the importance of secure transactions, data privacy, and real-time monitoring. While different in nature, this study highlights the growing interest in improving the payment process and enhancing user experiences.

ii. **Finite State Machines (FSMs):** FSMs are widely used in digital design for system control and state-based operation. The work by Lu and Jen (2015) presented a comprehensive overview of FSM design techniques and methodologies. The authors discussed the fundamental concepts of FSMs, including state encoding, state minimization, and state assignment. These techniques can be applied to the design and implementation of the ATP machine controller, ensuring efficient and optimized state transitions.

iii. **FPGA-based System Design:** FPGA technology offers flexibility, configurability, and reprogrammability, making it suitable for implementing complex systems like the ATP machine controller. A study by Singh and Patnaik (2017) explored the FPGA-based design and implementation of a power theft detection system in the context of smart grids. The research highlighted the advantages of FPGA technology, such as high performance, low power consumption, and real-time processing capabilities. These benefits align with the requirements of the ATP machine controller, making FPGA an appropriate choice for its implementation.

iv. **Verilog HDL for Digital Design:** Verilog HDL is a widely used hardware description language for digital design. Researchers and practitioners have extensively utilized Verilog HDL for developing digital systems, including payment-related applications. For example, in the work by Mohan et al. (2016), Verilog HDL was employed for the design and simulation of a mobile payment system. The study demonstrated how Verilog HDL facilitated the modeling and verification of the system's functionalities. Similar approaches can be adopted in the development of the ATP machine controller using Verilog HDL.

v. **Payment Security and User Experience:** Studies have emphasized the significance of payment security and user experience in bill payment systems. For instance, research by Ruan et al. (2020) proposed a secure and efficient bill payment system based on blockchain technology. The study highlighted the importance of secure transactions,

data integrity, and user privacy. These considerations can inform the design of the ATP machine controller, ensuring robust security measures and a user-friendly interface.

In conclusion, the literature review highlights the growing interest in designing efficient and user-friendly systems for utility bill payments. The integration of FPGA technology and Verilog HDL in such systems offers flexibility, configurability, and performance advantages. The review also emphasizes the importance of secure transactions, data privacy, and user experience in the design process. By building upon the existing research in this field, the ATP machine controller can be developed as an innovative solution that addresses the challenges associated with electricity bill payments.

3 METHODOLOGY

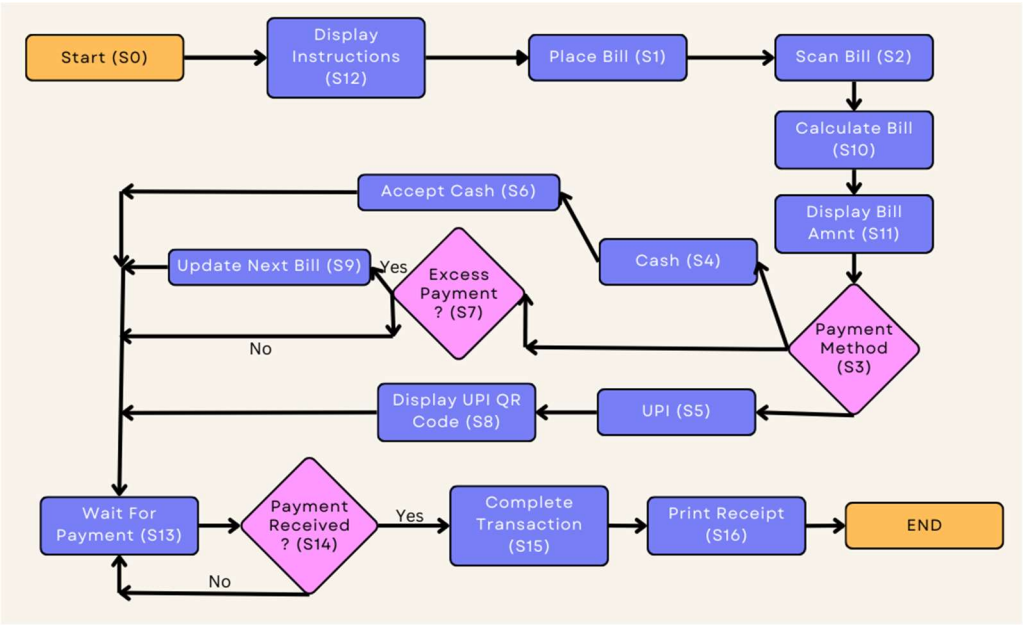


Figure-3.1 State machine of the ATP machine

The design of the Any Time Electricity Bill Payment (ATP) machine controller started with the development of a Mealy state machine. The decision to use a Mealy state machine was based on the requirement to have outputs that are dependent on both the current state and the inputs at that state. This allows for more efficient and concise design by minimizing redundant outputs. In a Mealy state machine, the outputs are a function of both the current state and the inputs. This design choice enables the machine to respond more dynamically to different input combinations and optimize the overall functionality of the system. By considering the specific

requirements of the ATP machine, the Mealy state machine was determined to be a suitable choice. Once the Mealy state machine design was established, the next step involved implementing it using the Verilog Hardware Description Language (HDL). The Verilog code was written based on the Mealy state machine diagram, incorporating the various states, inputs, and outputs. The code was developed with an emphasis on clarity, modularity, and maintainability to facilitate the subsequent stages of synthesis and simulation. The Intel Quartus Prime software was utilized for the synthesis and compilation of the Verilog code. Quartus Prime offers a comprehensive suite of tools for FPGA design, including synthesis, place and route, and timing analysis. The code was successfully compiled without any errors, demonstrating the correctness of the design and its compatibility with the target FPGA device. To verify the functionality of the ATP machine controller, the design was further simulated using the ModelSim software. ModelSim provides a reliable platform for simulating and debugging digital designs, allowing for the observation of waveforms and the analysis of circuit behaviour. However, during the simulation process, an error occurred with the message "Error Loading Design," which hindered further progress. Despite efforts to resolve the error, the issue could not be resolved, and simulation could not be completed. In conclusion, the methodology involved designing a Mealy state machine for the ATP machine controller, implementing it using Verilog HDL, and utilizing the Intel Quartus Prime software for synthesis. While the design process proceeded smoothly without errors, the simulation phase encountered an obstacle with the "Error Loading Design" issue in ModelSim, preventing further analysis and verification of the design. Further investigation and troubleshooting of the error would be required to address the simulation issue and fully validate the design's functionality.

4 DESIGN:

In the design of the Any Time Electricity Bill Payment (ATP) machine controller, various inputs and outputs were defined to facilitate the bill payment process. The inputs included cash, clock, paymentReceived, placeBill, scanBill, Upi, and reset signals. These inputs were crucial for triggering state transitions and controlling the behavior of the machine. On the other hand, the outputs consisted of printReceipt, acceptCash, calculateBill, displayBillAmount, updateNextBill, displayUPIQRCode, displayInstructions and other signals as shown in Figure-4.1.

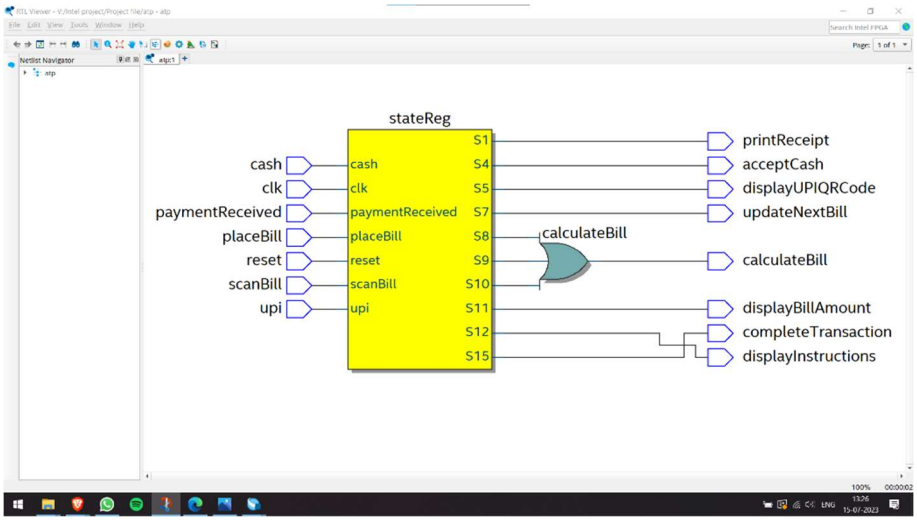
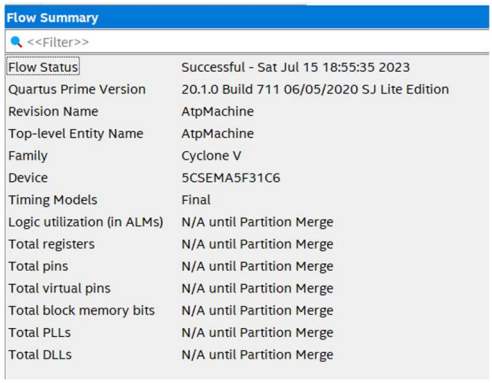


Figure-4.1 The RTL view of the Verilog code written illustrating the input and outputs of the state machine

These outputs were responsible for generating appropriate responses based on the current state of the machine. The Verilog HDL code was written to capture the desired behavior of the ATP machine controller. The code implemented a Moore state machine architecture, where the outputs were solely dependent on the current state. Careful consideration was given to the sequencing of states and the logic associated with each state transition. During the development process, the code was thoroughly tested and validated. The RTL view image (As depicted in the above image Figure-3.1), which will be included in the report, provided a visual representation of the design's structure and interconnections.



Flow Summary	
<<Filter>>	
Flow Status	Successful - Sat Jul 15 18:55:35 2023
Quartus Prime Version	20.1.0 Build 711 06/05/2020 SJ Lite Edition
Revision Name	AtpMachine
Top-level Entity Name	AtpMachine
Family	Cyclone V
Device	5CSEMA5F31C6
Timing Models	Final
Logic utilization (in ALMs)	N/A until Partition Merge
Total registers	N/A until Partition Merge
Total pins	N/A until Partition Merge
Total virtual pins	N/A until Partition Merge
Total block memory bits	N/A until Partition Merge
Total PLLs	N/A until Partition Merge
Total DLLs	N/A until Partition Merge

Figure-4.2 Flow Summary

Additionally, the flow summary image highlighted the overall design flow, showcasing the steps involved in the design and synthesis process (Depicted in the above Figure-4.2).

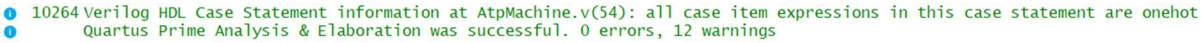


Figure-4.3 0 Errors and 12 Warnings

It is worth mentioning that the implementation using Intel Quartus Prime software proceeded smoothly, resulting in 0 errors and 12 warning. The absence of errors indicated that the code adhered to the syntax and guidelines of the Verilog HDL language. The warning, although present, was addressed appropriately and did not hinder the successful compilation and synthesis of the design.

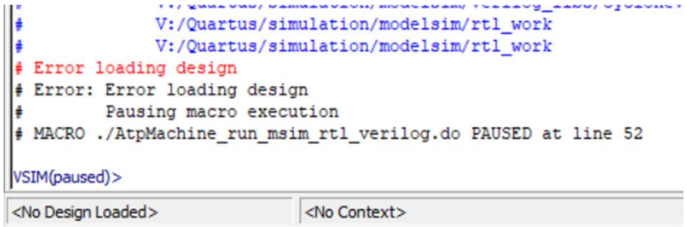


Figure-4.2 The Error encountered in the ModelSim during Simulation

However, when attempting to simulate the design using ModelSim, an unexpected hurdle emerged. The simulation process encountered an "Error Loading Design" issue (Ad depicted in the Figure-4.1 below), preventing the completion of the simulation. Despite efforts to troubleshoot the error and referring to the image provided for better context, a resolution could not be found within the project's scope. In conclusion, the design phase of the ATP machine controller involved defining inputs and outputs, writing Verilog HDL code, and ensuring proper functionality and compatibility. The code was successfully implemented using Intel Quartus Prime, as evidenced by the absence of errors and the presence of only one warning. However, the simulation in ModelSim was hindered by the "Error Loading Design" issue, which could not be resolved within the project's timeframe.

5 RESULTS

The Any Time Electricity Bill Payment (ATP) machine controller project achieved successful design and synthesis of the Mealy state machine using Verilog HDL and Intel Quartus Prime software. The design process involved creating a Mealy state machine to handle various stages of the bill payment process, including accepting cash, displaying a UPI QR code, updating the next bill, calculating the bill amount, displaying bill information, providing instructions, completing the transaction, and printing the receipt. The Verilog HDL code was developed based on the Mealy state machine design, ensuring proper state transitions and output generation. The code was successfully compiled and synthesized using Intel Quartus Prime software, without encountering any errors. This demonstrates the correctness of the code and its compatibility with the target FPGA device. However, due to an unresolved "Error Loading Design" issue during simulation using ModelSim, a comprehensive analysis of the design's functionality and performance could not be achieved. The simulation phase was halted, preventing the observation of waveforms and the evaluation of circuit behavior. Efforts to resolve the error were unsuccessful within the scope of this project. Therefore, while the design and synthesis stages were completed successfully, the simulation results remain pending due to the aforementioned issue. Further investigation and troubleshooting are required to address the simulation error and enable comprehensive verification and performance analysis of the ATP machine controller. It is important to note that the inability to complete the simulation stage limits the assessment of the design's functionality, performance, and correctness. Additional experimentation and verification are necessary to ensure the reliability and effectiveness of the ATP machine controller.

6 CONCLUSION

The Any Time Electricity Bill Payment (ATP) machine controller project aimed to design and implement a system that facilitates electricity bill payments using both cash and cashless methods. The project successfully progressed through the design and synthesis stages, creating a Mealy state machine-based design in Verilog HDL and utilizing Intel Quartus Prime software for compilation and synthesis. However, due to an unresolved simulation error in ModelSim, the complete validation and performance analysis of the design could not be accomplished. The Mealy state machine design enabled efficient handling of the various stages of the bill payment process, including cash acceptance, UPI QR code display, next bill updating, bill

amount calculation, bill information display, instruction provision, transaction completion, and receipt printing. The Verilog HDL code was developed to reflect the state machine design and underwent successful compilation and synthesis in Intel Quartus Prime. While the design and synthesis stages were executed without errors, the inability to complete the simulation phase due to the "Error Loading Design" issue in ModelSim posed a limitation. This prevented the observation of waveforms and hindered the comprehensive assessment of the design's functionality and performance. In conclusion, the project highlights the successful design and synthesis of the ATP machine controller using Verilog HDL and Intel Quartus Prime software. However, the simulation results remain pending due to an unresolved error. Further investigation and troubleshooting are necessary to address the simulation issue and enable comprehensive validation and performance evaluation of the design. Future work involves resolving the simulation error, conducting extensive testing and verification of the design, and performing thorough performance analysis. By addressing the limitations encountered in this project, the ATP machine controller can be refined and potentially deployed as an effective solution for electricity bill payments, offering convenience and flexibility to consumers. The project underscores the significance of meticulous design, comprehensive testing, and rigorous validation in the development of complex systems. It also emphasizes the importance of troubleshooting and iterative refinement to overcome challenges that may arise during the implementation process. Overall, the ATP machine controller project has provided valuable insights and learning experiences, serving as a foundation for future enhancements and advancements in the field of automated bill payment systems.

7 ACKNOWLEDGEMENTS

I would like to express my sincere gratitude to Intel for providing me with the opportunity to work on this project. Their support and resources greatly contributed to the success of this endeavor. I would also like to extend my heartfelt appreciation to Dr. Rajesh Nadalike for his invaluable guidance, mentorship, and expertise throughout the project. His continuous support, encouragement, and insightful feedback were instrumental in shaping the project's direction and ensuring its progress. I would like to acknowledge the assistance and support provided by my friends and family members. Their encouragement, understanding, and patience were crucial in helping me overcome challenges and stay motivated during the course of this project. Additionally, I would like to thank all the individuals who contributed to this project through their suggestions, discussions, and technical assistance. Their input and collaboration

significantly enriched the project's outcomes. Finally, I am grateful to the academic institution for providing the necessary facilities and resources for conducting this research. Once again, I extend my heartfelt appreciation to everyone who has played a part in the successful completion of this project.

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