

#### STP08CP05

#### Low voltage, low current power 8-bit shift register

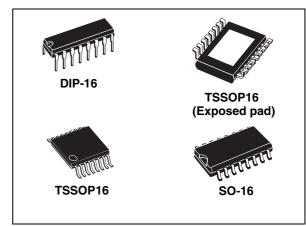
#### **Features**

- Low voltage power supply down to 3 V
- 8 constant current output channels
- Adjustable output current through external resistor
- Serial data IN/parallel data OUT
- 3.3 V micro driver-able
- Output current: 5-100 mA
- 30 MHz clock frequency
- Available in high thermal efficiency TSSOP exposed pad
- ESD protection 2.5 kV HBM, 200 V MM



The STP08CP05 is a monolithic, low voltage, low current, power 8-bit shift register designed for LED panel displays. The STP08CP05 contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. In the output stage, eight regulated current sources were designed to provide 5-100 mA constant current to drive the LEDs, the output current setup time is 11 ns (typ), thus improving the system performance.

The STP08CP05 is backward compatible in functionality and footprint with STP8C/L596. Through an external resistor, users can adjust the STP08CP05 output current, controlling in this way the light intensity of LEDs, in addition, user can



adjust LED's brightness intensity from 0% to 100% via  $\overline{OE}$  pin.

The STP08CP05 guarantees a 20 V output driving capability, allowing users to connect more LEDs in series. The high clock frequency, 30 MHz, also satisfies the system requirement of high volume data transmission. The 3.3 V of voltage supply is useful for applications that interface with any micro from 3.3 V. Compared with a standard TSSOP package, the TSSOP exposed pad increases heat dissipation capability by a 2.5 factor.

Table 1. Device summary

Order codes	Package	Packaging
STP08CP05B1R	DIP-16	25 parts per tube
STP08CP05MTR	SO-16 (Tape and reel)	2500 parts per reel
STP08CP05TTR	TSSOP16 (Tape and reel)	2500 parts per reel
STP08CP05XTTR	TSSOP16 exposed-pad (Tape and reel)	2500 parts per reel

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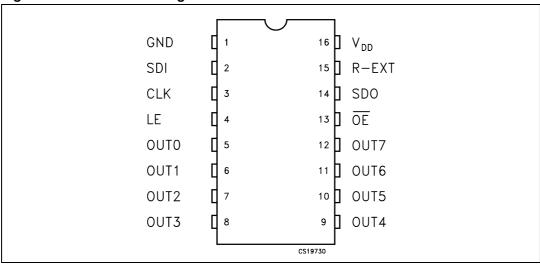
## 1 Summary description

Table 2. Typical current accuracy

Output voltage	Current a	Output current	
Output voitage	Between bits	Between ICs	Output current
≥ 1.3 V	± 1.5%	± 3%	20 to 100 mA

### 1.1 Pin connection and description

Figure 1. Connections diagram



Note:

The exposed pad should be electrically connected to a metal land electrically isolated or connected to ground.

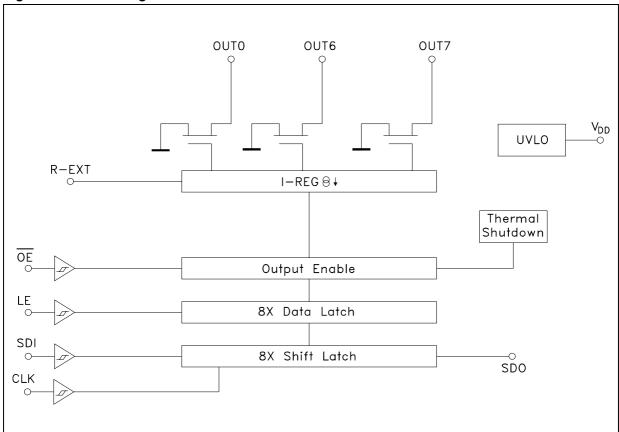
Table 3. Pin description

Pin N°	Symbol	Name and function			
1	GND	Ground terminal			
2	SDI	Serial data input terminal			
3	CLK	Clock input terminal			
4	LE	Latch input terminal			
5-12	OUT 0-7	Output terminal			
13	ŌĒ	Output enable input terminal (active low)			
14	SDO	Serial data out terminal			
15	R-EXT	Constant current programming			
16	$V_{\mathrm{DD}}$	5 V supply voltage terminal			

Block diagram STP08CP05

## 2 Block diagram

Figure 2. Block diagram



STP08CP05 Maximum rating

### 3 Maximum rating

Stressing the device above the rating listed in the "absolute maximum ratings" table may cause permanent damage to the device. these are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### 3.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply voltage I <sub>GND</sub>	0 to 7	V
V <sub>O</sub>	Output voltage	-0.5 to 20	V
I <sub>O</sub>	Output current	100	mA
I <sub>GND</sub>	GND terminal current	800	mA
f <sub>CLK</sub>	Clock frequency	50	MHz
T <sub>OPR</sub>	Operating temperature range	-40 to +125	°C
T <sub>STG</sub>	Storage temperature range	-55 to +150	°C

#### 3.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	DIP-16	SO-16	TSSOP-16	TSSOP-16 <sup>(1)</sup> (exposed pad)	Unit
R <sub>thJA</sub>	Thermal resistance junction-ambient	90	125	140	37.5	°C/W

<sup>1.</sup> The exposed-pad should be soldered to the PBC to realize the thermal benefits

Maximum rating STP08CP05

## 3.3 Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
V <sub>DD</sub>	Supply voltage		3.0		5.5	V
V <sub>O</sub>	Output voltage				20	V
Io	Output current	OUTn	5		100	mA
Іон	Output current	SERIAL-OUT			+1	mA
l <sub>OL</sub>	Output current	SERIAL-OUT			-1	mA
V <sub>IH</sub>	Input voltage		0.7 V <sub>DD</sub>		V <sub>DD</sub> +0.3	V
V <sub>IL</sub>	Input voltage		-0.3		0.3 V <sub>DD</sub>	V
t <sub>wLAT</sub>	LE pulse width		20			ns
t <sub>wCLK</sub>	CLK pulse width		20			ns
t <sub>wEN</sub>	OE pulse width	V <sub>DD</sub> = 3.0 to 5.0 V	200			ns
t <sub>SETUP(D)</sub>	Setup time for DATA	VDD = 3.0 to 3.0 V	7			ns
t <sub>HOLD(D)</sub>	Hold time for DATA		4			ns
t <sub>SETUP(L)</sub>	Setup time for LATCH		15			ns
f <sub>CLK</sub>	Clock frequency	Cascade operation (1)			30	MHz

<sup>1.</sup> In order to achieve high cascade data transfer, please consider  $t_{\text{r}}/t_{\text{f}}$  timings carefully.

## 4 Electrical characteristics

 $V_{DD}\!=3.3$  V to 5 V, T = 25 °C, unless otherwise specified.

Table 7. Electrical characteristics

Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
V <sub>IH</sub>	Input voltage high level		0.7 V <sub>DD</sub>		$V_{DD}$	V
V <sub>IL</sub>	Input voltage low level		GND		0.3V <sub>DD</sub>	V
I <sub>OH</sub>	Output leakage current	V <sub>OH</sub> = 20 V		0.5	10	μΑ
V <sub>OL</sub>	Output voltage (Serial-OUT)	I <sub>OL</sub> = 1 mA		0.03	0.4	V
V <sub>OH</sub>	Output voltage (Serial-OUT)	I <sub>OH</sub> = -1 mA	V <sub>OH</sub> - V <sub>DD</sub> =- 0.4 V			V
I <sub>OL1</sub>		$V_{O} = 0.3 \text{ V}, R_{ext} = 3.9 \text{ k}\Omega$	4.25	5	5.75	
I <sub>OL2</sub>	Output current	$V_{O} = 0.3 \text{ V, R}_{ext} = 970 \Omega$	19.4	20	20.6	mA
I <sub>OL3</sub>		$V_{O} = 1.3 \text{ V, R}_{ext} = 190 \Omega$	97	100	103	
Δl <sub>OL1</sub>	Output current error	$V_O = 0.3 \text{ VR}_{EXT} = 3.9 \text{ k}\Omega$		± 5	± 8	
Δl <sub>OL2</sub>	between bit	$V_{O} = 0.3 \text{ VR}_{EXT} = 970 \Omega$		± 1.5	± 2.75	%
Δl <sub>OL3</sub>	(All Output ON)	$V_O = 1.3 \text{ VR}_{EXT} = 190 \Omega$		± 1.2	± 2.5	
R <sub>SIN(up)</sub>	Pull-up resistor		150	300	600	ΚΩ
R <sub>SIN(down)</sub>	Pull-down resistor		100	200	400	KΩ
I <sub>DD(OFF1)</sub>	Supply ourrent (OEE)	R <sub>EXT</sub> = 980 OUT 0 to 7 = OFF		4	5	
I <sub>DD(OFF2)</sub>	Supply current (OFF)	R <sub>EXT</sub> = 250 OUT 0 to 7 = OFF		11.2	13.5	mA
I <sub>DD(ON1)</sub>	Supply current (ON)	R <sub>EXT</sub> = 980 OUT 0 to 7 = ON		4.5	5	IIIA
I <sub>DD(ON2)</sub>	Supply current (ON)	R <sub>EXT</sub> = 250 OUT 0 to 7 = ON		11.7	13.5	
Thermal	Thermal protection (1)			170		°C

Guaranteed by design (not tested)
The thermal protection switches OFF only the outputs

# 5 Switching characteristics

 $V_{DD}$  = 5 V, T = 25 °C, unless otherwise specified.

Table 8. Switching characteristics

Symbol	Parameter	Test conditions			Min	Тур	Max	Unit
	Propagation delay time,			$V_{DD} = 3.3 \text{ V}$		35	50	
t <sub>PLH1</sub>	CLK-OUTn, LE = H, OE = L			$V_{DD} = 5 V$		18	28	ns
	Propagation delay time,			V <sub>DD</sub> = 3.3 V		48	74	
t <sub>PLH2</sub>	DE = L			V <sub>DD</sub> = 5 V		30	50	ns
_	Propagation delay time,			V <sub>DD</sub> = 3.3 V		55	82	
t <sub>PLH3</sub>	OE -OUTn, LE = H			V <sub>DD</sub> = 5 V		37	58	ns
	Propagation delay time,			V <sub>DD</sub> = 3.3 V		21	28	ns
t <sub>PLH</sub>	CLK-SDO			$V_{DD} = 5 V$		17	22	115
	Propagation delay time,	$V_{DD} = 3.3 \text{ V}$ $V_{IH} = V_{DD}$ $V_{IL} = \text{GND}$ $C_L = 10 \text{ pF}$		$V_{DD} = 3.3 \text{ V}$		11	17	
t <sub>PHL1</sub>	CLK-OUTn, LE = H, OE = L			$V_{DD} = 5 V$		7	11	ns
	Propagation delay time,	$I_0 = 20 \text{ mA}$	_	V <sub>DD</sub> = 3.3 V		24	40	
t <sub>PHL2</sub>	DE = L	$R_{\text{EXT}} = 1 \text{ K}\Omega$	$R_{EXT} = 1 \text{ K}\Omega$ $R_L = 60 \Omega$	V <sub>DD</sub> = 5 V		21	31	ns
	Propagation delay time,			V <sub>DD</sub> = 3.3 V		20	35	
t <sub>PHL3</sub>	OE -OUTn, LE = H			V <sub>DD</sub> = 5 V		18	28	ns
t	Propagation delay time,			V <sub>DD</sub> = 3.3 V		24	32	ns
t <sub>PHL</sub>	CLK-SDO			$V_{DD} = 5 V$		19	25	115
	Output rise time			$V_{DD} = 3.3 \text{ V}$		26	40	
t <sub>ON</sub>	10~90% of voltage waveform			$V_{DD} = 5 V$		11	17	ns
	Output fall time			$V_{DD} = 3.3 \text{ V}$		5	10	
t <sub>OFF</sub>	90~10% of voltage waveform			V <sub>DD</sub> = 5 V		4	8	ns
t <sub>r</sub>	CLK rise time (1)						5000	ns
t <sub>f</sub>	CLK fall time (1)	]					5000	ns

<sup>1.</sup> In order to achieve high cascade data transfer, please consider tr/tf timings carefully.

# 6 Equivalent circuit and outputs

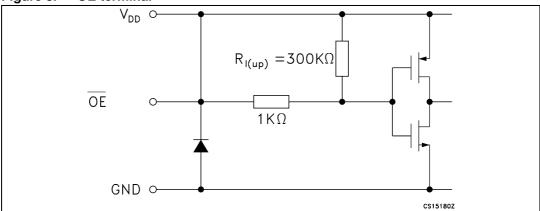


Figure 4. LE terminal

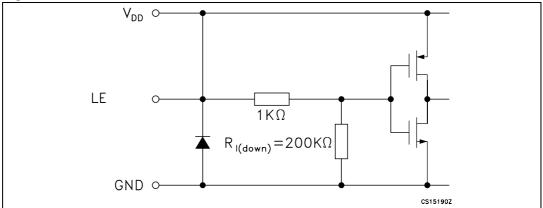


Figure 5. CLK, SDI terminal

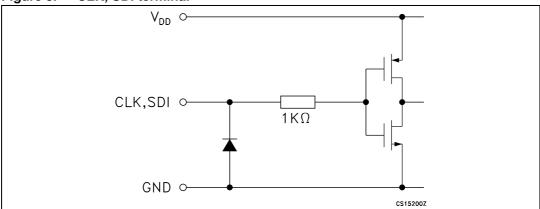
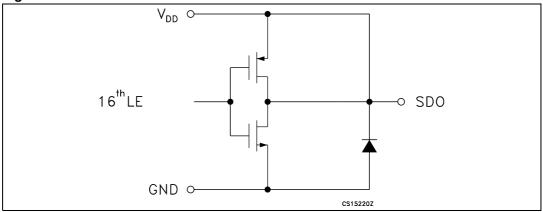


Figure 6. SDO terminal



# 7 Truth table and timing diagram

#### 7.1 Truth table

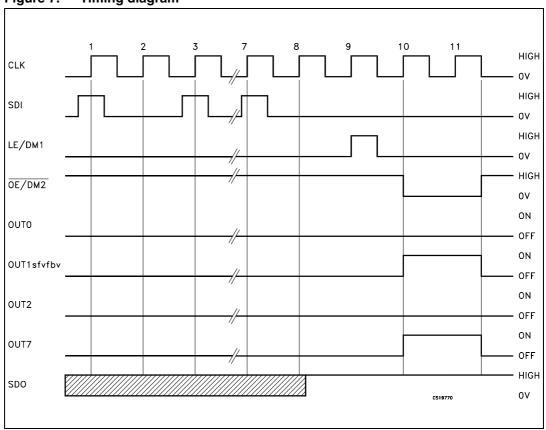
Table 9. Truth table

Clock	LE	ŌĒ	SDI	OUT0 OUT0 OUT7	SDO
<b>_</b>	Н	L	Dn	Dn Dn -5 Dn -7	Dn -7
<b>_</b>	L	L	Dn + 1	No change	Dn -7
	Н	L	Dn + 2	Dn +2 Dn -3 Dn -5	Dn -5
<b>T</b>	Х	L	Dn + 3	Dn +2 Dn -3 Dn -5	Dn -5
<b>—</b>	Х	Н	Dn + 3	OFF	Dn -5

Note: OUT0 to OUT7 = ON when Dn = H; OUT0 to OUT7 = OFF when Dn = L.

## 7.2 Timing diagram

Figure 7. Timing diagram



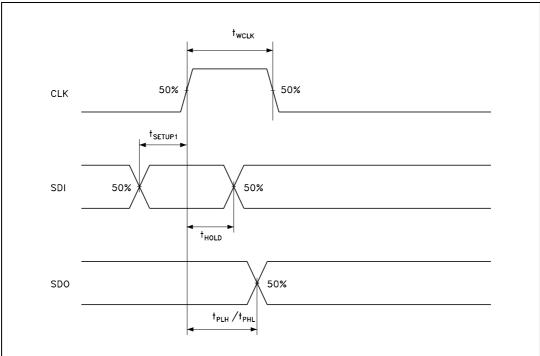
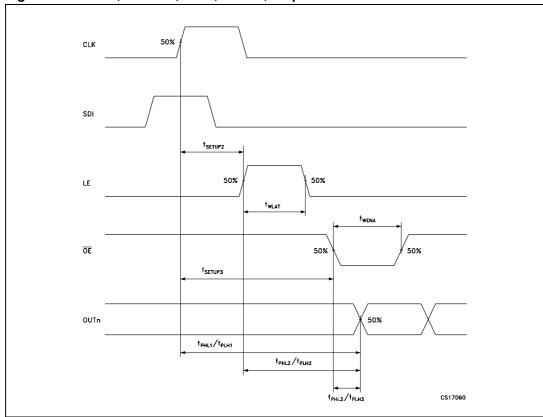


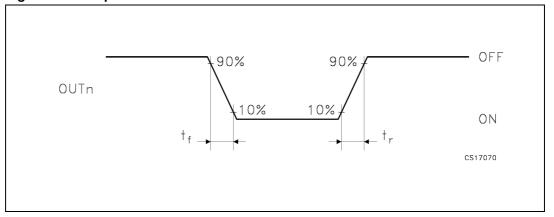
Figure 8. Clock, serial-in, serial-out





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Figure 10. Outputs



## 8 Typical characteristics

Figure 11. Output current- $R_{\text{EXT}}$  resistor

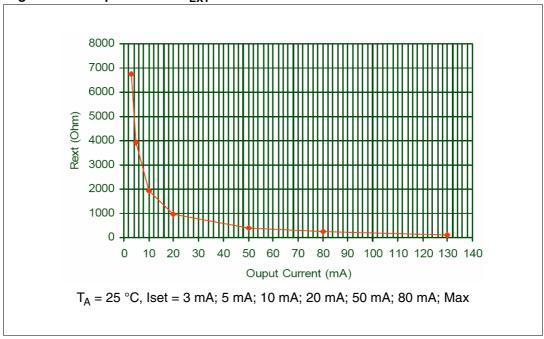


Table 10. Output current-R<sub>EXT</sub> resistor

Output current (mA)	3	5	10	20	50	80	130
Rext (Ω)	6740	3930	1913	963	386	241	124

Note:

Maximum output current capabilities setting was 130 mA applying an Rext = 124  $\Omega$ 

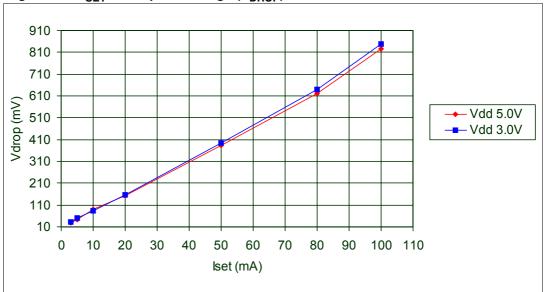


Figure 12.  $I_{SET}$  vs drop out voltage ( $V_{DROP}$ )

Table 11. I<sub>SET</sub> vs drop out voltage (V<sub>DROP</sub>)

Vdd (V)	I set (mA)	Rext (Ω)	Vdrop min (mV)	Vdrop max (mV)	Vdrop AVG (mV)
3	3	6470	30.6	31.2	30.93
	5	3930	46.5	52.9	48.63
	10	1910	80.9	100	82.26
	20	963	150	161	157
	50	386	392	396	394.3
	80	241	636	646	640.3
	100	192	846	850	848
5	3	6470	25.6	29	26.96
	5	3930	40.8	41.7	41.16
	10	1910	80.1	105	89.2
	20	963	153	154	154
	50	386	379	386	382
	80	241	618	626	621
	100	192	825	830	827

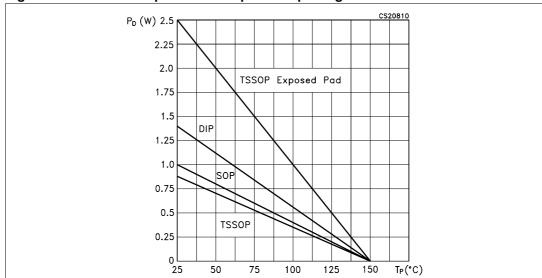


Figure 13. Power dissipation vs temperature package

Note: The exposed-pad should be soldered to the PBC to realize the thermal benefits.

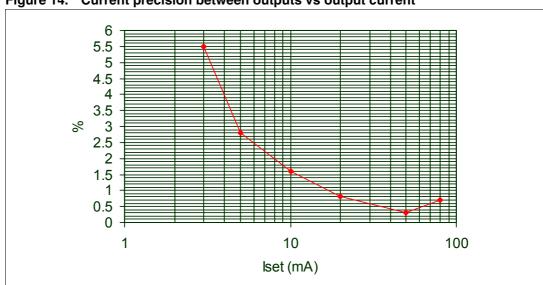


Figure 14. Current precision between outputs vs output current

Test circuit STP08CP05

## 9 Test circuit

Figure 15. DC characteristics

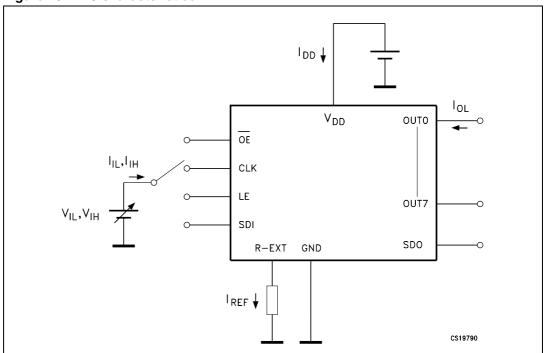
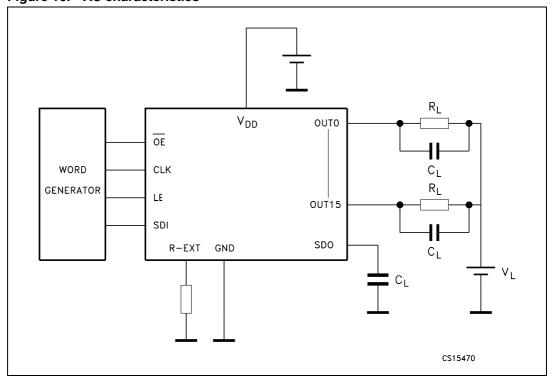


Figure 16. AC characteristics



STP08CP05 Test circuit

V<sub>0</sub> = 0.3 to 1.5V V<sub>DD</sub> = 3.3 to 5V V<sub>DD</sub> = 3.3 to 5V V<sub>DD</sub> = 0 to 100KHz

Figure 17. Typical application schematic

## 10 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

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Figure 18. DIP-16 mechanical data

### Plastic DIP-16 (0.25) MECHANICAL DATA

DIM	mm.			inch		
DIM.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
В	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
е		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

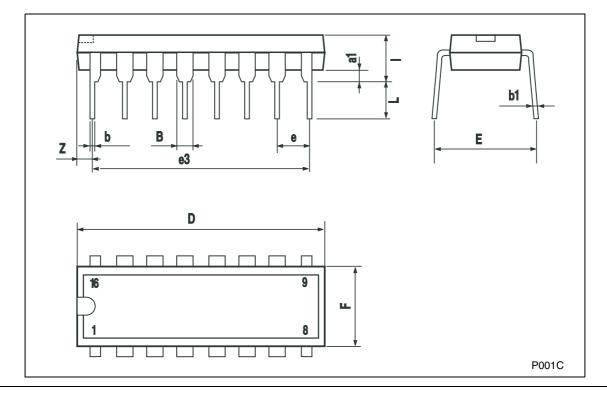


Figure 19. TSSOP16 mechanical data

#### **TSSOP16 MECHANICAL DATA**

DIM.	mm.			inch		
DIW.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
А			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
С	0.09		0.20	0.004		0.0079
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
е		0.65 BSC			0.0256 BSC	
К	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030

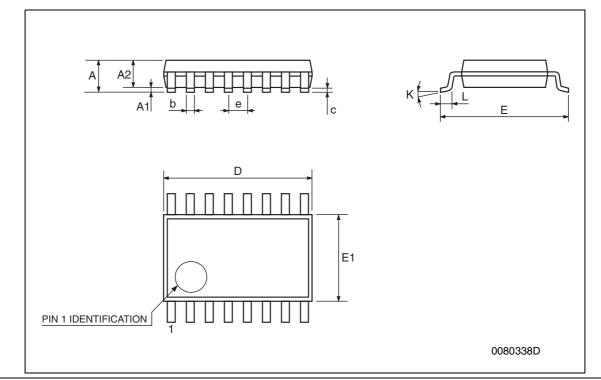


Figure 20. TSSOP16 exposed pad mechanical data

#### **TSSOP16 EXPOSED PAD MECHANICAL DATA**

DIM		mm.			inch		
DIM.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.	
А			1.2			0.047	
A1			0.15		0.004	0.006	
A2	0.8	1	1.05	0.031	0.039	0.041	
b	0.19		0.30	0.007		0.012	
С	0.09		0.20	0.004		0.0089	
D	4.9	5	5.1	0.193	0.197	0.201	
D1	2.7	3.0	3.3				
Е	6.2	6.4	6.6	0.244	0.252	0.260	
E1	4.3	4.4	4.5	0.169	0.173	0.177	
E2	2.7	3.0	3.3				
е		0.65			0.0256		
K	0°		8°	0°		8°	
L	0.45	0.60	0.75	0.018	0.024	0.030	

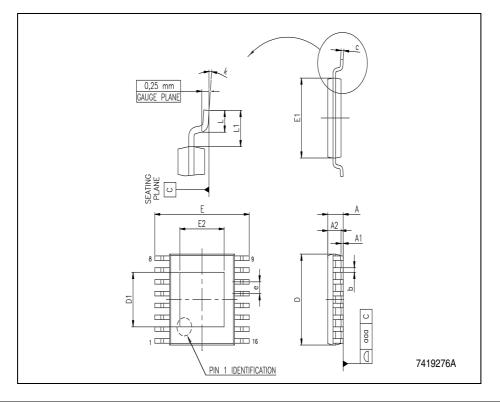


Figure 21. TSSOP16 tape and reel

### Tape & Reel TSSOP16 MECHANICAL DATA

DIM.	mm.			inch		
DIN.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
А			330			12.992
С	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
Т			22.4			0.882
Ao	6.7		6.9	0.264		0.272
Во	5.3		5.5	0.209		0.217
Ко	1.6		1.8	0.063		0.071
Po	3.9		4.1	0.153		0.161
Р	7.9		8.1	0.311		0.319

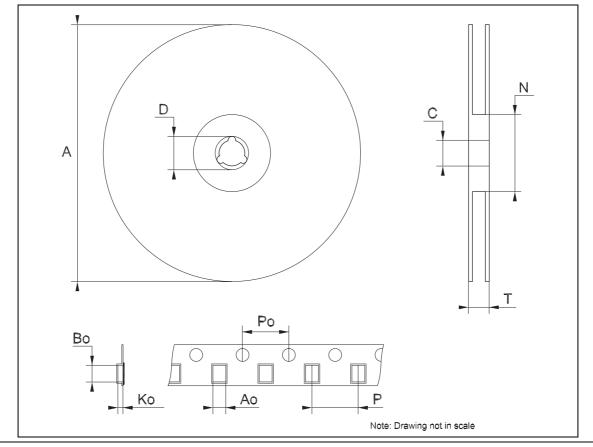


Figure 22. SO-16 mechanical data

#### **SO-16 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
Α			1.75			0.068
a1	0.1		0.25	0.004		0.010
a2			1.64			0.063
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
С		0.5			0.019	
c1		45° (typ.)				
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
е		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
М			0.62			0.024
S		•	8° (r	nax.)	•	

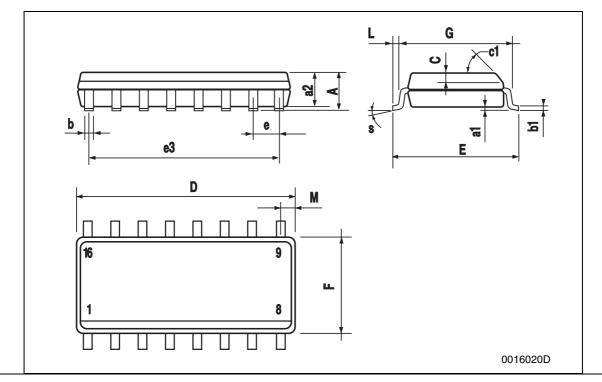
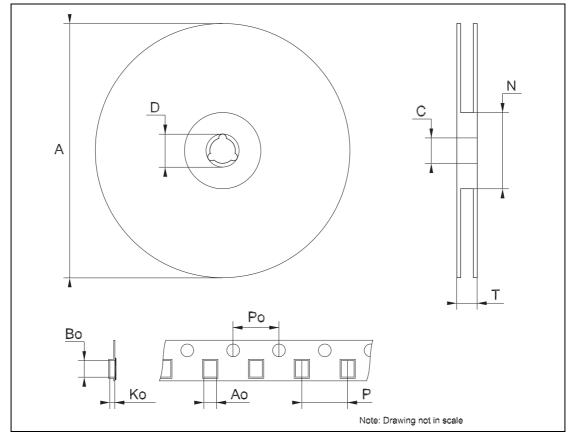


Figure 23. SO-16 tape and reel

### Tape & Reel SO-16 MECHANICAL DATA

DIM.	mm.			inch		
DIIVI.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
А			330			12.992
С	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
Т			22.4			0.882
Ao	6.45		6.65	0.254		0.262
Во	10.3		10.5	0.406		0.414
Ko	2.1		2.3	0.082		0.090
Po	3.9		4.1	0.153		0.161
Р	7.9		8.1	0.311		0.319



STP08CP05 Revision history

# 11 Revision history

Table 12. Document revision history

Date	Revision	Changes
23-May-2007	1	First release
28-Jun-2007	2	Updated Table 7 on page 7
12-Mar-2008	3	Updated <i>Table 8 on page 8</i> and added <i>Figure 11</i> and <i>Figure 12 on page 16</i>
07-Aug-2008	4	Updated Section 8: Typical characteristics on page 15
27-Aug-2010	5	Updated Note: on page 3

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