A digital clock designed for chess games. It mainly consists of two timers which cannot count at the same time. The source clock is alternatively transmitted between the two down counters using a switcher.

ABR-2005 Add files via upload 262bcf3 · 10 months ago

logisim	Add files via upload	last year
snapshots	Add files via upload	last year
verilog	Update chessclock.v	last year
videos	Add files via upload	10 months ago
README.md	Update README.md	10 months ago

The Chess Clock

Team Members

▼ Detail

> Semister: 3rd Sem B.Tech CSE

> Section: S2

> Member-1: Abhyuday Rayala, 221CS239, rayalaabhyuday.221cs239@nitk.edu.in

> Member-2: Pramod Chaitanya Dandu, 221CS235, pramodchaitanya.221cs235@nitk.edu.in

> Member-3: Manohar Rohit Vijay, 221CS230, rohitvijaymanohar.221cs230@nit.edu.in

Abstract

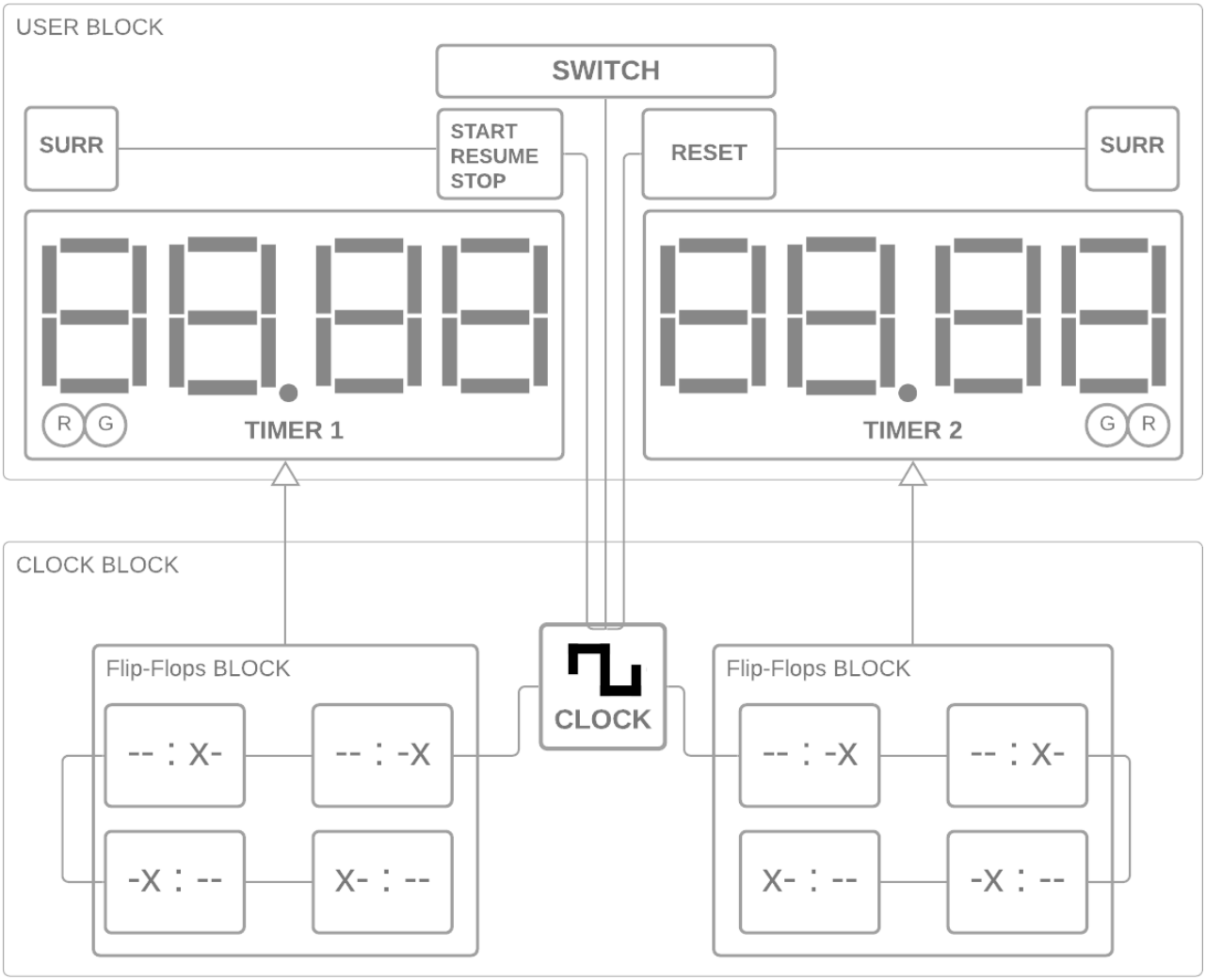
▼ Detail

Chess, a timeless strategy game, has long relied on analog chess clocks for timed play. As the game evolves in the digital age, there is a growing need for a modern, versatile, and user-friendly digital chess clock system. The aim of this mini project, "Development of a Digital Chess Clock System," is to address the shortcomings of traditional chess clocks and provide a solution that enhances the chess playing experience. With the advent of technology, we seek to offer a convenient and feature-rich alternative for chess enthusiasts and tournament organizers. This project introduces a state-of-the-art digital chess clock system that combines precision, usability, and flexibility. The key contributions include: User-Friendly Interface: Our system features an intuitive LCD interface with easily accessible control buttons, ensuring straightforward operation for players of all levels. Customizable Time Controls: Chess players can tailor time settings to suit their preferences, incorporating delay and increment options for added tactical depth. Dual-Clock Mode: The system supports competitive play with dual clocks, making it ideal for tournament use. Accessibility Features: To promote inclusivity, we have integrated audio cues, making the system accessible to visually impaired players.

Description:

A digital clock designed for chess games. It mainly consists of two timers which cannot count at the same time. The source clock is alternatively transmitted between the two down counters using a switcher

The following is a schematic diagram of the idea behind the implementation of this clock:



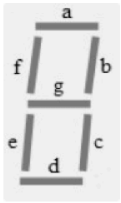
Working

▼ Detail

Timer Logic

-7-seg Display

s03	s02	s01	s00	g	f	e	d	c	b	a
0	0	0	0	0	1	1	1	1	1	1
0	0	0	1	0	0	0	0	1	1	0
0	0	1	0	1	0	1	1	0	1	1
0	0	1	1	1	0	0	1	1	1	1
0	1	0	0	1	1	0	0	1	1	0
0	1	0	1	1	1	0	1	1	0	1
0	1	1	0	1	1	1	1	1	0	1
0	1	1	1	0	0	0	0	1	1	1
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	0	1	1	1	1
1	0	1	0	1	0	1	1	0	1	1
1	0	1	1	0	0	0	0	1	1	0
1	1	0	0	1	0	1	0	0	0	0
1	1	0	1	1	0	0	1	1	0	0
1	1	1	0	1	0	0	0	0	1	0
1	1	1	1	1	0	0	1	1	1	0



OBJ

Game Start

- When the 'start' button is pressed, the clock transitions to player 1's turn. Their timer starts counting down, and the other player's timer is paused.

Player Turn

- During each player's turn, their timer counts down while the opponent's timer remains paused. Players can switch the timers by pressing the 'switch' button. This feature is useful in games where players take turns alternately.

Surrender

- If a player decides to surrender by pressing the 'surrender' button, their timer stops, and their opponent is declared the winner. The losing player's timer displays a red light, while the winning player's timer displays a green light, signaling the game outcome.

Reset

- This option resets the timer of both the players. To start a new match or to end up the match, this can be used.

This digital chess clock ensures fair play by limiting the time available for each move and provides a visual indication of the game's progress, making it a valuable tool for competitive chess matches.

Operation Mode

	Stop/ Start	Nex t	Res et	0 (zero)	Surrend er
Start the game	1	x	0	0	0
Stop the game	0	x	0	0	0
Resume the game	1	x	0	0	0
Bob's turn	1	0	0	0	0
Alice's turn	1	1	0	0	0
Surrender – Finish the game	x	x	x	x	1
Reset the timers	1	x	1	1	0

Functioning

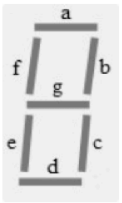
- **Clock Logic**: The main clock feeds both timers with pulses periodically. It is designed in such a way that if any one of the players surrenders, then it stops giving pulses to the timers.
- **Reset Logic**: Moving to the next state by passing only one pulse. Must push on 0 first.
- **Stop/Start Logic**:
    - **Stop**: When Stop/Start pin is set to 0, which is connected to surrender and clock to simulate the required timer.
    - **Start**: When Stop/Start pin is set to 1, Clock gate gets supplied by null voltage, hence activation of one of the timers.

This digital chess clock ensures fair play by limiting the time available for each move and provides a visual indication of the game's progress, making it a valuable tool for competitive chess matches.

Timer Logic

-7-seg Display

s03	s02	s01	s00	g	f	e	d	c	b	a
0	0	0	0	0	1	1	1	1	1	1
0	0	0	1	0	0	0	0	1	1	0
0	0	1	0	1	0	1	1	0	1	1
0	0	1	1	1	0	0	1	1	1	1
0	1	0	0	1	1	0	0	1	1	0
0	1	0	1	1	1	0	1	1	0	1
0	1	1	0	1	1	1	1	1	0	1
0	1	1	1	0	0	0	0	1	1	1
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	0	1	1	1	1
1	0	1	0	1	0	1	1	0	1	1
1	0	1	1	0	0	0	0	1	1	0
1	1	0	0	1	0	1	0	0	0	0
1	1	0	1	1	0	0	1	1	0	0
1	1	1	0	1	0	0	0	0	1	0
1	1	1	1	1	0	0	1	1	1	0



OBJ

Surrender logic

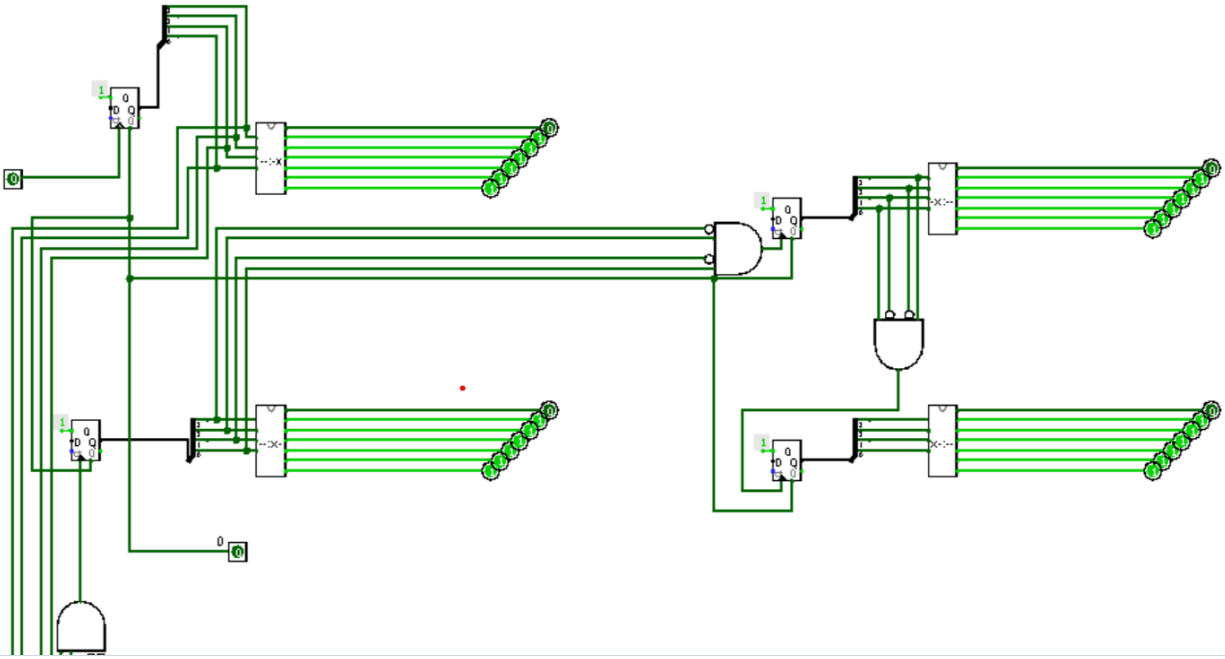
When surrender pin is set to 1, It is in connection with start button, finally resulting in stoppage of the timer and declaring the winner with green light.

README

Logisim Circuit Diagram

▼ Detail

-Clock IC



Releases

No releases published

Create a new release

Packages

No packages published
Publish your first package

Contributors 3

 **rohitmanohar2108** Rohit Manohar

 **PramodC140**

 **ABR-2005** ABHYUDAY RAYALA

Deployments 49

github-pages 10 months ago

+ 48 deployments

Languages

Verilog 100.0%