Rohan-Chandra-04 Update README.md 8430ef4 · 10 months ago

Logisim	submitting dds mini-project	last year
Snapshots	submitting dds mini-project	last year
Verilog_code	submitting dds mini-project	last year
Videos	adding hardware demo	10 months ago
README.md	Update README.md	10 months ago

Patient-Friendly-Digital-Medical-Remainder

Team Details

▼ Detail

> Semester: 3rd Sem B. Tech. CSE

> Section: S2

> Member-1: 221CS215, D R Vikas, drvikas.221cs215@nitk.edu.in,9380745737

> member-2: 221CS221, H Vignesh, hanumanlavignesh.221cs221@nitk.edu.in, 6281971681

> Member-3: 221CS241, R Rohan Chandra, regulagaddarohanchandra.221cs241@nitk.edu.in, 8639884378

Abstract

▼ Detail

IDEA:- The central idea behind our project is to develop a patient- friendly medication reminder system that eliminates the complexities associated with medication scheduling and enhances adherence

OBJECTIVES:- To address the issue, we have developed a patient-friendly medication reminder system using a digital clock interface and LED indicator. The system requires patients to input their preferred dosing time, which can be either morning, afternoon, or evening.

The core functionality of the system is to compare the current time with the patient's selected dosing time and activate an LED indicator when it's time to take the medication. This visual cue makes it easier for patients to adhere to their medication regimen.

The system incorporates real-time clock synchronization to ensure accurate dosing time notifications. Patients can easily set their dosing preferences and adjust them as needed. The LED indicator serves as an intuitive and non-intrusive reminder, enhancing medication adherence while minimizing the risk of missed doses.

This innovative solution provides a user-friendly approach to medication management, improving patient engagement, and potentially contributing to better health outcomes. The abstract outlines the core features of the patient-friendly medication reminder system, which offers a simple and effective way for patients to stay on track with their medication schedules.

COMPONENTS:- 1)T - FLIP - FLOP

2)REGISTERS

3)COMPARTORS

4)LED FLASH LIGHT

5)DECODERS

Working

▼ Detail
The Patient-Friendly Digital Clock with Alarm is a

specialized digital clock designed to cater to the unique needs of patients. It provides a binary display, ensuring patients can easily keep track of time. The clock is equipped with customizable alarm settings, making it an essential tool for individuals who require timely medication, appointments, or rest.

Key Features:

Customizable Alarms: Patients can set 3 alarms throughout the day, helping them remember important tasks such as medication schedules.

Components Description:-

3 Registers: -Each Registers comprising 7 bits. These registers are activated by a single 'enable' bit, granting them functionality. Within their structure, 3 bits are dedicated to timekeeping. Additionally, 2 sets of 2 bits are reserved for storing up to 4 different medicines. The flexibility of these registers allows any combination of 2 of 4 medicines to be stored at a time.

the registers. When a match occurs, the system suggests the medicines stored in the corresponding registers to the patient.

6 Decoders:- each decoder converts binary to decimal equivalent which represents to take which medicines.

LED flash-lights:- The LED Flashlights in our system serve as instant visual indicators. When the comparators successfully match the timings, these LED flashlights illuminate, providing a clear and immediate signal to the patient.

3 T flip-flop:- They are employed to facilitate the up- counting process of the three bits.

Working:-

Flowchart

Working Model:

1. Clock Pulse Trigger: A clock pulse initiates and synchronizes the circuit's operation, serving as the system's heartbeat.

2. T Flip-Flop Up-Counter (Counts 0-7):

• Three T flip-flops work in tandem, enabling the up-counter to cycle through values from 0 to 7.

• These values represent different time intervals in the patient's daily schedule.

3. Display of 3 Bits:

• A display module showcases the 3 bits from the up-counter, which together represent the current time interval.

4. Comparator Operation:

• Dedicated comparators diligently compare the 3 bits from the up-counter with the 3 bits stored within each of the three registers.

• The purpose is to pinpoint a precise match with the time settings stored in the registers.

5. Activation of Decoders:

• When a match occurs, the corresponding comparator activates the enable bit for the associated decoder.

• This decision-making step ensures that only the decoder relevant to the current time interval is enabled.

6. Decoder Operation:

• Enabled by the comparators, the decoders come into play.

• They convert the 2 bits assigned to medicines into a decimal representation.

• This decimal value corresponds to a specific medicine to be

7)LED Flashlights Activation:

• The system doesn't rely solely on numeric output; it incorporates immediate visual cues.

• When the comparators find a match, indicating the prescribed time interval, the corresponding LED flashlights come to life.

• This serves as an unmistakable signal for the patient to take the medicines associated with the matched timings.

By following this intricate but well-structured sequence, the system ensures that patients receive timely and specific medication

reminders, promoting health and adherence to their prescribed

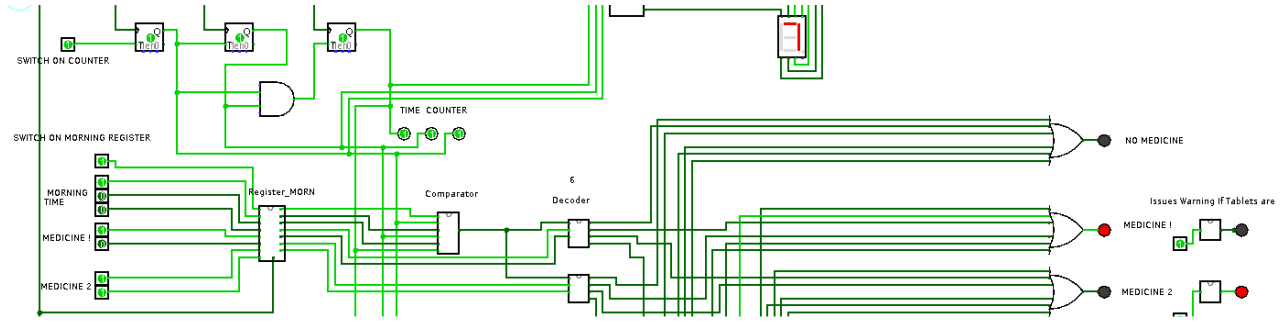
regimen.

CLOCK	RESET	LD_MORN	DATA_MORN	LD_NOON	DATA NOON	LD_NIGHT	DATA_NIGHT
0	X	X	XXX XX XX	X	XXX XX XX	X	XXX XX XX
1	0	1	110 00 01	1	100 10 11	0	111 00 10
1	0	1	110 00 01	1	100 10 11	1	111 00 10
1	0	0	110 00 01	1	100 10 11	1	111 00 10

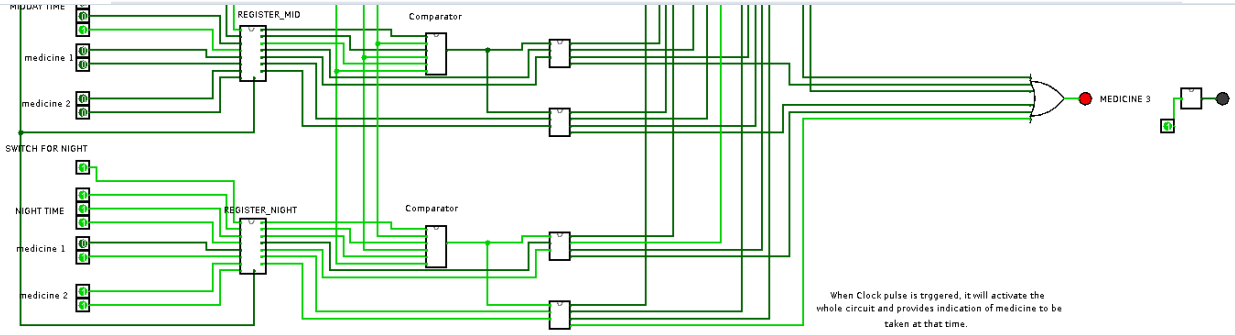
morning shift medication for person				afternoon shift medication for person				night shift medication for person			
med_1	med_2	med_3	med_4	med_1	med_2	med_3	med_4	med_1	med_2	med_3	med_4
1	1	0	0	0	0	1	1	0	0	0	0
1	1	0	0	0	0	1	1	1	0	1	0
1	1	0	0	0	0	1	1	1	0	1	0

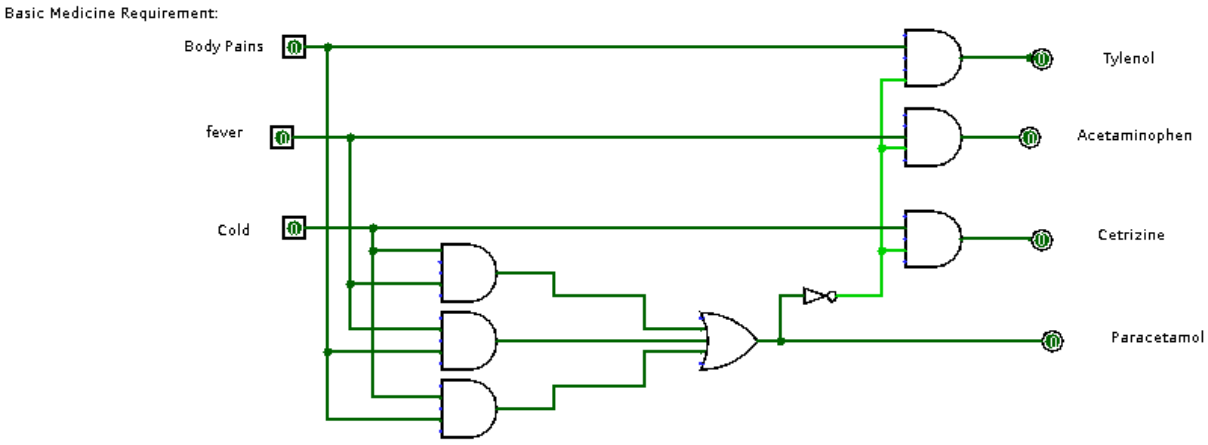
Logisim Circuit Diagram

▼ Detail



README





Verilog Code

Releases

No releases published
Create a new release

Packages

No packages published
Publish your first package

Languages

- **Verilog** 100.0%