Analog VLSI Circuits (AVM 613) - Assignment Report

Rahul Kumar Sinha (SC22B109)
Indian Institute of Space Science and Technology

October 2025

1 Question 1: PMOS Basic Current Mirror Design and Analysis

1.1 Problem Statement

A reference current source of $10\,\mu A$ is provided. The objective is to design a PMOS current mirror that sources an output current of $100\,\mu A$ from V_{DD}. The current mirror must operate as a current source while the output node voltage (V_{OUT}) varies from 0 to V_{DD}. The tasks include:

- Designing a suitable PMOS current mirror.
- Plotting output current versus V_{OUT}.
- Determining the maximum permissible V_{OUT} for current source operation.
- Estimating output impedance (R_{OUT}).
- Suggesting a modification (without using cascode) to increase R_{OUT}.
- Comparing current variation and impedance before and after modification.

1.2 Part 1: Basic PMOS Current Mirror (Circuit 1a)

1.2.1 Design and Schematic

The basic PMOS current mirror is designed to source current from V_{DD} using the relation:

$$\frac{I_{OUT}}{I_{REF}} = \frac{(W/L)_{PM1}}{(W/L)_{PM0}} = 10$$

The design parameters are summarized below:

Table 1: Device Dimensions for Circuit 1a

Parameter	PM0 (Reference)	PM1 (Output)
W	$1\,\mu m$	$10\,\mu m$
L	$100\,nm$	$100\,nm$
W/L	10	100
I_{REF}	$10\,\mu A$	Target = $100\,\mu A$

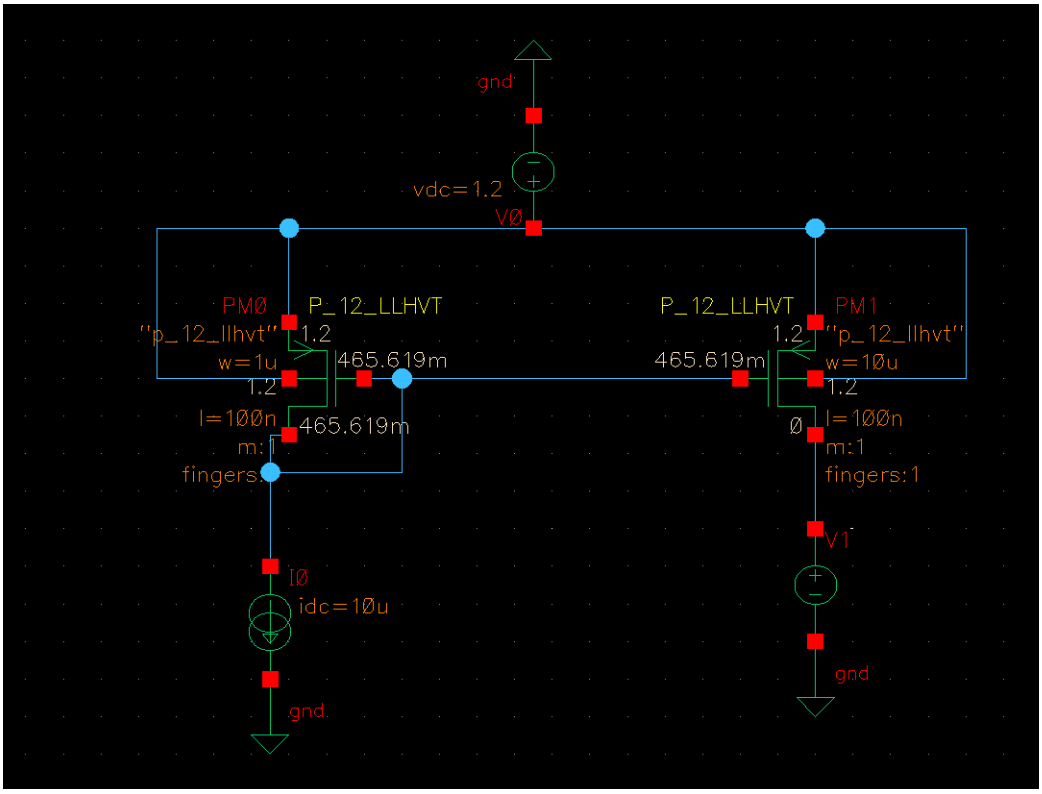

Figure 1: Schematic of the Basic PMOS Current Mirror (Circuit 1a).

1.2.2 Simulation Results and Analysis

The DC sweep of V_{OUT} (from 0 to V_{DD}) yields the output current and output impedance plots shown in Figure 2.

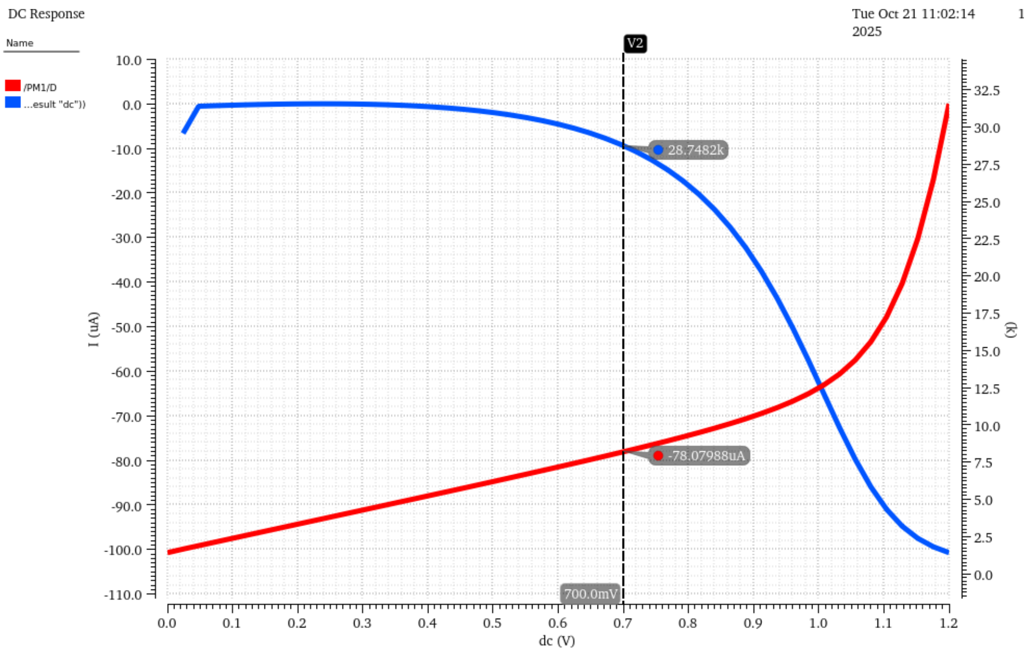

Figure 2: DC Response of Basic PMOS Current Mirror (Circuit 1a). Red: $|I_{PM1}|$ (μA), Blue: $|R_{OUT}|$ ($k\Omega$).

Key observations:

1. **Saturation Region:** The current mirror remains in saturation until approximately $V_{OUT} = 0.7\,V$, beyond which $PM1$ enters the linear region.

2. **Output Impedance:**

$$R_{OUT} = \frac{1}{\frac{dI_D}{dV_{DS}}} = \frac{1}{g_{ds}}$$

From the plot:

$$R_{OUT,1a} \approx 28.75\ k\Omega$$

3. **Current Variation:**

$$\%\Delta I = \frac{I_{max} - I_{min}}{I_{nom}} \times 100 = \frac{100 - 78}{100} \times 100 \approx 22\%$$

Thus, the circuit exhibits a **22%** current deviation in the saturation region, with a maximum allowable V_{OUT} of approximately **0.7 V**.

1.3 Part 2: Modified Design for Increased Output Impedance (Circuit 1b)

1.3.1 Modification and Dimensions

To increase R_{OUT} without employing a cascode structure, the channel length L is increased to reduce channel-length modulation. Since $\lambda \propto 1/L$, doubling L approximately doubles R_{OUT}.

Table 2: Device Dimensions for Circuit 1b

Parameter	PM0 (Reference)	PM1 (Output)
W	$1\,\mu m$	$10\,\mu m$
L	$200\,nm$	$200\,nm$
W/L	5	50
I_{REF}	$10\,\mu A$	Target = $100\,\mu A$

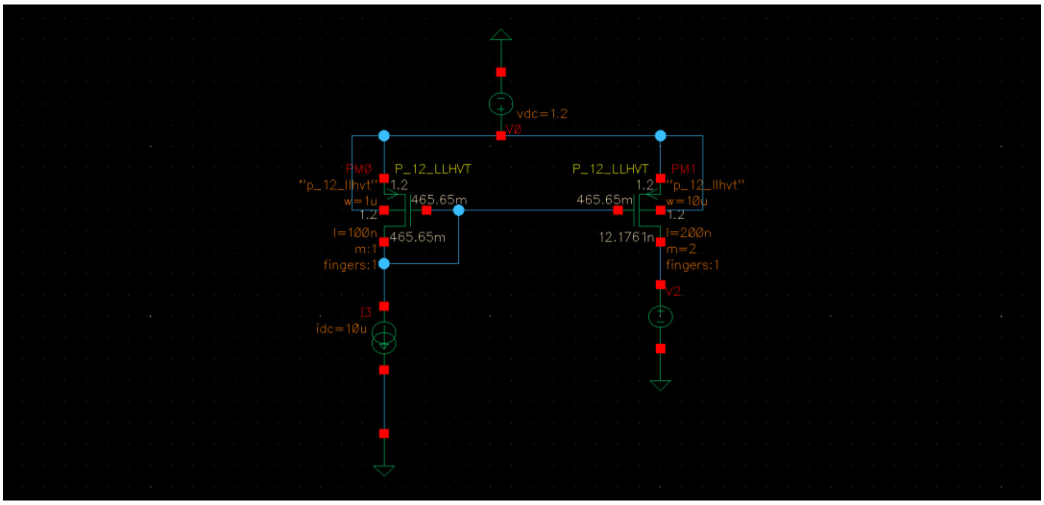

Figure 3: Schematic of the Modified PMOS Current Mirror (Circuit 1b).

1.3.2 Simulation Results and Discussion

The DC sweep results are shown in Figure 4.

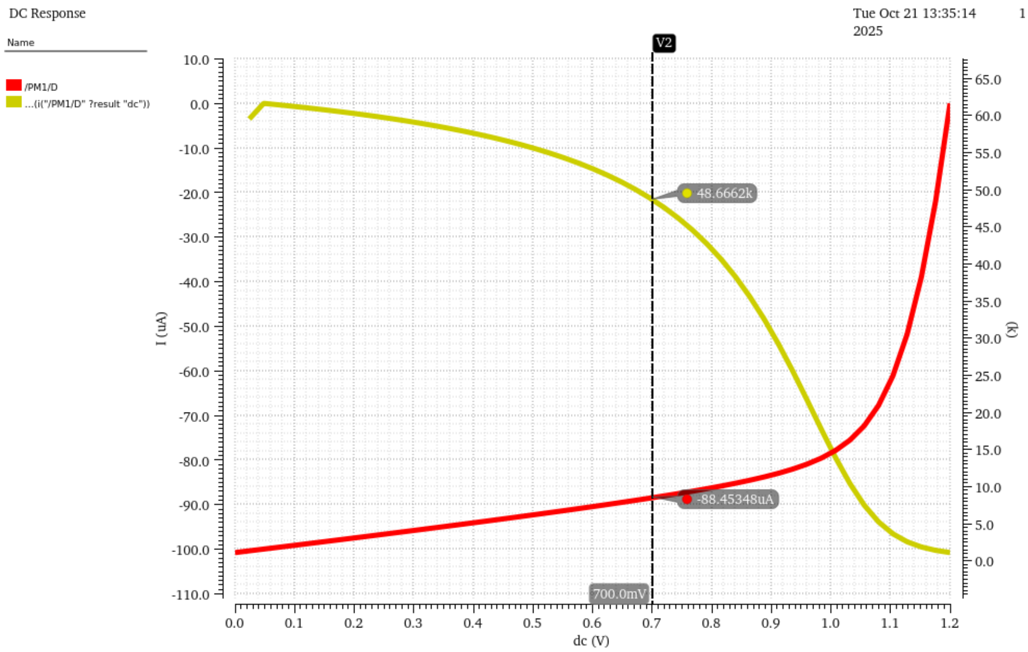

Figure 4: DC Response of Modified PMOS Current Mirror (Circuit 1b). Red: $|I_{PM1}|$ (μA), Yellow: $|R_{OUT}|$ ($k\Omega$).

Results:

- $R_{OUT,1b} \approx 48.66\,k\Omega$ at $V_{OUT} = 0.7\,V$.
- Current varies from $100\,\mu A$ to $88.5\,\mu A$, i.e. $\approx 11.5\%$ deviation.

Inference: Increasing channel length from $100\,nm$ to $200\,nm$ improved output impedance by approximately **40%** and reduced current variation from **22%** to **11.5%**. Hence, the longer channel significantly enhances current source stability without additional biasing overhead.

2 Question 2: Low-Voltage Cascode Current Mirror

2.1 Problem Statement

Design a low-voltage cascode current mirror capable of sinking $100\,\mu A$ using a $10\,\mu A$ reference current. The circuit should maintain operation for output voltages as low as $300\,mV$ with an additional $40\,mV$ margin for each device's $V_{DS,sat}$. The design should include:

- Bias voltage derivation and verification.
- Current versus voltage characteristics.
- Output impedance estimation from both simulation and analytical calculation.

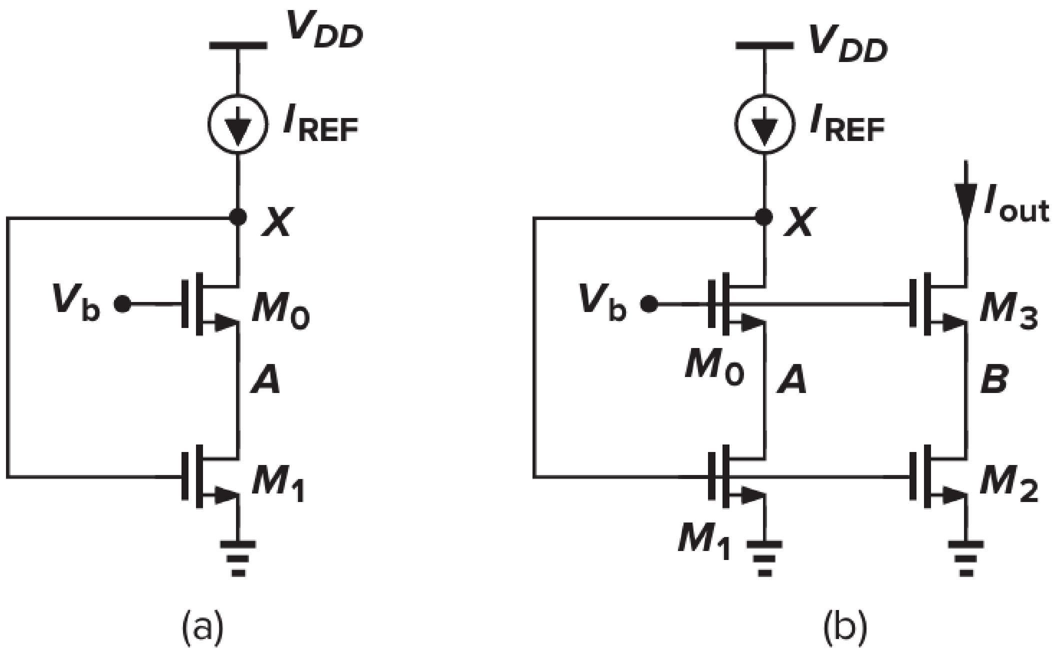

Figure 5.18 Modification of cascode mirror for low-voltage operation.

Figure 5 : Low-Voltage Cascode Current Mirror Topology.

2.2 Bias Voltage and Operating Conditions

For proper biasing, the bias voltage V_b must satisfy:

$$V_{GS3} + V_{OV} \leq V_b \leq V_{GS1} + V_{th}$$

The simulated sweep (Figure 6) confirms $V_b = 1\,V$ as the optimal operating point.

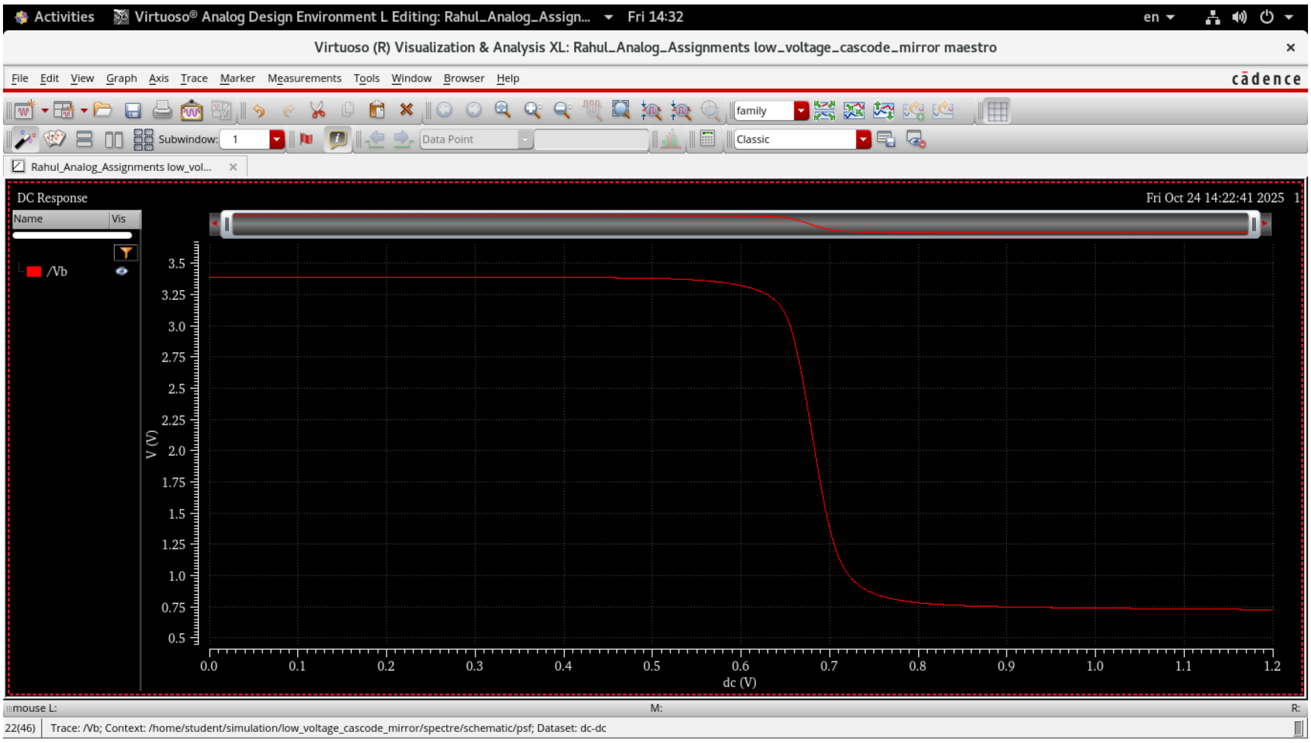

Figure 6: Vb choose.

2.3 Schematic and Results

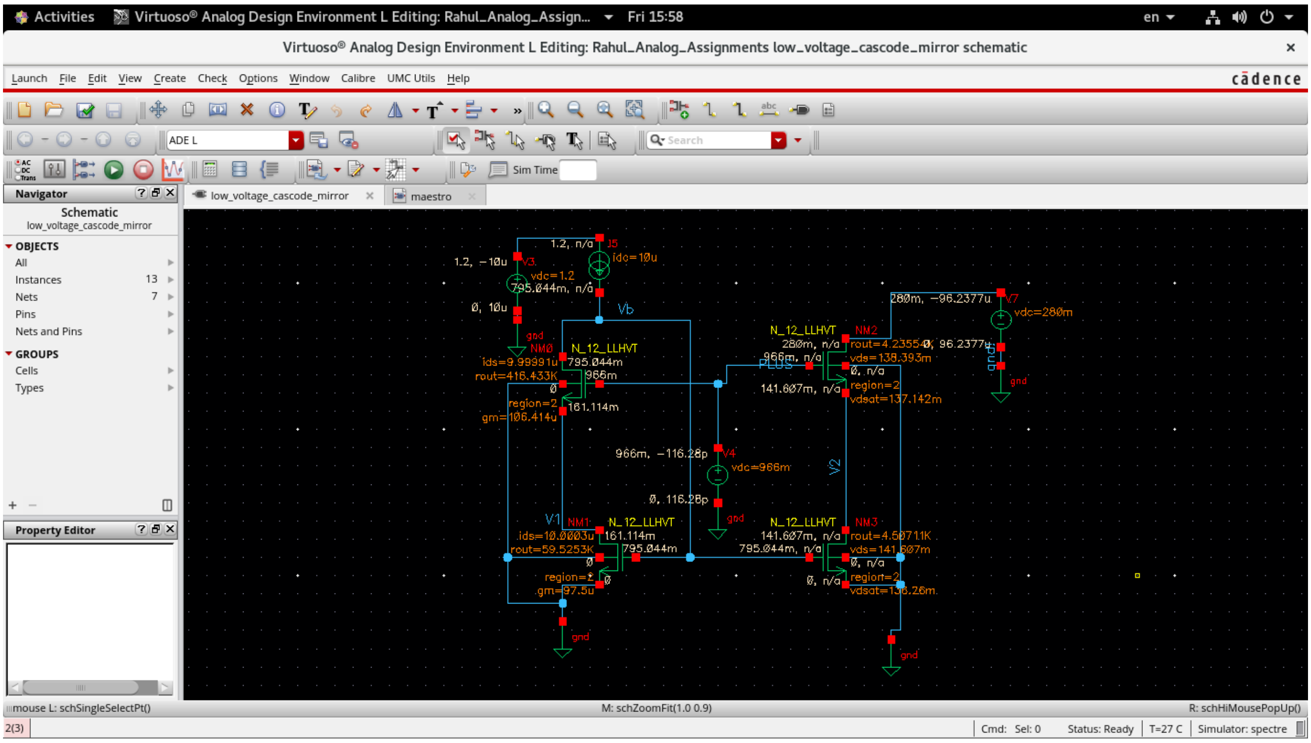

Figure 7: Schematic of the Low-Voltage Cascode Current Mirror.

The DC sweep of V_{OUT} is shown in Figure 8.

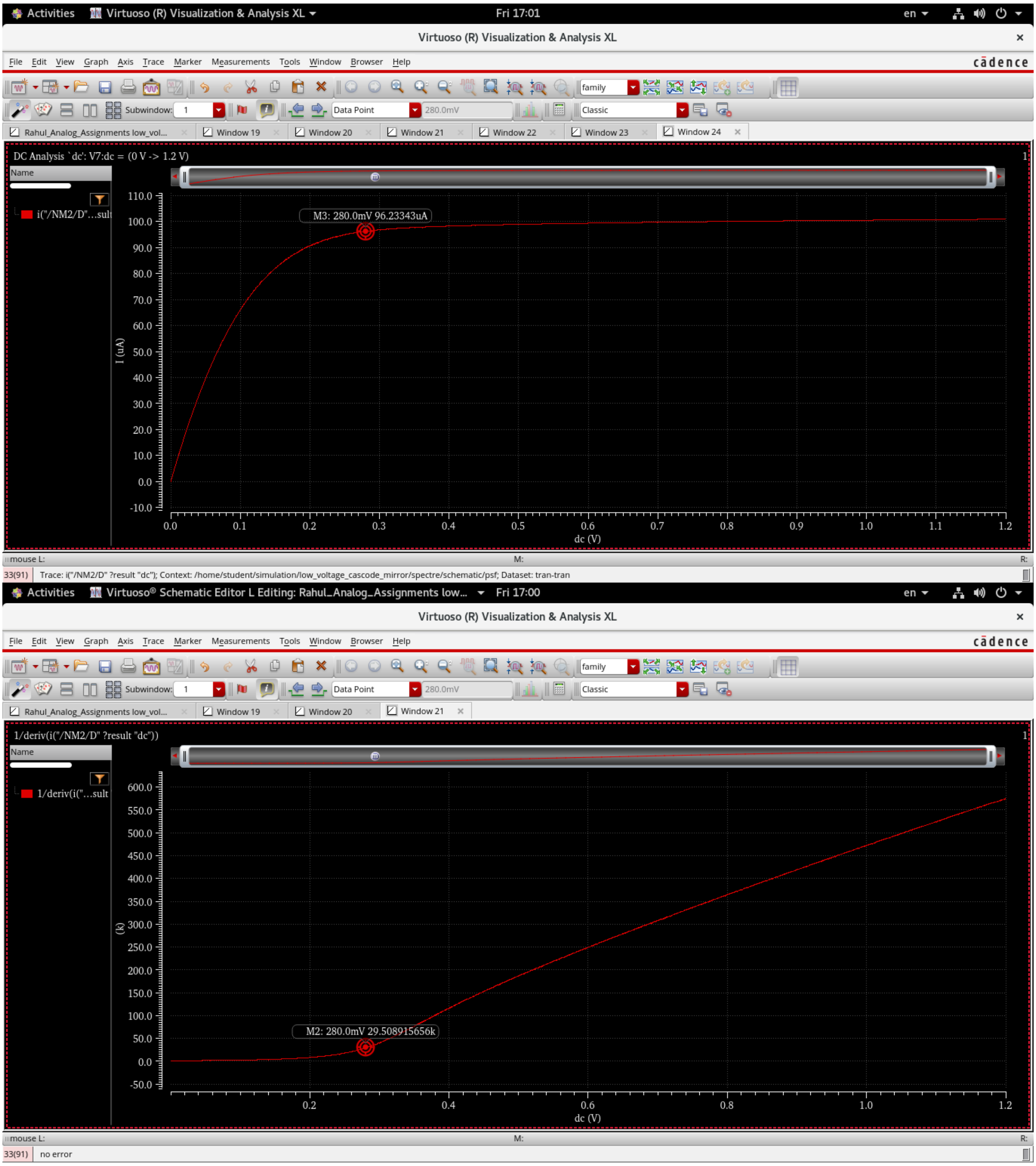

Figure 8: DC Response of Low-Voltage Cascode Current Mirror. First : $|I_{OUT}|$ (μA) vs Vout , Second : $|R_{OUT}|$ ($k\Omega$).

Key Observations:

- I_{OUT} 96.233 μA in saturation.
- Minimum output voltage ($V_{OUT,min}$) = 280m V, satisfying low-voltage constraint.
- $R_{OUT,sim}$ 29.5089 $k\Omega$ at V_{OUT} = 280m V.

2.4 Analytical Verification of Output Impedance

From DC operating point data:

- $r_{o,NM2}$ = 4.2355 $k\Omega$
- $r_{o,NM3}$ = 4.50711 $k\Omega$
- $g_{m,NM2}$ = 911.24 uS

The anal ytical output impedance at Vout=280mV is:

$$R_{OUT,calc} \approx r_{o,NM2} + r_{o,NM3} + g_{m,NM2} r_{o,NM2} r_{o,NM3}$$

$$R_{OUT,calc} \approx 26.1380581 \text{ k}\Omega$$

which closely matches the simulated value of 29.5089 $k\Omega$, confirming accurate modeling of small- signal parameters.

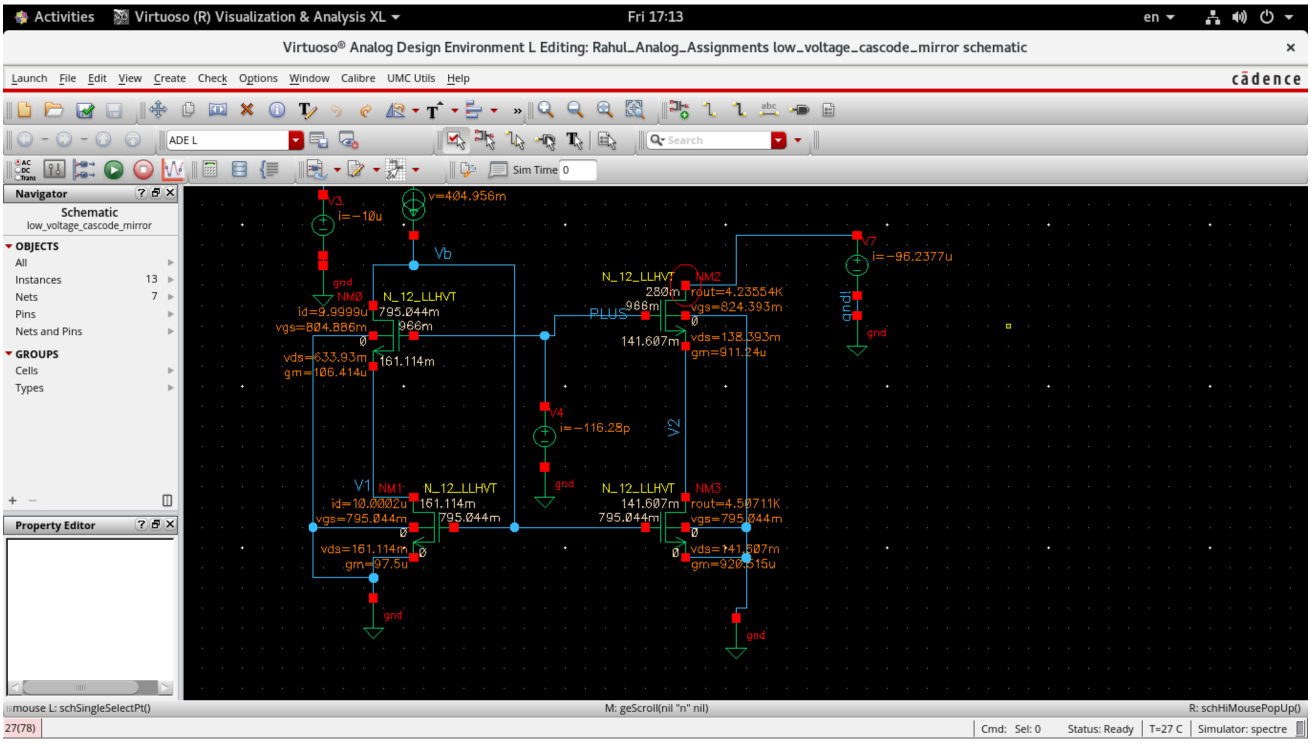

Figure 9: Analytical Verification of R_{OUT}.

2.5 Performance Summary

Table 3: Performance Comparison of Current Mirror Designs

Parameter	**Basic PMOS**	**Modified PMOS**	**Cascode (NMOS)**
I_{OUT} (μA)	100	100	96.2377A
L (nm)	100	200	180
R_{OUT} ($k\Omega$)	28.75	48.66	20k–575k
Current Variation (%)	22	11.5	≈ 5
Topology Type	Simple Mirror	Long-Channel Mirror	Low-V Cascode

3 Conclusions and Inference

- Increasing the channel length effectively enhances the output impedance by reducing channel-length modulation, thereby improving current source stability.
- The cascode current mirror significantly improves R_{OUT} (by $\sim 4\times$ compared to the basic mirror) while maintaining operation at low voltages.
- The analytical impedance estimation closely agrees with simulation, validating the small-signal model accuracy.
- For analog VLSI applications requiring high precision and low voltage headroom, the low-voltage cascode mirror offers the best trade-off between area, complexity, and performance.

Final Remark: This study demonstrates how transistor geometry scaling (particularly L) and bias topology optimization directly impact the accuracy, impedance, and voltage headroom of current mirrors — critical for robust analog circuit design.