

(1)

Date.:

<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
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Number System

Decimal	Binary	Octal	Hexadecimal
0	0	0	0 A → 10
1	1	1	1 B → 11
2		2	2 C → 12
3		3	3 D → 13
4		4	4 E → 14
5		5	5 F → 15
6		6	6
7		7	7
8			8
9			9

★ Decimal to Binary

i) $(128)_{10} = (10000000)_2$

2	128	0	↑
2	64	0	
2	32	0	
2	16	0	
2	8	0	
2	4	0	
2	2	0	

ii) $(23)_{10} = (10111)_2$

2	23	1
2	11	1
2	5	1
2	2	0

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iii) $(255.25)_{10} = (1111111.01)_2$

2	255	1
2	127	1
2	63	1

$$0.25 \times 2 = 0.5$$

$$0.5 \times 2 = 1.0 \downarrow$$

2	32	1
2	15	1
2	7	1
2	3	1
	1	1

iv)

iv) $(191.75)_{10} = (1011111.11)_2$

2	191	1
2	95	1
2	47	1
2	23	1
2	11	1
2	5	1
2	2	0
	1	1

★ Decimal to Octal

i) $(23)_{10} = (27)_8$

8	23	7
2	2	

ii) $(128)_{10} = (200)_8$

8	128	0
8	16	0
2	2	

iii) $(255.25)_{10} = (377.2)_8$

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$$0.25 \times 8 = 2.0$$

8	255	7
8	31	7
3	3	

iv) $(191.75)_{10} = (277.6)_8$

8	191	7
8	23	7
2	2	

★ Decimal to Hexadecimal

i) $(192)_{10} = (C0)_{16}$

16	192	0
12	C	

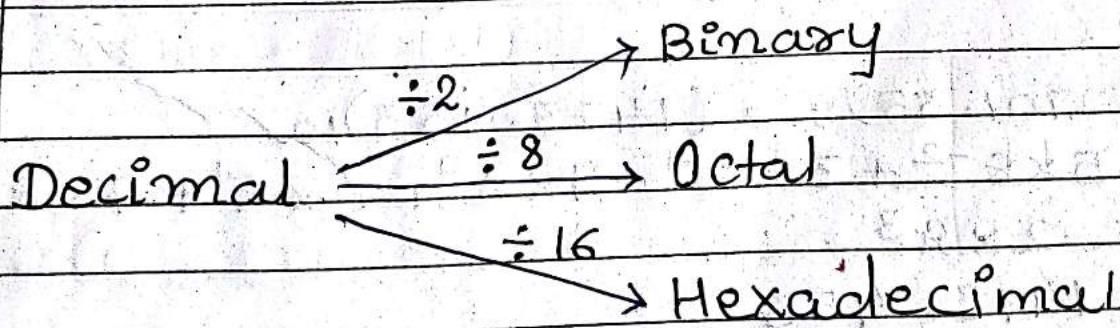
ii) $(2138)_{10} = (85A)_{16}$

16	2138	10
16	133	5
8	8	

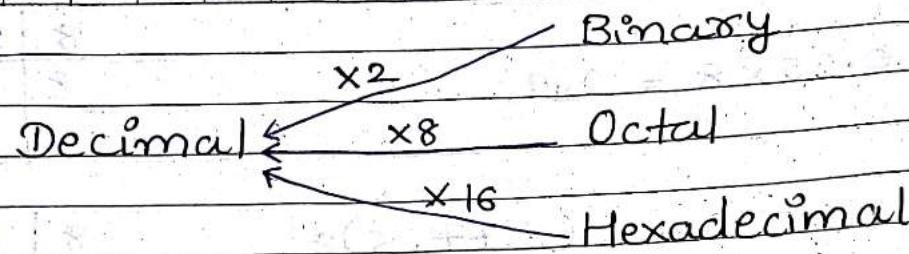
iii) $(255.75)_{10} = (FF.C)_{16}$

16	255	15
15	15	

$$0.75 \times 16 = 12$$



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★ Binary to Decimal

i) $(10110)_2 = (22)_{10}$

$$= 0 \times 2^0 + 1 \times 2^1 + 1 \times 2^2 + 0 \times 2^3 + 1 \times 2^4 \\ = 22$$

ii) $(11011.110)_2 = (27.75)_{10}$

$$= 1 \times 2^0 + 1 \times 2^1 + 0 \times 2^2 + 1 \times 2^3 + 1 \times 2^4 + 1 \times 2^{-1} + \\ 1 \times 2^{-2} + 0 \times 2^{-3} \\ = 27.75$$

★ Octal to Decimal

i) $(356)_8 = (238)_{10}$

$$= 6 \times 8^0 + 5 \times 8^1 + 3 \times 8^2 \\ = 238$$

ii) $(2701.35)_8 = (1473.453)_{10}$

$$= 5 \times 8^{-2} + 3 \times 8^{-1} + 1 \times 8^0 + 0 \times 8^1 + 7 \times 8^2 + \\ 2 \times 8^3 \\ = 1473.453$$

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* Hexadecimal to Decimal

$$\text{i) } (2FC3)_{16} = (12227)_{10}$$

$$= 3 \times 16^0 + 12 \times 16^1 + 15 \times 16^2 + 2 \times 16^3$$

$$= 12227$$

$$\text{ii) } (F2.2F)_{16} = (242.18)_{10}$$

$$= 15 \times 16^{-2} + 2 \times 16^{-1} + 2 \times 16^0 + 15 \times 16^1$$

$$= 242.1835$$

* Binary to Octal

$$\text{i) } (110110)_2 = (66)_8$$

$$= 0 \times 2^0 + 1 \times 2^1 + 1 \times 2^2 + 0 \times 2^3 + 1 \times 2^4 + 1 \times 2^5$$

$$= (54)_{10}$$

$$= (66)_8$$

	8	54	6
	6	6	

$$\text{ii) } (1101111.111)_2$$

$$= (157.7)_8$$

$$1 \quad 5 \quad 7 \quad 7$$

$$8 = 2^3$$

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	8	4	2	1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
A	1	0	1	0
B	1	0	1	1
C	1	1	0	0
D	1	1	0	1
E	1	1	1	0
F	1	1	1	1

★ Octal to Binary

i) $(54)_8 = (101100)_2$

ii) $(62.57)_8 = (110010.101111)_2$

★ Hexadecimal to Binary

i) $(2F3E)_{16} = (0010111100111110)_2$

$16 = 2^4$

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★ Binary to Hexadecimal

$$i) (101101.01011)_2 = (2D.58)_{16}$$

$$ii) (11011001)_2 = (D9)_{16}$$

★ Octal to Hexadecimal

$$i) (437)_8 = (100011111)_2 \\ = (11F)_{16}$$

$$ii) (456.71)_8 = (10010110.111001)_2 \\ = (12E.E4)_{16}$$

★ Hexadecimal to Octal

$$i) (A3F4)_{16} = (101000111110100)_2 \\ = (121764)_8$$

$$ii) (DF.AB)_{16} = (01101111.10101011)_2 \\ = (337.526)_8$$

$$iii) (E2.C)_{16} = (011100010.1100)_2 \\ = (342.60)_8$$

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Complement → Use for Binary Subtraction

$$\begin{array}{r} \text{last } \rightarrow \\ \text{as it is,} \\ \text{before it,} \\ \text{all comple-} \\ \downarrow \\ \text{2's} \\ (1011011)_2 - 1's \rightarrow (0100100)_2 \\ (0100101)_2 \end{array}$$

$$2^{\text{'s}} \text{ Complement} = 1^{\text{'s}} \text{ Complement} + 1$$

$$\begin{array}{r} \text{2's} \\ \downarrow \\ (100110)_2 - 1's \rightarrow (011001)_2 \\ (011010)_2 \end{array}$$

$$\begin{array}{r} \text{2's} \\ \downarrow \\ (100000)_2 - 1's \rightarrow (011111)_2 \\ (100000)_2 \end{array}$$

$$\begin{array}{r} 9 & 1001 \xrightarrow{\text{As it is}} 1001 \\ -5 & -0101 \xrightarrow{\text{2's}} +1011 \\ 4 & 0100 \xrightarrow{\text{ignore}} \end{array}$$

Step-1
Step-2
Step-3
Step-4

Step-5

Step-6

- Steps of Combinational Circuit

Step-1 The problem is stated.

Step-2 Identify number of input or output required.

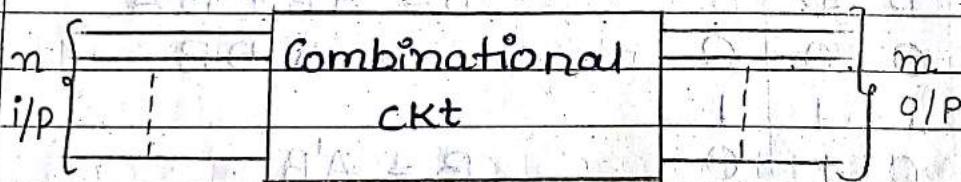
Step-3 Assign letter symbol to each input & output.

Step-4 Make a truth table which shows relationship between input & output.

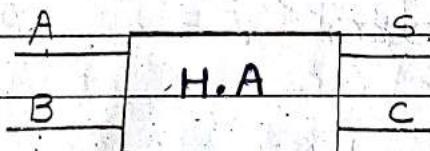
Step-5 Obtain simplified boolean function for each output.

Step-6 Draw circuit diagram.

- Combinational CKT



- Half adder



- T.T

I/P	O/P
-----	-----

A	B	S	C
---	---	---	---

0	0	0	0
---	---	---	---

0	1	1	0
---	---	---	---

1	0	1	0
---	---	---	---

1	1	0	1
---	---	---	---

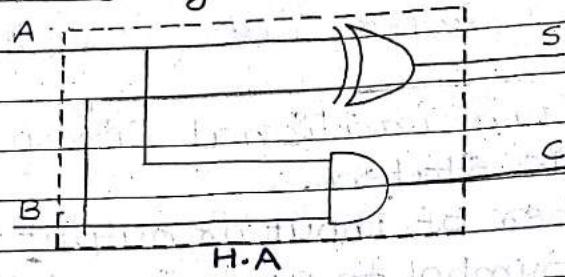
$$S = A'B + B'A$$

$$= A \oplus B$$

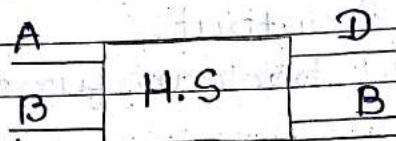
$$C = A \cdot B$$

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Circuit Diagram



Design Half Subtractor



T.T

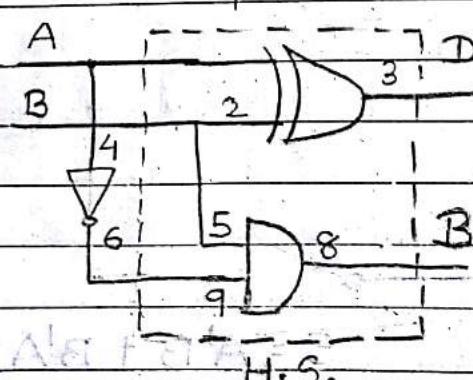
A	B	D	B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

$$D = A'B + B'A$$

$$= A \oplus B$$

$$B = A'B$$

Circuit Diagram



H.S.

$B \oplus A$

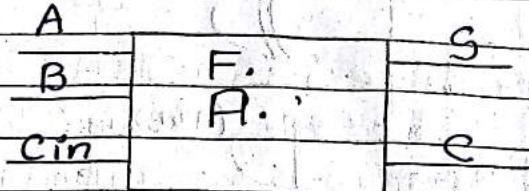
$B \cdot A = 0$

$0 \cdot 1 = 0$

$1 \cdot 0 = 0$

$1 \cdot 1 = 1$

Design Full Adder ckt



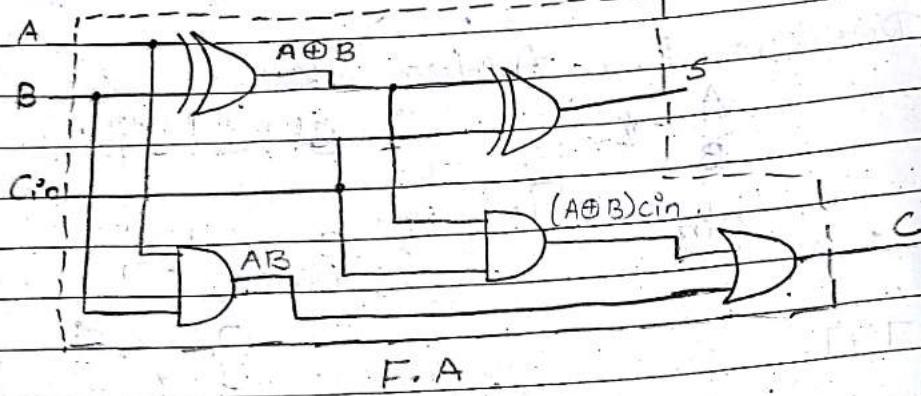
T.T.

I/P			O/P	
A	B	Cin	S	C
0	0	0	0	0
0	1	0	1	0
0	0	1	1	0
1	0	0	1	0
1	1	0	0	1
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

$S = A'B'Cin + A'B'C'in + AB'C'in + ABCin$
 $= A'C(BC'in + B'Cin) + AC(B'C'in + BCin)$
 $= A'(B \oplus C'in) + A(B \ominus Cin)$
 $C = 0$
 $= A'(B \oplus C'in) + A(B \oplus C'in)$
 $= A'x + Ax'$
 $= A \oplus x$
 $S = A \oplus B \oplus Cin$

$$\begin{aligned}
 C &= ABC'_{in} + AB'C_{in} + A'BC_{in} + ABC_{in} \\
 &= A(BC'_{in} + B'C_{in}) + BC_{in}(A' + A) \\
 &= A(B \oplus C) + BC_{in} \\
 &= (A \oplus B)C_{in} + AB
 \end{aligned}$$

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Design Full Subtractor CKT

A	B	Cin	F.S	D
0	0	0	0	$D = A'B'Cin + A'BCin +$
0	0	1	1	$AB'Cin + ABCin$
0	1	0	1	$= A'(B'Cin + BCin) +$
0	1	1	0	$A(BCin + BCin)$
1	0	0	1	$= A'(B \oplus C) + A(B \oplus C)$
1	0	1	0	$= A'x + Ax'$
1	1	0	0	$= A \oplus x$
1	1	1	1	$= A \oplus B \oplus Cin$

$$Bx = A'B'Cin + A'BCin +$$

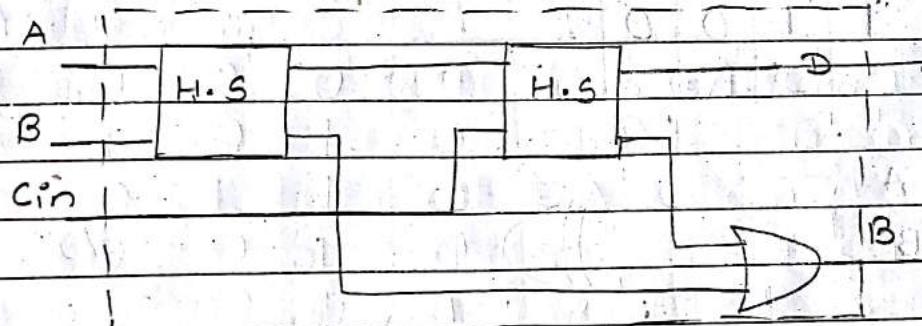
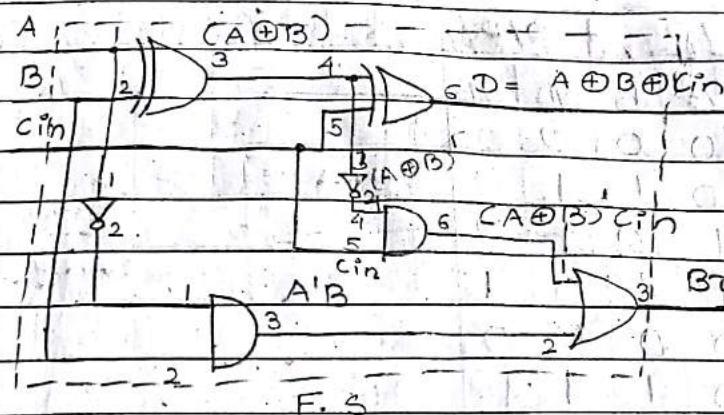
$$A'BCin + ABCin$$

$$= A'(B'Cin + BCin) +$$

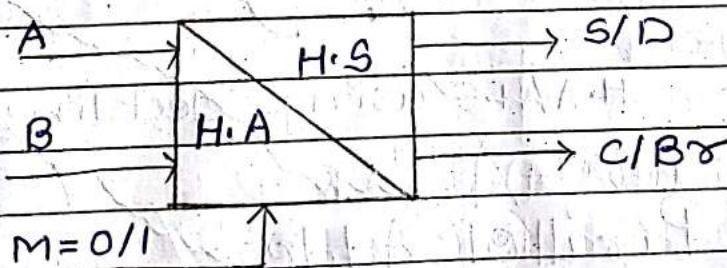
$$BCin(A' + A)$$

$$= A'(B \oplus C) + BCin$$

$$= (A \oplus B)'Cin + A'B$$



Design Half Adder & Half Subtractor
using Select line .

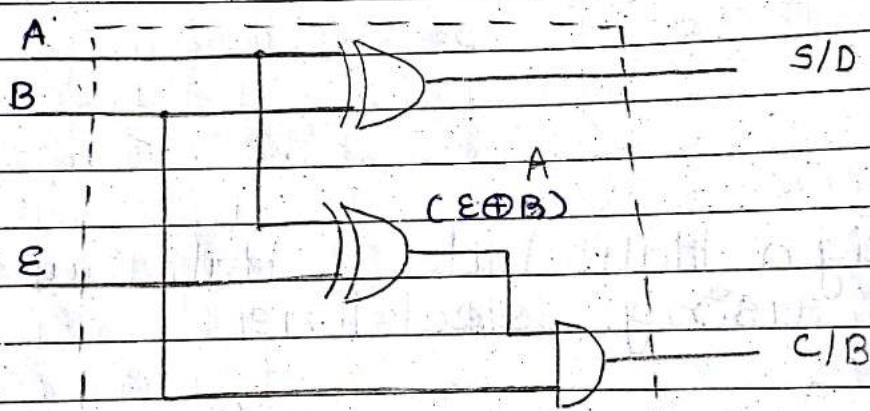


$$S/D = A \oplus B$$

$$\begin{aligned} C/B &= E'AB + EA'B \\ &= (E'A + EA')B \\ &= (E \oplus A)B \end{aligned}$$

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I/P	O/P	A-B	A-B
E A B S/D C/B		A ₁ A ₂ B ₁ B ₂ H ₁	H ₂
0 0 0 0 0		00 00 1	0
0 0 1 1 0	H.A	01 01 0	1
0 1 0 1 0		10 00 0	0
0 1 1 0 1		11 11 1	0
1 0 0 0 0	H.S	11 11 1	
1 0 1 1 1		Y ₁ (A-B) = A ⊕ B	
1 1 0 1 0		Y ₂ = A'B	
1 1 1 0 0		Y ₃ = AB	



H.A/H.S using select line

Repetit Carry Adder

Binary Parallel Adder /

B₄ A₄ B₃ A₃ B₂ A₂ B₁ A₁ + 0001 10000

↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓

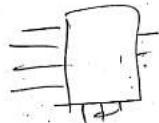
C₅ C₄ C₃ C₂ C₁

← F.A ← F.A ← F.A ← F.A ← F.A ←

S₄ S₃ S₂ S₁

0 0 0 0

2^{n+m}



0 0 1 0
Date: _____

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A₄ A₃ A₂ A₁ B₄ B₃ B₂ B₁

C₅ ←

4-Bit Binary
Parallel Adder

A = B

A = B A ≈ B A ≈ B

S₄ S₃ S₂ S₁

excess

Design BCD to excess three converter
(Binary coded Decimal)

No.	BCD	Excess-3	BCD
0	0 0 0 0	0 0 1 1	+ 0011 Excess-3
1	0 0 0 1	0 1 0 0	
2	0 0 1 0	0 1 0 1	X-3
3	0 0 1 1	0 1 1 0	
4	0 1 0 0	0 1 1 0	10 11, 12, 13
5	0 1 0 1	1 0 0 0	
6	0 1 1 0	1 0 0 1	
7	0 1 1 1	1 0 1 0	
8	1 0 0 0	1 0 1 1	
9	1 0 0 1	1 1 0 0	14, 15

BCD

0 0 1 1

B₄ B₃ B₂ B₁

C₅ ←

4-Bit Binary
Parallel Adder

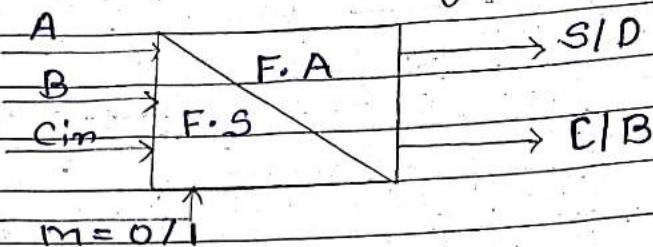
← C₁ = 0

S₄ S₃ S₂ S₁

Excess-3

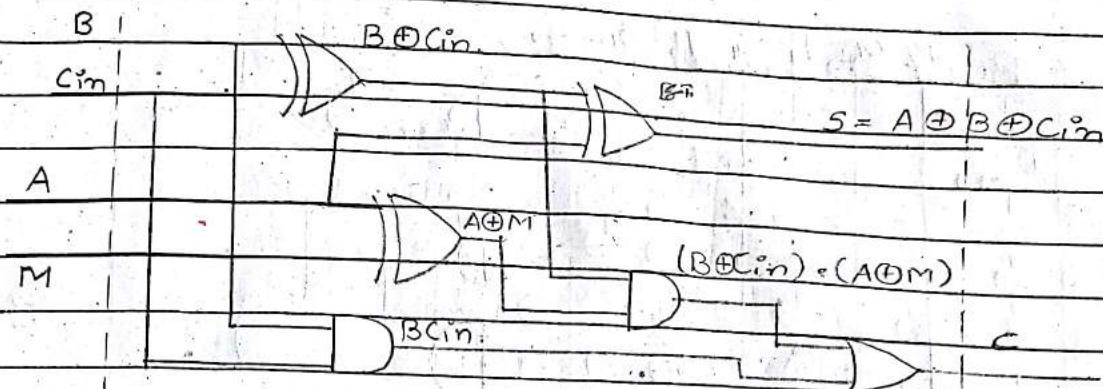
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Design Full Adder and Full Subtractor using select line



	I/P .			O/P	
M	A	B	Cin	S/D	C/B
0	0	0	0	0	0
0	0	0	1	1	0
0	0	1	0	1	0
0	0	1	1	0	1
1	0	0	0	1	0
1	0	1	0	1	$S/D = A \oplus B \oplus Cin$
1	1	0	0	1	$C/B = B \oplus Cin$
1	1	1	1	1	$C/B = B \oplus Cin$
1	0	0	0	0	$(E \oplus A)(B \oplus Cin)$
1	0	1	1	1	$(E \oplus A)(B \oplus Cin)$
1	0	1	0	0	$(E \oplus A)(B \oplus Cin)$
1	1	0	0	1	$(E \oplus A)(B \oplus Cin)$
1	1	0	1	0	$(E \oplus A)(B \oplus Cin)$
1	1	1	0	0	$(E \oplus A)(B \oplus Cin)$
1	1	1	1	1	$(E \oplus A)(B \oplus Cin)$

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Look Ahead Carry Generator

$$\text{Let } P = A \oplus B.$$

$$- G_1 = AB.$$

$$S = A \oplus B \oplus C_{in}$$

$$= P \oplus C_{in}.$$

$$C = (A \oplus B)C_{in} + AB.$$

$$= PC_{in} + G_1$$

$$C_{i+1} = G_{i+1} + P_i C_i$$

$$C_1 = G_{10} + P_0 C_0$$

$$C_2 = G_{11} + P_1 C_1$$

$$= G_{11} + P_1 (G_{10} + P_0 C_0)$$

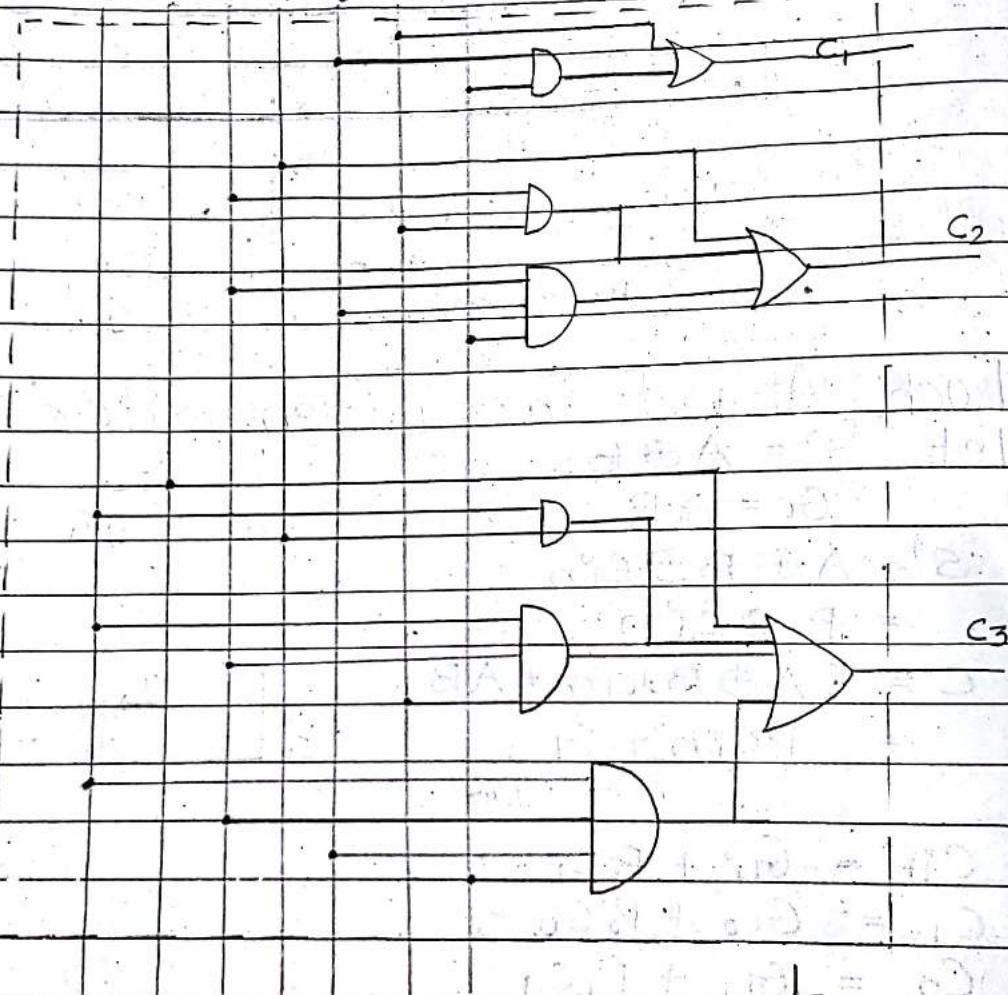
$$= G_{11} + P_1 G_{10} + P_1 P_0 C_0$$

$$C_3 = G_{12} + P_2 C_2$$

$$= G_{12} + P_2 G_{11} + P_2 P_1 G_{10} + P_2 P_1 P_0 C_0$$

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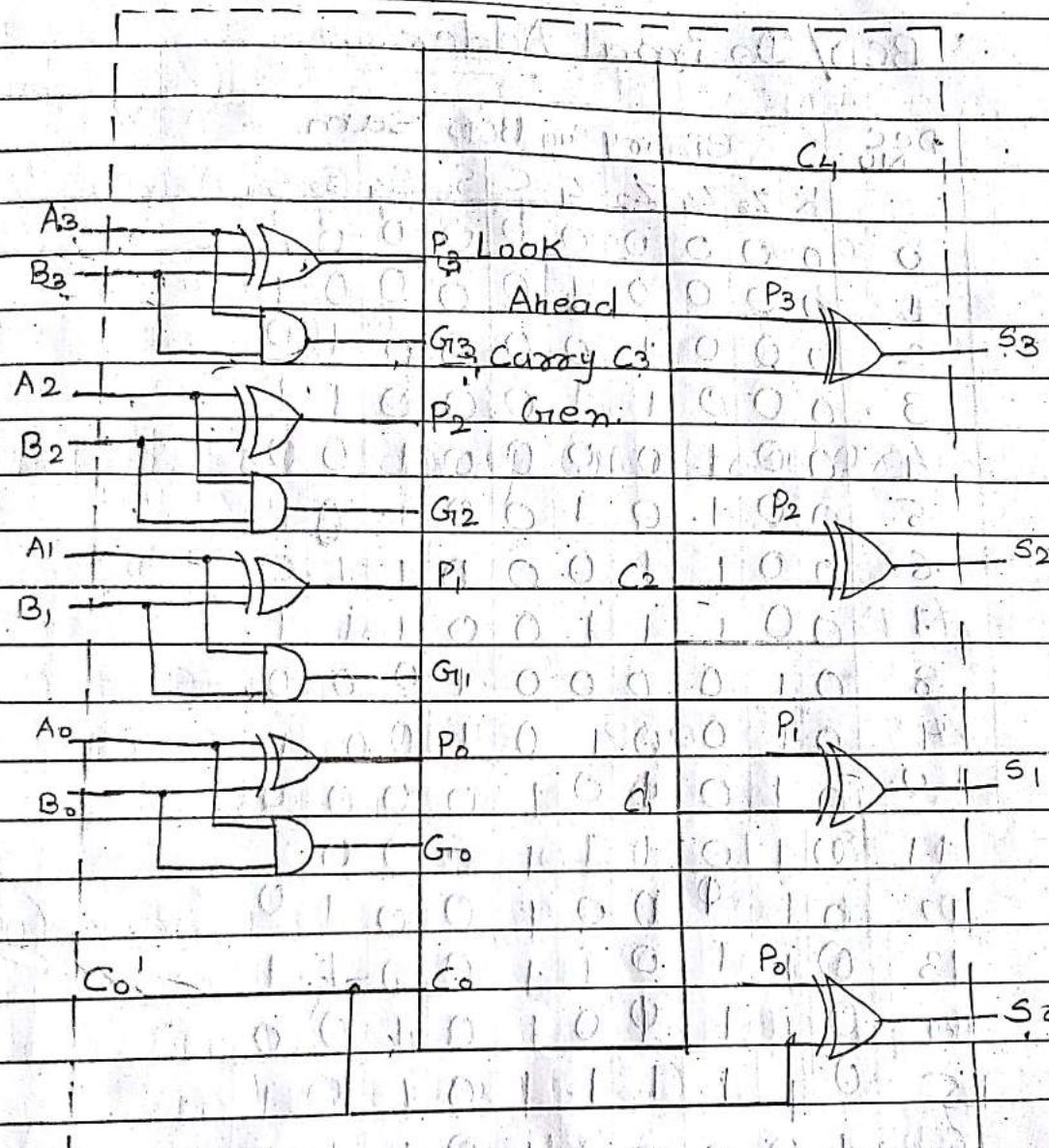
$P_2 \ G_2 \ P_1 \ G_1 \ P_0 \ G_0 \ C_0$



Carry Look

$m = (3)^2$

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MON TUE WED THU FRI SAT



Carry Look ahead adder

Date: _____
 MON TUE WED THU FRI SAT

B3
G0

BCD/ Decimal Adder

DEC NO	Binary Sum	BCD Sum	A ₄ A ₃ A ₂ A ₁
0	K Z ₈ Z ₄ Z ₂ Z ₁ C S ₈ S ₄ S ₂ S ₁ , A ₂ A ₁ A ₀	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0
1	0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 1	0 0 1	0 0 0 0 0
2	0 0 0 1 0 0 0 0 0 0 1 0 0 0 0 1	0 1 0	0 0 0 1 0
3	0 0 0 1 1 0 0 0 0 0 1 1 0 0 0 1	0 1 1	
4	0 0 1 0 0 0 0 0 1 0 0 0 0 0 0 0	1 0 0	
5	0 0 1 0 1 0 0 0 1 0 1 0 0 0 0 1	1 0 1	
6	0 0 1 1 0 0 0 1 1 0 1 1 0 0 0 0	1 1 0	
7	0 0 1 1 1 0 0 0 1 1 1 1 1 0 0 0	1 1 1	1 1 0 0 0
8	0 1 0 0 0 0 1 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	
9	0 1 0 0 0 1 0 1 0 0 0 1 0 0 0 1	0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1	69
10	0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0		
11	0 1 0 0 1 1 1 0 0 0 0 0 0 0 0 1		32168421
12	0 1 0 0 1 0 0 1 0 0 1 0		1 1 0 0 0 1
13	0 1 1 0 1 1 0 0 1 0 0 1 1		
14	0 1 1 0 0 1 0 1 0 1 0 0		
15	0 1 1 1 1 0 1 0 1 0 1		1 0 0 1
16	1 0 0 0 0 0 1 0 1 1 0		1 0 0 0 1 0
17	1 0 0 0 0 1 1 0 1 1 1		1 0
18	1 0 0 1 0 1 1 0 0 0		
19	1 0 0 1 1 1 1 0 0 1		A ₄ A ₃ A ₂ A ₁

10011	1001	0010	9	1001
+ 0001	A ₄ A ₃ A ₂ A ₁	B ₄ B ₃ B ₂ B ₁	+ 2	+ B ₄ B ₃ B ₂ B ₁
				+ 0010
10100	4-B ₄ B ₃ B ₂ B ₁	C		+ Z ₈ Z ₄ Z ₂ Z ₁
+ 0110	- K			0110
11010	Z ₈ Z ₄ Z ₂ Z ₁			10001
		1011		

$$\begin{array}{r}
 B3 \\
 + 60 \\
 \hline
 A C \\
 + 66 \\
 \hline
 59 \rightarrow BCD \\
 + 32 \rightarrow 7 \\
 \hline
 9B H \\
 \times \quad + 0G H
 \end{array}$$

0 → 9 + 6
 A, B, C, D IFF, To
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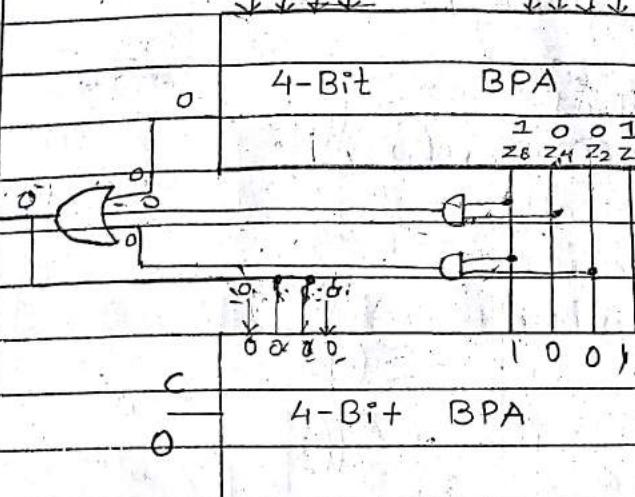
$$C = K + Z_8 Z_4 + Z_8 Z_2$$

1001 0010

$$\begin{array}{r}
 1000 \ 1011 \\
 + 0000 \ 0110 \\
 \hline
 \end{array}$$

↓↓↓ ↓↓↓

BCD



$$(32)_9$$

decompose

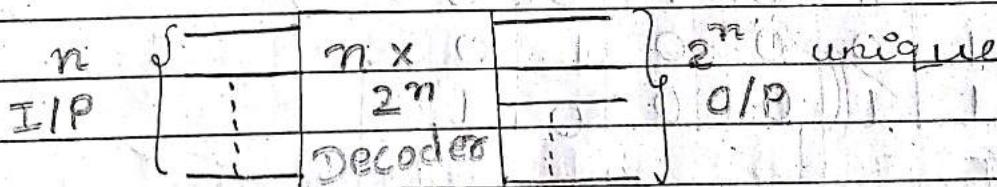
$$\begin{array}{r}
 9 \cdot 9 \\
 - 32 \\
 \hline
 (617) \underline{95}
 \end{array}$$

$$\begin{array}{r}
 \downarrow \downarrow \downarrow \\
 S_6 \ S_4 \ S_2 \ S_1 \\
 1 \ 0 \ 0 \ 1
 \end{array}
 \qquad
 \begin{array}{r}
 910 \quad 911 \\
 - 101 \quad - 100 \\
 \hline
 101 \quad 100
 \end{array}$$

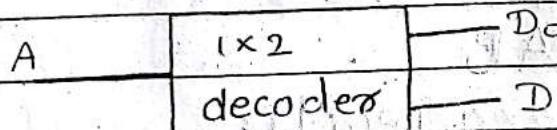
Decoder

combinational CKT.

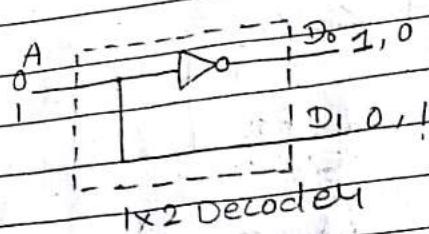
$m=2$



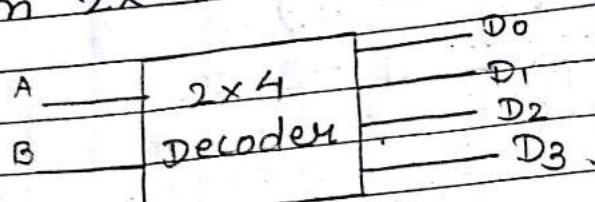
e.g.-1 1×2 Decoder



I/P	O/P	$D_0 = A'$
A	$D_0 \ D_1$	$D_1 = A$
0	1 0	
1	0 1	



Design 2×4 Decoder



T.T

I/P		O/P			
A	B	D ₀	D ₁	D ₂	D ₃
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

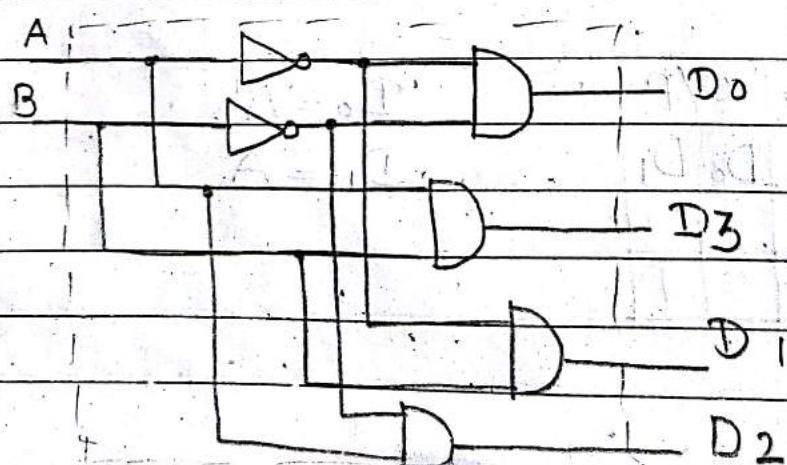
$$D_0 = AB = A'B'$$

$$D_1 = A'B = A'B$$

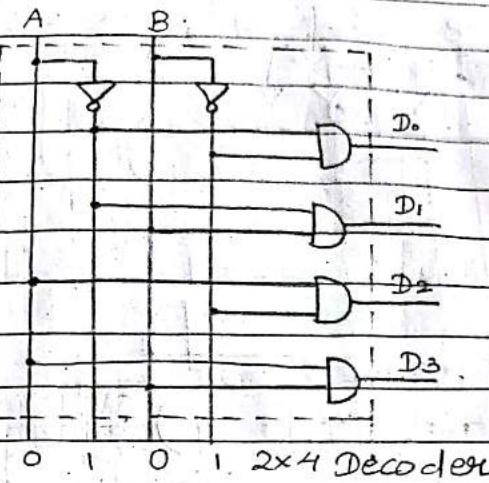
$$D_2 = AB = AB$$

$$D_3 = A'B = AB$$

2×4 Decoder



Date.: _____
 MON TUE WED THU FRI SAT



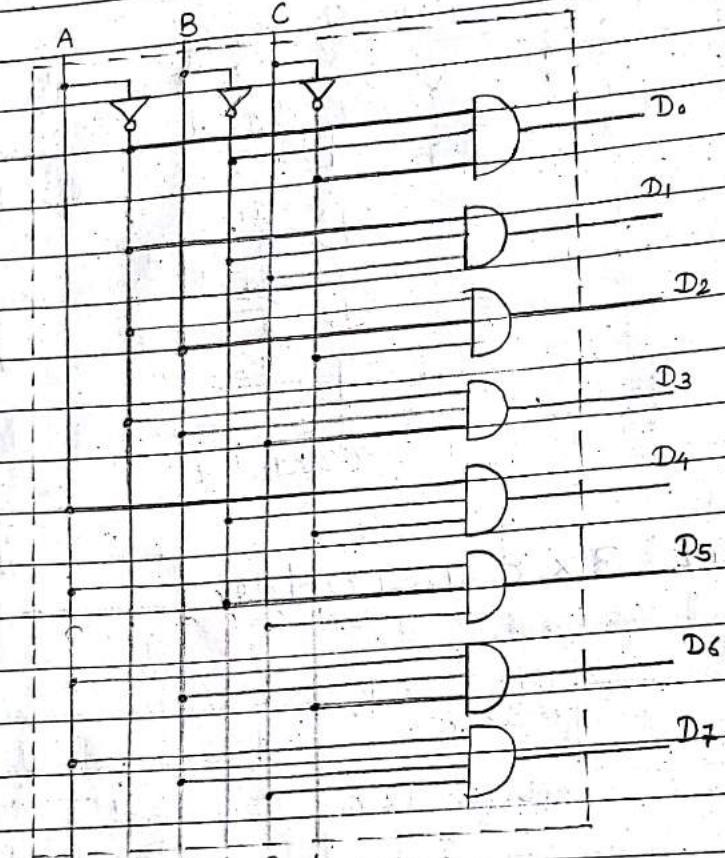
Design 3x8 Decoder

A		D ₀
B	3x8 Decoder	D ₁
C		D ₂
		D ₃
		D ₄
		D ₅
		D ₆
		D ₇

T.T

I/P			O/P								
A	B	C	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	
0	0	0	1	0	0	0	0	0	0	0	D ₀ = A'B'C'
0	0	1	0	1	0	0	0	0	0	0	D ₁ = A'B'C
0	1	0	0	0	1	0	0	0	0	0	D ₂ = A'B'C'
0	1	1	0	0	0	1	0	0	0	0	D ₃ = A'B'C
1	0	0	0	0	0	0	1	0	0	0	D ₄ = AB'C'
1	0	1	0	0	0	0	0	1	0	0	D ₅ = AB'C
1	1	0	0	0	0	0	0	1	0	0	D ₆ = ABC'
1	1	1	0	0	0	0	0	0	1	0	D ₇ = ABC

Date: _____
 MON TUE WED THU FRI SAT



3x8 Decoder

Implement foll. boolean funⁿ using
Decoder & OR Gate

1) $f(a, b, c) = \sum m(1, 3, 5, 7)$

~~a b c~~ 0 0 0 1 1 1 0 0 0 0 0 1 0 0 1 0

~~0 1 2 3 4 5 6 7~~ = ~~c~~ 0 1 0 1 0 0 0

~~0 1 2 3 4 5 6 7~~ = ~~b~~ 0 0 0 1 0 0 0 1 0

~~0 1 2 3 4 5 6 7~~ = ~~a~~ 0 0 1 0 0 0 0 1 0

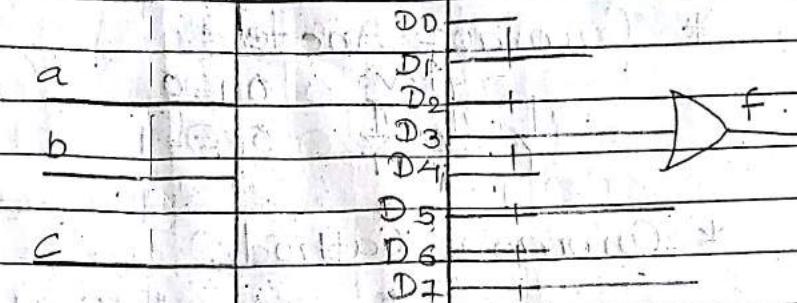
~~0 1 2 3 4 5 6 7~~ = ~~f~~ 1 0 1 0 0 0 0 1 1

~~0 1 2 3 4 5 6 7~~ = ~~f~~ 1 0 0 1 0 0 0 1 1

Date: _____
 MON TUE WED THU FRI SAT

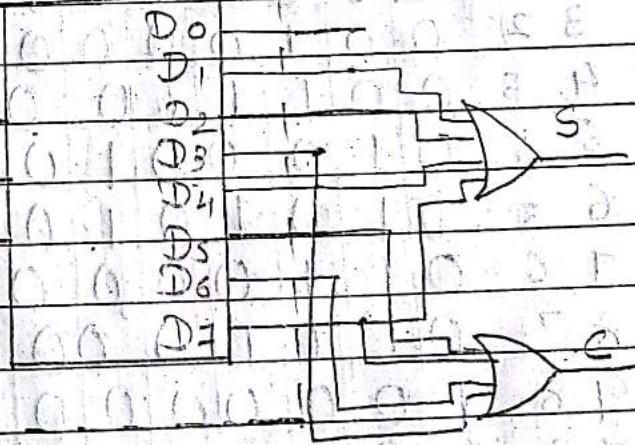
I/P O/P

a	b	c	y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0



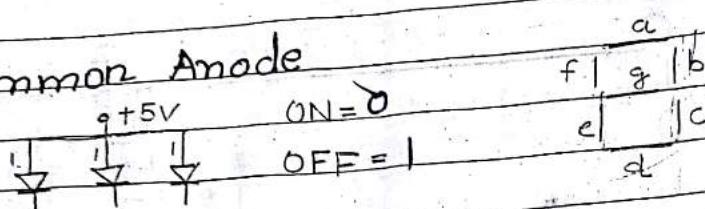
Implement full adder using decoders
& two OR Gates

a	b	c	s	c'
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	0	0

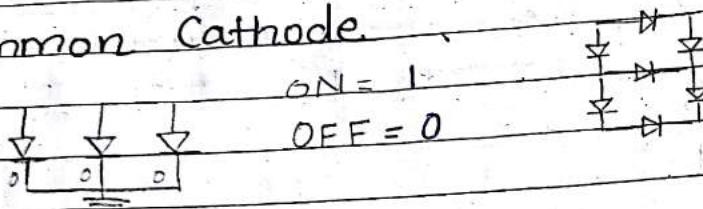


BCD to 7-Segment Decoder

* Common Anode



* Common Cathode



	B ₃	B ₂	B ₁	B ₀	a	b	c	d	e	f	g
0	0	0	0	0	0	0	0	0	0	0	1
1	0	0	0	1	1	0	0	1	0	0	0
2	0	0	1	0	0	1	0	0	1	0	0
3	0	1	0	0	0	0	0	1	1	0	0
4	0	0	1	1	1	0	0	1	0	0	0
5	0	1	0	0	1	0	0	1	0	0	0
6	0	1	0	1	0	1	0	0	0	0	0
7	0	1	1	0	0	0	0	0	0	0	1
8	1	0	0	0	0	0	0	0	1	0	0
9	1	0	0	0	0	0	0	0	1	0	0
10	1	0	0	1	1	0	0	1	1	1	1

$$a = 1+4$$

$$b = 5+6$$

$$c = 2$$

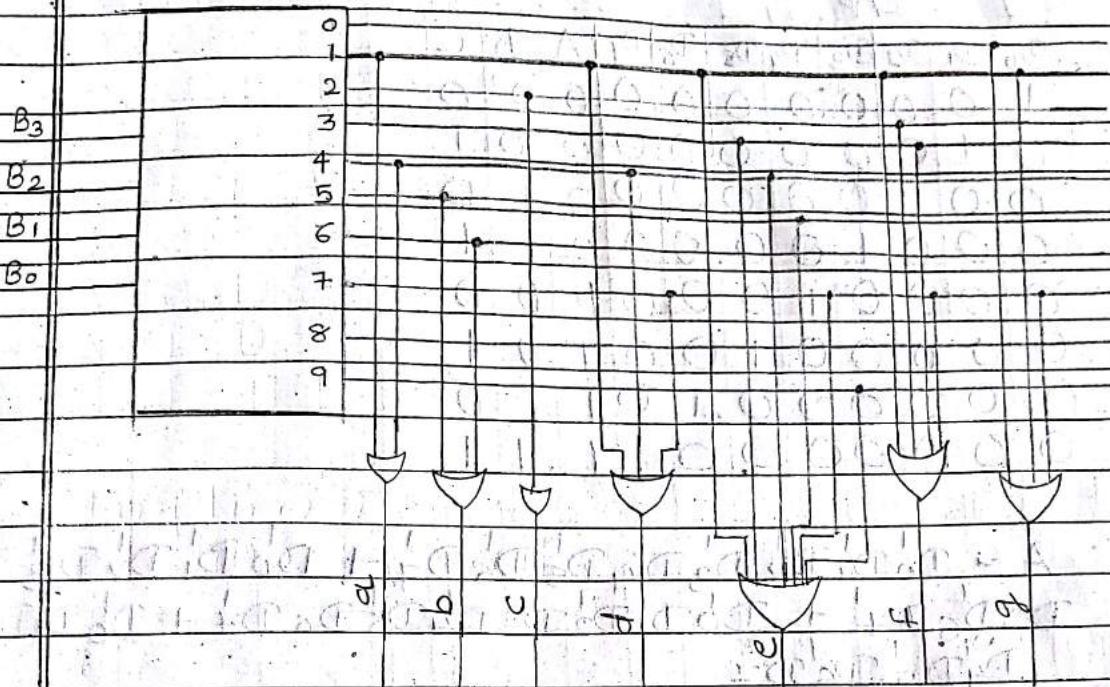
$$d = 1+4+7$$

$$e = 1+3+4+5+7+9$$

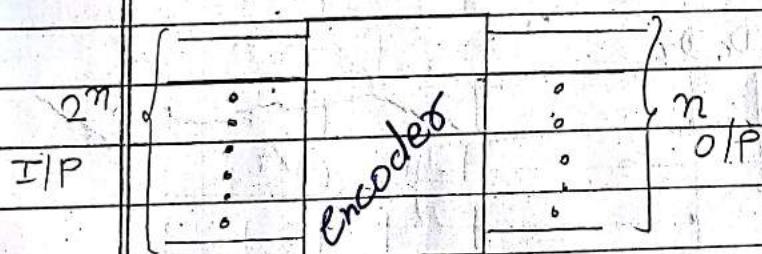
$$f = 1+2+3+7$$

$$g = 0+1+7$$

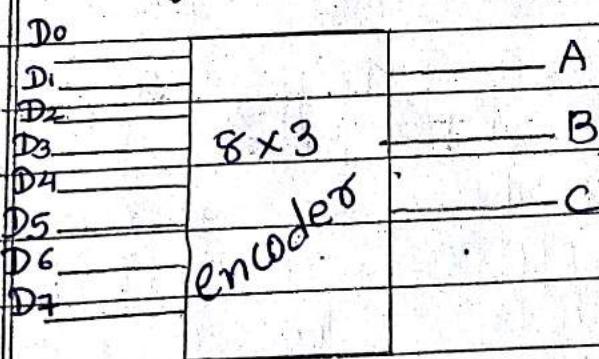
Date: _____
 MON TUE WED THU FRI SAT



Digital Encoders



Design 8x3 encoder (Octal to Binary)



Date.:
 MON TUE WED THU FRI SAT

I/P							O/P			
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	A	B	C
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	1	
0	0	1	0	0	0	0	0	1	0	
0	0	0	1	0	0	0	0	1	1	
0	0	0	0	1	0	0	1	0	0	
0	0	0	0	0	1	0	0	1	0	
0	0	0	0	0	0	1	0	1	0	
0	0	0	0	0	0	0	1	1	1	

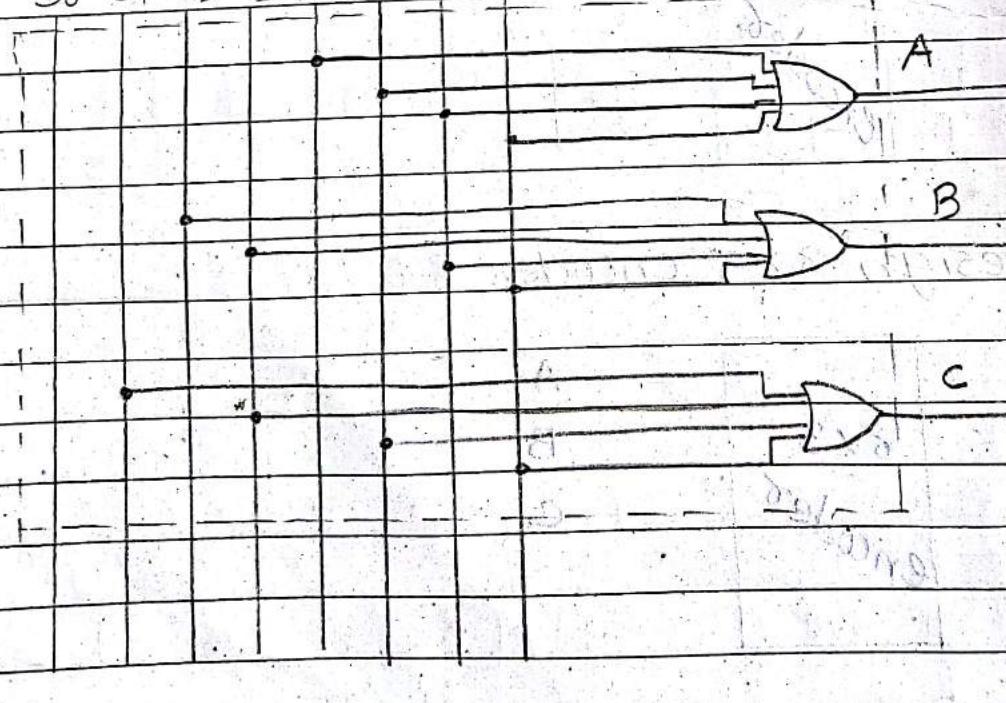
$$A = D_0' D_1' D_2' D_3' D_4' D_5' D_6' D_7' + D_0' D_1' D_2' D_3' D_4' \\ D_5' D_6' D_7' + D_6 D_1' D_2' D_3' D_4' D_5' D_6' D_7' + D_0 D_1' D_2' D_3' \\ D_4' D_5' D_6' D_7'$$

$$A = D_4 + D_5 + D_6 + D_7$$

$$B = D_2 + D_3 + D_6 + D_7$$

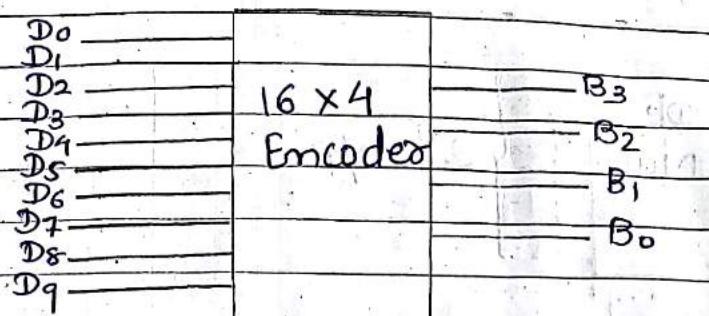
$$C = D_1 + D_3 + D_5 + D_7$$

$D_0 \ D_1 \ D_2 \ D_3 \ D_4 \ D_5 \ D_6 \ D_7$

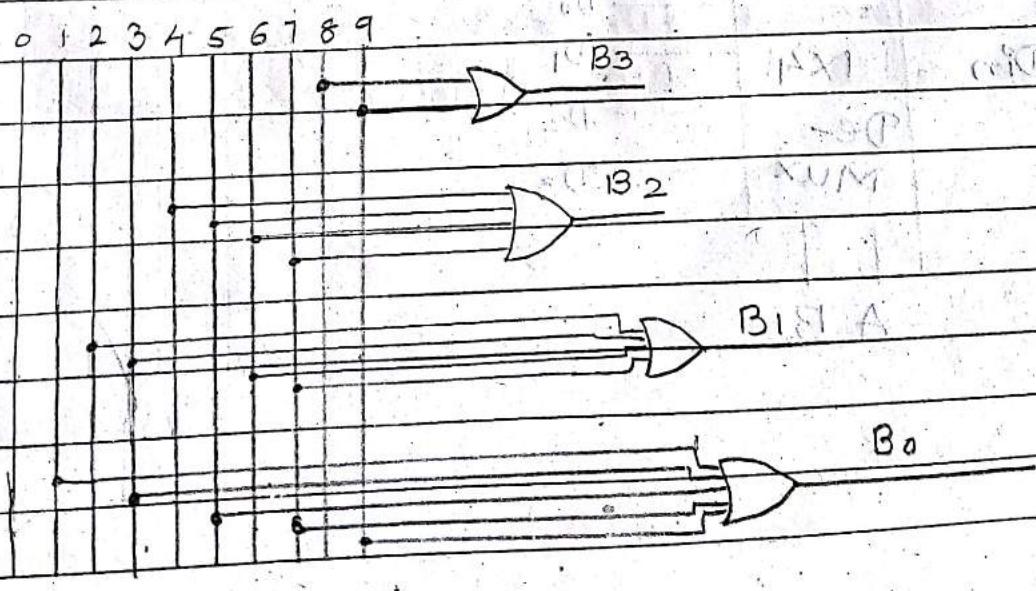


Date.: _____
 MON TUE WED THU FRI SAT

Design Decimal to BCD Encoder

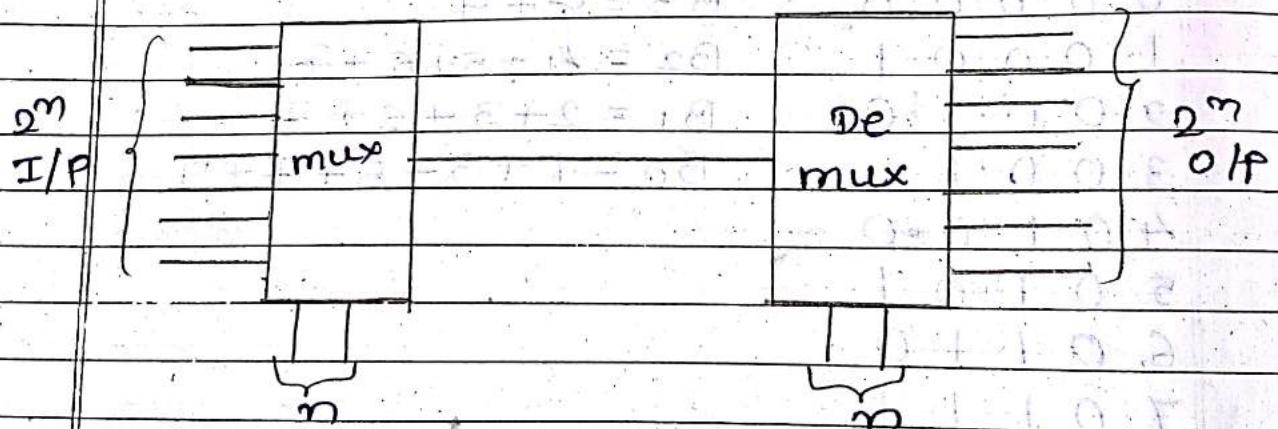
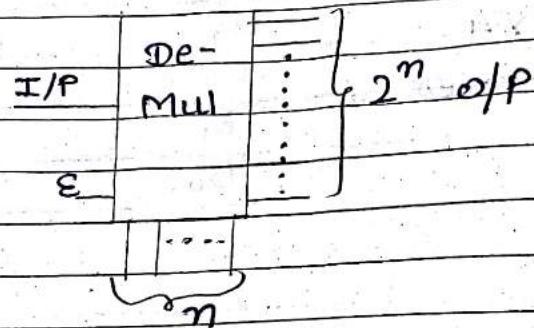


I/P	O/P			
Dec no	B ₃	B ₂	B ₁	B ₀
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

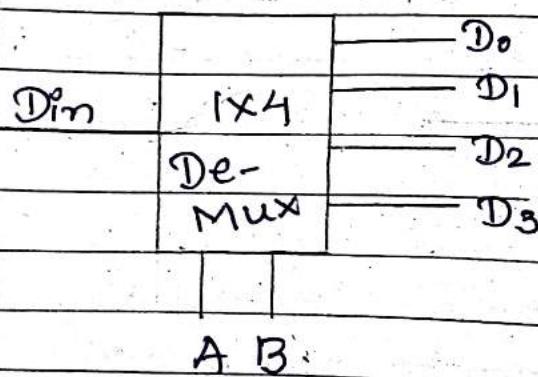


Date.: _____
 MON TUE WED THU FRI SAT

De-Multiplexer



* 1x4 Demux



Date.: MON TUE WED THU FRI SAT

T-T

I/P O/P

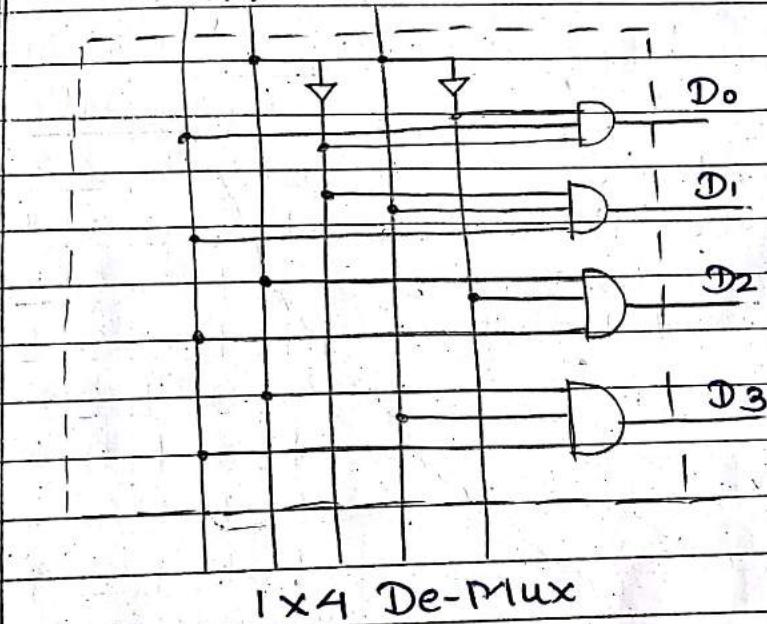
A	B	D ₀	D ₁	D ₂	D ₃
0	0	D _{in}	0	0	0
0	1	0	D _{in}	0	0
1	0	0	0	D _{in}	0
1	1	0	0	0	D _{in}

D_{in} Mux

D_{in} Mux

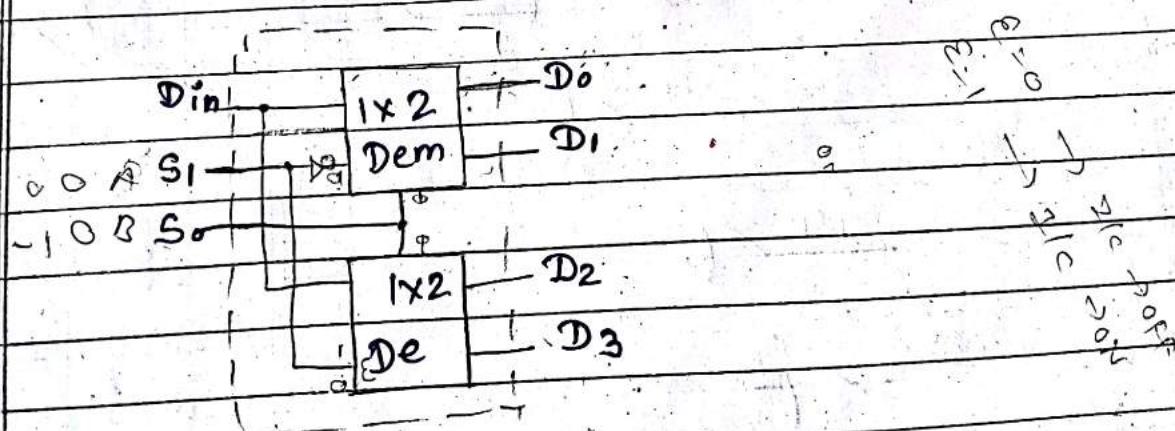
Ckt

D_{in} A B



1x4 De-Mux

Implement / Design 1x4 Demux using
Two 1x2 Demux.



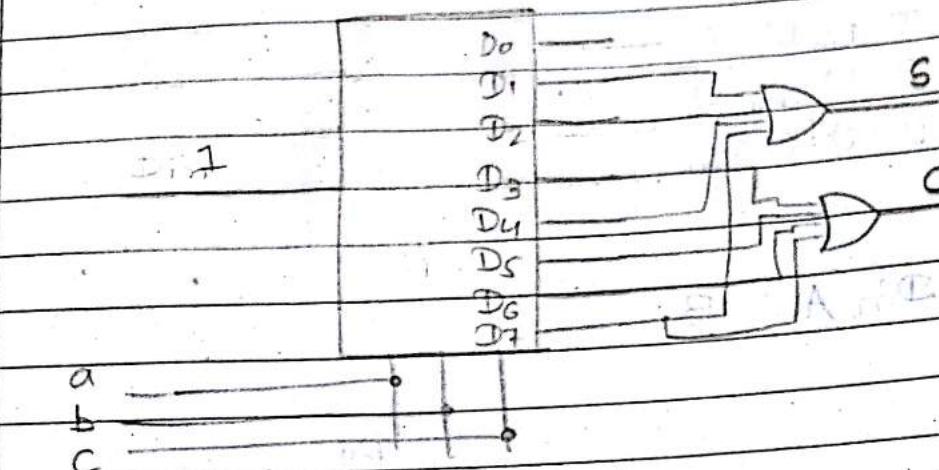
S & C

2
 $n = 1$

Date: _____

MON	TUE	WED	THU	FRI	SAT
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Design Full Adder using De-Mux



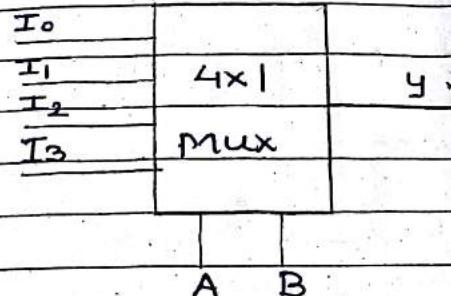
T.T

A	B	C_{in}	S	C
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	1	0
1	0	0	1	0
1	0	1	0	1
1	1	0	1	1
1	1	1	1	1

Date: _____
 MON TUE WED THU FRI SAT

Multiplexers:

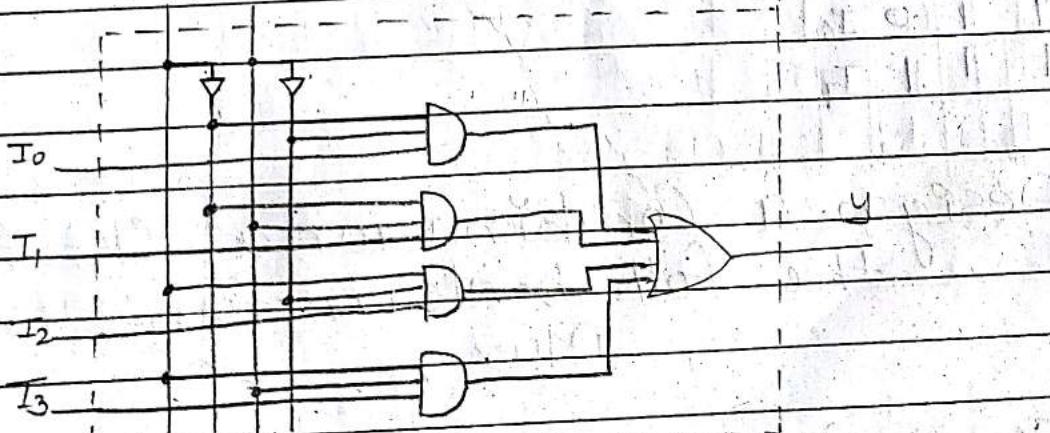
* Design 4x1 Mux:



T.T

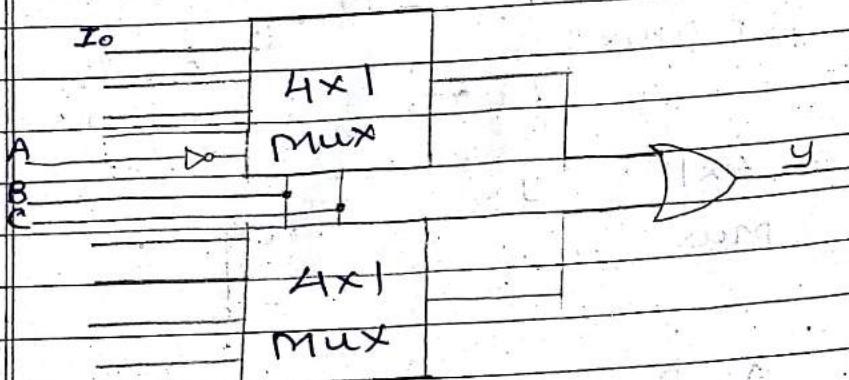
I/P	O/P
A	B
0	I_0
0	I_1
1	I_2
1	I_3

0 0
A B



Date: _____
 MON TUE WED THU FRI SAT

Design 8x1 Mux



T.T

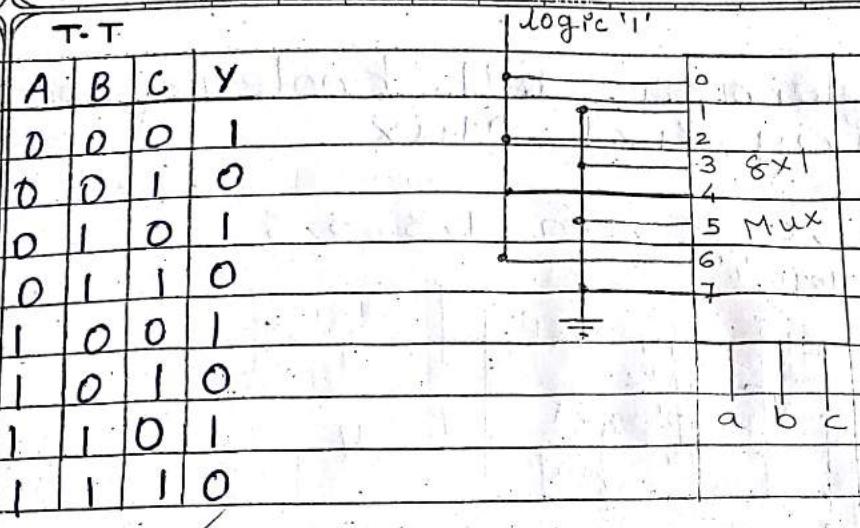
A	B	C	D	
0	0	0	I ₀	
0	0	1	I ₁	
0	1	0	I ₂	
0	1	1	I ₃	
1	0	0	I ₄	
1	0	1	I ₅	
1	1	0	I ₆	
1	1	1	I ₇	

Design a Combinational Ckt for
the foll. boolean fun'ns using
Mux,

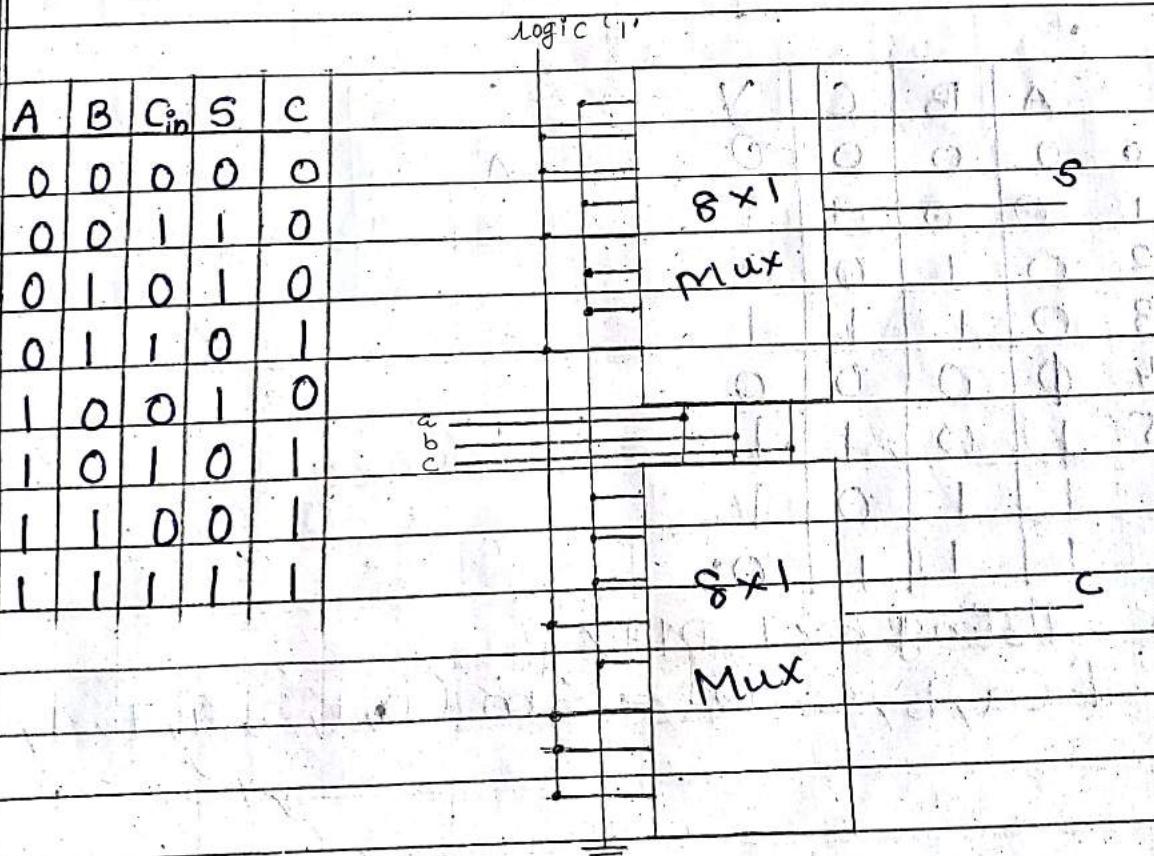
1. $f(a, b, c) = \sum m(0, 2, 4, 6)$

S.S Magnitude
Comparator

Date: _____
 MON TUE WED THU FRI SAT



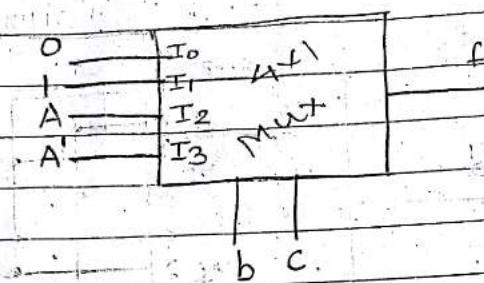
Design Full Adder using Mux.



Date.: MON TUE WED THU FRI SAT

Implement foll. boolean Fun
using 4x1 Mux.

$$F(a, b, c) = \sum m(1, 3, 5, 6)$$



	A	B	C	y		I ₀	I ₁	I ₂	I ₃
0	0	0	0	0	A'	0	1	2	3
1	0	0	1	1	A	4	5	6	7
2	0	1	0	0		0	1	a	a
3	0	1	1	1					
4	1	0	0	0				1	0
5	1	0	1	1		0		6	
6	1	1	0	1		a	0	1	0
7	1	1	1	0				1	1

⇒ Using 8x1 Mux

$$f(a, b, c, d) = \sum m(0, 1, 3, 4, 7, 9, 15)$$

$\Sigma m(2, 4, 6)$

$$2^n = 8$$

$m=3$

Date: _____
 MON TUE WED THU FRI SAT

	A	B	C	D	F
0	0	0	0	0	1
1	0	0	0	1	1
2	0	0	1	0	0
3	0	0	1	1	1
4	0	1	0	0	1
5	0	1	0	1	0
6	0	1	1	0	0
7	0	1	1	1	1
8	1	0	0	0	0
9	1	0	0	1	1
10	1	0	1	0	0
11	1	0	1	1	0
12	1	1	0	0	0
13	1	1	0	1	0
14	1	1	1	0	0
15	1	1	1	1	1

A'	I ₀							
I	I ₁							
O	O ₂							
A'	I ₃							
A'	I ₄	8x1						
O	O ₅							
O	O ₆							
1	I ₇							
b	c	d						
I ₀	I ₁	I ₂	I ₃	I ₄	I ₅	I ₆	I ₇	
A'	⑥	①	2	③	④	5	6	⑦
A	7	5	10	17	12	13	14	15
A'	1	0	A'	A'	0	0	1	

$$f(a, b, c) = \sum m(0, 1, 3, 5, 7)$$

$$= \Sigma m(2, 4, 6)$$

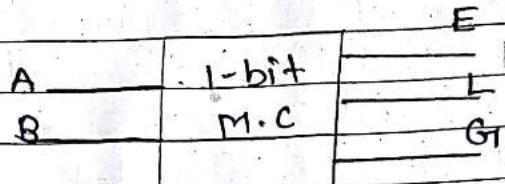
	A	B	C	F
0	0	0	0	0
1	0	0	1	0
2	0	1	0	1
3	0	1	1	0
4	1	0	0	1
5	1	0	1	0
6	1	1	0	1
7	1	1	1	0

b. c.

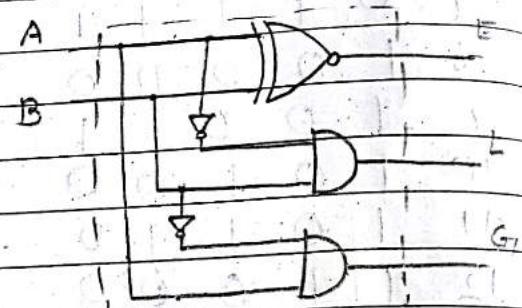
Date: _____
 MON TUE WED THU FRI SAT

Magnitude Comparator

* 1-bit



I/P		O/P		
A	B	E	L	G
0	0	1	0	0
0	1	0	1	0
1	0	0	0	1
1	1	1	0	0



$$E = A'B' + AB = A \oplus B$$

$$L = A'B$$

$$G = AB'$$

Design a Combinational CKT for d-bit

$$\text{let } A = A_1 A_0$$

$$B = B_1 B_0$$

Condⁿ

$$A = B \rightarrow A_1 = B_1 \text{ & } A_0 = B_0$$

$$E = (A_1 \oplus B_1)(A_0 \oplus B_0)$$

Date: _____
 MON TUE WED THU FRI SAT

$$A < B \rightarrow A_1 = 0 \& B_1 = 1 \quad 10 < 11$$

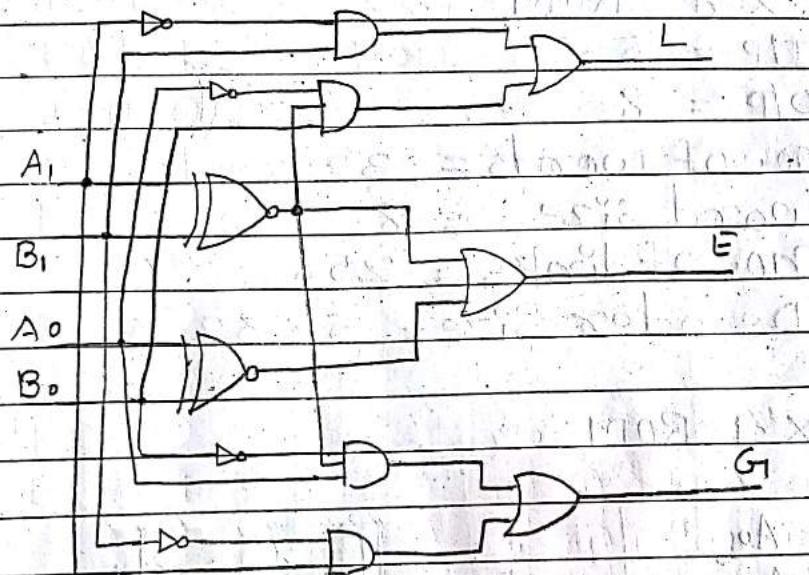
$$A_1 = B_1 \& A_0 = 0 \& B_0 = 1 \quad 00 < 01$$

$$L = A_1'B_1 + (A_1 \oplus B_1)A_0'B_0$$

$$A > B \rightarrow A_1 = 1 \& B_1 = 0$$

$$A_1 = B_1 \& A_0 = 1 \& B_0 = 0$$

$$G_I = A_1B_1 + (A_1 \oplus B_1)A_0B_0'$$



ROM

→ Decoder
→ OR

n I/P

$2^m \times m$

ROM

m O/P

Date.:
 MON TUE WED THU FRI SAT

* 32×4 ROM

$$I/P = 5$$

$$O/P = 4$$

$$\text{no. of words} = 32$$

$$\text{word size} = 4$$

$$\text{no. of links} = 128$$

$$\text{Decoder Size} = 5 \times 32$$

* 32×8 ROM

$$I/P = 5$$

$$O/P = 8$$

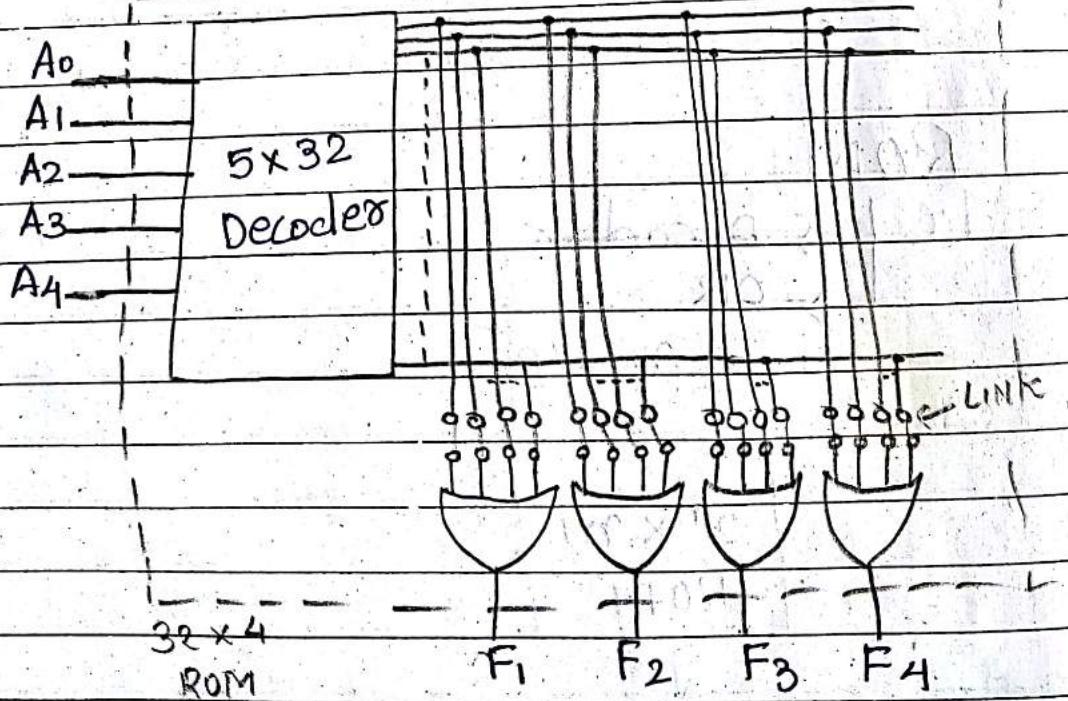
$$\text{no. of words} = 32$$

$$\text{word size} = 8$$

$$\text{no. of links} = 256$$

$$\text{Decoder Size} = 5 \times 32$$

* 32×4 ROM



Implement foll. boolean fun using rom (ROM):

$$1) F_1(A_1, A_0) = \Sigma(1, 2, 3)$$

$$2) F_2(A_1, A_0) = \Sigma(0, 2)$$

Sol^m:

$$I/P = 2 = n$$

$$O/P = 2 = m$$

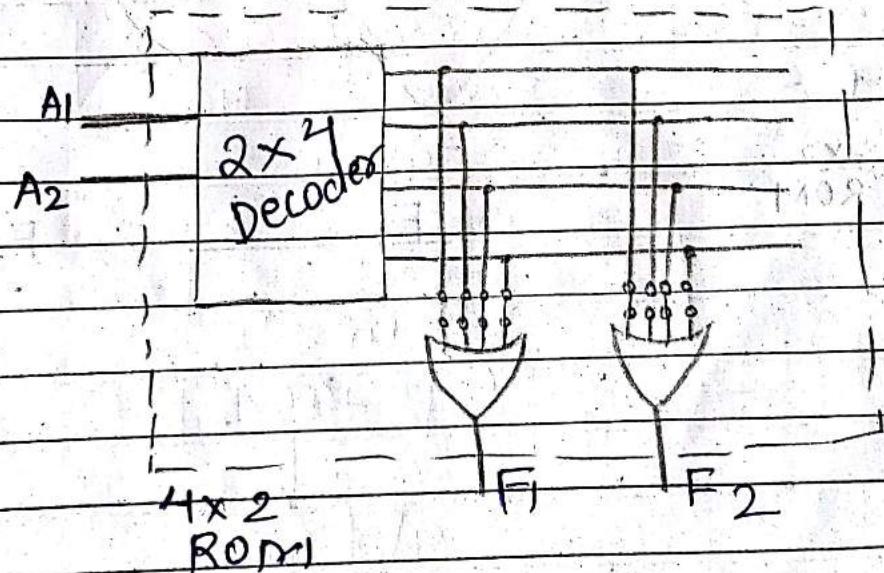
$$ROM = 2^n \times m = 2^2 \times 2 \\ = 4 \times 2$$

$$\text{Decoder} = 2 \times 4$$

$$OR = 2$$

$$\text{Links} = 8$$

	I/P		O/P	
	A ₁	A ₀	F ₁	F ₂
0	0	0	0	1
1	1	0	1	0
2	1	0	1	1
3	1	1	1	0



Date: _____
 MON TUE WED THU FRI SAT

Implement Full Adder,

1) $F_1(S) = \Sigma(1, 2, 4, 7)$
 2) $F_2(S) = \Sigma(3, 5, 6, 7)$

T/P = 3

O/P = 2

ROM = $2^3 \times m = 8 \times 2$

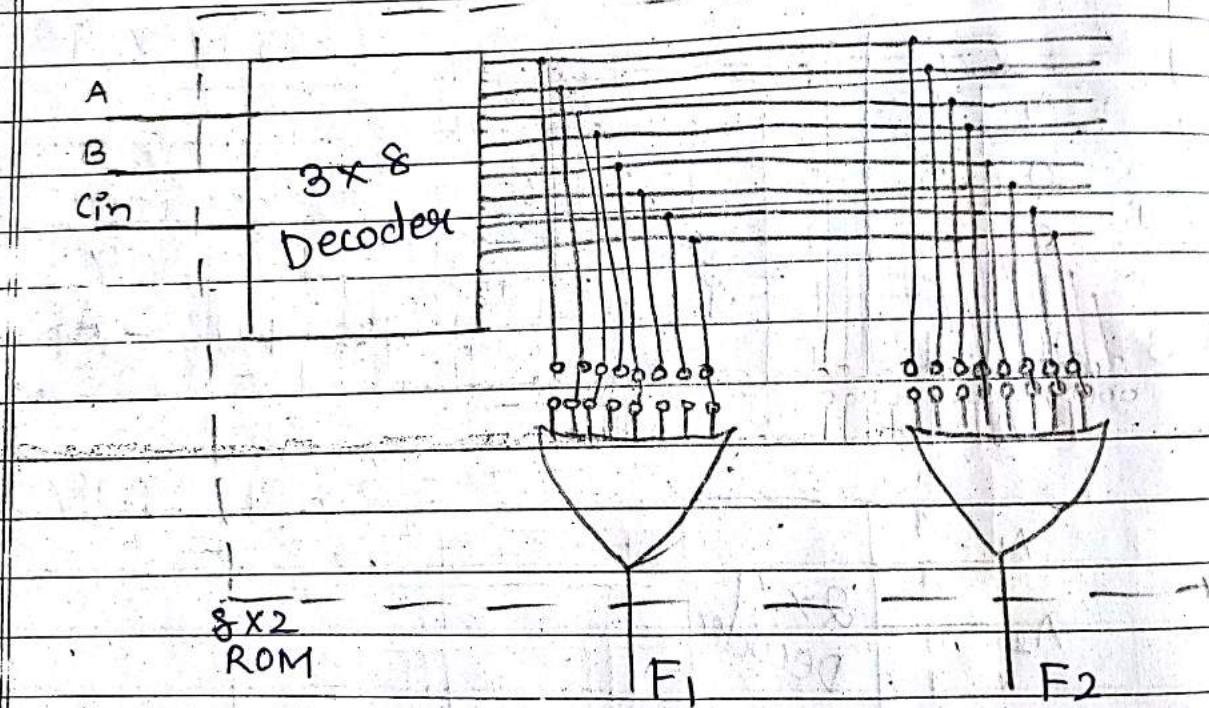
Decoder = 3×8

OR = 2

no. of link = 16

$n \times 2^m$

1)
 2)
 3)
 4)



Date: _____
 MON TUE WED THU FRI SAT

- 1) $F_1(A, B, C) = \Sigma m(0, 1, 4, 6)$
- 2) $F_2(A, B, C) = \Pi m(1, 2, 3, 4)$
- 3) $F_3(A, B, C) = \Pi m(0, 1, 6, 7)$
- 4) $F_4(A, B, C) = \Sigma m(2, 4, 5, 6)$

$$I/P = 3$$

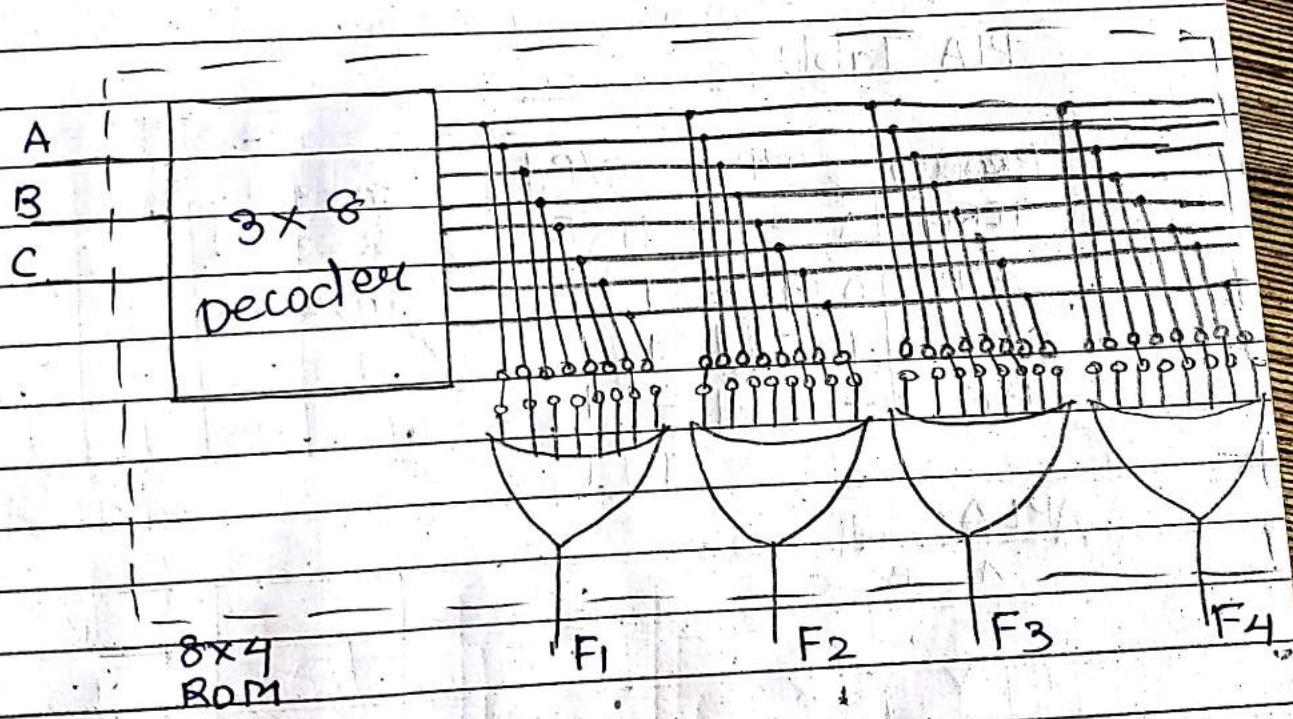
$$O/P = 4$$

$$ROM = 2^3 \times 4 = 8 \times 4$$

$$\text{Decoder} = 3 \times 8$$

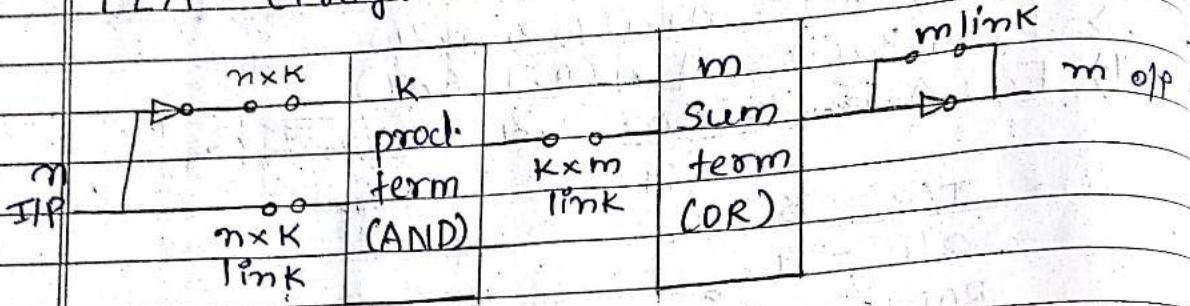
$$OR = 4$$

$$\text{No. of links} = 32$$



Date: _____
 MON TUE WED THU FRI SAT

PLA (Program)



Implement foll. boolean fun" using PLA

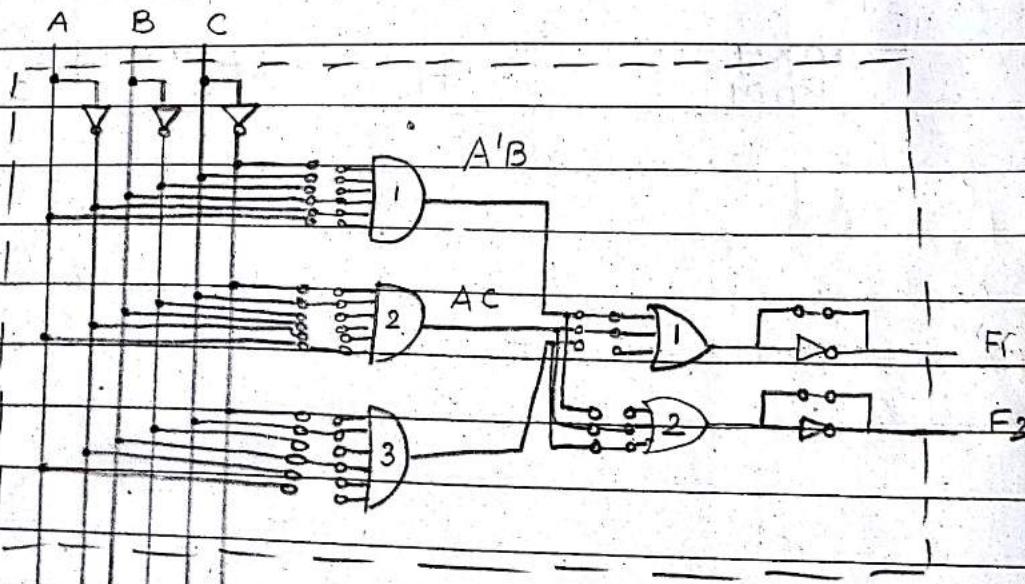
$$F_1 = A'B + AC$$

$$F_2 = ACT + BC$$

PLA Table

PRODUCT TERM	I/P A	I/P B	I/P C	O/P F_1	O/P F_2	$n=3$
TERM	A	B	C	F_1	F_2	$K=3$
$A'B$	0	1	-	1	-	$m=2$
AC	1	-	1	1		
BC	-	1	1	-	1	
				T	T	

PLA



Date: _____
 MON TUE WED THU FRI SAT

$$F_1(A, B, C) = \sum m(3, 5, 6, 7)$$

$$F_2(A, B, C) = \sum m(0, 2, 4, 7)$$

A	B	C	00	01	11	10
0	X ₀	.	1 ₃	X ₂		
1	X ₄	1 ₅	X ₇	1 ₆		

0	X ₁	X ₃	1 ₂
1	X ₄	X ₅	X ₆

$$\begin{aligned} F_1 &= BC + AC + AB \\ &= BC + A'C + AB \end{aligned}$$

$$\begin{aligned} F_2 &= B'C' + ABC + A'BC' \\ &= B'C' + B(A \oplus C) \\ &= B'C' + A'C' + ABC \end{aligned}$$

$$F_1' = B'C' + A'B' + A'C'$$

$$F_2' = B'C + A'C + ABC'$$

$$F_1 F_2 = 6$$

$$F_1' F_2' = 6$$

$$F_1' F_2 = 4$$

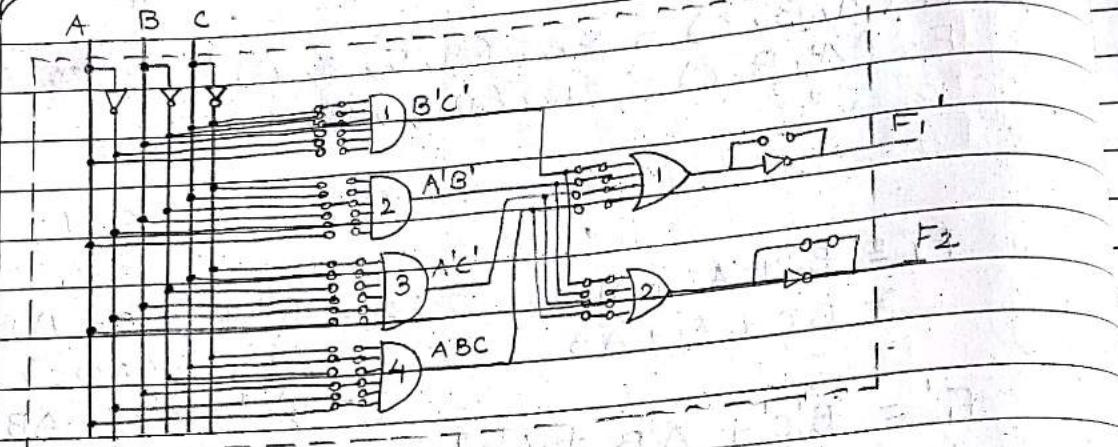
$$F_1 F_2' = 6$$

PLA Table

Product Term	I/P A	I/P B	I/P C	O/P F ₁ ' F ₂ '
B'C'	-	0	0	1 1
A'B'	0	0	-	1 -
A'C'	0	-	0	1 1
ABC	1	1	1	- 1
				C T

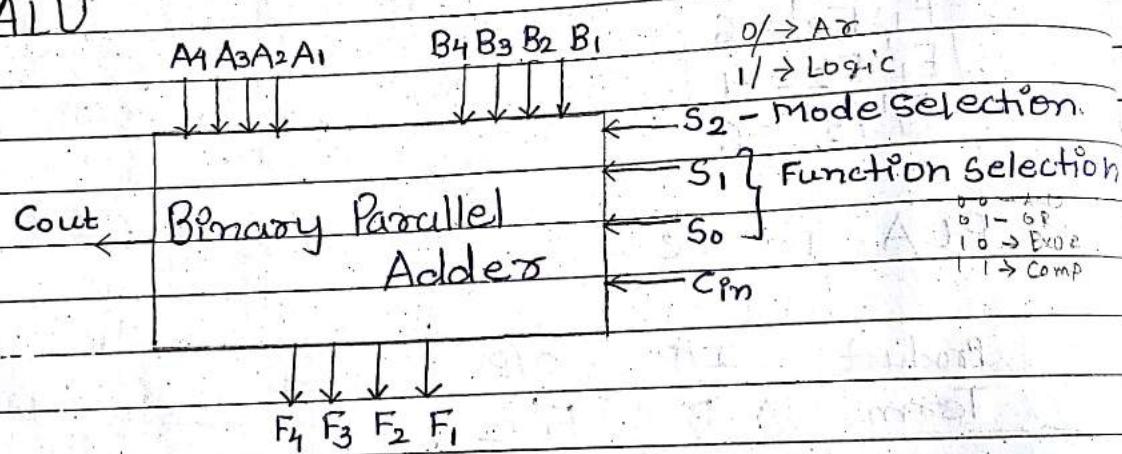
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Processor Logic Design



Chp Start

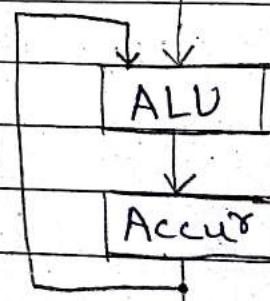
ALU



* Accumulator

Data I/P

Processor Reg
or
Memory unit



Data O/P

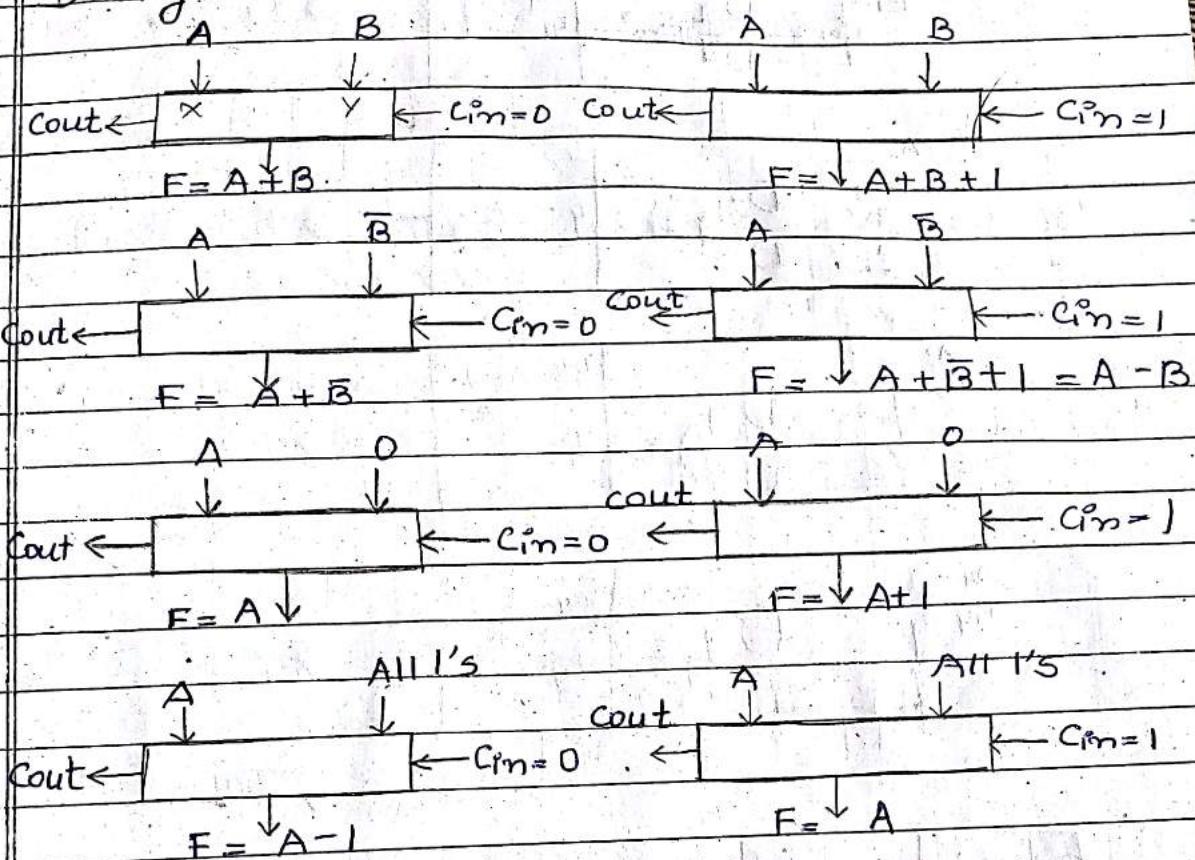
$op^n R_1 + R_2$

$t_1: A \leftarrow 0$

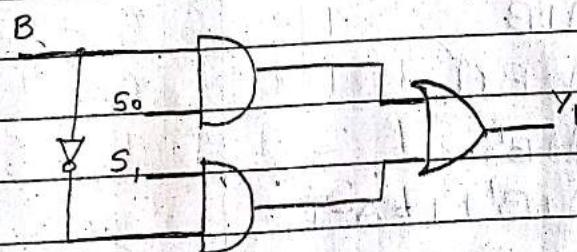
$t_2: A \leftarrow A + R_1$

$t_3: A \leftarrow A + R_2$

Design of Arith. Ckt.



Logic diagram of Arith. Ckt

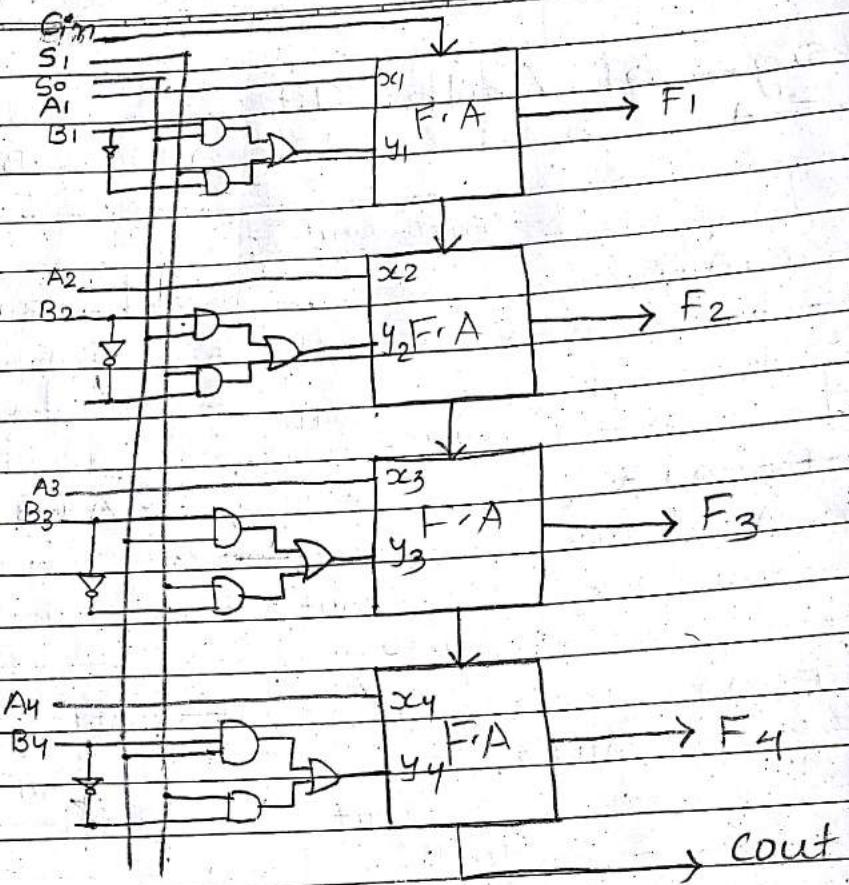


S_1	S_0	y_1
0	0	0
0	1	B
1	0	\bar{B}
1	1	1

$$x_i = A_i$$

$$y_i = B_i S_0 + \bar{B}_i S_1$$

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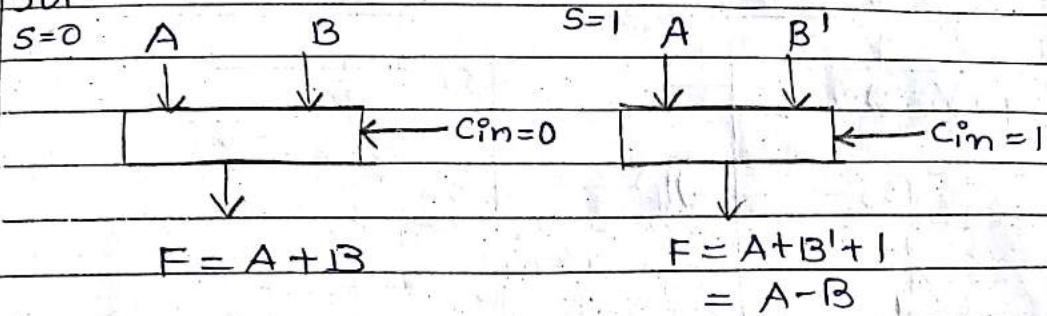
S_1	S_0	C_{in}	y	f
0	0	0	0	A
0	0	1	0	$A+1$
0	1	0	B	$A+B$
0	1	1	B	$A+B+1$
1	0	0	B'	$A+B'$
1	0	1	B'	$A+B'+1 = A-B$
1	1	0	$AII's$	$A-1$
1	1	1	$AII's$	A

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Design Adder/Subtractor using Selection Line

Condition : $S=0 \Rightarrow F=A+B$
 $S=1 \Rightarrow F=A-B$

Soln



S	X	Y	Cin
0	A	B	0
1	A	B'	1

S	A	B	X	Y
0	0	0	0	0
0	0	1	0	1
0	1	0	1	0
0	1	1	1	1
1	0	0	0	1
1	0	1	0	0
1	1	0	1	1
1	1	1	1	0

$$x = A$$

$$Cin = S$$

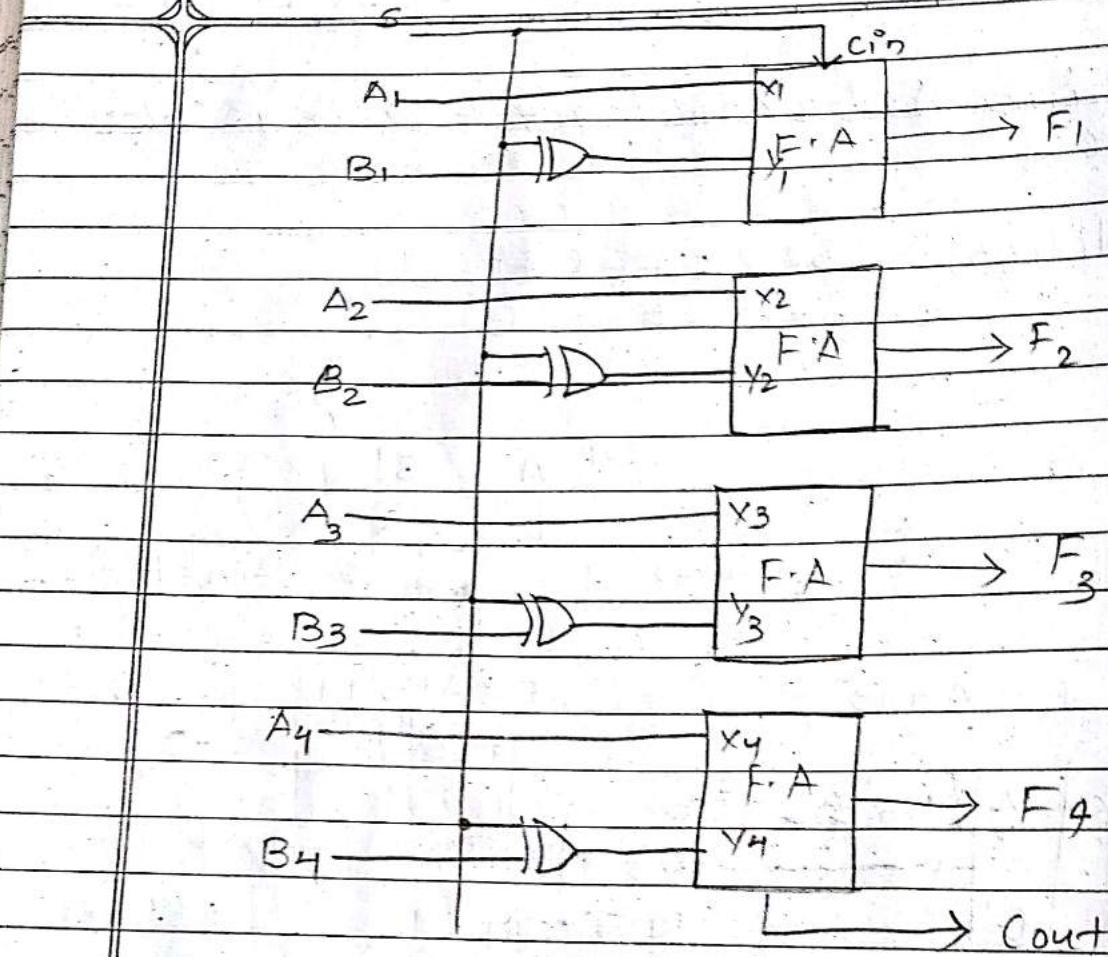
$$y = S'A'B + S'AB + SA'B' + SAB'$$

$$y = S'B(A' + A) + S'B'(A + A)$$

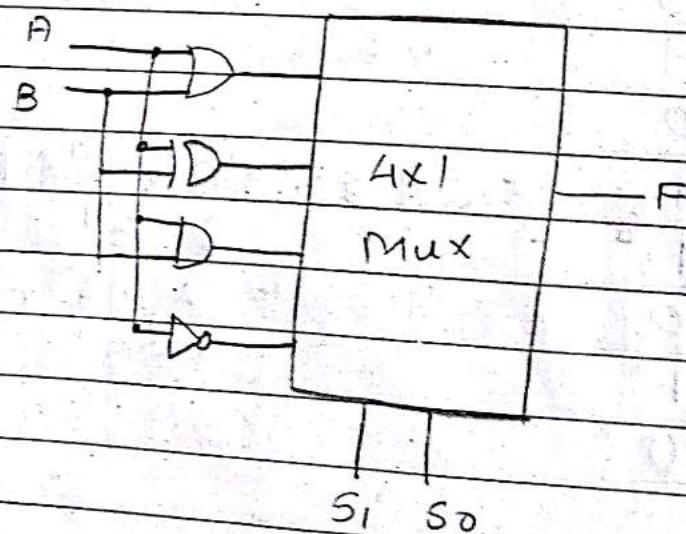
$$= S'B + S'B'$$

$$= S \oplus B$$

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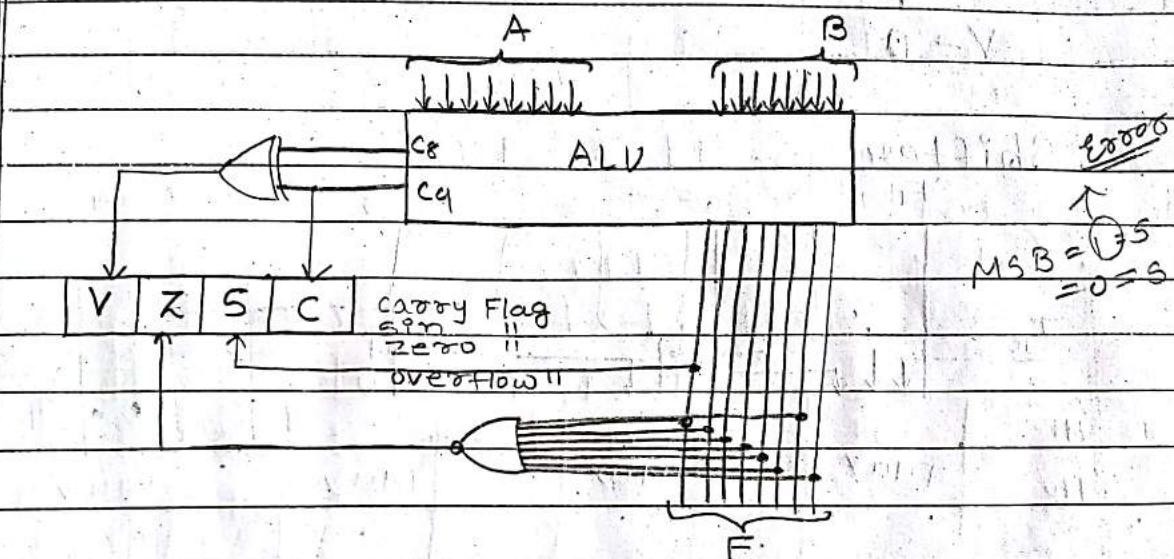
Logical Opⁿ



S.	S ₀	F	1	1	1	1	1	1	1	1
0	0	A+B	1	1	1	1	1	1	1	1
0	1	A⊕B	1	0	0	0	0	0	0	0
1	0	A·B	0	1	0	1	0	1	0	1
1	1	A'	1	0	1	0	1	0	1	0

0 → Posi
1 → Nega

Status Reg :-



eg:

$$A = \underline{11011010}$$

$$\beta = 11010010$$

	C₈ C₇ C₆ C₅ C₄ C₃ C₂ C₁
A	1 0 1 1 0 1 0
+ B	1 1 0 1 0 0 1 0
	1 1 0 1 0 1 1 0 0 → F

$$C = 1$$

$$S = 1$$

$$z=0$$

$$V = 0$$

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$C_8 C_7 C_6 C_5 C_4 C_3 C_2 C_1$

eg: $\begin{array}{cccccc} 1 & 1 & 1 & 1 & 1 & 1 \end{array}$

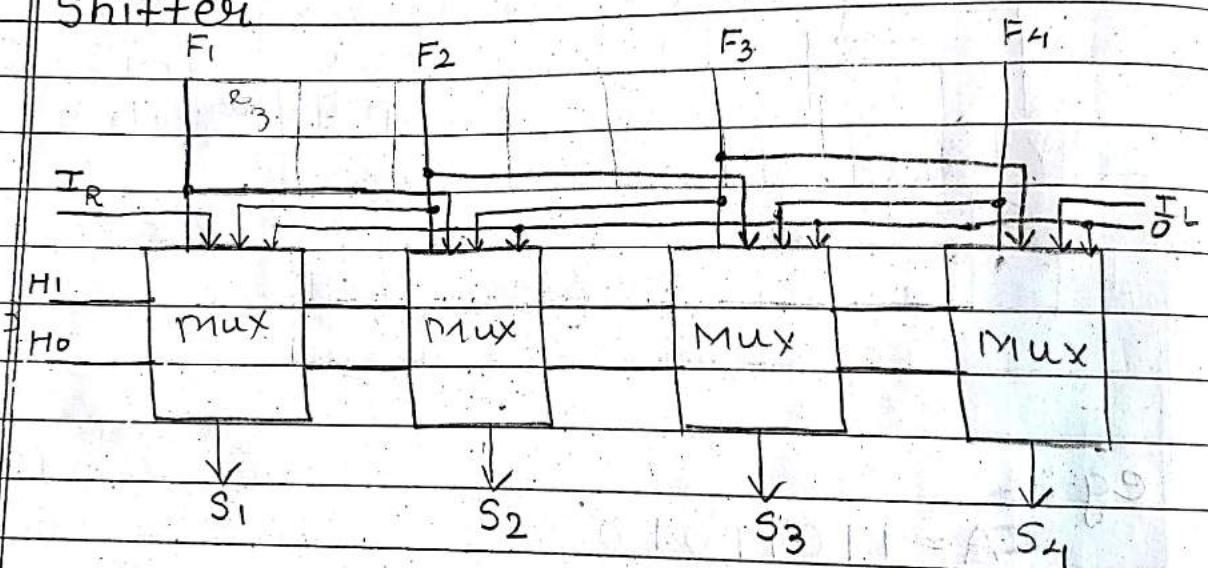
$A = \begin{array}{cccccc} 1 & 1 & 1 & 1 & 1 & 1 \end{array}$

$B = \begin{array}{cccccc} 0 & 0 & 0 & 0 & 0 & 1 \end{array}$

$c_9 \quad \begin{array}{cccccc} 1 & 0 & 0 & 0 & 0 & 0 \end{array}$

$C = 1$	\Rightarrow comparison purpose
$S = 0$	
$Z = 1$	\Rightarrow
$V = 0$	

Shifter



H ₁	H ₀	Function
----------------	----------------	----------

0	0	SFF
---	---	-----

0	1	S \leftarrow Shift right F (Shr F)
---	---	--------------------------------------

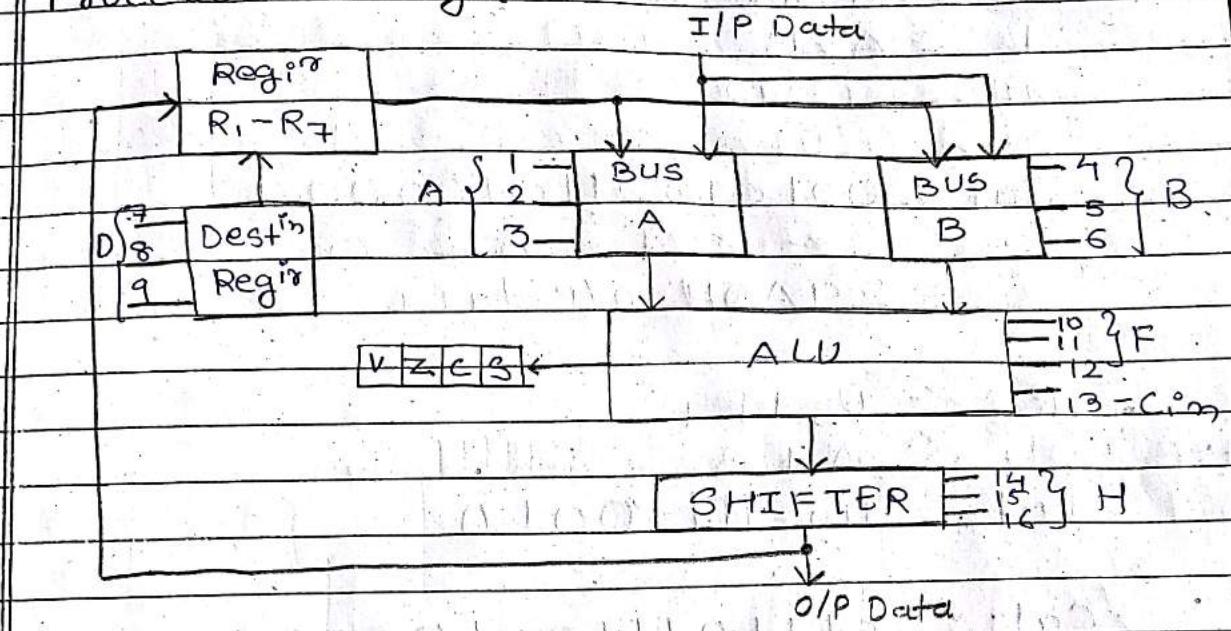
1	0	S \leftarrow ShL F
---	---	----------------------

1	1	S \leftarrow 0
---	---	------------------

~~I_R 1 0 0~~

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Processor Design



Control Word

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	B	D	F	G _{in}	H										
001	010	011	010	0	000										

Binary No	A	B	D	Op ₁ with Cin=0	Op ₂ with Cin=1	Op ₃
0 0 0	I/P data	I/P data	None	A	A+1	Transfer \leftarrow No shift
0 0 1	R ₁	R ₁	R ₁	A+B	A+B+1	Shift right
0 1 0	R ₂	R ₂	R ₂	A-B	A-B+1	Shift left
0 1 1	R ₃	R ₃	R ₃	A-1	A	Zero
1 0 0	R ₄	R ₄	R ₄	A AND B	-	-
1 0 1	R ₅	R ₅	R ₅	A XOR B	-	Circular right with carry
1 1 0	R ₆	R ₆	R ₆	A OR B	-	Circular left with carry
1 1 1	R ₇	R ₇	R ₇	A	-	-

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$$R_3 \leftarrow R_1 - R_2$$

$$D \leftarrow A - B$$

011 001 010

$$\text{Cal : } \begin{array}{r} 001010011010000 \\ \underline{2} \quad 9 \quad A \quad 0 \\ = 29A0H \text{ O/P data} \end{array}$$

$$R_5 \leftarrow R_6 + R_7$$

$$D \leftarrow A + B$$

101 110 111 0010

$$\text{Cal : } \begin{array}{r} 101110110010000 \\ 1101111010010000 \\ \underline{D} \quad \underline{E} \quad \underline{9} \quad \underline{0} \\ = 1DE90H \text{ D/P data} \end{array}$$

$$R_1 \leftarrow R_2 \text{ AND } R_3$$

$$D \leftarrow A - \text{AND } B$$

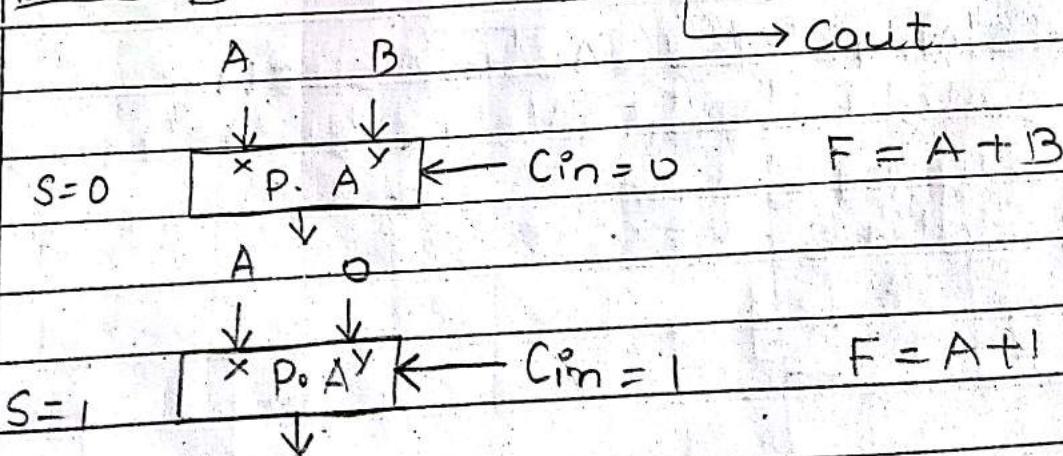
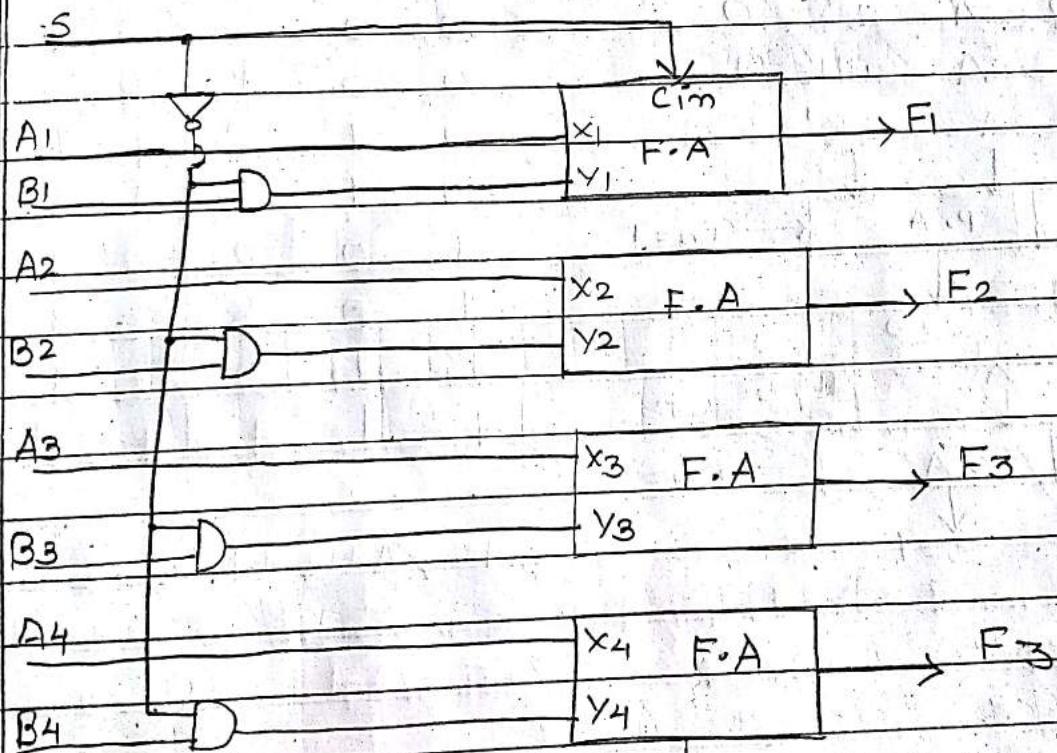
001 010 011

$$\text{Cal : } \begin{array}{r} 0100110011000000 \\ \underline{4} \quad \underline{C} \quad \underline{C} \quad \underline{0} \\ = 4CC0H \text{ O/P data} \end{array}$$

Design an arithmetic CKT with one Selection Variable S and 2 inputs A & B when $S=0$ the CKT performs the addition operation $F=A+B$ when $S=1$ the CKT performs the increment operation $F=A+1$

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	S	X	Y	Cin	S	A	B	X	Y
$A+B$	0	A	B	0	1	0	0	0	0
$A+1$	1	A	0	1	0	0	1	0	1
					0	1	0	1	0
$x = A$					0	1	1	1	1
$y = S'A'B + S'A'B$					1	0	0	0	0
					1	0	1	0	0
					1	1	0	1	0
					1	1	1	1	0



Q. Design an arithmetic CKT with one selection variable S & 2 inputs A & B . When $S=0$ the CKT perform the subtraction operation $F=A-B$ by taking 2's complement of B when $S=1$ the CKT perform the decrement operation $F=A-1$.

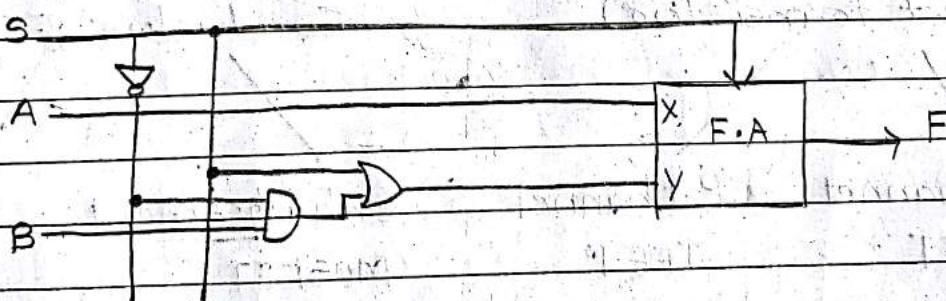
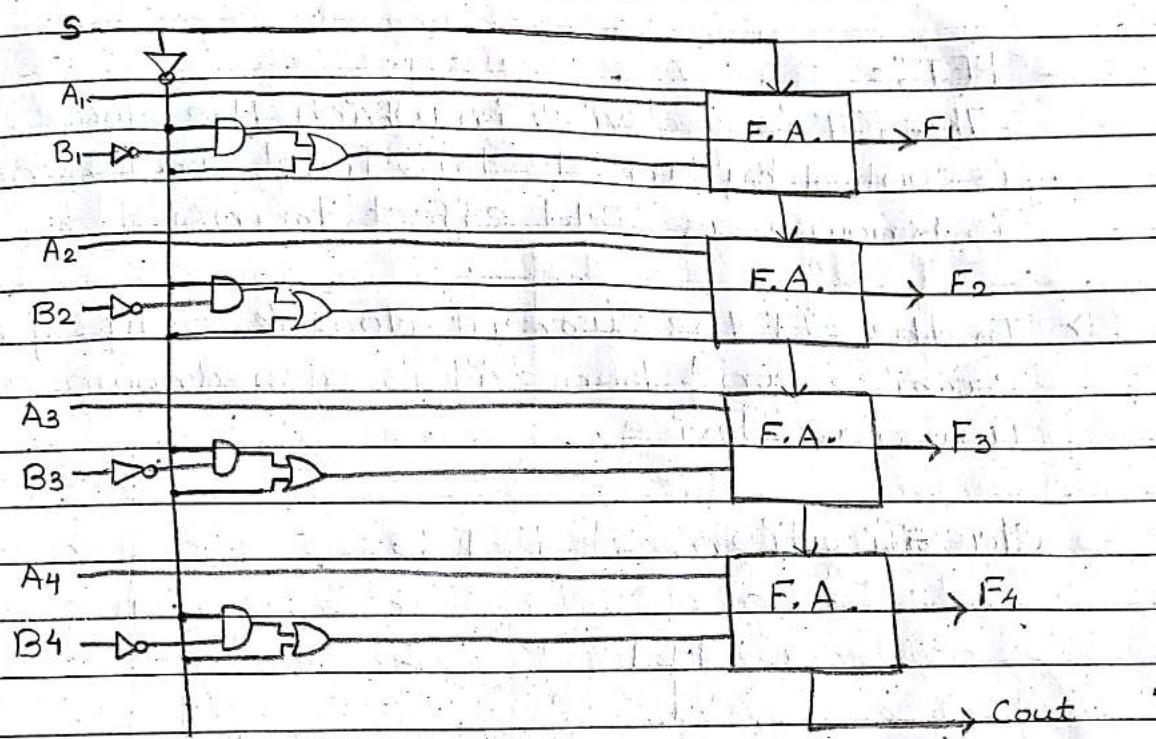
$$X = S'AB' + S'AB + SAB' + SAB = A$$

$$Y = S'A'B' + S'AB' + SA'B' + SA'B + SAB' + SAB$$

$$= S'B' + SA' + SA$$

$$= S'B' + S$$

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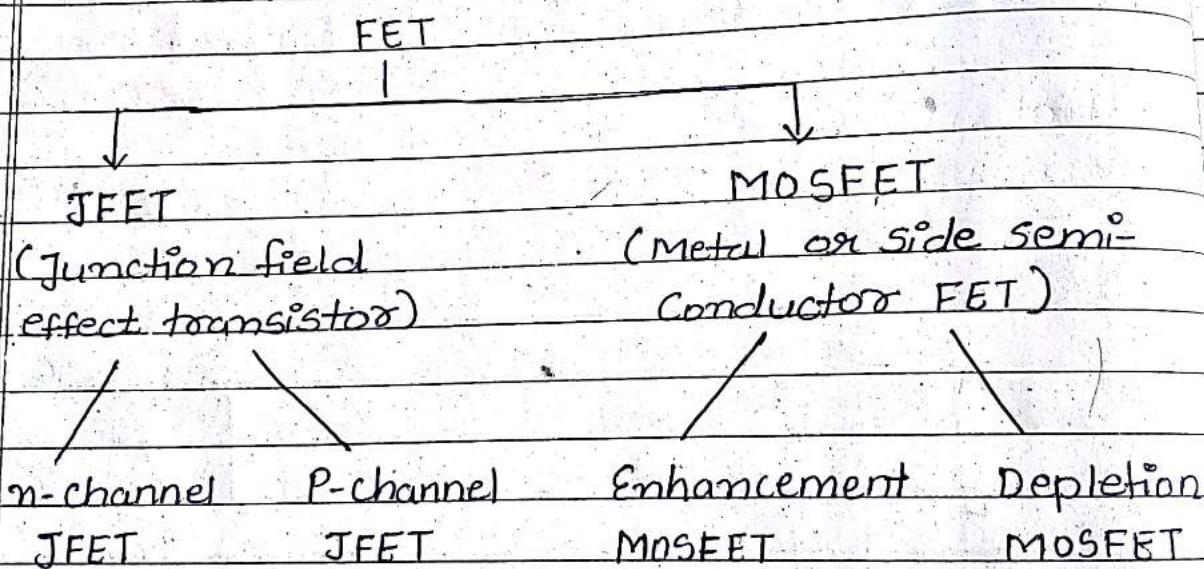
FET - Field effect transistor

FET :-

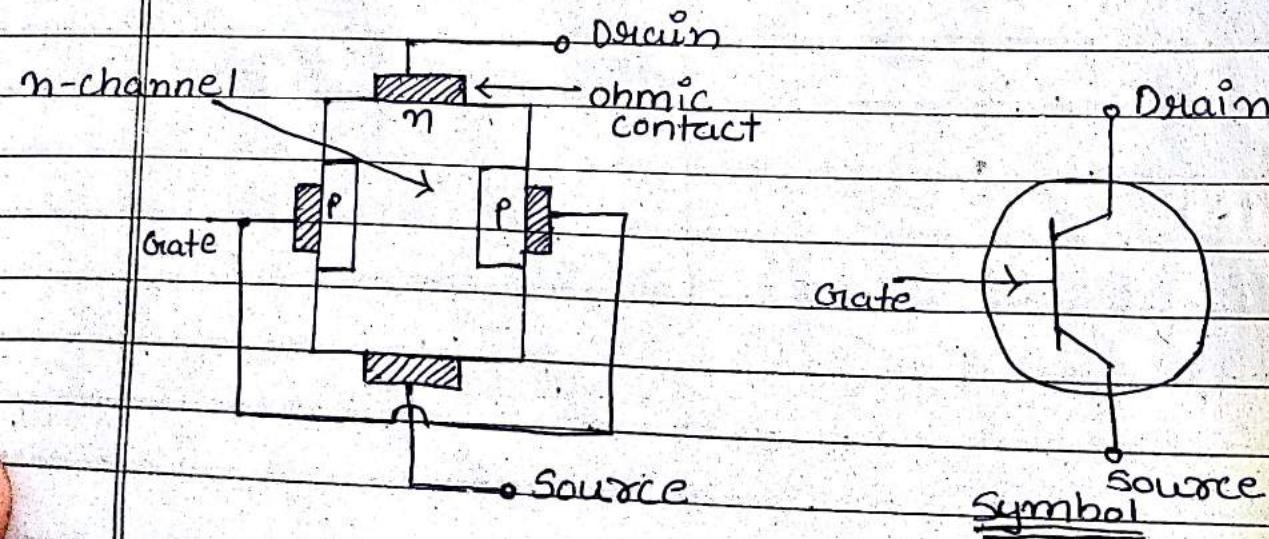
The FET is a device in which the flow of current is controlled by an electric field and hence it is known as field effect transistor.

In the FET the current flow is only by majority carriers and hence it is also known as unipolar device.

Classification of FET :-



Construction of n-channel JFET :-

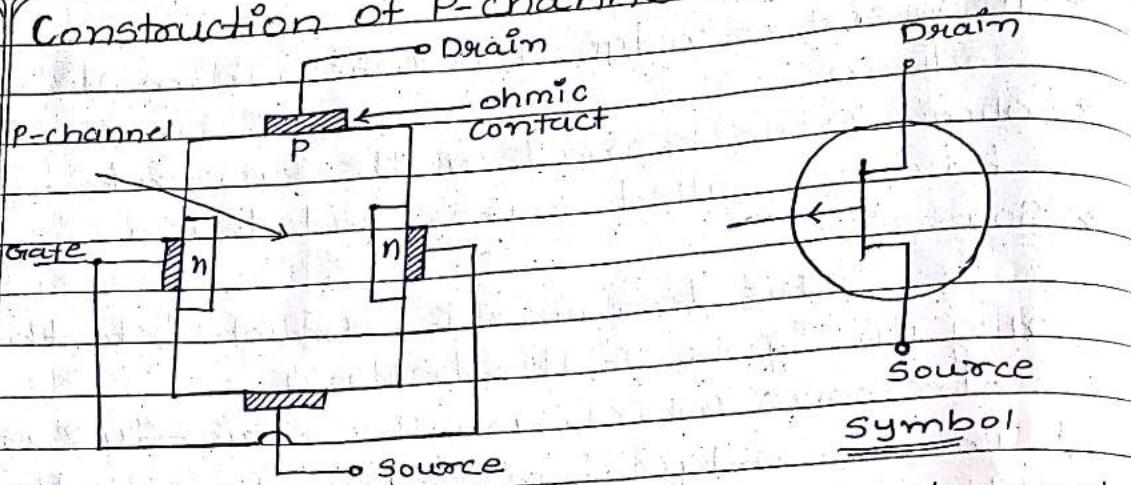


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- It consists of n-type bar which is made of silicon.
- Ohmic contacts made at the two ends of the bar are called source and drain.
- Source :-
This terminal is connected to the negative pole of the battery.
 - Electrons which are the majority carriers in the n-type bar, enter the bar through this terminal.
- Drain :-
This terminal is connected to the positive pole of the battery.
 - The majority carriers leave the bar through this terminal.
- Gate :-
Heavily doped p-type silicon is diffused on both sides of the n-type silicon bar by which P-N junction are performed.
 - These layers are joined together and called gate.
- Channel :-
Channel is the N-type material between the two gate regions.
 - The majority carriers move through this channel from source to drain.
 - Since the channel is made of n-type material this FET is called as N-channel FET.

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Construction of P-channel JFET :-

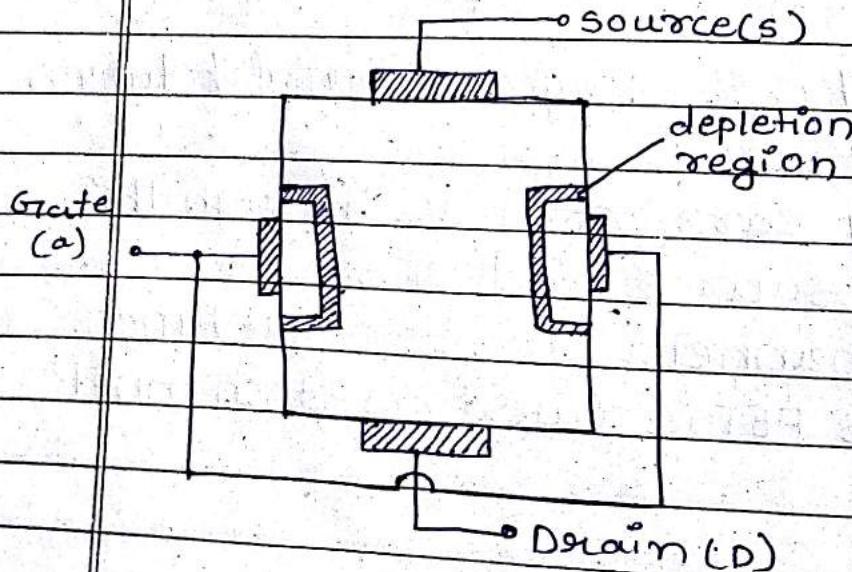


Case: 2

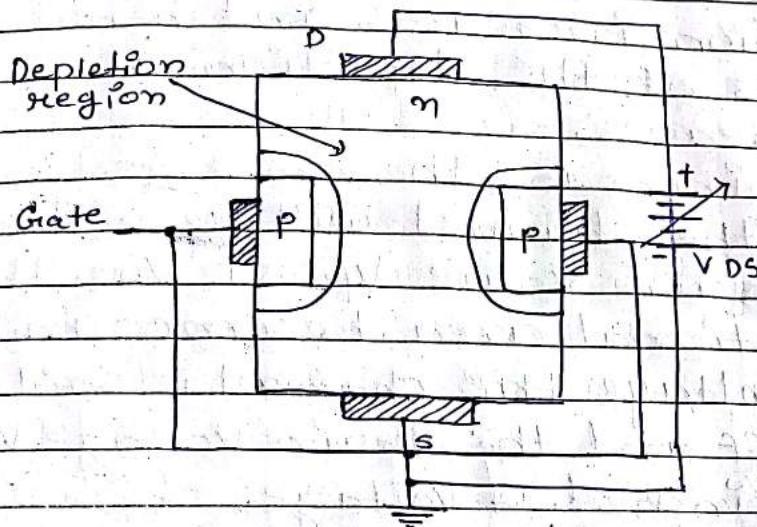
- The only difference between the p-channel and n-channel JFET is that a p-type semiconductor bar is being use with two n-type gate region.
- In P-channel JFET current flows due to the holes because holes are majority carriers in P-type semiconductor bar.

Operation on n-channel JFET :-

case: 1 $V_{GS} = 0$ and $V_{DS} = 0$



case: 2 $V_{GS} = 0V$ & $V_{DS} > 0$



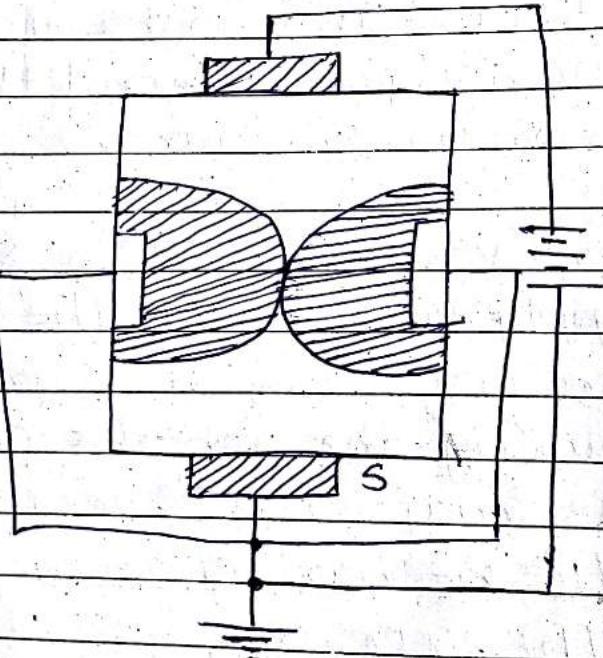
Case: 1 → No Voltage is applied between drain and source and gate and source the thickness of the depletion region around the p-n junction as shown in figure.

case: 2 → when $V_{GS} = 0V$ and $V_{DS} > 0$

Due to applying voltage V_{DS} the drain is +ve with respect to source and current starts flowing through the channel.
 → now, the majority carriers flow through the n-channel from source to drain so the current flows from drain to source.

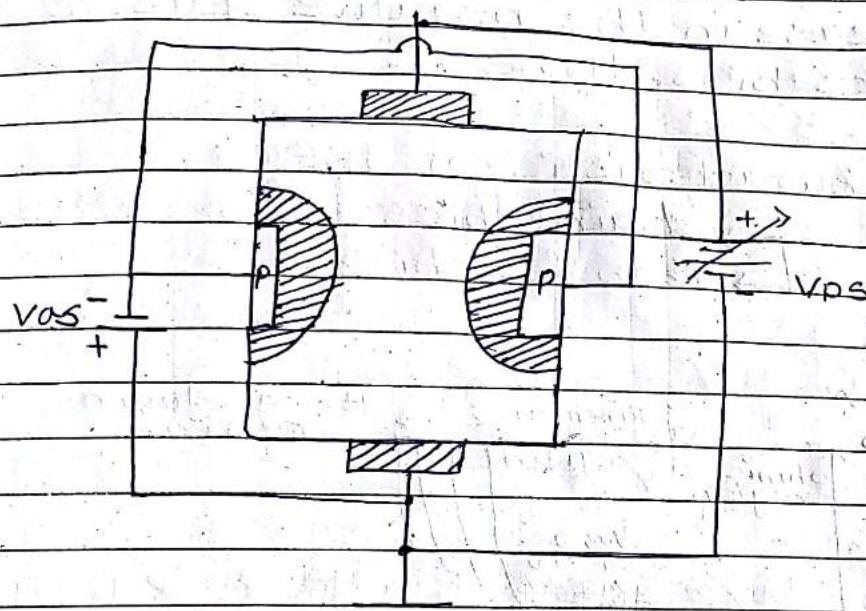
→ because of the resistance of the channel and the applying voltage V_{DS} there is a gradual increase of +ve potential along the channel from source to drain.

- Thus, the reverse voltage across the P-N junction increases and hence the thickness of the depletion region also increases.
- As V_{DS} is increase the cross sectional area of the channel will be reduced.
- At a certain value V_p of V_{DS} the cross-sectional area becomes minimum at this Voltage the channel is said to be pinched off and the drain voltage V_p is call the pinched off voltage.
- The figure shows the depletion layer at $V_{DS} > 0$ & $V_{DS} = V_p$



$$V_{AS} = 0 \quad \& \quad V_{DS} = V_p$$

Case: 3 $V_{DS} > 0$ & small -ve V_{GS}



$V_{DS} > 0$ & small negative V_{GS}

- As V_{GS} decrease from zero the P-N junction are reverse bias and hence the thickness of the depletion region increases.
- As V_{GS} is decrease from zero the reverse bias voltage across the p-n junction is increase and hence the thickness of the depletion region in the channel increase until the two depletion region make contact with each other in this condition the channel is said to be cut-off.
- The value of V_{GS} which is required to cut-off the channel is called cut-off voltage V_C .

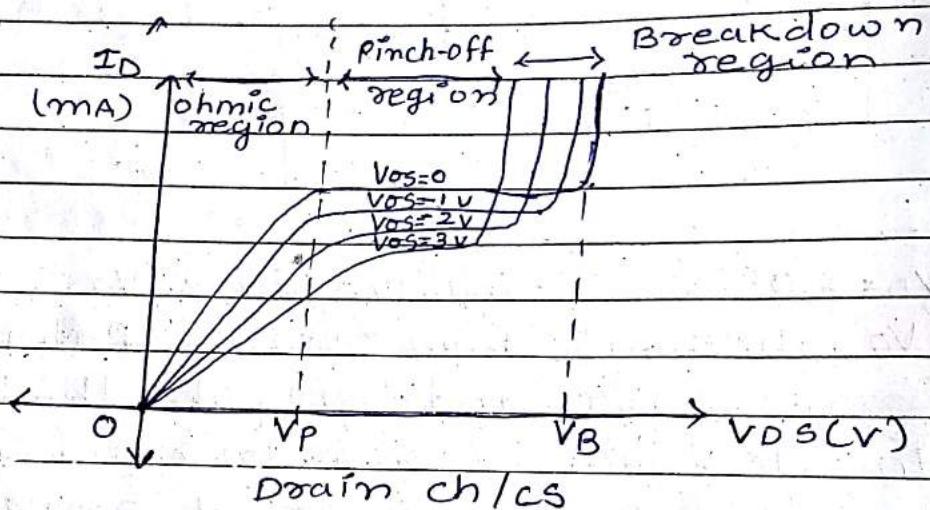
* Why FET is voltage control device?

- for $V_{GS} = 0$ maximum drain current I_D will flow through JFET.

→ The drain current that reduces with increase in the negative gate to source bias. Hence...

V-I characteristic of JFET :-

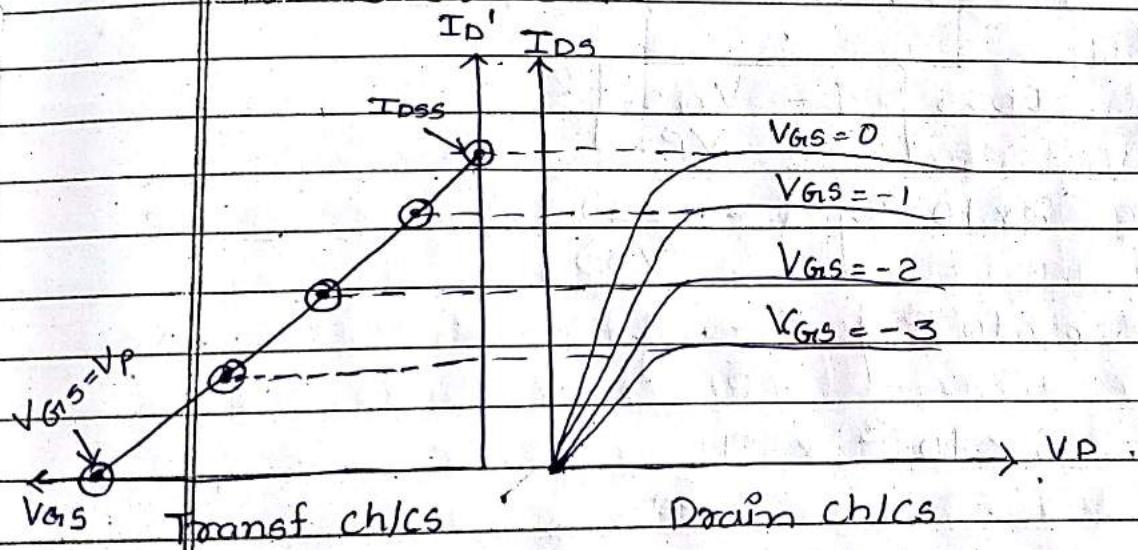
- drain ch/cs
- Transfer ch/cs.



- figure shows a plot of drain current I_D vs drain to source voltage V_{DS} at different value of gate to source voltage V_{GS} .
- ohmic region : As V_{DS} is increase from zero. I_D also increase
- The region form $V_{DS}=0V$ to $V_{DS}=V_p$ is called the ohmic region.
- Saturation region when $V_{GS} = V_p$, I_D become maximum

- when V_{DS} is increase beyond V_p the length of the pinch-off or saturation region increases, hence there is no further increases of I_D .
- Breakdown region: At a certain voltage corresponding to the point B. I_D suddenly increases the drain voltage at which the breakdown occurs is denoted by V_p and is known as breakdown voltage.

Transfer ch/cs :-



$$I_{DS} = I_{DSS} \left[1 - \frac{V_{GS}}{V_p} \right]^2 \rightarrow \textcircled{1}$$

I_{DSS} = max. Drain current.

V_p = Pinch-off Voltage

The Plot of output current I_d verses controlling gate voltage V_{GS} is known as Transfer characteristics. The relationship betn i_d & v_{GS} is defined by foll.

eqⁿ ①

Ex: An n-channel JFET as $I_{DSS} = 8\text{mA}$ & $V_P = -5\text{V}$. Determine the min. value of V_{DS} for pinch-off region & Drain current I_{DSS} for $V_{GS} = -2\text{V}$ in the pinch-off region.

$$\Rightarrow V_{DS\min} = V_{GS} - V_P \\ = -2 - (-5) \\ = 3 \text{ Volt}$$

$$\Rightarrow I_{DS} = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2 \\ = 8 \times 10^{-3} \left[1 - \frac{(-2)}{(-5)} \right]^2 \\ = 8 \times 10^{-3} \left[\frac{5-2}{5} \right]^2 \\ = 8 \times 10^{-3} \times \frac{9}{25} \\ = 2.88 \times 10^{-3} \text{ A} \\ = 2.88 \text{ mA}$$

Ex: JFET has driven current of 4mA if $I_{DSS} = 8\text{mA}$, $V_P = -6\text{V}$. Find the value of V_{GS} .

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$$

$$4 \text{ m} = 8 \text{ m} \left[1 + \frac{V_{GS}}{6} \right]^2$$

$$\frac{I}{2} = \left[\frac{1 + V_{GS}}{6} \right] 2$$

$$\frac{1 + V_{GS}}{6} = \frac{1}{\sqrt{2}}$$

$$\frac{V_{GS}}{6} = \frac{1 - \sqrt{2}}{\sqrt{2}}$$

$$V_{GS} = 6 \left(\frac{1 - \sqrt{2}}{\sqrt{2}} \right)$$

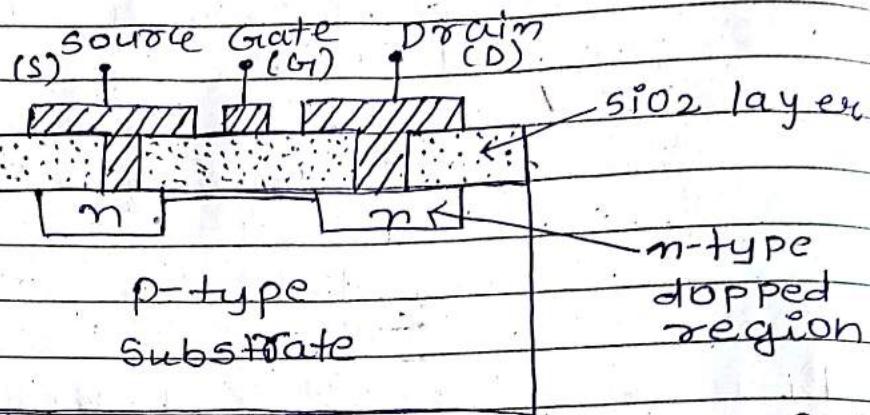
$$= -1.75 \text{ V}$$

Difference betⁿ BJT and JFET

1. BJT is bipolar device.	JFET is unipolar device.
2. It is current controlled device.	It is voltage controlled device.
3. Low input impedance.	High Input impedance.
4. Noise generated by BJT is high.	Noise generated by JFET is low.
5. Size of BJT is more than JFET.	Size of JFET is smaller than BJT.
6. It is cheaper.	It is costly than BJT.
7. Thermal breakdown occurs due to positive temp.	It is unaffected by temp. changes.

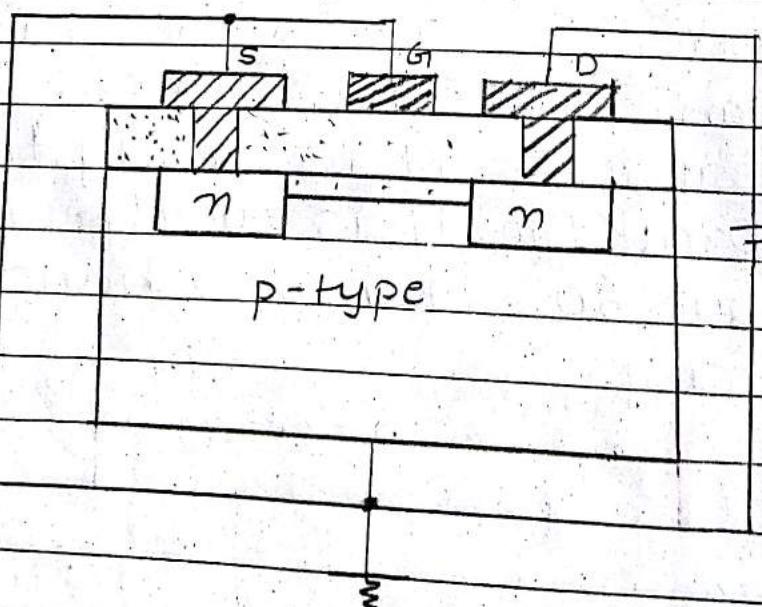
MOSFET

* Construction of Depletion Type MOSFET



- A P-type Semiconductor material is used as substrate.
- The Drain & Source terminal are connected to the n-type region through the metallic contact.
- The Gate terminal is insulated from the n-channel by thin SiO_2 layer.

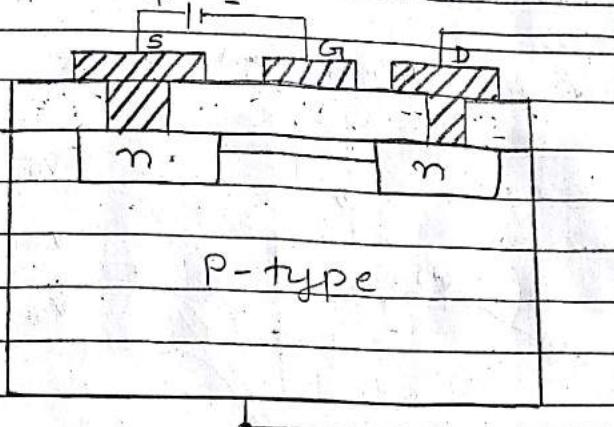
Case: 1 $V_{GS} = 0$ & $V_{DS} > 0$



Case:

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Case:2 $V_{GS} < 0$ & $V_{DS} > 0$



Case:1

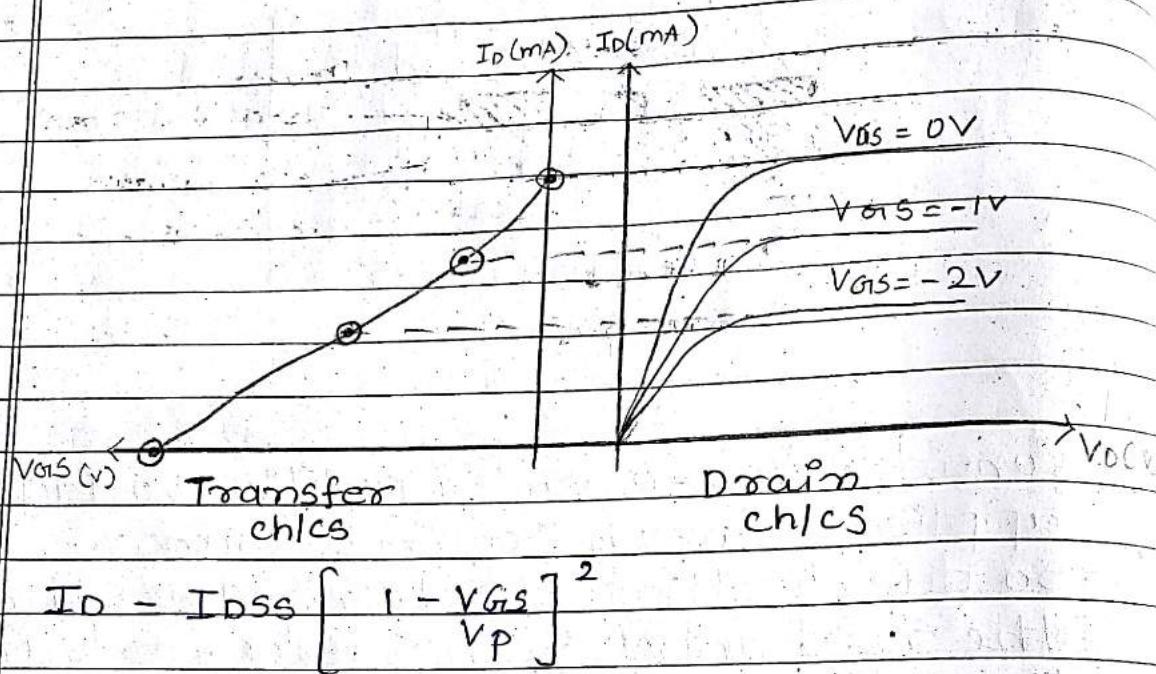
- Consider $V_{GS} = 0$ and a positive voltage is applied between Drain & Source.
- So due to that electron flow through the n-channel from Source to Drain therefore the conventional current I_D flows through the channel from Drain to Source.

Case:2

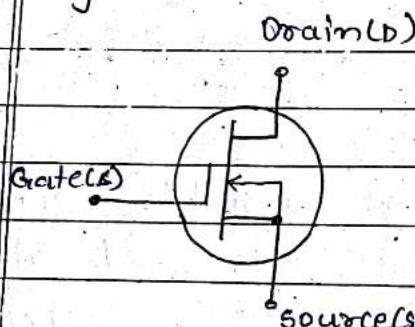
- Due to negative voltage applied at gate terminal it will repel the electrons towards the p-type substrate and attract the holes from the substrate, therefore the drain current will decrease with increase in negative value of V_{GS} .
- So, as V_{GS} increases, I_D decreases for a constant value of V_{DS}

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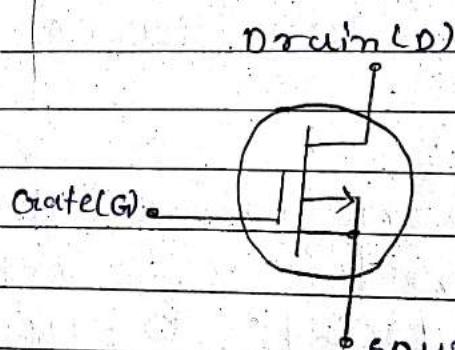
Chics of n-channel depletion Type MOSFET



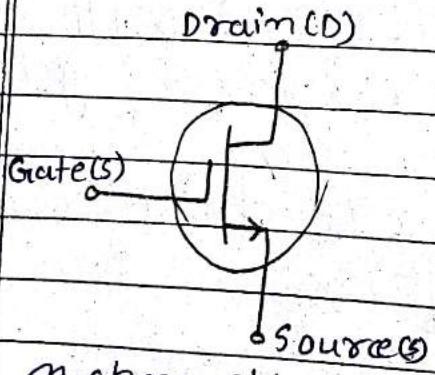
Symbol:



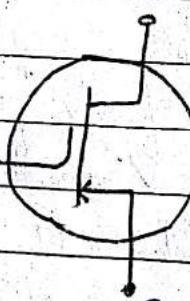
n-channel
Depletion MOSFET



p-channel
Depletion MOSFET



n-channel
Depletion MOSFET



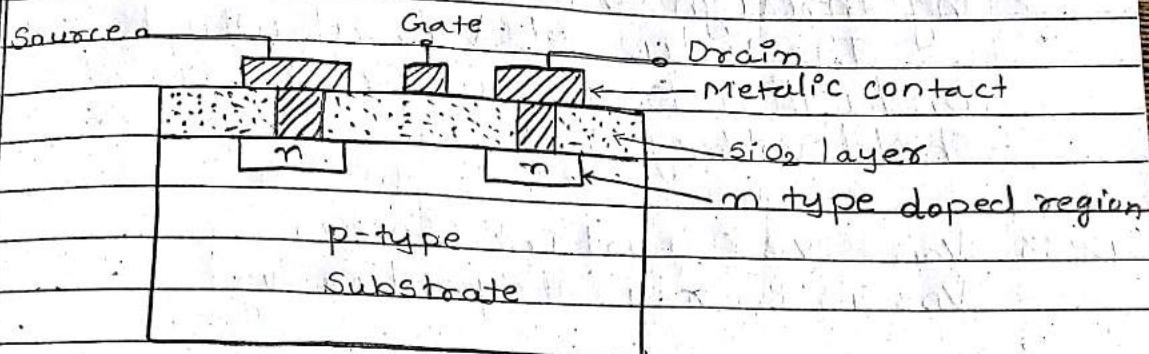
p-channel
Depletion MOSFET

case : 1

Case : 2

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* Enhancement MOSFET



Construction of enhancement MOSFET is same as depletion MOSFET but channel is absent in the enhancement MOSFET.

* Operation

case:1 $V_{GS} = 0$ & $V_{DS} > 0$

In this case $V_{GS} = 0$ and hence due to the absence of n-type channel '0' current will flow.

Case:2 $V_{GS} > 0$ & $V_{DS} > 0$

Due to the positive potential at gate terminal the holes will repel in the p-type substrate. This result in creation of a depletion region near the SiO_2 insulating layer.

As V_{GS} increase the no. of electron getting near the SiO_2 layer will increase.

This electron concentration creates & induce n-channel which connect the n-type doped region.

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The drain current then starts flowing through this induce channel.

The value of V_{DS} at which this conduction begins is called as the threshold voltage.

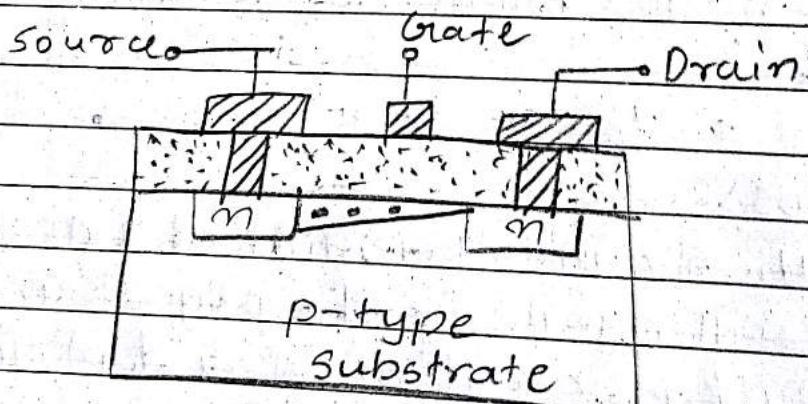
Case:3 $V_{GS} = \text{tve constant (Some)}$

V_{DS} is increased gradually

Due to this the Gate terminal will become less & less positive w.r.t drain.

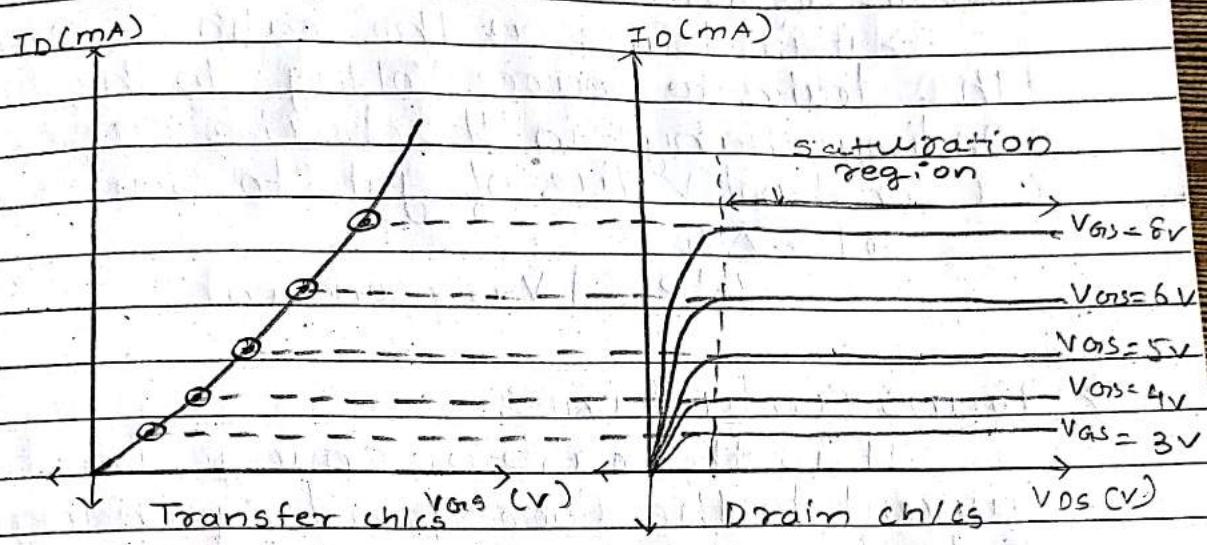
So, less no. of electrons are attracted towards gate terminal and the induce channel becomes narrow.

Eventually the channel width will be reduced to a point of pitch-off & the Saturation condition will be establish.

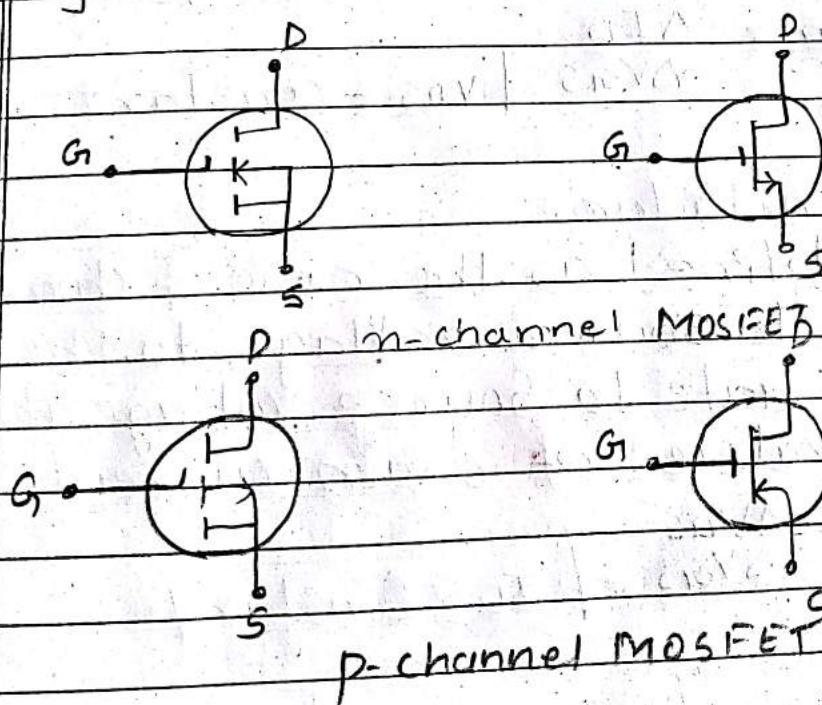


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* Characteristics of n-channel enhancement MOSFET



* Symbol of Enhancement MOSFET



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Parameters of JFET

→ Drain resistance r_d

→ It is defined as the ratio of change in the drain to source voltage to the corresponding change in the drain current at a constant value of gate to source voltage.

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D}$$

| $V_{GS} = \text{constant}$

→ Transconductance.

It is the ratio of change in drain current to the corresponding change in Gate to source voltage at a constant value of Drain to source voltage.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

| $V_{DS} = \text{constant}$

→ Amplification Factor.

It is defined as the ratio of change in the drain to source voltage to the change in the Gate to source voltage at a constant value of drain current I_D .

$$h_f = \frac{\Delta V_{DS}}{\Delta V_{GS}}$$

|

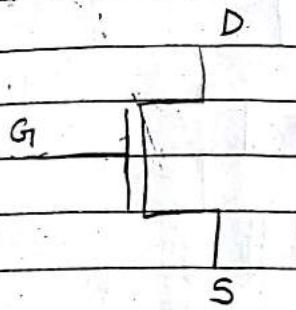
$I_D = \text{constant}$

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CMOS

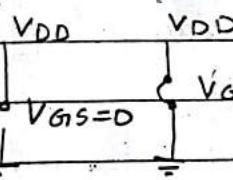
→ NMOS
→ PMOS

NMOS

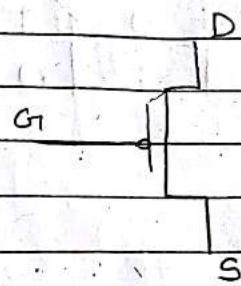


If $V_{GS} = 0 \rightarrow NMOS = OFF$

$V_{GS} = 1 \rightarrow NMOS = ON$

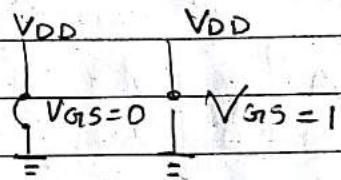


PMOS



If $V_{GS} = 0 \rightarrow PMOS = ON$

$V_{GS} = 1 \rightarrow PMOS = OFF$

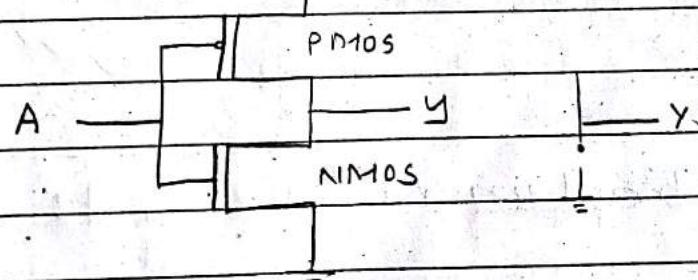


Implement inverter using CMOS

A	y
0	1
1	0

+VDD

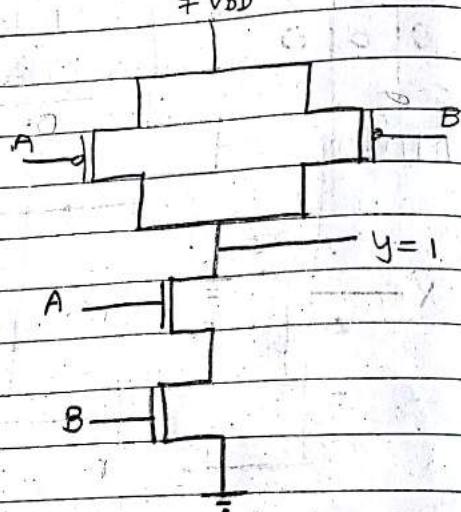
\rightarrow logic '1'
Gnd \rightarrow logic '0'



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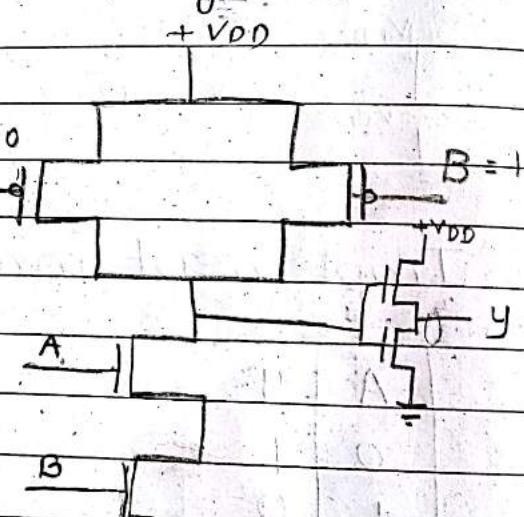
Implement Nand Gate using CMOS

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



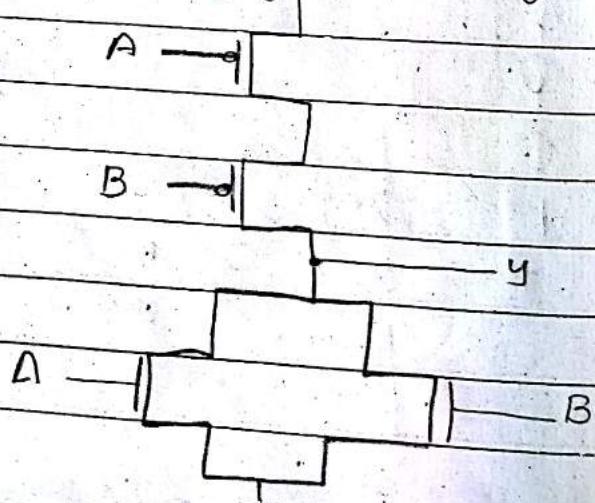
Implement And Gate Using CMOS

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1



Implement NOR Gate using CMOS logic ckt

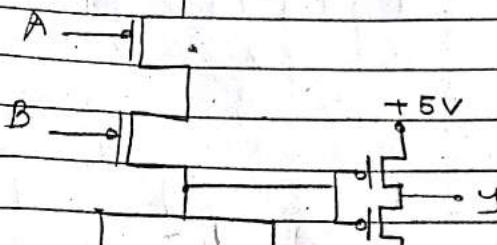
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0



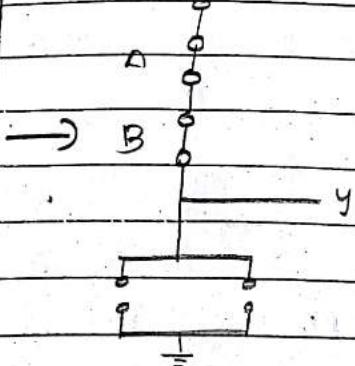
Date: _____
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Implement OR Gate using CMOS

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1



For
NOR



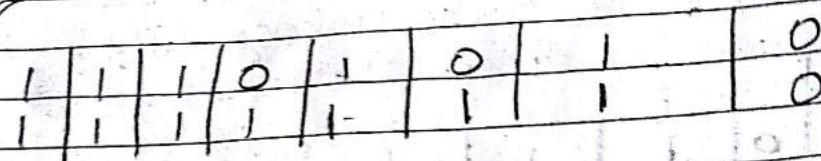
	$\bar{A} \cdot \bar{B}$	$\bar{A} + \bar{B}$	$A \cdot B'$	$(A + B')'$
NMOS	S	P	S	
PMOS	P	S		

logic

$Y = \overline{AB} + \overline{CD} \rightarrow$ Design using CMOS CKT

A	B	C	D	AB	CD	$AB+CD$	$\overline{AB+CD}$
0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	1
0	0	1	0	0	0	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	0	0	1
0	1	0	1	0	0	0	1
0	1	1	0	0	0	0	1
0	1	1	1	0	1	1	0
1	0	0	0	0	0	0	1
1	0	0	1	0	0	0	1
1	0	1	0	0	0	0	1
1	0	1	1	0	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	0
1	1	1	0	1	0	1	0
1	1	1	1	1	1	1	0

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$+5V$

$A \rightarrow$ $B \rightarrow$

$C \rightarrow$ $D \rightarrow$

\downarrow y

$A \rightarrow$ $C \rightarrow$

$B \rightarrow$ $D \rightarrow$

$=$

$$y = \overline{(A+B)}(C+D)$$

A	B	C	D	$A+B$	$C+D$	$(A+B)(C+D)$	$\overline{(A+B)}(C+D)$
0	0	0	0	0	0	0	1
0	0	0	1	0	1	0	1
0	0	1	0	0	1	0	1
0	0	1	1	0	1	0	1
0	1	0	0	1	0	0	1
0	1	0	1	1	1	1	1
0	1	1	0	1	1	0	0
0	1	1	1	1	1	1	0

Date.:

1	0	0	0	1	0	0	1	1
1	0	0	1	1	1	1	1	0
1	0	1	0	1	1	1	1	0
1	0	1	1	1	1	1	1	0
1	1	0	0	1	0	0	1	1
1	1	0	1	1	1	1	1	0
1	1	1	0	1	1	1	1	0
1	1	1	1	1	1	1	1	0

A — d | | p — C.

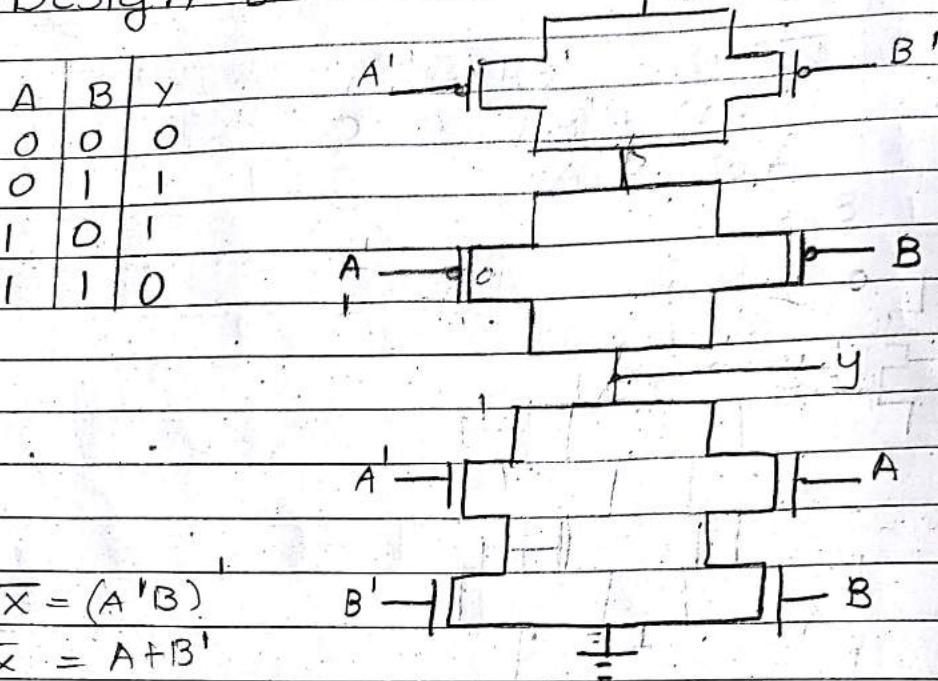
B — d | | p — D

y.

A — | | | — B

C — | | | — D

Design EX-OR Gate Using CMOS



$$\overline{X} = (A'B)$$

$$\overline{X} = A + B'$$

Design EX-NOR Gate using CMOS

