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$$\boxed{\quad} + \boxed{\quad} + \boxed{\quad} + \boxed{\quad} + \boxed{\quad} = \boxed{101101}$$

## \* Addition Part

Q-1 Register :- A Register is a memory device that can be used to store more than one bit of information.

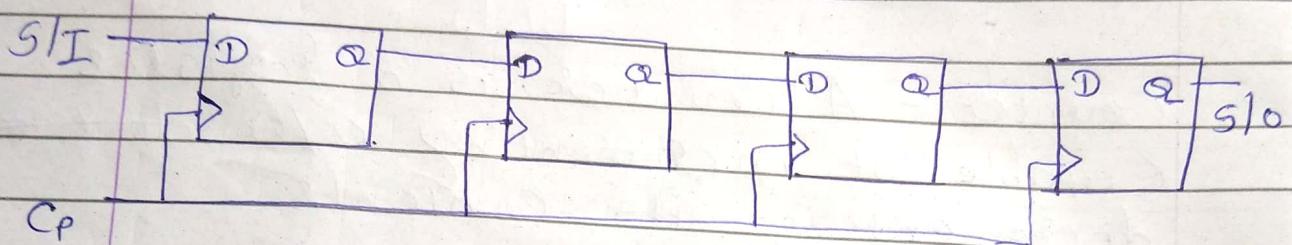
Counter :- A Counter is a register capable of incrementing & / or decrementing its contents.

Q-2 Application of Shift Register.

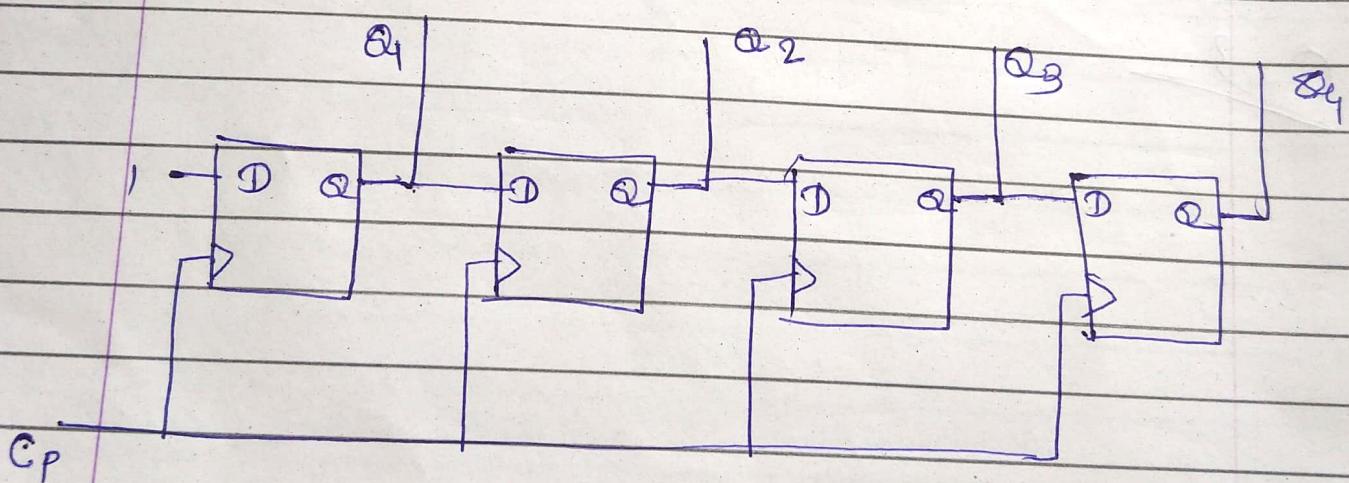
Q-3

Q-4 Draw logical dia.

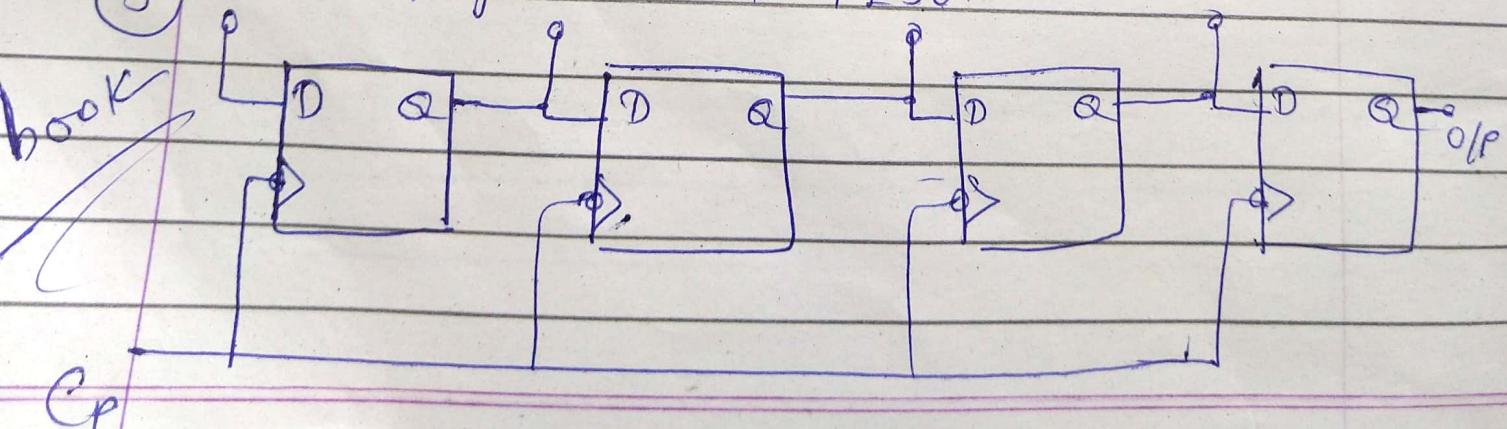
① 4 bit register in SJ SO.



② 4 bit register in SJ PO



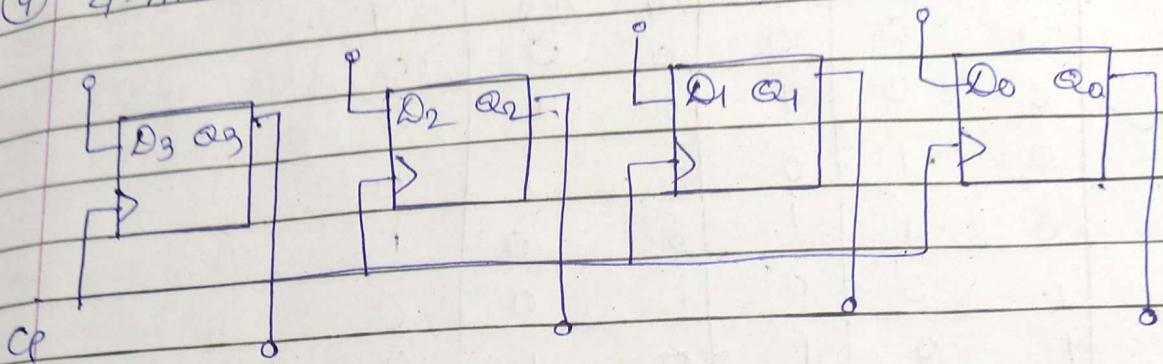
③ 4 bit register in PI SO.



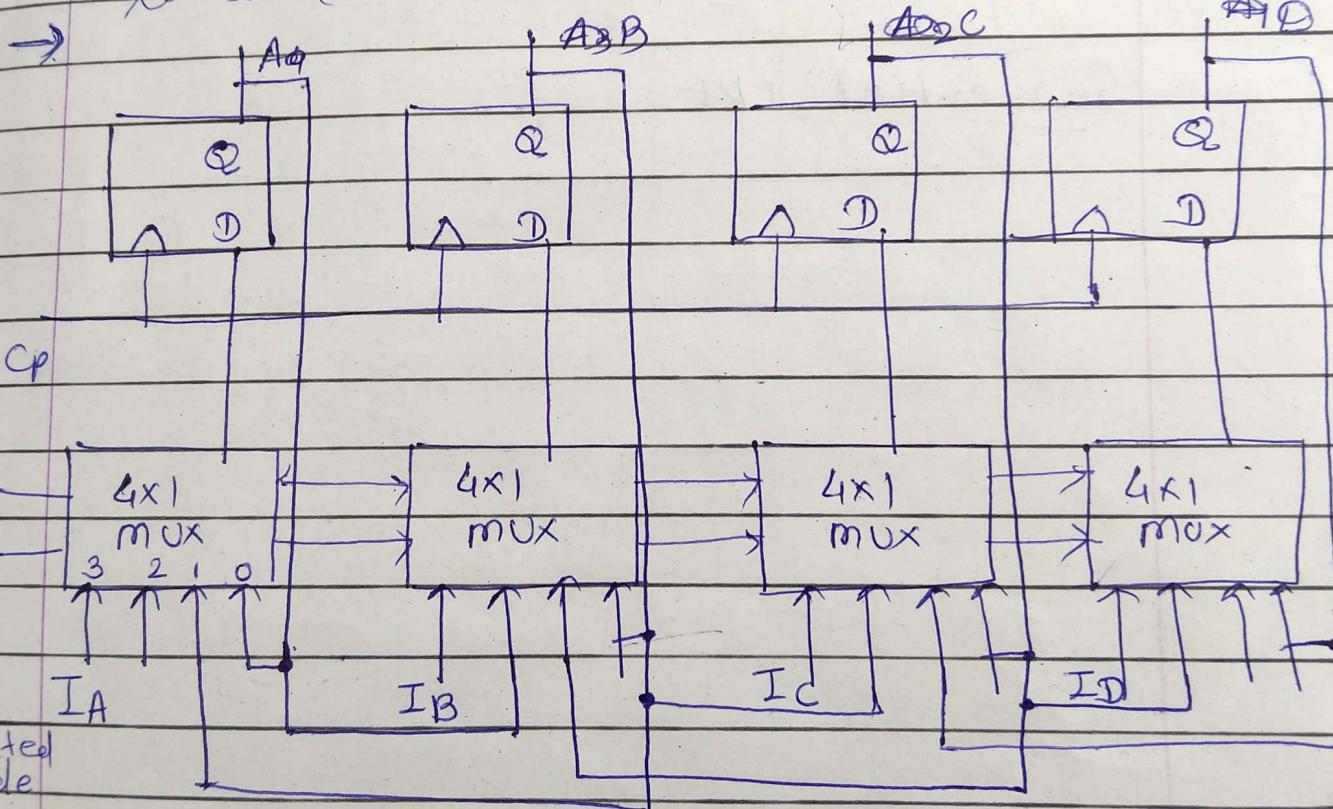
... 10 ms to the ... in the most

481  
21 481  
3413

④ 4-bit Register in PIPPO



Q5 Bidirectional Shift Register with parallel load (universal shift register)



$S_0\ S_1$	Selected mode
0 0	No change
0 1	Shift left
1 0	Shift right
1 1	Parallel load

- $I_1$  - Serial i/p for shift-left  
 $I_2$  - Serial i/p for shift-right

Step-4 Repeat step 4 & 5 until stack is  
 1. amine  
 Step-4

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$$[ ] + [ ] + [ ] + [ ] + [ ] = [ ]$$

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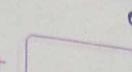
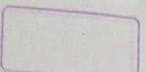
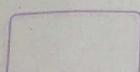
rising flip-flop

(Q-6)

P. S	I/P	N. S.	O/P		
A <sub>1</sub>	A <sub>2</sub>	X	A <sub>1</sub>	A <sub>2</sub>	Y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	0	0	1
1	0	0	1	0	0
1	0	1	0	1	0
1	1	0	1	1	0
1	1	1	0	1	1

Sequential CKT

421  
21421  
5413



Q<sub>n</sub>  
0

Q<sub>n+1</sub>  
0



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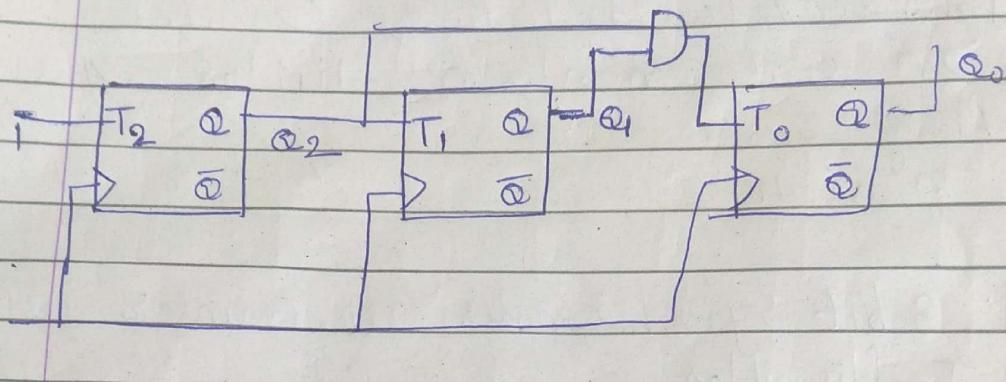
0

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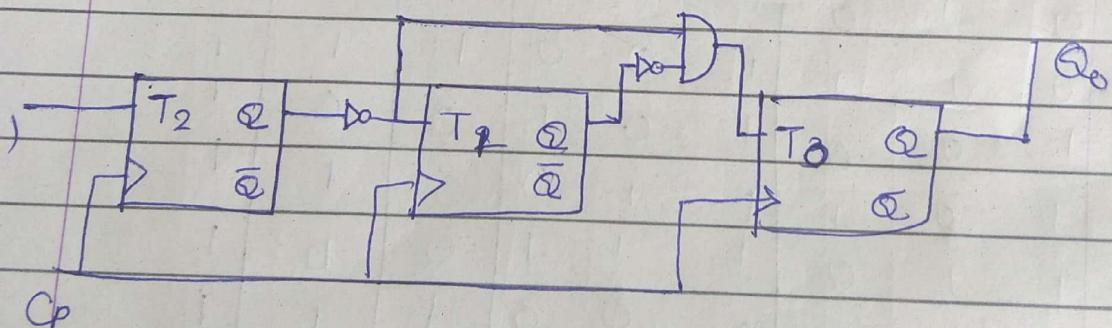
$$\boxed{\quad} + \boxed{\quad} + \boxed{\quad} + \boxed{\quad} + \boxed{\quad} = \boxed{\quad}$$



~~Q-10~~ 3-bit synchronous down counter using  
T-flip flop.

Reverse ~~then~~ Up

$$T_1 = \bar{Q}_2, \quad T_0 = \bar{Q}_1 \bar{Q}_2, \quad T_2 = 1$$



~~Q-11~~ 3 bit syncrh. Up/Down using T F.F

$m_{20} \rightarrow$  Up

$m=1 \rightarrow$  down

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ક્રમિક

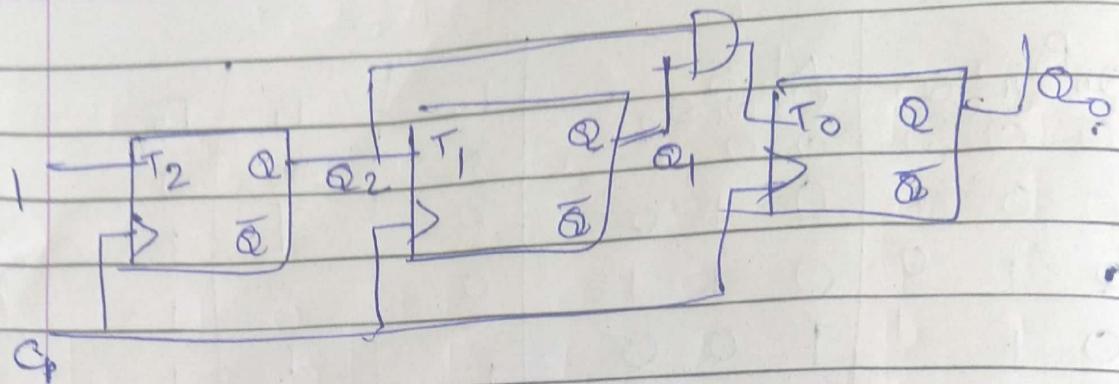
M	Q1	Q2	N.	S.	Q1	Q2	T0	T1	T2
0	0	0	0	0	0	1	0	0	1
0	0	0	1	0	0	0	0	1	1
0	0	1	0	0	0	1	0	0	1
0	1	0	0	1	0	1	0	1	1
0	0	1	1	0	0	0	1	1	1
0	1	0	0	1	0	1	0	0	1
0	1	0	1	1	0	0	0	1	1
0	1	1	0	1	1	1	0	0	1
0	1	1	1	0	0	0	1	1	1
1	0	0	0	0	0	1	0	0	1
1	0	0	1	0	1	0	0	1	1
1	0	1	0	0	1	1	0	0	1
1	0	1	1	0	0	0	1	1	1
1	1	0	0	1	0	1	0	0	1
1	1	0	1	1	0	0	0	1	1
1	1	1	0	1	1	1	0	0	1
1	1	1	1	0	0	0	1	1	1

m	Q1	Q2	Q2	Q1	Q1	Q2	T0	T1	Q1
00	0	0	0	0	1	0	0	0	0
01	0	0	0	1	1	0	0	1	0
11	0	0	0	1	1	0	0	1	0
10	0	0	1	1	1	0	1	1	0

$T_1 = Q_2$

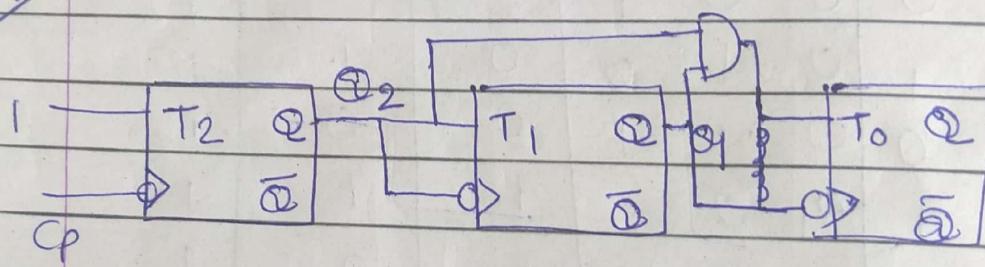
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ક્રમાંક

$$[ ] + [ ] + [ ] + [ ] = [ ]$$



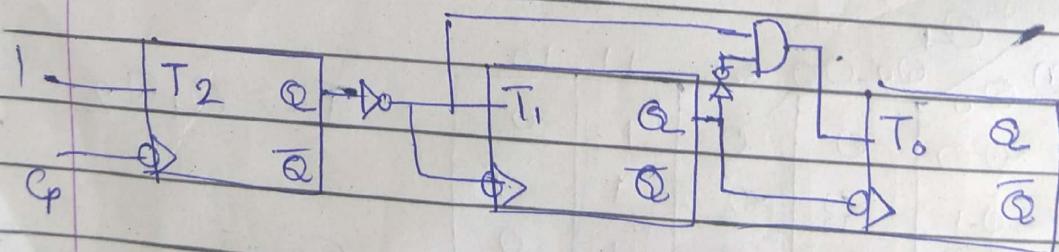
~~Q-12~~ 3-bit Asynchronous up Counter  
using T.

T.T.  
Q-1



~~Q-B~~ 3-bit Asyn. down C. using T.

T.T.  
Q-10

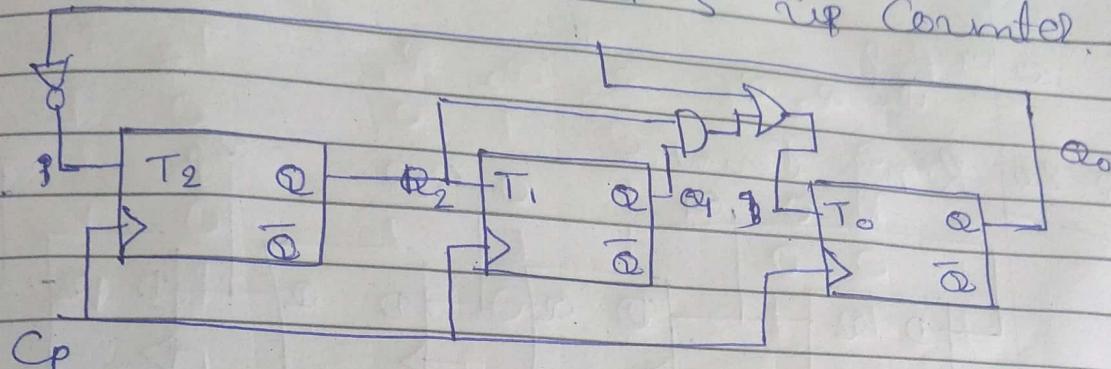


(Q-14)

→ Q-12

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Q-15 Synchronous Mod-5 up Counter.



P.S.	N.S.							
$Q_0$	$Q_1$	$Q_2$	$Q_0$	$Q_1$	$Q_2$	$T_0$	$T_1$	$T_2$
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	-1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	-1	1
1	0	0	0	0	0	1	0	0
1	0	1	x	x	x	x	x	x
1	1	0	1	1	0	1	1	1

$Q_0 \quad Q_2 \quad 0 \quad 0 \quad 0 \quad 1 \quad 1 \quad 10$   

0	0	0	1	0
1	1	x	x	x

 $T_0 = Q_0 + Q_1 Q_2$

$Q_0$	$Q_1$	$Q_2$	$0$	$1$	$10$
0	0	0	1	1	0
1	0	x	x	x	x

$T_1 = Q_2$

$Q_0$	$Q_1$	$Q_2$	$0$	$1$	$10$
0	1	1	1	0	x
1	0	x	x	x	x

$T_2 = \overline{Q_0}$

Q16 Down

Q-17 Asyn  
Up- down

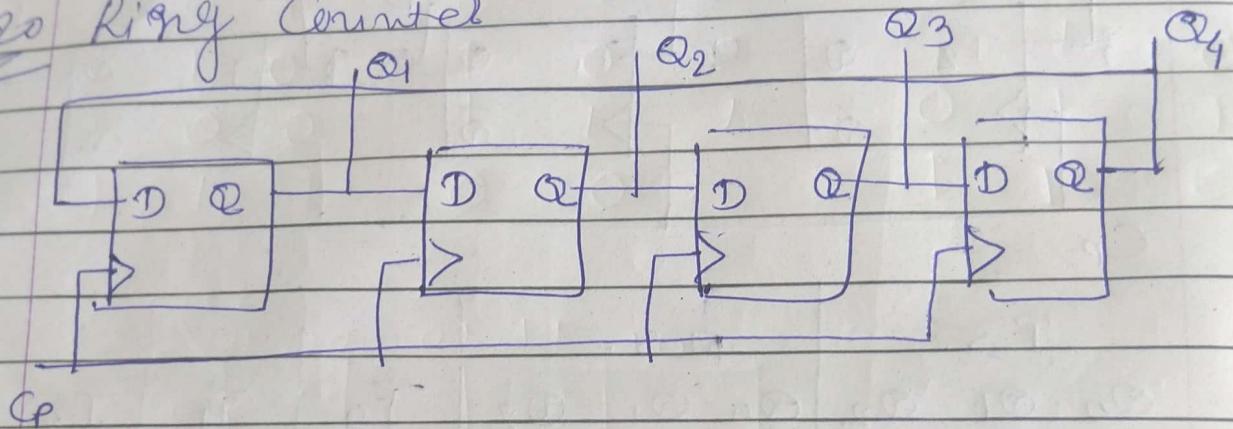
Q-18

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$$\boxed{\quad} + \boxed{\quad} + \boxed{\quad} + \boxed{\quad} = \boxed{\quad}$$

$\frac{Q_1}{2} = ?$

Q-20 Ring Counter

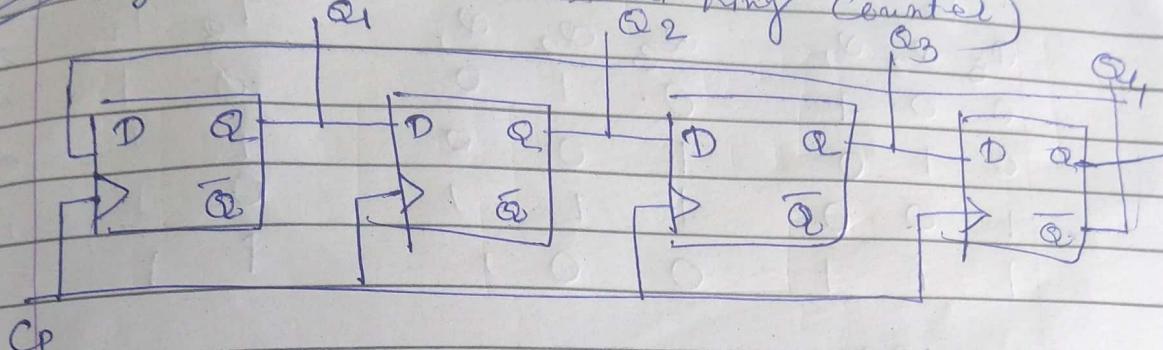


clk	$Q_3$	$Q_2$	$Q_1$	$Q_0$
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1

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$$[ ] + [ ] + [ ] + [ ] + [ ] = [ ]$$

Q-21 Johnson (Twisted Ring Counter)



CP

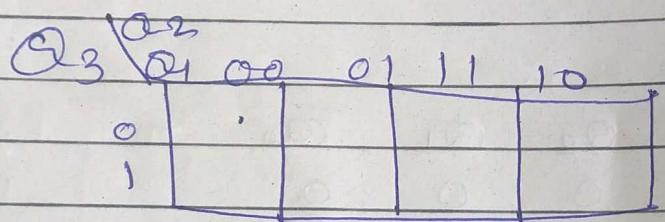
CLK	Q <sub>3</sub>	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>
0	0	0	0	0
1	1	0	0	0
2	1	0	1	0
3	1	1	0	0
4	1	1	1	0
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1
8	0	0	0	0

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ક્રમાંક

$$\boxed{\quad} + \boxed{\quad} + \boxed{\quad} + \boxed{\quad} = \boxed{\quad}$$

1, 2, 4, 7

PS	NS	$T_3$	$T_2$	$T_1$
$Q_3 \ Q_2 \ Q_1$	$\bar{Q}_3 \ \bar{Q}_2 \ \bar{Q}_1$	0	1	1
0 0 1	0. 1 0	0	1	0
0 1 0	1 0 0	1	1	1
1 0 0	1 1 .	0	1	1
1 1 1	0 0 )	1	1	0



$$T_2 = 1 \quad T_1 = \bar{Q}_2 \quad T_0 = \bar{Q}_3$$

