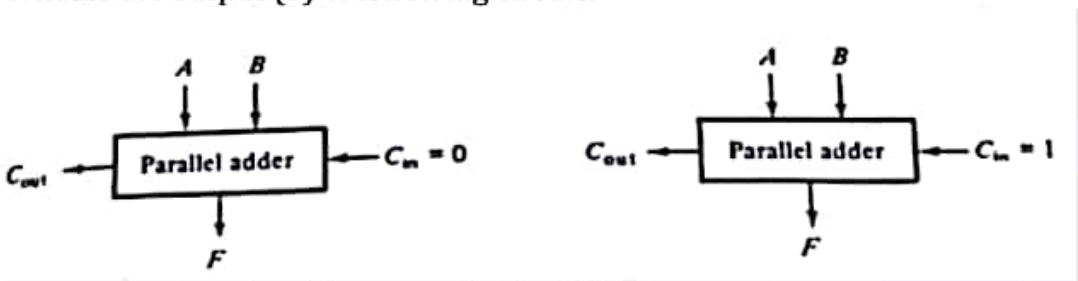
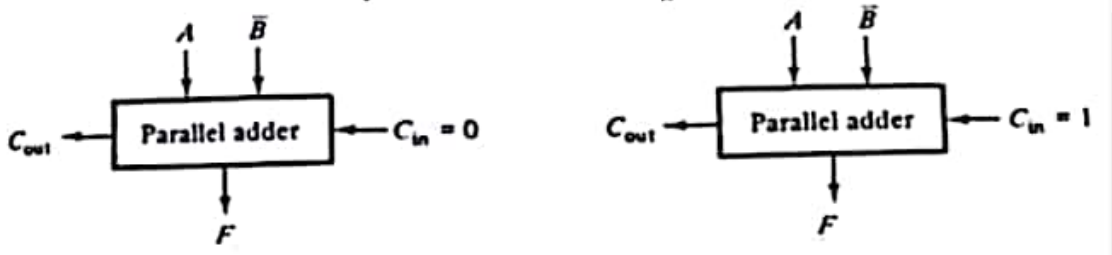
# Question Bank of Unit 5: Processor Logic Design

1 Define: Microoperation
2 Define: Accumulator.
3 Define: Status Register.
4 List of the micro operations perform by an accumulator.
5 Briefly explain the accumulator register in ALU.
6 Draw and explain basic block diagram of Processor unit in detail.
7 Discuss the effect of output carry in the arithmetic circuit.
8 Draw block diagram of ALU and explain ALU in detail.
9 Explain how the value of overflow bit is calculated in status register.
10 What is micro-operation? Enlist the micro-operation performed by accumulator.
11 What is the basic building block of ALU? Design arithmetical unit which perform four different arithmetical operation on number X and Y.
12 Design an Arithmetic unit which performs any four different arithmetic operations on 4-bit binary numbers A and B.
13 Design Arithmetical unit which perform following operations on two bits numbers A and B.
1. Addition of A and B.(A+B)
2. Addition of A and B with carry.(A+B+1)
3. Subtraction of A and B using 1's complement method.(A+B')
4. Subtraction of A and B using 2's complement method.(A+B'+1)
14 What is the output (F) of following circuit?




15 Determine the value of output F for the following circuit.




16 Draw a single block of logical unit which can perform following operation of A1 and B1.
(i) A1 and B1
(ii) A1 xor B1
(iii) A1 or B1
(iv) not(A1)

17 Design an arithmetic circuit with a selection variables S, that generates the following arithmetic operations. Draw the logic diagram of one typical stage.

| S | $C_{In}=0$ | $C_{In}=1$ |
|---|---|---|
| 0 | F=A+B | F=A+B+1 |
| 1 | F=A-1 | F=A |

18 Draw a logical diagram using parallel adder block for the following Operations:
1. Addition of A and B with carry
2. Subtraction of A and B using 2's complement method.

19 Design a logical unit which can perform four different logical operations of A and B n-bit binary data.

20 Design an arithmetic circuit with two selection variables, S1 and S0, that generates the following arithmetic operations. Draw the logic diagram of one typical stage.

| $S_1$ | $S_0$ | $C_{In}=0$ | $C_{In}=1$ |
|---|---|---|---|
| 0 | 0 | F=A | F=A+1 |
| 0 | 1 | F=A+B | F=A+B+1 |
| 1 | 0 | F=A-1 | F=A |
| 1 | 1 | F=A+B' | F=A+B'+1 |

21 Design logical unit which perform following eight logical operation on number A and B.
1. A XOR B
2. A XNOR B
3. A AND B
4. A OR B
5. A NAND B
6. A NOR B
7. Complement of A
8. Transfer of A

22 Draw a logical diagram using parallel adder block for the following operations.
1. Subtraction of A and B using 1's complement method
2. Subtraction of A and B using 2's complement method

23 Explain the Zero flag(bit) in status register with proper logical diagram.

24 Draw one stage of logical unit which performs following Logical operations.
Ai +Bi , (Ai XOR Bi )

25 Draw a logical diagram using parallel adder block for the following operations a.
1. Decrement of A.
2. Transfer of A

26 Design logical unit which perform (a) AND (b) OR (c) Ex-OR (d) NOT operation of number A and B.

27 Design Arithmetical unit which perform following operations on two numbers A and B of two bits. The operations are:
1. Transfer of A
2. Increment A by 1
3. Addition of A and B.
4. Addition of A and B with carry.