Sub:- Digital Logics Design

Unit Test - 2

Syllabus (Chap-2, 3, 4 &5)

	Unit 2
4	**Combinational logic with MSI and LSI:** Read Only Memory (ROM), Programmable Logic Arrays (PLA).
	Unit 3
5	**Sequential logic:** Introduction, Flip-Flops, Triggering of Flip-Flops, Analysis of clocked sequential circuits, Flip-flop excitation tables, Flip flop conversion, State reduction and assignment, Design procedure.
	Unit 4
6	**Registers, Counters and The Memory Unit:** Introduction, Registers, Shift registers, Ripple counters, Synchronous counters, Timing sequences, Memory Unit.
	Unit 5
7	**Processor logic design:** Introduction, Accumulator register, Arithmetic logic unit, Design of Arithmetic circuit, Design of logic circuit, Status Register, Design of Shifter, Processor Unit.

Text book:

- Mano Morris - "Digital Logic and Computer Design", Pearson education.

Reference books:

- Anand Kumar - "Fundamentals of Digital electronics and circuits", Prentice Hall India Pvt. Ltd.

Digital Logic Design
Chap 4 (Q Bank)

Q.1 Define:
- Register
- Counter

Q.2 List out applications of shift register.

Q.3 How many number of flip-flop needed to store number
(a) $(104)_{10}$
(b) $(ACF2)_{16}$
(c) $(457)_8$
(d) $(1010111011)_2$

Q.4 Draw logical diagram of
(a) 4bit register in Serial in Serial out configuration (SISO).
(b) 4bit register in SIPO.
(c) 4bit register in PISO.
(d) 4bit register in PIPO.

Q.5 Explain bidirectional shift register with parallel load. [Universal shift register]

Q.6 Design sequential circuit whose state table is listed in below table using register.

Present State		Input	Next State		Output
A1	A2	X	A1	A2	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	0	0	1
1	0	0	1	0	0
1	0	1	0	1	0
1	1	0	1	1	0
1	1	1	0	1	1

Q.7 How many flip-flops needed for twisted-ring (Johnson) counter having 8 different states?

Q.8 How many flip-flops needed for ring counter having 8 different states?

Q.9 Design 3bit synchronous Up counter using T flip-flop.

Q.10 Design 3bit synchronous Down counter using T flip-flop.

Q.11 Design 3bit synchronous UP/Down counter using T flip-flop.

Q.12 Design 3bit asynchronous/ripple Up counter using T flip-flop.

Q.13 Design 3bit asynchronous/ripple Down counter using T flip-flop.

Q.14 Design 3bit asynchronous/ripple UP/Down counter using T flip-flop.

Q.15 Design synchronous Mod-5 UP counter.

Q.16 Design synchronous Mod-5 down counter.

Q.17 Design asynchronous Mod-5 UP counter.

Q.18 Design asynchronous Mod-5 down counter.

Q.19 Design counter which count n=binary sequence 1,4,2, 7 and repeat.

Q.20 Explain ring counter.

Q.21 Explain twisted ring counter (Johnson counter).

Sub: Digital Logic Design
Chap 3 (Q. Bank)

Q.1 What is sequential circuit?

Q.2 Differentiate combination and sequential circuit.

Q.3 Explain SR flip-flop with logic diagram.

Q.4 Explain JK flip-flop with logic diagram.

Q.5 Draw the circuit diagram of positive edge-triggered JK flip-flop and explain its operation with the help of a truth table.

Q.6 Derive characteristic equation for SR flip-flop.

Q.7 Obtain excitation table for SR flip-flop.

Q.8 Convert JK flip-flop to D flip-flop.

Q.9 Explain Master slave flip-flop.

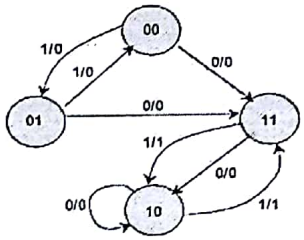
Q.10 What is race–around condition and how to avoid it?

Q.11 List out Steps for designing of sequential circuit.

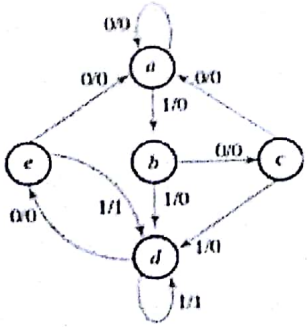
Q.12 Discuss the application of flip-flops.

Q.13 Definitions: state diagram, state table, flip-flop.

Q.14 Design sequential circuit from following state diagram.



Q.15 Obtain reduced state table and reduced state diagram for the sequential machine whose state diagram is shown in given figure.



Digital Logics Design

Question Bank (Chap-2)

Q.1	Explain design procedure of combinational circuit.
Q.2	Define / Write truth table and logical expression for following Combinational circuit. • Half adder • Full adder • Half Subtractor • Full Subtractor • Multiplexer (4x1) • De-multiplexer (1x4) • Encoder (4 to 2) or (2^n to n) • Decoder (3 to 8) or (n to 2^n)
Q.3	Design a full subtractor with two half subtractor and an OR gate.
Q.4	Explain Binary Parallel adder (BPA). Discuss carry propagation in BPA.
Q.5	Explain Binary Parallel subtractor (BPS).
Q.6	Explain Binary Parallel adder - subtractor.
Q.7	What is disadvantage of Binary Parallel adder? How it can be overcome?
Q.7	Design n-bit binary to gray code convertor. (n= 2,3,4)
Q.8	Design combinational circuit to convert BCD number to Excess-3.
Q.9	Design combinational circuit to detect the Decimal numbers 0, 1, 4, 6, 7, 8 in a 4-bit XS-3 code input.
Q.10	Design a combinational circuit that generates the 9′ complement of a BCD digit.
Q.11	Design a combinational circuit that accepts a three bit binary number and generates an output binary number equal to the square of the input number.
Q.12	Design a combinational circuit whose input is four bit binary number and output is the 2's complement of the input binary number.
Q.13	Write short note on 2 bit magnitude comparator.
Q.14	Write short note on 4 bit magnitude comparator.
Q.15	Explain working of Decoder with logical diagram,
Q.16	Explain working of Encoder with logical diagram,
Q.17	Construct 4x16 decoder with two 3x8 decoders.
Q.18	Design a BCD to decimal decoder.
Q.19	Explain BCD to 7-segment display decoder in common cathode configuration.
Q.20	Implement following Boolean function using Decoder. a) $F_1(a,b,c,d) = \sum(1,3,5,2,11,15)$and $F_2(a,b,c,d) = \sum(1,5,7,14,13)$ b) $F_1(a,b,c,d) = \sum(1,12,3,2,14,15)$and $F_2(a,b,c,d) = \sum(0,5,7,8,9)$ c) $F = x'y'z' + x'y'z + xy'z' + xy'z$ d) $F(w,x,y,z) = \prod(1,2,3,5,8,11,15)$ e) Full adder.
Q.21	What is difference between encoder and priority encoder?

Q.22	Implement 16:1 multiplexer using 4:1 multiplexers.
Q.23	Implement a full adder circuit using two 4:1 MUX. Discuss a few applications of Multiplexers.
Q.24	Implement following Boolean function using Multiplexer. a) $F_1(a,b,c,d) = \sum(1,3,5,2,11,15)$and $F_2(a,b,c,d) = \sum(1,5,7,14,13)$ b) $F = x'y'z' + x'y'z + xy'z' + xy'z$ c) $F(w,x,y,z) = \prod(1,2,3,5,8,11,15)$ d) Full adder.
Q.25	Implement following function using 4:1 multiplexer F(A,B,C)=Σ (1,3,4,6)
Q.26	Implement the following function using 8:1 multiplexer a) F(A,B,C,D)=Σ (2,4,5,7,10,14) b) F(A,B,C,D)=Π(0,2,4,6,8,10,12,14)
Q.27	What is de-multiplexer? Design 1:4 de-multiplexer with truth table and select line.
Q.28	Implement the following Boolean functions using ROM F1(A,B,C)= Σ (1,3,4,6) F2(A,B,C)= Σ (0,5,6,7) F3(A,B,C)= Σ (2,3,5,6)
Q.29	What is the minimum size of ROM to implement Full adder?
Q.30	Classification of ROM.
Q.31	Write a short note on Read Only Memory (ROM).
Q.32	Write a short note on Programmable Logic Array (PLA).
Q.33	Implement following Boolean function using PLA. a) $F_1(a,b,c,d) = \sum(1,3,5,2,11,15)$and $F_2(a,b,c,d) = \sum(1,5,7,14,13)$ b) $F_1(a,b,c,d) = \sum(1,12,3,2,14,15)$and $F_2(a,b,c,d) = \sum(0,5,7,8,9)$ c) $F_1(a,b,c) = \sum(1,4,5,7)$and $F_2(a,b,c) = \sum(1,4,5,6)$ d) $F = x'y'z' + x'y'z + xy'z' + xy'z$ e) $F(w,x,y,z) = \prod(1,2,3,5,8,11,15)$ f) Full adder.