6	Stod Sogned Sogn	Date	
	Working of circuit	Characteristice of ECLOS In In another	9
	The state of the s	(1) It is the fastest logic family	
	A B B B B B B B B B B B B B B B B B B B	The propogation allow is ly than	1na
sidan	mo 1800 70FF 0 0FF 0 1000	(2) Frankistons are not allowed to go	Into
The D	ON OFF ON O	Saturation mode so that logical	enels
	Transitional long of a stand of our said	ace kept close to each other.	
them	Experiment in a now wife on the state of the	(3) A logical levels are kept close t	to eac
1, a (1)	Provided 14th Alakante Ala Alaka 114 Dia Luciona	Other noise margin is reduc	ed Ep
1 1 2	RTL Circuit consists of Resistores & transistor	it is difficult to achieve good	1 nois
anno	The figure shoul 2 Input RTL NOR gate,	Such but a suintering out the interingues	
My rtage	emittle of both triansistal are connected to	(4) Another Idisaduantage of this ap)	proach
wholeding	a common ground by collectors of both.	ie that power consumption is more	e.
Hearthy	teransistor of are told through a	and to as I think of the second of the	
0	common collector Resistor Re to a supply	(a) Basic ECL Circuit of Invertor/ Buffer Circu	ult
	Voltage Vcc. The Relistor Re is commonly known as a pull up Resistor.	130 Mentione do 150 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
	known al Pull up Resistor	AND THE RESIDENCE OF THE PARTY	
~~~	2 de la companya della companya de la companya della companya dell	Regarded Raid Andrianolds	
(111)	Emitter Coupled Logic Family (ECL)	300 € 300 · 2 \ Out1	
	The TTL family uses toronsistors operating	VIN N 00t2	
4.	in saturation mode, As a everelt, there	02	
Sat norma	suttering speed is limited by storage	TI O L. PA NO.	
Stakes tis	a delay time alsociated with Iransistor.		0.0
in ECL to	I delay time associated with Translitor. I That is deiven into the Saturation. Prother logic family has been developed	FCI ou for More Company to the company of the compa	(11)
Satuzathmed	e prother logic family has all developed	SLOVE & RE	
	that prevents transition lateration thereby	Tricking and that I was The E-ON	
3(9)	inculating overall suitching speed. This	VIN - Imput of Circuit	
14/6	Jogic family is capled Emiller Coupled yransister. Ett de subted mode coupled	Out 1- Output of Invertor NOT gate	
hara o	granditure, etter ou turbunt nywood coupled	Out 2 + Output of Buffer Corcuit	
HAD A	Logic family	Voltage level required at Input side	0
		hogic 1 - 4.40 the at Imput side.	Ó
		Logico 3.6 V	