Working of circuit

A	B	Q_1	Q_2	Y = Output
0	0	OFF	OFF	1
0	1	OFF	ON	0
1	0	ON	OFF	0
1	1	ON	ON	0

RTL Circuit consists of Resistors & transistor. The figure shows 2 Input RTL NOR gate. emitters of both transistor are connected to a common ground. & collectors of both transistor Q1 & Q2 are tied through a common collector Resistor R_C to a supply voltage V_{CC}. The Resistor R_C is commonly known as Passive pull up Resistor.

(iii) Emitter coupled logic family (ECL)

The TTL family use transistors operating in saturation mode. As a result, there switching speed is limited by storage delay time associated with Transistor. That is driven into the saturation.

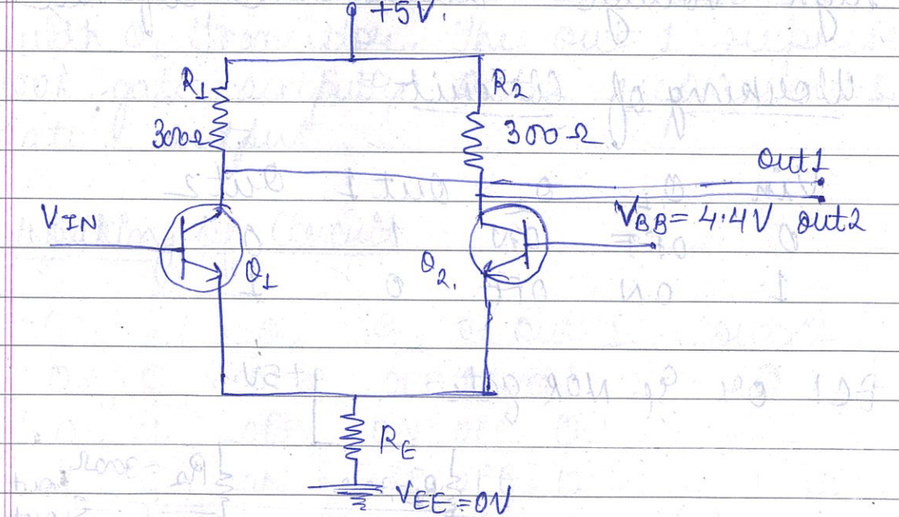
Another logic family has been developed that prevents transistor saturation thereby increasing overall switching speed. This logic family is called Emitter coupled Transistor. [ECL] or ~~current~~ mode coupled logic family.

Sat → normal mode mode It takes time so we stop in ECL to go it into Saturation mode

Characteristics of ECL:

(1) It is the fastest logic family.
(2) The propagation delay is less than 1 nanosec-end.
(2) Transistors are not allowed to go into Saturation Mode. So that logical levels are kept close to each other.
(3) As logical levels are kept close to each other, noise margin is reduced & it is difficult to achieve good noise immunity.
(4) Another disadvantage of this approach is that power consumption is more.

(a) Basic ECL Circuit of Inverter / Buffer Circuit



V_{IN} → Input of Circuit
Out 1 → Output of Inverter NOT gate
Out 2 → Output of Buffer Circuit
Voltage level required at Input side:
Logic 1 → 4.4V
Logic 0 → 3.6V