VERA SoM Development kit

User Guide Datasheet

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Autor	Date	Modifications
LBO	07/06/2024	Initialisation

Chapter 1: Kit Overview & Setup

1.1. Hardware

The hardware kit is delivered assembled, pre-programmed with a demo application and is composed of the following components:

- VERA SoM carrier board
- VERA SoM
- HDMI Extension daughter board
- GPIO Extension daughter board
- MIPI Extension daughter board
- UART to USB converter dongle
- IMX327 Sensor proxy board
- USB-C cable

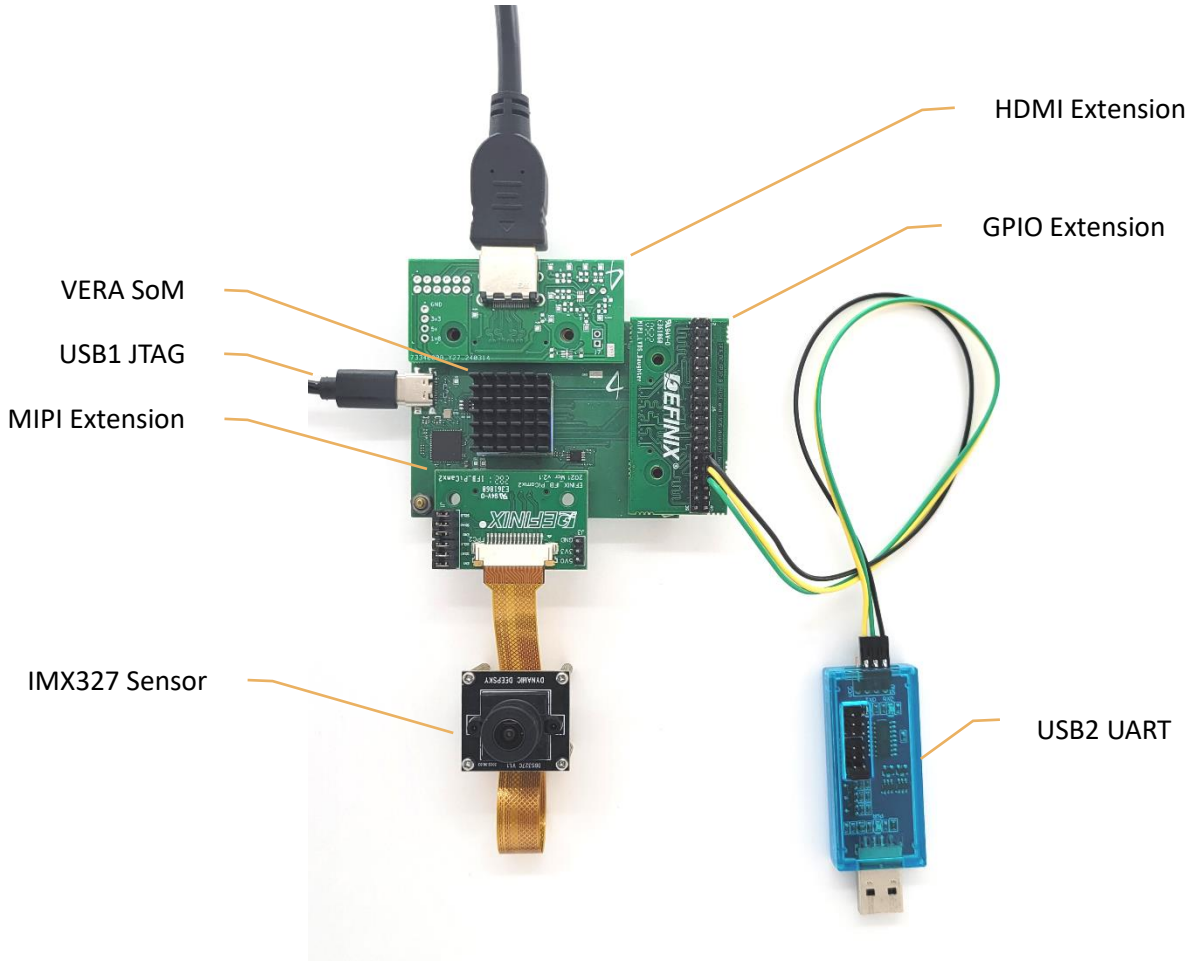


Figure 1 : Hardware setup overview

1.2. Gateware

VERA is delivered with a system on chip ready for edge AI applied to vision.

This includes the following components

- ISP for computer vision tasks
- NPU for AI function acceleration
- RISC-V for control and additional processing
- MIPI-CSI interface with image sensor
- HDMI interface with display

An overview of the SoC is presented below

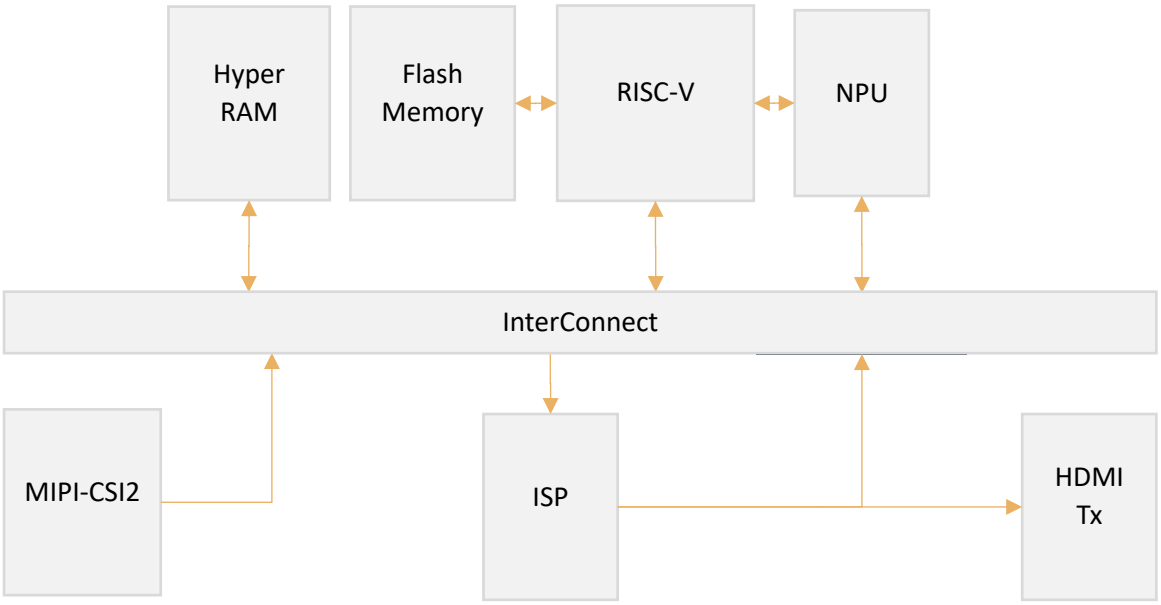


Figure 2 : System On Chip overview

1.2.1. ISP features

The Image Signal Processor includes sensor debayering, color gain correction, gamma correction and image downscale. A detail view of the ISP dataflow is given below

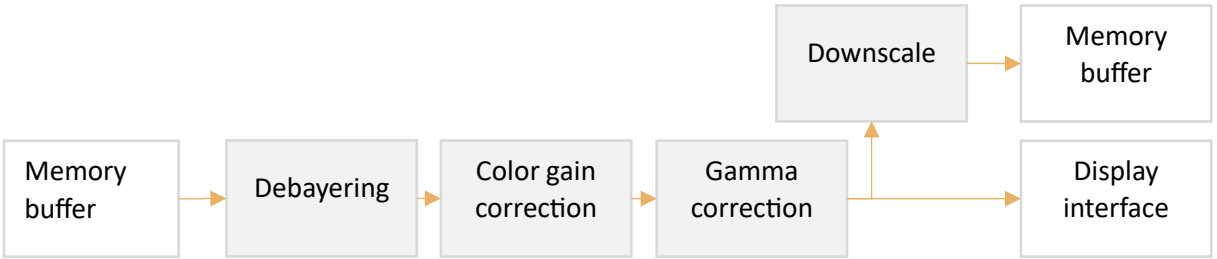


Figure 3 : ISP overview

1.2.2. NPU features

The Neural Processing Unit includes hardware accelerators for the following operations

- 2D Convolution
- 2D DepthWise Convolution
- 2D Addition

1.3. Software

A Software example design is provided as quick-start developing template. This software is based on a standard C/C++ Eclipse IDE.

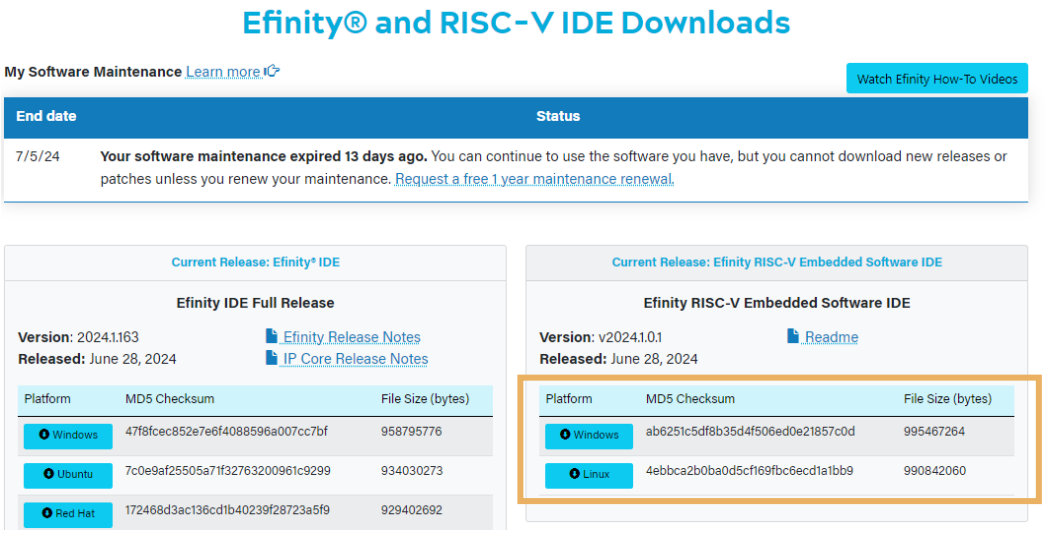
1.3.1. USB driver installation

To enable communication between host computer and FTDI programming interface a USB driver update must be conducted. Download Zadig software (version 2.7 or later) from zadig.akeo.ie.

- Connect the board to your computer with the appropriate cable and power it up.
- Run Zadig software.
- Choose **Options** -> **List All Devices**.
- Repeat the following steps for each of 4 interfaces.
    - Select **libusb-win32** in the **Driver** drop-down list.
    - Click **Replace Driver**
- Close Zadig software.

1.3.2. RISC-V IDE installation

Download and install Efinity RISC-V from Efinix support center, you may be invited by Efinix to create an accompt.

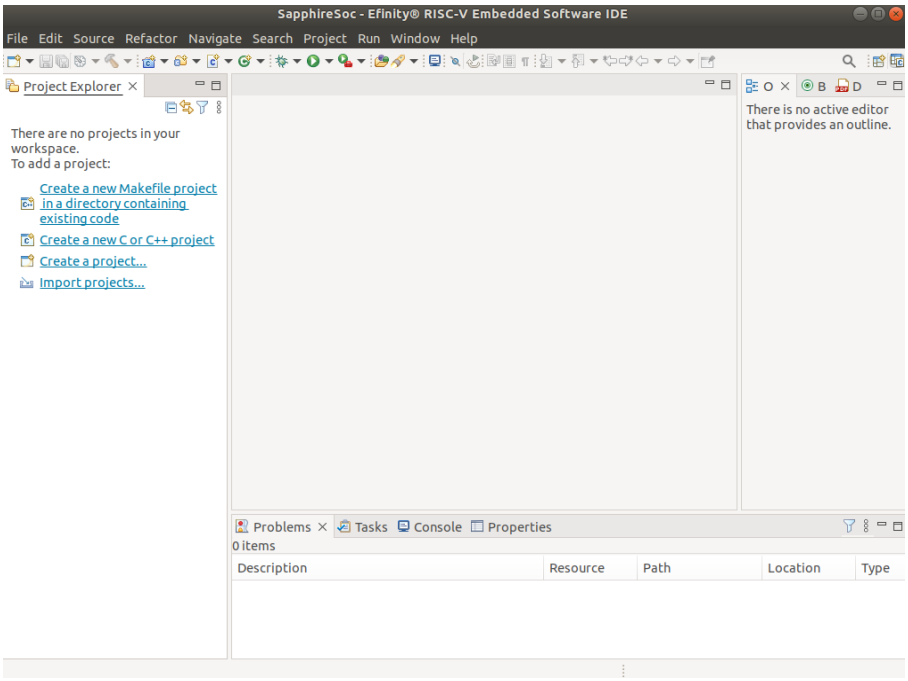


1.3.3. Project setup

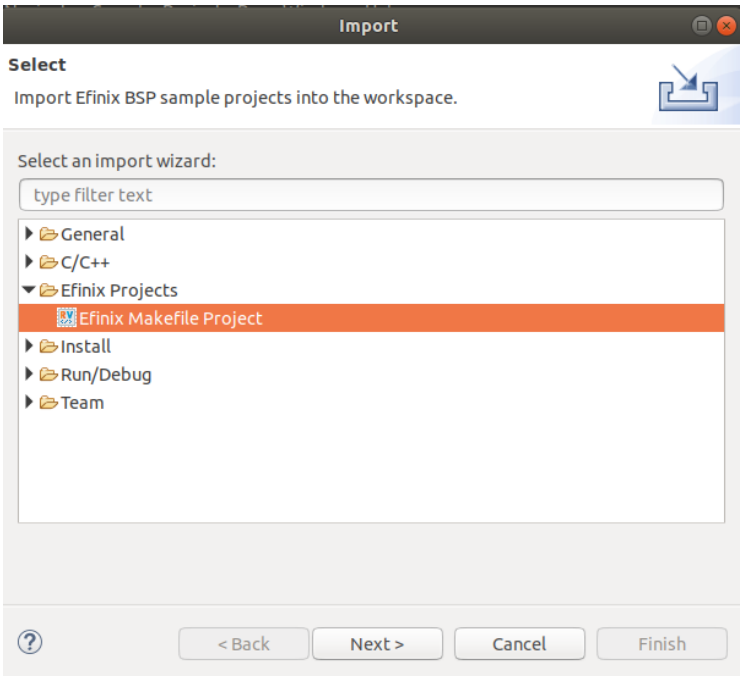
To setup the VERA SOM demo project, download the project archive

Open Efinity RISC-V IDE in the workspace path choose *[your_location]/VERA-SoM-AI-SDK/sw_workspace/VERASoc.*

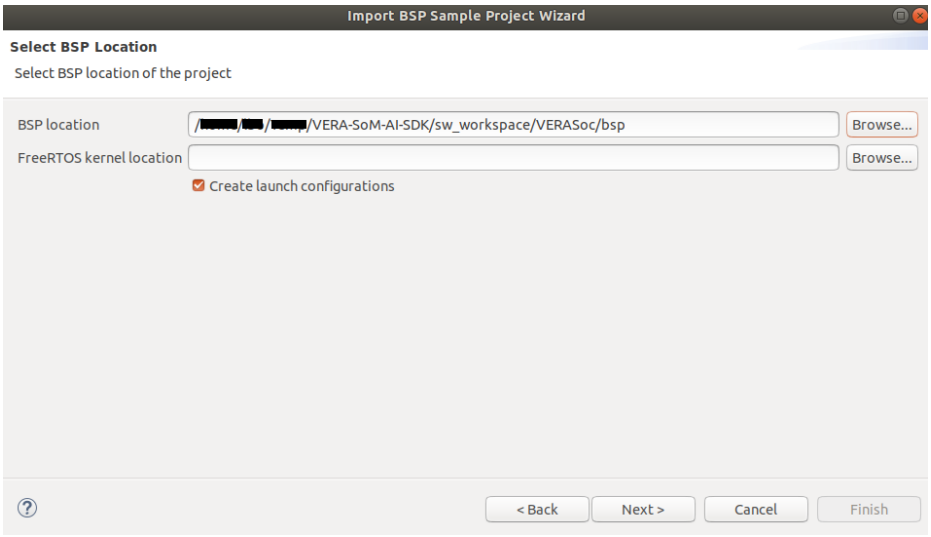
The Ide should open-up as follow



Next, load the project template by selecting File -> import -> Efinix Makefile Project.



Select “Next”, on the following page, in the BSP location enter the following path : *[your_location]/VERA-SoM-AI-SDK/sw_workspace/VERASoc/bsp/Efinix*



Select “Next” and tick the “evsoc_tinyml_ypd” in the drop-down list.

Your C/C++ project is now set.

Chapter 2: Demo overview

A demo application that runs a person detection is factory flashed on the SoM. The application starts automatically on power-up.

- Connect USB1 terminal to a host computer
- Open Putty or any other serial manager tool and select the COM port.
- Connect HDMI terminal to a screen
- Connect USB2 terminal to a host computer, this will power up the board

The HDMI will display the video feed from the image sensor, bounding boxes from person detection appear as on-screen overlay. You can see the detection feedback through the UART interface.

Chapter 3: Designing with the kit

3.1. C/C++ design flow

[This section is under build]

3.2. AI design flow

The following section explain how to run your own model on VERA platform.

At the moment, this application needs Ubuntu 18.04 or later version.

Under *[your_location]/VERA-SoM-AI-SDK/ai_workspace*, start the *run_ai_parser* application. Click on “Open” and select the tflite file of the model.

Click on “Generate”, the model will be analyzed, the results are available in the newly create “output” folder. The tool will create 4 files:

- Define.cc
- Define.h
- [model_name]_data.cc
- [model_name]_data.h

Copy these files in your C/C++ project under

*[your_location]/ VERA-SoM-AI-SDK/*sw_workspace/VERASoc/software/standalone/evsoc_tinyml_ypd/src/model

3.3. Application flash deployment

[This section is under build]