(Please write your Exam Roll No.) *Exam Roll No.* 032/4202015

END TERM EXAMINATION

THIRD SEMESTER [BCA] NOVEMBER-DECEMBER 2017

Paper Code: BCA-203 ***Subject: Computer Architecture***

Time: 3 Hours ***Maximum Marks: 75***

Note: Attempt any five questions including Q.no.1 which is compulsory. Select one question from each unit.

Q1 (a) Explain instruction set completeness. Is the Instruction set of the Basic Computer Complete? Justify your answer.
(b) Explain Direct Memory Access (DMA).
(c) Explain the various difficulties encountered in an instruction pipeline. Also explain how these can be avoided.
(d) Explain associative memory and how it function.
(e) Design a 4 bit Adder-Subtractor. **(5x5=25)**

Unit-I

Q2 (a) Explain the operation of a 4 bit Arithmetic Circuit. **(7.5)**
(b) Explain Instruction cycle. **(5)**

Q3 (a) The outputs of 4 registers R0, R1, R2, R3 are connected through 4 to 1 multiplexer to the input of a fifth register R5. Each register is 8 bits long. The following transfer are dictated by four timing variables T0, T1, T2, T3 as follows:

T0: R5 <- R0
T1: R5 <- R1
T2: R5 <- R2
T3: R5 <- R3

The timing variables are mutually exclusive that means only one can be active at one time while the remaining three are 0. Draw the block diagram showing the transfers. **(7.5)**

(b) The content of the AC in the Basic Computer is hexadecimal A937. The initial value of E is 1. Determine the contents of AC, E, PC, AR & IR in hexadecimal after the execution of the CLA instruction. Repeat 11 times more starting from each register reference instruction. The initial value of PC is hexadecimal 021. **(5)**

Unit-II

Q4 (a) Explain the various types of Instruction Formats. **(7.5)**
(b) Explain Instruction pipeline. **(5)**

Q5 (a) Explain the various Addressing Formats in detail. **(7.5)**
(b) Explain memory interleaving. **(5)**

Unit-III

Q6 (a) Construct a 4x4 Array Multiplier. **(7.5)**
(b) Explain the working of a First in First Out Buffer. **(5)**

P.T.O.

Q7 (a) Draw a flowchart for Booth Multiplication. **(7.5)**
(b) Explain Asynchronous Serial Transfer in detail. **(5)**

Unit-IV

Q8 (a) A virtual memory has address space of 8K words, memory space of 4K words & page & block sizes of 1K words. The following page reference occur at a given time:
4 2 0 1 2 6 1 4 0 1 2 3 5 7
Determine which 4 pages are there in main memory using LRU & FIFO strategy. **(7.5)**
(b) What is the purpose of a cache memory? Explain its Writing policies. **(5)**

Q9 What is Virtual Memory? Why is it required? Explain Logical to physical address mapping using segment and page table with the help of an example. **(12.5)**

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