(Please write your Exam Roll No.) *Exam Roll No.* 04121402015

END TERM EXAMINATION

THIRD SEMESTER [BCA] DECEMBER 2016

Paper Code: BCA-203	*Subject: Computer Architecture*
Time: 3 Hours	*Maximum Marks: 75*

Note: Attempt any five questions including Q.no.1 which is compulsory. Select one question from each Unit.

Q1 Answer **any ten** of the following: **(2.5x10=25)**

(a) Show the hardware that implements the following statement. Include the logic gates for the control function and a block diagram for the binary counter with account enable input.

$$xyT_0 + T_1 + yT_2: AR \leftarrow AR + 1$$

(b) Register A holds the 8-bit binary 11011001. Determine the B operand and the Logic microoperation to be performed in order to change the value of A to 01101101?

(c) Justify or refute the statement clearly, citing examples "Code written in RTL helps us to design digital systems systemically."

(d) A digital computer has a common bus system for 12 registers of 9 bits each. The bus is constructed with multiplexers. How many multiplexers are there in the bus and what is the size of multiplexers?

(e) Determine the number of clock cycle that it takes to process 200 tasks in a six segment pipeline.

(f) Discuss delayed load or delayed branch with example.

(g) What is the purpose of pipelining?

(h) How a subroutine call is different from branching?

(i) Consider an instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1contains the number 200. Evaluate the effective address if the addressing mode of the instruction is Direct.

(j) What are the various schemes used for Data Transfer between processor and I/O Devices?

(k) Explain the difference between hardwired control and micro programmed control? What is the advantage of the later over first?

(l) Why I/O interface is required?

(m) Assume that a processor receives an interrupt request and DMA request at the same time. Which request does the processor process first? Why?

(n) What is the different between isolated I/O and memory mapped I/O? What are the advantages and disadvantages of each?

(o) Formulate a mapping procedure that provides eight consecutive microinstructions for each routine. The operation code has six bits and the control memory has 2048 words.

(p) Explain relevance of memory interleaving in pipelining/vector processing.

(q) How many 128x8 memory chips are needed to provide a memory capacity of 4096x16?

Unit-I

Q2 (a) Design an arithmetic circuit with one selection variable S and two n-bit data inputs A and B. The circuit generates the following four arithmetic

operations in conjunction with the input carry C_{in}. Draw the logic diagram for the first two stages. **(5)**

S	Cin = 0	Cin = 1
0	D = A + B	D = A + 1
1	D = A – 1	D = A + B' + 1

(b) With the help of flow chart, explain the sequence of steps for an instruction cycle. How does an interrupt change in sequence of events? **(5)**

(c) Write Microoperation for ISZ operation. **(2.5)**

Q3 (a) Draw a diagram of the bus system for four register of four bits using three-state buffers and decoders instead of multiplexers? **(5)**

(b) Design bi-directional shift register with parallel load. **(5)**

(c) The memory unit of a computer has 256 K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers and an address parts.

(i) Specify the instruction format and the number of bits in each field if the instruction is in one memory word. **(1.5)**

(ii) How many bits are there in data and address input of the memory? **(1)**

Unit-II

Q4 (a) Design a micro program sequencer and explain its working. **(5)**

(b) Write a program to evaluate the arithmetic statement $X = (A + B) * (C + D)$. **(7.5)**

(i) Using a general register computer with three address instruction.

(ii) Using a general register computer with two address instruction.

(iii) Using an accumulator type computer with one address instructions.

(iv) Using a stack organized computer with zero address instructions.

Q5 (a) Discuss various Addressing Modes with examples. **(8)**

(b) Explain four possible hardware schemes that can be used in an instruction pipeline in order to minimize the performance degradation caused by instruction branching. **(4.5)**

Unit-III

Q6 (a) What is the advantage of using interrupt initiated data transfer over transfer under program control without an interrupt? **(2.5)**

(b) Using Booths algorithm, illustrate the sequence of steps in a tabular fashion, when 11101 is multiplied with 10111. **(5)**

(c) A commercial interface unit uses different names for the handshake lines associated with the transfer input handshake lines associated with the transfer of data from the I/O device into the interface unit. The interface unit handshake line is labeled STB (strobe), and the interface output handshake line is labeled IBF (input buffer full). A low-level signal on STB loads data from the I/O bus into the interface data register. A full high-level signal on IBF indicates that the data item has been accepted by the interface. IBF goes low after an I/O read signal from the CPU when reads the contents of the data register.

P.T.O.

(i) Draw a block diagram showing the CPU, the interface, and the device together with the pertinent interconnection among the th units.
(ii) Obtain a sequence-of-events flowchart for the device to interface and from the interface to the CPU.

Q7 (a) Explain in details Daisy Chain priority interrupt Scheme.
(b) Explain DMA transfer in a computer system.

Unit-IV

Q8 (a) What do you mean by Cache memory? Explain in detail mapp procedures used while considering organization of Cache Memory?
(b) Explain virtual memory segment and memory table for mappin virtual address.

Q9 (a) Discuss mapping in segment page memory management unit.
(b) Discuss Associative memory in details.
(c) An address space is specified by 24-bits and the correspond memory space by 16-bits.
(i) How many words are there in the address?
(ii) How many words are there in memory space?
(iii) If a page consist of 2K words, how many pages and blocks there in the system?

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