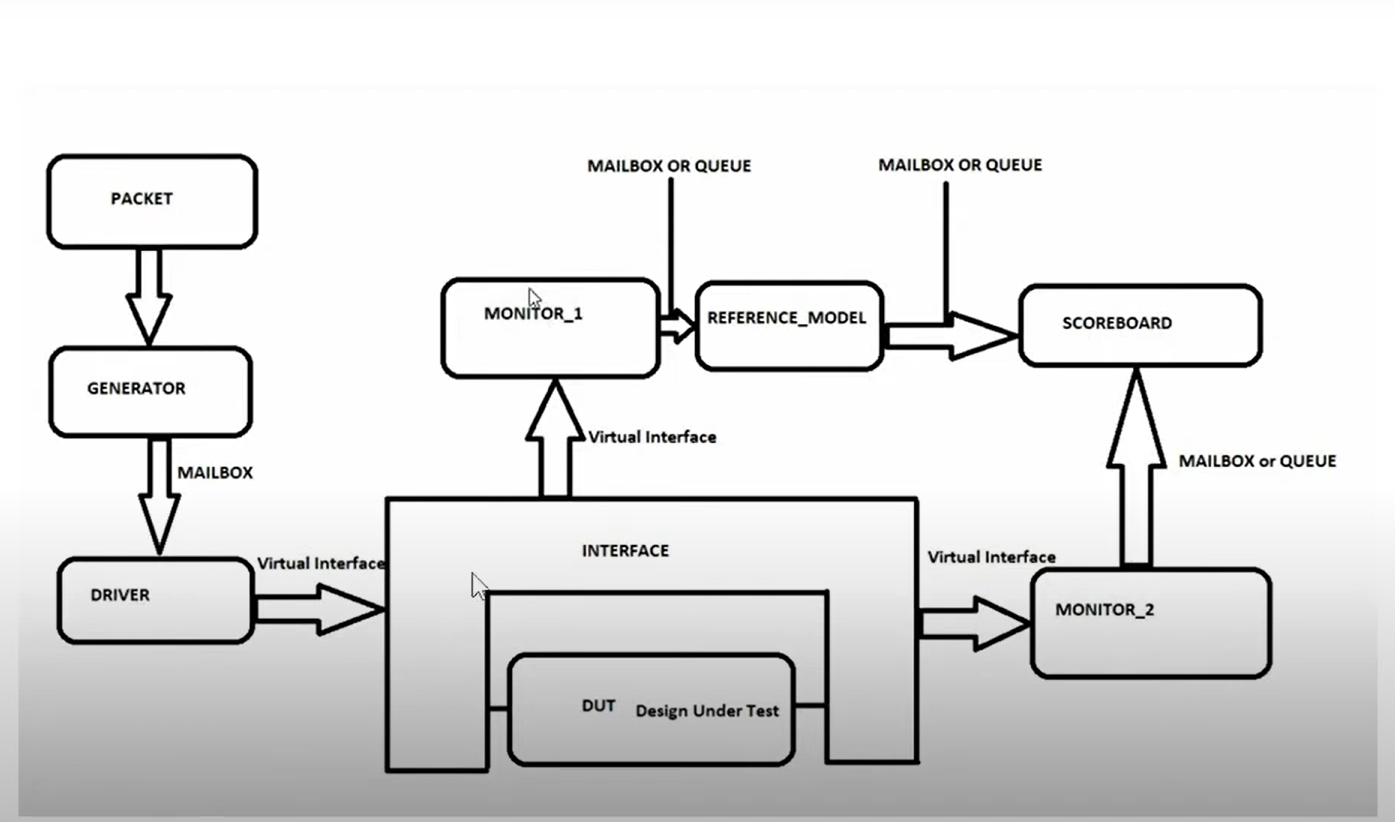
OUTPUT:



When reset =1, Enable =1 completely and when ,Write =1 in address b we are storing data d

When write =0,Read=1 in address b we are getting same data as d

Now performing Read Write operation

Now Writing the data keeping logic high for sometime logic 1 in address 3 we are writing data C4 after some time we are performing write =0 and read =1 in address 3 the data will be showed is C4 , the data will be displayed after next clock for the proper input delay is given in the environment as #10 and #20 and #20.

