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CS 520–03
Homework 2
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1 Propose the format of an entry in the LSQ and the conditions for issuing a LOAD and a STORE instruction. Assuming that registers are 64 bits wide and all LOAD and STORE instructions to have a 10-bit literal operand, what is the size of an individual LSQ entry in bits?

An entry in the LSQ will need slots for the source and destination registers, one of which will be used by the LSFU to calculate the effective memory address. A further 10 bits are used to store the third literal operand, and we need to include 1 bit to identify the entry as either a LOAD or a STORE operation as well as another single bit to mark whether the entry is ready for issue to the functional unit. A STORE will be ready for issue once the value in its second operand is known. A LOAD will be ready once the location of its second operand can be calculated. Altogether, an entry like this will require 140 bits.

2 Assume that a separate register file is used to hold the architectural registers. For this problem, assume that the most recent instances of registers R0 through R7 are represented by physical registers P0 through P7 and all of these physical registers contain the proper values.

2a Show the contents of the rename table after all instructions in the above code fragment are dispatched.

R0	P0
R1	P29
R2	P22
R3	P25
R4	P28
R5	P5
R6	P27
R7	P7

2b What are the contents of FPRL, LSQ and IQ immediately after dispatching the MUL instruction? You need to make sure that instruction issue, execution and writebacks are accounted for. Assume a one-cycle writeback delay and a one-cycle delay for moving a ready instruction (which has been selected for issue) to the function unit. Assume further that a physical register is freed up as soon as ALL of its consumers have been forwarded its value AND when it is no longer the most recent instance of the architectural register that it is currently associated with.

- FPRL

P30
P31
P32
P33
P34
P35
P36
P37
P38
P39
P40
P41
P1
P2
P21
P4
P3
P24
P6
P26
P23

- LSQ

  The load store queue is empty. The last store has just been issued.

- IQ

  The issue queue contains instruction six, SUB, instruction seven, ADD, and the MUL just dispatched.

3 Assume the following....

3a Show the contents of the (front-end) rename table and the back-end rename table (R-RAT) after all instructions in the above code fragment are dispatched.

Front end:

R0	P0
R1	P29
R2	P22
R3	P25
R4	P28
R5	P5
R6	P27
R7	P7

Back end:

R0	P9
R1	P21
R2	P22
R3	P20
R4	P7
R5	P19
R6	P6
R7	P8

3b What are the contents of FPRL, LSQ and IQ immediately after dispatching the MUL instruction? You need to make sure that instruction issue, execution and writebacks are accounted for. Assume a one cycle writeback delay and a one cycle delay for moving a ready instruction (which has been selected for issue) to the function unit. Assume that a physical register is freed up as soon as it's no longer the most recently committed instance of the associated architectural register.

1. FPRL

P30
P31
P32
P33
P34
P35
P36
P37
P38
P39
P40
P41
P2
P4
P1
P8
P3
P19
P9
P0
P7
P6

2. LSQ and IQ as above.