

EXPERIMENT - 9

Asynchronous Counter

AIM: Implementation of 2, 3, 4 Asynchronous up/down counters.

SOFTWARE: NI Multisim / circuit verbe

Requirement - IC trainer kit, Patch cords, IC 7476

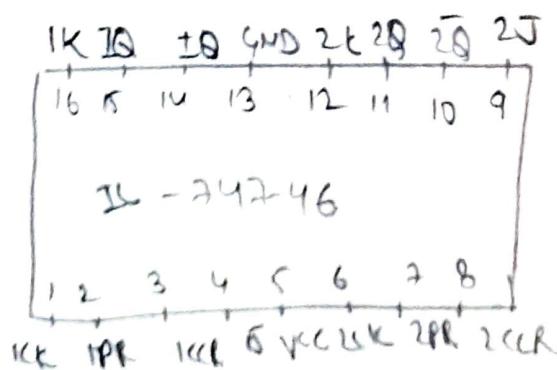
THEORY ASYNCHRONOUS COUNTERS

In this counter, flip-flops are connected in such a way that output of first clock drives clock for the next flip-flop.

All the flip-flop are not clocked simultaneously logic circuit is very simple even for more numbers of states.

Main drawback of the counter is their low speed as the clock is propagated through no. of flip-flops before it reaches that flip-flop.

PIN - CONFIGURATION

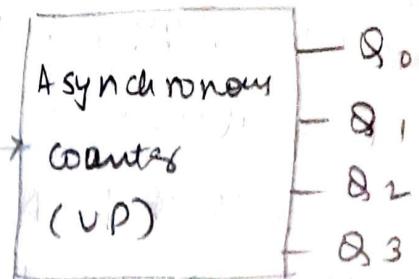


4-Bit - Asynchronous up-Counter

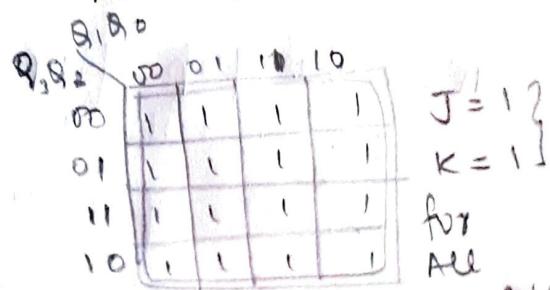
TRUTH TABLE For All 4-bit inputs

PS	NS	J	K
Q ₃ Q ₂ Q ₁ Q ₀	Q ₃ Q ₂ Q ₁ Q ₀	J	K
0 0 0 0	0 0 0 1	t	t
0 0 0 1	0 0 1 0	t	t
0 0 1 0	0 1 1 1	t	t
0 0 1 1	0 1 0 0	t	t, CLR
0 1 0 0	1 0 1 1	t	t
0 1 0 1	0 1 1 0	t	t
0 1 1 0	0 1 1 1	t	t
0 1 1 1	0 0 0 0	t	t
1 0 0 0	1 0 0 1	t	t
1 0 0 1	1 0 1 0	t	t
1 0 1 0	1 0 1 1	t	t
1 0 1 1	1 1 0 0	t	t
1 1 0 0	1 1 0 1	t	t
1 1 0 1	1 1 1 0	t	t
1 1 1 0	1 1 1 1	t	t
1 1 1 1	0 0 0 0	t	t

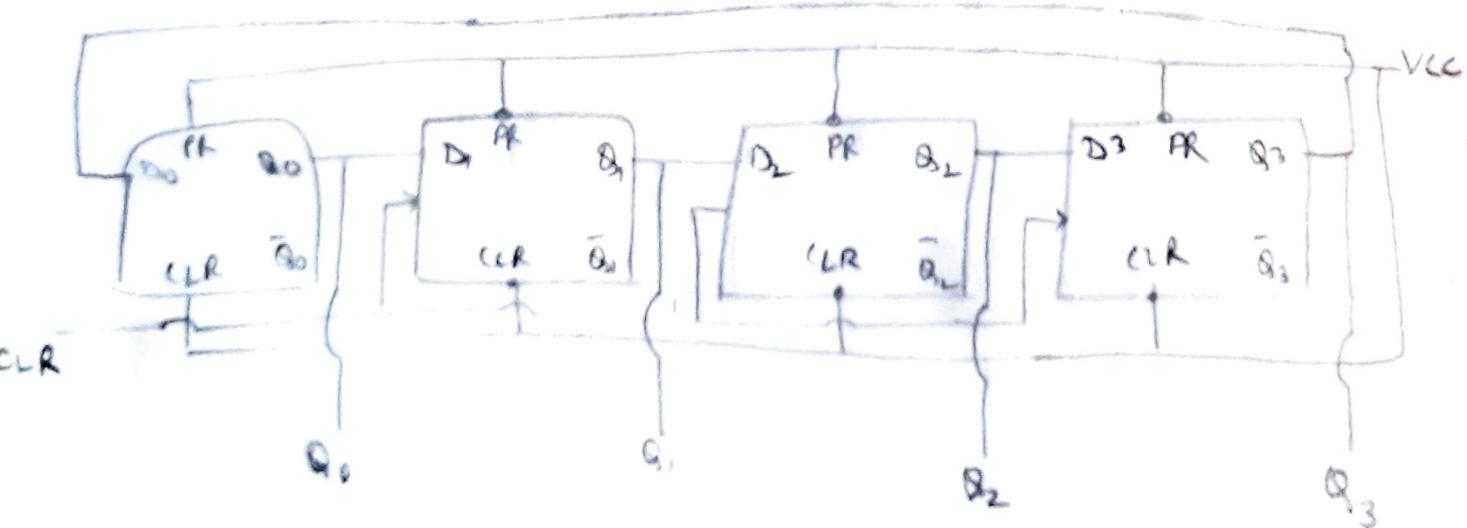
LOGIC DIAGRAM



K-MAP

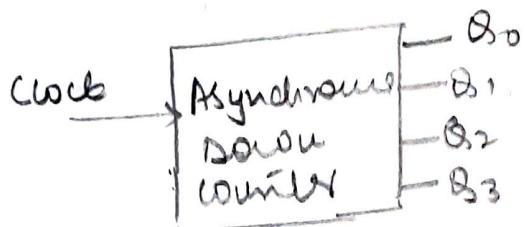


CIRCUIT DIAGRAM



4-Bit Asynchronous Down Counter

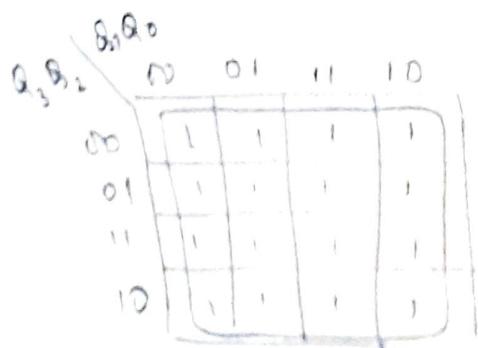
LOGIC DIAGRAM



TRUTH TABLE

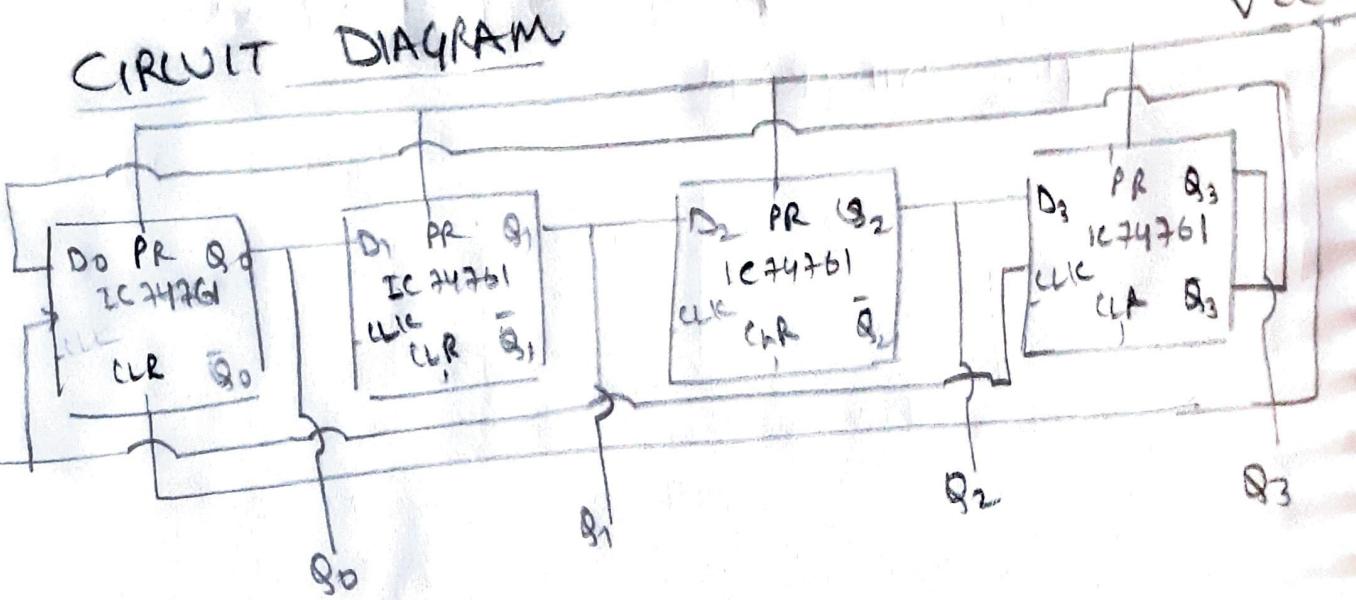
PS	NQ				for all 4				
Q_3	Q_2	Q_1	Q_0	Q_3	Q_2	Q_1	Q_0	J	K
0	0	0	0	1	1	1	1	1	1
0	0	0	1	0	0	0	0	1	1
0	0	1	0	0	0	0	1	1	1
0	0	1	1	0	0	1	0	1	1
0	1	0	0	0	0	1	1	1	1
0	1	0	1	0	1	0	0	1	1
0	1	1	0	0	1	0	1	1	1
0	1	1	1	0	1	1	0	1	1
1	0	0	0	0	1	1	1	1	1
1	0	0	1	1	0	0	0	1	1
1	0	1	0	1	0	0	1	1	1
1	0	1	1	1	0	1	0	1	1
1	1	0	0	1	0	1	0	1	1
1	1	0	1	1	1	0	0	1	1
1	1	1	0	1	1	1	0	1	1
1	1	1	1	1	1	1	1	1	1

* K-MAP



$J=1 \quad \{$ for all JK-PF
 $K=1 \quad \}$

CIRCUIT DIAGRAM



CONCLUSION

In this LAB we implemented 2, 3, 4 Asynchronous up/down counters using JK-flip-flops.

EXPERIMENT - 10

SYNCHRONOUS COUNTERS

AIM - Synchronous counters (up & down) Implementation of 2, 3 or 4 bit using J-K flip-flop.

REQUIREMENT - ICL7676, Patch cords, J-K flip flop (IC 7676)

SOFTWARE - Multisim / Circuit Venn

THEORY flip-flop

flip-flop is a sequential circuit driven by clock input either by positive edge. It is a binary storage device capable of storing one of information.

The flip-flop are of various types. Their characteristic can be easily seen from their truth table.

PRESERVE & CLEAR

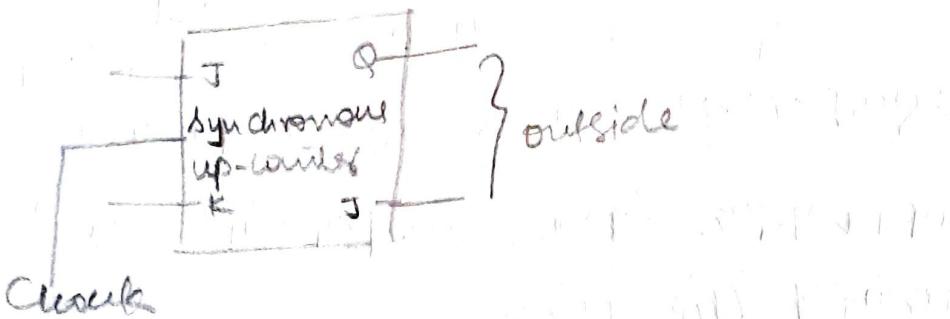
When power is turned on the state of flip-flop is uncertain. It may come to set ($Q=1$) or reset ($Q=0$) state. In many applications it is necessary to initially set or reset the flip-flop. These inputs are preset (\bar{P}) and clear (\bar{C}). They can be applied at anytime b/w clock pulses and are not in synchronism with clock.

PIN CONFIGURATION

K	Q	\bar{Q}	GND	2K	2Q	$\bar{2Q}$	I ₁
16	15	14	13	12	11	10	9
IC 7476							
22	3	4	5	6	7	8	
R	I _C	I _R	I _S	V _{CC}	2CK	2P	2CLR

2, 3, 4 Bit Synchronous Up Counter -

LOGIC DIAGRAM



Excitation table:

Previous State	New State	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

TRUTH TABLE

PS	NS	Q ₃	Q ₂	Q ₁	Q ₀	Q ₃	Q ₂	Q ₁	Q ₀	J ₀	k ₀	J ₁	K ₁	J ₂ K ₂	J ₃ K ₃	
0000	0000	0	0	0	0	0	1	1	1	X	0	X	0	X	0	X
0000	0001	0	0	1	0	0	1	0	X	1	X	1	X	0	X	0
0000	0010	0	0	1	1	0	1	1	1	X	1	X	0	X	0	X
0000	0011	0	0	1	1	0	1	1	1	X	1	X	1	X	0	X
0000	0100	0	0	1	0	1	0	1	0	X	1	X	0	X	0	X
0000	0101	0	0	1	0	1	0	1	0	X	1	X	0	X	0	X
0000	0110	0	0	1	0	1	1	1	1	X	1	X	0	X	0	X
0000	0111	0	0	1	0	1	1	1	1	X	1	X	1	X	0	X
0000	1000	0	0	1	1	0	1	0	1	X	1	X	0	X	0	X
0000	1001	0	0	1	1	0	1	0	1	X	1	X	1	X	0	X
0000	1010	0	0	1	1	1	1	1	1	X	1	X	0	X	0	X
0000	1011	0	0	1	1	1	1	1	1	X	1	X	1	X	0	X
0000	1100	0	0	1	1	0	0	1	0	X	1	X	0	X	0	X
0000	1101	0	0	1	1	0	0	1	0	X	1	X	1	X	0	X
0000	1110	0	0	1	1	1	1	1	1	X	1	X	0	X	0	X
0000	1111	0	0	1	1	1	1	1	1	X	1	X	1	X	0	X

K-MAP

$Q_1 Q_2$

$Q_3 Q_0$	00	01	11	10
00	1	x	x	1
01	1	x	x	1
11	1	x	x	1
10	1	x	x	1

$$J_0 = 1$$

$Q_3 Q_0$	00	01	11	10
00	x	1	1	x
01	x	1	1	x
11	x	1	1	x
10	x	1	1	x

$$K_0 = 1$$

$Q_1 Q_0$

$Q_3 Q_2$	00	01	11	10
00	0	1	x	x
01	0	1	x	x
11	0	1	x	x
10	0	1	x	x

$$B_1 = Q_0$$

$Q_1 Q_0$

$Q_3 Q_2$	00	01	11	10
00	0	0	1	0
01	x	x	x	x
11	x	x	x	x
10	0	0	1	0

$$J_2 = Q_1 Q_2$$

$Q_1 Q_0$

$Q_3 Q_2$	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	x	x	x	x
10	x	x	x	x

$$J_3 = Q_2 Q_1 Q_0$$

$Q_0 Q_1$

$Q_3 Q_2$	00	01	11	10
00	x	x	1	y
01	x	x	1	x
11	x	x	1	x
10	x	x	1	x

$$K_1 = Q_0$$

$Q_2 Q_0$

$Q_3 Q_2$	00	01	11	10
00	x	x	x	x
01	0	0	1	0
11	0	0	1	0
10	y	y	x	x

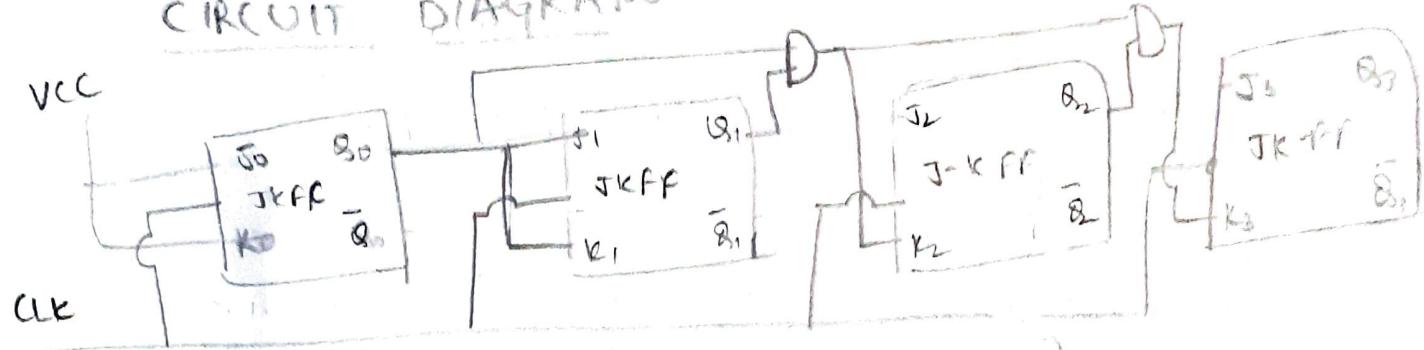
$$K_2 = Q_1 Q_0$$

$Q_1 Q_0$

$Q_3 Q_2$	00	01	11	10
00	x	x	x	x
01	x	x	x	x
11	0	0	1	0
10	0	0	0	0

$$K_3 = Q_2 Q_1 Q_0$$

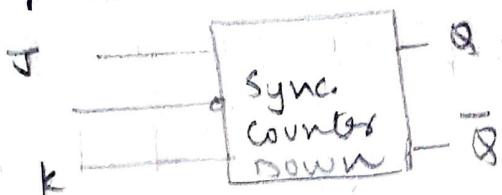
CIRCUIT DIAGRAM



four bit synchronous counter (up)

2, 3, 4 Bit Synchronous Counter (Down)

LOGIC DIAGRAM.



EXCITATION TABLE

P S	N S	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Truth Table

P S	N S	J ₀	K ₀	J ₁	K ₁	J ₂	K ₂	J ₃	K ₃
0 0 0 0	1 1 1 1	1	X	1	X	1	X	1	X
0 0 0 1	0 0 0 0	X	1	0	X	0	X	0	X
0 0 1 0	0 0 0 1	1	X	X	1	0	X	0	X
0 0 1 1	0 0 1 0	X	1	X	0	0	X	0	X
0 1 0 0	0 0 1 1	1	X	1	X	X	1	0	X
0 1 0 1	0 1 0 0	X	1	0	X	X	0	0	X
0 1 1 0	0 1 0 1	1	X	X	1	0	X	0	X
0 1 1 1	0 1 1 0	X	1	X	0	0	X	0	X
1 0 0 0	0 1 1 1	1	X	1	X	1	X	1	X
1 0 0 1	1 0 0 0	X	1	0	X	0	X	X	0
1 0 1 0	1 0 0 1	1	X	X	1	0	X	X	0
1 0 1 1	1 0 1 0	X	1	X	0	0	Y	X	0
1 1 0 0	1 0 1 1	1	X	1	X	X	1	X	0

1101	1100	X1	0X	X0	X0
1110	1101	1X	X1	X0	X0
1111	1110	X1	X0	X1	X0

K-MAP

Q ₃ Q ₂	00	01	11	10
00	1	X	X	1
01	1	X	X	1
11	1	X	X	1
10	1	X	X	1

$$J_0 = 1 \\ K_0 = 1$$

Q ₃ Q ₂	00	01	11	10
00	0	0	X	1
01	1	0	X	1
11	1	0	X	1
10	1	0	X	1

$$J_1 = \bar{Q}_0 \\ K_1 = Q_{10}$$

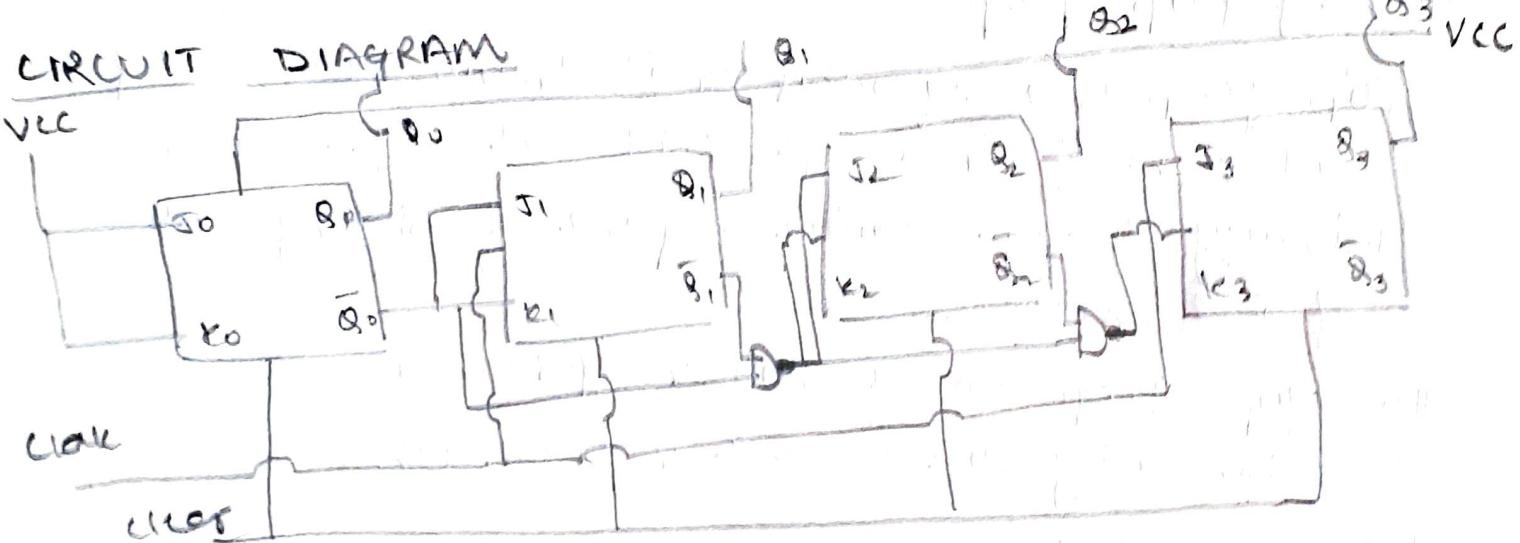
Q ₃ Q ₂	00	01	11	10
00	0	0	0	0
01	X	X	X	X
11	X	X	X	X
10	0	0	0	0

$$J_2 = \bar{Q}_1 \bar{Q}_0 \\ K_2 = \bar{Q}_2 \bar{Q}_0$$

Q ₃ Q ₂	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	X	Y	Y	X
10	X	Y	X	Y

$$J_3 = \bar{Q}_2 \bar{Q}_1 \bar{Q}_0 \\ K_3 = \bar{Q}_2 \bar{Q}_1 \bar{Q}_0$$

CIRCUIT DIAGRAM



CONCLUSION

In the Lab we learnt and build up & down Synchronous counter (2, 3, 4 bit)

EXPERIMENT - II

MOD COUNTERS

AIM: Realization of MOD-N counter using Decade Counter IC-7490 and to implement mode counter 4, 5 using 7476

Theory:

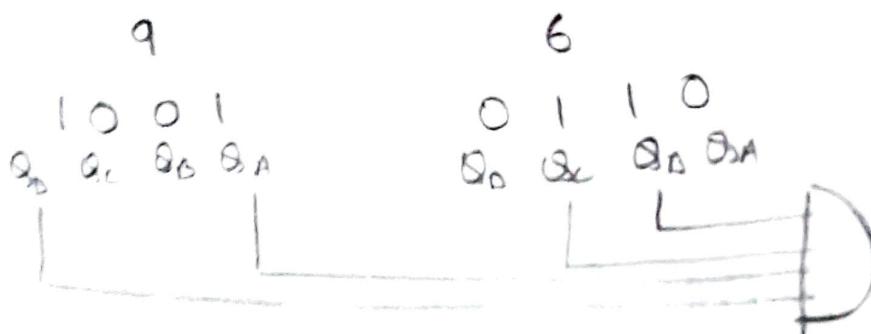
Decade Counter (IC 7490): It is a simple counter which can count from 0 to 9. As it is a 4-Bit binary decade counter, it has four output ports Q_A, Q_B, Q_C, Q_D . When the count reaches 10, binary output reset to 0 (0000). Every time another pulse starts at pin no. 9. This IC 7490 is an built divide by 2 and divides counts in it.

MOD counters:

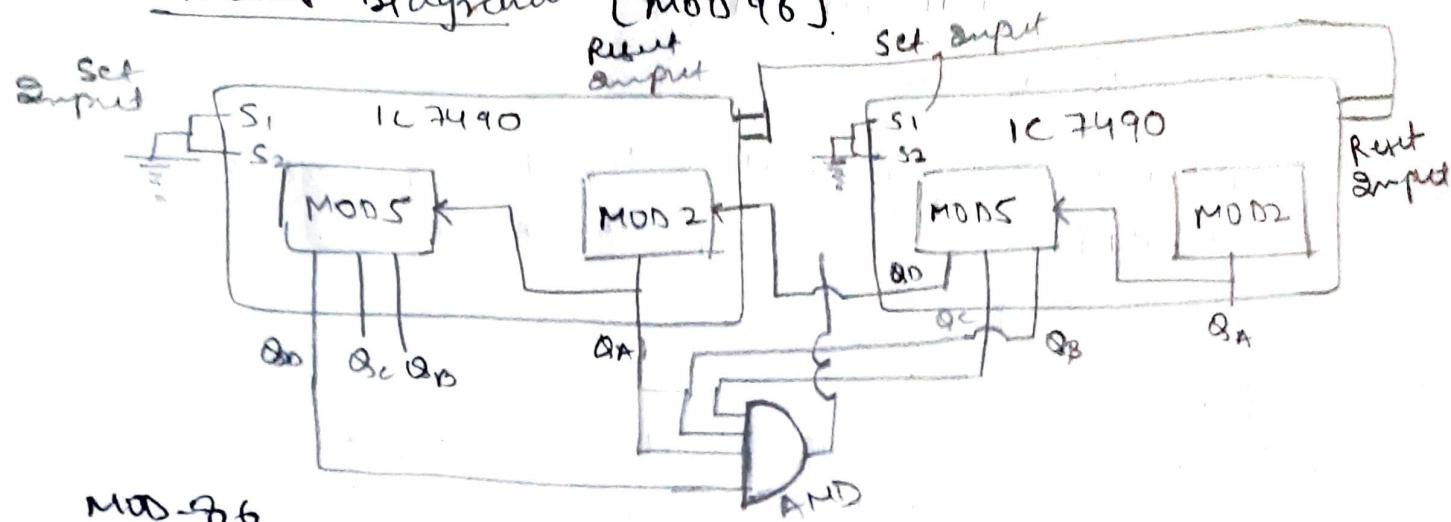
MOD counters are definitely based on no of states that the counter will sequence through before returning back to its original value.

MOD-96

States required 0, 1, 2, 3, 4, 5, ...,

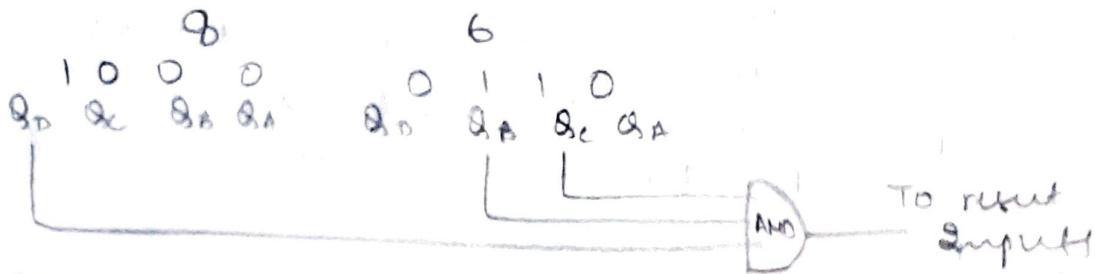


Circuit Diagram [MOD 96]

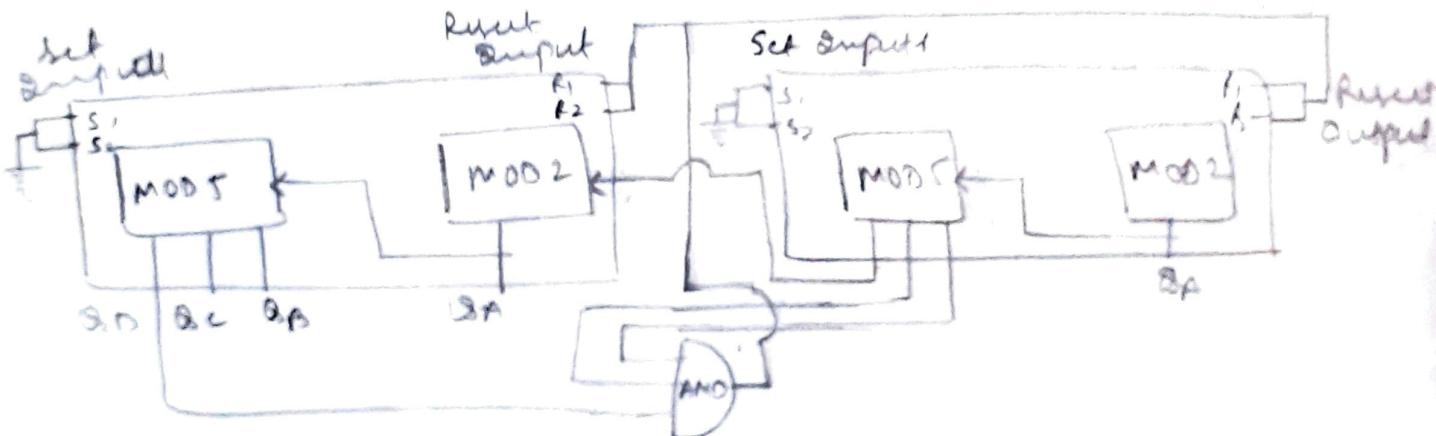


MOD-86

State Required - 0, 1, 2, ..., 84, 85.



Circuit Diagram (MOD 86)



MOD-5 counts
using IC 2476.

Excitation table for JK flip-flop.

Q_u	Q_{out}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

Truth Table

Present State

Q_C	Q_B	Q_A
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

Next State

Q_{C+1}	Q_{B+1}	Q_{A+1}
0	1	1
0	1	0
0	0	1
1	0	0
x	x	x
x	x	x
x	x	x

flip-flop output

J_C	K_C	J_B	K_B	J_A	K_A
0	x	0	x	1	x
0	0	1	x	x	1
x	x	x	0	0	x
x	x	x	x	x	x
x	x	x	x	x	x

K-map

Q_C	$Q_B Q_A$	Q_{C+1}
0	00 01 11 10	0 0 1 1
1	x x 1 0	x x x x

$J_C = \bar{Q}_B Q_A$

Q_C	$Q_B Q_A$	Q_{C+1}
0	00 01 11 10	0 0 1 1
1	x x 1 0	x x x x

$K_B = \bar{Q}_A$

Q_C	$Q_B Q_A$	Q_{C+1}
0	00 01 11 10	0 0 1 1
1	x x 1 0	x x x x

$J_B = 1$

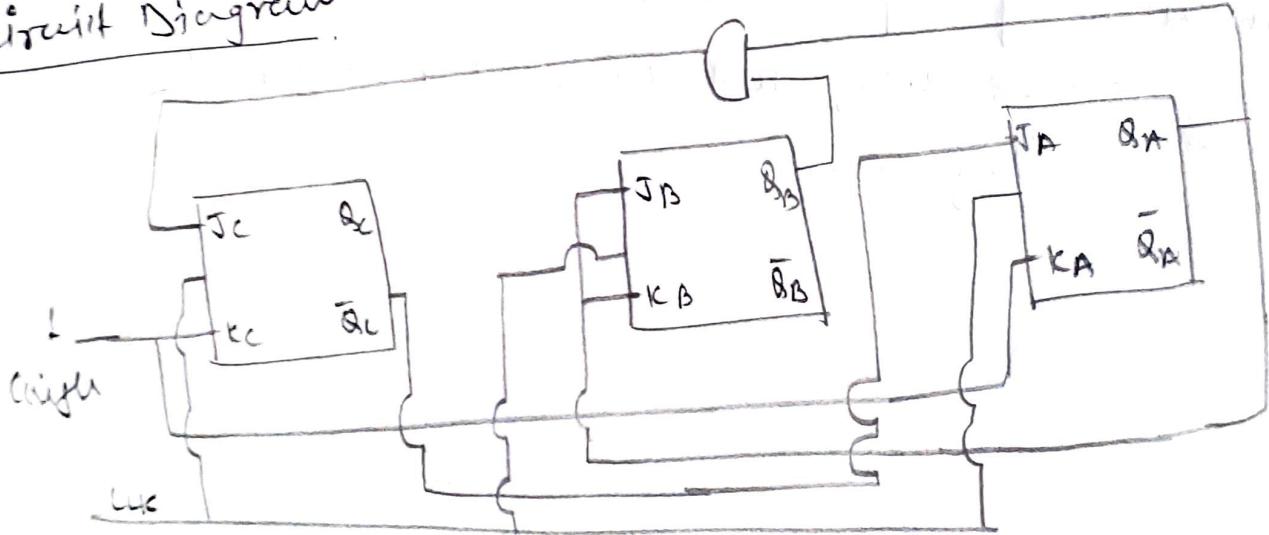
$K_C = 1$

Q_C	$Q_B Q_A$	Q_{C+1}
0	00 01 11 10	0 0 1 1
1	x x 1 0	x x x x

$J_A = 1$

$K_B = \bar{Q}_A$

Circuit Diagram



MOD-4 Counter

Q_B	Q_A	Q_{B+1}	Q_{A+1}	J_B	K_B	J_A	K_A
0	0	0	1	0	x	1	x
0	1	1	0	1	x	1	x
0	0	1	1	x	0	0	x
1	1	0	0	x	x	1	1

K-map

\bar{Q}_B	0	1
0	0	1
1	x	x

$J_B = \bar{Q}_A$

\bar{Q}_B	0	1
0	x	x
1	0	1

$K_B = Q_A$

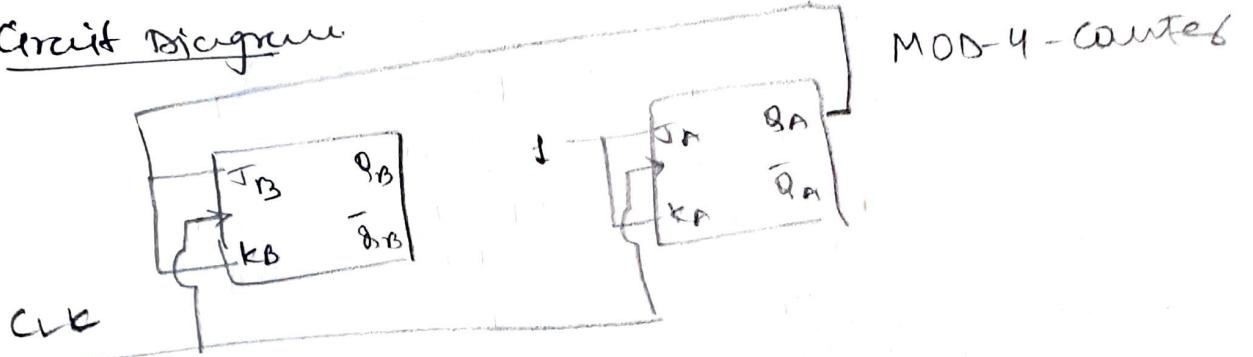
\bar{Q}_B	0	1
0	1	x
1	1	x

$J_A = 1$

\bar{Q}_B	0	1
0	x	1
1	x	1

$K_A = 1$

Circuit Diagram



Conclusion

successfully implemented Mod 8, mod 96,
counts using IC 7490 and mod 4 mod X
using IC 2476.

EXPERIMENT - 12

RING & JOHNSON'S COUNTER

AIM:

- 1) 4 Bit Ring counter using D flip-flop (IC 7474)
- 2) 4 Bit Johnson's counter using DFF

SOFTWARE Requirement

IC trainer kit, patch cords
IC 7474, multism / circuit verber

THEORY

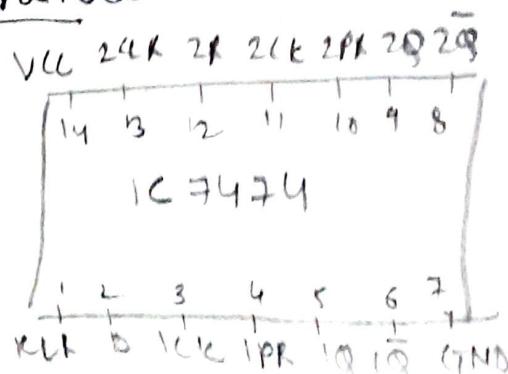
Ring counter

Ring counter is used in those applications in which several operations are to be controlled in a sequential manner. for ex. in assistance welding the operation called Squeeze, hold, weld and off are to be performed sequentially. we can use ring counter to initiate those operations.

Johnson's counter

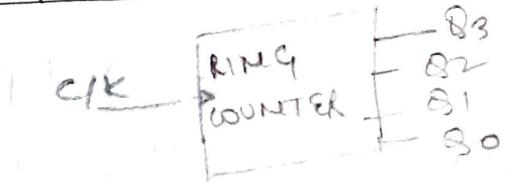
A Johnson counter is a modified ring counter where the inverted output of the last flip-flop is connected to the input of first. The register cycles through a sequence of bit patterns. The mod. of the Johnson's counter is 2^n if n-flip flop are used.

PIN configuration



RING COUNTER

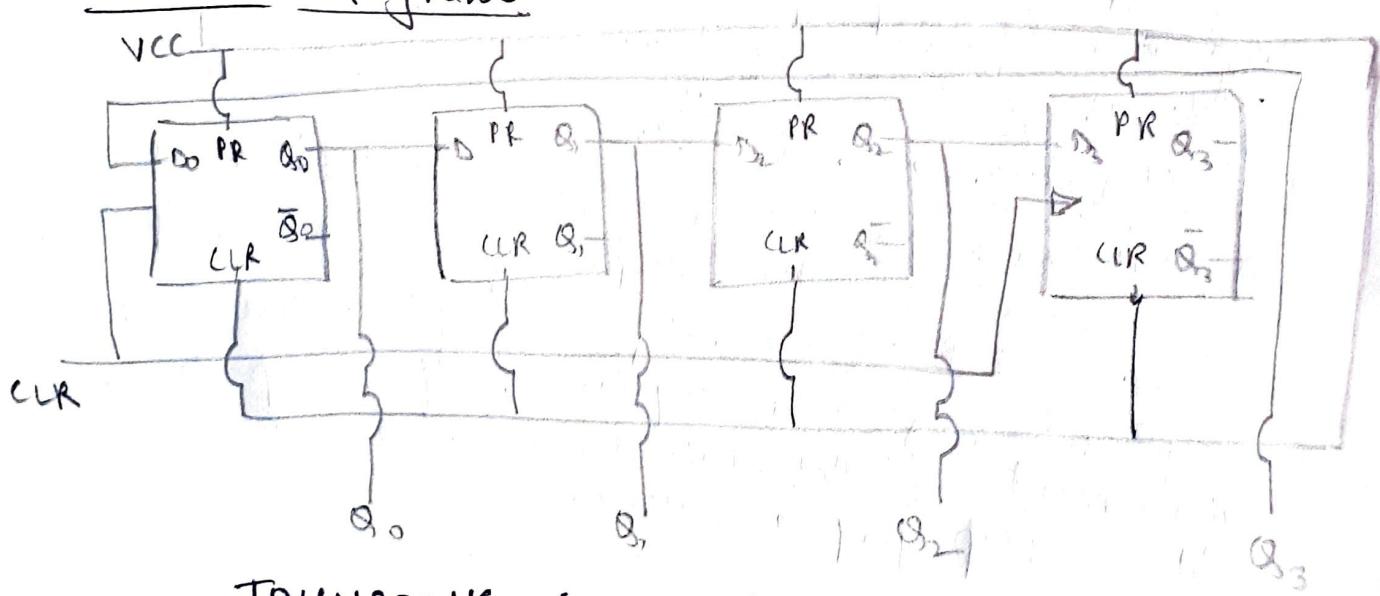
LOGIC DIAGRAM



Truth Table

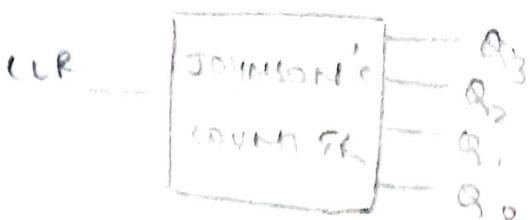
Q_3	Q_2	Q_1	Q_0
0	0	0	1
0	0	1	0
0	1	0	0
1	0	0	0
0	0	1	0
0	0	1	0
0	1	0	0
1	0	0	0

Circuit Diagram



JOHNSON'S COUNTER

LOGIC DIAGRAM

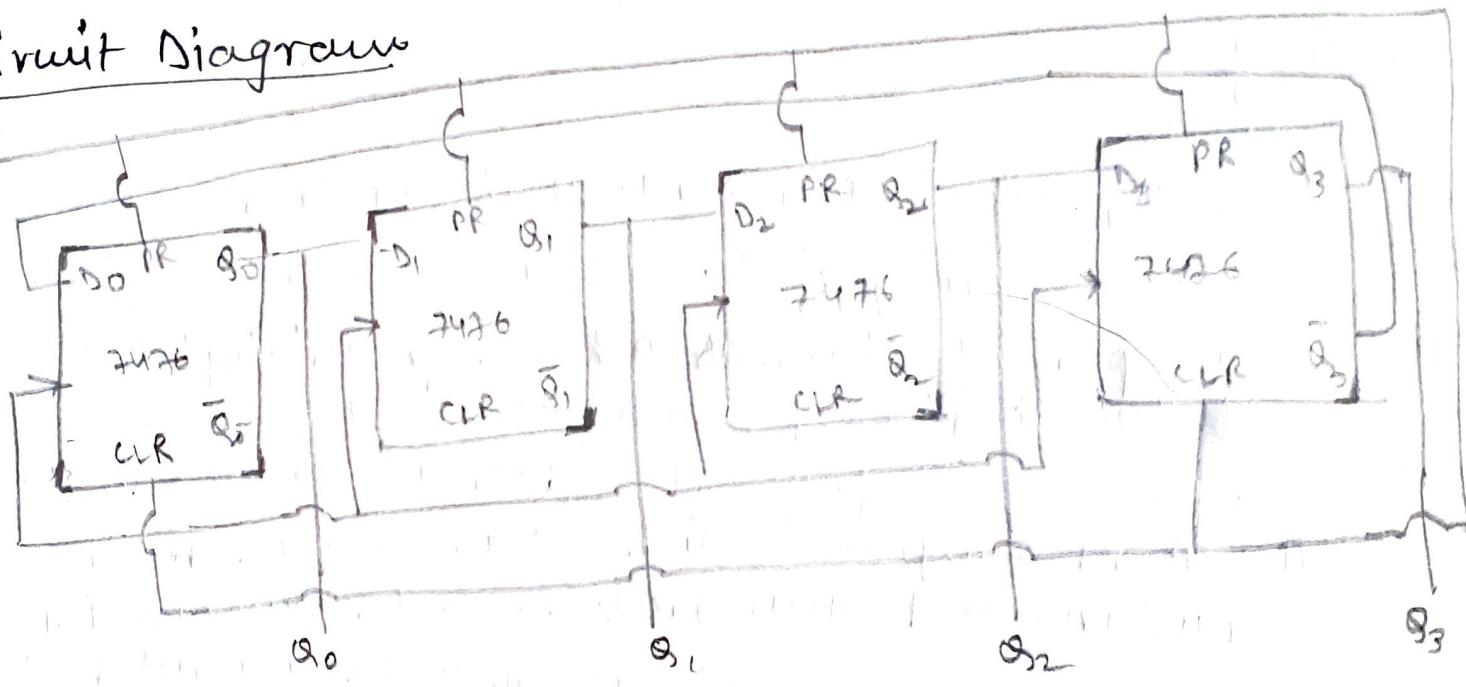


Truth table

Q_3	Q_2	Q_1	Q_0
0	0	0	1
0	0	1	1
0	1	1	1
1	1	1	1
0	1	1	1
0	0	1	1
0	0	0	1
0	0	0	0

Circuit Diagram

Vcc



Conclusion

In this lab, we learned to implement Ring counters and Johnson's Counter Ring IC 7476 (D-PR)

EXPERIMENT - 13

SEQUENCE GENERATOR

Aim:- Design and Implement Sequence generator using JK flip-flop.

Hardware / Software / DC Requirement

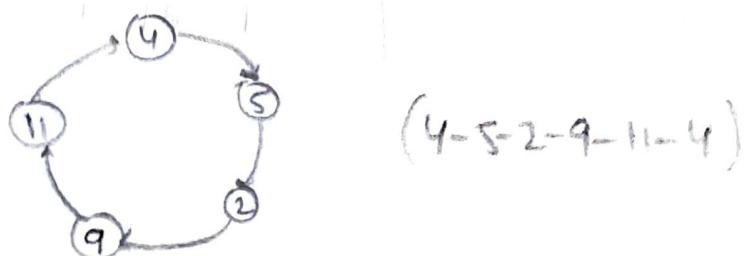
MS JK flip-flop , IC 7408 , IC 7432, IL4077

Theory

Sequence Generator

A digital logic circuit whose purpose is to produce a prescribed sequence of outputs. Each output will be one of a no of symbols of Binary or q-ary logic levels. The sequence may be of indefinite length or of predetermined fixed length. A binary counter is special type of Sequence generator.

State Diagram



Excitation table

Present	Next	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

State Table

Present Next

flip-flop.

Q_3	Q_2	Q_1	Q_0	Q_3^+	Q_2^+	Q_1^+	Q_0^+	J_3	K_3	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	x	x	x	x	x	x	x	x	x	x	x	x
0	0	0	1	x	x	x	x	x	x	x	x	x	x	x	x
0	0	1	0	1	0	0	1	1	x	x	x	x	x	x	x
0	0	1	1	x	x	x	x	x	x	x	x	x	x	x	x
0	1	0	0	0	1	0	1	0	x	x	x	1	x	x	x
0	1	0	1	0	0	1	0	0	x	x	x	x	x	x	x
0	1	1	0	x	x	x	x	x	x	x	x	x	x	x	x
0	1	1	1	x	x	x	x	x	x	x	x	x	x	x	x
1	0	0	0	x	x	x	x	x	x	x	x	1	x	x	x
1	0	0	1	1	0	1	1	0	x	x	x	x	x	x	x
1	0	1	0	x	x	x	x	x	x	x	x	x	x	x	x
1	0	1	1	0	1	0	0	x	x	x	x	x	x	x	x
1	1	0	0	x	x	x	x	x	x	x	x	x	x	x	x
1	1	0	1	x	x	x	x	x	x	x	x	x	x	x	x
1	1	1	0	x	x	x	x	y	x	x	x	x	x	x	x
1	1	1	1	x	x	x	x	y	x	x	x	x	x	x	x

$Q_1 Q_0$ J_3

$Q_2 Q_3$	00	01	11	10
00	x	x	x	1
01	0	0	x	x
11	x	x	x	x
10	x	x	x	x

$J_3 = Q_1$

$Q_1 Q_0$ K_3

$Q_2 Q_3$	00	01	11	10
00	x	x	x	x
01	x	x	x	x
11	x	x	x	x
10	x	0	1	x

$$k_3 = Q_1$$

$Q_1 Q_0$ J_2

$Q_2 Q_3$	00	01	11	10
00	x	x	x	0
01	x	x	x	x
11	x	x	x	x
10	x	0	1	x

$J_2 = Q_1, Q_0$

$Q_1 Q_0$ K_2

$Q_2 Q_3$	00	01	11	10
00	x	x	x	x
01	0	1	x	x
11	x	v	v	x
10	x	x	x	x

$$k_2 = Q_0$$

		J ₁		Q ₀	
		00	01	11	10
Q ₁ Q ₀	00	X	X	X	X
	01	0	1	X	X
	11	X	X	X	X
	10	X	1	X	X

$$J_1 = Q_0$$

		J ₂		Q ₁	
		00	01	11	10
Q ₂ Q ₃	00	X	X	X	1
	01	1	X	X	X
	11	X	X	X	X
	10	X	X	X	X

$$J_2 = Q_0$$

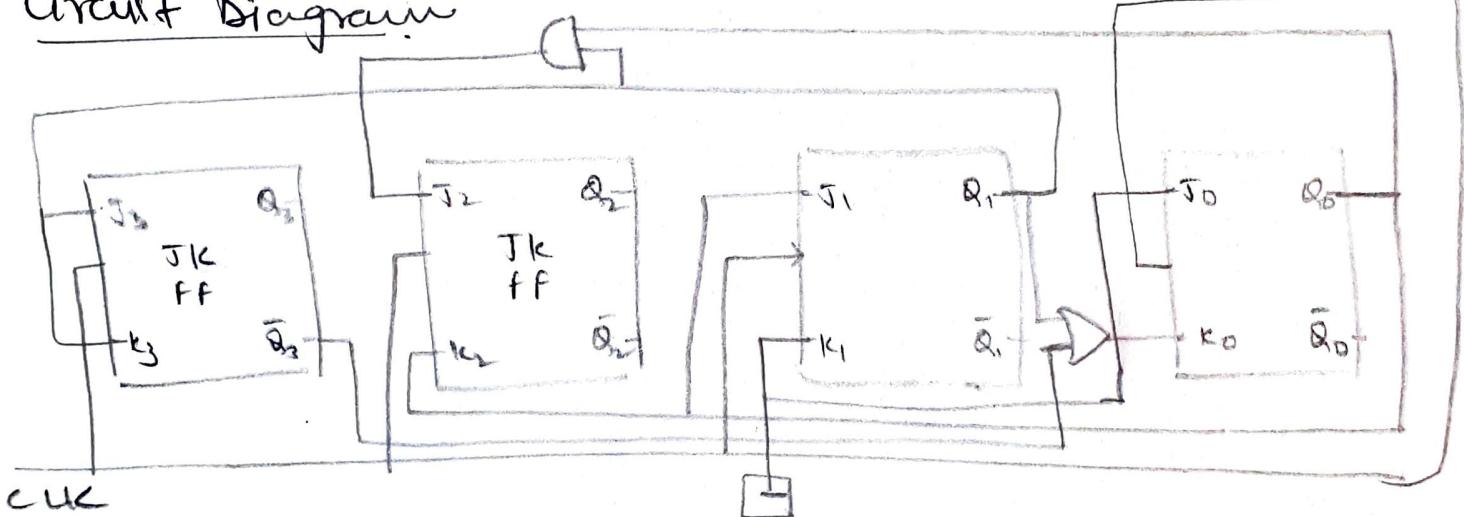
		J ₃		Q ₂	
		00	01	11	10
Q ₁ Q ₀	00	X	X	X	1
	01	1	X	X	X
	11	X	X	X	X
	10	X	X	X	X

$$J_3 = 1$$

		J ₄		Q ₃	
		00	01	11	10
Q ₂ Q ₃	00	X	X	X	X
	01	X	1	X	X
	11	X	X	X	X
	10	X	0	1	X

$$J_4 = \bar{Q}_3 + Q_1$$

Circuit Diagram



Conclusion

Successfully designed & implemented sequence generator for sequence (4-5-2-9-11)

EXPERIMENT - 14

SEQUENCE DETECTOR

AIM:- Design & Implement J-K flip-flop using MS-JK flip-flop.

Hardware | Software | IC required

MSTk-ff, Not Gate (IC7404) OR Gate (IC7432)

AMD Gate (IC7408) - Multism

THEORY

Sequence detector - A sequence detector is a sequential state machine which takes an input string of bits and generates an output whenever the target sequence has been detected. In a more mature, output depends upon no forced states & the external input

To detect Sequence 110

State diagram

$$S_0 = 0$$

$$S_1 = 1$$

$$S_2 = \text{0}$$

$$S_3 = 110$$

Input
Output

$y = 011101101000$

$4 = 000010010000$



Q_A	Q_B	Q_A^t	T	K
0	0	0	0	0
0	-	-	x	-
-	0	-	0	0
-	-	-	x	-

State Table

Q_A	Q_B	Input χ	Q_{A+1}	Q_{B+1}	Flip-flop J_A	Flip-flop K_A	Flip-flop J_B	Flip-flop K_B
0	0	0	0	0	0	x	0	x
0	-	-	0	0	0	x	x	-
-	0	0	-	0	0	x	0	x
-	-	-	-	-	0	x	x	-
-	-	-	D	-	0	x	x	0

$Q_A X$	T_A		
Q_A	00	01	11
0	0	0	1
1	X	0	0

$$T_A = \overline{Q_A} Q_B X$$

$Q_A X$	K_A		
Q_A	00	01	11
0	X	X	X
1	0	0	X

$$K_A = 0$$

$Q_A X$	00	01	11	12
Q_A	00	01	11	12
0	0	1	X	X
1	X	0	X	X

$$T_B = Q_A X + Q_A \bar{X}$$

$$T_B = Q_A \oplus X$$

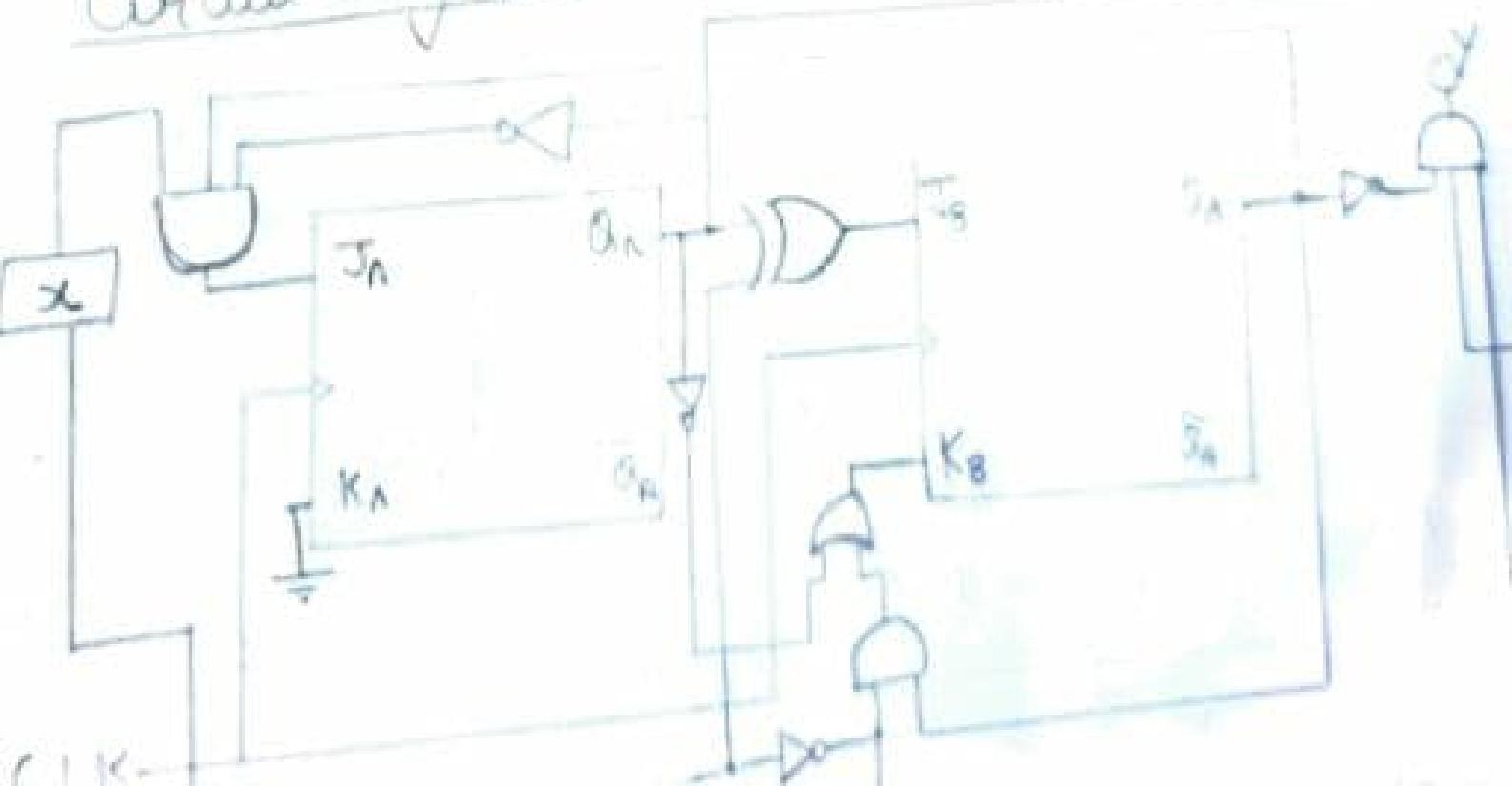
$Q_A X$	00	01	11	12
Q_A	00	01	11	12
0	X	X	L	T
1	X	X	0	U

$$K_B = \overline{T_A} + Q_A \bar{X}$$

output
Y

$$Y = Q_A \overline{Q_B}$$

Circuit Diagram



EXPERIMENT - 15

ASM

Aim: Implement 2 Bit up / down counters using mux controller method when $x=0$ then count up and $x=1$ then count down.

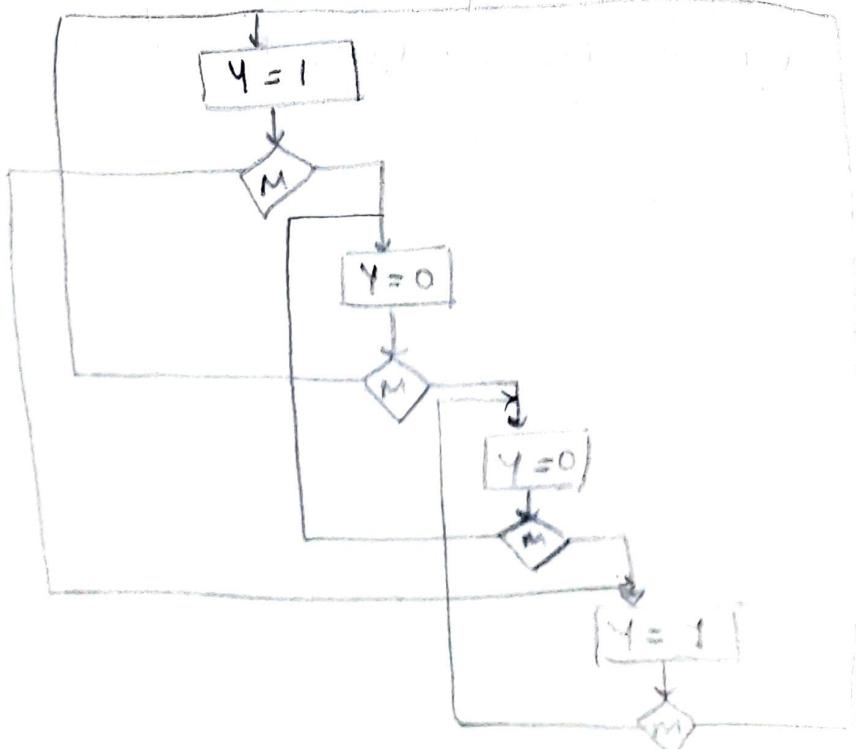
Hardware / Software / IC Required:

4:1 MUX, D-flip-flop, NOT gate (7404)

Theory

ASM Chart

The algorithmic state machine (ASM) method is a method for describing finite state machine originally developed by Thomas Osborne & Christopher Closs at Hewlett-Packard in the 1970s. It is used to represent diagrams of digital integrated circuits. The ASM diagram is like a state diagram but more structured and thus easier to understand. An ASM chart is a method of describing the sequential operation of a digital system.



ASM chart

2-Bit Up-Down-counters

State Diagram

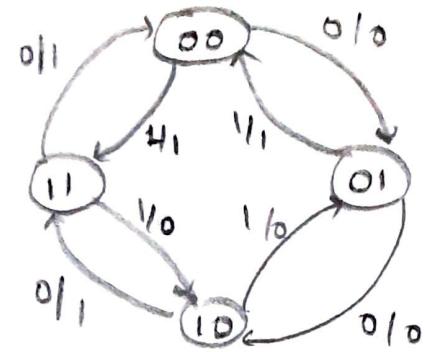
for two Bit Up / Down Counter

M=0 Up Counting

M=1 Down Counting

So Basically counting up when

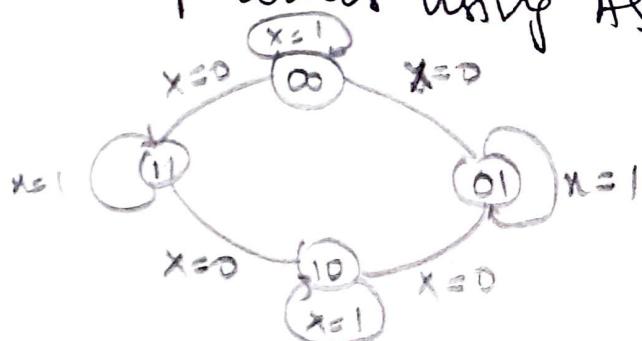
M=0 & counting down when M=1



EXCITATION TABLE (For D-flip flop)

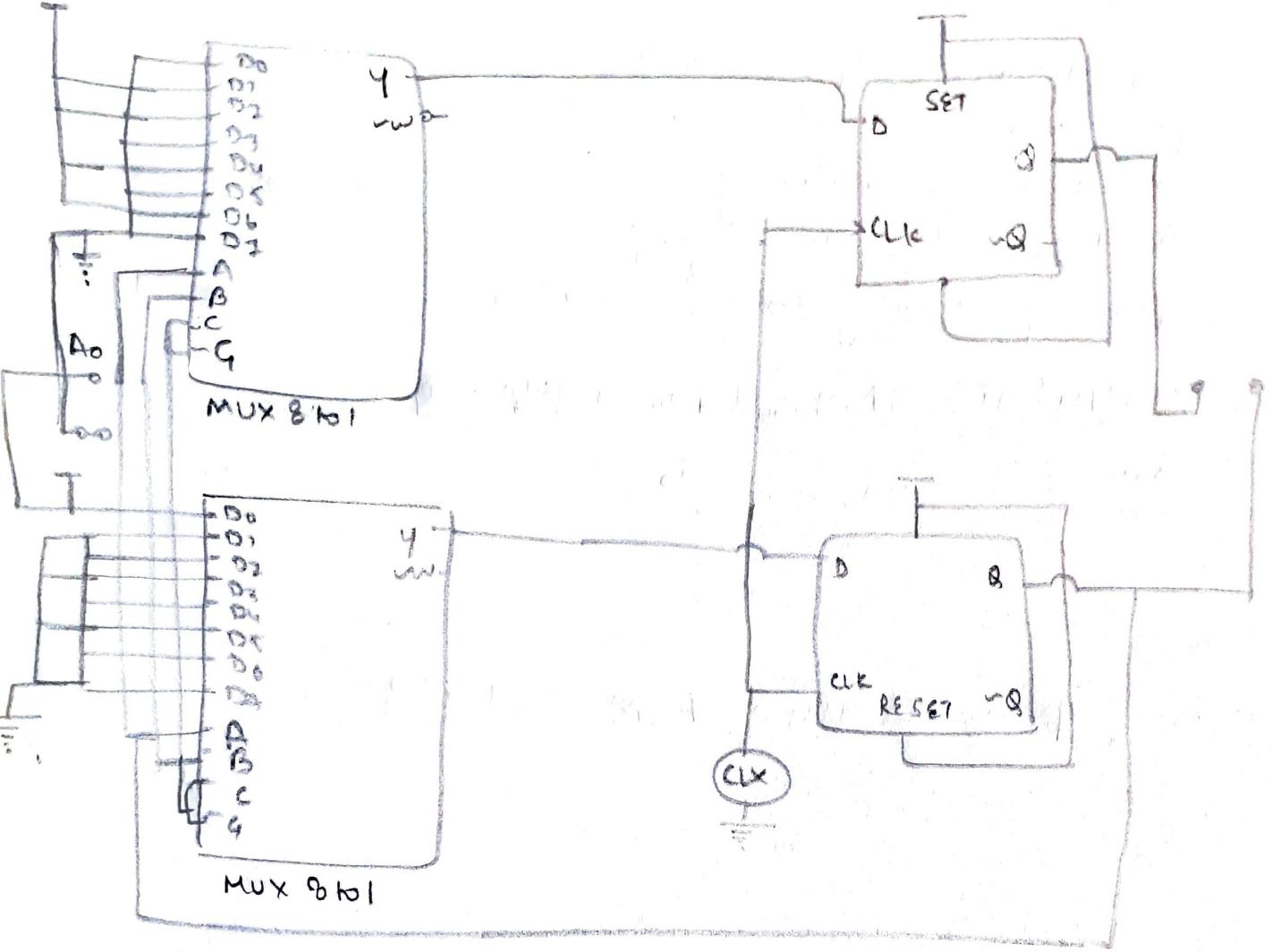
S _n	D _{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

2-Bit up counter using Agm with MUX



State Table

Present		Next		Input	MUX	
S ₁	S ₀	S _{1'}	S _{0'}	X	MUX1	MUX2
0	0	0	1	0	MUX1 D ₀ =0	MUX2 D ₀ =X
0	0	0	0	1		
0	1	1	0	0	D ₁ =X	
0	1	0	1	1		
1	0	1	1	0	D ₂ =1	D ₂ =X
1	0	1	1	0		
1	1	0	0	1	D ₃ =X	D ₃ =X
1	1	1	0	1		



Conclusion:

Successfully implemented & designed ATC with
MUX controlled method.