EXPERIMENT-1

Realization of Adder & Subtractor

Aim: To realise full adder / Subtractor using
(i) Basic gates (ii) Universal gates

SOFTWARE: Circuit verse / Multiverse, Multisim 14, IC 7400
Ic Trainer kit, IC 7408, IC 7432, IC 7400, IC 7404

THEORY

Full Adder Theory

Full Adder: It takes 3 inputs & produces 2 outputs
first two inputs are A & B and third one
is Carry → Cin

The outputs are Cout & S [Sum]

A full Adder is designed in such a manner that it can take 3 inputs and create a byte wide adder and cascade the carry bit from one adder to another.

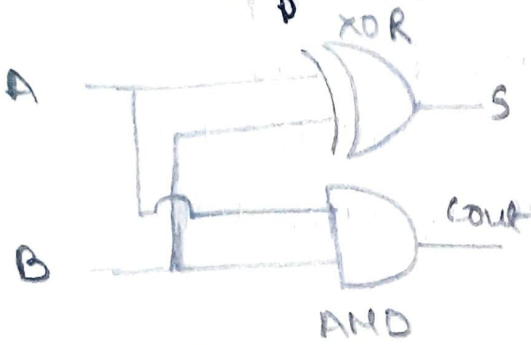
Full subtractor

A full subtractor is a conventional circuit that performs subtractions of two bits, one is minuend and other is subtrahend, taking into amount borrow of previous adjacent lower minuend. The circuit has 3 input & 2 outputs.

ADDERS

-K- map, circuit diagrams, truth table (Simulations)

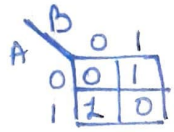
(1) Half Adder



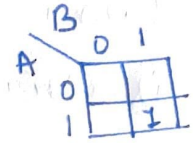
circuit

INPUT		OUTPUT	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	0	1
1	1	0	1

$A \oplus B$



$A \cdot B$

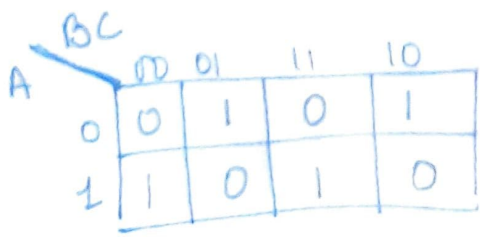


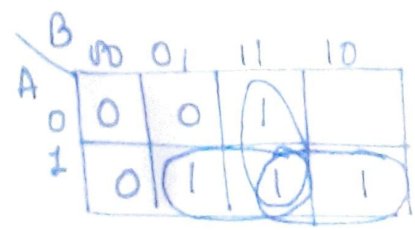
Half Adder = $A \oplus B$ for

$A \cdot B$ for carry o/p

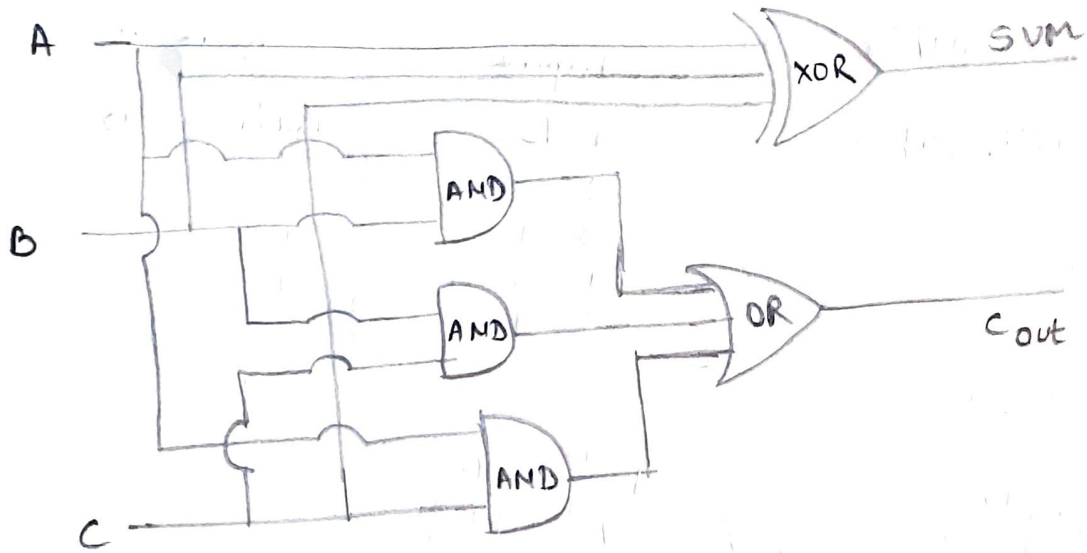
(2) Full Adder

Input			Output	
A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

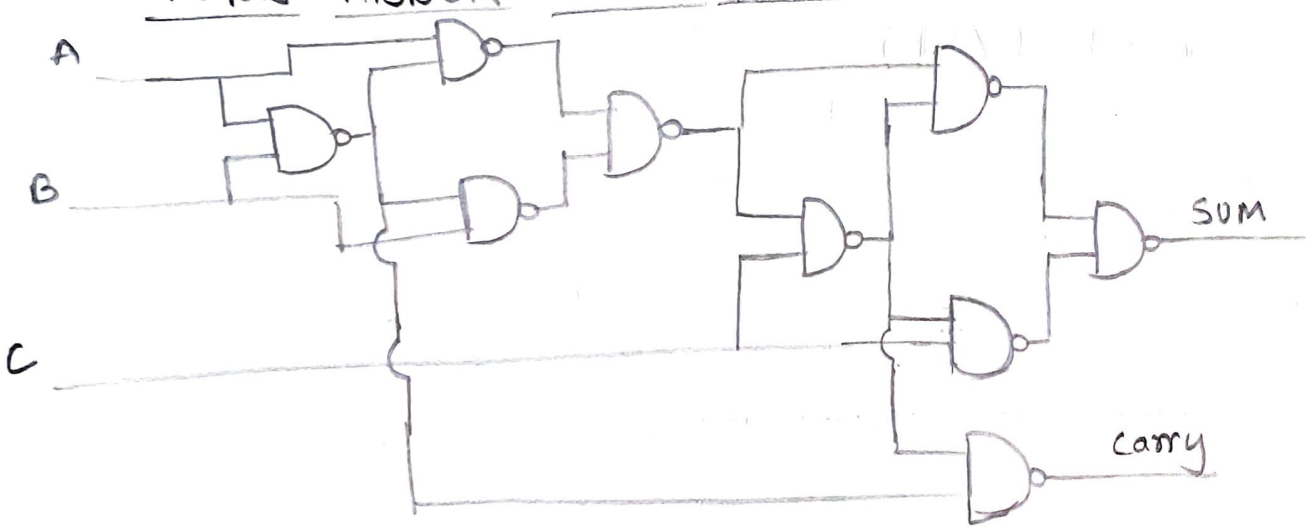




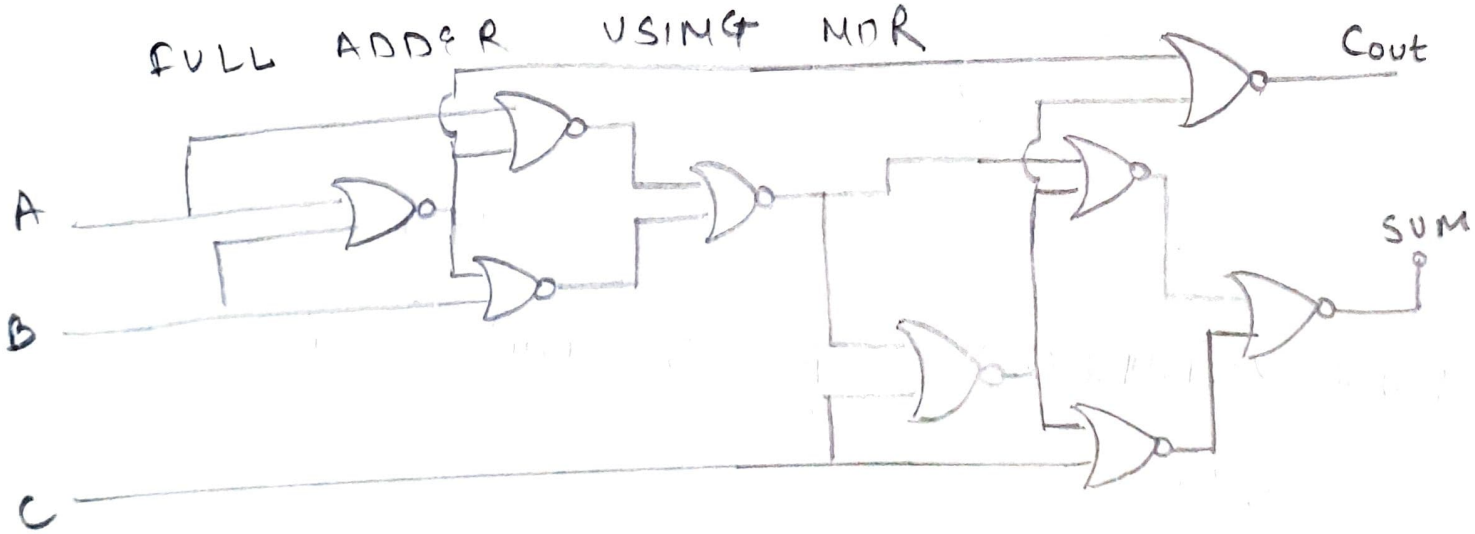
FULL ADDER USING LOGIC GATES



FULL ADDER USING NAND



FULL ADDER USING NOR



SUBTRACTOR

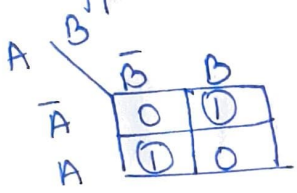
Truth table, karnaugh-Map circuit, Simulator

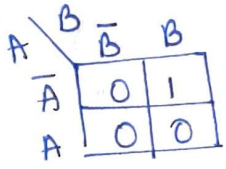
(1) Half-Subtractor

Truth Table

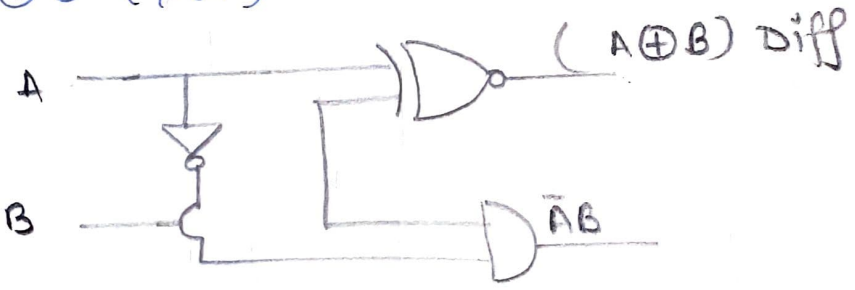
Input		Output	
A	B	Diff	Bor
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Difference

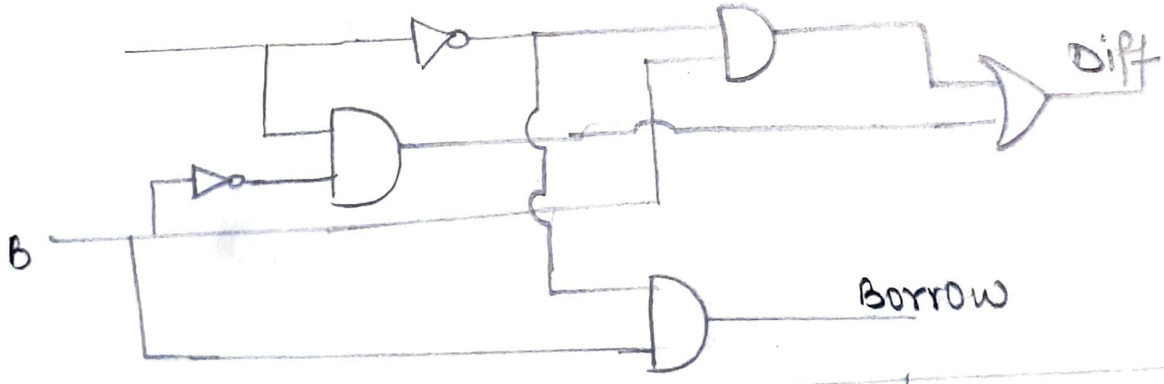




$A \oplus B$ (XOR)



Subtractor using Basic Gate



FULL SUBTRACTOR

truth table

A	B	Bin	Diff	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

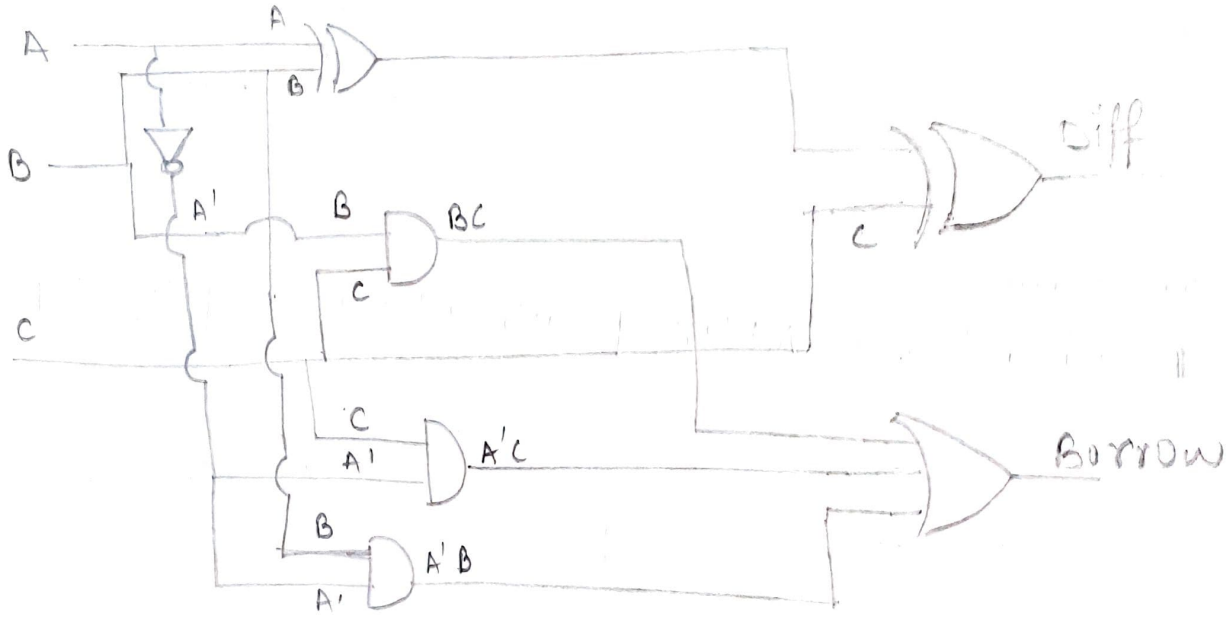
k-map

A \ BC	00	01	11	10
0	0	1	0	1
1	1	0	1	0

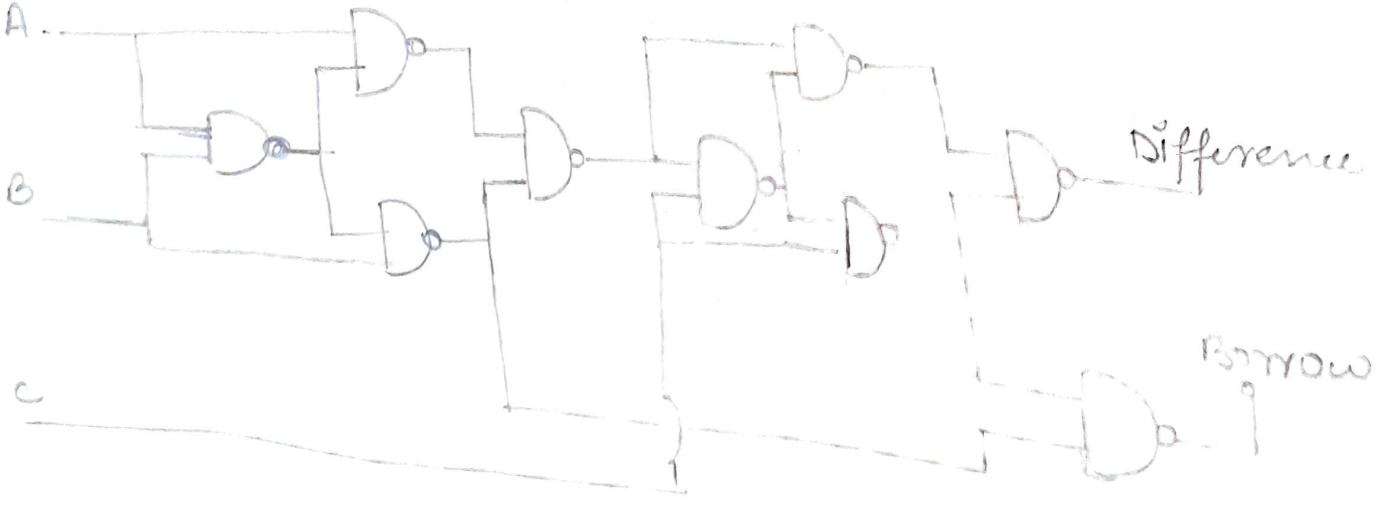
A \ BC	00	01	11	10
0	0	1	1	1
1	0	0	1	0

Diff - $A \oplus B \oplus C$

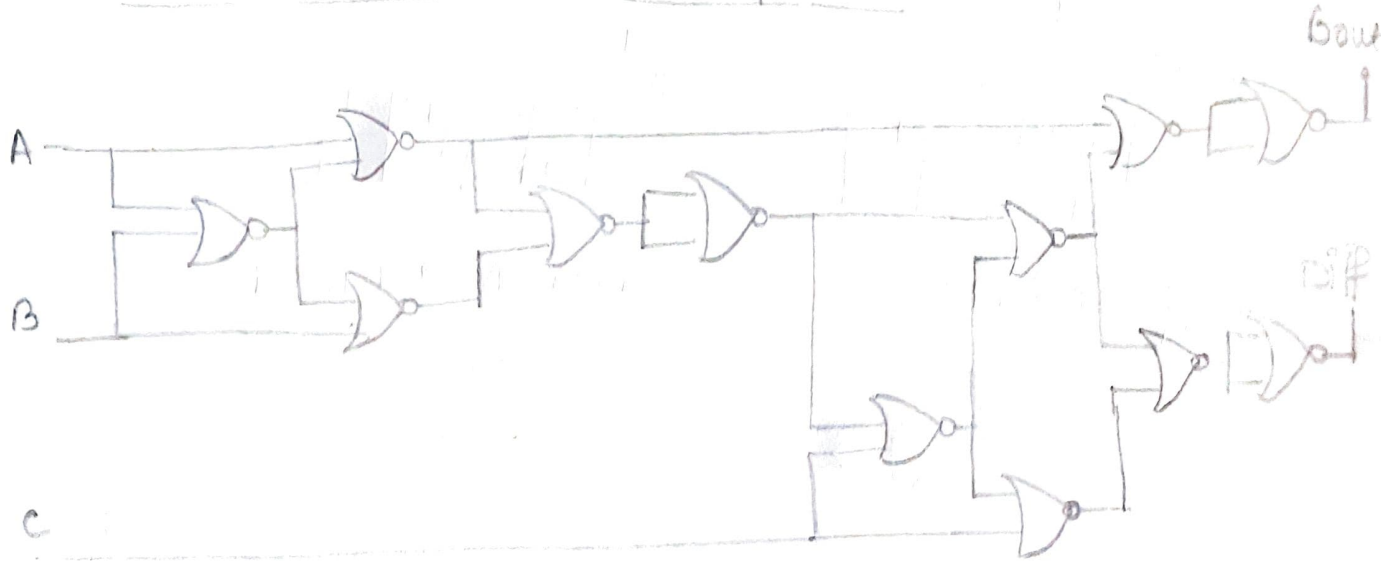
Bar - $A'C + A'B + BC$



FULL SUBTRACTOR USING NAND



FULL SUBTRACTOR USING NOR



Conclusion:

Realization of Adder & Subtractor successfully implemented