3 Bit CMOS Wallace Tree Multiplier

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Abstract

A fixed point Wallace tree multiplier architecture is used to perform multiple multiplications on different data paths. Various CMOS multiplier architectures are available, such as the array multiplier, carry-save multiplier, and Wallace-tree multiplier. Wallace-tree multiplier has been a very popular design due to its fast speed, ease for modularization and fabrication. Wallace-tree multiplier demonstrates significant speed enhancement.

1 Reference Circuit Details

The input is 3-bit numbers which will be multiplied using the Wallace tree algorithm and it will produce a 6-bit product. This structure is implemented using half adders, full adders and AND gates.
Initially, every bit is multiplied with every bit of the other number, then these partial products which have weight equal to the product of its factors are further reduced to obtain the respective weights by using half adders or full adders based on the size. The final result is calculated by the sum of all these partial products.

2 Reference Circuit

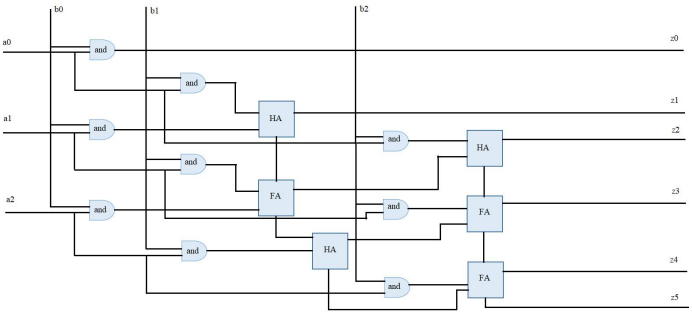

Figure 1: Reference circuit diagram.

3 Reference Circuit Waveforms

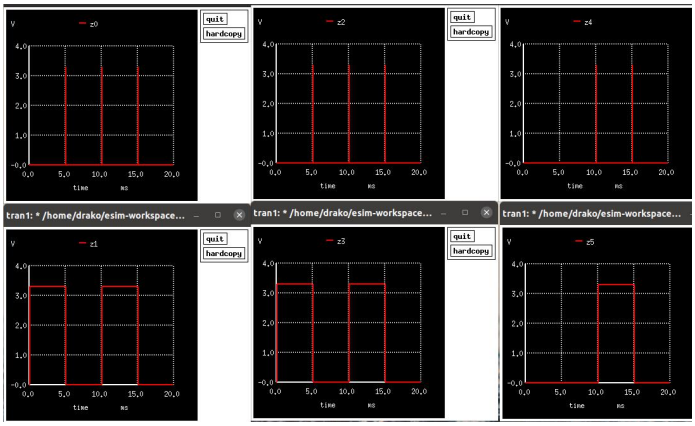

Figure 2: Reference waveform (Source : eSim)

References

[1] Priyanka Mishra and Seema Nayak. A Study on Wallace Tree Multiplier. https://www.researchgate.net/publication/327209221_A_study_on_Wallace_tree_multiplier

[2] Xiaoping Li, Xingguo Xiong, Hassan Bajwa, Prabir Patra. Implementation of a CMOS Wallace-tree Multiplier.

https://scholarworks.bridgeport.edu/xmlui/bitstream/handle/123456789/1256/Implementation%20of%20a%20CMOS%20Wallace-tree%20Multiplier%20.pdf?sequence=1