Serializer (vsdserializer_v1) spec sheet for 130nm tech node

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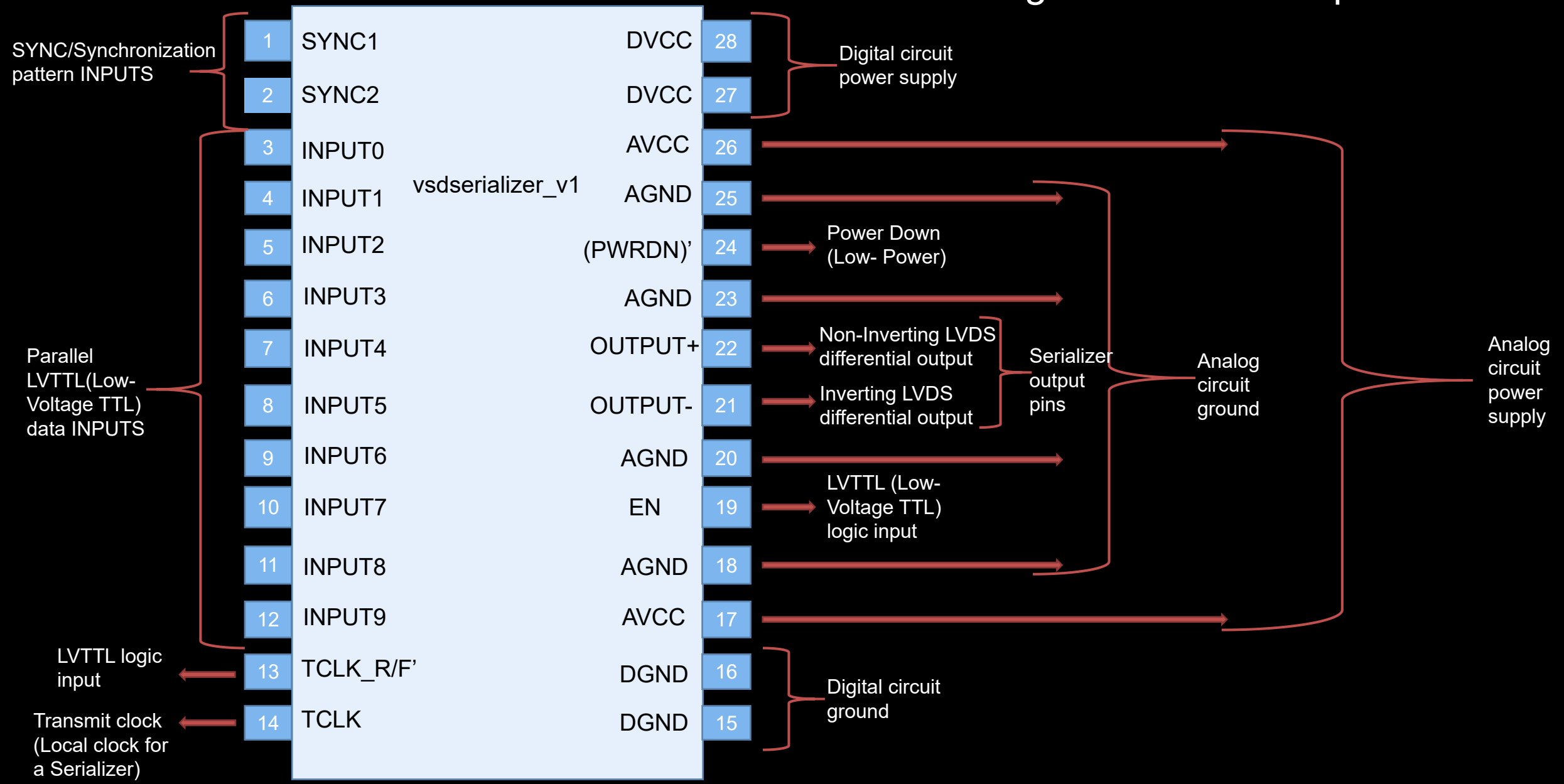
- Please contact Kunal at **kunalpghosh@gmail.com** in case of any doubts.

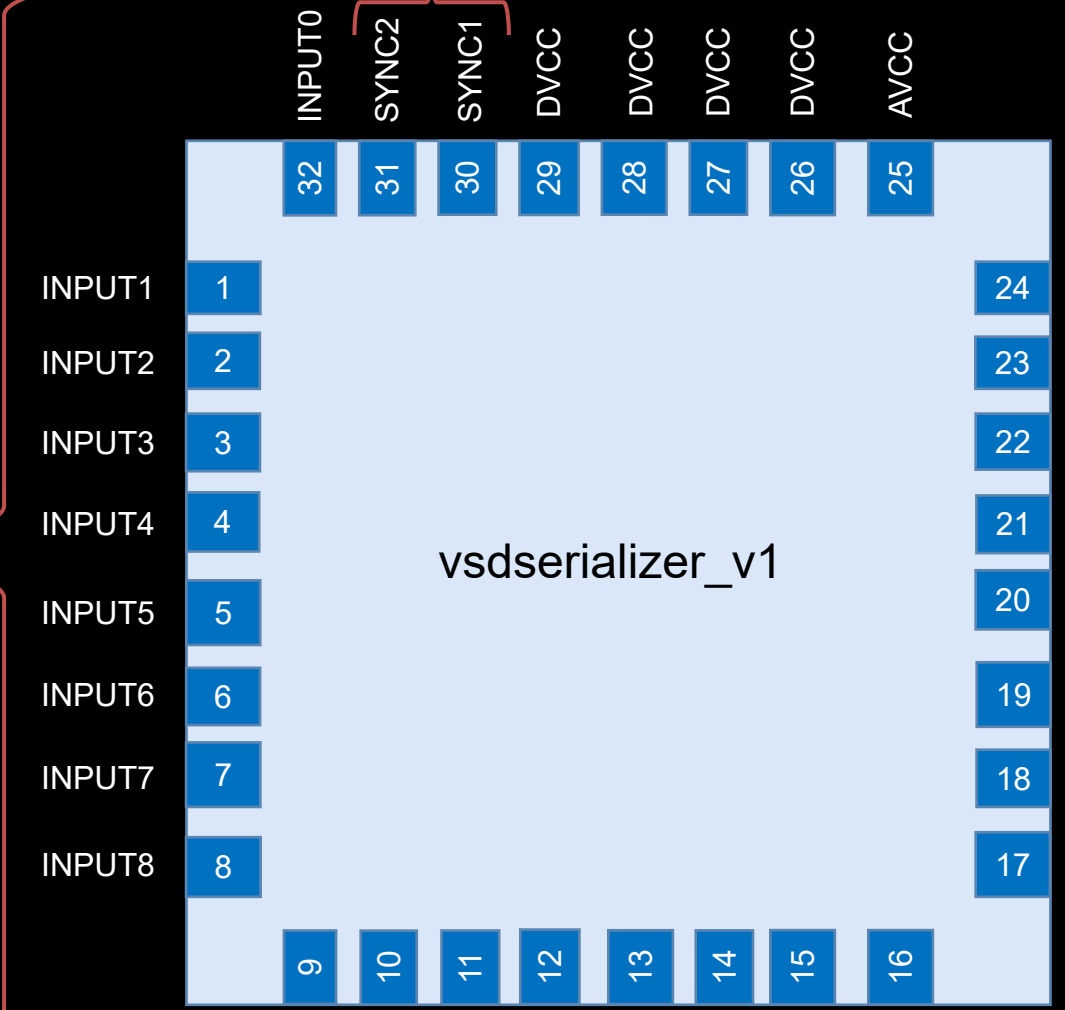
Pin Configuration & Description

- TOP VIEW



Functional Description

When at least one of the two pins are asserted high('1') for at least 6 cycles of TCLK, the serializer initiates a transmission of 1024 SYNC patterns.



Data is loaded into a 10-bit latch by the selected TCLK edge.

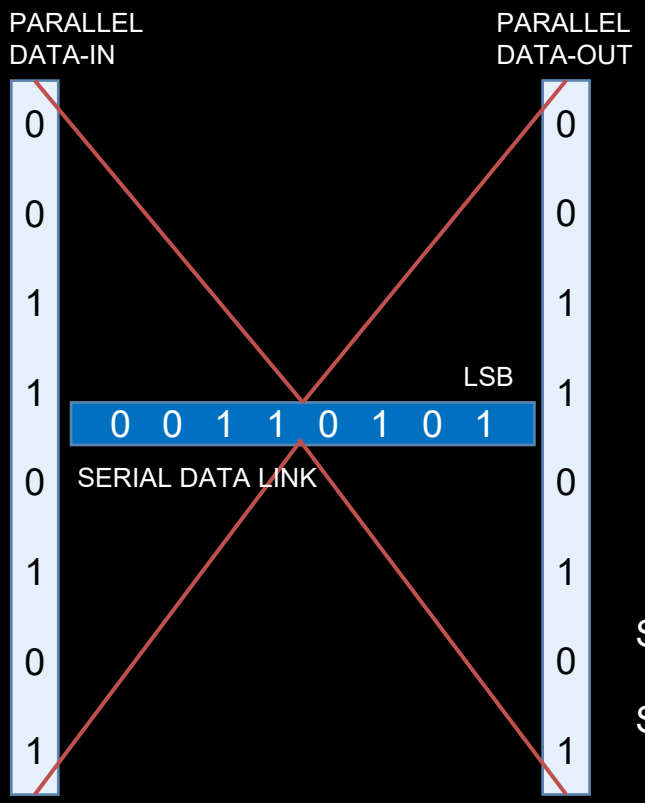
When PWRDN pin = 0, Power-down mode is entered. Here, PLL(Phase-Locked Loop) of the serializer is stopped and the outputs (OUTPUT+ and OUTPUT-) are in high impedance, disabling drive current(Id) and also reducing supply current(Is).

Setting EN/PWRDN = 0, sets device in high impedance. OUTPUT+ and OUTPUT- are held inhigh impedance when the supply voltage(V) is initially applied.

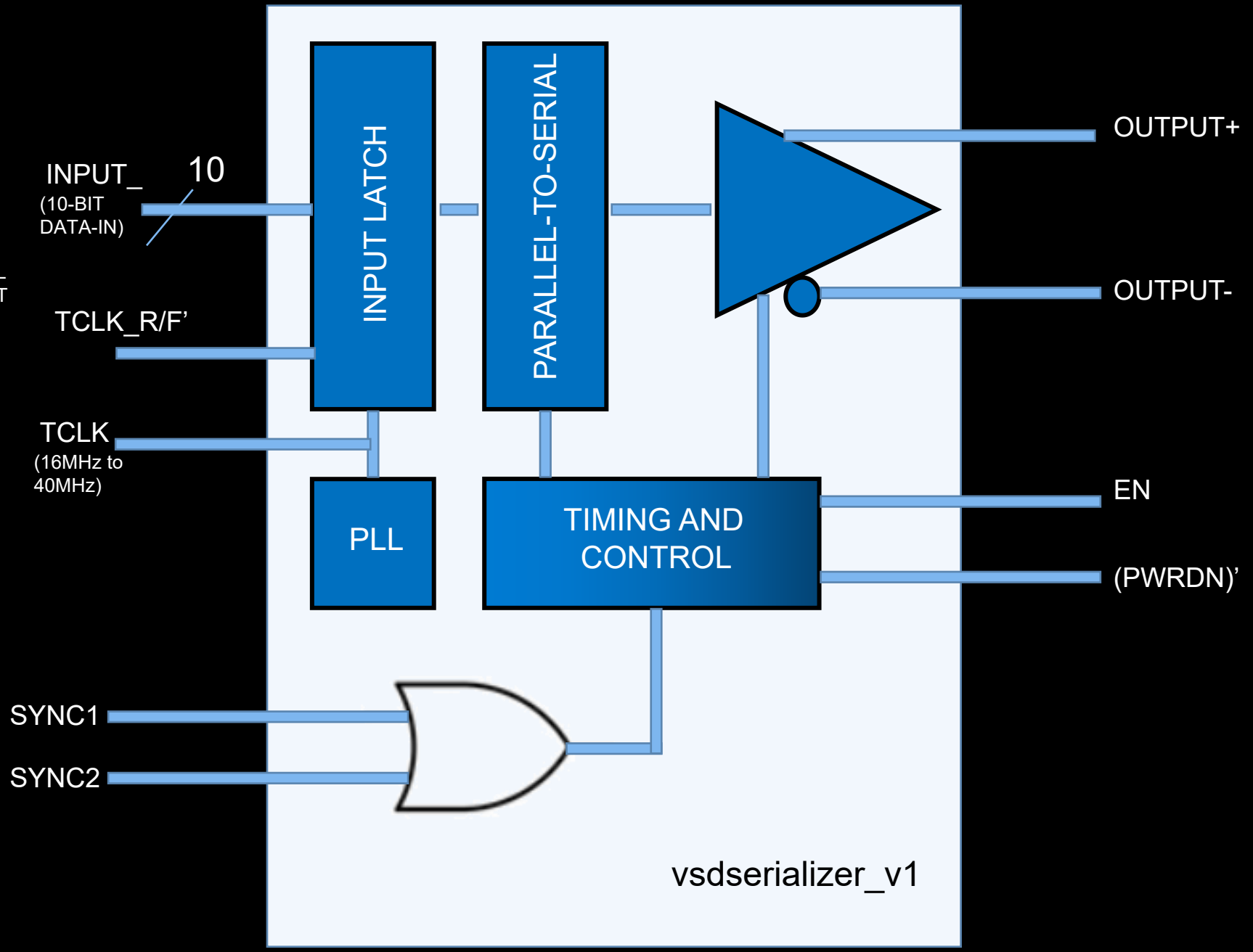
High(R) selects a TCLK rising-edge data strobe. Low(F) selects a TCLK falling-edge data strobe.

The serializer uses the TCLK input to latch the incoming data.

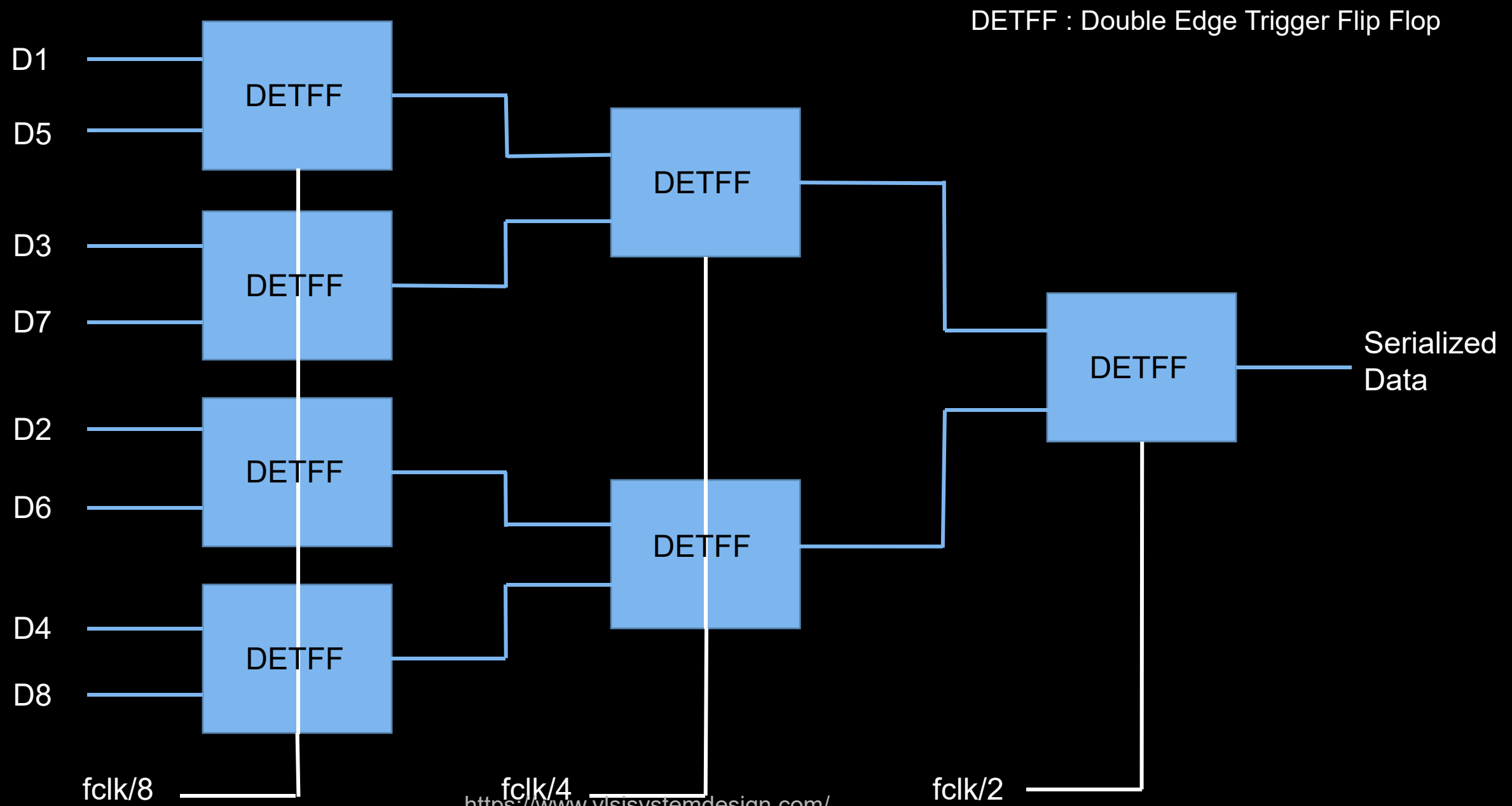
Functional Diagram



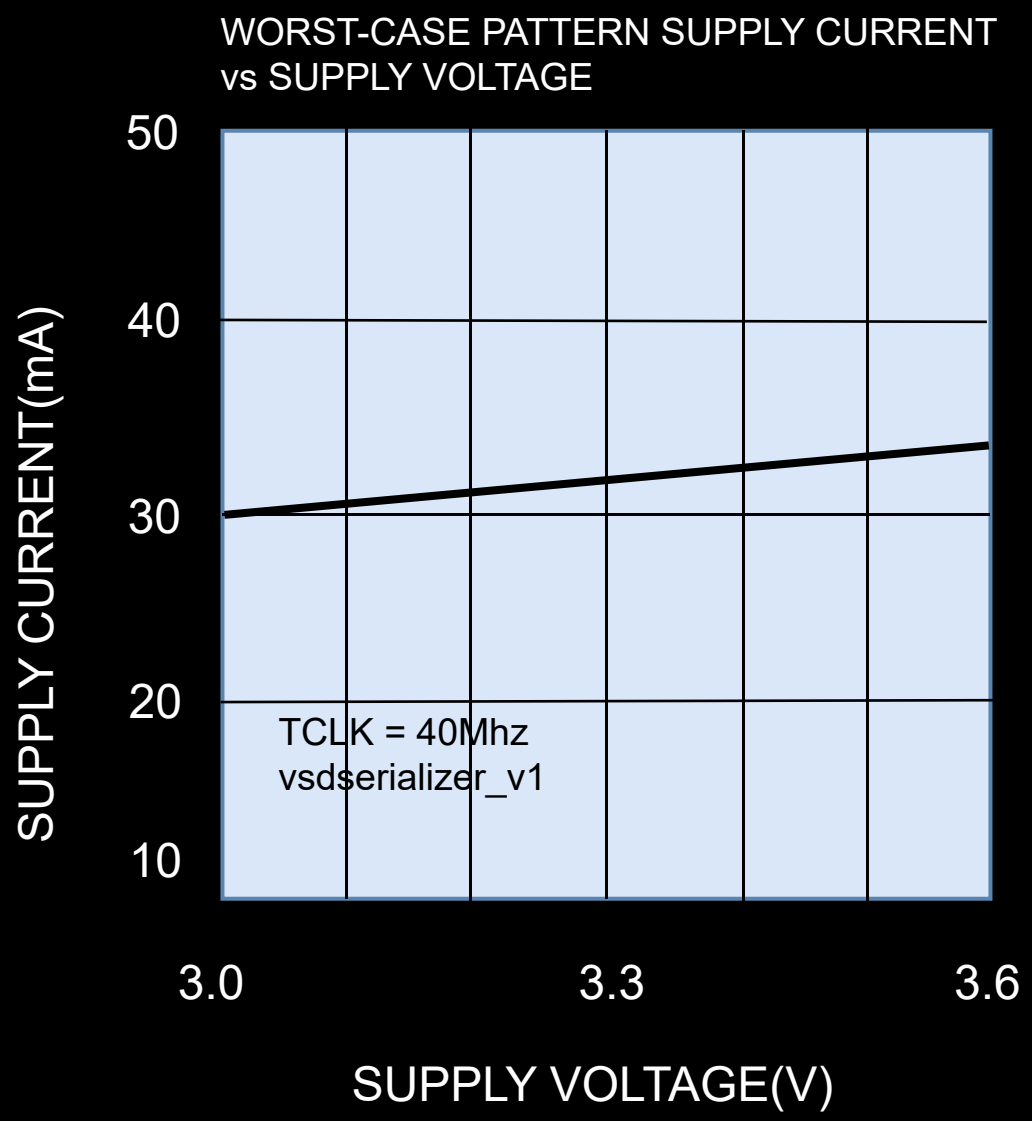
Serializer expected behavior

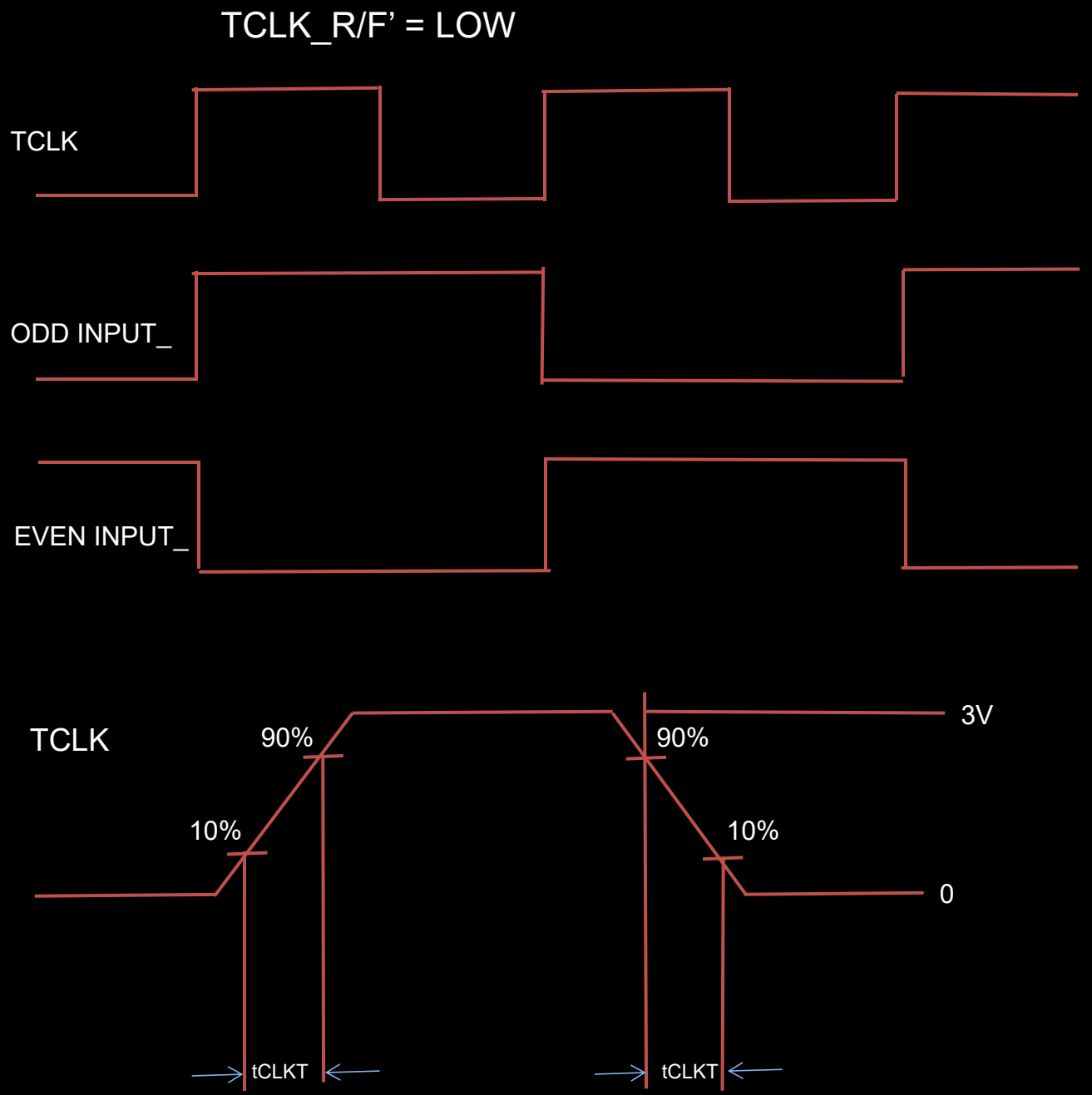


Block Diagram of a Serializer

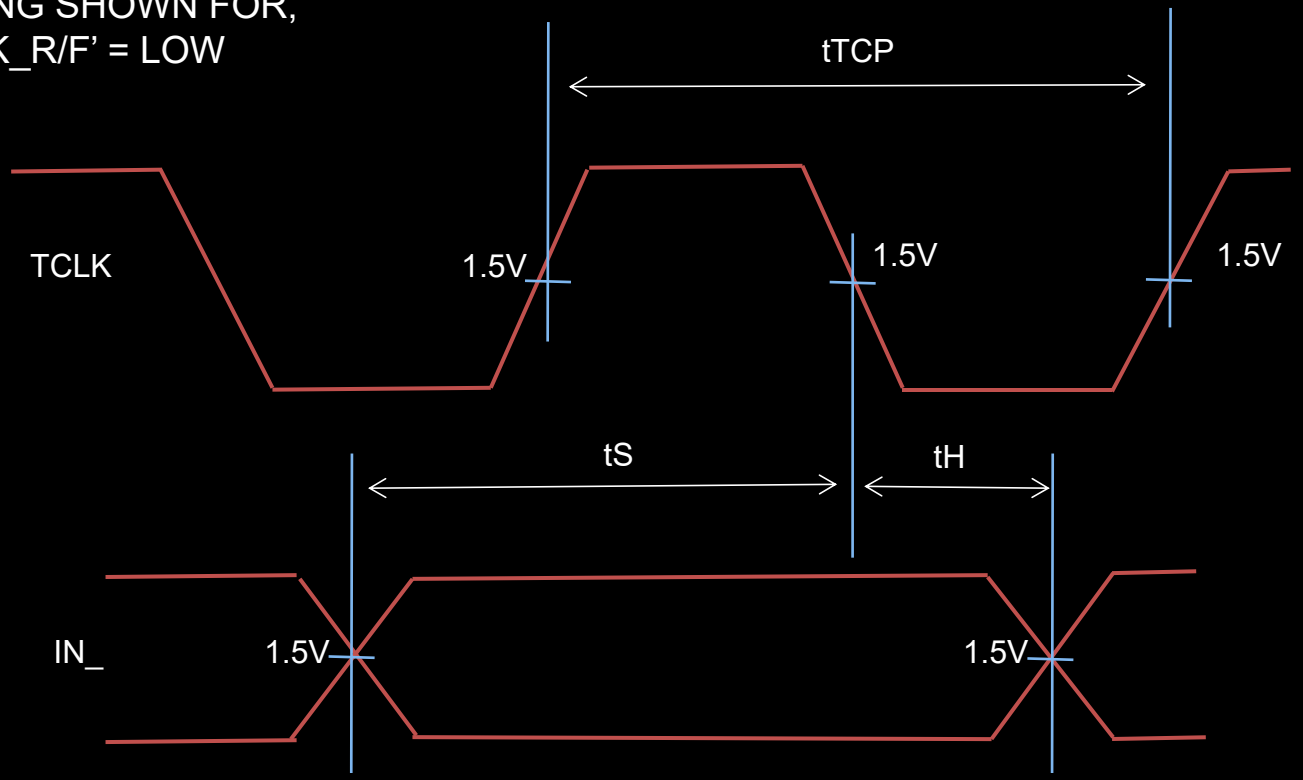


Typical Operating Characteristics





TIMING SHOWN FOR,
TCLK_R/F' = LOW



Condition for Output(OUTPUT+/OUTPUT-) in High Impedance:

- SYNC1 = SYNC2 = LOW
- EN = HIGH
- TCLK_R/F' = HIGH

INPUTS				OUTPUTS
EN	**(PWRDN)'**	**SYNC1**	**SYNC2**	**OUTPUT+, OUTPUT-**
H	**H**	**SYNC1/SYNC2, either of the two or both are '1' for atleast 6 TCLK cycles.**		**Synchronization Mode(SYNC patterns of six 1's and six 0's are transmitted for atleast 1024 TCLK cycles).**
H	**H**	**L**	**L**	**Data Transmission Mode(INPUT-9 and 2 frame bits are transmitted every TCLK cycle).**
X	**L**	**X**	**X**	**Output in high impedance**
L	X	X	X	Output in high impedance

Input /Output Function Table