Computer Architecture
Von Neuman and Harvard Architecture

How does cumtoer architecture work?
7 level Stack Hierarchical model of Levels of design of digital systems
Focus entirely on Processor Architecture this entire semester.
Basic Concepts of Digital Images
Pixels, Definition, Role in Images, Example, Resolution, High Resolution, Low Resolution
30 fps <- calculate bandwidth width by height
Q1.

a. What is the minimum size in bytes of the frame buffer to store a frame?
   Each pixel has 3 channels.
   Each channel needs 8 bits
   Pixel needs 3 Bytes Total pixels = 1280*1024 = 1,310,720 Frame
   Buffer size= 1,310,720*3 = 3,932,160
b. How long would it take, at a minimum, for the frame to be sent over a 100 Mbit/s network?
   Choose a base -> bit 2. Unit conversion Byte to bit: 3,932,160 × 8 = 31,457,280 bit Mbit to bit: 100 * 10^6 = 10^8 bit/s 3. 31,457,280/10^8 = 0.31 seconds 1 Mbit = e^6 bit (10^6)
   E = 2.718 1 10^8 x 31,457,280

Q2.

a. Which processor has the highest performance expressed in instructions per second?
b. If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.
c. We are trying to reduce the execution time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?

3 GHz clock rate
CPI of 1.5

2.5 GHz clock rate
CPI of 1.0

4.0 GHz clock rate
CPI of 2.2

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Performance = (1 / Execution time)
Execution time = CPU clock cycles x clock cycle time
Execution time = CPU clock cycles / clock rate
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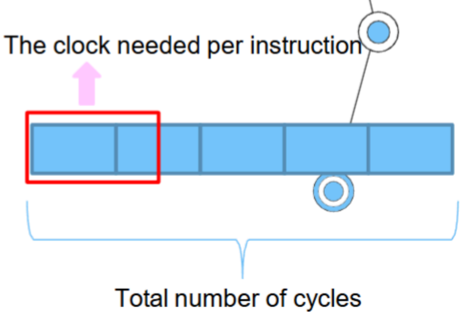
performance of P1 (instructions/sec) = 3 × 10^9/1.5 = 2 × 10^9
performance of P2 (instructions/sec) = 2.5 × 10^9/1.0 = 2.5 × 10^9
performance of P3 (instructions/sec) = 4 × 10^9/2.2 = 1.8 × 10^9

cycles(P1) = 10 × 3 × 10^9 = 30 × 10^9
cycles(P2) = 10 × 2.5 × 10^9 = 25 × 10^9
cycles(P3) = 10 × 4 × 10^9 = 40 × 10^9

No. instructions(P1) = 30 × 10^9/1.5 = 20 × 10_9
No. instructions(P2) = 25 × 10_9/1 = 25 × 10_9
No. instructions(P3) = 40 × 10_9/2.2 = 18.18 × 10_9



Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes according to their CPI (class A, B, C, and D). P1 with a clock rate of 2.5 GHz and CPIs of 1, 2, 3, and 3, and P2 with a clock rate of 3 GHz and CPIs of 2, 2, 2, and 2. a. Given a program with a dynamic instruction count of 1.0E6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D, which implementation is faster? b. b. What is the global CPI for each implementation? c. Find the clock cycles required in both cases.

Q3. a.

Instructions type:
A,B,C,D

	A	B	C	D	CR(GHz)
P1 CPI	1	2	3	3	2.5
P2 CPI	2	2	2	2	3

Class A: 10^5 instr.
Class B: 2 × 10^5 instr.
Class C: 5 × 10^5 instr.
Class D: 2 × 10^5 instr.
Time = No. instr. × CPI / clock rate
Total time P1 = (10^5 + 2 × 10^5 × 2 + 5 × 10^5 × 3 + 2 × 10^5 × 3)/(2.5 × 10^9) = 10.4 × 10^-4 s
Total time P2 = (10^5 × 2 + 2 × 10^5 × 2 + 5 × 10^5 × 2 + 2 × 10^5 × 2)/(3 × 10^9) = 6.66 × 10^-4 s

1	1
10^5	x

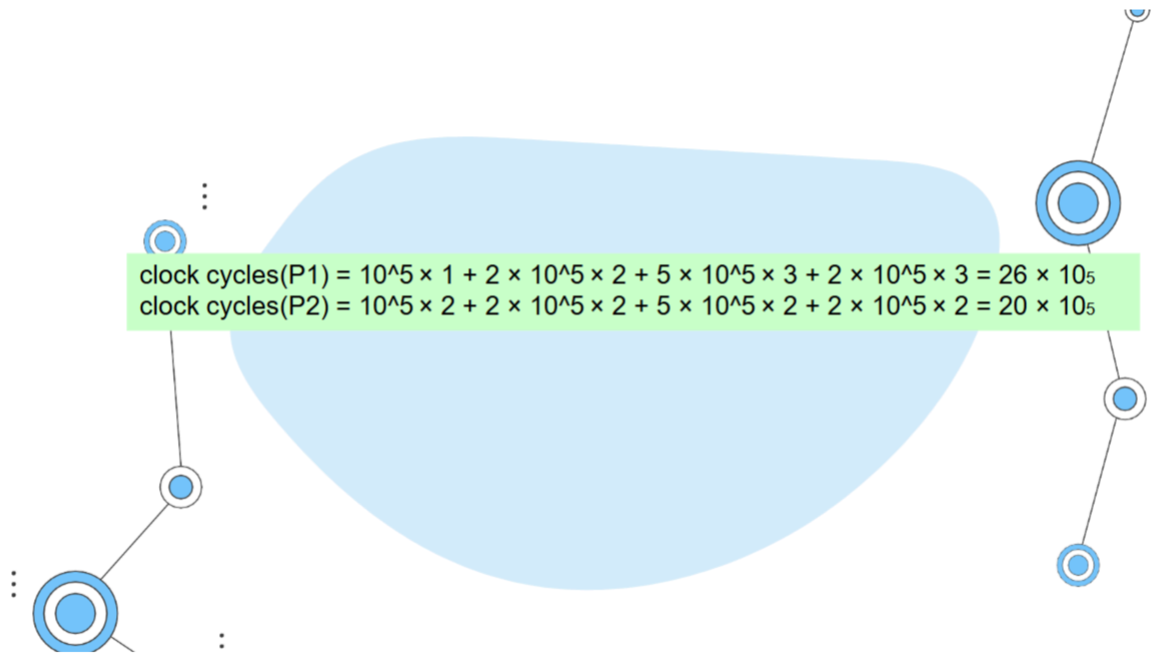
P2 is faster

Q3. b.

Execution time = Instruction Count x CPI / clock rate

CPI = time * clock rate / instruction count

CPI(P1) = 10.4 × 10^-4 × 2.5 × 10^9/10^6 = 2.6
CPI(P2) = 6.66 × 10^-4 × 3 × 10^9/10^6 = 2.0



Consider two different implementations of the same instruction set architecture.
The instructions can be divided into four classes according to their CPI (class A, B, C, and D).
P1 with a clock rate of 2.8 GHz and CPIs of 2,3,1, and 2, and P2 with a clock rate of 1.7 GHz and CPIs of 2,1,1, and 2.

a.

Given a program with a dynamic instruction count of 1.0E6 instructions divided into classes as follows: 5% class A, 25% class B, 60% class C, and 10% class D, which implementation is faster?

(Please include the formulas and procedure for calculations.)

- P1
  - Clock Rate: 2.8 GHz
  - CPI for classes A, B, C, D: 2, 3, 1, 2

- P2
  - Clock Rate: 1.7 GHz
  - CPI for classes A, B, C, D: 2, 1, 1, 2

- Instruction Mix (Total = 1,000,000 instructions):
  - Class A: 5% = 50,000

  - Class B: 25% = 250,000

- Class C: 60% = 600,000

- Class D: 10% = 100,000

Formula:

CPU Time = (Sum of Instruction Count × CPI per class) / Clock Rate

P1 Total Cycles:

(50,000 × 2) + (250,000 × 3) + (600,000 × 1) + (100,000 × 2)
= 100,000 + 750,000 + 600,000 + 200,000
= 1,650,000 cycles

P1 Execution Time:
1,650,000 / (2.8 × 10^9)
= 0.000589 seconds

P2 Total Cycles:

(50,000 × 2) + (250,000 × 1) + (600,000 × 1) + (100,000 × 2)
= 100,000 + 250,000 + 600,000 + 200,000
= 1,150,000 cycles

P2 Execution Time:
1,150,000 / (1.7 × 10^9)
= 0.000676 seconds