NOTES:

REV	DATE	PAGES	DESCRIPTION
A	2018/Apr/04		Initial
B	2018/May/05		Update R14/R315 Pull up Power
D	2021/Mar/25		
E	2021/Apr/26		Update the HP VCCO

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Clock Diagram

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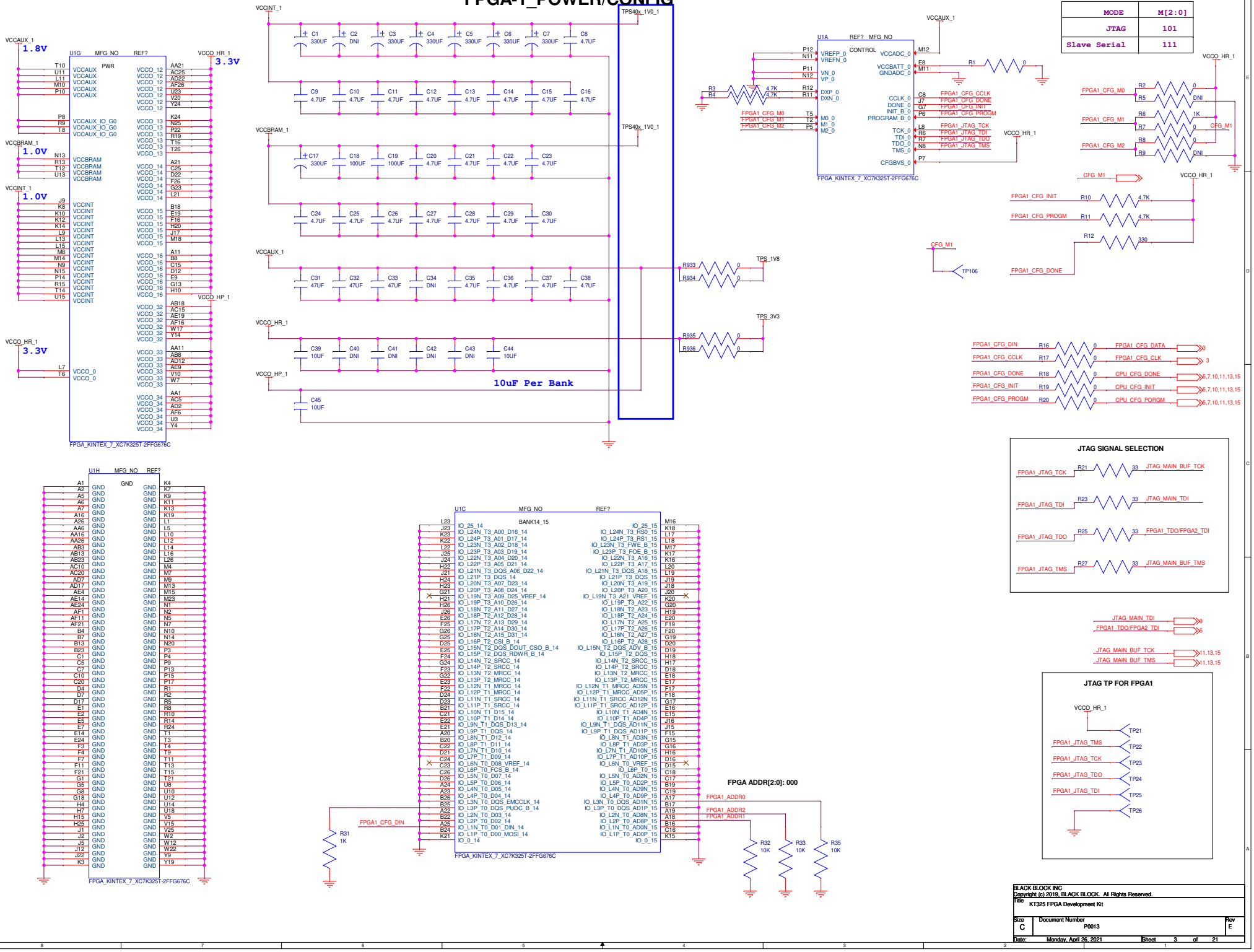
FPGA-1_POWER/CONFIG



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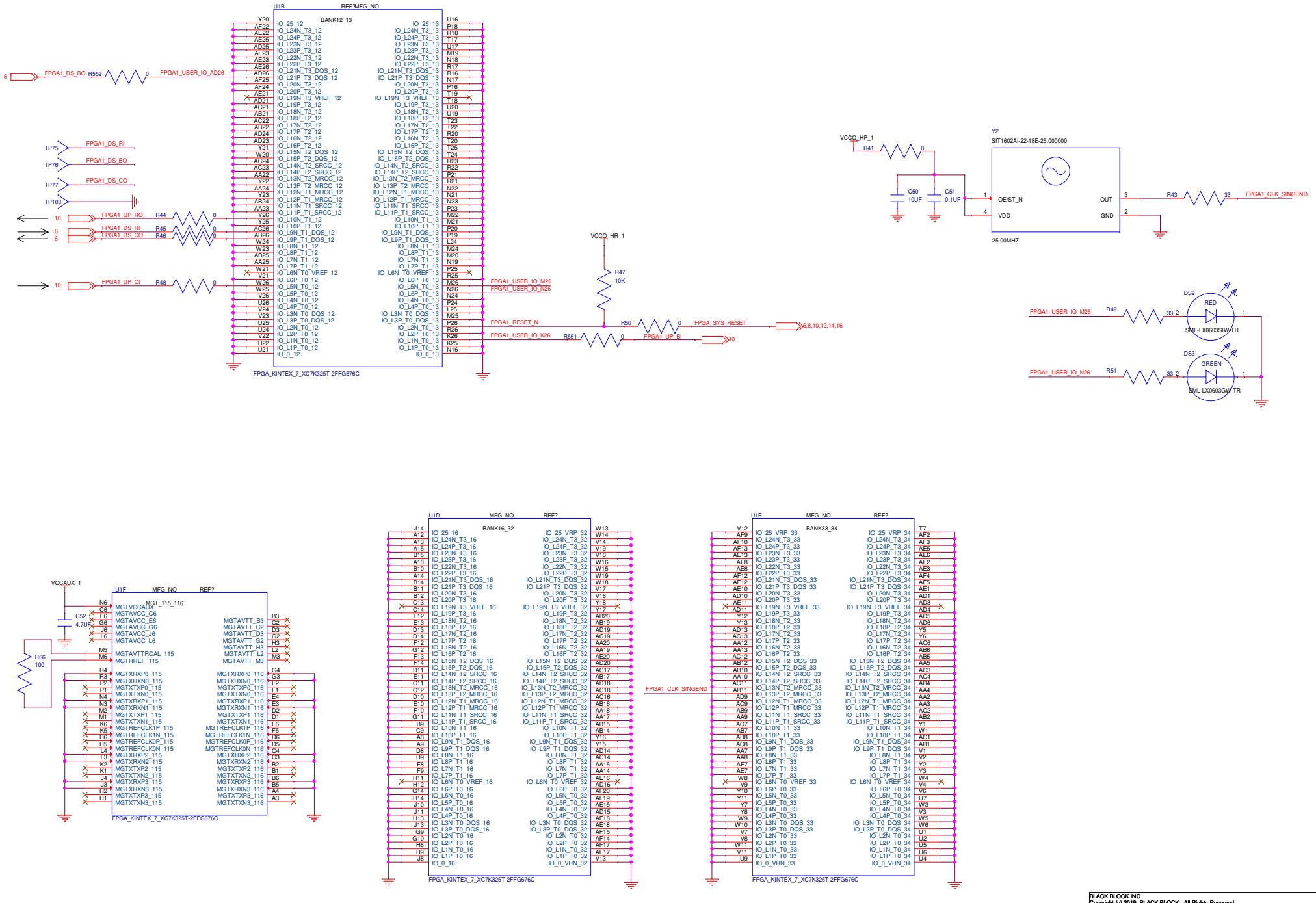
FPGA-1_IO_BANK



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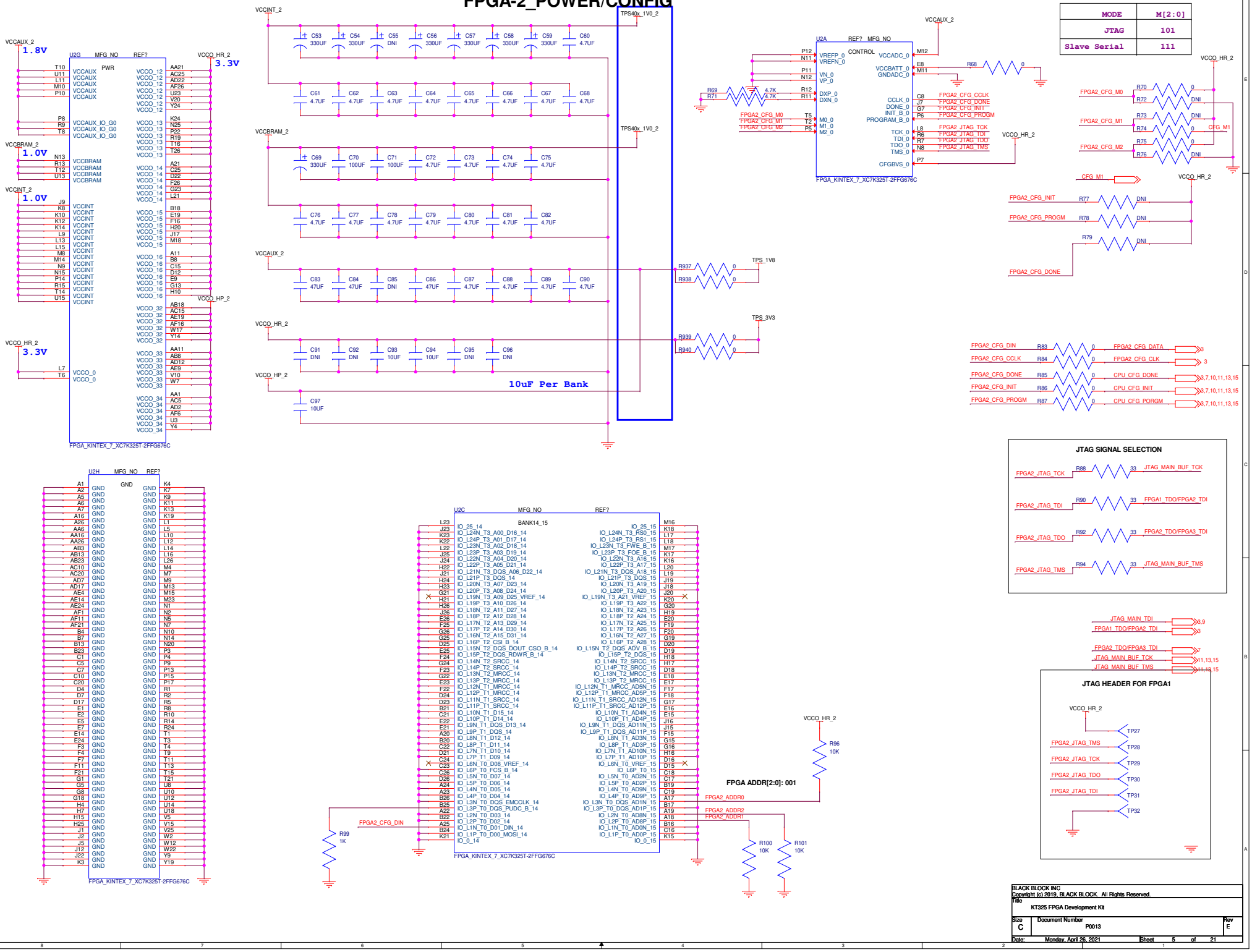
FPGA-2_POWER/CONFIG



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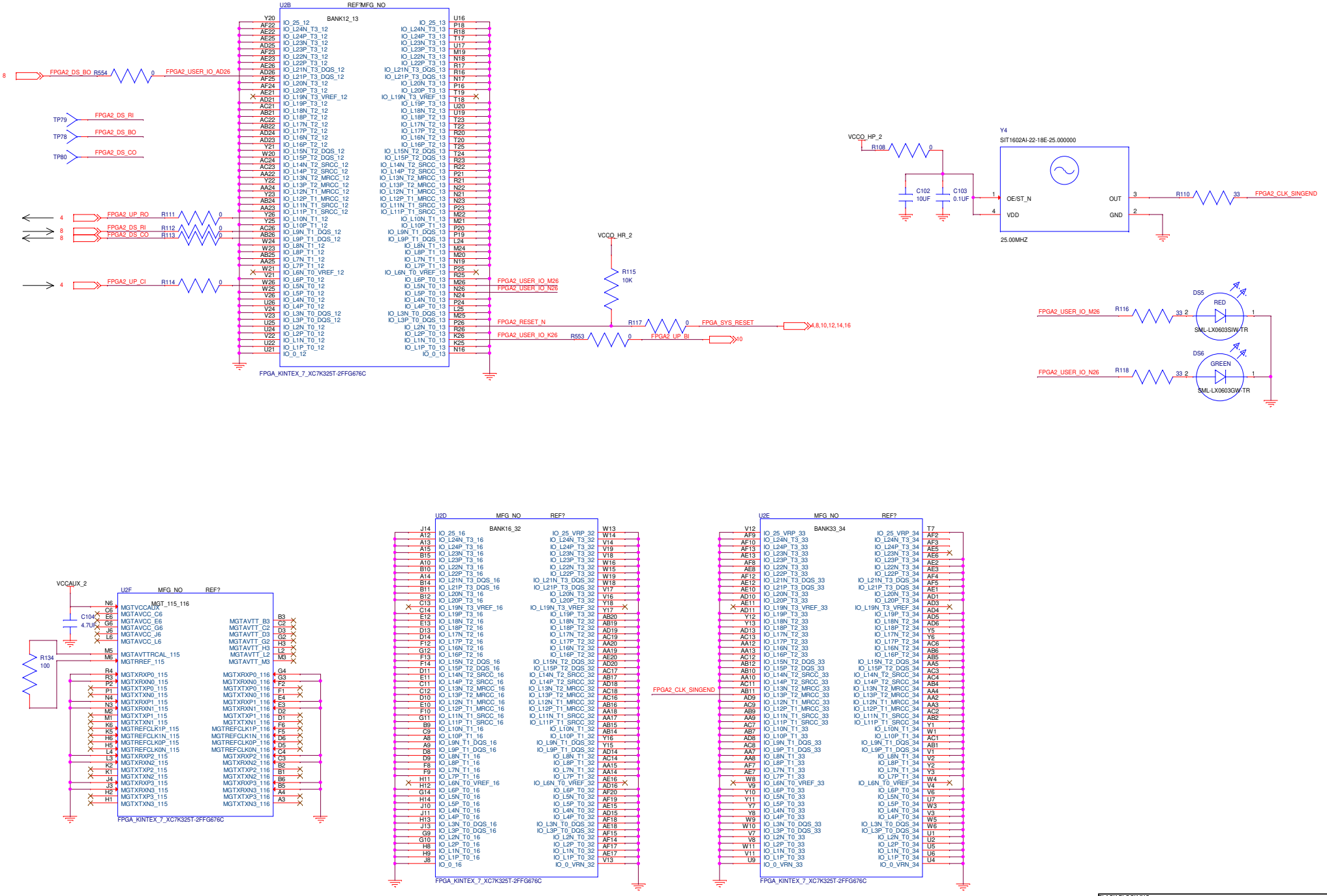
FPGA-2_IO_BANK



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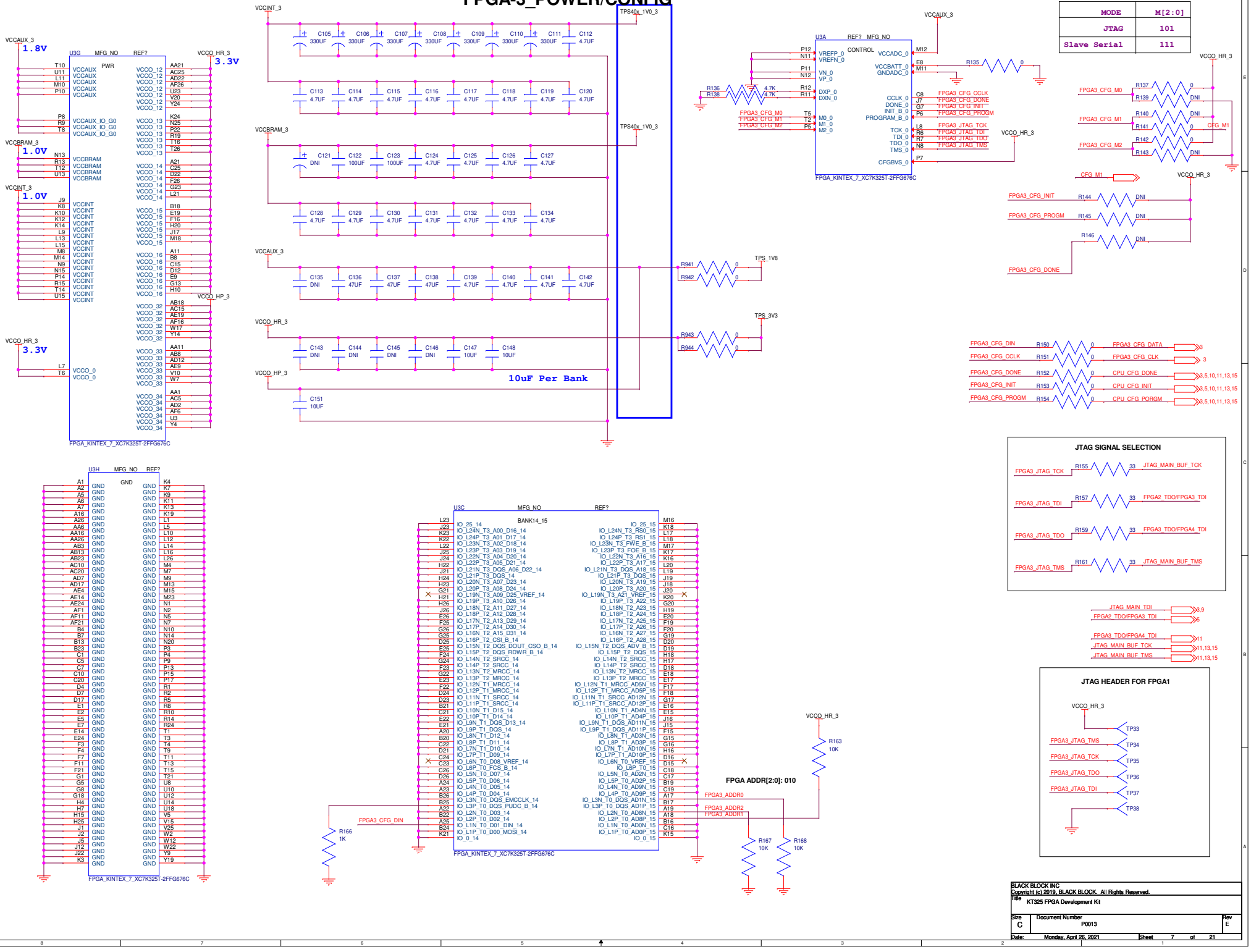
FPGA-3_POWER/CONFIG



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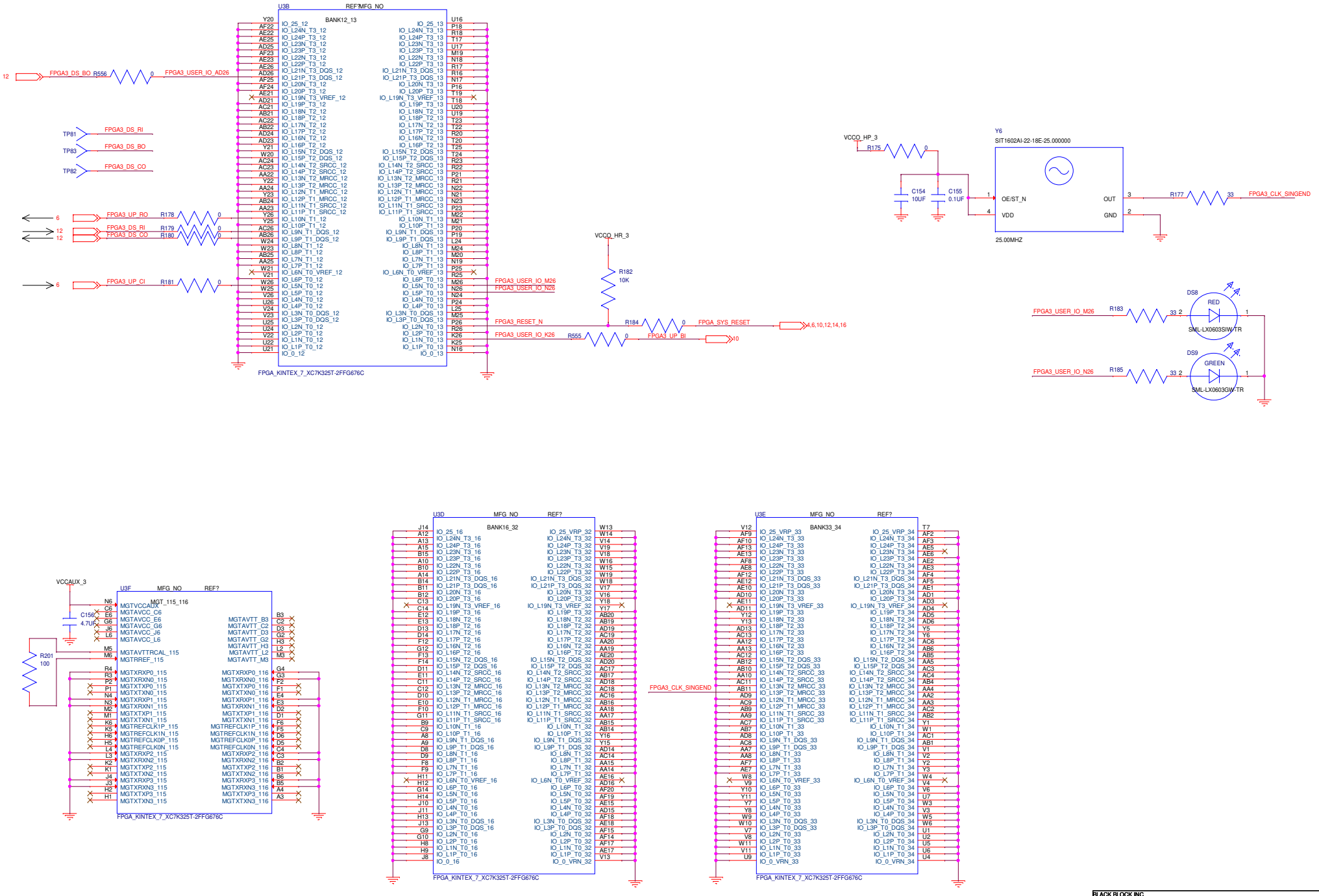
FPGA-3_IO_BANK



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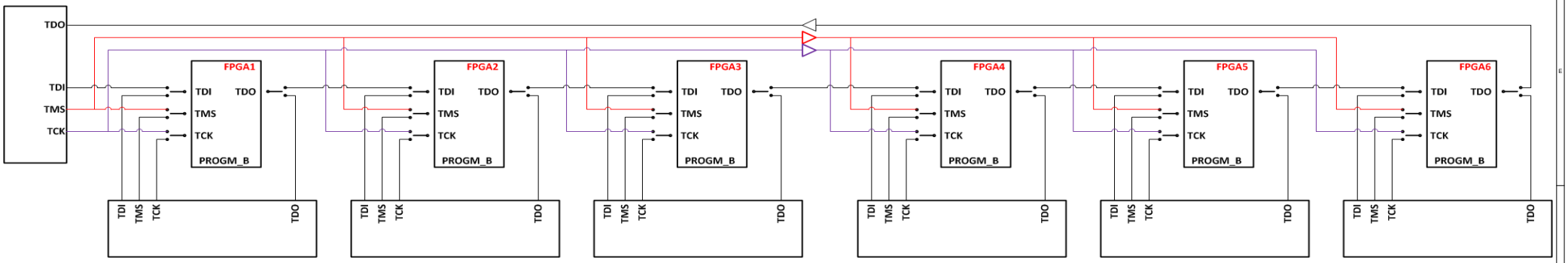
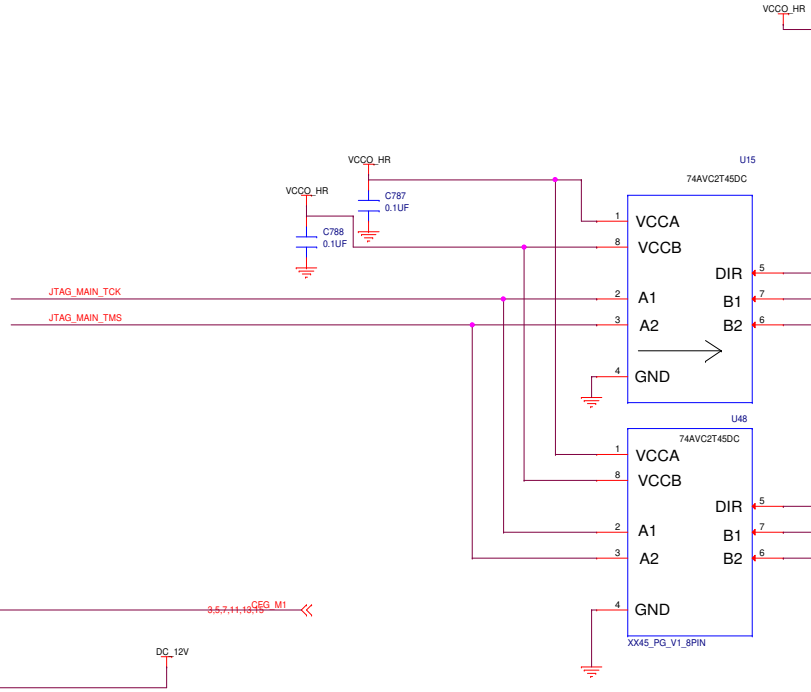
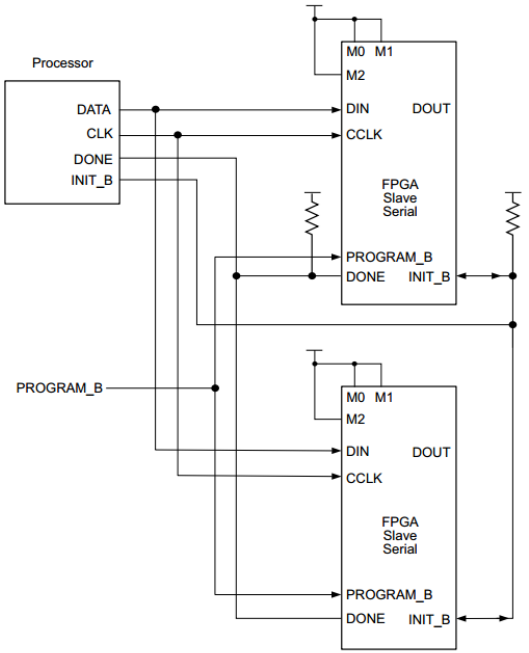
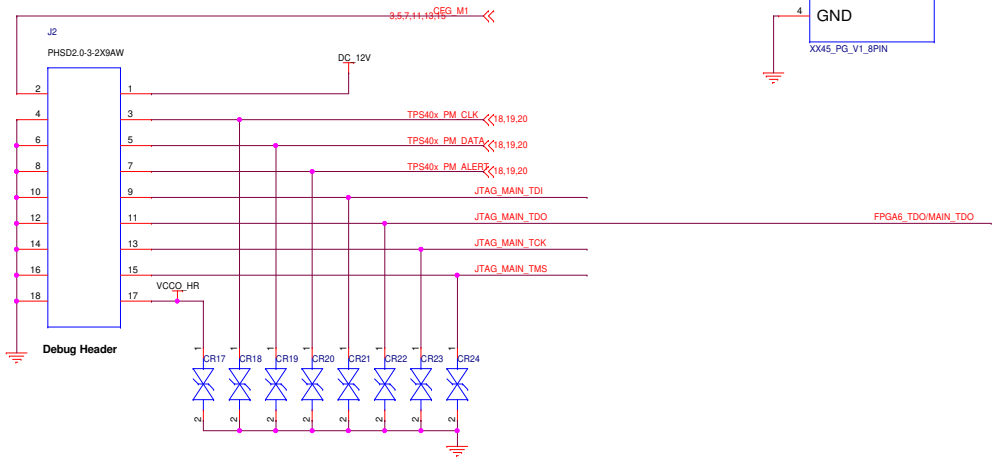
FPGA_CFG_JTAG_LINK





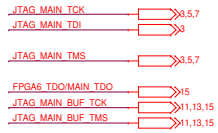




1. The DONE pin is an open-drain output.
2. The INIT_B pin is a bidirectional, open-drain pin. An external pull-up resistor is required.
3. The startup clock setting must be set for CCLK for serial configuration.
4. For ganged serial configuration, all devices must be identical (same IDCODE) and must be configured with the same bitstream. If all devices are set for Slave Serial mode, the DONE pins can be disconnected if the external CCLK source continues toggling until all DONE pins go High.

UG470_c09_02_041715

JTAG



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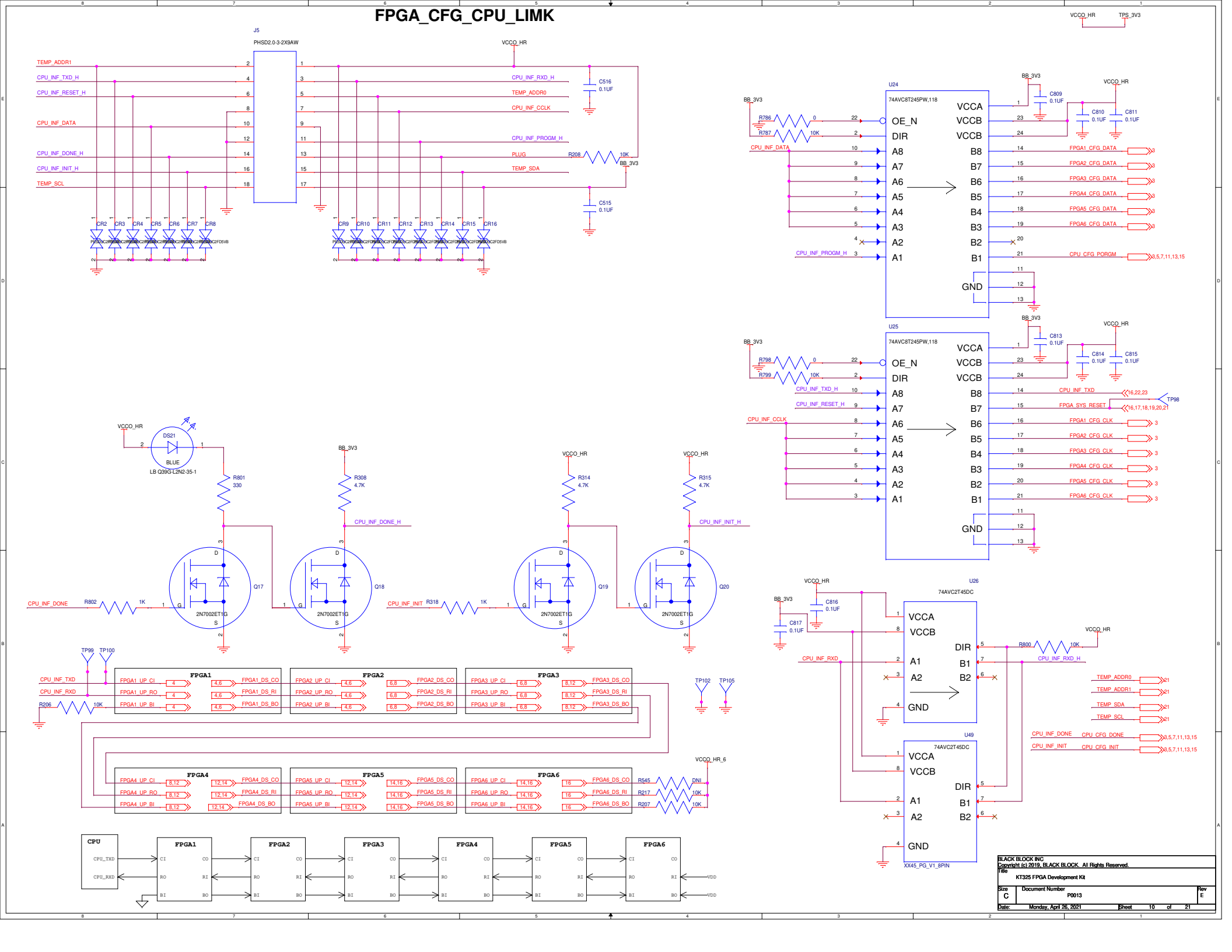
FPGA_CFG_CPU_LIMK



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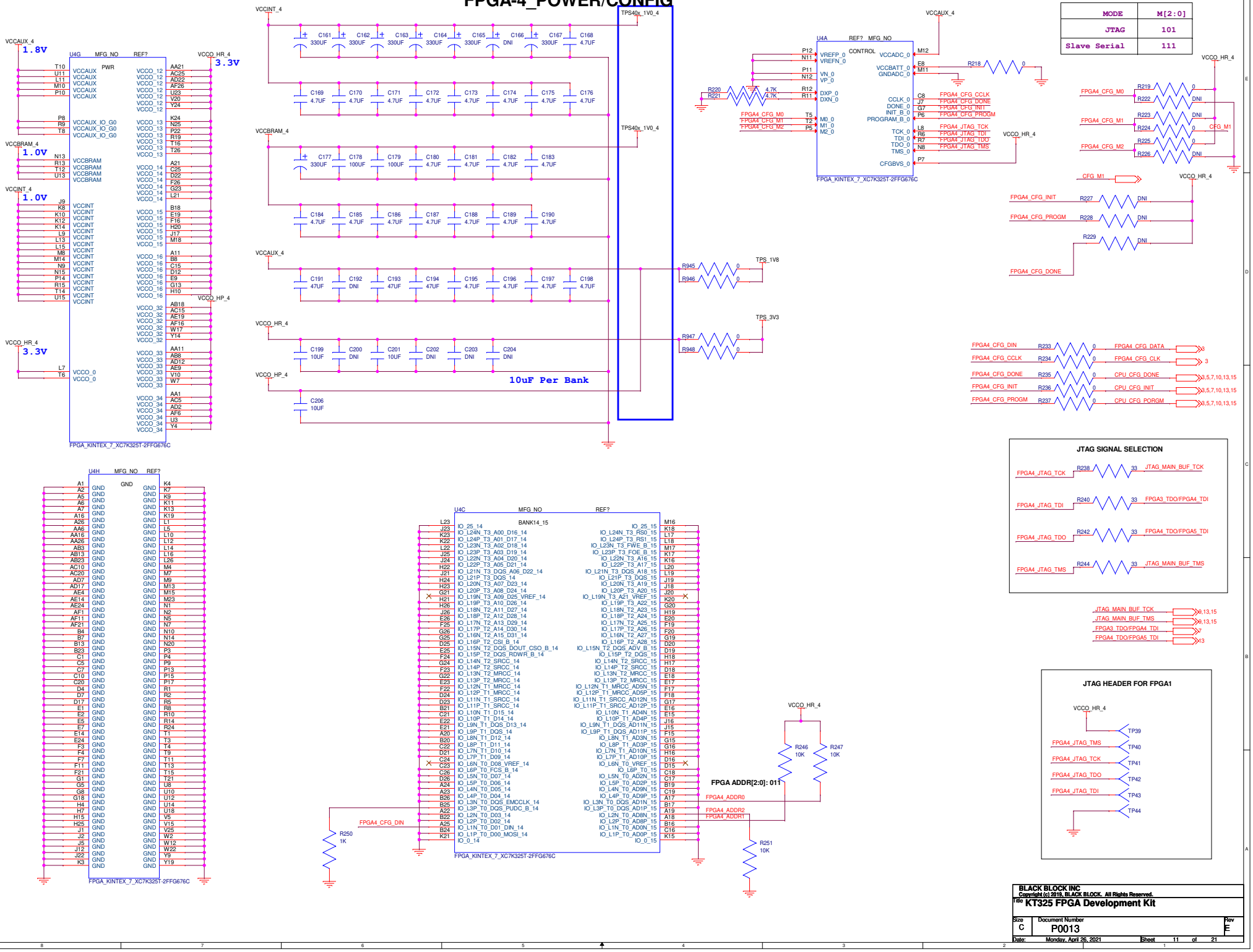
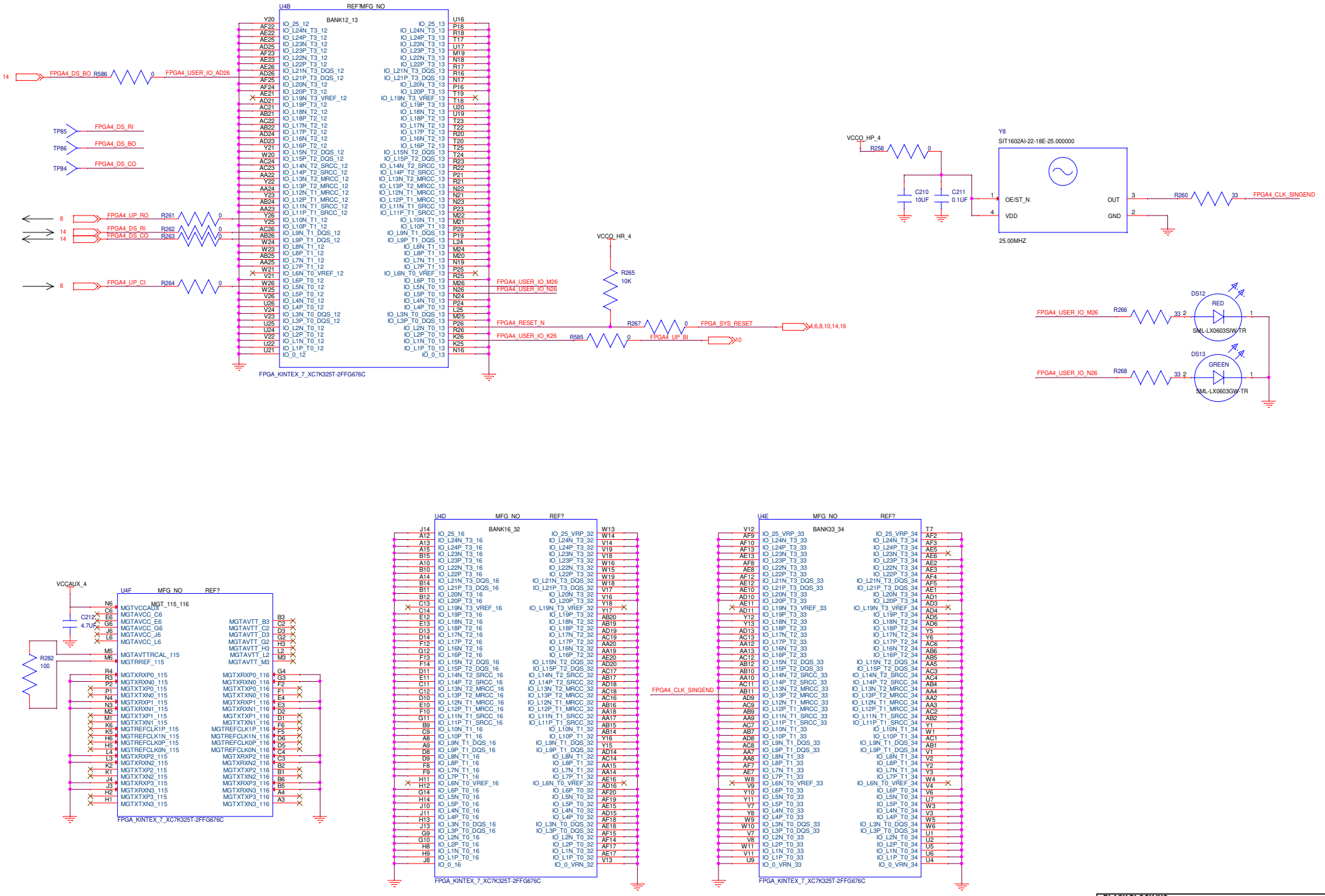
FPGA-4_POWER/CONFIG



FPGA-4_IO_BANK



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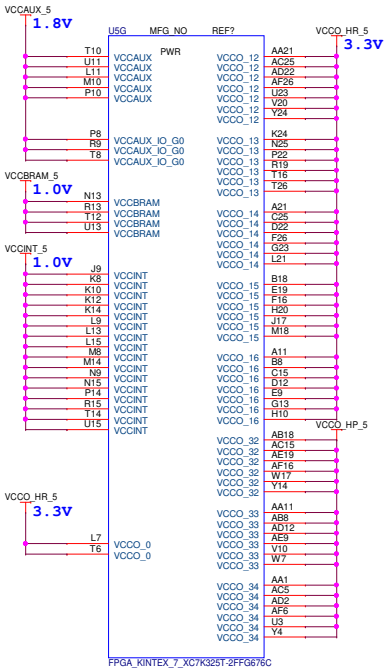
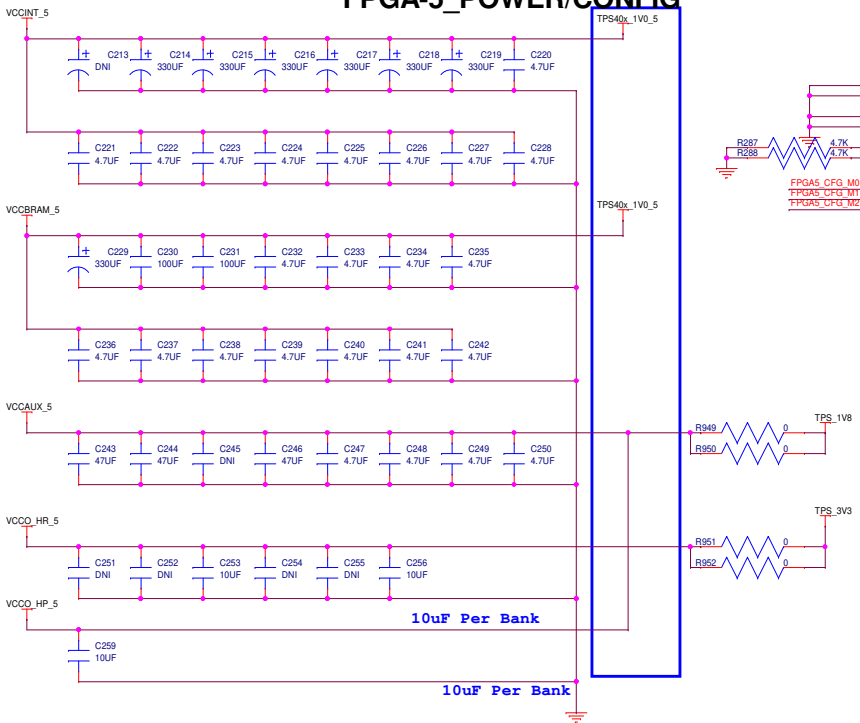
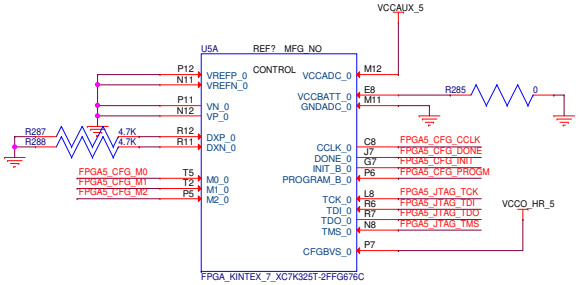
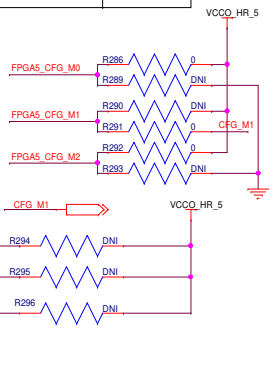
FPGA-5_POWER/CONFIG

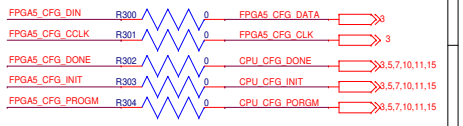


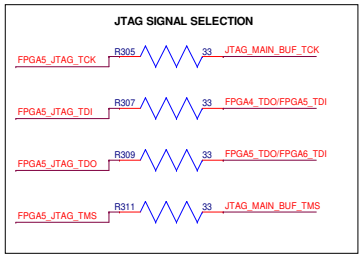


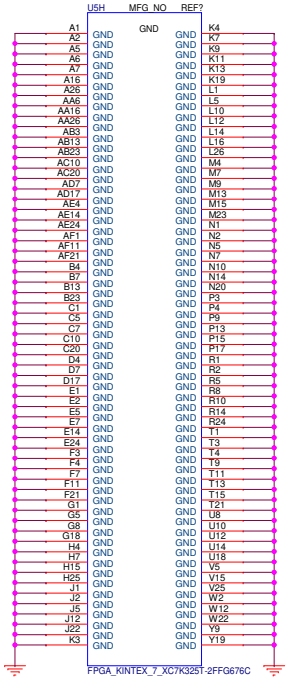


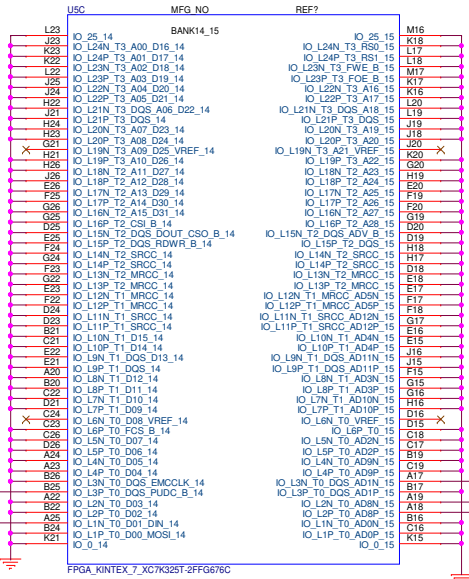
MODE	M[2:0]
JTAG	101
Slave Serial	111

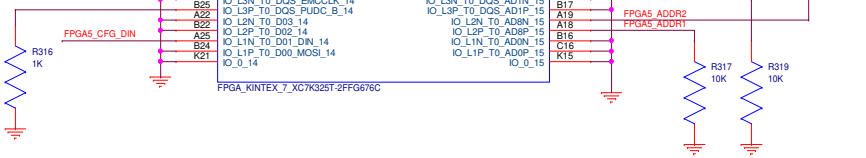


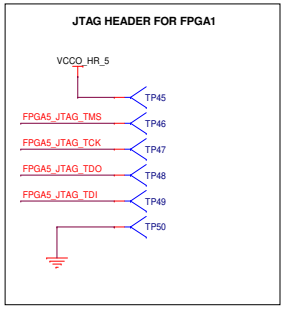












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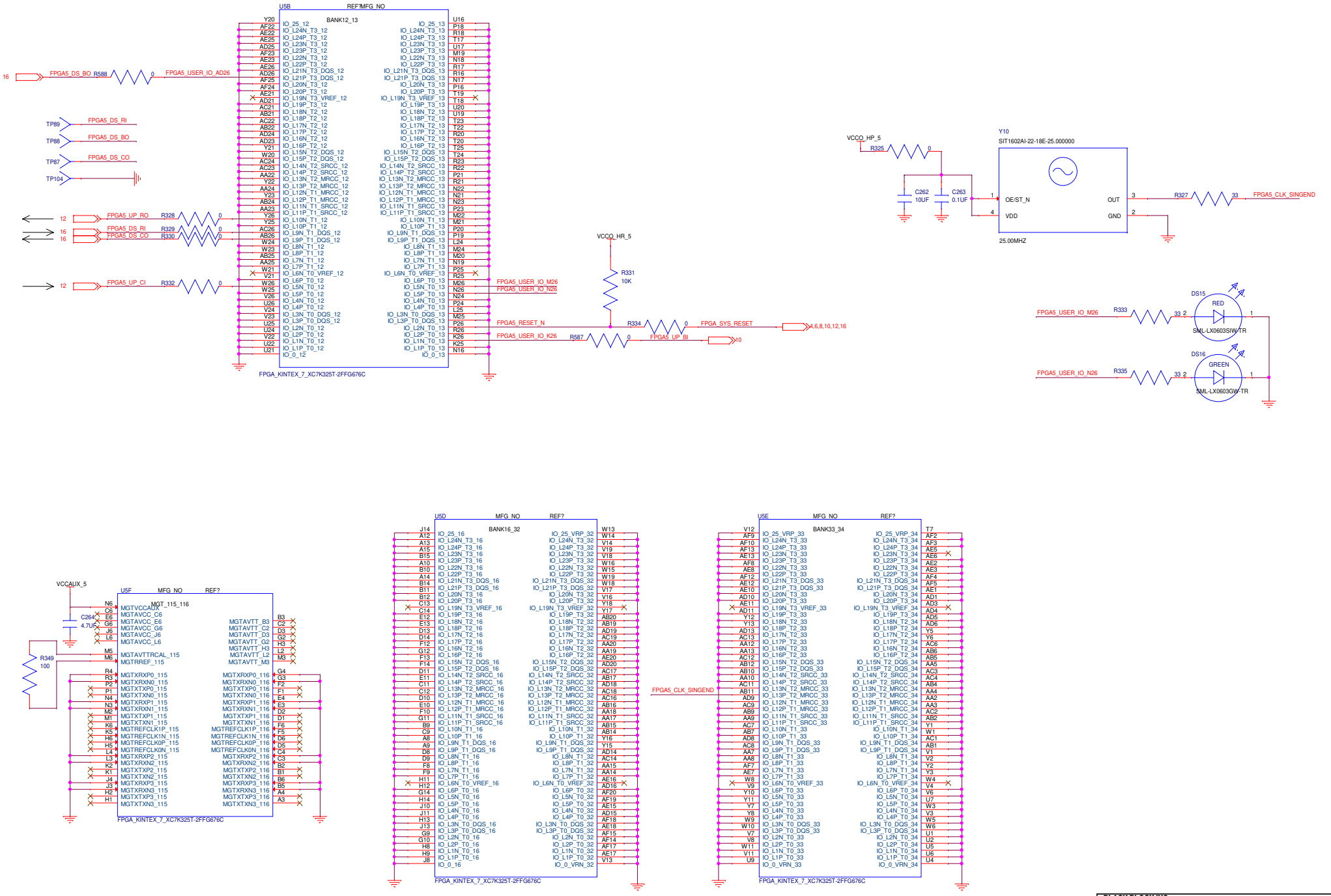
FPGA-5_IO_BANK



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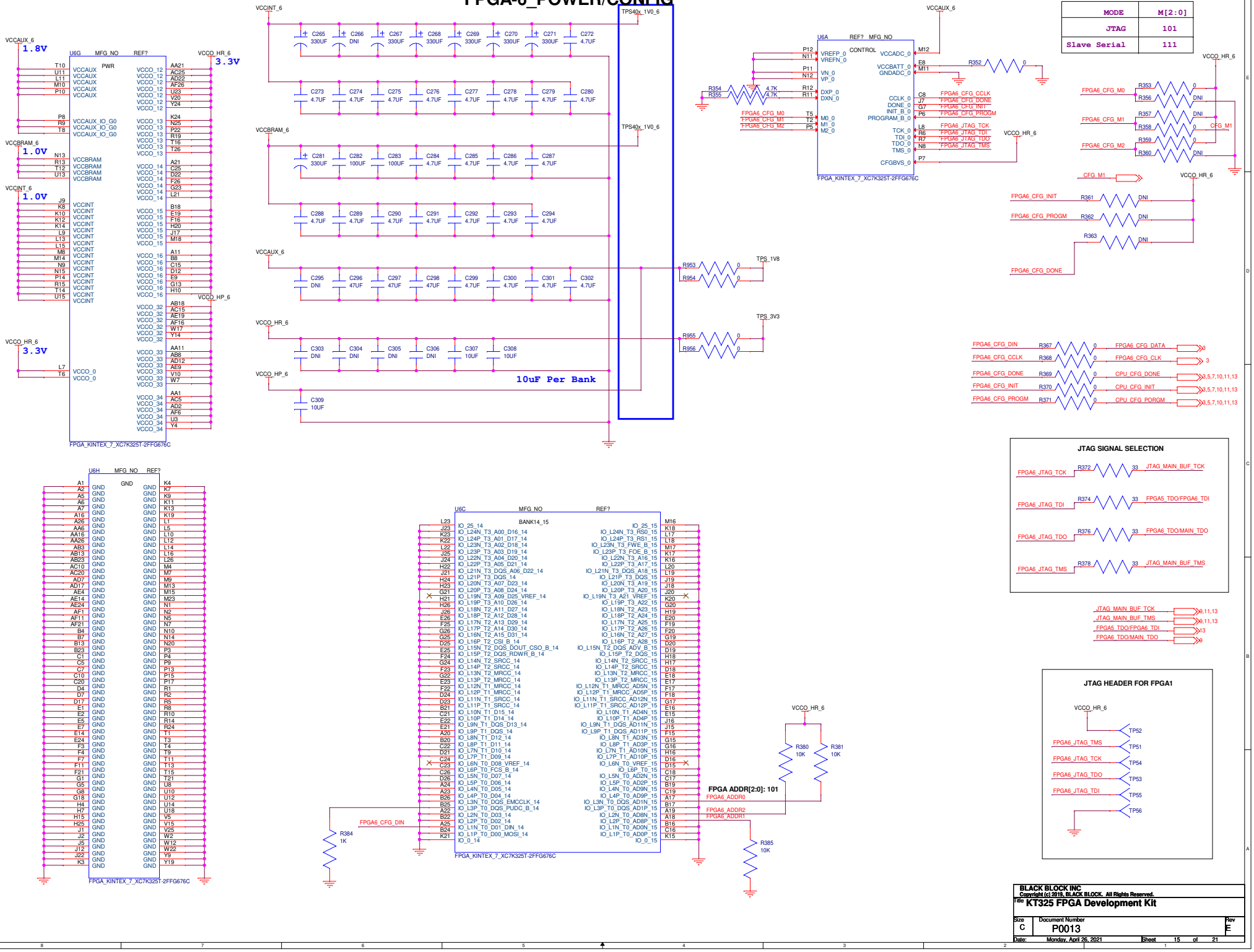
FPGA-6_POWER/CONFIG



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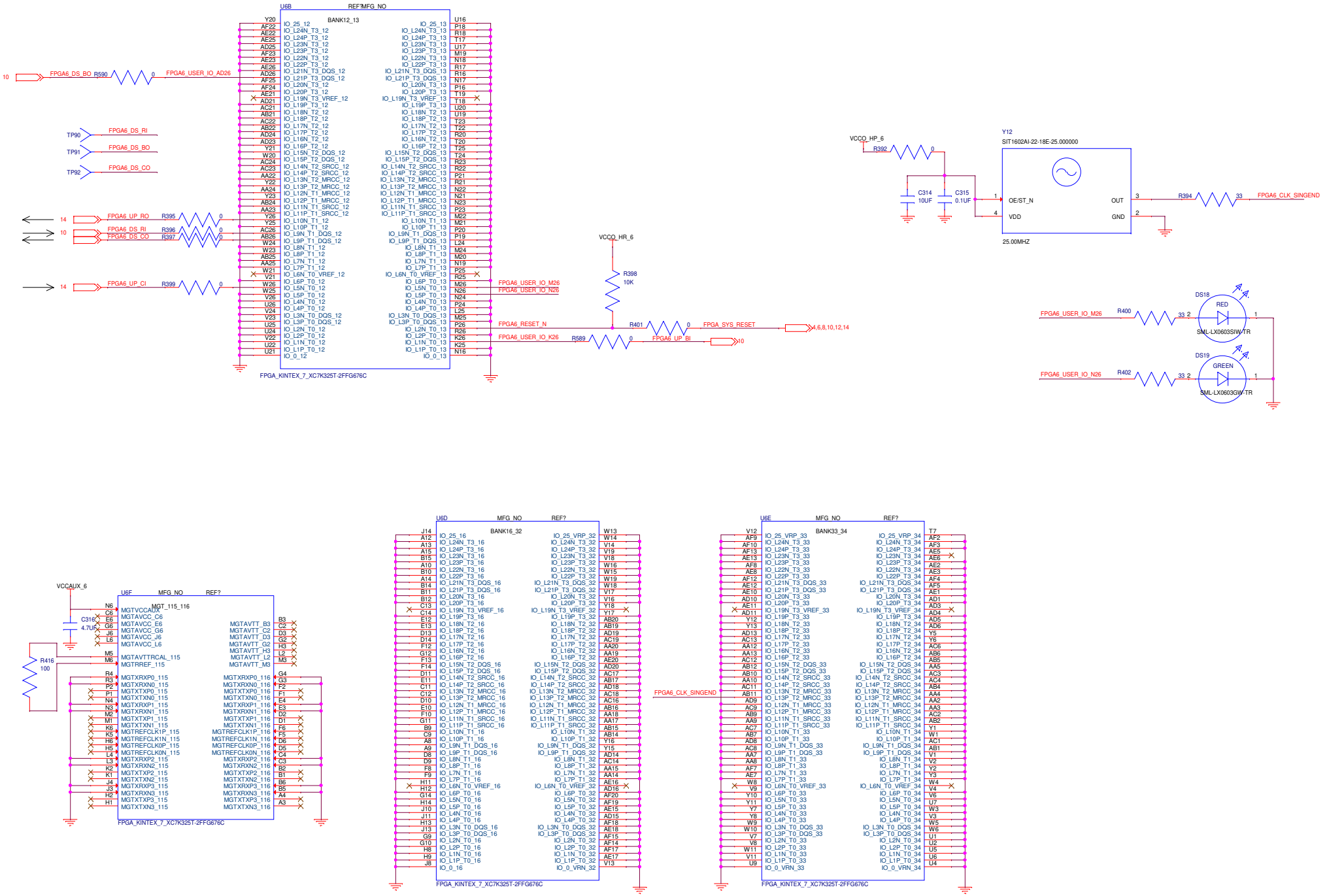
FPGA-6_IO_BANK



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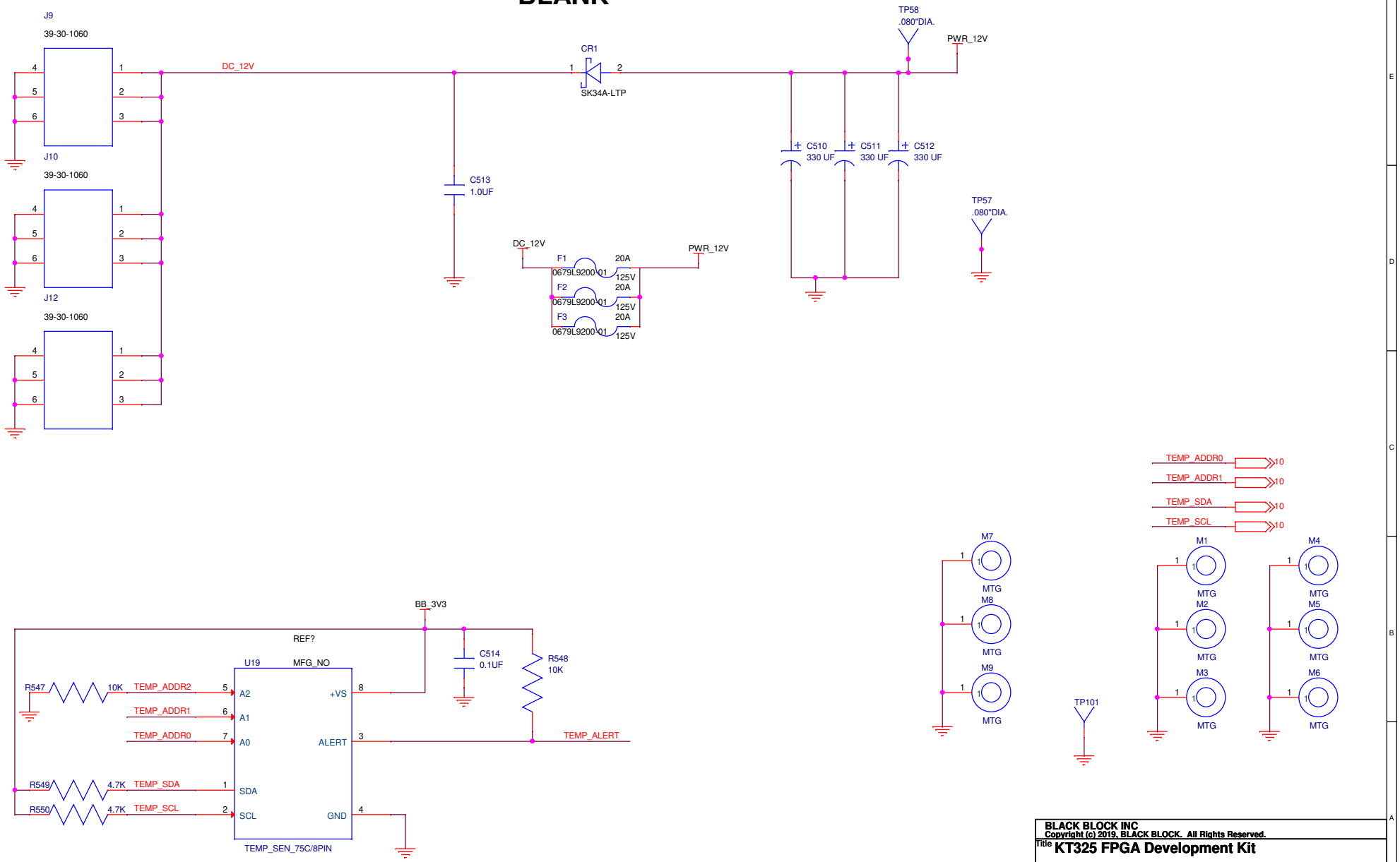

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