

NOTES:

PAGE	DESCRIPTION	PAGE	DESCRIPTION
1	Title, Notes, Block Diagram, Rev. History	37	
2	Clock Diagram	38	
3	FPGA-1_POWER/CONFIG	39	
4	FPGA-1_IO_BANK	40	
5	FPGA-2_POWER/CONFIG	41	
6	FPGA-2_IO_BANK	42	
7	FPGA-3_POWER/CONFIG	43	
8	FPGA-3_IO_BANK	44	
9	FPGA_CFG_JTAG_LINK	45	
10	FPGA_CFG_CPU_LINK	46	
11	FPGA-4_POWER/CONFIG	47	
12	FPGA-4_IO_BANK	48	
13	FPGA-5_POWER/CONFIG	49	
14	FPGA-5_IO_BANK	50	
15	FPGA-6_POWER/CONFIG	51	
16	FPGA-6_IO_BANK	52	
17	POWER_1V0_1/2	53	
18	POWER_1V0_3/4	54	
19	POWER_1V0_5/6	55	
20	DC12VIN/1V8/3V3	56	
21	TEMPSENSOR	57	
22		58	
23		59	
24		60	
25		61	
26		62	
27		63	
28		64	
29		65	
30		66	
31		67	
32		68	
33			
34			
35			
36			

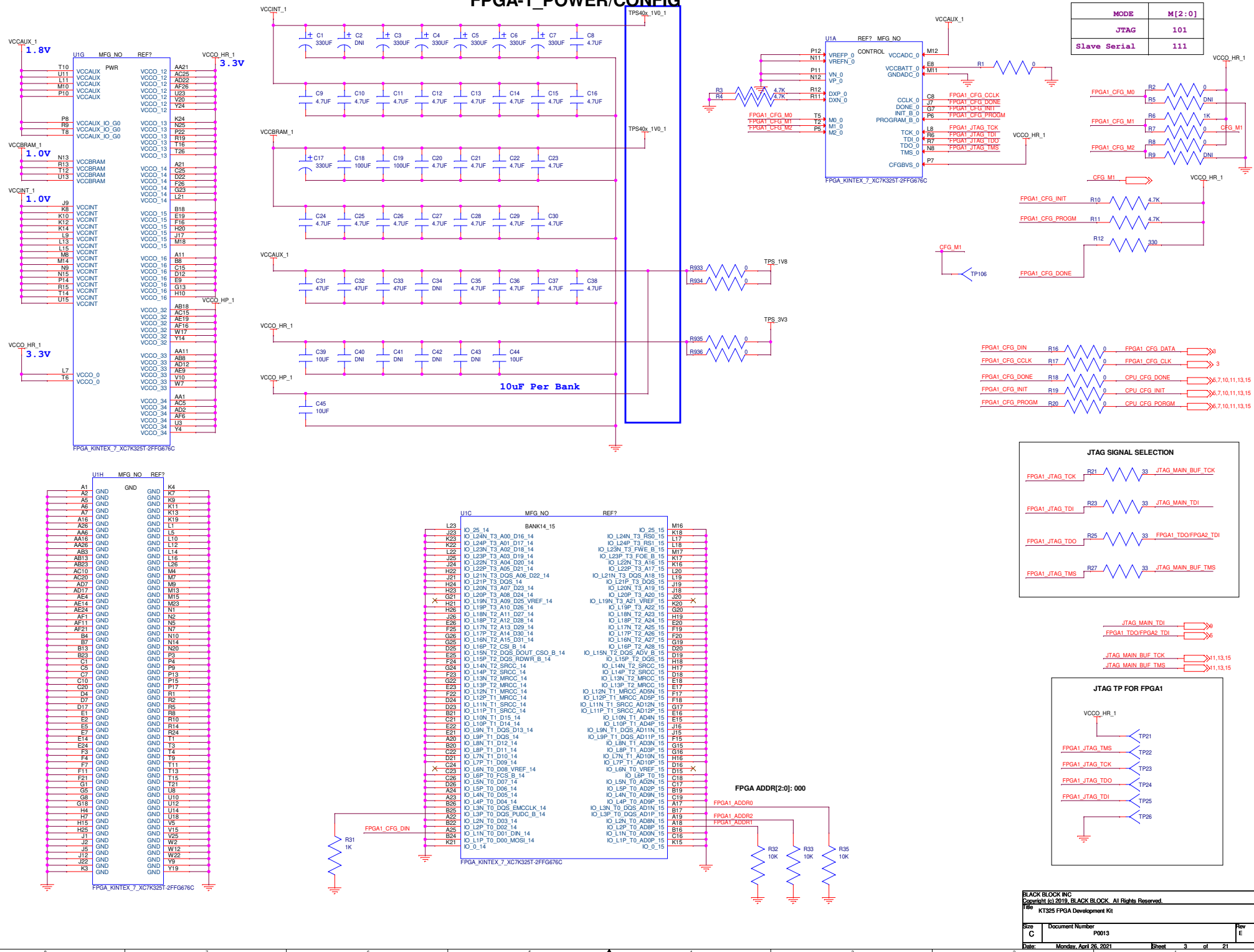
REV	DATE	PAGES	DESCRIPTION
A	2018/Apr/04		Initial
B	2018/May/05		Update R14/R315 Pull up Power
D	2021/Mar/25		
E	2021/Apr/26		Update the HP_VCCO

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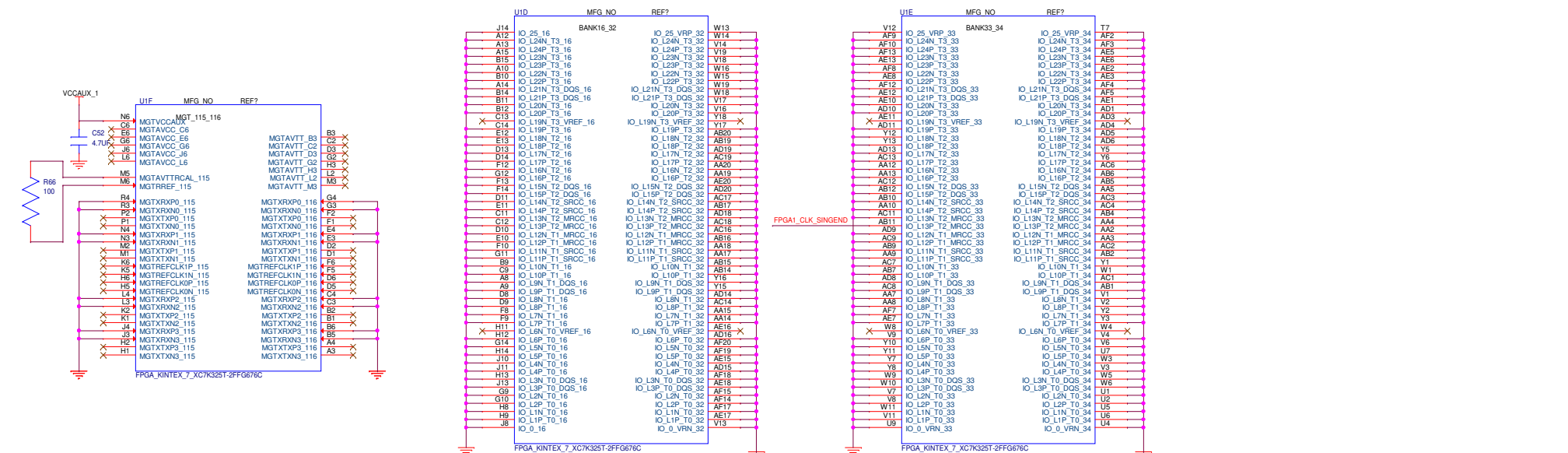
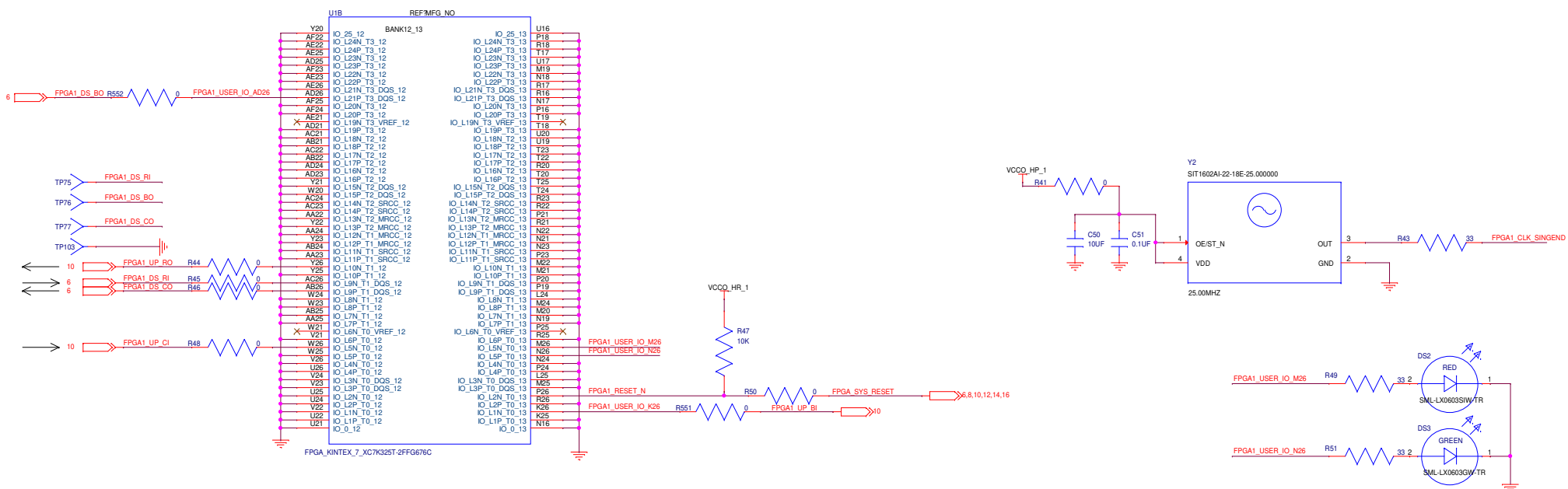
# Clock Diagram

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Title			
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Size	Document Number		Rev
B	P0013		E
Date:	Monday, April 26, 2021	Sheet	2 of 21

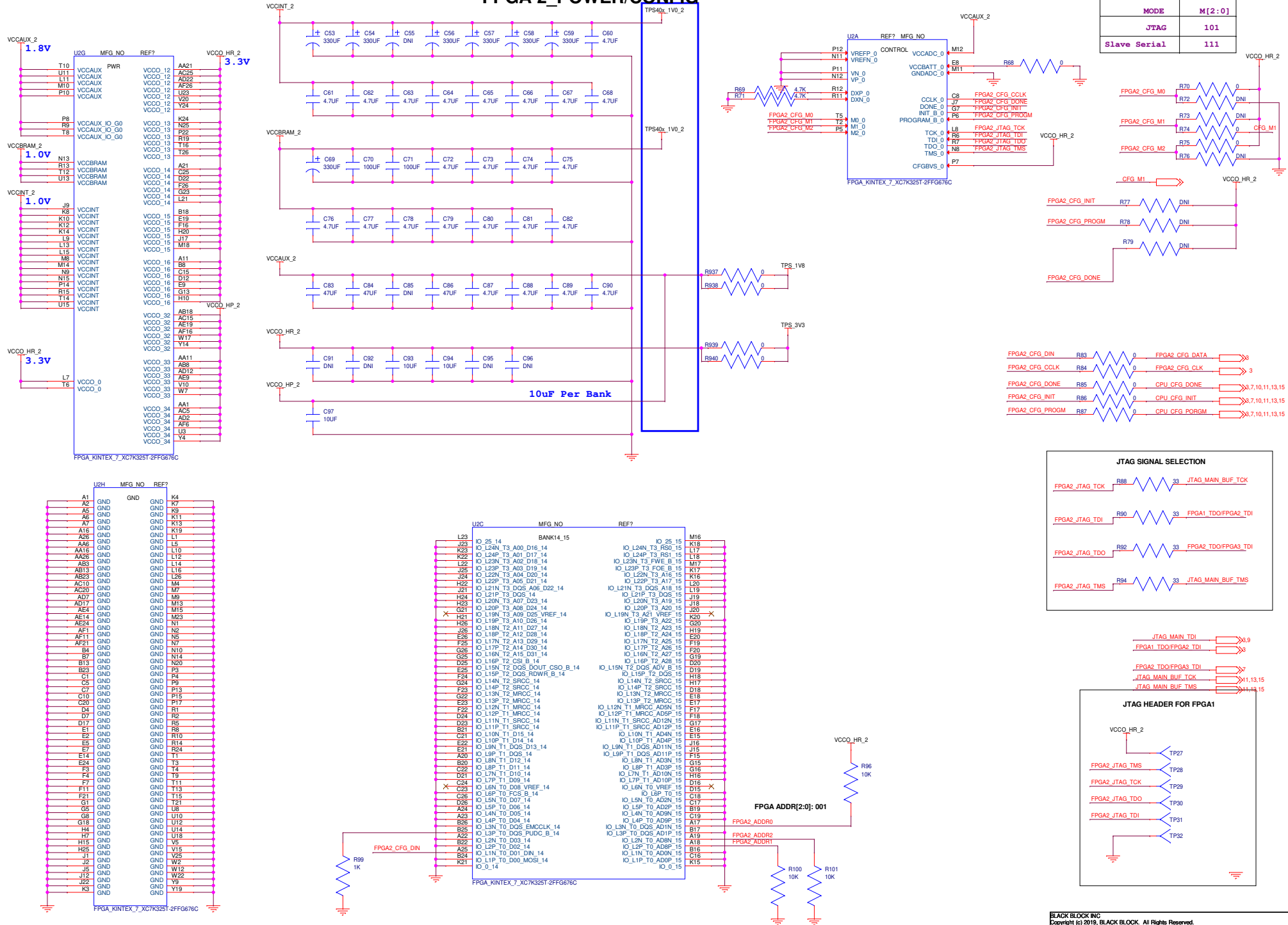
## FPGA-1 POWER/CONFIG



**FPGA-1 IO BANK**



# FPGA-2\_POWER/CONFIG



MODE	M[2:0]
JTAG	101
Slave Serial	111

FPGA2_CFG_M0	R70	0	DNI
FPGA2_CFG_M1	R72	0	DNI
FPGA2_CFG_M2	R73	0	DNI
FPGA2_CFG_M3	R74	0	DNI
FPGA2_CFG_M4	R75	0	DNI
FPGA2_CFG_M5	R76	0	DNI
FPGA2_CFG_M6	R77	0	DNI
FPGA2_CFG_M7	R78	0	DNI
FPGA2_CFG_M8	R79	0	DNI
FPGA2_CFG_M9	R80	0	DNI
FPGA2_CFG_M10	R81	0	DNI
FPGA2_CFG_M11	R82	0	DNI
FPGA2_CFG_M12	R83	0	DNI
FPGA2_CFG_M13	R84	0	DNI
FPGA2_CFG_M14	R85	0	DNI
FPGA2_CFG_M15	R86	0	DNI
FPGA2_CFG_M16	R87	0	DNI

JTAG_MAIN_TCK	R88	33	JTAG_MAIN_BUF_TCK
FPGA2_JTAG_TDI	R89	33	FPGA1_TDO/FPGA2_TDI
FPGA2_JTAG_TDO	R90	33	FPGA2_TDO/FPGA3_TDI
FPGA2_JTAG_TMS	R91	33	JTAG_MAIN_BUF_TMS

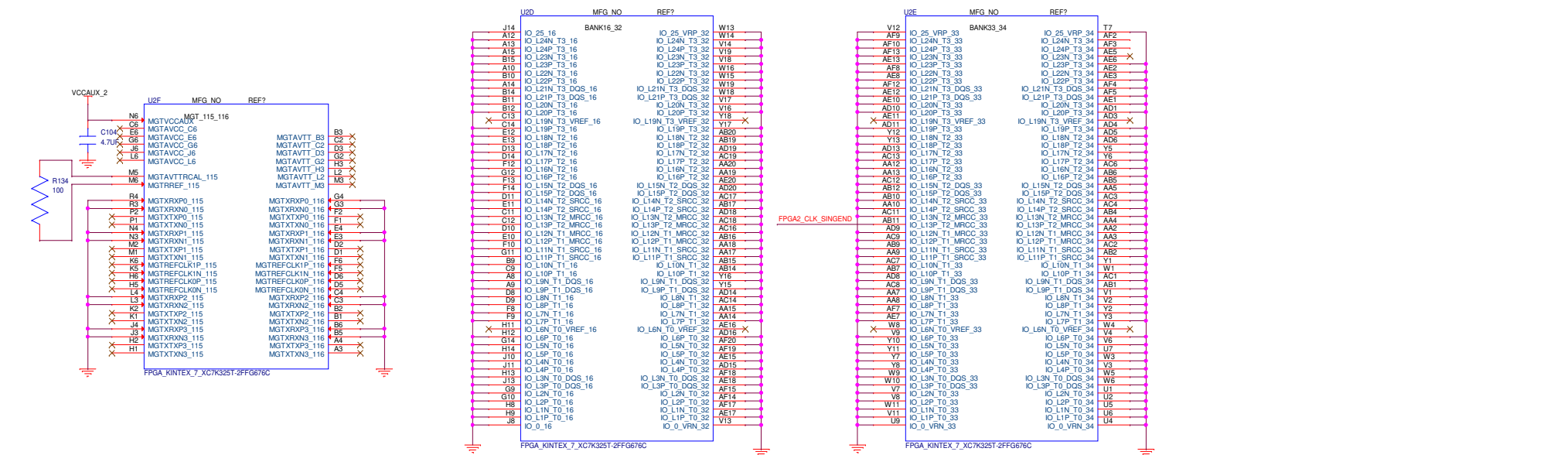
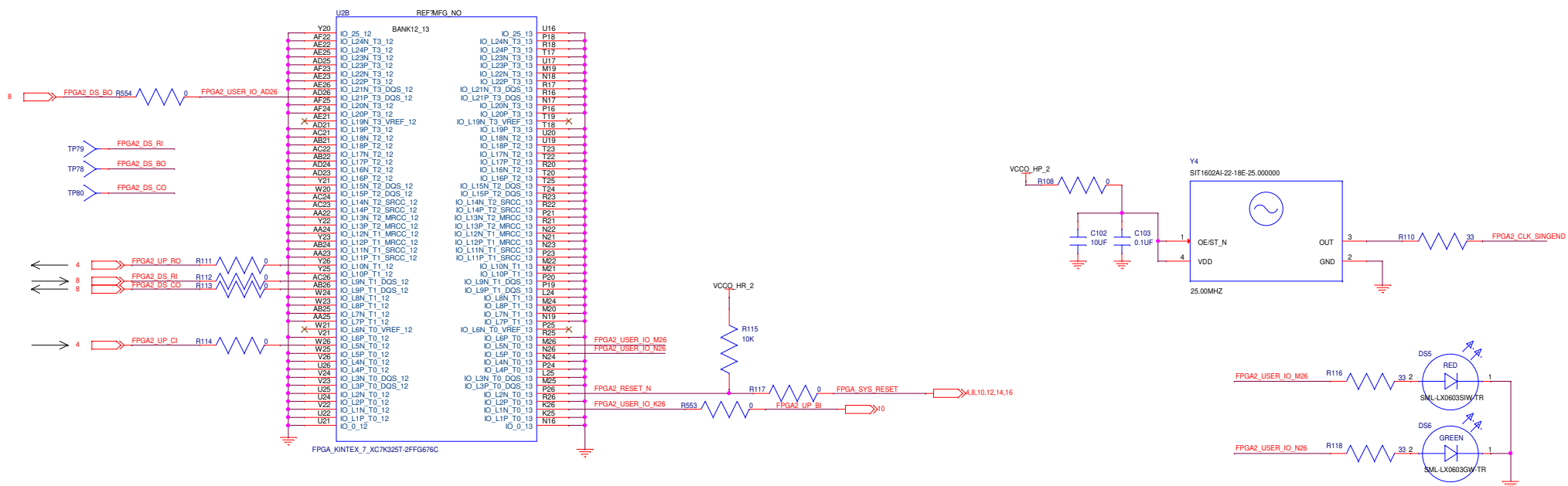
  

JTAG_MAIN_TDI	R92	33	JTAG_MAIN_BUF_TDI
FPGA1_TDO/FPGA2_TDI	R93	33	FPGA2_TDO/FPGA3_TDI
JTAG_MAIN_BUF_TCK	R94	33	JTAG_MAIN_BUF_TCK
JTAG_MAIN_BUF_TMS	R95	33	JTAG_MAIN_BUF_TMS

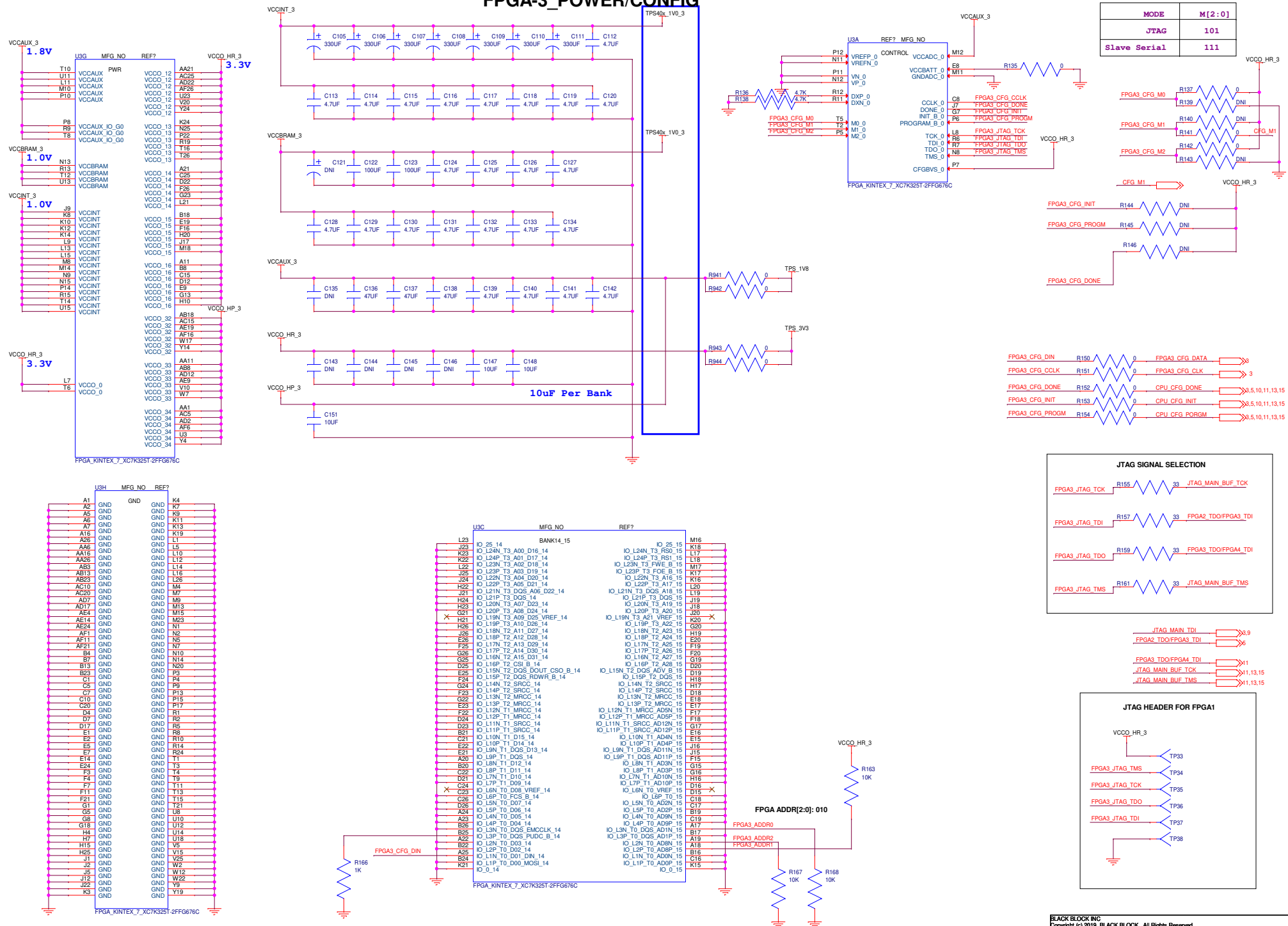
  

VCCQ_HR_2	TP27	TP28	TP29	TP30	TP31	TP32
FPGA2_JTAG_TMS	TP27	TP28	TP29	TP30	TP31	TP32
FPGA2_JTAG_TCK	TP27	TP28	TP29	TP30	TP31	TP32
FPGA2_JTAG_TDO	TP27	TP28	TP29	TP30	TP31	TP32
FPGA2_JTAG_TDI	TP27	TP28	TP29	TP30	TP31	TP32

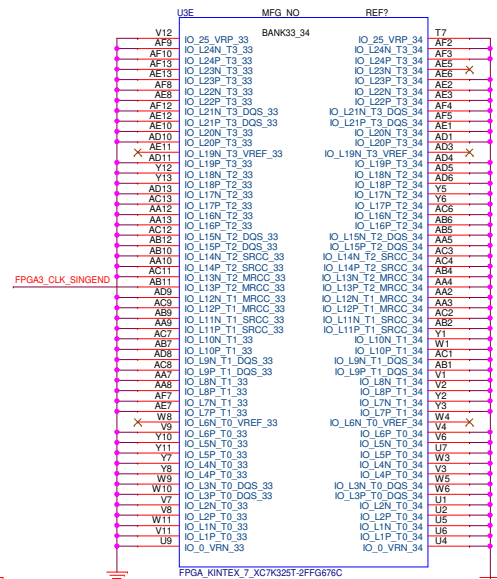
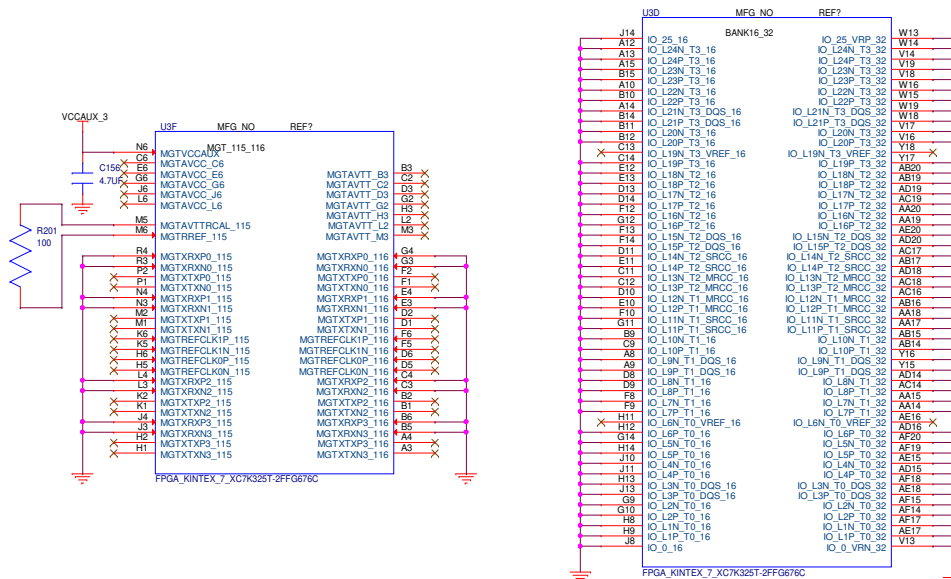
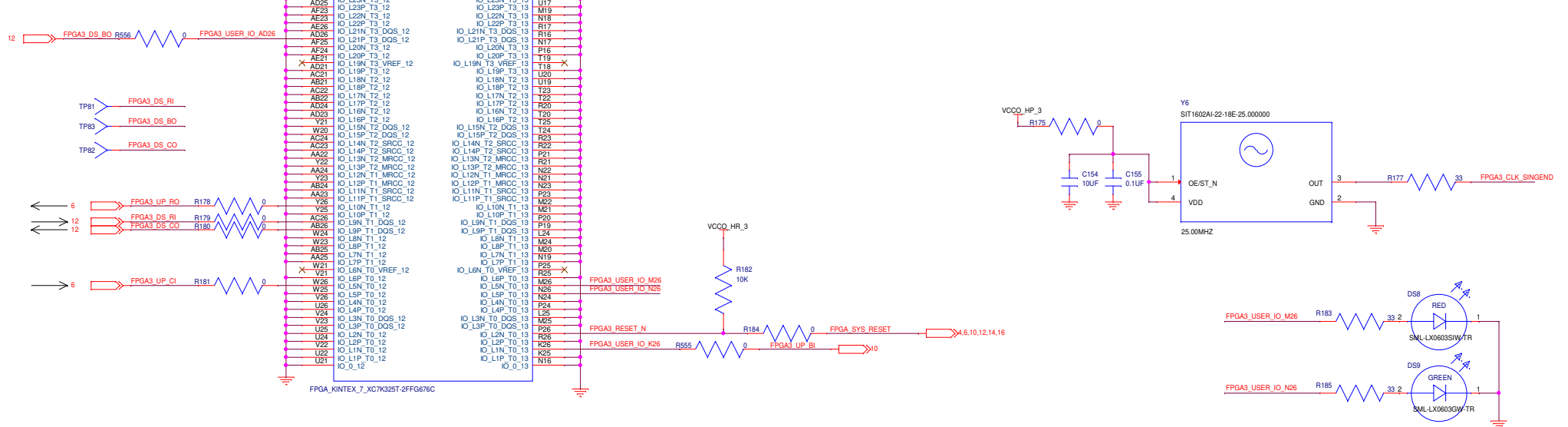
## FPGA-2 IO BANK



### FPGA-3 POWER/CONFIG

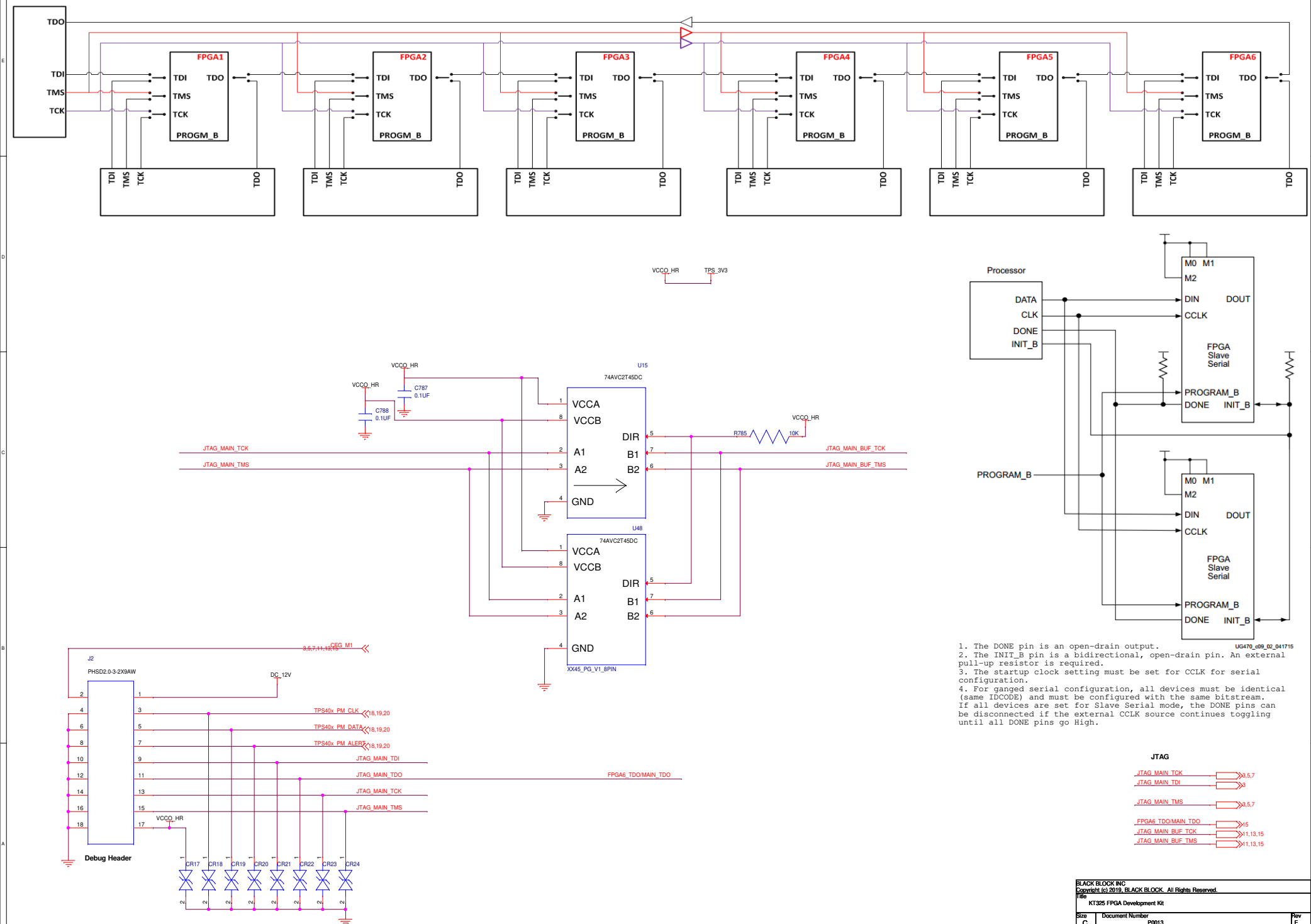


8	7	6	5	4	3	2	1
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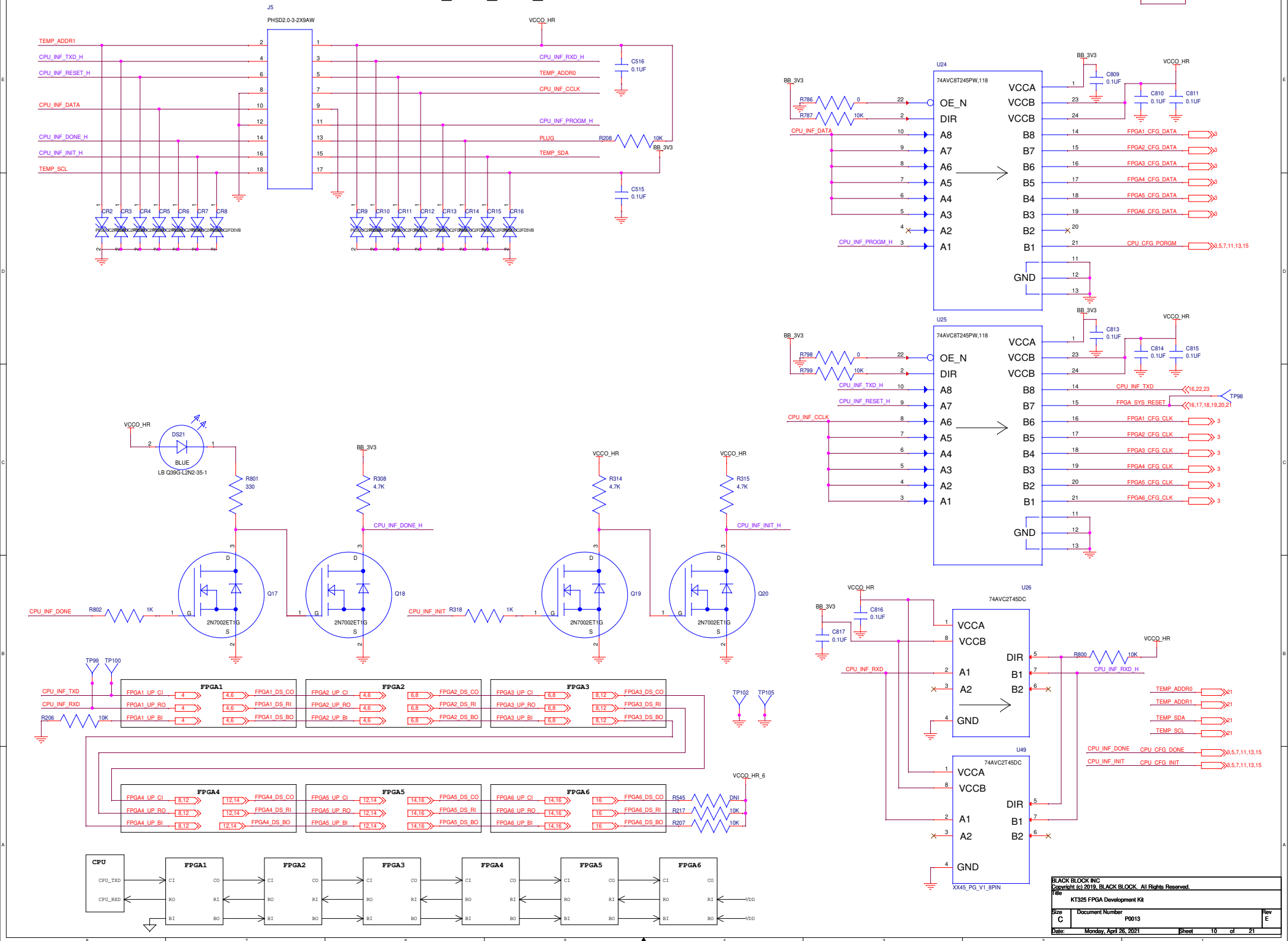
## FPGA\_CFG\_JTAG\_LINK



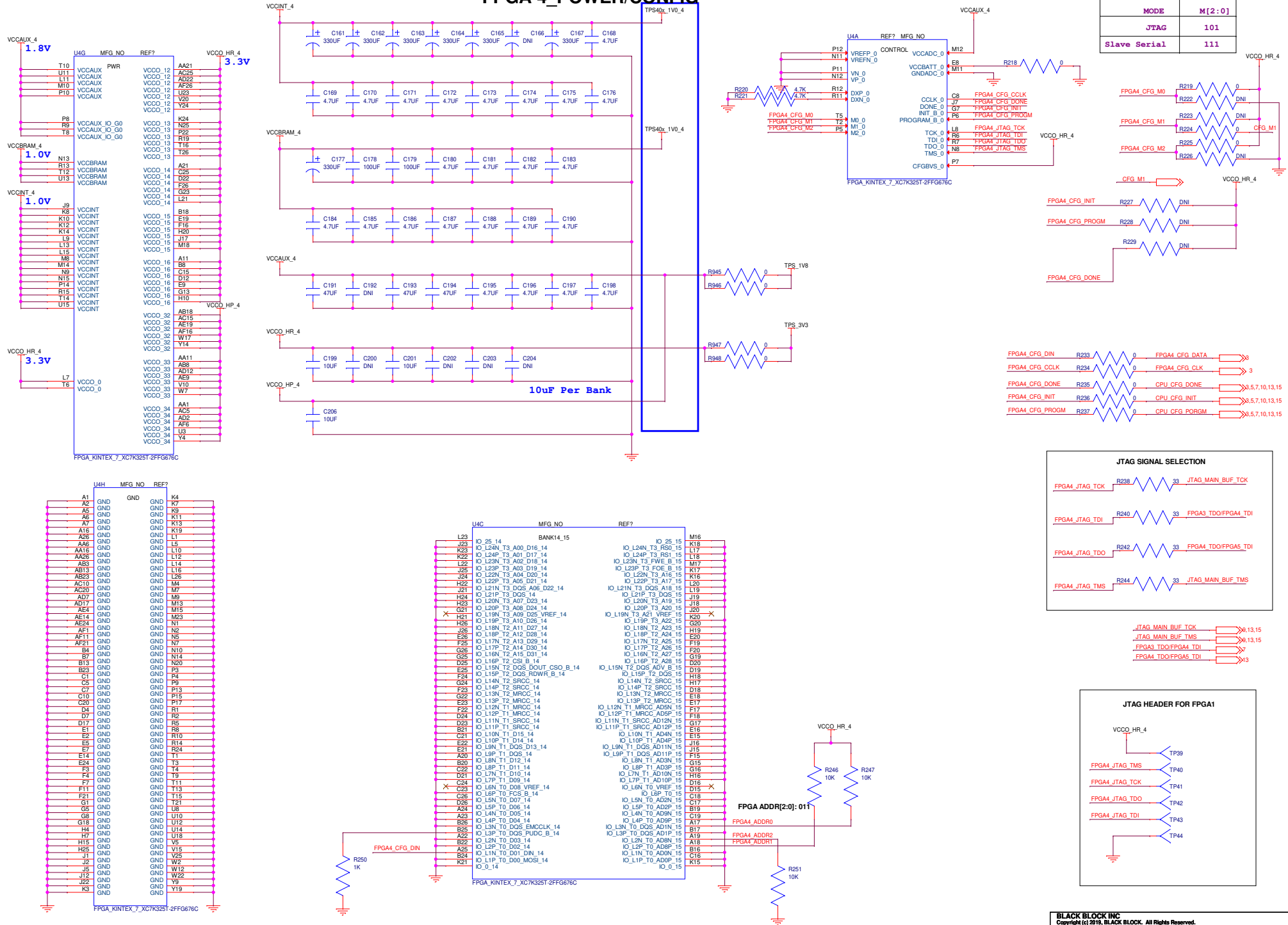
1. The DONE pins are open-drain output. UG470\_000\_041715
2. The INIT\_B pin is a bidirectional, open-drain pin. An external pull-up resistor is required.
3. The start-up clock setting must be set for CCLK for serial configuration.
4. For gated serial configuration, all devices must be identical (same ICDCODE) and must be configured with the same bitstream.
5. If all devices in Slave Serial mode, the DONE pins can be disconnected if the external CCLK source continues toggling until all DONE pins go High.

JTAG

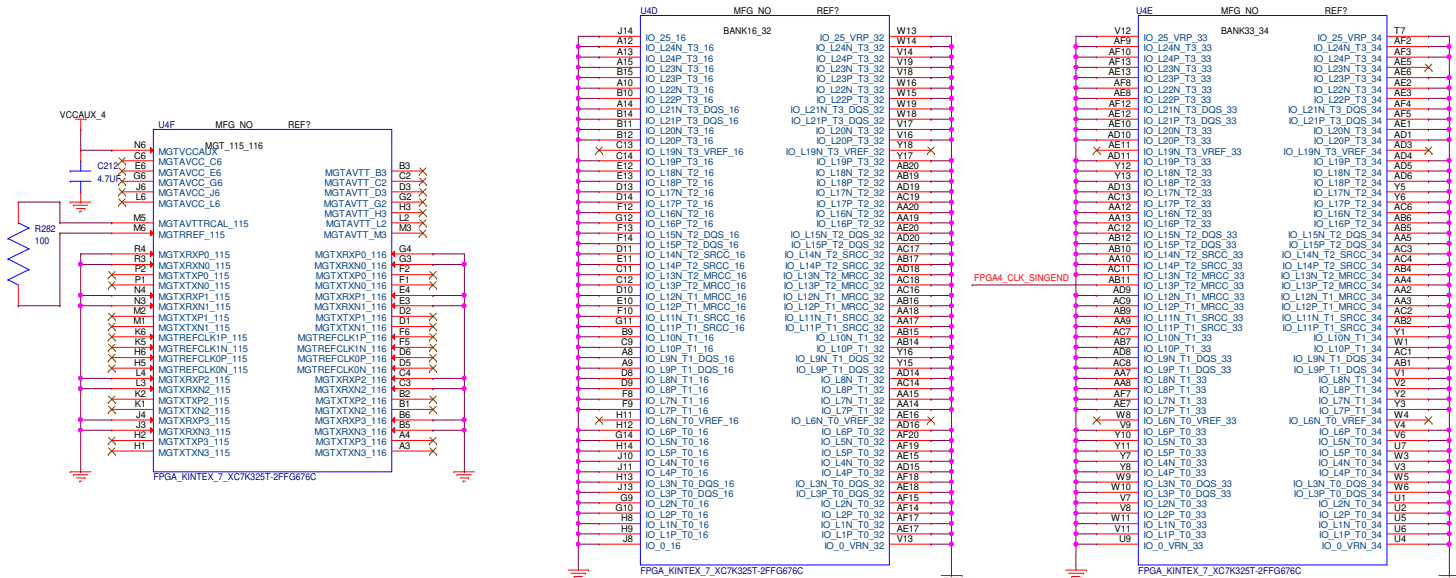
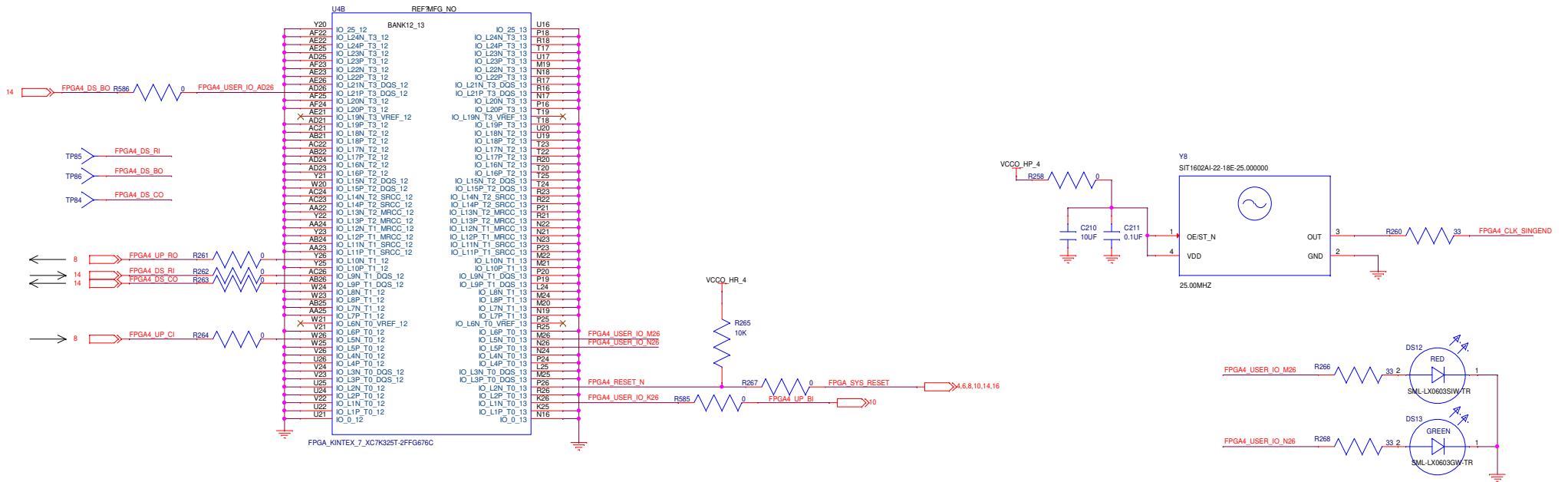
## FPGA\_CFG\_CPU\_LIMK



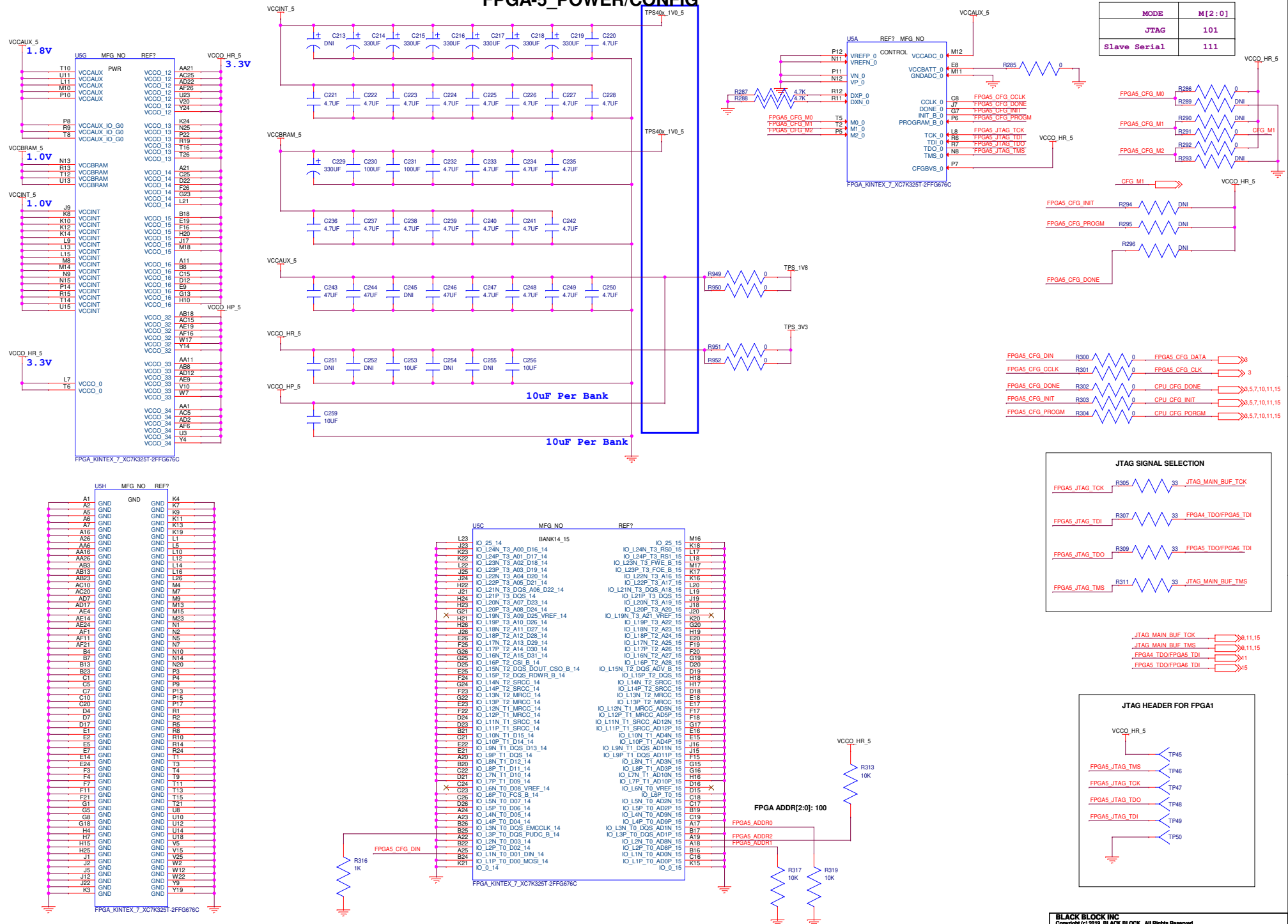
# FPGA-4\_POWER/CONEIG



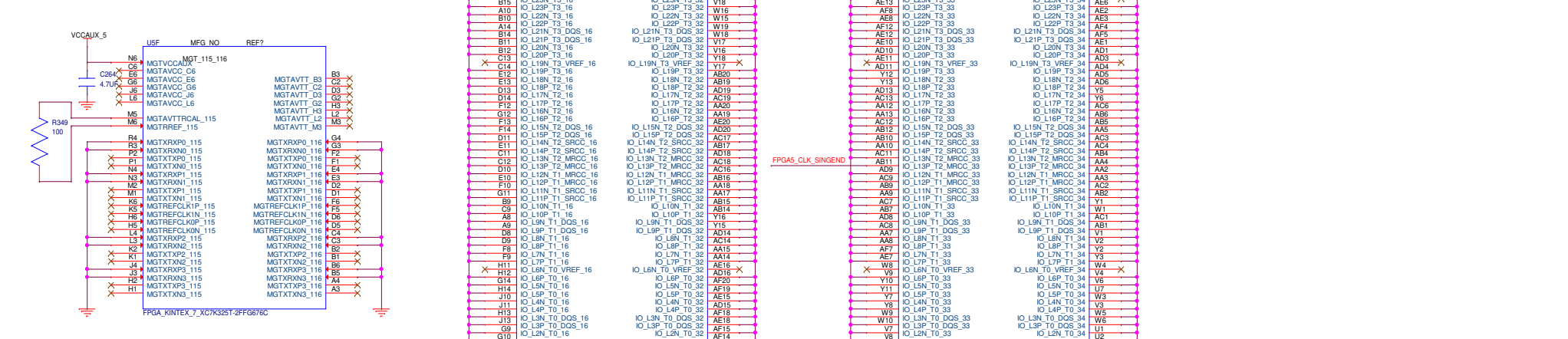
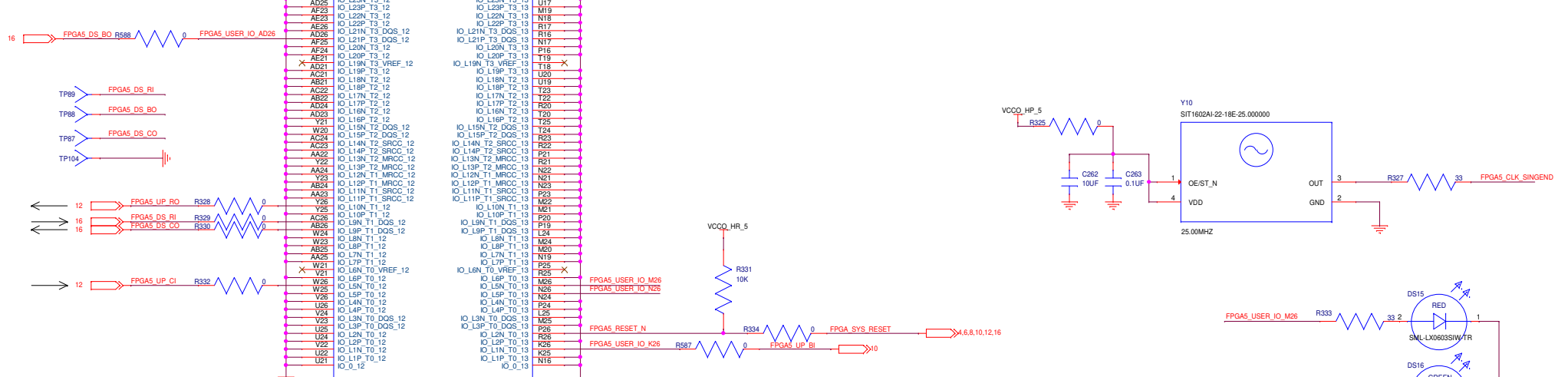
## FPGA-4\_IO\_BANK



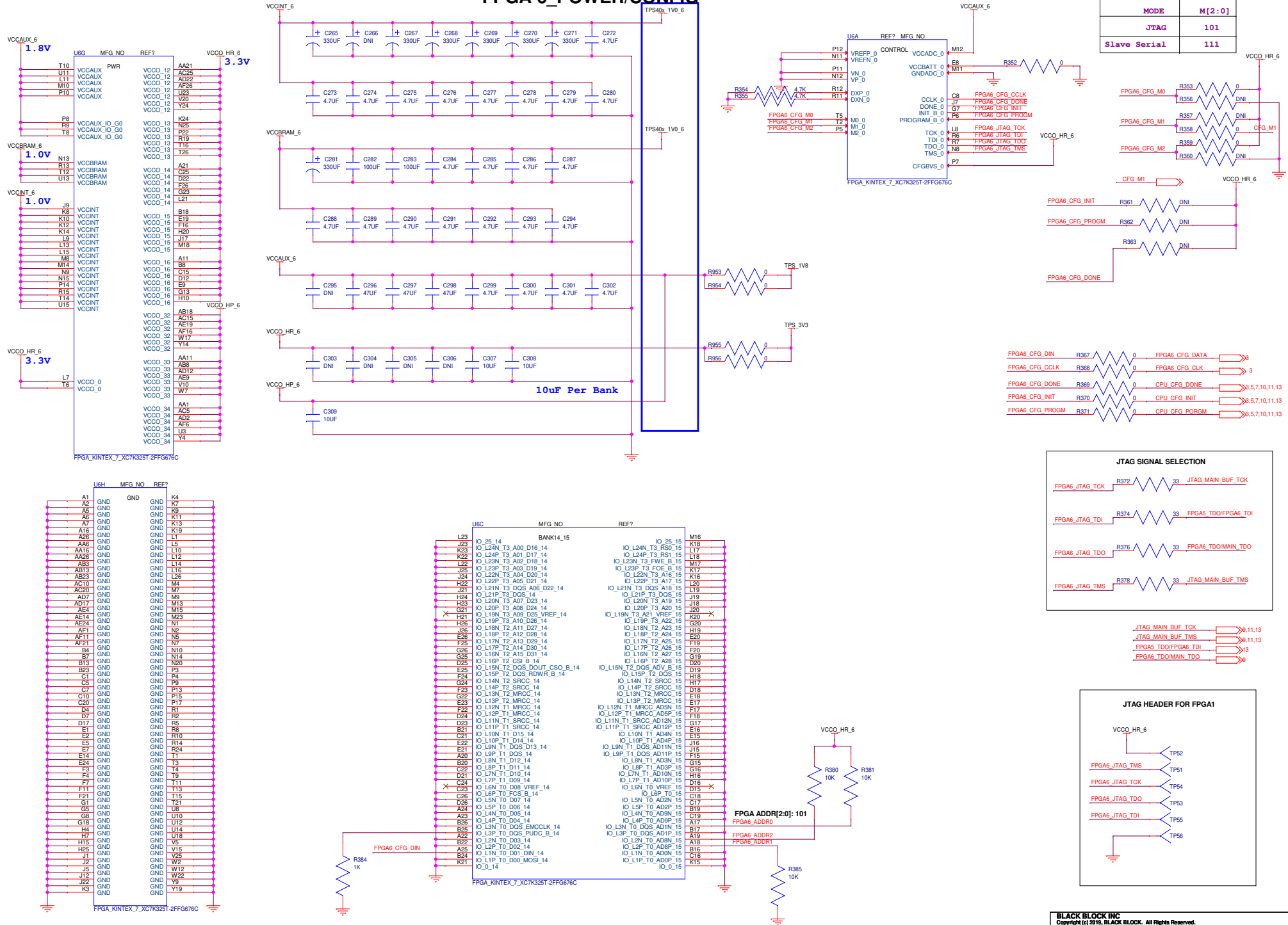
## FPGA-5 POWER/CONFIG



A horizontal timeline diagram consisting of a long rectangle divided into 8 equal segments, numbered 8 to 1 from left to right. Segment 6 is highlighted with a dashed line. An arrow points from the right edge of segment 5 towards segment 6.



# FPGA-6\_POWER/CONEIG

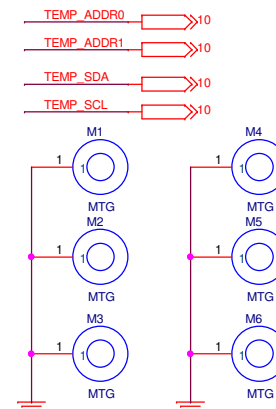
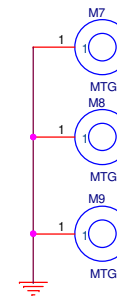
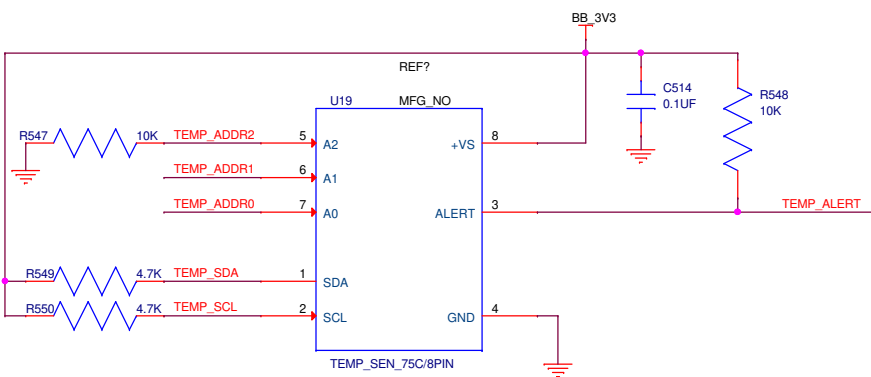
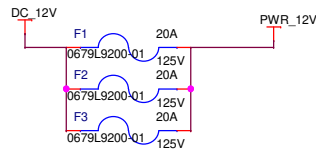
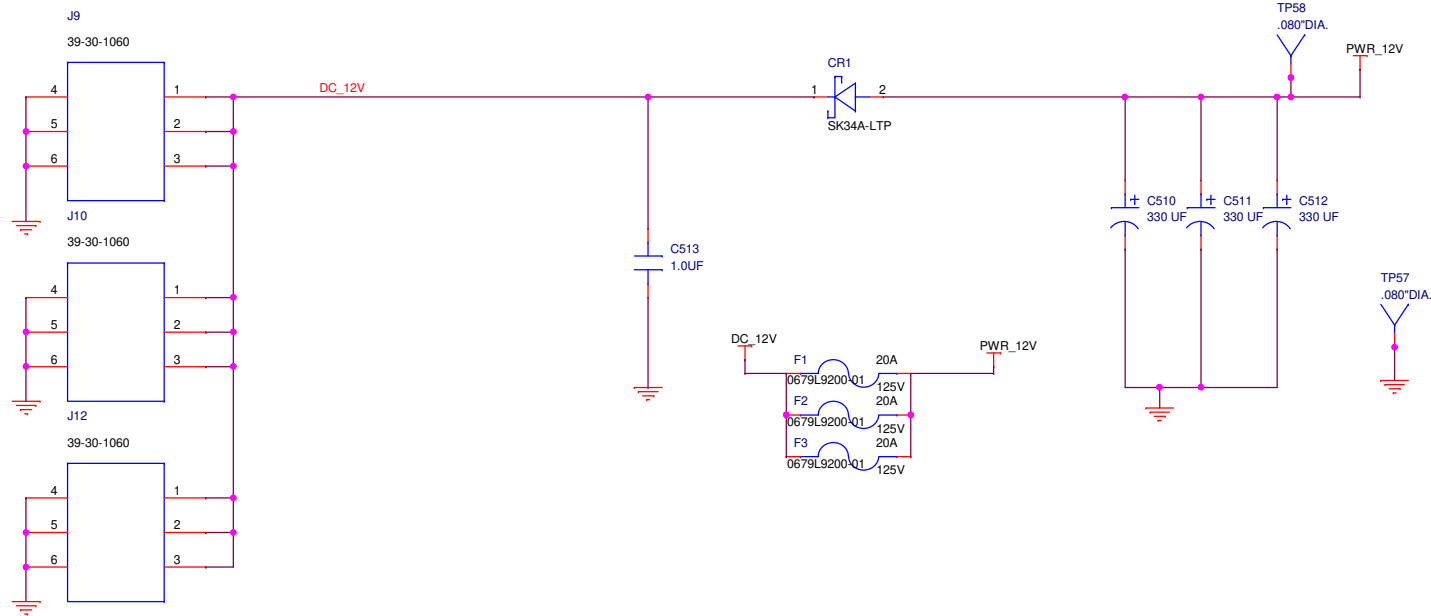








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Size	Document Number		Rev
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Date:	Monday, April 26, 2021	Sheet	21 of 21