NOTES:

REV	DATE	PAGES	DESCRIPTION
A	2020JUNE		Initial
B	2020JUNE		1. CFGBVS Connect to GND to compatible 1.8V IO 2. FPGA CLK input chang to AL29 3. R342 chang to 13.7K 4. TPS_3V3 chang to NET TPS_1V8_IO 5. Change VCCO_HR to VCCO_HP and connect to TPS_1V8_IO 6. chang net name VCCO_HR_X to VCCO_HP_X, and connect to TPS_1V8_IO 7. R93, DS7, R97,R345 Pull UP change to BB_3V3 8. FOR LED STATUS INDICATOR: CHANG TO 330 ohm:R29,R30,R59,R60,R89,R90,R138,R139,R168,R169,R198,R199 ADD 1k RES: R610,R611,R612,R613,R614,R615,R616,R617,R618,R619,R620,R621 ADD Trans: Q21,Q22,Q23,Q24,Q25,Q26,Q27,Q28,Q29,Q30,Q31,Q32 9. PMBUS ADDR Change: R440 ---> 36K R438 ---> 10K R467 ---> 10K R492 ---> 15K R519 ---> 15K R548 ---> 15K R546 ---> 36K 10. J3 Pin1 connect to BB_3V3

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Clock Diagram

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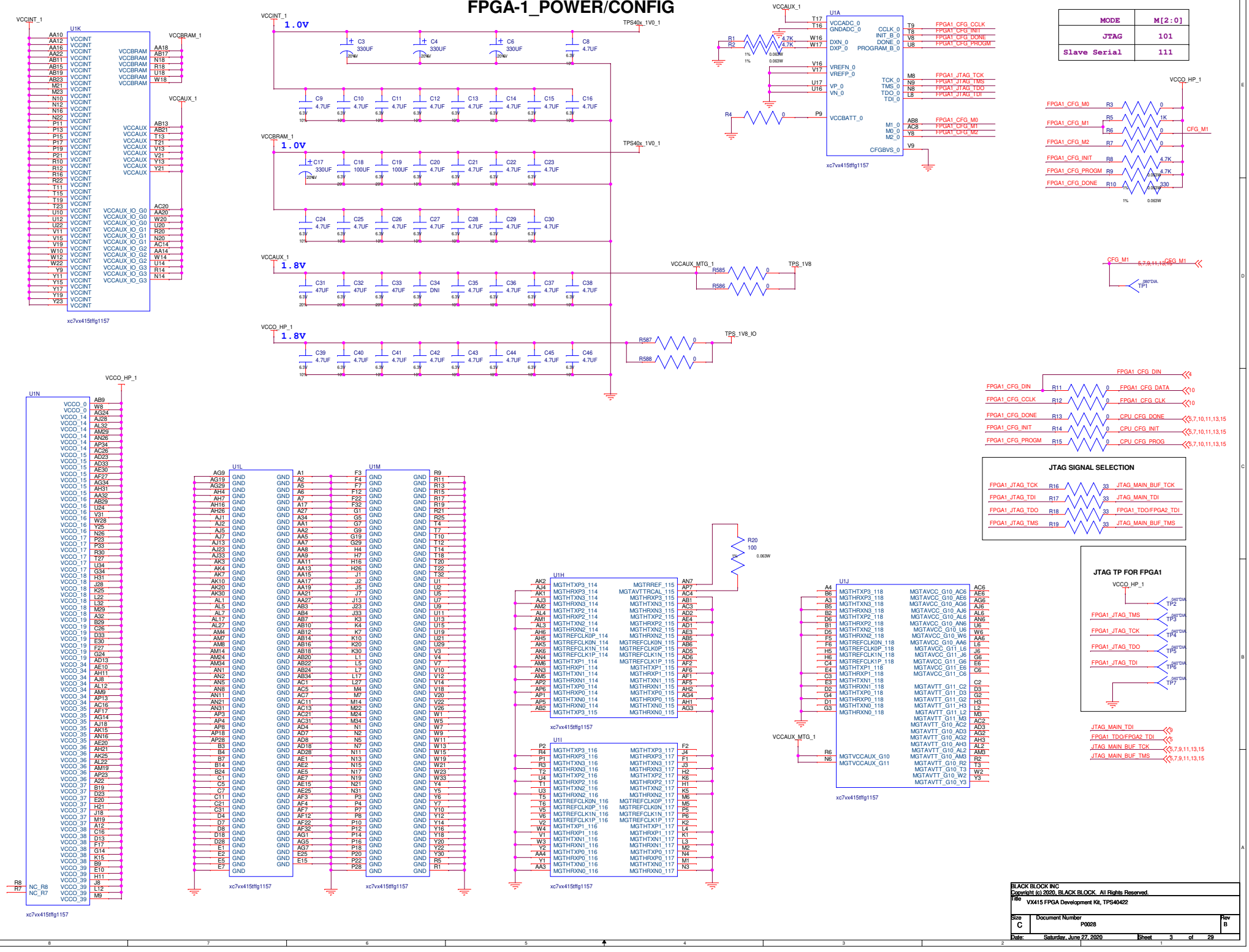
FPGA-1_POWER/CONFIG



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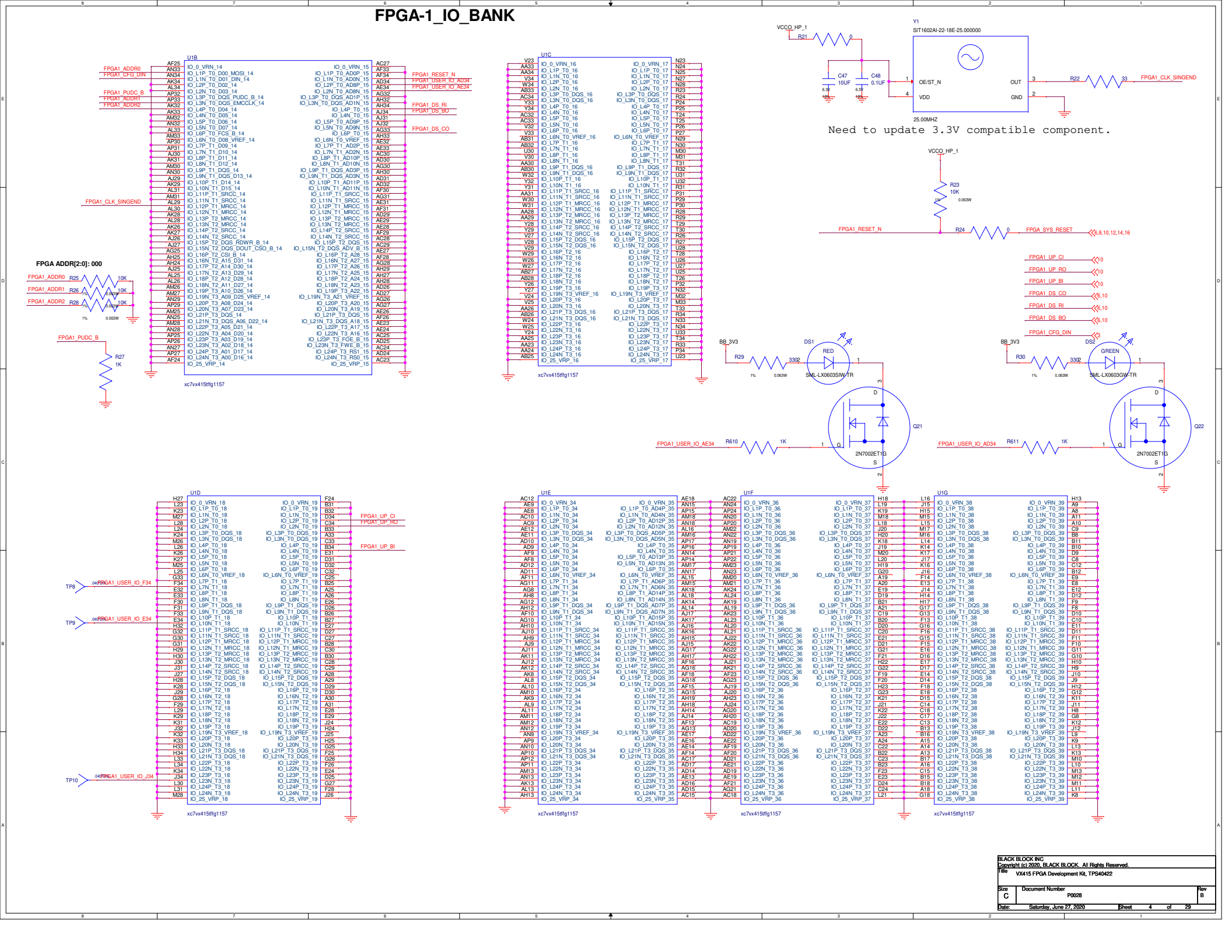
FPGA-1_IO_BANK



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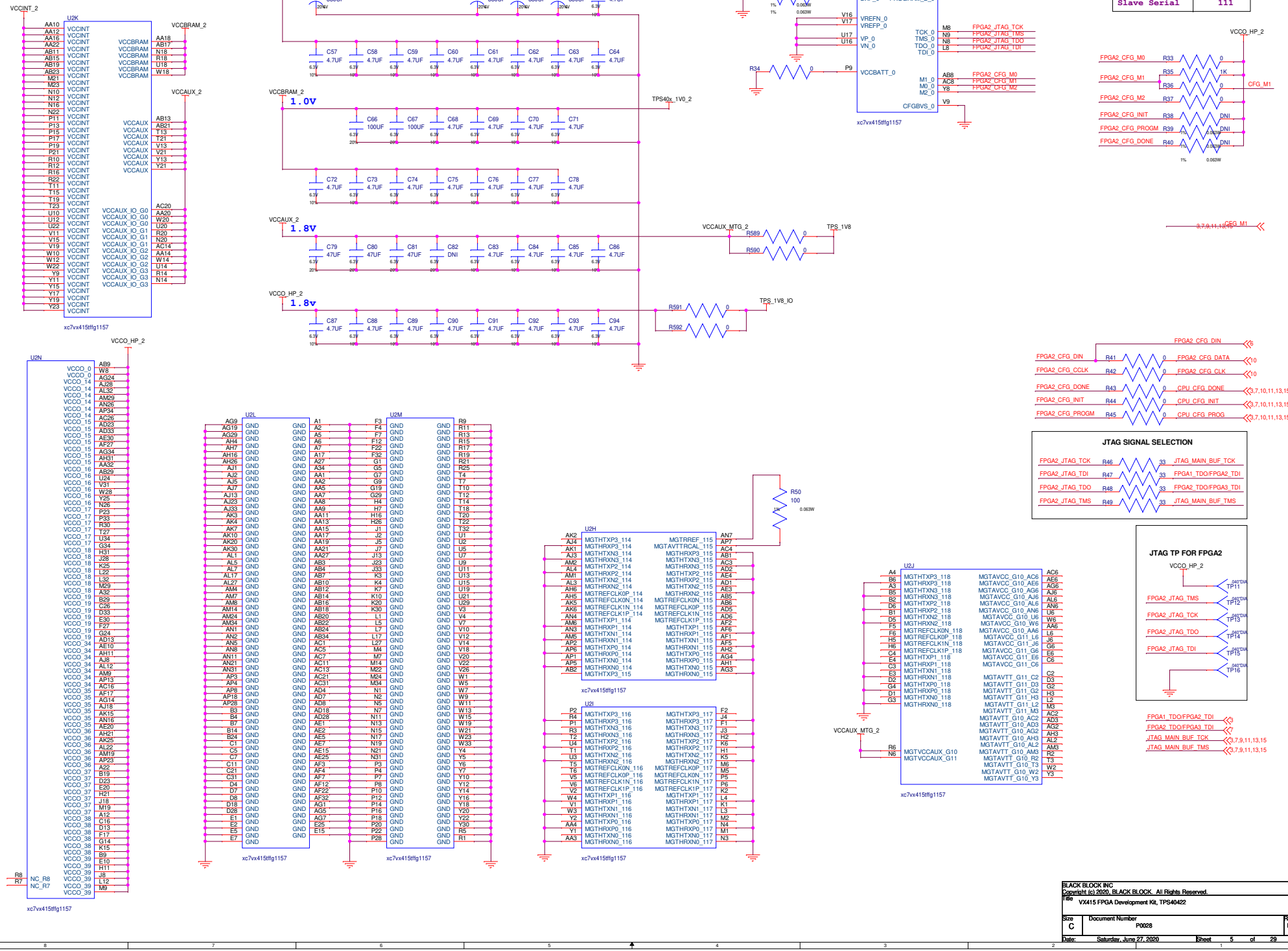
FPGA-2_POWER/CONFIG

MODE	M[2:0]
JTAG	101
Slave Serial	111



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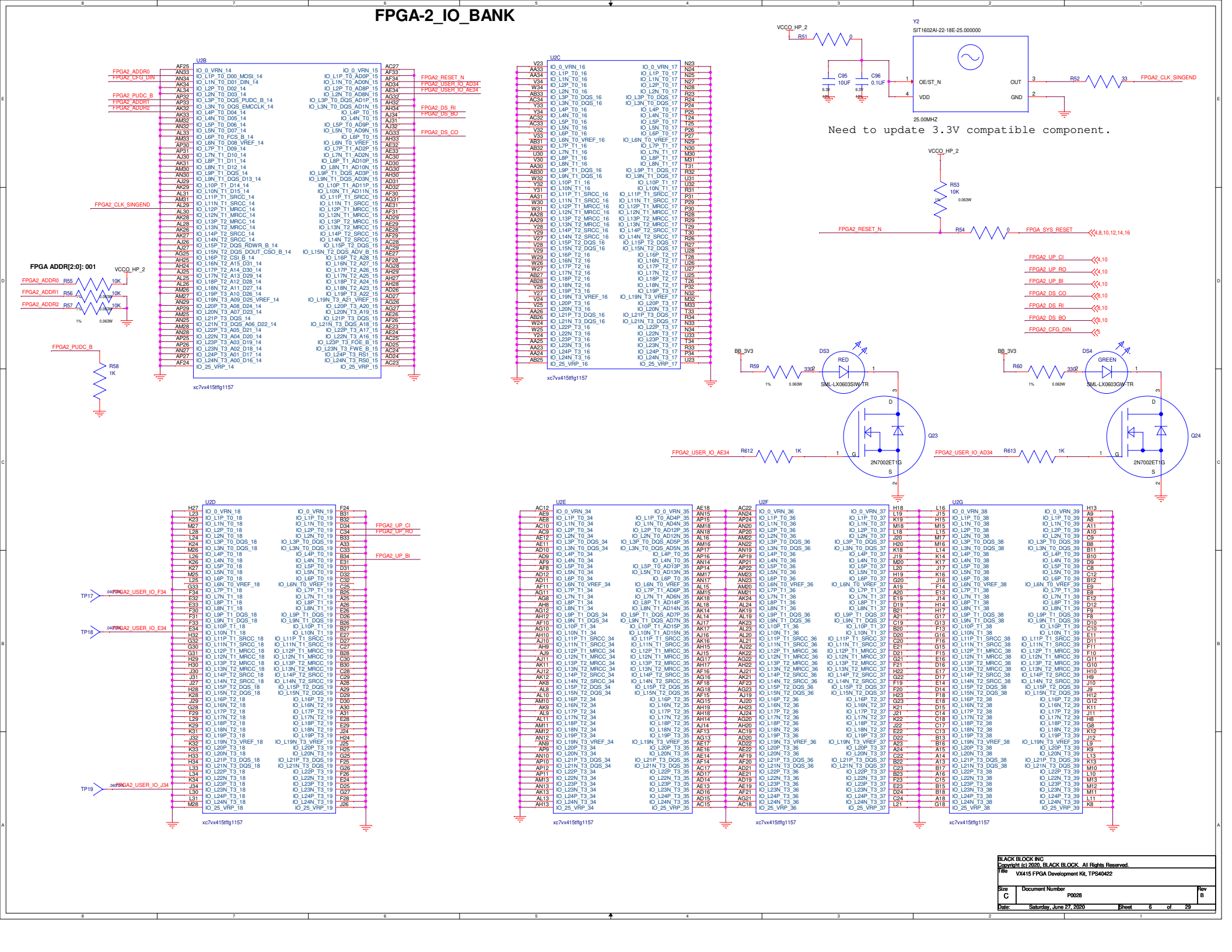
FPGA-2_IO_BANK



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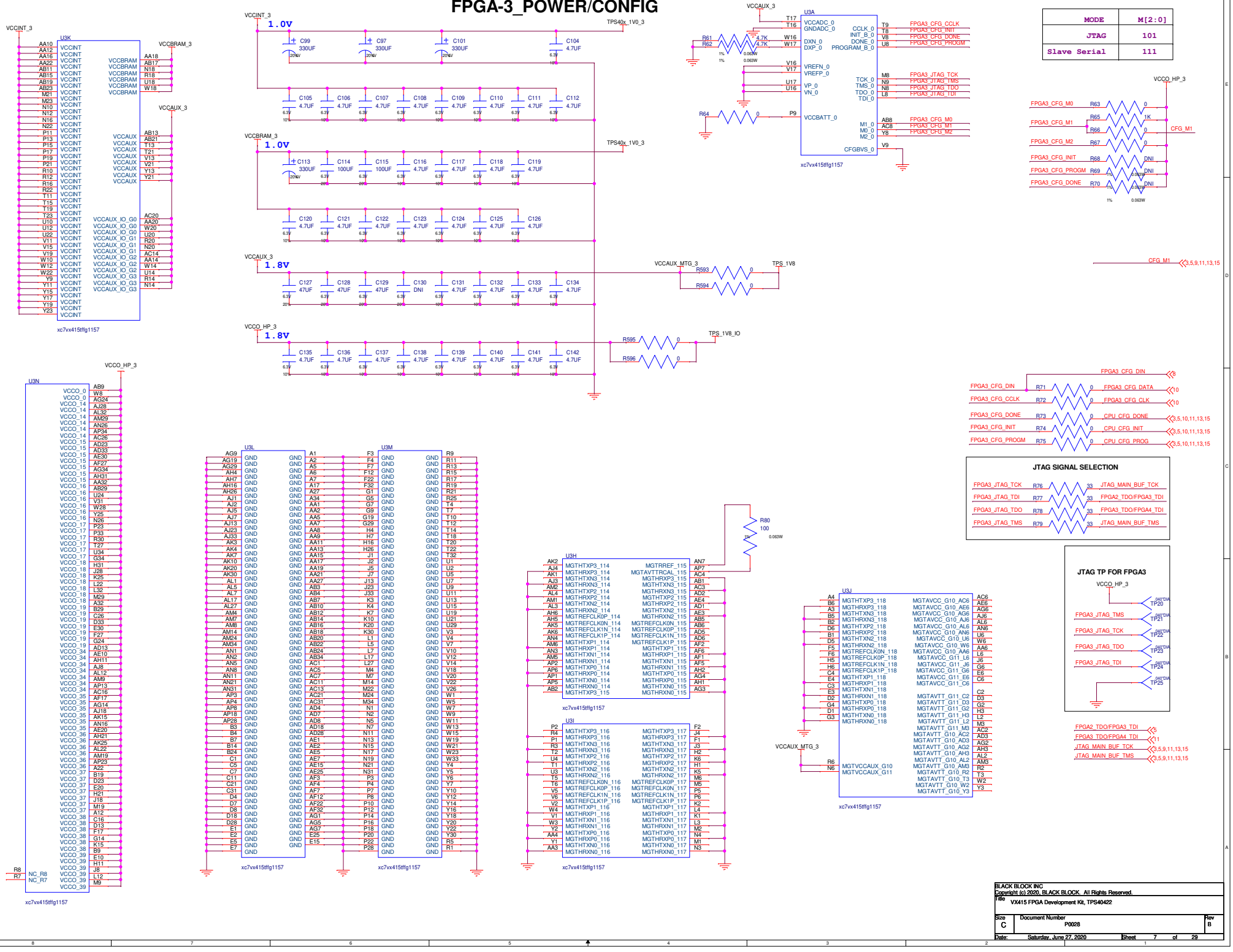
FPGA-3_POWER/CONFIG



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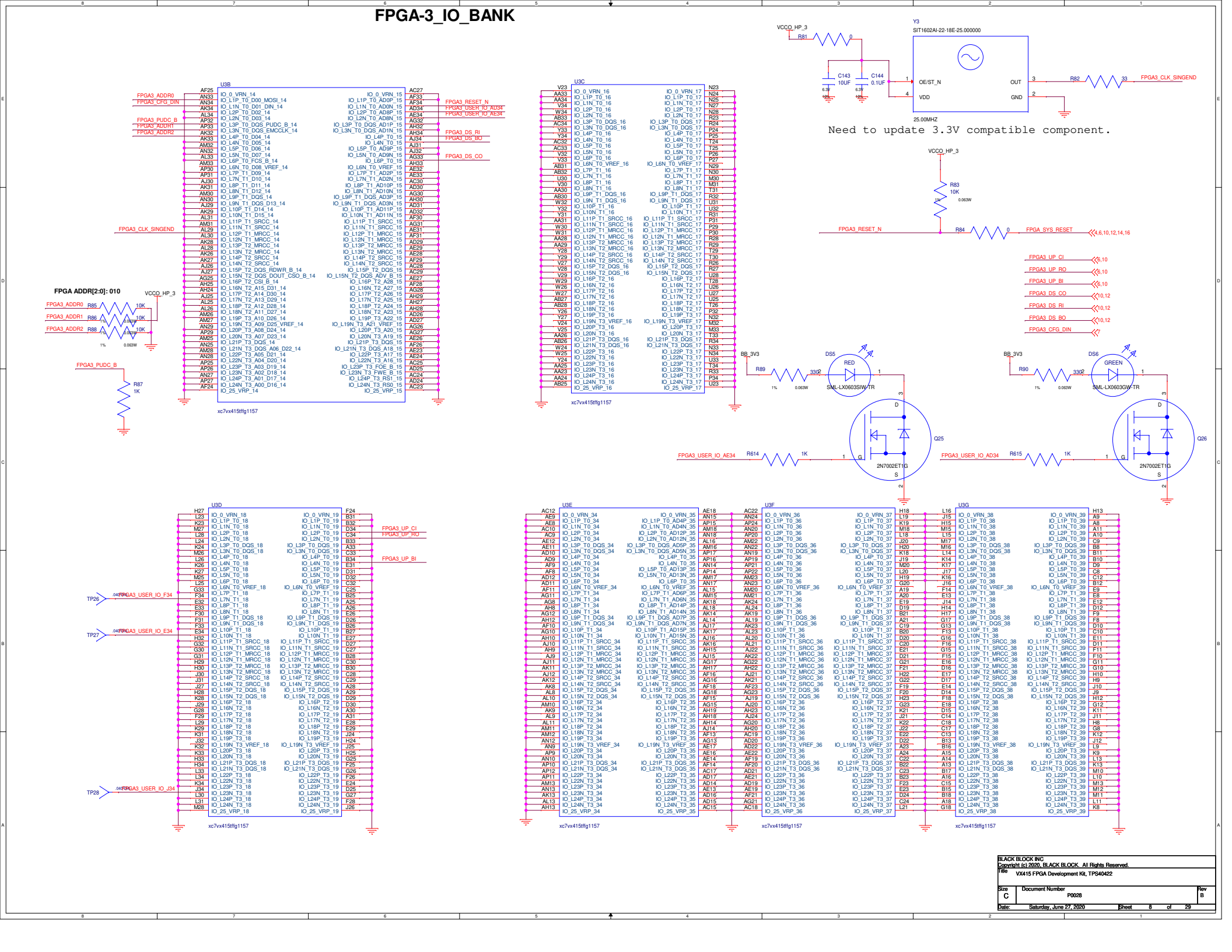
FPGA-3_IO_BANK



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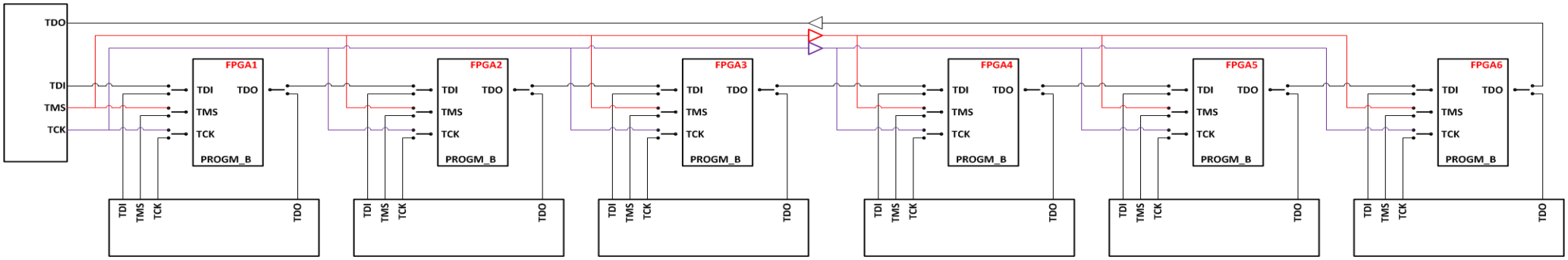
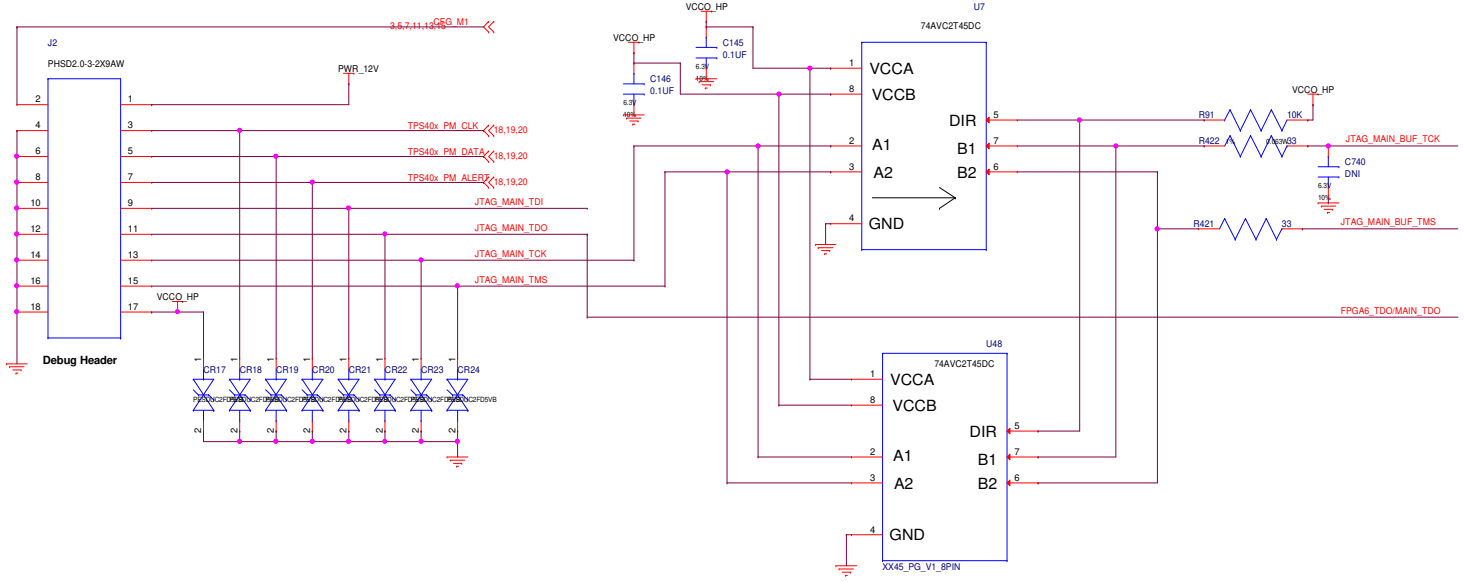
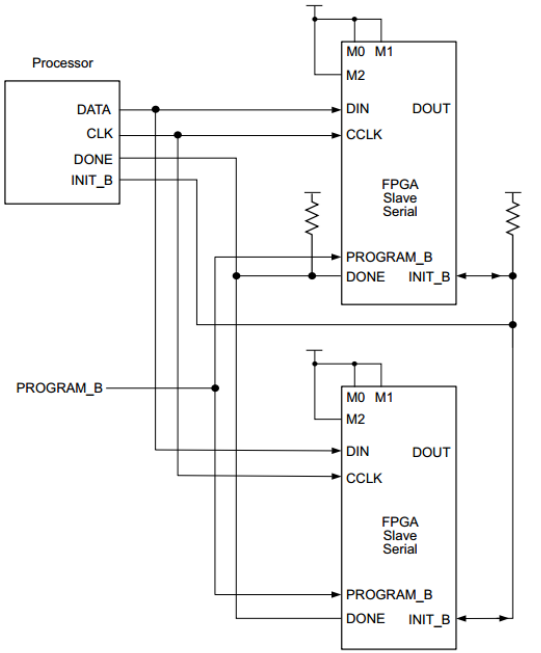
FPGA_CFG_JTAG_LINK







1. The DONE pin is an open-drain output.
2. The INIT_B pin is a bidirectional, open-drain pin. An external pull-up resistor is required.
3. The startup clock setting must be set for CCLK for serial configuration.
4. For ganged serial configuration, all devices must be identical (same IDCODE) and must be configured with the same bitstream. If all devices are set for Slave Serial mode, the DONE pins can be disconnected if the external CCLK source continues toggling until all DONE pins go High.

UG470_c09_02_041715

JTAG

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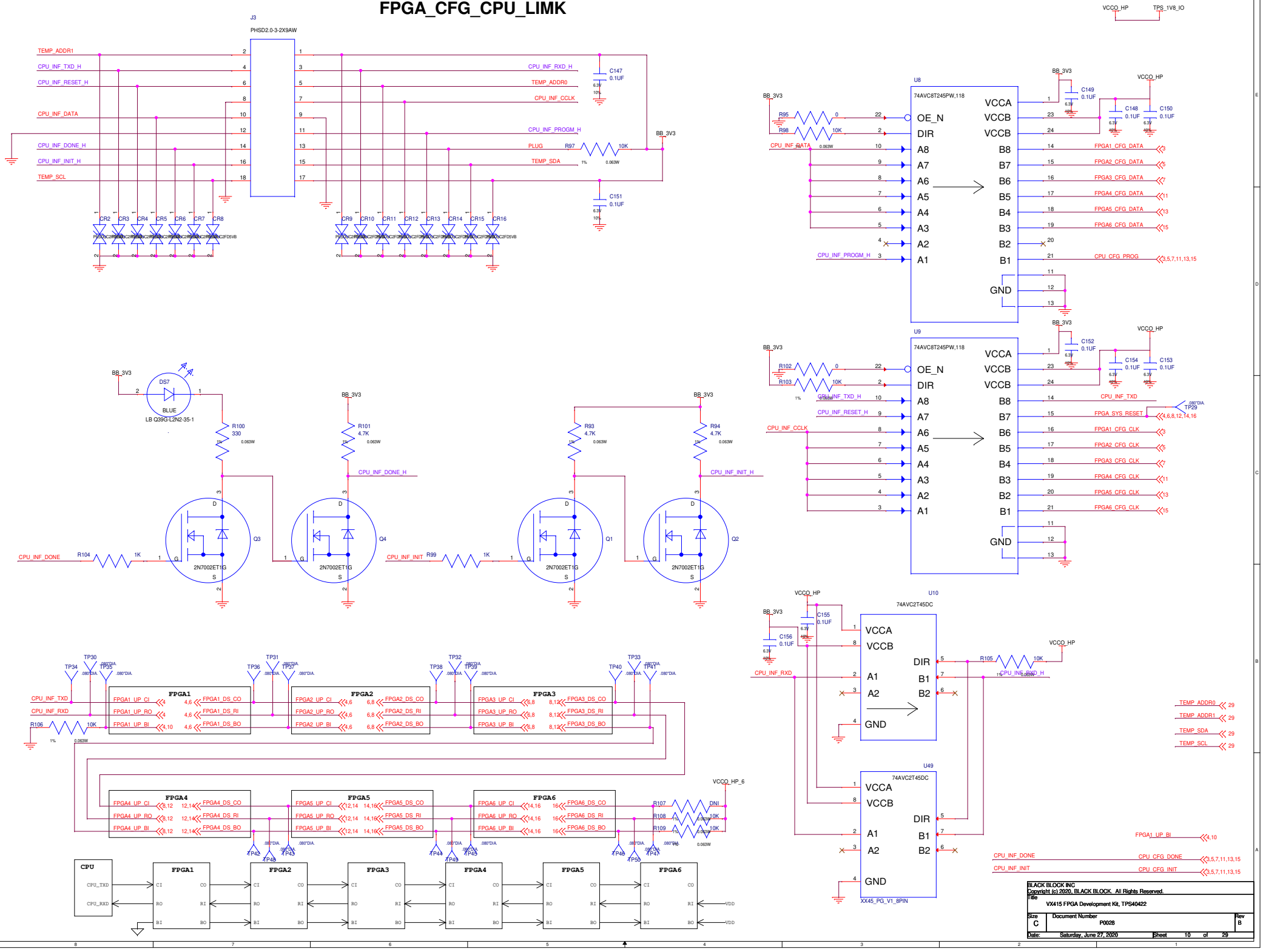
FPGA_CFG_CPU_LIMK



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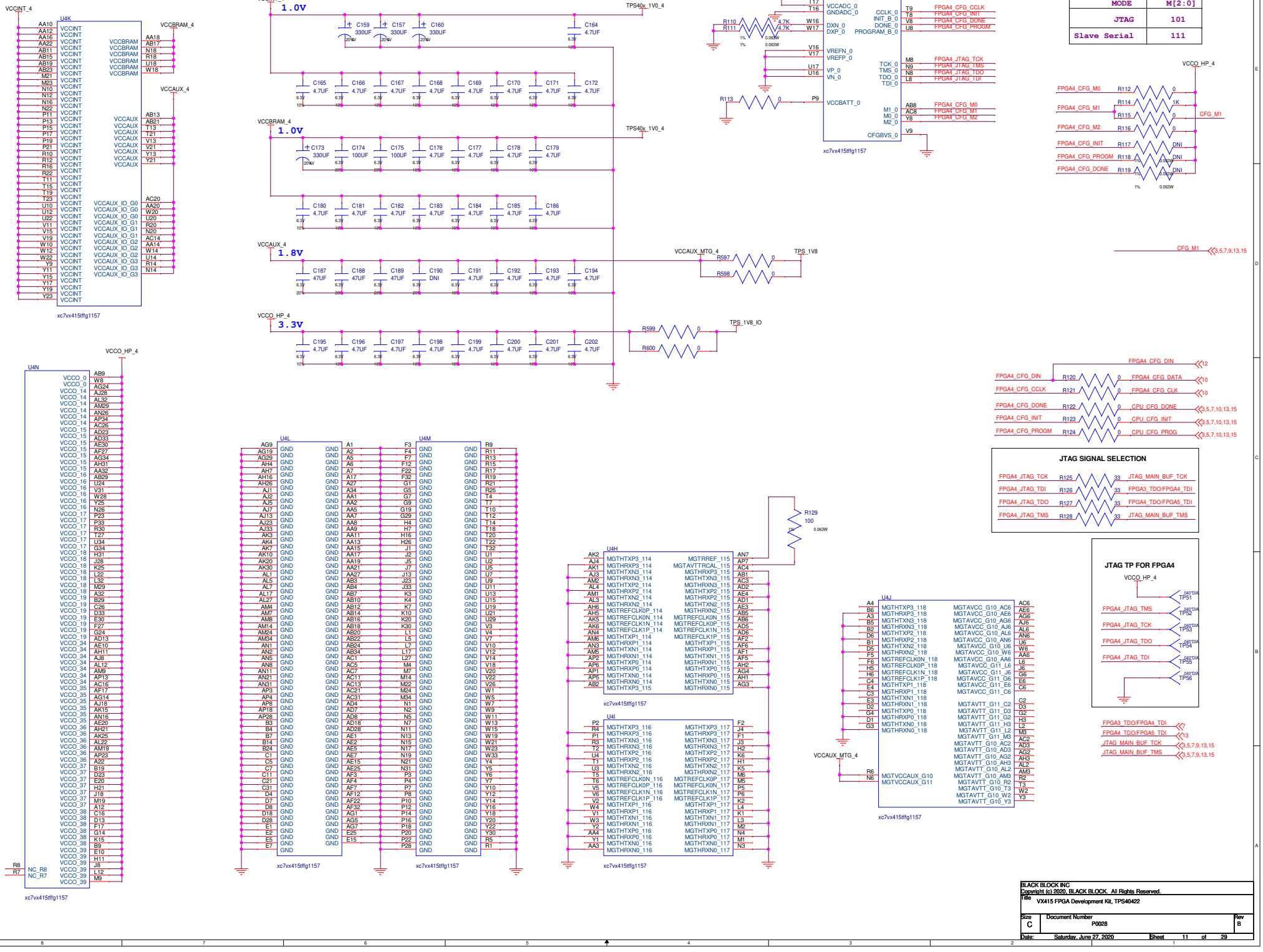
FPGA-4_POWER/CONFIG



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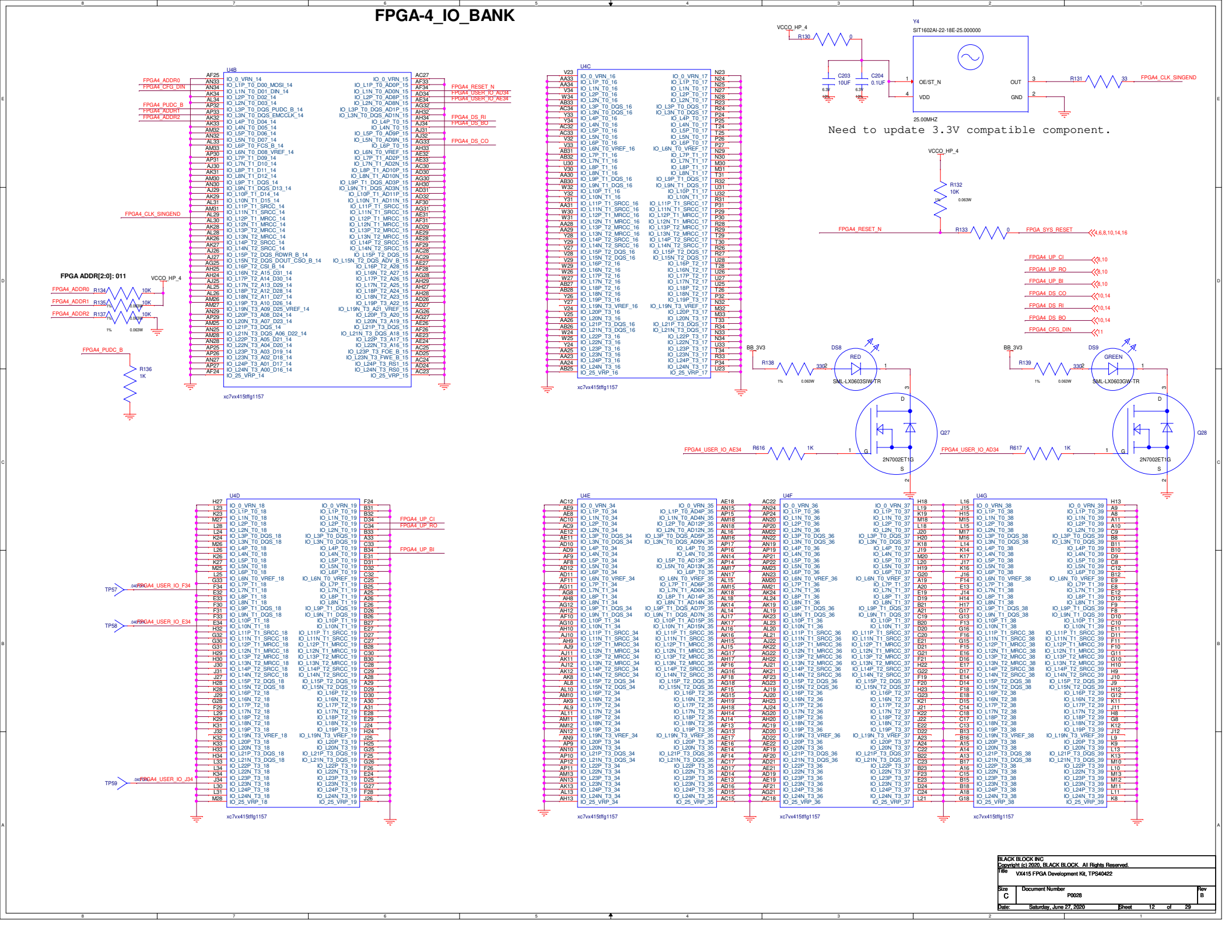
FPGA-4_IO_BANK



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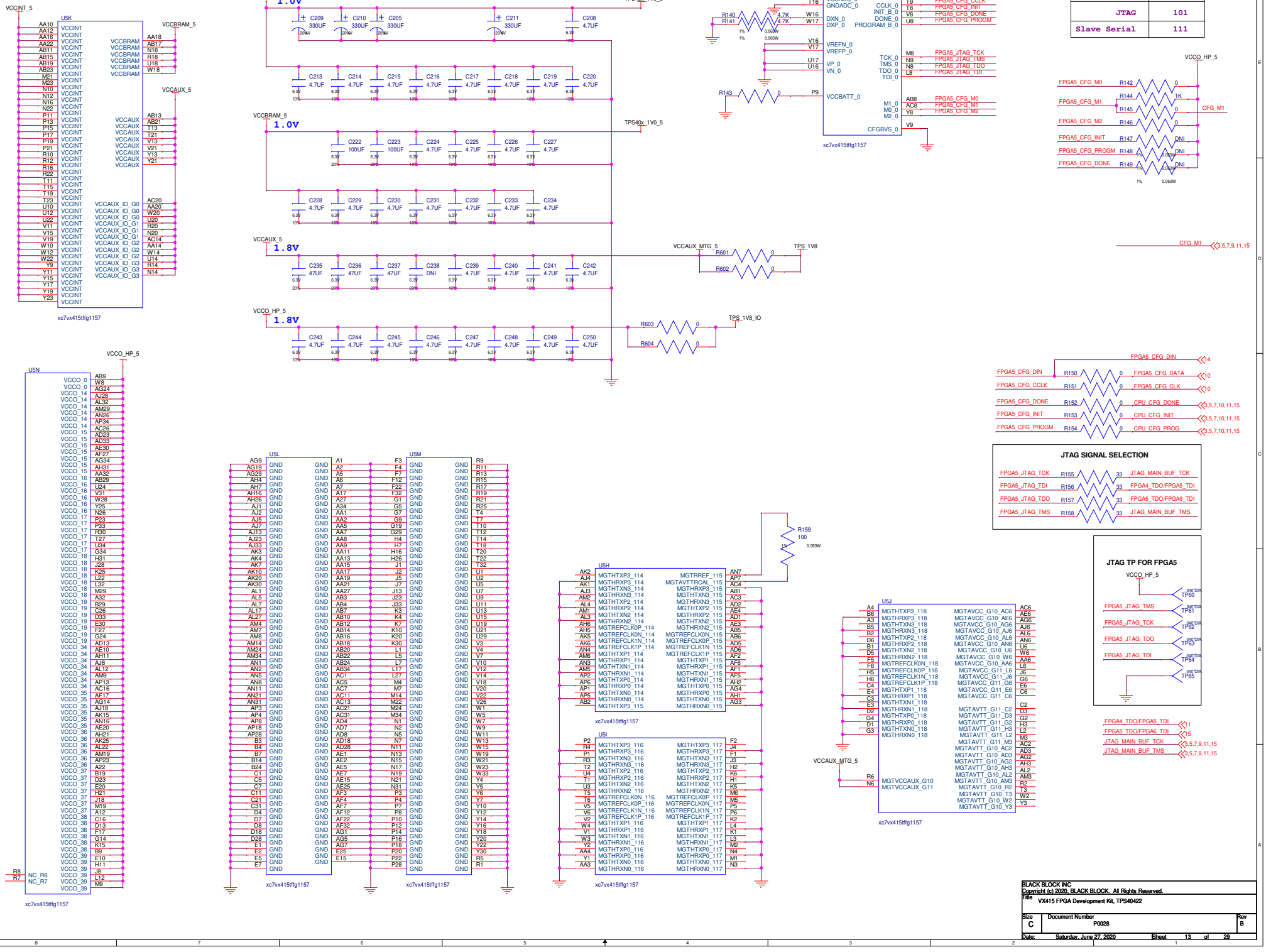
FPGA-5_POWER/CONFIG



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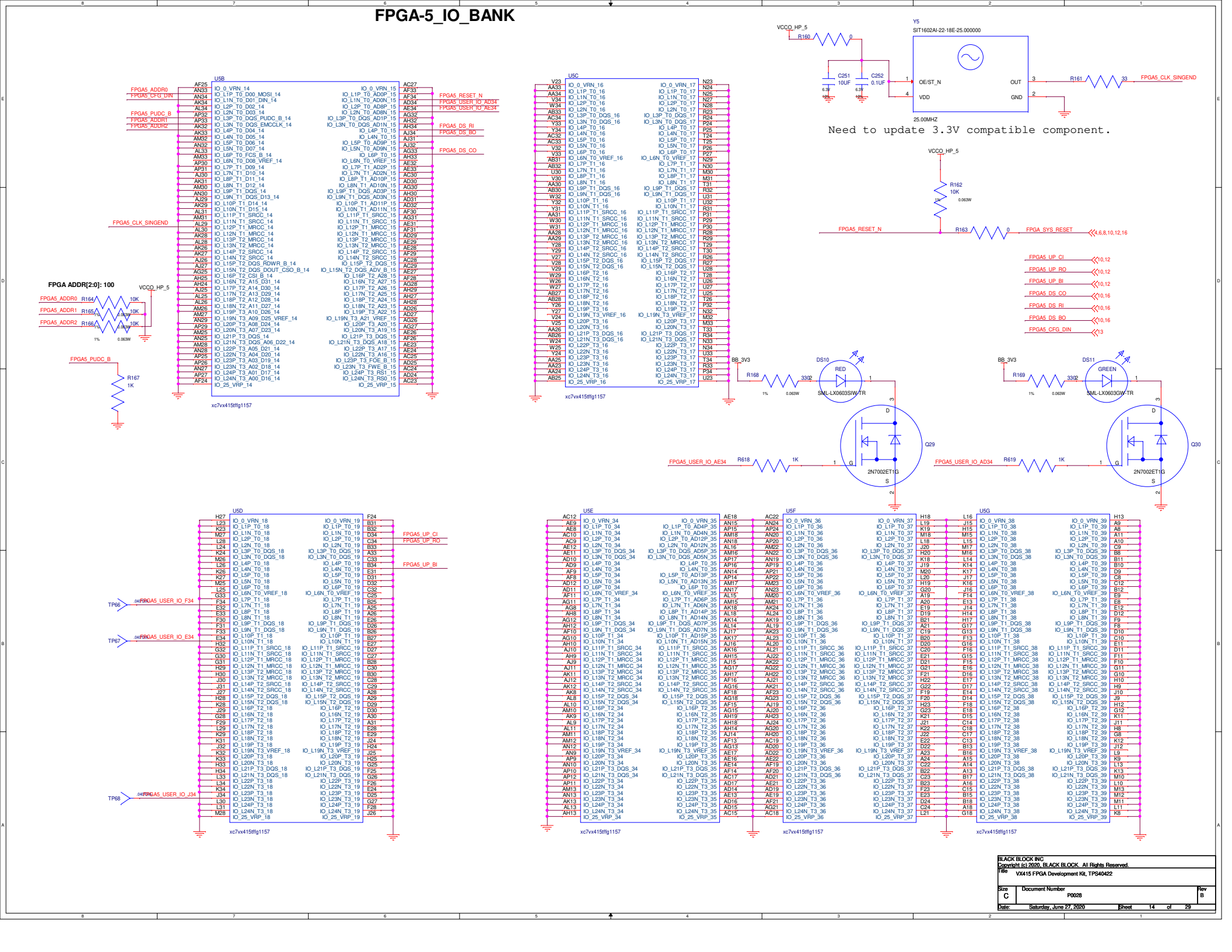
FPGA-5_IO_BANK



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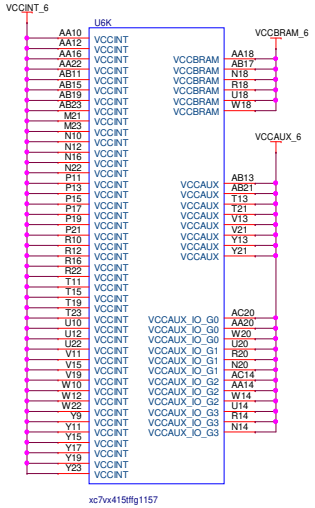
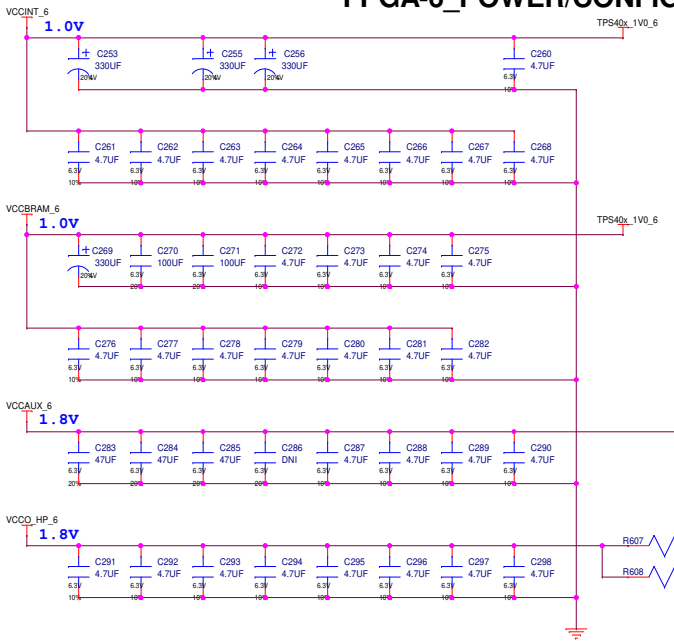
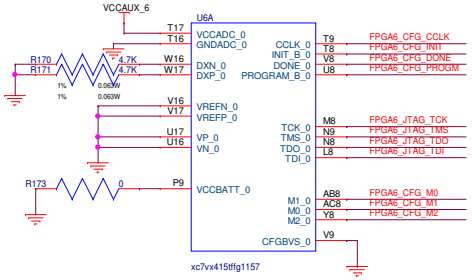
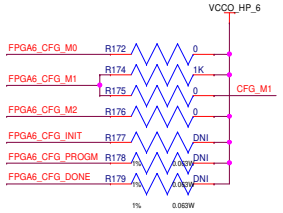
FPGA-6_POWER/CONFIG

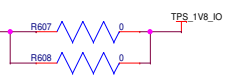


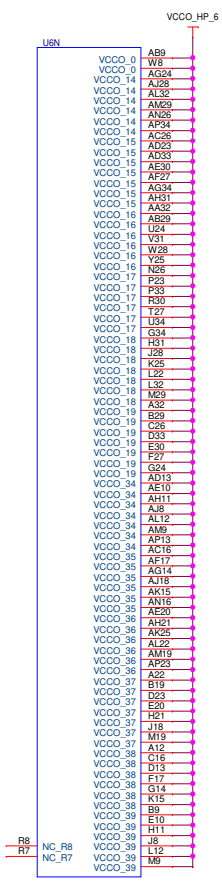


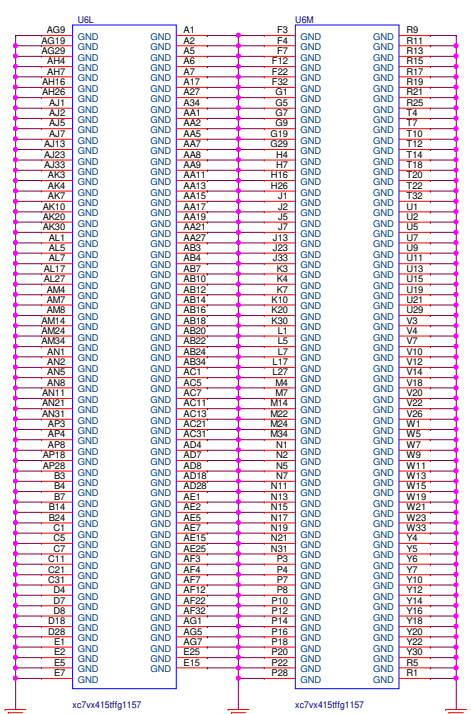


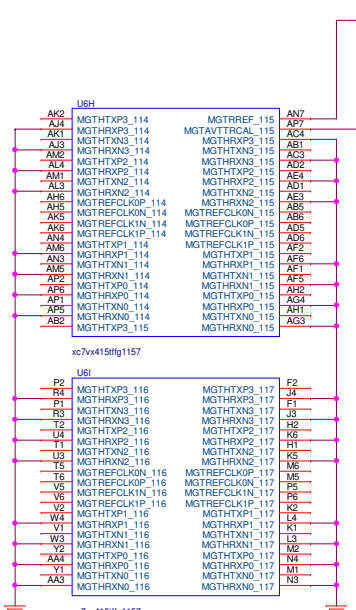
MODE	M[2:0]
JTAG	101
Slave Serial	111

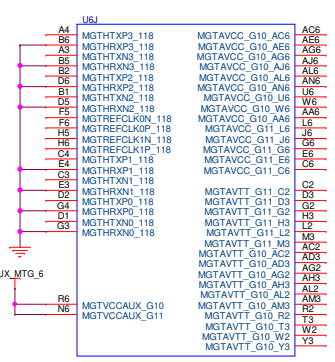


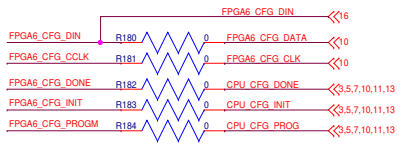


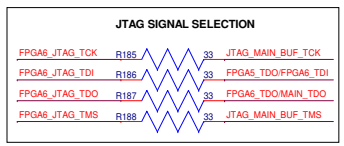


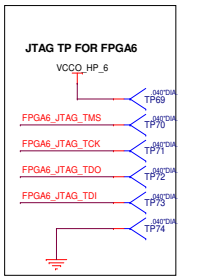












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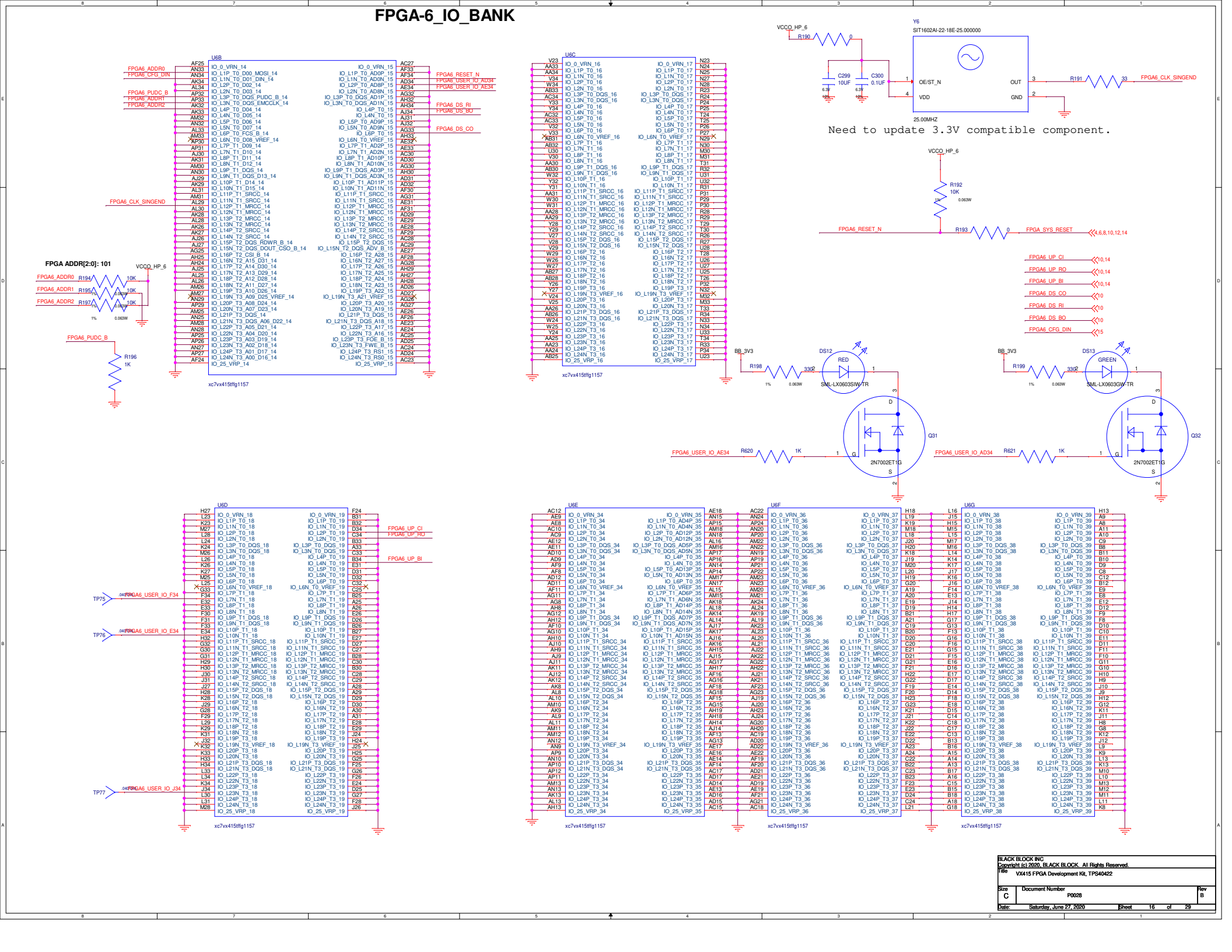
FPGA-6_IO_BANK



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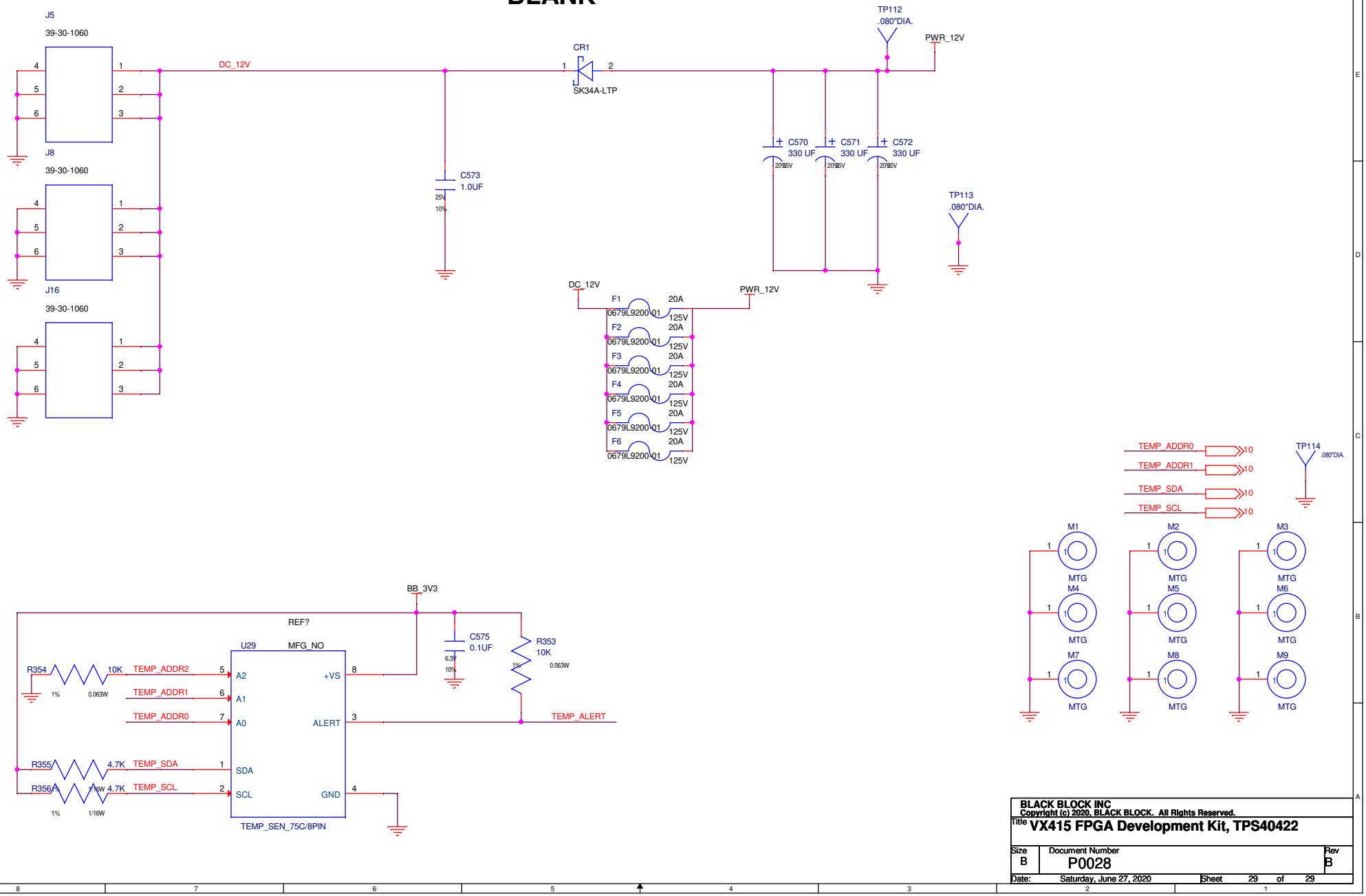

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