

SH7000 Series

Affine Transform

Label: AFIN

Functions Used: MAC.W Instruction
 Post-Increment Register Indirect Addressing

Contents

1. Function	2
2. Arguments.....	2
3. Internal Register Changes and Flag Changes.....	3
4. Programming Specifications	4
5. Description	5
6. Flowchart.....	8
7. Program Listing	9

1. Function

Performs matrix operations of the affine transform. A the data table of the sort shown below must be prepared beforehand.

Affine transform matrix

$$\begin{bmatrix} A & B & t_x \\ C & D & t_y \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} X \\ Y \\ 1 \end{bmatrix} = \begin{bmatrix} X' \\ Y' \\ 1 \end{bmatrix}$$

(X, Y) : Coordinate values before affine transform
(X', Y') : Coordinate values after affine transform
A, B, C, D : Affine transform parameters
t_x, t_y : Amount of X/Y coordinate shift during affine transform

Affine transform parameter table

7	⋮	0
t _x		
A		
B		
t _y		
C		
D		
⋮		

Coordinates before affine transform

7	⋮	0
X		
Y		
⋮		

2. Arguments

Description	Storage Location	Data Length (Bytes)
Input	Start address of affine transform parameter table	R0 4
	Storage address of coordinates before affine transform	R1 4
	Storage address of coordinates after affine transform	R2 4

3. Internal Register Changes and Flag Changes

(Before Execution) → (After Execution)	
R0	Start address of affine transform parameter table → Undefined
R1	Storage address of coordinates before affine transform → Undefined
R2	Storage address of coordinates after affine transform → Undefined
R3	Work
R4	
R5	
R6	
R7	
R8	
R9	
R10	
R11	
R12	
R13	
R14	
R15	(SP)

- T

—

 — : No change
* : Change
0 : Fixed 0
1 : Fixed 1

4. Programming Specifications

Program memory (bytes)
34
Data memory (bytes)
0
Stack (bytes)
4
Number of states
22
Reentrant
Yes
Relocation
Yes
Intermediate interrupt
Yes

5. Description

(1) Function

Details of the arguments are as follows.

R0: Set the affine transform parameter table start address as the input argument.

R1: Set the storage address of the coordinates before affine transform as the input argument.

R2: Set the storage address of the coordinates after affine transform as the input argument.

Figure 1 shows an execution example for the software AFIN instruction. In memory, affine transform parameters are allocated in advance from address H'1000 0000 through t_x , A, B, t_y , C, and D, in that order. Coordinates before affine transform are allocated from address H'1000 1000 in the order X, Y. The affine transform parameter table start address, storage address for coordinates before affine transform, and storage address for coordinates after affine transform are transferred to the software AFIN as the input argument. Transform matrix operations are performed in AFIN software and coordinates after affine transform are allocated as specified in the input argument from address H'1000 1100 in the order X', Y'.

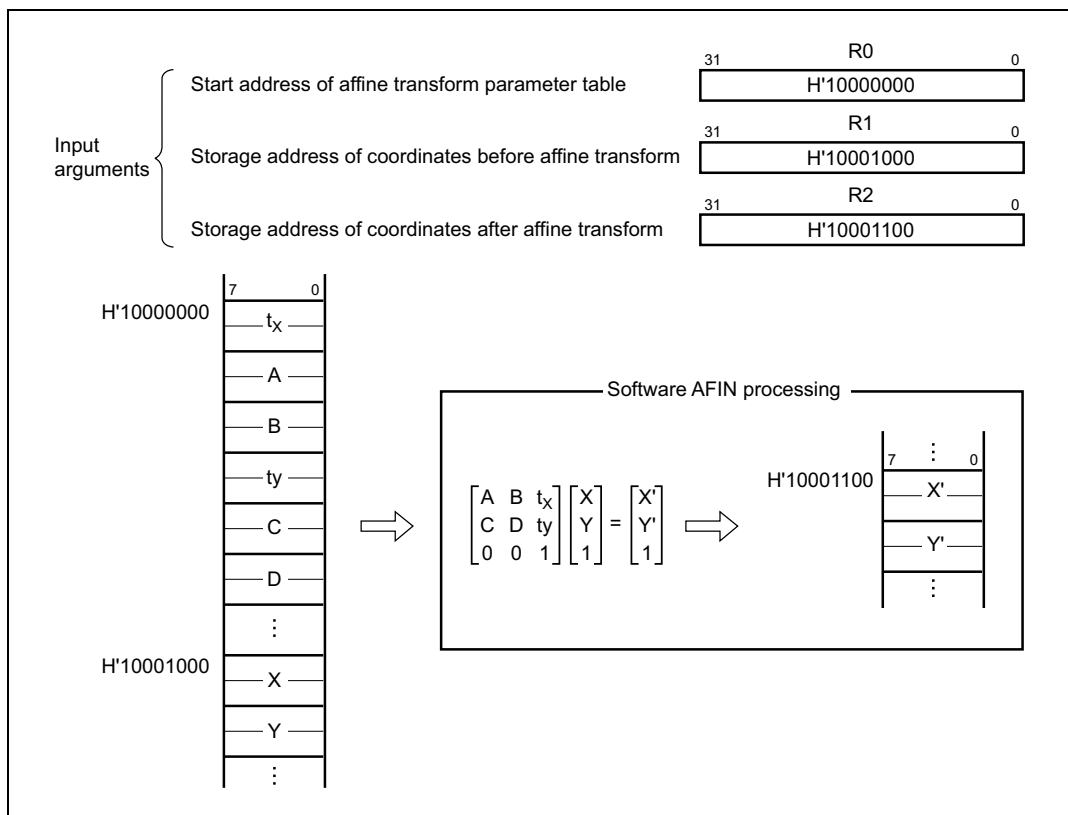


Figure 1 Software AFIN Execution Example

(2) Usage Notes

Affine transform parameters and coordinates should be allocated before the affine transform, as shown in figure 1.

(3) RAM Used

No RAM is used by the software AFIN instruction.

(4) Usage Example

After the affine transform parameter table start address, the storage address for coordinates before affine transform, and the storage address for coordinates after affine transform are set in input arguments, the AFIN software instruction is called from a subroutine.

```

MOV.L  DATA1, R0    . . . Sets affine transform parameter table start address in input argument
MOV.L  DATA2, R1    . . . Sets the storage address for coordinates before affine transform in input
                      argument
BSR    AFIN          . . . Subroutine call to software instruction AFIN
MOV.L  DATA3, R2    . . . Sets storage address for coordinates after affine transform in input argument
.
.
.
.
.align  4
DATA1  .data.1  H'10000000
DATA2  .data.1  H'10001000
DATA3  .data.1  H'10001100

```

(5) Operating Principle

- (a) Expanding the affine transform matrix produces the following formulas:

$$X' = AX + BY + t_x$$

$$Y' = CX + DY + t_y$$

- (b) As shown in figure 2, $AX + BY + t_x$ and $CX + DY + t_y$ are determined using the multiply and accumulate instruction (MAC).

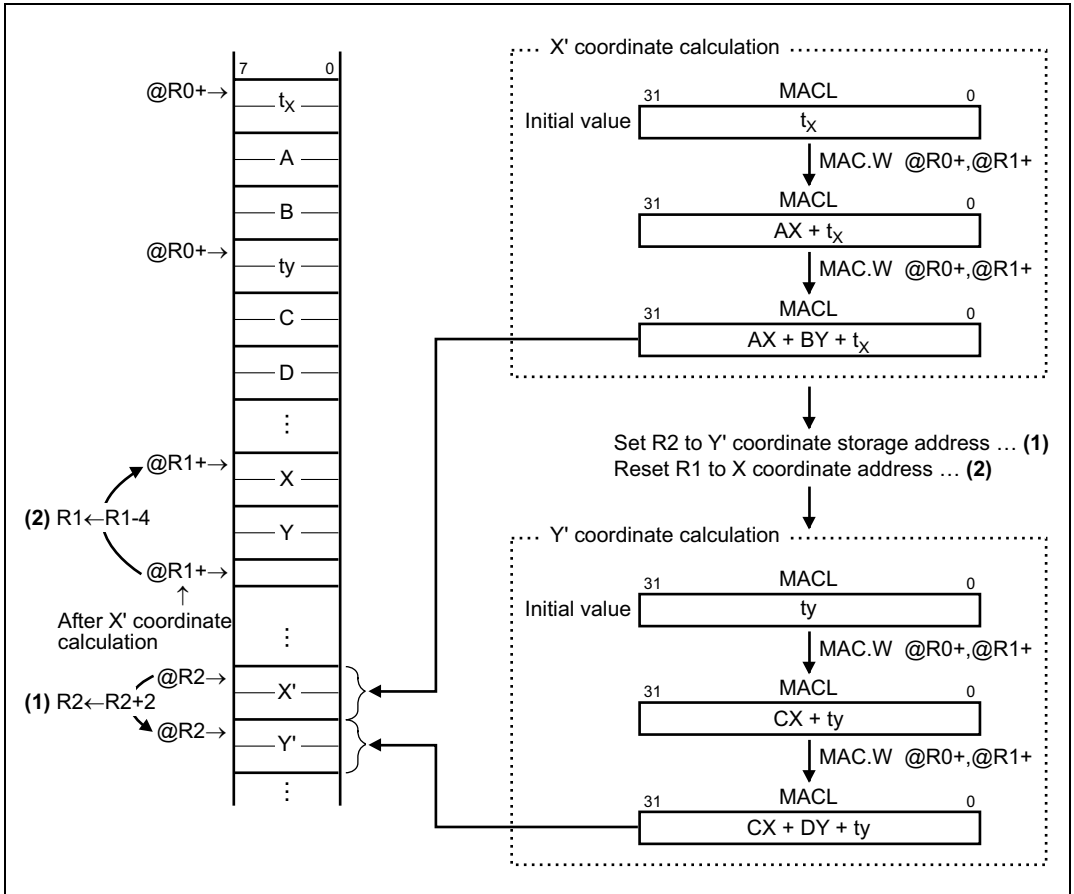
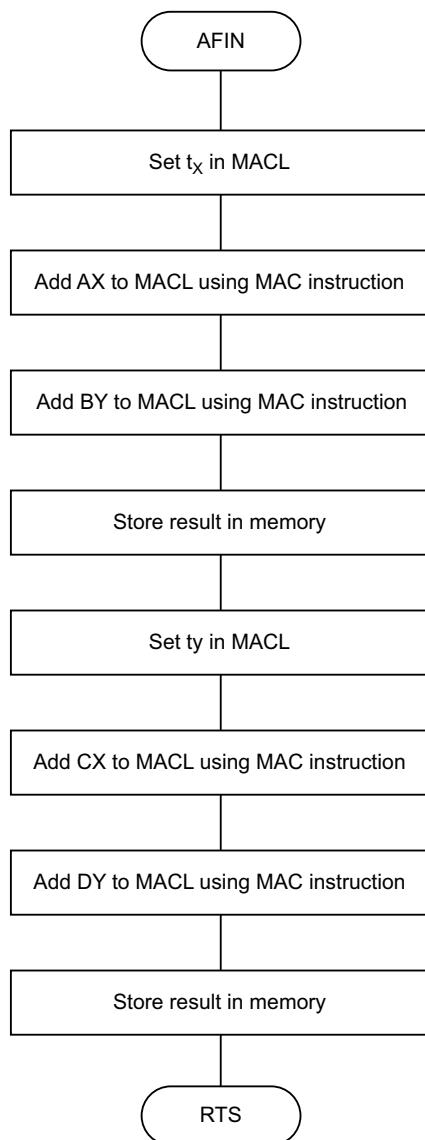


Figure 2 Calculation of X' and Y' Coordinates

6. Flowchart



7. Program Listing

```

1          1  ;*****
2          2  ;*
3          3  ;*      NAME ; AFIN CONVERSION (AFIN)
4          4  ;*
5          5  ;*****
6          6  ;*
7          7  ;*      ENTRY : R0 (TOP ADDRESS OF PARAMETER)
8          8  ;*      R1 (STORED ADDRESS OF BEFORE AFIN CONVERSION)
9          9  ;*      R2 (STOR ADDRESS OF AFTER AFIN CONVERSION)
10         10 ;*
11         11 ;*****
12 00001000 12      .SECTION A, CODE, LOCATE=H'1000
13          13  AFIN .EQU $      ; Entry point
14 00001000 2F36 14      MOV.L R3, @-R15 ; Escape register
15 00001002 6305 15      MOV.W @R0+, R3 ; tx -> MACL
16 00001004 431A 16      LDS R3, MACL ;
17 00001006 410F 17      MAC.W @R0+, @R1+ ; A=X+MACL -> MACL(=AX+Tx)
18 00001008 410F 18      MAC.W @R0+, @R1+ ; B=Y+MACL -> MACL(=AX+BY+Tx)
19 0000100A 031A 19      STS MACL, R3 ; MACL -> X'
20 0000100C 2231 20      MOV.W R3, @R2 ;
21 0000100E 7202 21      ADD #2, R2 ;
22 00001010 6305 22      MOV.W @R0+, R3 ; Ty -> MACL
23 00001012 431A 23      LDS R3, MACL ;
24 00001014 71FC 24      ADD #-4, R1 ;
25 00001016 410F 25      MAC.W @R0+, @R1+ ; C=X+MACL -> MACL(=CX+Ty)
26 00001018 410F 26      MAC.W @R0+, @R1+ ; D=Y+MACL -> MACL(=CX+DY+Ty)
27 0000101A 031A 27      STS MACL, R3 ; MACL -> Y'
28 0000101C 2231 28      MOV.W R3, @R2 ;
29 0000101E 000B 29      RTS ;
30 00001020 63F6 30      MOV.L @R15+, R3 ; Return register
31          31      .END

*****TOTAL ERRORS 0
*****TOTAL WARNINGS 0

```

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