HITACHI MICROCOMPUTER TECHNICAL UPDATE

DATE	25 January 2001	No.	TN-SH7-296A/E
THEME	Cache Behavior on Stopping Store Queue Clock Supply		
CLASSIFICATION	☐ Spec change ■ Limitation on Use ☐ Supplement of Documents		
PRODUCTNAME	SH7751		Lot
REFERENCE DOCUMENTS	SH7751 Hardware Manual SH-4 Programming Manual	Rev.	Effective Date
			Eternity

When using module standby function and stopping clock supply to Store Queue (SQ) , (Refer to SH7751 Hardware manual on Standby Control Register 2 at section 9.2.4), there occurs a limitation on cache behavior.

There is no limitation when clock supply to Store Queue is not stopped.

1. Contents

During the power-down mode stopping clock supply to Store Queue (MSTP6 bit in STBCR2 register is set to 1), write-back from cache to external memory cannot be performed correctly.

2. Workaround

When write-back is performed using operand cache (OC) (*1), the power-down mode stopping clock supply to Store Queue should not be used.

(*1) Write-back is performed where

Copy-back mode is specified for operand cache write mode selection (decided by CCR.CB bit, CCR.WT bit, or the value of the WT bit in the page management information when address translation is performed) or

OC address array write is performed using memory-mapped cache operation and an entry whose V bit and U bit are both 1’s is generated.