HITACHI SEMICONDUCTOR TECHNICAL UPDATE

Classification of Production	Development Environment		No	TN-OS*-074B/E	Rev	2
THEME	HI7700/4 The restriction matter at the time of undefined interruption	Classification of Information	1. Spec change 2. Supplement of Documents 3. Limitation of Use 4. Change of Mask 5. Change of Production Line			
PRODUCT NAME	HS0770ITI41SRE, HS0770ITI41SRB, HS0770ITI41SRS, HS0770ITI41SRE-E, HS0770ITI41SRB-E, HS0770ITI41SRS-E	Lot No. V1.00r1, V1.01r1, V1.0Ar1, V1.0Br1, V1.0Cr1, V1.1.00, V1.2.00	Reference Documents	HI7000/4 series User's Manual (ADE-702-248A)	Effective Date Forever	

Please care about a restriction matter given in the following appending data about undefined interruption.

[Attached document]

" [HI7700/4] The restriction matter at the time of undefined interruption " (HI7700/4-INTDWN-030225(E))"

Note:

This document corrects the clerical error of TN-OS-074A/E.

There is no change of attached document(HI7700/4-INTDWN-030225(E)).

Correction part:

Clerical error correction of the version number of a product

[Before] V1.00r1, V1.01r1, V1.0Ar1, V1.0Br1, V1.0Cr1, V1.0.04, V1.0.05

[After] V1.00r1, V1.01r1, V1.0Ar1, V1.0Br1, V1.0Cr1, **V1.1.00, V1.2.00**

[HI7700/4] The restriction matter at the time of undefined interruption

1. Phenomenon

If undefined interruption occurs when no interrupt handler is performed, the parameter "inf1" (R6 register : PC at the interruption) and "inf2" (R7 register : SR at the interruption) passed to the system-down routine will become inaccurate.

2. Countermeasure

Please modify the file "***nnnn***_intdwn.src" which is stored in the "hiuser\sh***nnnn***" folder as follows.

[Note] "***nnnn***" Bold-faced-italic ***nnnn*** is the CPU name used for the sample file name.
Example: The actual file for SH7729 is "7729_intdwn.src".

```
;************************************************************************;
;*  NAME      = __kernel_undefint                                       ;*;
;*  FUNCTION  = undefined interrupt routine                             ;*;
;************************************************************************;
__kernel_undefint:

    (Omission)

        mov.l   @(EXPEVT,r5),r5         ; get EXPEVT code
        mov.l   #SYSDWN16,r4            ; get error type
        mov.l   @(36,r15),r6            ; get PC
        mov.l   @(40,r15),r7            ; get SR


    (Omission)

        mov.l   #__kernel_sysdwn,r0
        jsr     @r0                     ; call __kernel_sysdwn
        nop
;
        .pool

    (Omission of the rest)
```

Please replace these 2-lines the following.

```
  stc     r6_bank,r0  ; get R6_bank1
  and     #H'3f,r0    ; get nest counter
  cmp/eq  #1,r0       ; if nest == 1
  bt      undefint020 ; then undefint020
  mov     r15,r1      ; get frame address
undefint010:
  mov.l   @(36,r1),r6 ; get PC
  mov.l   @(40,r1),r7 ; get SR
```

Please add the 4-lines just before ".pool."

```
undefint020:
  stc     r7_bank,r0  ; get R7_bank1
  bra     undefint010
  mov.l   @r0,r1      ; get frame address
```