SH-5 EVALUATION DEVICE

64-Bit Embedded SuperH RISC Evaluation Device

PRELIMINARY DATA

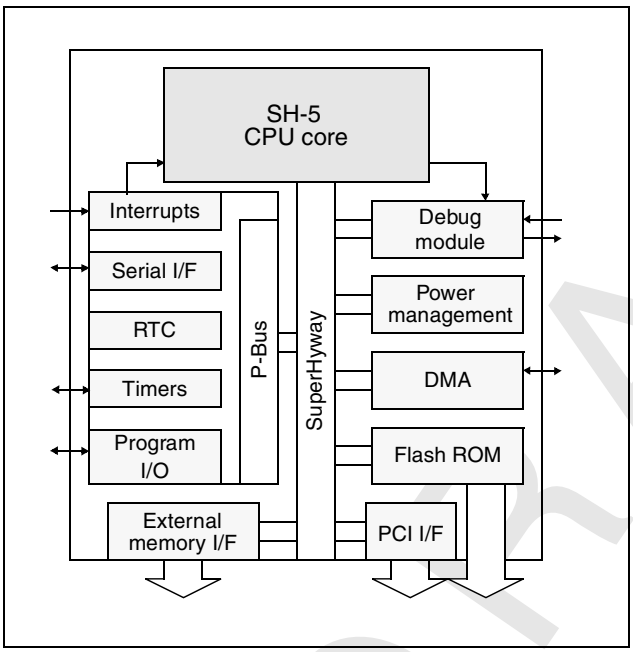
Overview

The SH-5 evaluation device is the first implementation of the SH-5 CPU core developed by SuperH.

It has been designed for use in development systems and application reference platforms for both 3rd party developers and SH-5 customers.

The integration of a PCI interface allows many standard peripherals to work with the SH-5 prior to application specific silicon devices being developed.

Evaluation platforms will be provided that include this device enabling developers to benchmark and start development with the SH-5 family.



CPU features

- **SH-5 core operating at 400 Mhz**
  - 604 Dhrystone v2.1 MIPS, 714 Dhrystone v1.1 MIPS
  - 9.6 GOPS
  - 2.8 GFLOPS
  - 64-bit CPU
- **64-bit multimedia unit (SIMD)**
- **64x64-bit integer/multimedia register set**
- **IEEE 754 floating point unit**
  - Vector 3D graphics operations
  - 64x32-bit FP register set
- **Efficient support for 32 and 64-bit applications**
- **Advanced debug support**
- **Virtual caches for high performance and low power**
  - 4-way set associative, 32 byte line
  - 32 Kbyte instruction cache, 32 Kbyte data cache
  - Extensive support for SW control of caches including locking of critical instructions and data
- **Memory protection and relocation through memory management unit**
  - Fully associative TLBs (64 entry ITLB, DTLB)
  - Variable page sizes (4 K, 64 K, 1 M, 512 M)

System Features

- **3.2 Gbytes/s SuperHyway interconnect with integrated analyzer for advanced trace and watchpoint**
- **Advanced debug module with special support for system debug and a high speed full duplex SHDebug link**
- **PCI interface 32-bit @ 66MHz**
- **32-bit flash/ROM/MPX interface**
- **High performance SDRAM interface**
  - Supports both PC100 and DDR 266 (PC2100)
  - 32/64 bit at up to 133MHz
- **Interrupt controller**
  - Up to 64 interrupts
  - 15 programmable priority levels and NMI
- **4-channel DMA controller**
- **Real time clock with calendar functions**
- **3 channel timer unit**
- **Watchdog timer**
- **Asynchronous serial interface**
- **Power management unit**
- **456 pin BGA package**

Table of Contents

1 Scope of this document

This document serves as an introduction to the SH-5 evaluation device. It also provides a preliminary guide for platform designers. Programming and configuring the device is described in the following documents:

- SH-5 CPU Core Architecture Manual,
- SH-5 System Architecture Manual.

2 SH-5 documentation suite

This document describes the device specific aspects of the SH-5 evaluation device. It references a number of other, more general, SH-5 documents that combine to support deployment of this device.

2.1 CPU documentation

The SH-5 CPU core and its instruction set are documented in the *SH-5 CPU Core Architecture Manual* which is organized as 4 volumes:

- SH-5 CPU core, Volume 1: Architecture
- SH-5 CPU core, Volume 2: SHMedia
- SH-5 CPU core, Volume 3: SHCompact
- SH-5 CPU core, Volume 4: Implementation

2.2 System documentation

Devices listed in the system address map, *Section 6.2 on page 24* are documented in the *SH-5 System Architecture Manual*:

- *Volume 1: System*, details the system organization and standard peripherals.
- *Volume 2: Bus Interfaces*, details the standard PCI, EMI and FEMI bus interfaces.
- *Volume 3: Debug*, details the debug module, the SHDebug link, the CPU's watchpoint controller and the bus analyzer.

2.3 Application notes

In addition to the architectural information, a number of application notes will be available.

3 CPU core overview

3.1 Introduction

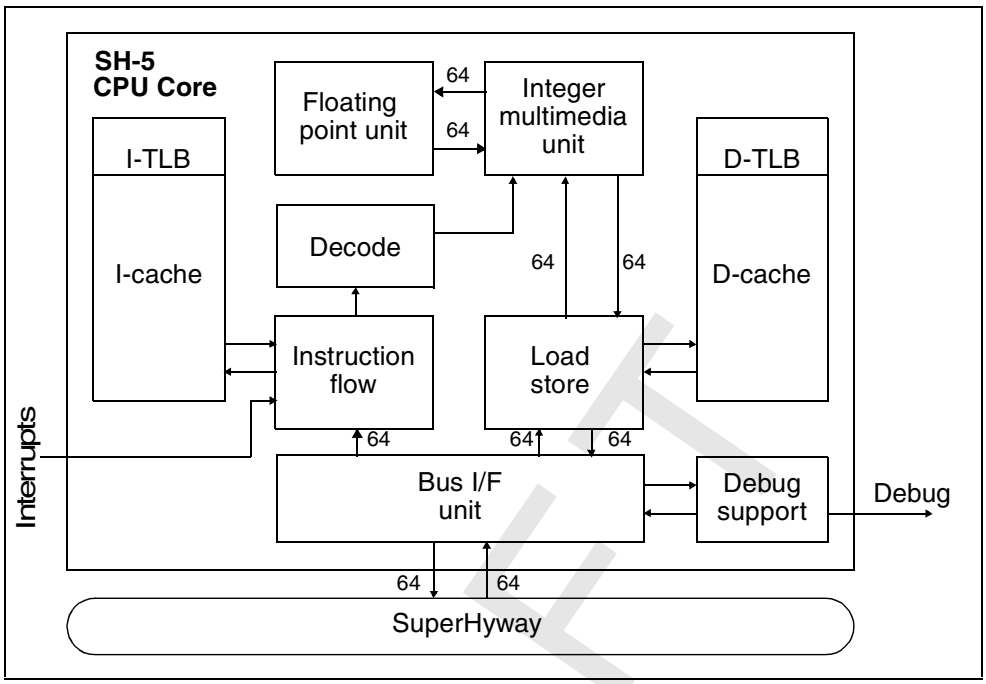


Figure 1: CPU core overview

The SH-5 core is a high performance, low power, small silicon area, 64-bit embedded processor RISC CPU and is the latest member of the industry leading SuperH family.

It is designed for use in embedded systems in the Consumer, Digital TV, Telecommunications, and Automotive markets with support for software applications written in C/C++ and Java, running in environments such as WinCE and Linux.

The SH-5 is a single issue, pipelined processor with full data forwarding to ensure minimum CPU stalls. It is equipped with optimized, four-way set associative, virtual instruction and data caches, as well as fully associative instruction and data TLBs.

This core provides powerful support for multimedia applications through its comprehensive set of SIMD instructions. An optional IEEE 754 floating point unit provides outstanding support for 3D Graphics processing by inner product and vector transformation instructions.

The instruction set architecture supports a fully SH-4 compatible mode for legacy software or higher code density and a 64-bit native mode for high performance or multimedia modules. Fully flexible mode switching allows compilers to optimize for code density or performance, and implements a split branch feature to allow cost effective branch performance

Advanced, non-intrusive debug capabilities promote development of real time systems. These capabilities include real time trace.

This core is provided as an ASIC module for incorporation into system-on-chips. It has an interface to the 200 MHz, pipelined, split transaction, on-chip SuperHyway interconnect.

3.2 Features

3.2.1 General

- 64-bit architecture: 64-bit data and addressing.
- SHmedia for performance, multimedia and future.
- SHcompact for code density and compatibility.
- Fully flexible mode switch (typically at call/return).
- Split branch for cost-effective branch performance.
- Support for real-time embedded kernels.

3.2.2 Registers and memory

- Program counter.
- 64 x 64-bit integer/multimedia registers (R63 is 0).
- Large register files for optimizing compilers.
- Allow aggressive in-line, unroll, s/w pipelining.
- Easily mix scalar and multimedia operations.
- 64 x 32-bit floating-point registers + status register.
- 8 target registers for branch target addresses.
- 2 user-visible control registers.
- 15 privileged control registers (status, events).
- 32-bit configuration space for MMU and cache.

3.3 Instruction set

The SH-5 CPU core supports two basic instruction set formats, SHcompact and SHMedia, which may be intermixed in general code. The SHcompact set is based on a 16 bit encoding which is compatible with SH-4 code, and ensures high code density giving efficient use of memory. The SHMedia instruction set uses a 32 bit encoding allowing code full access to the performance advantage of an advanced 64 bit architecture with SIMD support, and allowing future optimizations whilst maintaining code compatibility.

3.3.1 SHCompact

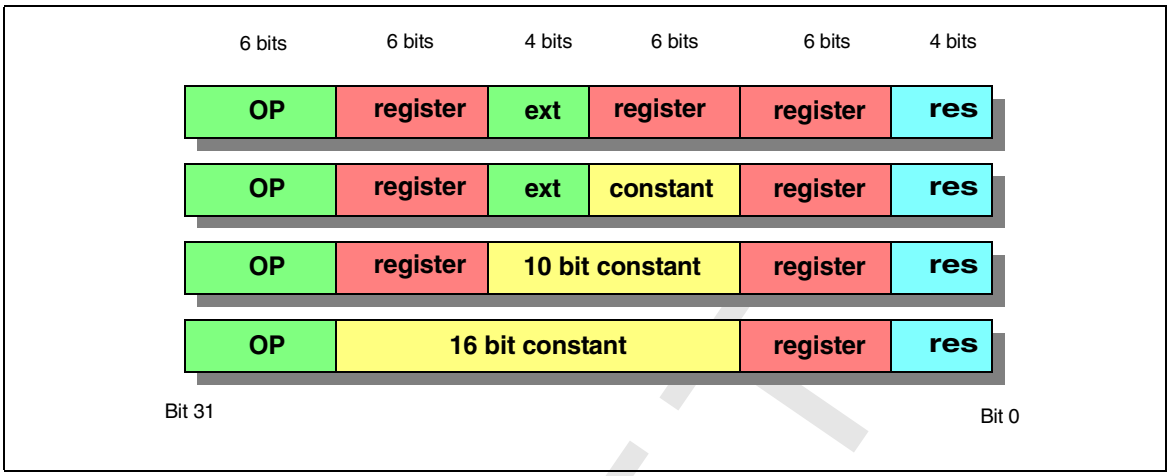
Overview

- Instruction set is binary compatible with SH-4.
- 16-bit encoding for code density.
- Provides all SH-4 user instructions.
- All privileged-only instructions cause exception.
- Mode switch mechanism through bottom bit of PC.

3.3.2 SHMedia

Overview

- Regular 32-bit encoding, 1/2/3-operand formats.
- 6(+4)-bit opcodes, 6-bit register fields, 4 reserved.



Branch

- Prepare-target: load address into target register.
- Typically used to prefetch target instructions.
- Branch instructions: compare and branch to target.
- Static prediction bits on prepare-target and branch.
- Mode switch mechanism through bottom bit of PC.

Integer

- Sufficient set for 32-bit and 64-bit operation.
- 32-bit integers held in a sign-extended 64-bit form.
- 32 x 32 to 64-bit multiply.
- No overflow checking, no condition code, no carry.
- Count sign bits, byte reversal, conditional move.

Memory

- Memory accessed by 64-bit effective address.
- Aligned load/store for B, UB, W, UW, L and Q.
- Addressing: reg + reg and reg + scaled 10-bit imm.
- Specific support for misaligned load and store.
- Cache control and synchronization instructions.

Multimedia

- Optimized for DSP, image and audio processing.
- Packed 8-bit, 16-bit and 32-bit data.
- Compare, add, subtraction, absolute.
- Shifts (with and without saturation).
- Fractional multiplication and multiply accumulate.
- 2 MACs or 4-way sum of products in 1 instruction.
- Sum of absolute differences (motion estimation): byte data, 24 operations in a single instruction.
- Conditional move, conversions, shuffle, permute.

Floating point

- Detachable floating-point unit, IEEE754 arithmetic.
- Single (32-bit) and double (64-bit) precision.
- Support for 4-element vectors, and 4x4-matrices.
- Graphics support: e.g. 4-way sum-of-products.

System

- Control and configuration register access.
- Kernel trap, debug trap, return from exception.

3.4 Memory management and caches

The CPU core is equipped with 32 Kbyte virtual instruction and data caches that are four-way set associative (32-byte cache line) and optimized for high speed and low power. Fully-associative transaction lookahead buffers (TLBs) with 64 entries for memory management, including memory protection and translation, are provided.

The caches are organized as 4 sets of 256 lines, each line containing 32 bytes, provide four operating modes, (WB, WT, UN, DEV) using a LRU replacement algorithm with the ability to lock specific areas of the cache to avoid critical code/data eviction. The CPU is able to control the caches directly via memory mapped register state and the use of cache control instructions.

3.5 Debug support

The SH-5 evaluation device supports advanced non-intrusive debug features for both the core and the system, and may be attached to an external debugger via the JTAG or SHdebug ports.

The JTAG port corresponds to the industry standard bi-directional JTAG interface, and may be used to download code, issue commands such as read/write, single step, for example. The 11-pin SHdebug port also provides all of these features, and additionally supports high peformance debug features such as conditional tracing to branches or memory operations, and can supply visibility of all SuperHyway traffic external to the core. Extensive support is also available for performance analysis of the system, allowing measurement of cache misses, TLB operations, pipeline freezes for example.

4 SHmedia performance characteristics

4.1 Definitions

The definition of the terms **pitch** and **latency** (which are used in the following sections) is:

Pitch	The pitch of an instruction X is the number of machine cycles which must occur between the issuing of an instance of X and the issuing of the immediately following instruction when its operands are independent of X's results. SH-5 is a single-issue implementation and all instructions have a pitch of at least 1.
Latency	The latency of an instruction X is the number of machine cycles which must occur between the issuing of an instance of X and the issuing of a following instruction which uses one of X's results as an operand. This following instruction will be stalled until the required latency is reached. There can be other independent instructions between X and the stalled instruction in some cases. Many integer instructions have latency 1. Instructions with latency greater than 1 compute their results later in the pipeline. The following instruction must be stalled until the result is available.

4.2 SHmedia branching

The tables below show the penalties incurred by the SHmedia branch operations. All data assumes a PTA instruction is followed by a branch instruction some number of instructions later. The number of extra penalty cycles depends on the number of instructions between the PTA and the branch, referred to in the table as the **gap**.

Table 1 shows the branch penalties when the PTA instruction indicates a branch to the target is unlikely. The gap=0 row **includes** the one cycle penalty due to the PTx instructions having latency 2.

PTA/U	Uncond.	Cond. Branch Not Taken		Cond. Branch Taken	
Gap		Predicted	Mispredict	Mispredict	Predicted
	BLINK	BNE/U 0,0	BNE/L 0,0	BEQ/U 0,0	BEQ/L 0,0
0	3	1	3	6	3
>0	2	0	2	5	2

Table 1: Branch penalties without prefetch

Table 2 shows the branch penalties when the PTA instruction indicates a branch to the target is likely. The ranges 0-1, 1-2 and 2-3 indicate that one of two penalties is possible, depending on whether the branch instruction itself is 8 byte aligned.

PTA/L Gap	Target is 8 byte aligned?	Uncond.	Cond. branch not taken		Cond. branch taken	
			Predicted	Mispredict	Mispredict	Predicted
		BLINK	BNE/U 0,0	BNE/L 0,0	BEQ/U 0,0	BEQ/L 0,0
0	YES or NO	3	1	3	3	3
1	YES or NO	2	0	2	2-3	2
2	YES or NO	1-2	0	2	2	1-2
3	NO	1	0	2	2	1
3	YES	0-1	0	2	2	0-1
4	NO	0-1	0	2	2	0-1
4	YES	0	0	2	2	0
>4	YES or NO	0	0	2	2	0

Table 2: Branch penalties with prefetch

The table assumes that no other PTA/L instructions have recently been issued. If more than one PTA/L has been issued, prefetching is prioritized according to target register numbers. TR0 has the highest priority and TR7 the lowest. A branch which specifies a lower priority target register can incur additional penalty cycles if contention for prefetch occurs.

When two conditional branches are adjacent in the instruction stream, a one cycle penalty occurs. If other penalties are associated with the second branch (for example, its target has not been prefetched), this penalty will be hidden by the other penalties.

4.3 CPU pipeline

Pitches and latencies for the integer and multimedia instructions are shown in *Table 3*. Branch instructions are discussed in *Section 4.2*. Memory access instructions are discussed in *Section 4.5* and privileged operations in *Section 4.6*.

Instruction	Notes	Pitch	Latency
ADD		1	1
ADD.L		1	1
ADDI		1	1
ADDI.L		1	1
ADDZ.L		1	1
AND		1	1
ANDC		1	1
ANDI		1	1
BEQ, BEQI BGE, BGEU BGT, BGTU BLINK, BNE BNEI	See *Section 4.2*	varies	varies

Table 3: Pitches and latencies for integer and multimedia instructions

Instruction	Notes	Pitch	Latency
BYTEREV		1	1
CMPEQ		1	1
CMPGT		1	1
CMPGTU		1	1
CMVEQ		1	1
CMVNE		1	1
GETCON		1	2
GETTR		1	1
MABS.L		1	2
MABS.W		1	2
MADD.L		1	1
MADD.W		1	1
MADDS.L		1	2
MADDS.UB		1	2
MADDS.W		1	2
MCMPEQ.B		1	2
MCMPEQ.L		1	2
MCMPEQ.W		1	2
MCMPGT.L		1	2
MCMPGT.UB		1	2
MCMPGT.W		1	2
MCMV		1	1
MCNVS.LW		1	2
MCNVS.WB		1	2
MCNVS.WUB		1	2
MEXTR1		1	1
MEXTR2		1	1
MEXTR3		1	1
MEXTR4		1	1
MEXTR5		1	1
MEXTR6		1	1
MEXTR7		1	1
MMACFX.WL MMACNFX.WL	When result is used as the accumulation operand of following MAC-class operation[a]	1	1
	Otherwise	1	3

Table 3: Pitches and latencies for integer and multimedia instructions

Instruction	Notes	Pitch	Latency
MMUL.L		2	4
MMUL.W		1	3
MMULFX.L		2	4
MMULFX.W		1	3
MMULFXRP.W		1	3
MMULHI.WL		1	3
MMULLO.WL		1	3
MMULSUM.WQ	When result is used as the accumulation operand of following MAC-class operation[A]	1	1
	Otherwise	1	3
MOVI		1	1
MPERM.W		1	1
MSAD.UBQ	When result is used as the accumulation operand of following MAC-class operation[A]	1	1
	Otherwise	1	3
MSHALDS.L		1	2
MSHALDS.W		1	2
MSHARD.L		1	1
MSHARD.W		1	1
MSHARDS.Q		1	2
MSHFHI.B		1	1
MSHFHI.L		1	1
MSHFHI.W		1	1
MSHFLO.B		1	1
MSHFLO.L		1	1
MSHFLO.W		1	1
MSHLLD.L		1	1
MSHLLD.W		1	1
MSHLRD.L		1	1
MSHLRD.W		1	1
MSUB.L		1	1
MSUB.W		1	1
MSUBS.L		1	2
MSUBS.UB		1	2
MSUBS.W		1	2
MULS.L		1	3

Table 3: Pitches and latencies for integer and multimedia instructions

Instruction	Notes	Pitch	Latency
MULU.L		1	3
NOP		1	1
NSB		1	1
OR		1	1
ORI		1	1
PTA, PTABS PTB, PTREL	When TR result is used by following branch	1	2
	When TR result is used by following GETTR	1	5
PUTCON		5	5
SHARD		1	1
SHARD.L		1	1
SHARI		1	1
SHARI.L		1	1
SHLLD		1	1
SHLLD.L		1	1
SHLLI		1	1
SHLLI.L		1	1
SHLRD		1	1
SHLRD.L		1	1
SHLRI		1	1
SHLRI.L		1	1
SHORI		1	1
SUB		1	1
SUB.L		1	1
XOR		1	1
XORI		1	1

Table 3: Pitches and latencies for integer and multimedia instructions

a. The MAC-class operations are MMACFX.WL, MMACNFX.WL, MMULSUM.WQ and MSAD.UBQ

4.4 FPU pipeline

Table 4 shows the pitches and latencies for the floating point instruction set. The pitch information for FDIV and FSQRT must be interpreted in conjunction with *Section 4.4.1*.

The instruction latencies depend on the relationship between the precision of the result produced by the operation, and the precision of the input operand of the dependent instruction. For example, FADD.S has a latency of 6 cycles in:

```
FADD.S FR0, FR0, FR2
FMOV.S FR2, FR4
```

and a latency of 7 cycles in:

```
FADD.S FR0, FR0, FR2
FMOV.D DR2, DR4
```

The operand types are as follows. In each example, the dependency is between the result of the first instruction (DR18 or R10) and the first operand of the following instruction.

Instruction	Notes	Pitch	Latency with dependent operand of type:					
			S	D	P	V	M	Int
FABS.D		1	7	4	4	7	7	
FABS.S		1	4	7	7	7	7	
FADD.D		1	7	6	6	7	7	
FADD.S		1	6	7	7	7	7	
FCMPEQ.D		1						3
FCMPEQ.S		1						3
FCMPGE.D		1						3
FCMPGE.S		1						3
FCMPGT.D		1						3
FCMPGT.S		1						3
FCMPUN.D		1						3
FCMPUN.S		1						3
FCNV.DS		1	6	7	7	7	7	
FCNV.SD		1	7	6	6	7	7	
FCOSA.S		5	10	11	11	11	11	
FDIV.D	*Section 4.4.1*	32	36	35	35	36	36	
FDIV.S	*Section 4.4.1*	16	19	20	20	20	20	
FGETSCR		1	6	7	7	7	7	
FIPR.S		1	6	7	7	7	7	
FLOAT.LD		1	7	6	6	7	7	
FLOAT.LS		1	6	7	7	7	7	
FLOAT.QD		1	7	6	6	7	7	
FLOAT.QS		1	6	7	7	7	7	

Table 4: Pitches and latencies for FPU instructions

Instruction	Notes	Pitch	Latency with dependent operand of type:					
			S	D	P	V	M	Int
FMAC.S		1	6	7	7	7	7	
FMOV.D		1	7	4	4	7	7	
FMOV.DQ		1						3
FMOV.LS		1	4	7	7	7	7	
FMOV.QD		1	7	4	4	7	7	
FMOV.S		1	4	7	7	7	7	
FMOV.SL		1						3
FMUL.D		4	10	9	9	10	10	
FMUL.S		1	6	7	7	7	7	
FNEG.D		1	7	4	4	7	7	
FNEG.S		1	4	7	7	7	7	
FPUTSCR	*Section 4.4.3*	8	8	8	8	8	8	
FSINA.S		5	10	11	11	11	11	
FSQRT.D	*Section 4.4.1*	32	36	35	35	36	36	
FSQRT.S	*Section 4.4.1*	16	19	20	20	20	20	
FSRRA.S		5	10	11	11	11	11	
FSUB.D		1	7	6	6	7	7	
FSUB.S		1	6	7	7	7	7	
FTRC.DL		1	6	7	7	7	7	
FTRC.DQ		1	7	6	6	7	7	
FTRC.SL		1	6	7	7	7	7	
FTRC.SQ		1	7	6	6	7	7	
FTRV.S	*Section 4.4.2*	4	6-9	8 or 10	8 or 10	10	10	

Table 4: Pitches and latencies for FPU instructions

4.4.1 Execution of divide and square-root instructions

The divide and square-root instructions (FDIV.S, FDIV.D, FSQRT.S, FSQRT.D) are executed in part using resources separate from the main FPU pipeline. Subject to certain conditions, this allows these instructions to execute in parallel with other FPU activity. After completing the ‘offline’ phase, the partial results merge with the main FPU pipeline for final processing.

An instance of FDIV or FSQRT occupies a normal issue cycle when first encountered. Each instance requires further issues slots when the completion phase occurs: 1 cycle for FDIV.S / FSQRT.S, and 2 cycles for FDIV.D/FSQRT.D. The insertion of these slots delays the issue of FPU instructions later in the execution sequence.

The conditions for a subsequent FPU instruction to be able to execute in parallel with the ‘offline’ phase of FDIV and FSQRT are:

- None of its operands must depend on the FDIV or FSQRT result.
- Its result must not lie in the same vector group (of 4 FPU registers) as that of the FDIV/FSQRT. For example, suppose an FDIV.D has DR2 as its result register. Then any instruction having FR0, FR1, FR2, FR3, DR0 or DR2 as its result will be blocked until the FDIV.D has completed. An instructions having FR4-FR63 or DR4-DR62 as its result will be able to execute in parallel, subject to the other conditions being met.
- It must not be another FDIV or FSQRT instruction.

If any of these conditions are not met, the non-compliant instruction will not be issued until after the FDIV/FSQRT has re-merged with the main FPU pipeline. In that case, the new instruction will be issued at least 16 cycles after a FDIV.S/FSQRT.S or 32 cycles after a FDIV.D/FSQRT.D. After a instruction becomes blocked in this way by the FDIV/FSQRT, no other instruction can be issued until the FDIV/FSQRT completes; there is no further out-of-order issue.

4.4.2 Execution of the FTRV.S instruction

The FTRV.S instruction can be considered as 4 FIPR.S instructions executed in sequence by a single instruction. The 4 single precision results making up the result vector will be available on successive cycles. If the result is FVn, the 4 results FRn, FR(n+1), FR(n+2), FR(n+3) will be available in that order.

Consequently, the latency of the FTRV.S instruction depends on which of the 4 results is required. If the dependent instruction takes a double precision operand, both the single precision results making up the double precision operand must be available before the dependent instruction can be issued.

4.4.3 Execution of the FPUTSCR instruction

This has a fixed pitch and latency of 8 cycles regardless of the type of the next floating point instruction.

4.5 Memory operations

This section describes the performance for memory operations. These figures only take account of penalties within the SH-5 core itself, up to and including its interface with the SuperHyway bus. Access cycles on the SuperHyway and in external RAM are **not** included in these figures.

The information in *Table 5* below shows the pitch of the indicated pattern of loads and stores. In the cases with two operations, both are to addresses in the same cache line. The table shows whether the same address or different addresses in the line
is/are accessed. The second operation is therefore effectively a cache hit in each case. The LD/ST cases assume the target of the load is not the register read by the store.

The “virtual miss, physical hit” column is for the case where there are multiple virtual addresses mapping to the same physical address, and the physical line is in the cache but tagged with one of the alternative virtual addresses. Note that these cases are **not** subject to additional penalties arising from external memory access.

If the result of a load instruction is used too soon afterwards, stalls will occur in accordance with the latency of the load instruction. *Table 6* shows the increments that have to be added to the pitch values to arrive at the latencies, depending on the type of load instruction and type of dependent operand in the following instruction.

Instruction sequence	Same address?	Write-through cache				Write-back cache			
		Cache hit	Virtual miss physical hit	Cache miss clean eviction	Cache miss dirty eviction	Cache hit	Virtual miss physical hit	Cache miss clean eviction	Cache miss dirty eviction
LD	n/a	1	6	14	14	1	6	14	16
ST	n/a	5	5	5	5	1	5	8	10
SWAP.Q	n/a	17	17	17	17	17	17	17	17
LD/LD	YES	2	12	20	20	2	12	20	22
LD/LD	NO	2	12	20	20	2	12	20	20
ST/LD	YES	9	9	22	22	5	9	20	22
ST/LD	NO	6	11	19	19	2	11	20	22
LD/ST	YES	6	11	24	24	2	11	20	22
LD/ST	NO	6	11	24	24	2	11	20	22
ST/ST	YES	13	13	13	13	5	9	20	22
ST/ST	NO	10	10	10	10	2	10	20	22

Table 5: Cycles taken by combinations of load and store operations

Type of load	Additional latency cycles for dependent operand of type:					
	S	D	P	V	M	Int
LD*						+2
FLD.S	+3	+6	+6	+6	+6	
FLD.P	+6	+3	+3	+6	+6	
FLD.D	+6	+3	+3	+6	+6	

Table 6: Conversion factors to give load latency from pitch

4.6 Privileged instructions and exceptions

Table 7 shows the number of penalty cycles incurred when exception are launched or returned from. The instruction causing the change of flow requires 1 issue slot itself, as usual, whether this is an explicit instruction or one that causes a TLB miss.

Instruction or condition	Penalty cycles
TRAPA Rm	9
BRK	9
RTE	7
DTLB miss	9

Table 7: Penalty cycles for exception launch/return

Table 8 shows the number of penalty cycles incurred by the GETCFG and PUTCFG instructions (in addition to the 1 cycle taken by any instruction). The pitch of the instructions can be considered to be 1 cycle more. The figures assume the load/store hardware is quiescent before the measurement starts (for example, by using SYNCO).

Accesses to MMUIR, ICACHETAG and ICACHEDATA are arbitrated with instruction fetch and can occur additional penalties depending on fetch timing. It is assumed that the next 8 instructions are in the cache[1], and that no PREFI instructions for addresses not currently in the cache have recently been issued. If either of these conditions is not met, the penalties will be extended accordingly.

The worst case assumes all branch target registers are marked ‘likely, and have just been assigned. The best case assumes all branch target registers are either marked ‘unlikely’, or have not recently been assigned to.

Area of config. register space	Address	GETCFG		PUTCFG	
		Best case penalty cycles	Worst case penalty cycles	Best case penalty cycles	Worst case penalty cycles
MMUIR	0x000xxxxx	10	28	8	25
MMUDR	0x008xxxxx	8	8	6	6
ICACHETAG	0x010xxxxx	10	28	Undefined behavior	
ICACHEDATA	0x012xxxxx	10	28		
ICCR	0x016xxxxx	6	6	8	8
OCACHETAG	0x018xxxxx	8	8	Undefined behavior	
OCACHEDATA	0x01axxxxx	8	8		
OCCR	0x01exxxxx	8	8	6	6

Table 8: Penalty cycles for GETCFG and PUTCFG

1. When there is a branch in the next 3 instructions, the branch target and its following instruction need to be in the cache as well.

5 System overview

5.1 Introduction

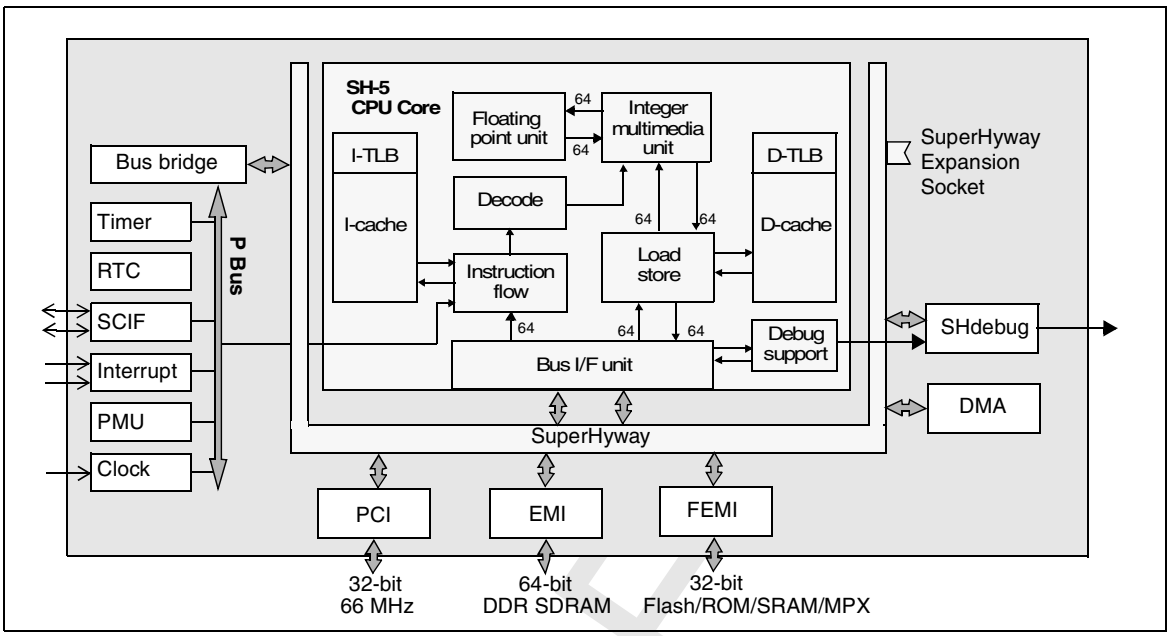


Figure 2: SH-5 architecture

The SH-5 evaluation device is the first product of the SH-5 range of devices and supplies a high performance core with a rich set of peripherals. These are described in the following text.

5.2 SuperHyway internal interconnect

The SH-5 evaluation device uses the SuperHyway memory mapped interconnect for high performance on-chip communication. The interconnect supports a pipelined, split transaction system allowing non-block, low latency, high throughput systems to be built.

This device implementation supports transfer rates between system peripherals of upto 3.2 GBytes/sec with the ability to simply add additional on-chip peripherals with full access for customer specific variants.

5.3 On-chip peripherals

5.3.1 DMA controller

The device includes a four channel, high performance DMA controller designed to support high speed device to memory, memory to device and memory to memory transfers. The DMA controller supports transfer widths from 1 to 32 bytes and has a number of operating modes designed to efficiently support multiple transfers without loading the CPU.

5.3.2 Interrupt controller

The interrupt controller supports upto 64 interrupt signals. Each interrupt has user defined priority between 0 and 15, may be individually masked and can generate an unique event code to the CPU. The interrupt controller may be cascaded with additional off-chip interrupt controllers.

5.3.3 Real time clock

The device includes a real time clock macro, which includes all the on chip logic required to generate a low speed clock from a 32.768 kHz crystal. This includes clock and calendar functions, alarm and periodic interrupts and has a maximum resolution of $^1/_{256}$ second.

5.3.4 Timers

The 3-channel, auto-reload, 32-bit timer has an input capture function and a choice of seven counter input clocks. The timers may be used to generate periodic interrupts, or for providing a watchdog function for the system. Whilst in low power modes, the timers may use the 32 kHz real time clock.

5.3.5 Synchronous serial channel

There is a full-duplex communication channel (SCIF). Asynchronous mode is supported. A separate 16-byte FIFO is provided for the transmitter and receiver.

5.3.6 PMU

The power management unit provides the following power modes:

- normal mode,
- economy mode,
- sleep mode,
- standby mode:
  - ➢ quick wakeup standby,
  - ➢ deep standby.

5.4 Clocks

The SH-5 evaluation device includes support for two crystal oscillators, which supply the main system clock and the RTC clocks. The system clock is derived from a crystal using an on-chip PLL from which is derived the internal system clocks.

The frequency of the internals may be configured using the MODE pins at reset, and may be re-configured by software to optimize system performance or reduce system power consumption.

5.5 Bus Interfaces

5.5.1 External memory interface

The EMI supports both SDRAM and DDR-SDRAM at speeds of up to 133MHz, and can use 16, 32 or 64-bit bus widths. The interface can use 2 and 4 bank 16, 64, 128 or 256-Mbit devices in x4, x8, x16 and x32 packages, and can have 4 banks open simultaneously.

The EMI pads are dual mode pads electrically compatible with LVTTL (for standard SDRAM) and SSTL_2 (for DDR SDRAM).

5.5.2 Flash external memory interface (FEMI)

The flash external memory interface (FEMI) provides interfaces between the SuperHyway and external memory subsystem. These interfaces may include non-DRAM/SDRAM components such as flash memory, SRAM, or other external devices using communications protocols such as MPX.

This provides support for upto five independent memory areas. Each area can be specified to be 8, 16 or 32 bits, and may support conventional memory/devices using SRAM/ROM protocols, byte controlled SRAMS, flash memory devices or MPX companion chips.

The FEMI may act as either a bus master or slave, and when used with a companion chip allows access by external bus masters to SH-5 evaluation device core peripherals.

5.6 PCI interface

The SH-5 evaluation device integrates a fully featured PCI 2.1 bus bridge. The main features of the bridge are:

- Provision of a channel for a SuperHyway initiator to access PCI devices on the external PCI bus
- Provision of a channel for PCI devices to access the address space of SH-5, particularly the system memory through the EMI.
- Support for high-speed DMA-controlled transfer of data between the SuperHyway address space and PCI address space.
- Support for host and normal modes of operation on the PCI bus.

The PCI implementation supports 0 - 66 Mhz operation, PCI master and target functionals, revision 1.1 power management, upto 4 external masters, burst transfers, parity and error reporting, exclusive access, and external interrupts. The SH-5 evaluation device additionally supports hardware cache coherency when it is in host mode.

6 System organization

6.1 Introduction

This section discuses implementation specific aspects of the SH-5 evaluation device design.

6.2 Memory map

The SH-5 evaluation device implements a unified 32 bit physical address map. This is defined as follows in this implementation:

P-port acronym (or reserved)	Block type	Destination range	Physical address range	Physical address space
FEMI_db	DB	0x00 to 0x07	0x00000000-0x07FFFFFF	128 M
FEMI_cb	CB	0x08	0x08000000 - 0x08FFFFFF	16 M
PERIPHERAL_cb	CB	0x09 to 0x0A	0x09000000 - 0x0AFFFFFF	32 M
Debug_link	DB	0x0B	0x0B000000 - 0x0BFFFFFF	16 M
Debug_cb	CB	0x0C	0x0C000000 - 0x0CFFFFFF	16 M
CPU	CB	0x0D	0x0D000000 - 0x0DFFFFFF	16 M
DMAC	CB	0x0E	0x0E000000 - 0x0EFFFFFF	16 M
Reserved	UB	0x0F to 0x3F	0x0F000000 - 0x3FFFFFFF	784 M
PCI_db	DB	0x40-0x5F	0x40000000 - 0x5FFFFFFF	512M
PCI_cb	CB	0x60	0x60000000 - 0x60FFFFFF	16 M
Reserved	UB	0x61 to 0x6F	0x61000000 - 0x6FFFFFFF	240 M
SuperHyway socket	UB	0x70-0x7F	0x07000000 - 0x07FFFFFF	256M
EMI_DRAM	DB	0x80 to 0xFE	0x80000000 -0xFEFFFFFF	2032 M
EMI_cb	CB	0xFF	0xFF000000 - 0xFFFFFFFF	16 M

6.3 Interrupt mapping

The SH-5 evaluation device architecture supports upto 64 interrupt channels.

In this implementation they are allocated as follows:

Interrupt causes (in order of default precedence)		Interrupt number	INTEVT code	Interrupt priority	
				Reset value	
IRL0		0	0x240	0	Programmable
IRL1		1	0x2A0	0	
IRL2		2	0x300	0	
IRL3		3	0x360	0	
PCI	INTA	4	0x800	0	
	INTB	5	0x820	0	
	INTC	6	0x840	0	
	INTD	7	0x860	0	
Reserved		8-11	0x020-0x080	0	
PCI	SERR#	12	0xA00	0	
	ERR	13	0xA20	0	
	Pwr3	14	0xA40	0	
	Pwr2	15	0xA60	0	
	Pwr1	16	0xA80	0	
	Pwr0	17	0xAA0	0	

Interrupt causes (in order of default precedence)		Interrupt number	INTEVT code	Interrupt priority	
				Reset value	
DMAC	DMTE0	18	0x640	0	Programmable
	DMTE1	19	0x660		
	DMTE2	20	0x680		
	DMTE3	21	0x6A0		
	DAERR	22	0x6C0	0	
Reserved		23-31	0x0A0-0x1A0	0	
TMU	TUNI0	32	0x400	0	
	TUNI1	33	0x420	0	
	TUNI2	34	0x440	0	
	TICPI2	35	0x460		
RTC	ATI	36	0x480	0	
	PRI	37	0x4A0		
	CUI	38	0x4C0		
SCIF	ERI	39	0x700	0	
	RXI	40	0x720		
	BRI	41	0x740		
	TXI	42	0x760		
Reserved		43	0x1C0	0	
		44	0x1E0		
		45-62	0xC00-0xE20		
WDT	ITI	63	0x560	0	

6.4 DMA channel mapping

The DMAC architecture supports upto 16 resources, and allows each resource to be associated with a specific channel under software control. The device to resource mapping is as follows:

0 ⟹ Auto request
1 ⟹ Peripheral 0 transfer request
2 ⟹ Peripheral 1 transfer request
3 ⟹ Peripheral 2 transfer request
4 ⟹ Peripheral 3 transfer request
5 ⟹ TMU transfer request
6 ⟹ SCIF transmit transfer request
7 ⟹ SCIF receive transfer request

[8-15] Values reserved.

The mapping between the DMA channel number and resource is defied by the register **DMAC.CTRL[channel_number].resource_select**.

6.5 Clock

6.5.1 Structure

The structure of the clock generator is illustrated in *Table 3*.

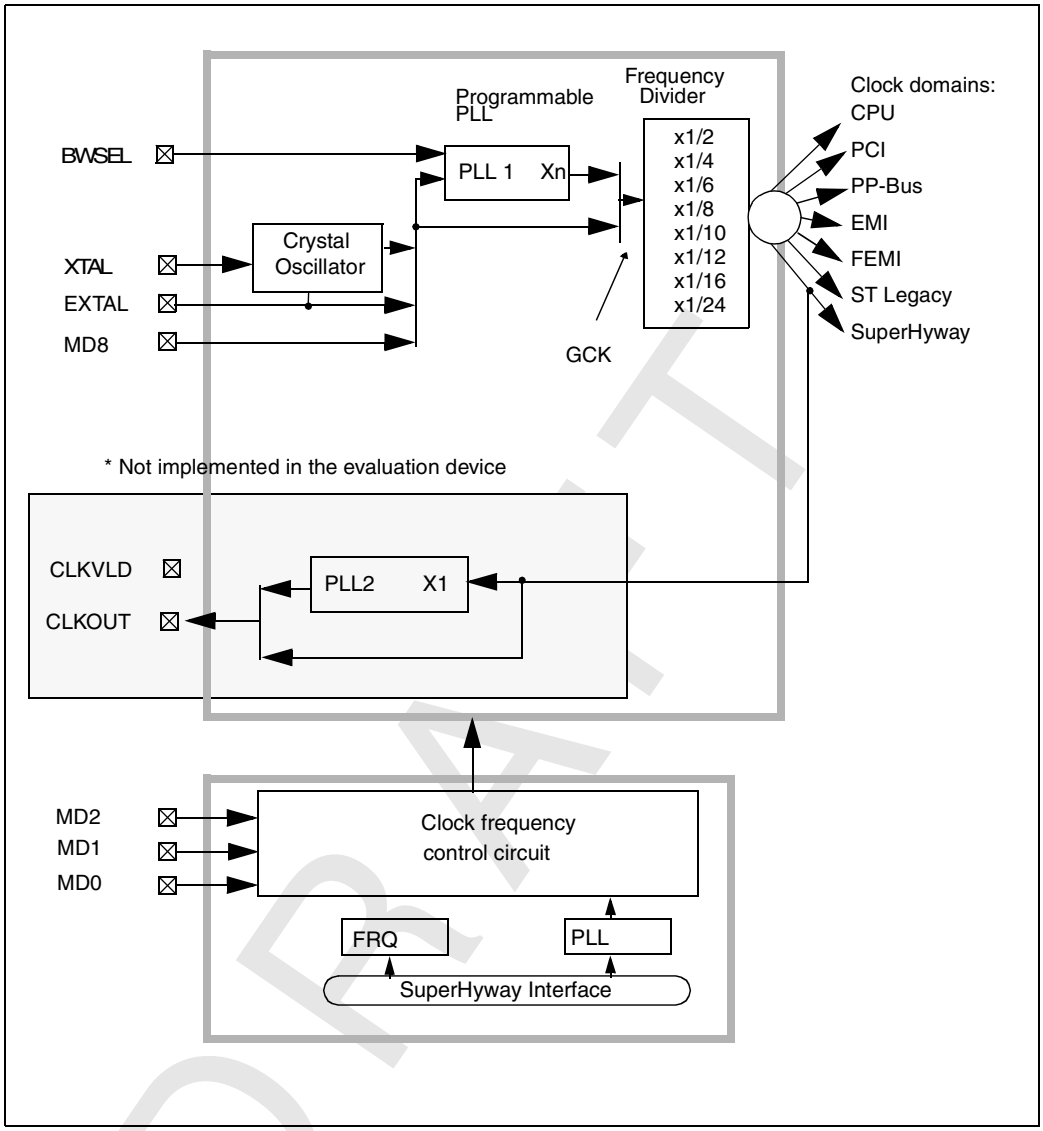


Figure 3: Clock generator

6.5.2 Operating mode at reset

Table 9 shows the clock operating modes corresponding to various combinations of mode control pin (MD2-MD0) settings. *Table 9 on page 28* shows CRPC.FRQ settings and internal clock frequencies[1].

Clock operating mode	External pin combination			PLL1	PLL2[a]	Frequency ratios			
	MD2	MD1	MD0			CPU clock	SuperHyway clock	EMI clock	Other clock domains
0	0	0	0	On	On	X1/2	X1/8	X1/16	slowest clock
1	0	0	1	On	On	X1/2	X1/12	X1/24	slowest clock
2	0	1	0	On	On	X1/2	X1/6	X1/12	slowest clock
3	0	1	1	On	On	X1/2	X1/4	X1/8	slowest clock
4	1	0	0	On	On	X1/2	X1/2	X1/4	slowest clock
5	1	0	1	Off	On	X1/2	X1/2	X1/4	slowest clock
6	1	1	0	Off	On	X1/2	X1/4	X1/8	slowest clock
7	1	1	1	Reserved					

Table 9: Clock operating modes

a. PLL2 is not implemented in the evaluation device.

6.6 EMI

The following EMI registers are implementation specific

Pin buffer strength register (PBS)

Define the buffer strength for each pin (to be defined).

EMI.PBS				0x(VCR.TOP_MB)000000 + 0x00000020	
Field	**Bits**	**Size**	**Volatile?**	**Synopsis**	**Type**
PBS	0	1	-	Pin Buffer Strength	RW
	Operation		0: output buffer strength is half 1: output buffer strength is full		
	When read		Returns current value		
	When written		Updates current value		
	HARD reset		0x00000000		

Table 10: Pin buffer strength register (PBS)

1. SH-5 will support a CPU clock domain frequency of 400MHz.

EMI.PBS				0x(VCR.TOP_MB)000000 + 0x00000020	
Field	**Bits**	**Size**	**Volatile?**	**Synopsis**	**Type**
—	[1-63]	32	-	Reserved	RES
	Operation		Software should always write 0 to these bits. Software should always ignore the value read from these bits.		

Table 10: Pin buffer strength register (PBS)

6.6.1 Clock offset control (COC)

The EMI.COC register controls and reports the status of the two DLLS in the EMI padlogic. DLL1 is used when driving SDRAM to control the phase relationship between the output clock and the internal clock used for sampling. DLL2 is used in DDR mode to provide the 1/4 and 3/4 cycle offset between DQS and DQ.

Caution: Configuration software should ensure that DLL1 and DLL2 are locked (by polling the COC register) following reset or a frequency change before attempting to use the EMI.

Note: It is not expected that this register will need to be written to by software. The manual override facility provided by this register is intended only for silicon validation purposes.

EMI.COC				0x(VCR.TOP_MB)000000 + 0x00000028	
Field	**Bits**	**Size**	**Volatile?**	**Synopsis**	**Type**
LOCK1	0	1	✓	DLL1 lock status	R
	Operation		Indicate whether DLL1 locks or not.		
	When read		Returns current value		
	When written		ignore		
	HARD reset		Undefined		
MOE1	1	1	Yes	Manual offset enable on DLL1	RW
	Operation		0: Normal operation 1: Delay value of DLL1 manually defined by DO1		
	When read		Returns current value		
	When written		Updates current value		
	HARD reset		0x0		

Table 11: Clock offset control register (COC)

EMI.COC				0x(VCR.TOP_MB)000000 + 0x00000028	
Field	**Bits**	**Size**	**Volatile?**	**Synopsis**	**Type**
DOC1	[2-10]	9	Yes	Delay offset value ofDLL1	RW
	Operation		Delay offset value set and read.		
	When read		Returns current DLL1 delay value		
	When written		When MOE1=1, written value is used as delay constant.		
	HARD reset		0x0		
LOCK	16	1	Yes	DLL2 lock status	R
	Operation		Indicate whether DLL2 locks or not.		
	When read		Returns current value		
	When written		Ignore		
	HARD reset		Undefined		
MOE2	17	1	Yes	Manual offset enable on DLL2	RW
	Operation		0: Normal operation 1: Delay value of DLL2 manually defined by DO2		
	When read		Returns current value		
	When written		Updates current value		
	HARD reset		0x0		
DO2	[18-26]	9	Yes	Delay offset value of DLL2	RW
	Operation		Delay offset value set and read.		
	When read		Returns current DLL2 delay value		
	When written		When MOE2=1, written value is used as delay constant.		
	HARD reset		0x0		
—	[11-15], [27-63]	42	No	Reserved	RES
	Operation		Software should always write 0 to these bits. Software should always ignore the value read from these bits.		
	When read		—		
	When written		—		
	HARD reset		—		

Table 11: Clock offset control register (COC)

6.7 Mode selection

During the power on reset cycle a range of basic system configurations can be setup by the use of resistive pull-ups or pull-downs. A detailed description of these selections can be found in the relevant chapters of the *SH-5 System Architecture Manual*.

Pin Name	Function	Default Setting	Meaning
MODE 0	Clock operating mode	1	Mode 3: 1/2:1/4:1/8 300:150:75 MHz CPU:BUS:EMI
MODE 1		1	
MODE 2		0	
MODE 3	Use/non-use of crystal	1	Use crystal resonator
MODE 4	Endianness	1	0: Big endian 1: Little endian
MODE 5	FEMI CS area merge	0	specify merge mode of area 1~4 into a single area 0: Non merge, 1: merge
MODE 6	FEMI CS0 bus type	0	specify memory type of area 0 0: Normal memory, 1: MPX
MODE 7	FEMI CS0 bus size	0	specify bus width of area 0 00: 8-bit, 01; 16-bit, 10; 32-bit, 11: Reserved
MODE 8		1	
BWSEL	PLL bandwidth select	0	Selects the PLL bandwidth according to - Crystal resonator frequency - BWSEL: 0 for a low frequency crystal - BWSEL: 1 for a high frequency crystal
PCICKSEL	PCI clock select	1	0: Internal PCI bridge move by internal clockd¦_ 1: Internal PCI bridge move by pciclk
HOSTEN	PCI host enable	1	0: Normal 1: Host bus bridge mode,

7 Electrical specification

Note: All of these readings were taken at T_a = 25 ^{o}Celsius.

7.1 DC characteristics

Item		Symbol	Min	Typ	Max	Unit	Test conditions
Power supply voltage		VCC, VCC-CPG, VCC-RTC	-	3.3	-	V	Normal mode, sleep mode, standby mode
		VCC-2.5	-	2.5	-		Normal mode, sleep mode, standby mode when using DDR-SDRAM
		VCC-2.5	-	3.3	-		Normal mode, sleep mode, standby mode when using SDRAM
		VDD-PLL, VDD-DLL, VDD	-	1.6	-		Normal mode, sleep mode, standby mode
Current dissipation	Normal operation use DDR-SDRAM	IDD	-	TBD	-	mA	VCC, VCC-CPG,VCC-RTC = 3.3v VDD,VDD-PLL,VDD-DLL = 1.5v VCC-2.5 = 2.5v
			-	TBD	-		
			-	TBD	-		
	Normal operation use SDRAM		-	TBD	-		VCC, VCC-CPG,VCC-RTC = 3.3v VDD,VDD-PLL,VDD-DLL = 1.5v VCC-2.5 = 3.3v
			-	TBD	-		
			-	TBD	-		
	Sleep mode use DDR-SDRAM		-	TBD	-		VCC, VCC-CPG,VCC-RTC = 3.3v VDD,VDD-PLL,VDD-DLL = 1.5v VCC-2.5 = 2.5v
			-	TBD	-		
			-	TBD	-		
	Sleep mode use SDRAM		-	TBD	-		VCC, VCC-CPG,VCC-RTC = 3.3v VDD,VDD-PLL,VDD-DLL = 1.5v VCC-2.5 = 3.3v
			-	TBD	-		
			-	TBD	-		
	Deep sleep mode use DDR-SDRAM		-	TBD	-	uA	VCC, VCC-CPG,VCC-RTC = 3.3v VDD,VDD-PLL,VDD-DLL = 1.5v VCC-2.5 = 2.5v
			-	TBD	-		
	Deep sleep mode use SDRAM		-	TBD	-		VCC, VCC-CPG,VCC-RTC = 3.3v VDD,VDD-PLL,VDD-DLL = 1.5v VCC-2.5 = 3.3v
			-	TBD	-		

Table 12: Absolute maximum ratings

Item		Symbol	Min	Typ	Max	Unit	Test conditions
Current dissipation	Normal operation use DDR-SDRAM	I_{DDQ}	-	TBD	-	mA	V_{CC}, V_{CC-CPG},V_{CC-RTC} = 3.3v V_{DD},V_{DD-PLL},V_{DD-DLL} = 1.5v $V_{CC-2.5}$ = 2.5v
			-	TBD	-		
			-	TBD	-		
	Normal operation use SDRAM		-	TBD	-		V_{CC}, V_{CC-CPG},V_{CC-RTC} = 3.3v V_{DD},V_{DD-PLL},V_{DD-DLL} = 1.5v $V_{CC-2.5}$ = 3.3v
			-	TBD	-		
			-	TBD	-		
	Sleep mode use DDR-SDRAM		-	TBD	-		V_{CC}, V_{CC-CPG},V_{CC-RTC} = 3.3v V_{DD},V_{DD-PLL},V_{DD-DLL} = 1.5v $V_{CC-2.5}$ = 2.5v
			-	TBD	-		
			-	TBD	-		
	Sleep mode use SDRAM		-	TBD	-		V_{CC}, V_{CC-CPG},V_{CC-RTC} = 3.3v V_{DD},V_{DD-PLL},V_{DD-DLL} = 1.5v $V_{CC-2.5}$ = 3.3v
			-	TBD	-		
			-	TBD	-		
	Deep sleep mode use DDR-SDRAM		-	TBD	-	uA	V_{CC}, V_{CC-CPG},V_{CC-RTC} = 3.3v V_{DD},V_{DD-PLL},V_{DD-DLL} = 1.5v $V_{CC-2.5}$ = 2.5v
			-	TBD	-		
	Deep sleep mode use SDRAM		-	TBD	-		V_{CC}, V_{CC-CPG},V_{CC-RTC} = 3.3v V_{DD},V_{DD-PLL},V_{DD-DLL} = 1.5v $V_{CC-2.5}$ = 3.3v
			-	TBD	-		

Table 12: Absolute maximum ratings

Item		Symbol	Min	Typ	Max	Unit	Test conditions
Input voltage	PRESET, MRESET, TRSTN, TMS, MODEn, PCICKSEL, HOSTEN, NMI	V_{IH}	V_{DDQ} X 0.9	-	V_{DDQ} + 0.3	V	
	PCI input pins		V_{DDQ} X 0.5	-	V_{DDQ} + 0.5	V	
	EMI input pins use DDR-SDRAM		V_{REF} + 0.15	-	$V_{DD\_2.5}$ + 0.30	V	
	EMI input pins use SDRAM		V_{DDQ} X 0.9	-	V_{DDQ} + 0.3	V	
	Other input pins		V_{DDQ} X 0.9	-	V_{DDQ} + 0.3	V	
	PRESET, MRESET, TRSTN, TMS, MODEn, PCICKSEL, HOSTEN, NMI	V_{IL}	-0.3	-	V_{DDQ} x 0.1	V	
	PCI input pins		-0.5	-	V_{DDQ} x 0.3	V	
	EMI input pins use DDR-SDRAM		-0.3	-	V_{REF} - 0.15	V	
	EMI input pins use SDRAM		-0.3	-	V_{DDQ} x 0.1	V	
	Other input pins		-0.3	-	V_{DDQ} x 0.2	V	
Output voltage	EMI output pins (DDR)	V_{OH}	$V_{CC\_2.5}$ - 0.43	-	-	V	
		V_{OL}	-	-	0.35	V	
	PCI output pins	V_{OH}	$V_{CC\_3.3}$ x 0.9	-	-	V	
		V_{OL}	-	-	$V_{CC\_3.3}$ x 0.1	V	
	Other output pins	V_{OH}	2.4	-	-	V	
		V_{OL}	-	-	0.55	V	
Pull-up resistance		R_{PULL}	20	60	180	kohm	
Pin capacitance		C_L	-	-	10	pF	

Table 12: Absolute maximum ratings

Item	Symbol	Min	Typ	Max	Unit
Permissible output low current (per pin) for SDRAM pins (DDR-SDRAM mode)	I_{OL}	-	-	16.8	mA
Permissible output low current (per pin) for SDRAM pins (SDRAM mode)		-	-	8.0	
Permissible output low current (per pin) for PCI pins		-	-	16.0	
Permissible output low current (per pin) for the output pins		-	-	2.0	
Permissible output low current (total pin)	ZI_{OL}	-	-	TBD	
Permissible output low current (per pin) for SDRAM pins (DDR-SDRAM mode)	$-I_{OH}$	-	-	16.8	
Permissible output low current (per pin) for SDRAM pins (SDRAM mode)		-	-	8.0	
Permissible output low current (per pin) for PCI pins		-	-	16.0	
Permissible output low current (per pin) for other output pins		-	-	2.0	
Permissible output low current (total pin)	$Z -I_{OH}$	-	-	TBD	

Table 13: Permissible output currents

7.2 AC characteristics

Item	Symbol	Typ	Unit	Note
Input reference voltage	VREF	1.25	V	
Termination voltage	VTT	1.25	V	1
High level ac input voltage	VIH(AC)	VREF + 0.31	V	
Low level ac input voltage	VIL(AC)	VREF - 0.31	V	

Table 14: Test conditions for DDR-SDRAM mode

Output waveform timing is measured where the output signal crossed through the VTT level

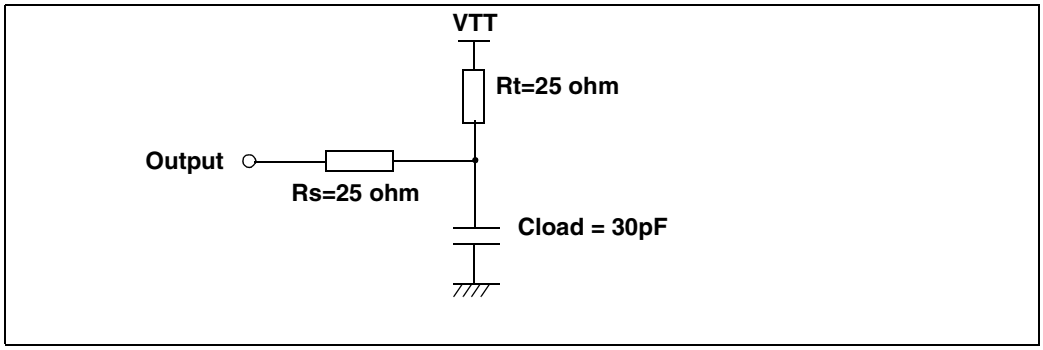


Figure 4: Test circuit for DDR-SDRAM mode

7.2.1 Clock and control signal timing

Item		Symbol	Min	Typ	Max	Unit
Operating Frequency	CPU, FPU, cache, TLB	f	160	-	320	MHz
	SHwy		1	-	160	
	PP-BUS modules		1	-	33	
	EMI(SDRAM)		60		80	
	EMI(DDR-SDRAM)		60	-	72	
	PCI		1		66	
	FEMI		1	-	60	

Table 15: Clock frequency

Item	Symbol	Min	Max	Unit	Notes
Clock cycle time	t_{CK}	12.5	16.7	ns	
Clock high-level width	t_{CH}	0.45	0.65	t_{CK}	
Clock low-level width	t_{CL}	0.45	0.65	t_{CK}	
Memory Address delay time	t_{MAD}	-	t_{CK} / 2 + 3	ns	
$\overline{MCS}$ delay time	t_{MCSD}	-	t_{CK} / 2 + 3	ns	
$\overline{MWE}$ delay time	t_{MWED}	-	t_{CK} / 2 + 3	ns	
$\overline{RAS}$ delay time	t_{RASD}	-	t_{CK} / 2 + 3	ns	
$\overline{CAS}$ delay time	t_{CASD}	-	t_{CK} / 2 + 3	ns	
$\overline{DQM}$ delay time	t_{DQMD}	-	t_{CK} / 2 + 3	ns	For normal SDRAM
$\overline{DQM}$ delay time	t_{DQMD}	-	t_{CK} * 3/4 + 2.5	ns	For DDR-SDRAM
Read MD setup time	t_{MSRDS}	2.5	-	ns	For normal SDRAM
Read MD hold time	t_{MSRDH}	1.5	-	ns	For normal SDRAM
Write access data Hi-z to drive delay time	t_{MAC}	-	t_{CK} / 2 + 3.8	ns	

Table 16: EMI bus timing

Item	Symbol	Min	Max	Unit	Notes
Write data delay time	tMWDD	-	tCK / 2 + 2.5	ns	For normal SDRAM
Write data delay time	tMWDD	-	tCK / 4 + 2.5	ns	For DDR-SDRAM
$\overline{DQS}$ output access time from MCLK, MCLK_N	tDQSCK	-0.75	0.75	ns	For DDR-SDRAM
$\overline{DQS}$ to MD skew	tDQSQ	-	0.7	ns	
MD input hold time from $\overline{DQS}$ (posedge)	tMDH	tCH -1.0	-	ns	For DDR-SDRAM
MD input hold time from $\overline{DQS}$ (negedge)	tMDH	tCL -1.0	-	ns	For DDR-SDRAM

Table 16: EMI bus timing

7.2.2 SDRAM interface timing

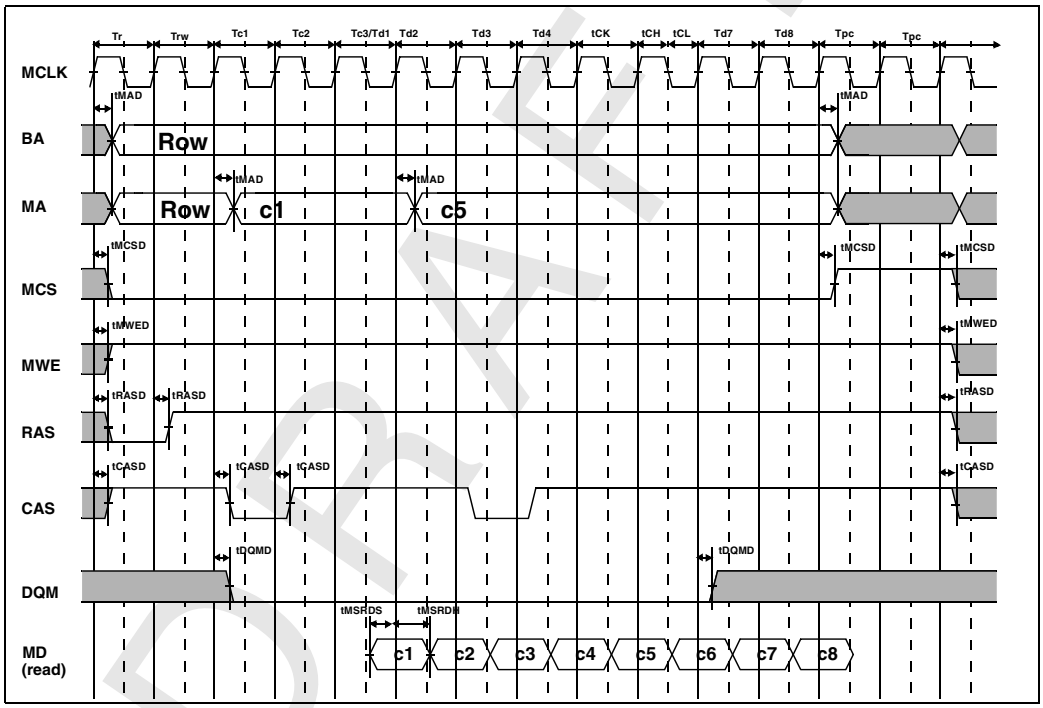


Figure 5: SDRAM read bus cycle: burst (RCD =1, CAS latency=2, TPC=2, DIMM=0)

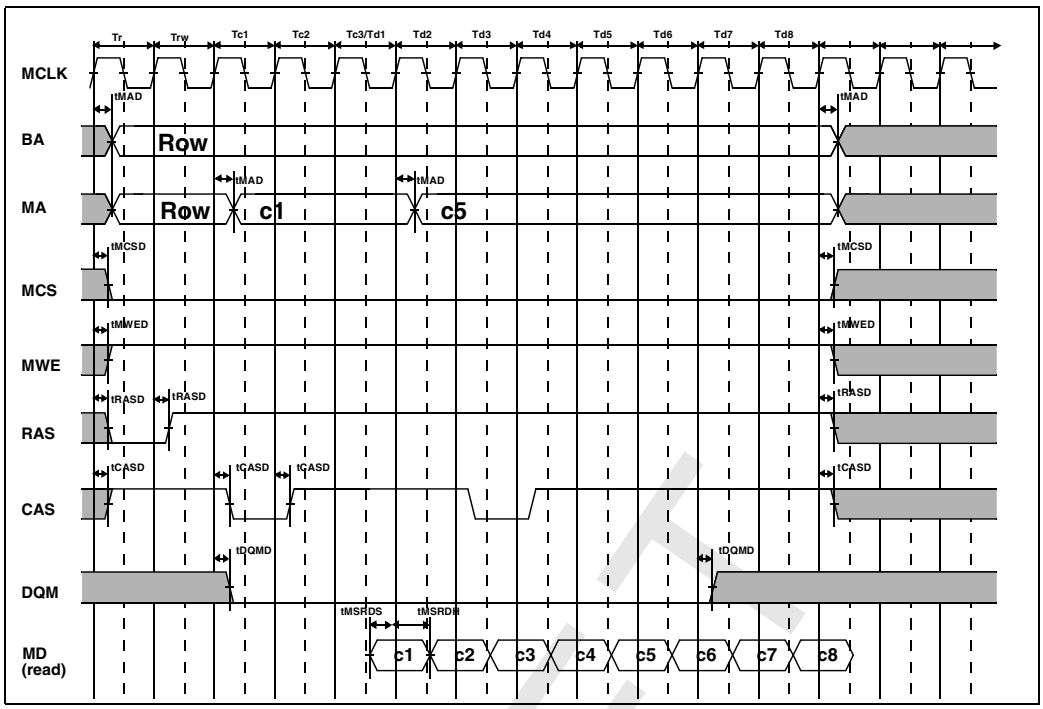


Figure 6: SDRAM normal read bus cycle: ACT+READ, burst (RCD =1, CAS latency=2, DIMM=0)

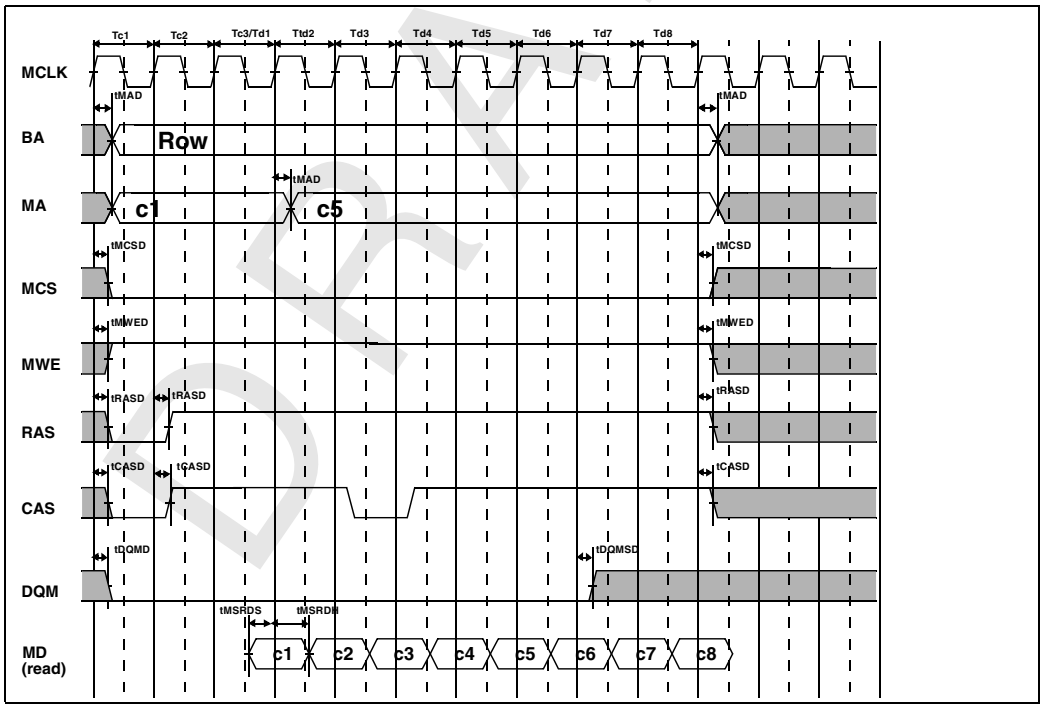


Figure 7: SDRAM normal read bus cycle: READ, burst (CAS latency=2, DIMM=0)

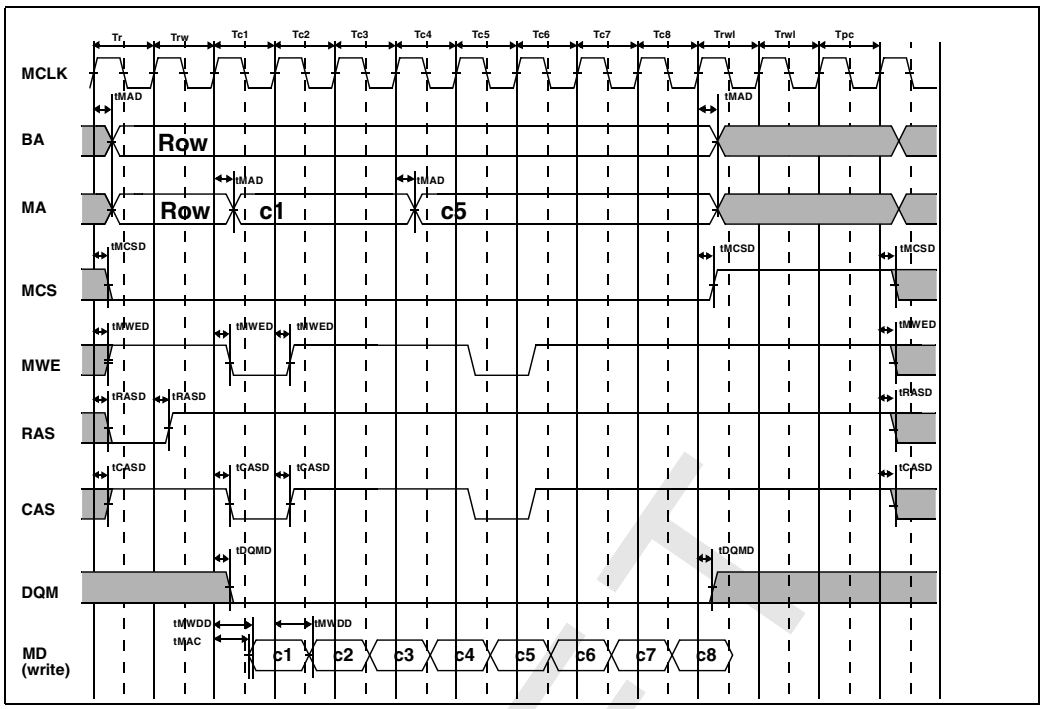


Figure 8: SDRAM write bus cycle: burst (RCD =1, TRWL=2, TPC=1, DIMM=0)

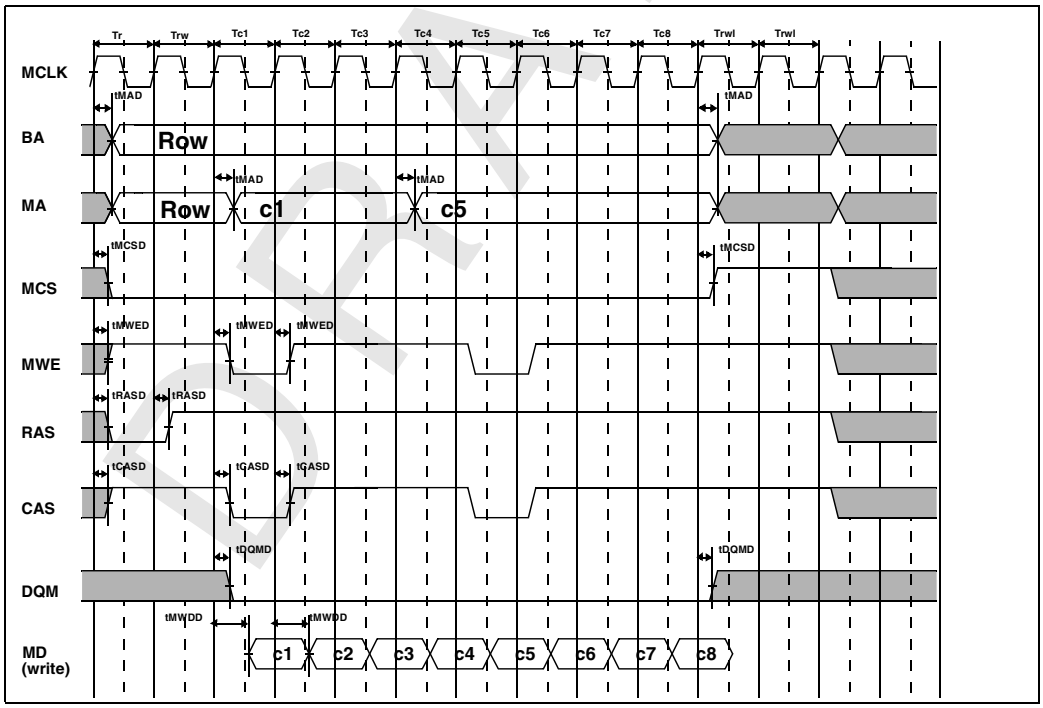


Figure 9: SDRAM normal write bus cycle: burst, ACT+WRITE (RCD =1, TRWL=2, DIMM=0)

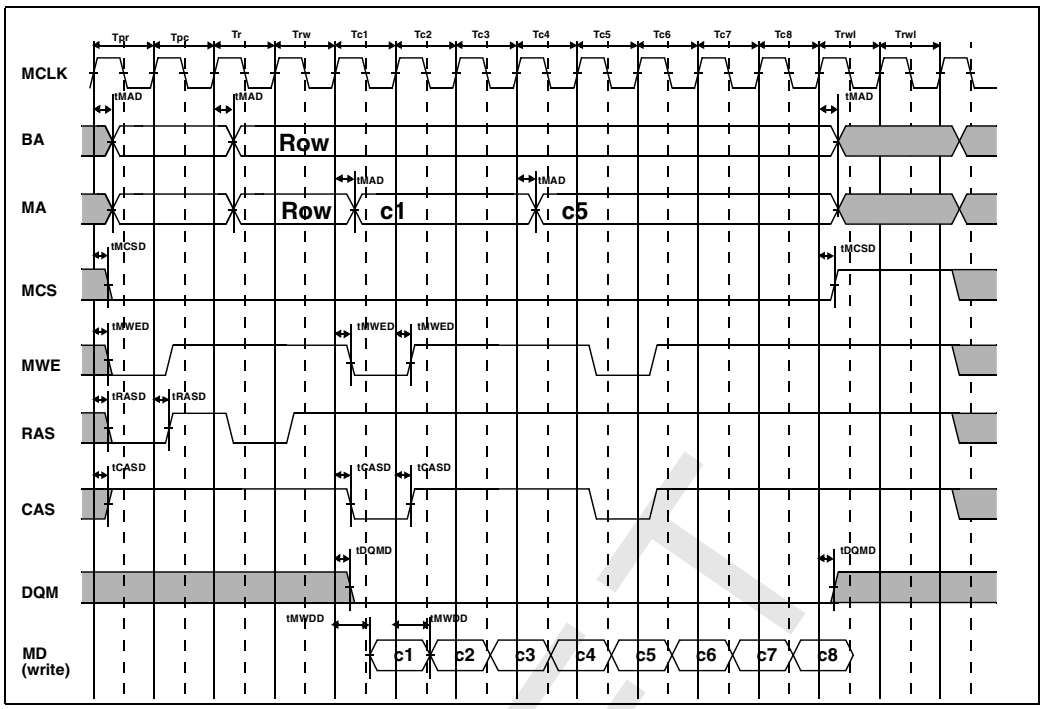


Figure 10: SDRAM normal write bus cycle: burst, PRE+ACT+WRITE (RCD =1, TCD=1, TRWL=2, DIMM=0)

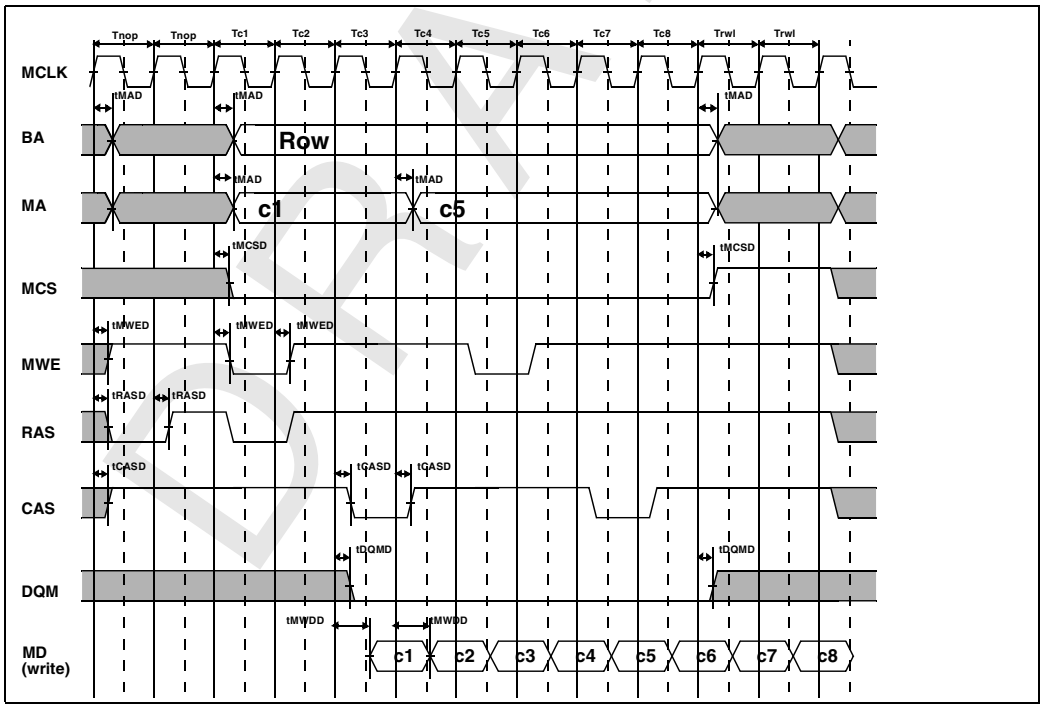


Figure 11: SDRAM normal write bus cycle: burst, WRITE (TRWL=2,DIMM=0)

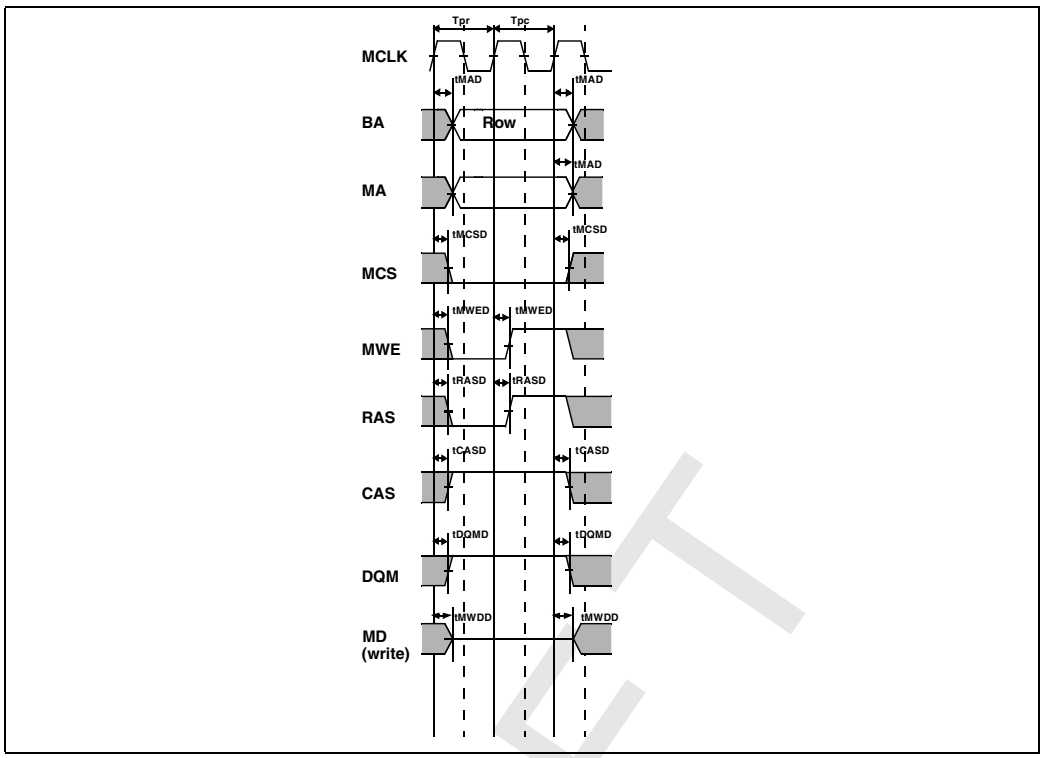


Figure 12: SDRAM precharge cycle: precharge (TPC=1)

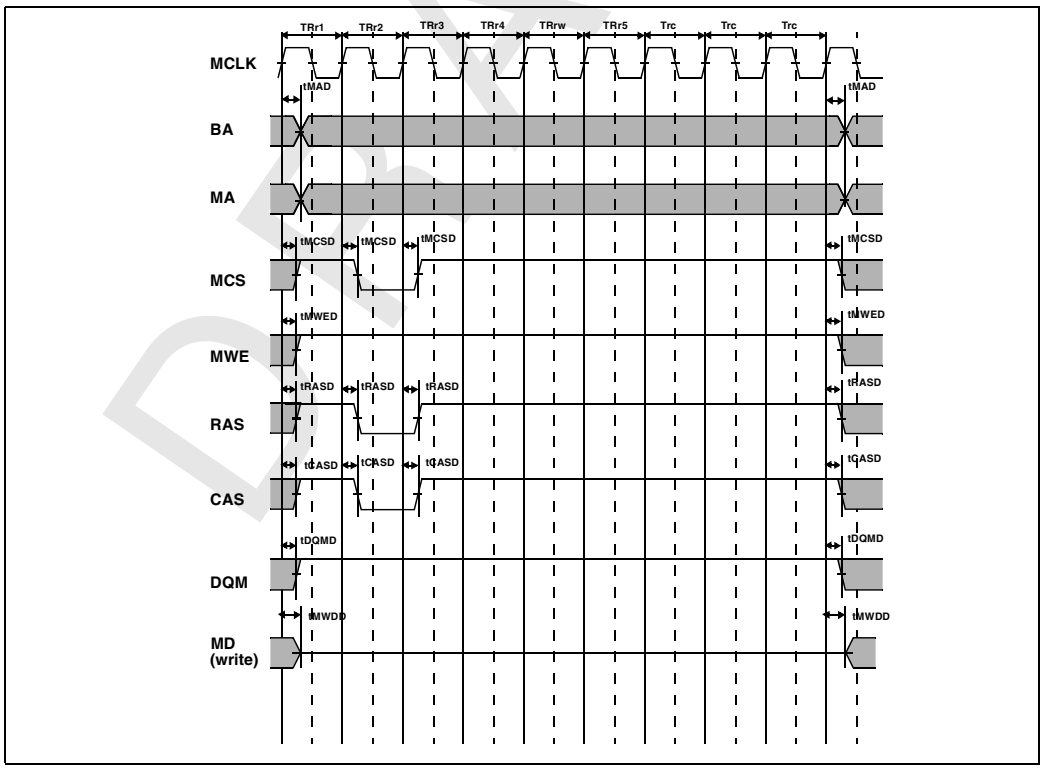


Figure 13: SDRAM auto refresh (TRAS=1, TRC=1)

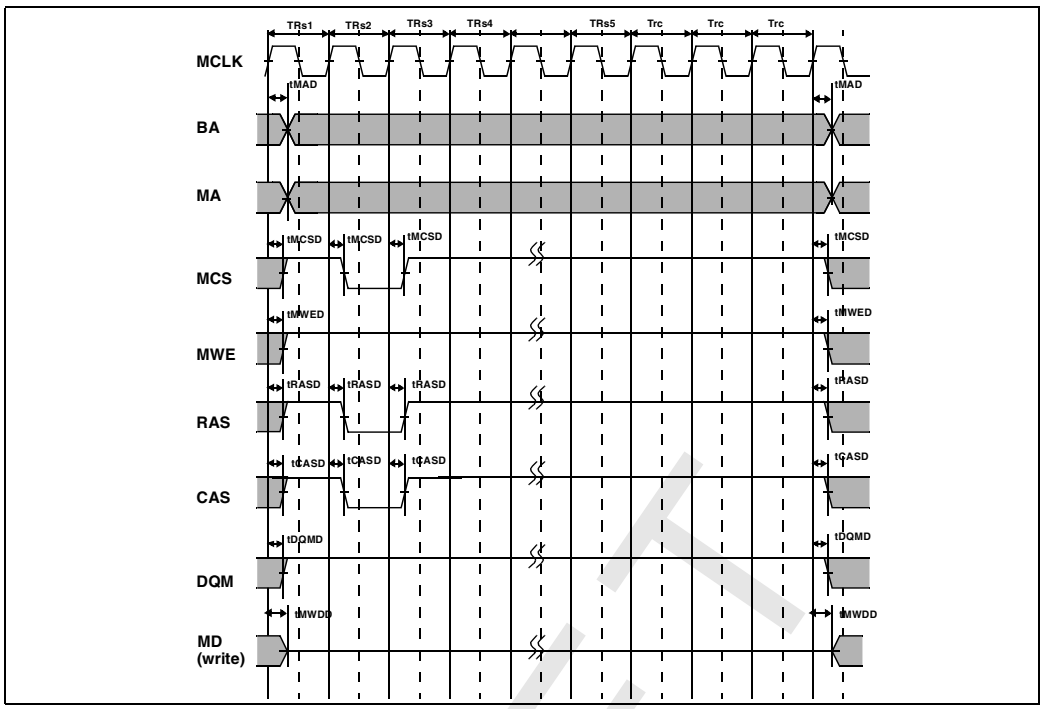


Figure 14: SDRAM self refresh (TRC=1)

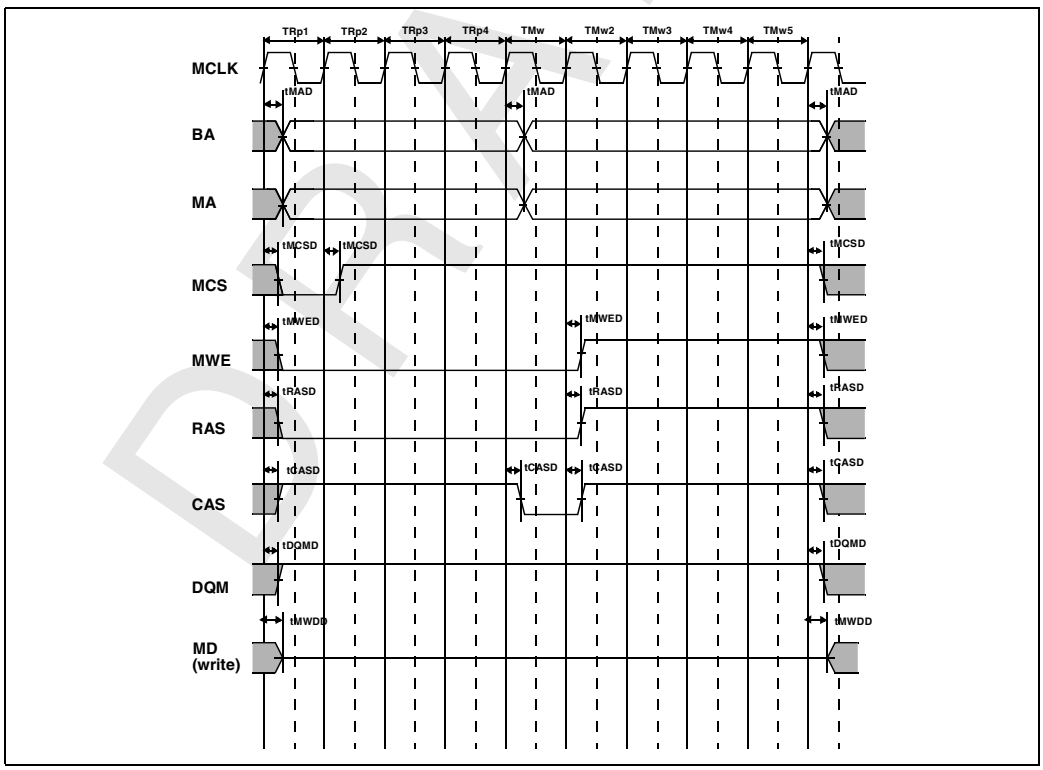


Figure 15: SDRAM mode register set (PALL)

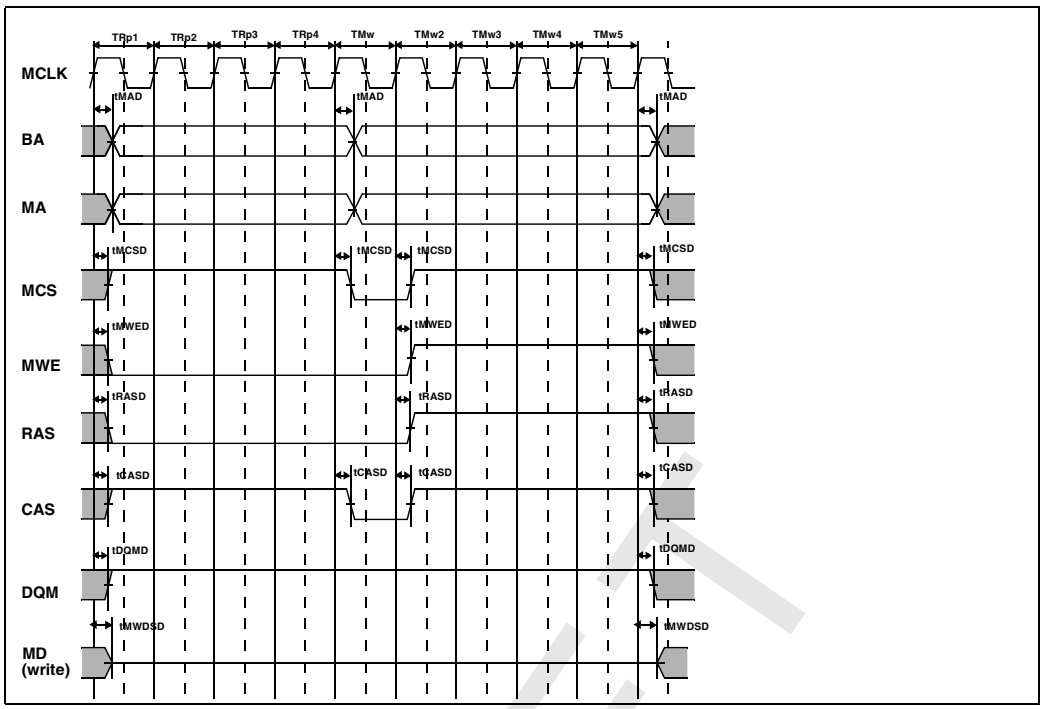


Figure 16: SDRAM mode register set (SET)

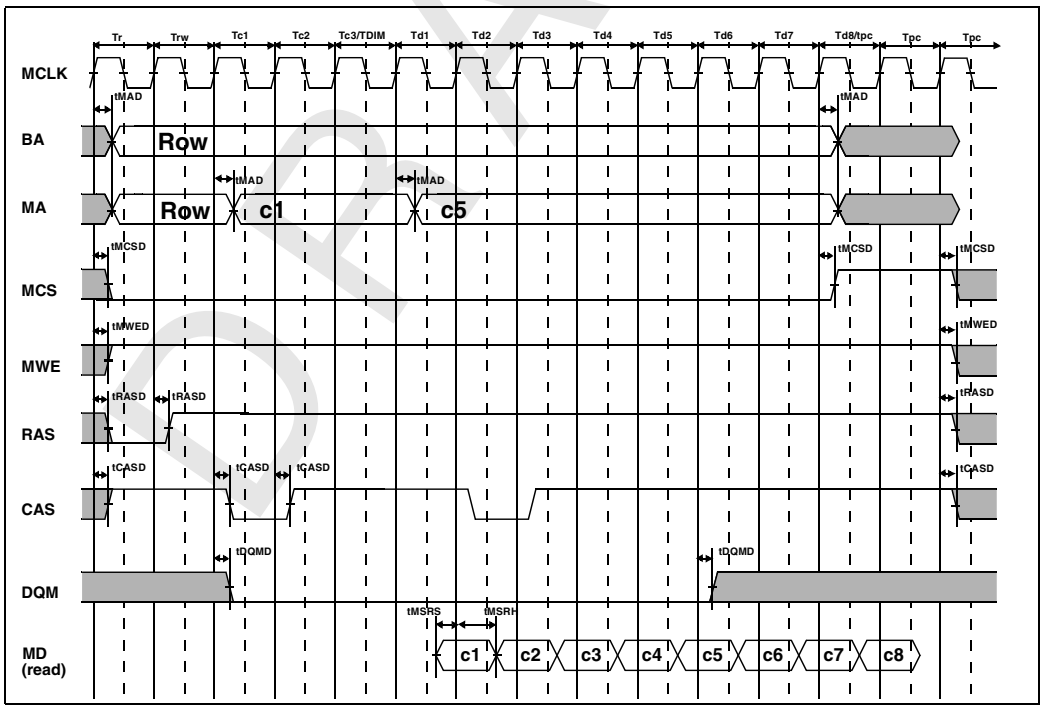


Figure 17: SDRAM read bus cycle: burst (RCD =1, CAS latency=2, TPC=2, DIMM=1)

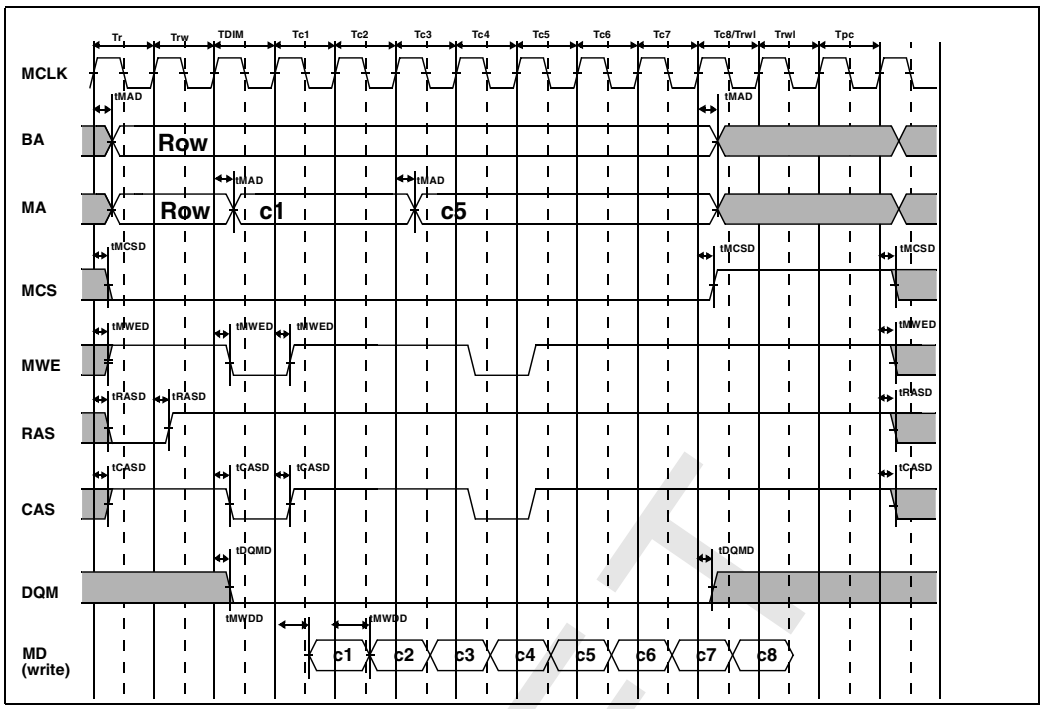


Figure 18: SDRAM write bus cycle: burst (RCD =1, TRWL=2, TPC=1, DIMM=1)

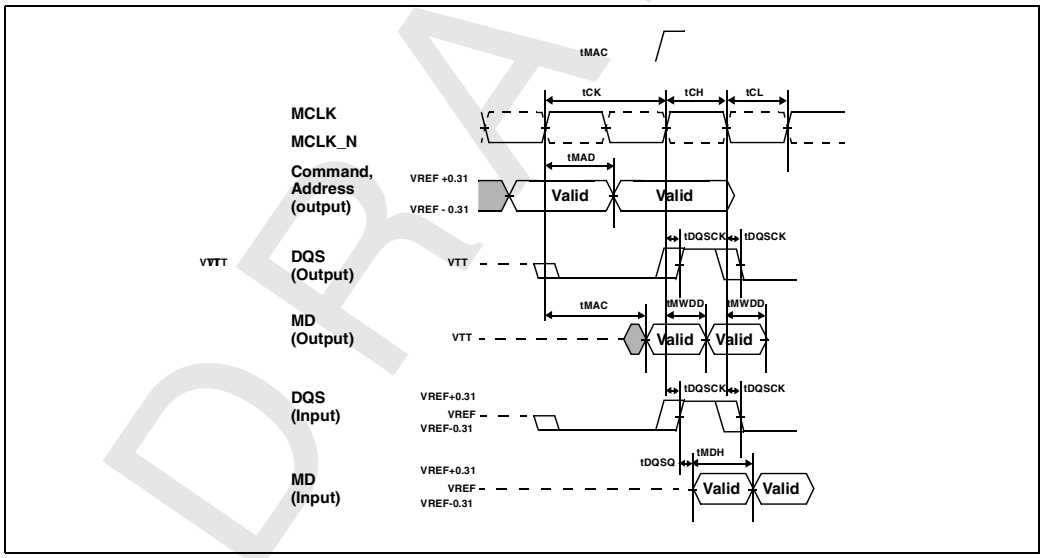


Figure 19: DDR-SDRAM basic timing

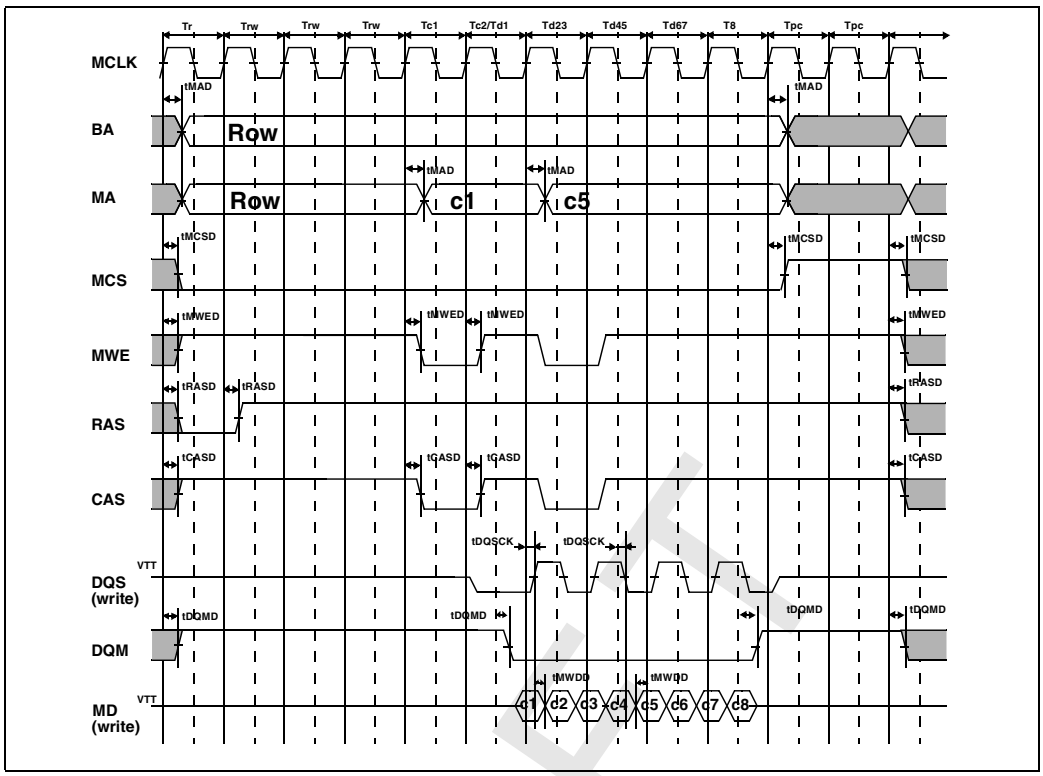


Figure 20: DDR-SDRAM write bus cycle: burst (RCD =3, CAS latency=2, TPC=2, DIMM=0)

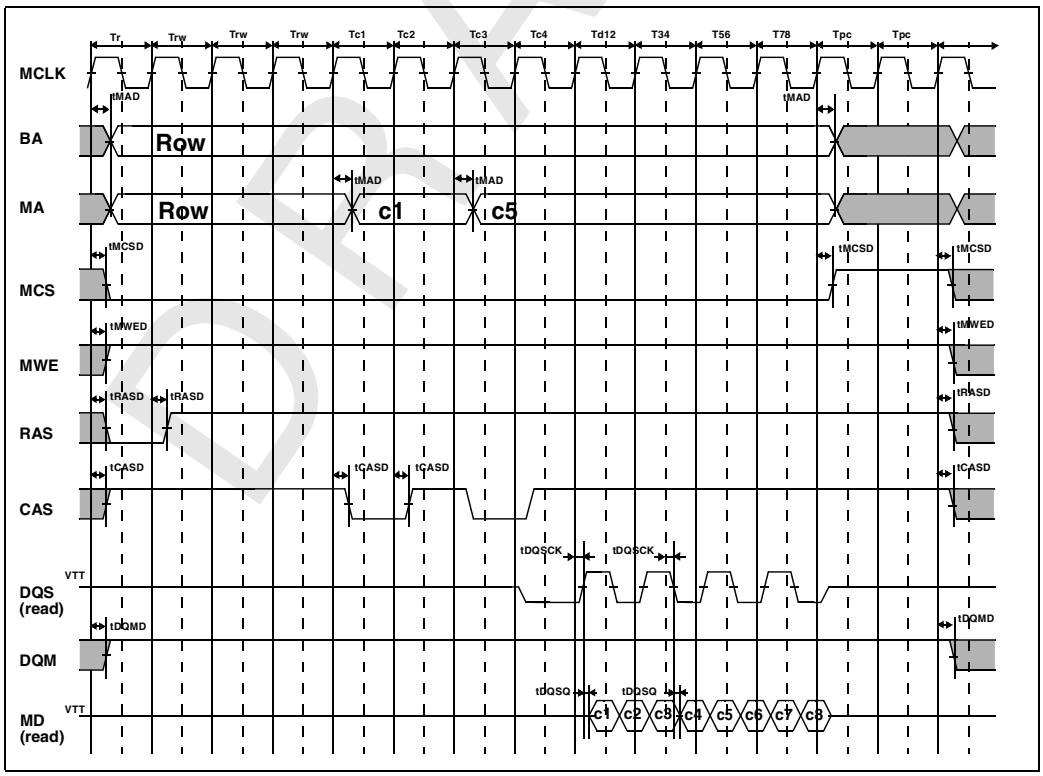


Figure 21: DDR-SDRAM read bus cycle: burst (RCD =3, CAS latency=2, TPC=2, DIMM=1)

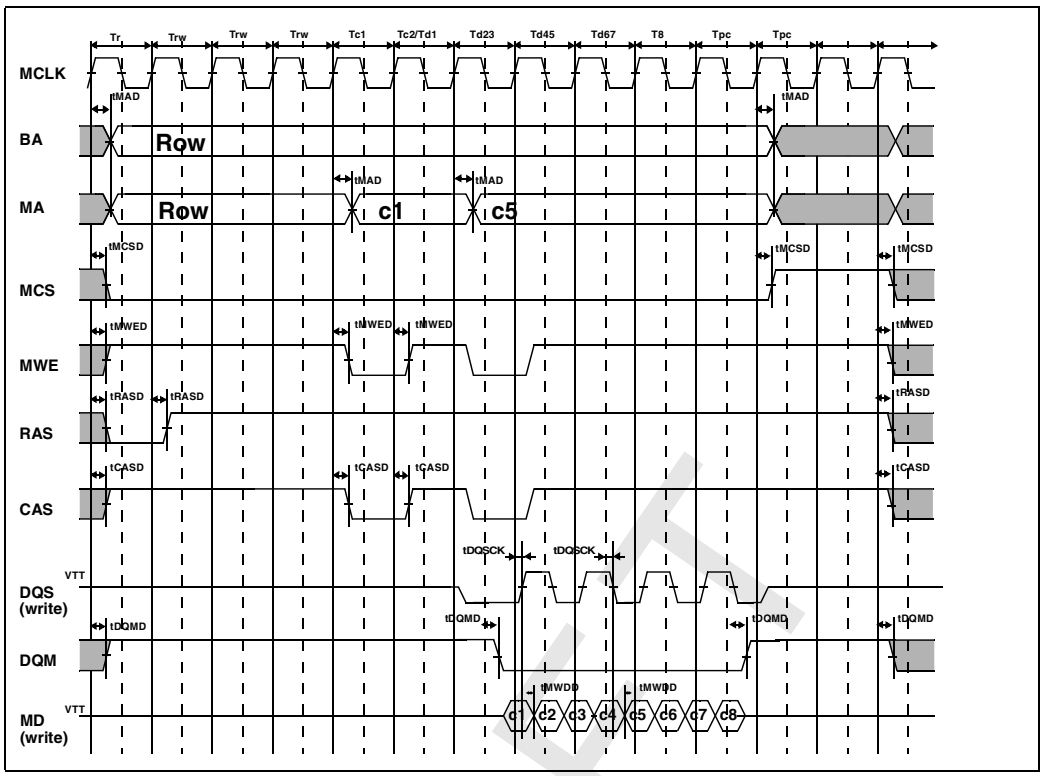


Figure 22: DDR-SDRAM write bus cycle: burst (RCD =3, CAS latency=2, TPC=2, DIMM=1)

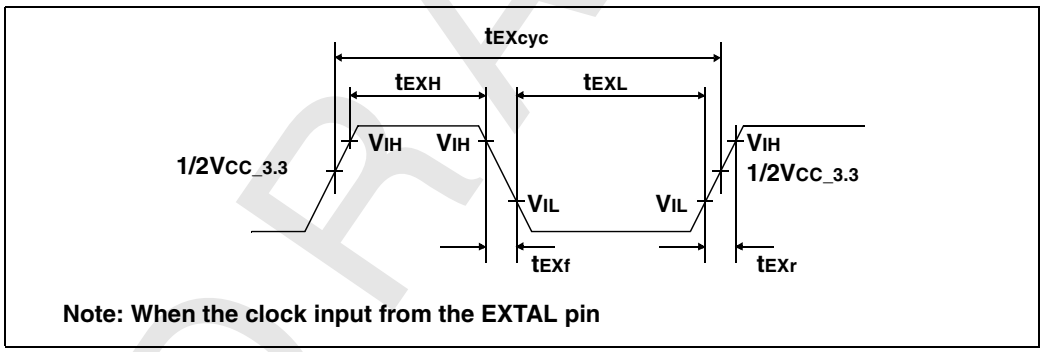


Figure 23: EXTAL clock input timing

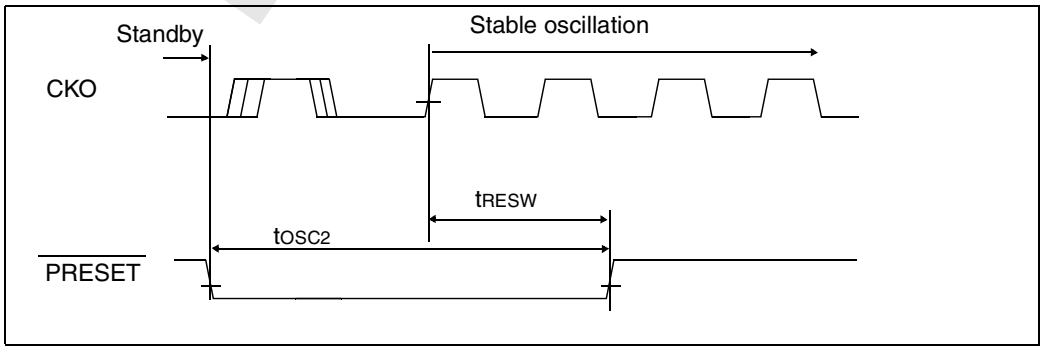


Figure 24: Standby return oscillation setting time (return by PRESET)

7.2.3 SRAM interface timing

Item	Symbol	Min	Max	Unit	Notes
Address delay time	t_{AD}	-	8.0	ns	
$\overline{BS}$ delay time	t_{BSD}	-	8.0	ns	
$\overline{CS}$ delay time	t_{CSD}	-	8.0	ns	
RDWR delay time	t_{RWD}	-	8.0	ns	
$\overline{RDFRM}$ delay time	t_{RSD}	-	8.0	ns	
Read data setup time	t_{RDS}	9.0	-	ns	
Read data hold time	t_{RDH}	1.0	-	ns	
$\overline{WE}$ delay time(falling edge)	t_{WEDF}	-	8.0	ns	
$\overline{WE}$ delay time	t_{WED1}	-	9.0	ns	
Write data delay time	t_{WDD}	-	10.0	ns	
$\overline{RDY}$ setup time	t_{RDYS}	9.0	-	ns	
$\overline{RDY}$ hold time	t_{RDYH}	1.0	-	ns	
CMD delay time	t_{CMDD}	-	8.0	ns	
DACK delay time	t_{DACD}	-	8.0	ns	

Table 17: Bus timing

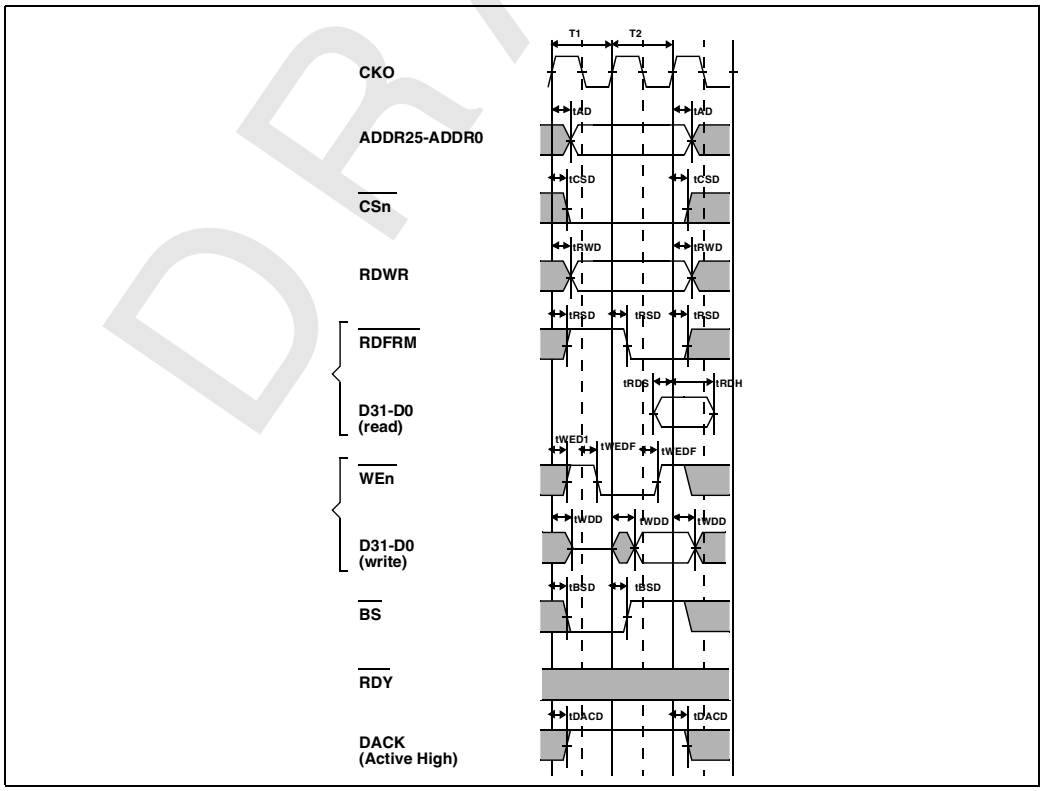


Figure 25: SRAM bus cycle: basic bus cycle (no wait)

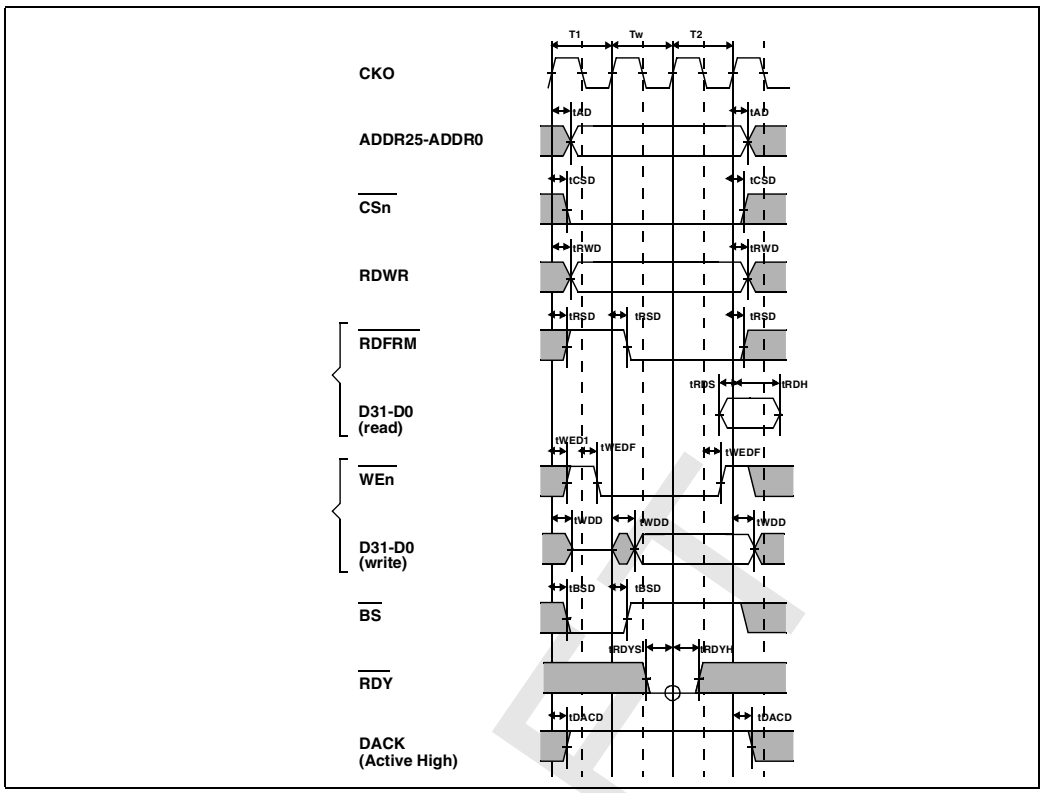


Figure 26: SRAM bus cycle: basic bus cycle (one internal wait)

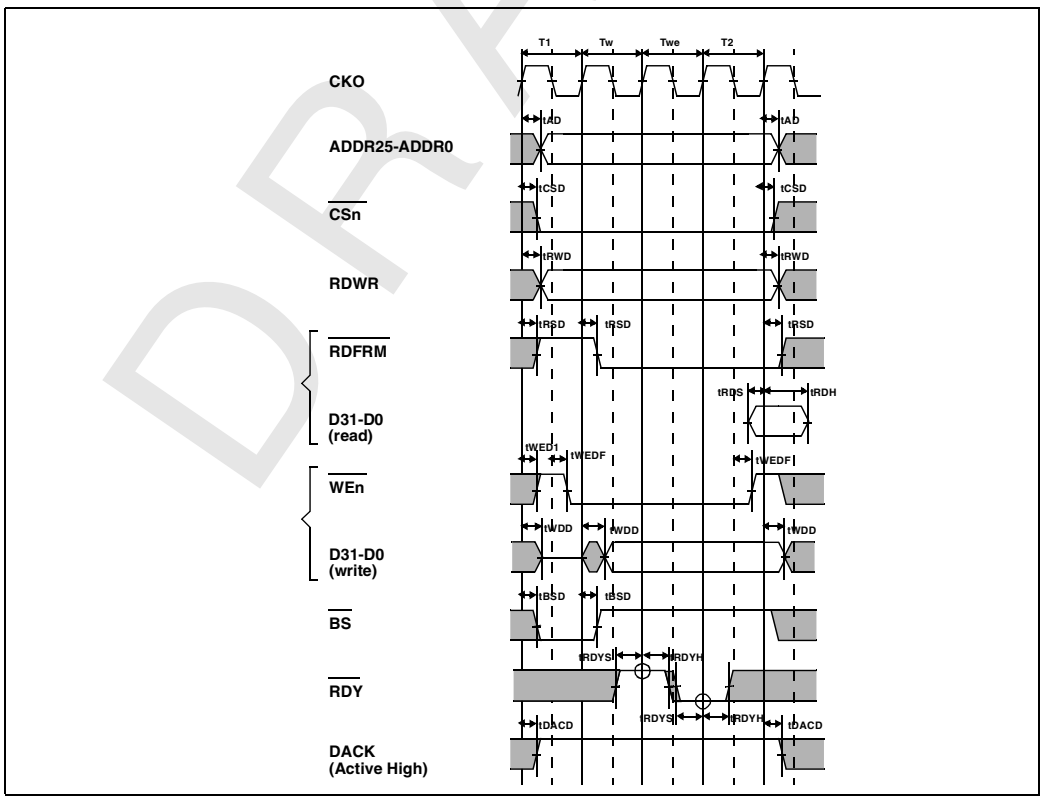


Figure 27: SRAM bus cycle: basic bus cycle (one internal wait + one external wait)

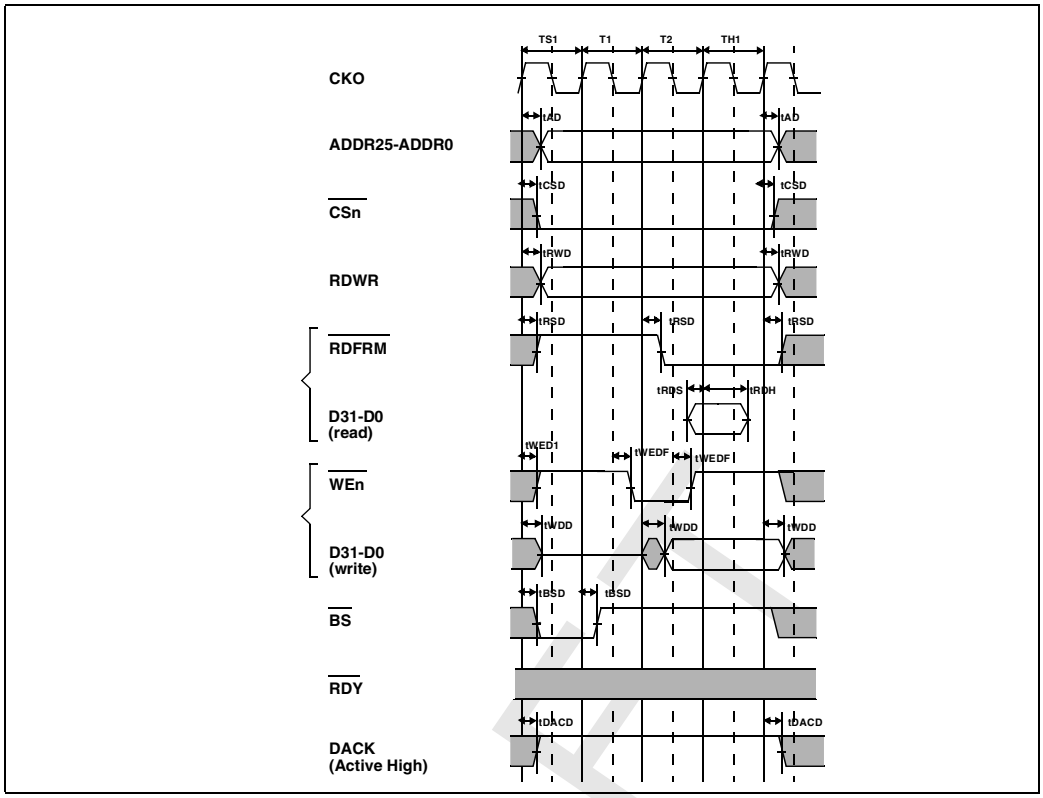


Figure 28: SRAM bus cycle: basic bus cycle (no wait + address setup/hold time insertion)

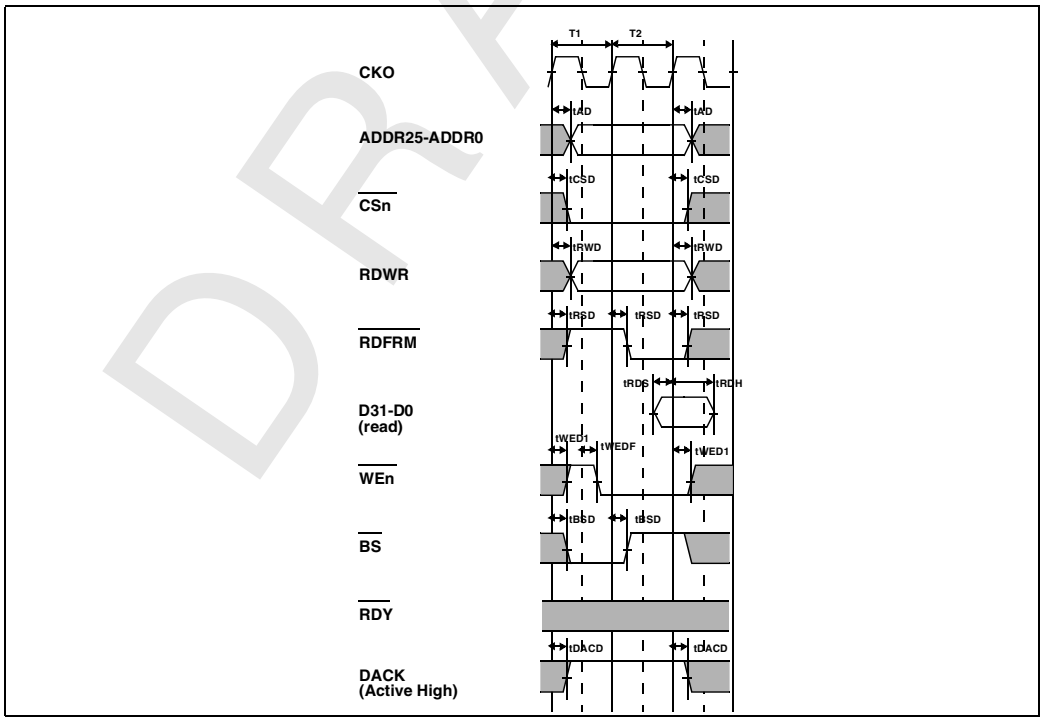


Figure 29: Byte control SRAM bus cycle: basic bus cycle (no wait)

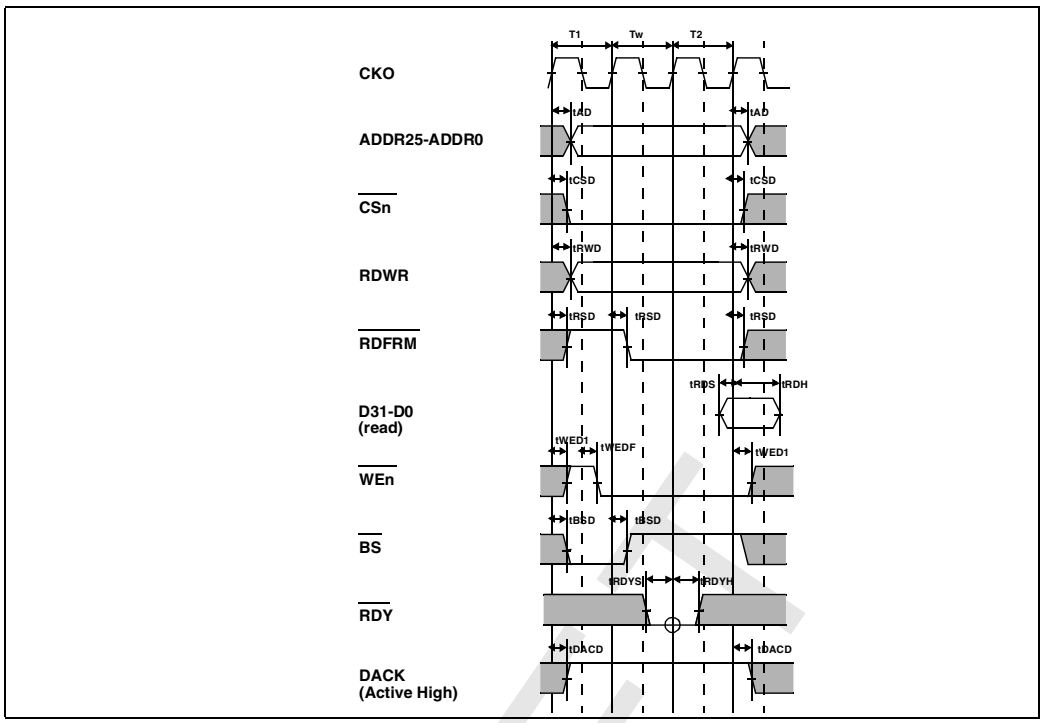


Figure 30: Byte control SRAM bus cycle: basic bus cycle (one internal wait)

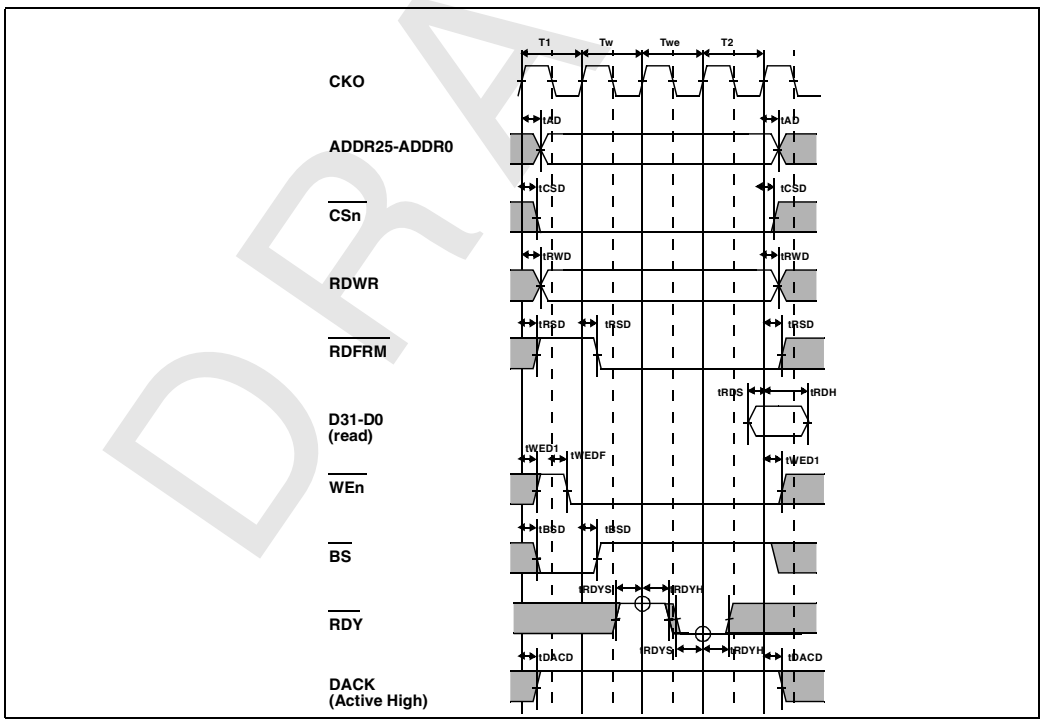


Figure 31: Byte control SRAM bus cycle: basic bus cycle (one internal wait + one external wait)

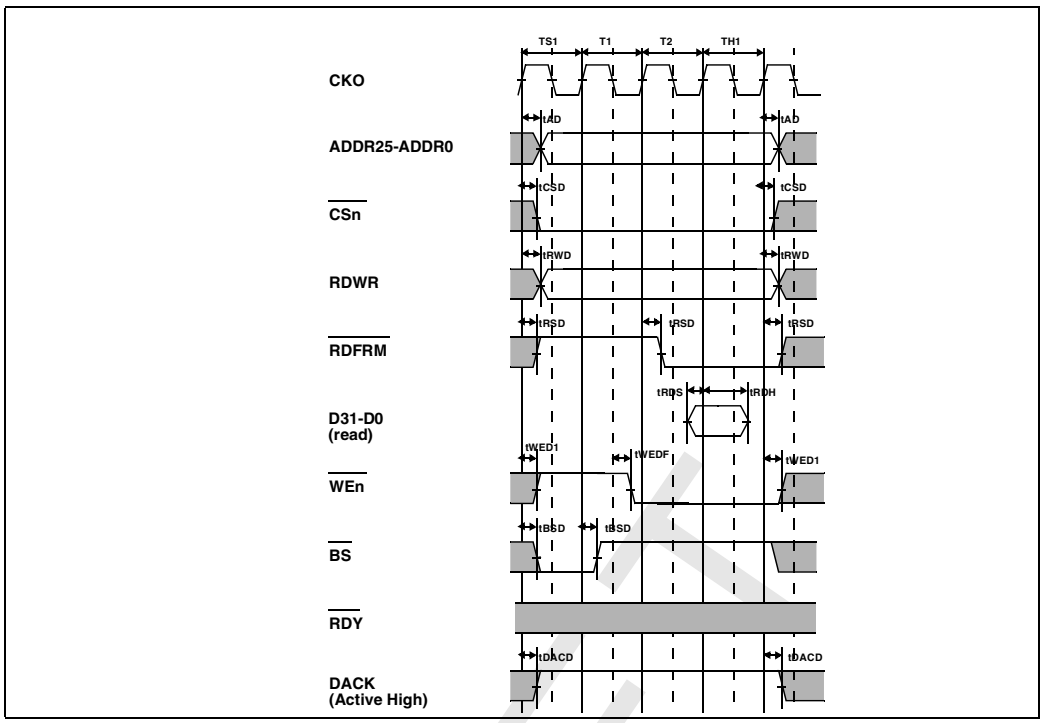


Figure 32: Byte control SRAM bus cycle: basic bus cycle (no wait + address setup/hold time insertion)

7.2.4 Flash memory interface timing

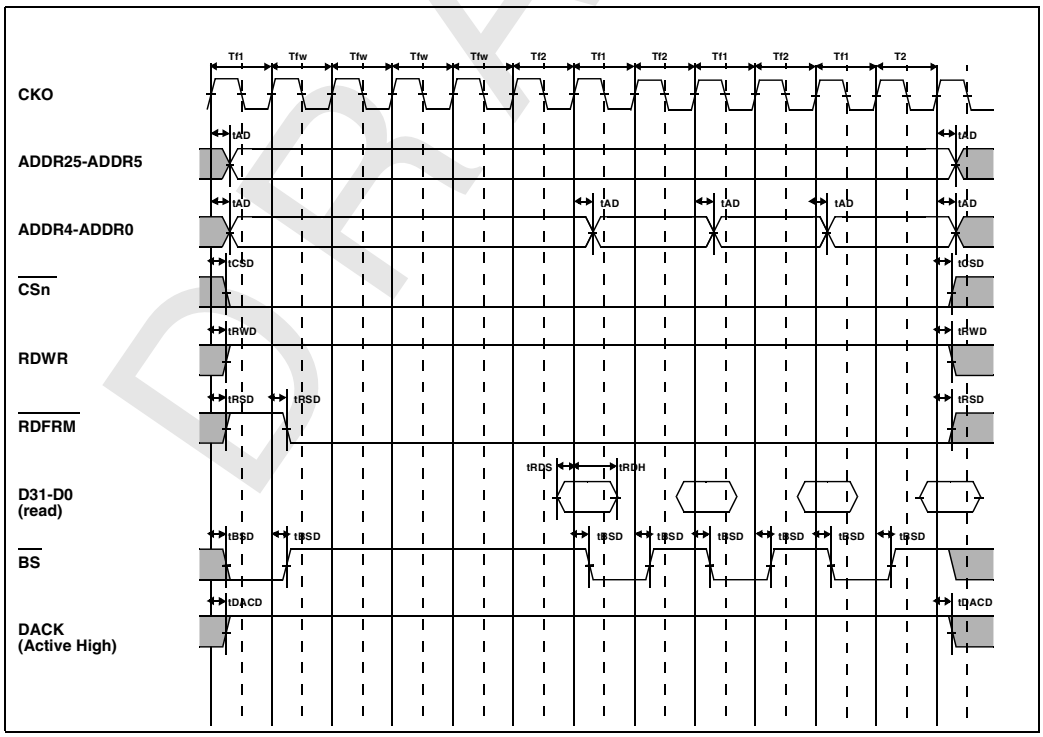


Figure 33: Flash memory bus cycle: asynchronous 16-byte read cycle (sz=32-bit, bst=4 burst, flmd=asynchronous, bp= 2 pitch, ws=4 wait, hld=hold wait 0, setup=setup wait 0)

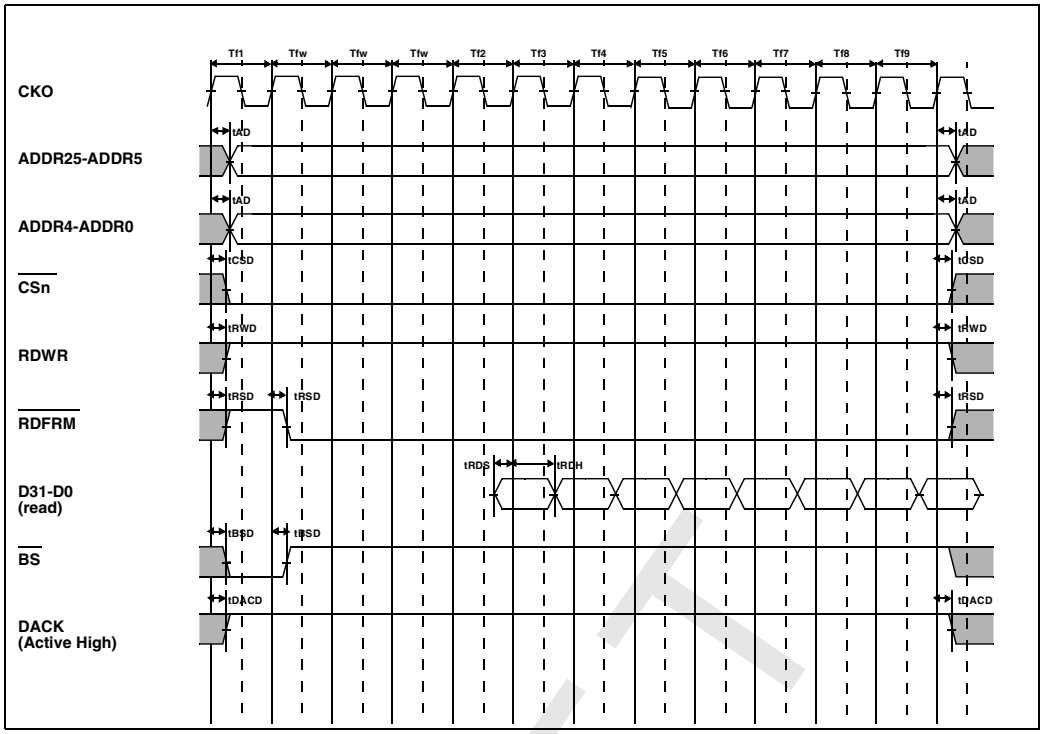


Figure 34: Flash memory bus cycle: synchronous 32-byte read cycle(sz=32-bit, bst=8 burst, flmd=synchronous, ws=3 wait, hld=hold wait 0, setup=setup wait 0)

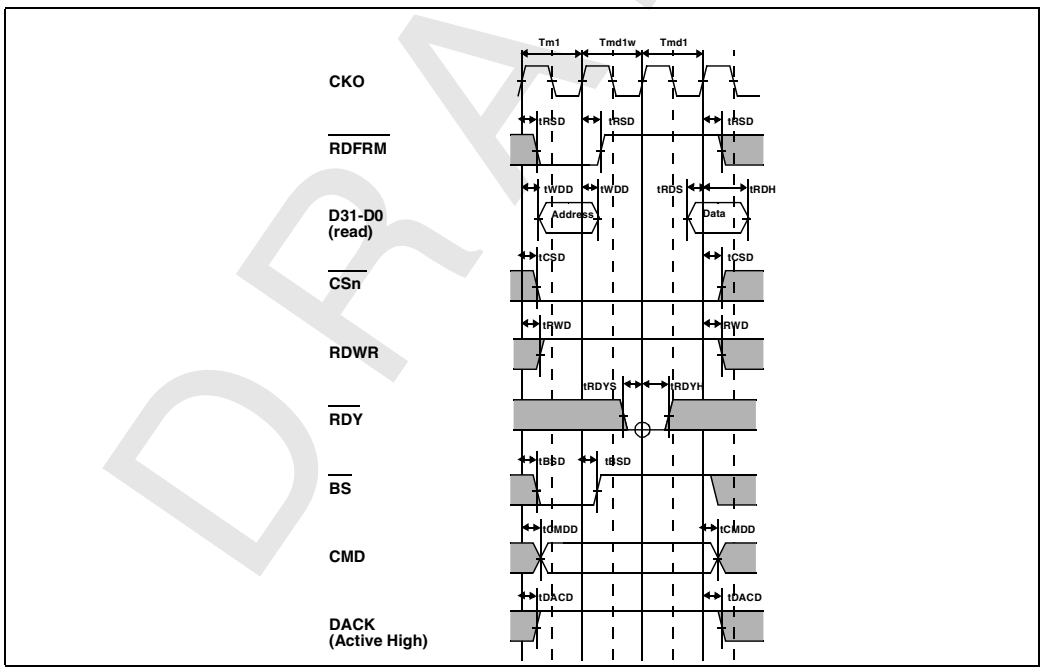


Figure 35: MPX bus cycle: basic read bus cycle (0 or 1 internal wait time insertion)

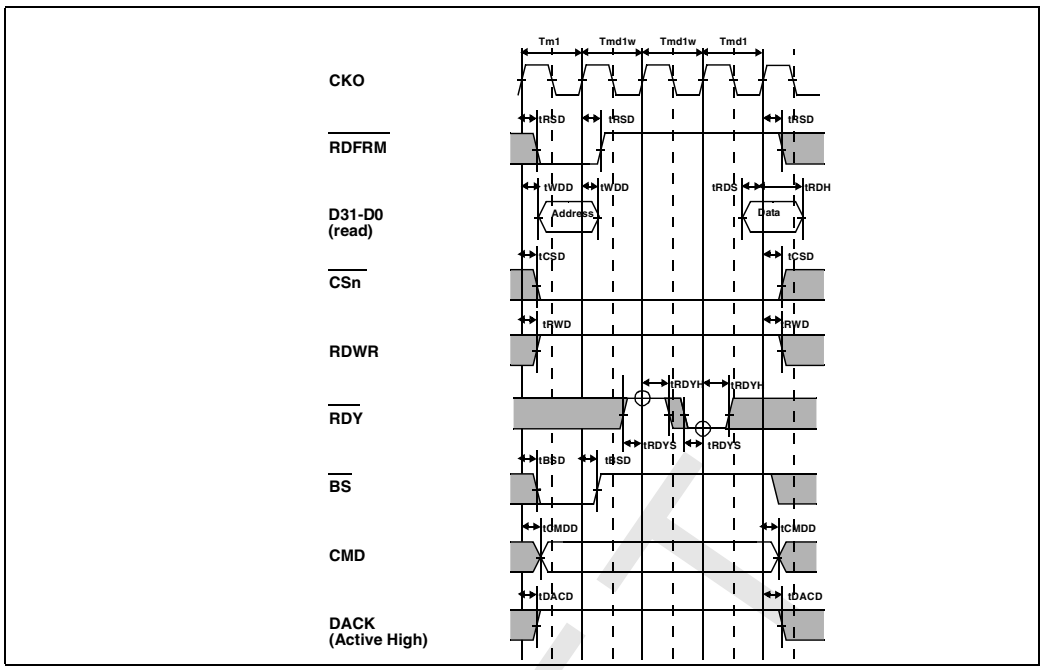


Figure 36: MPX bus cycle: basic read bus cycle (0 or 1 internal wait + 1 external wait time insertion)

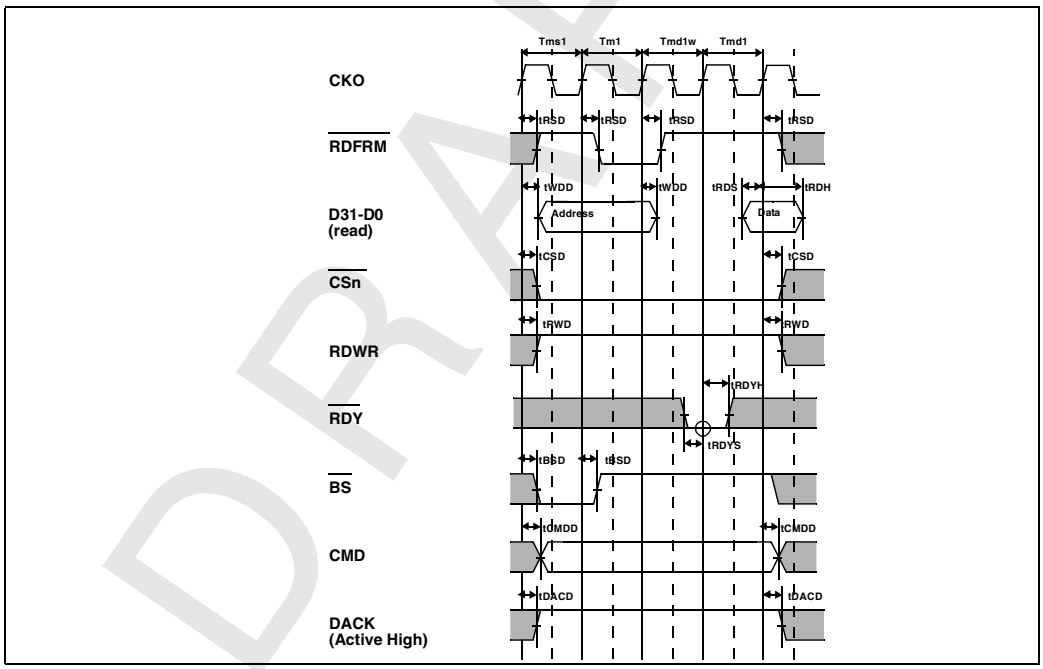


Figure 37: MPX bus cycle: basic read bus cycle (address setup cycle, 0 or 1 internal wait time insertion)

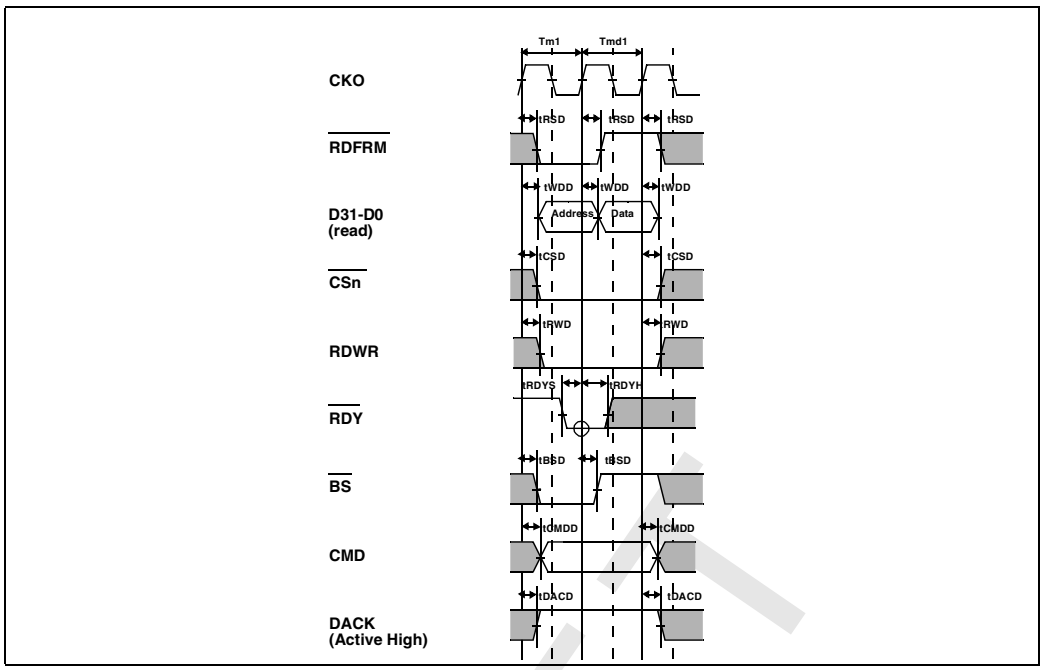


Figure 38: MPX bus cycle: basic write bus cycle (no wait)

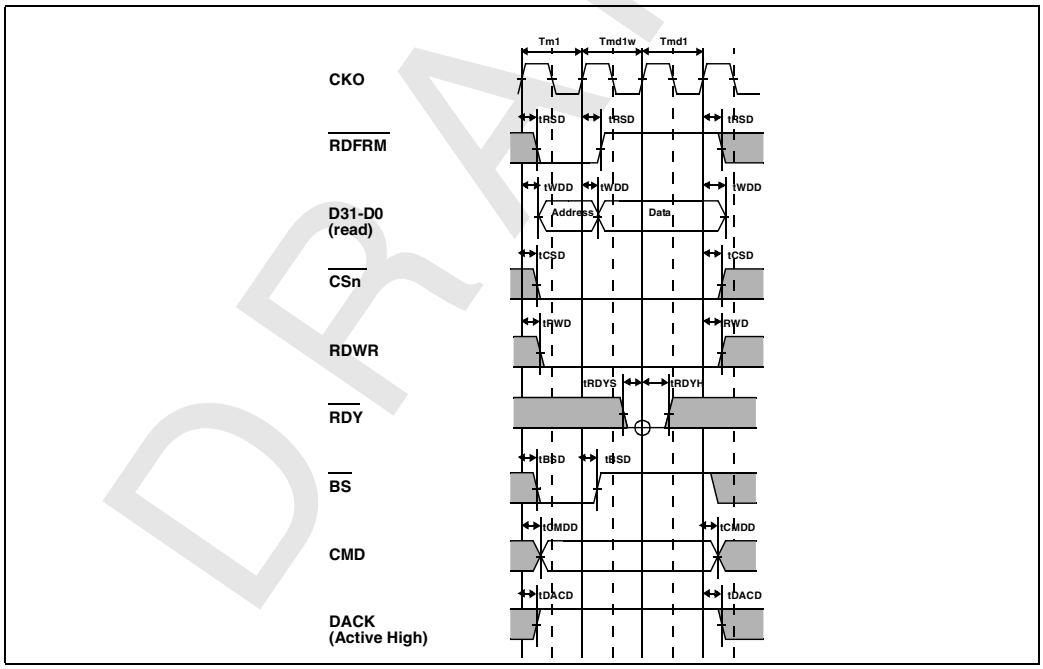


Figure 39: MPX bus cycle: basic write bus cycle (1 internal wait time insertion)

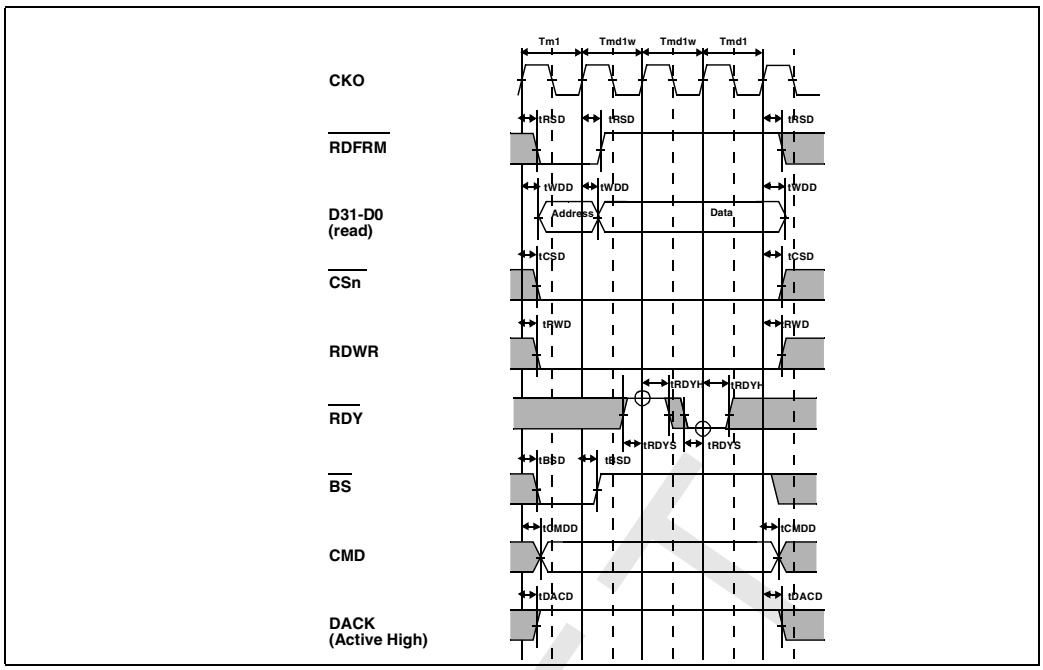


Figure 40: MPX bus cycle: basic write bus cycle (1 internal wait + 1 external wait time insertion)

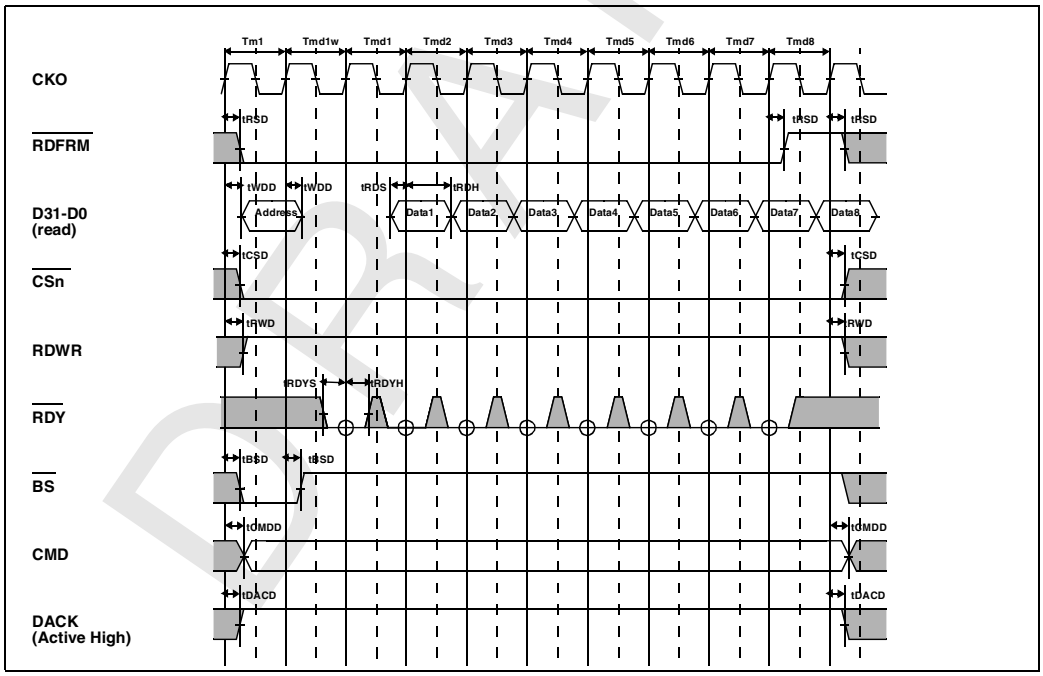


Figure 41: MPX bus cycle: burst read bus cycle (first access 0 or 1 internal wait time insertion)

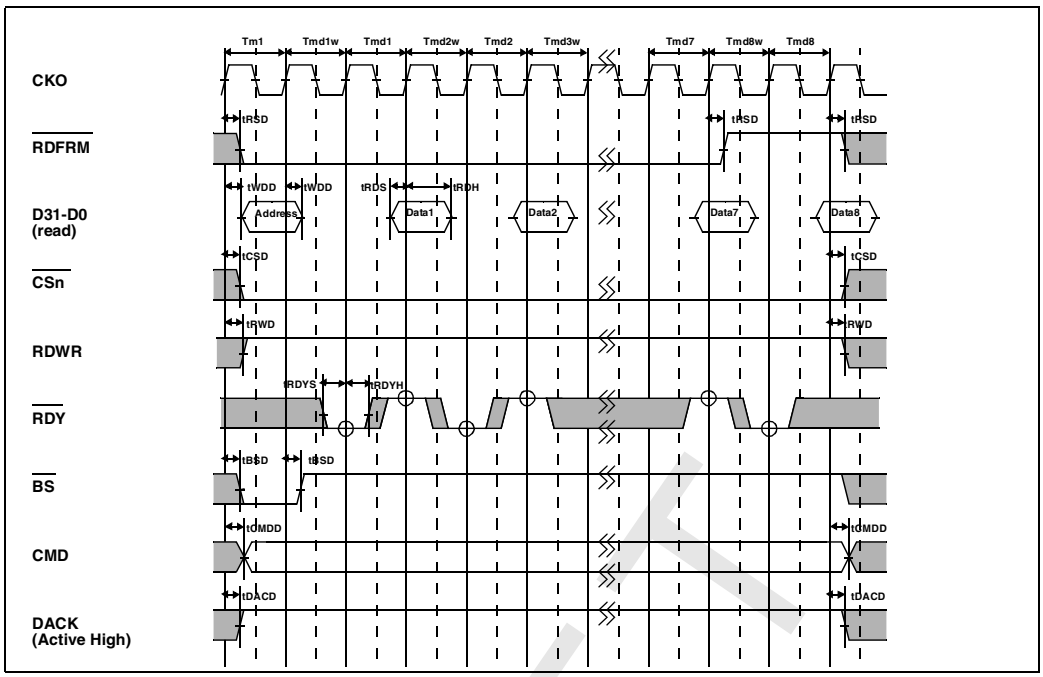


Figure 42: MPX bus cycle: burst read bus cycle (first access 0 or 1 internal wait + 2nd-8th access 1 external wait time insertion)

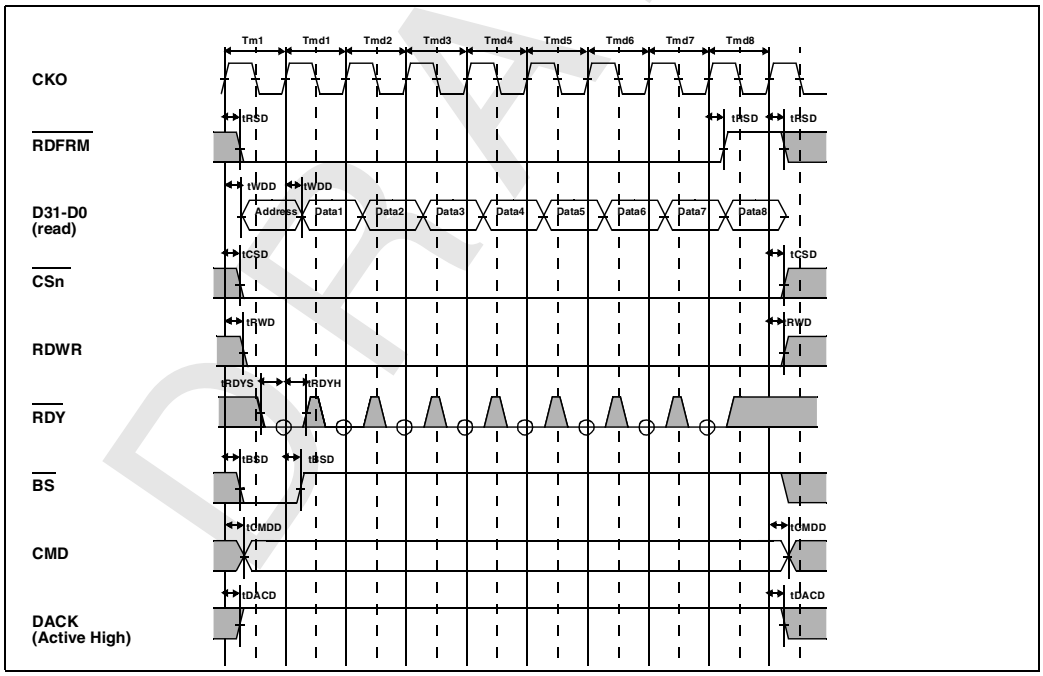


Figure 43: MPX bus cycle: burst write bus cycle (no wait time insertion)

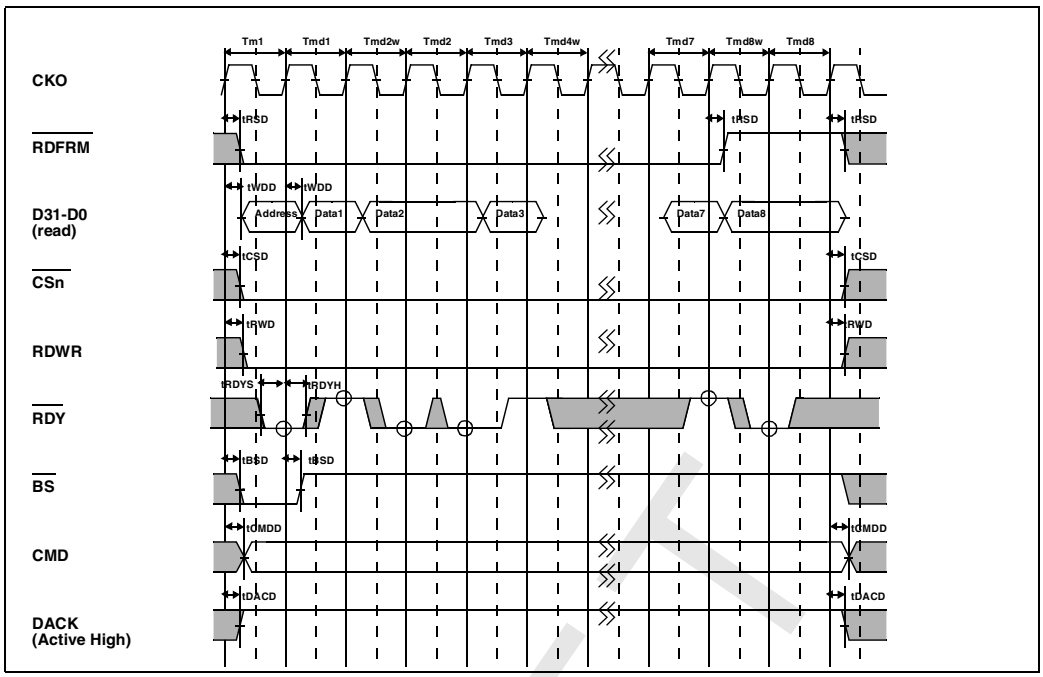


Figure 44: MPX bus cycle: burst write bus cycle (first access 0 internal wait + 2nd-8th access 1 external wait time insertion)

8 Pin descriptions

8.1 PBGA 27x27 ballout

This should be used in conjunction with *Figure 45: Package layout (viewed through package) on page 72*.

Pin No.	Name	Module	Function	Type	Note
D9	RESERVED2	-	Reserved	nc	-
T22	NC	-	No connect	-	-
U22	NC	-	-	-	-
V22	NC	-	No connect	-	-
AD13	RESERVED1	-	No connect	-	-
AD19	RESERVED	-	No connect	-	-
AD26	RESERVED	-	No connect	-	-
T26	TDI	DBG	Test data input	Input	LVTTL
U24	CLKIN	DBG	Debug clock in	Input	LVTTL
U25	ISYNC	DBG	Debug input sync	Input	LVTTL
U26	TDO	DBG	Test data output	Output	LVTTL
V23	TRIN_N	DBG	TRIN_N	Input	LVTTL
V24	IN	DBG	Debug input	Input	LVTTL
V25	TROUT_N	DBG	TROUT_N	Output	LVTTL
V26	TMS	DBG	Test mode select	Input	LVTTL
W23	OUT2	DBG	Debug output 2	Output	LVTTL
W24	OUT3	DBG	Debug output 3	Output	LVTTL
W25	CLKOUT	DBG	Debug clock out	Output	LVTTL
Y23	OUT0	DBG	Debug output 0	Output	LVTTL
Y24	OUT1	DBG	Debug output 1	Output	LVTTL
Y25	OSYNC	DBG	Output sync	Output	LVTTL
P5	DREQ3_N	DMA	DMA request 3 N	Input	LVTTL
U3	DACK2	DMA	DMA acknowledge 2	Output	LVTTL
U4	DREQ2_N	DMA	DMA request 2	Input	LVTTL
V3	DRAK2	DMAC	DMA request ACK2	Output	LVTTL
V4	DACK3	DMAC	DMA ACK3	Output	LVTTL
W2	DRAK1	DMAC	DMA request ACK1	Output	LVTTL
W3	DRAK0	DMAC	DMA request ACK0	Output	LVTTL

Table 18: PBGA ballout

Pin No.	Name	Module	Function	Type	Note
W4	DRAK3	DMAC	DMA request ACK3	Output	LVTTL
Y1	DACK1	DMAC	DMA ACK 1	Output	LVTTL
Y2	DREQ1_N	DMAC	DMA request 1	Input	LVTTL
Y3	DACK0	DMAC	DMA ACK 0	Output	LVTTL
AB1	DREQ0_N	DMAC	DMA request 0	Input	LVTTL
A3	VREF	EMI	Reference voltage	Supply	SSTL/LVTTL
A4	MD4	EMI	Memory data 4	Input/output	SSTL/LVTTL
A5	DQM0	EMI	Data mask 0	Output	SSTL/LVTTL
A6	MD7	EMI	Memory data 7	Input/output	SSTL/LVTTL
A7	MD8	EMI	Memory data 8	Input/output	SSTL/LVTTL
A8	DQM1	EMI	Data mask 1	Output	SSTL/LVTTL
A9	MCLK1	EMI	Memory clock 1	Output	SSTL/LVTTL
A10	CKE1	EMI	Clock enable 1	Output	SSTL/LVTTL
A11	MA12	EMI	Memory address 12	Output	SSTL/LVTTL
A12	MA11	EMI	Memory address 11	Output	SSTL/LVTTL
A13	MD22	EMI	Memory data 22	Input/output	SSTL/LVTTL
A14	MD23	EMI	Memory data 23	Input/output	SSTL/LVTTL
A15	MD28	EMI	Memory data 28	Input/output	SSTL/LVTTL
A16	DQM3	EMI	Data mask 3	Output	SSTL/LVTTL
A17	MD30	EMI	Memory data 30	Input/output	SSTL/LVTTL
A18	MA1	EMI	Memory address 1	Output	SSTL/LVTTL
A19	MCLK0	EMI	Memory clock 0	Output	SSTL/LVTTL
A20	BA1	EMI	Bank address 1	Output	SSTL/LVTTL
A21	MD37	EMI	Memory data 37	Input/output	SSTL/LVTTL
A22	MD38	EMI	Memory data 38	Input/output	SSTL/LVTTL
A23	MD35	EMI	Memory data 35	Input/output	SSTL/LVTTL
B4	MD0	EMI	Memory data 0	Input/output	SSTL/LVTTL
B5	DQS0	EMI	Data strobe 0	Input/output	SSTL/LVTTL
B6	MD3	EMI	Memory data 3	Input/output	SSTL/LVTTL
B7	MD9	EMI	Memory data 9	Input/output	SSTL/LVTTL
B8	MD13	EMI	Memory data 13	Input/output	SSTL/LVTTL
B9	MCLK1_N	EMI	Memory clock 1 N	Output	SSTL/LVTTL
B10	MD11	EMI	Memory data 11	Input/output	SSTL/LVTTL
B11	MD16	EMI	Memory data 16	Input/output	SSTL/LVTTL

Table 18: PBGA ballout

Pin No.	Name	Module	Function	Type	Note
B12	DQS2	EMI	Data strobe 2	Input/output	SSTL/LVTTL
B13	MD18	EMI	Memory data 18	Input/output	SSTL/LVTTL
B14	MD19	EMI	Memory data 19	Input/output	SSTL/LVTTL
B15	MD24	EMI	Memory data 24	Input/output	SSTL/LVTTL
B16	DQS3	EMI	Data strobe 3	Input/output	SSTL/LVTTL
B17	MD26	EMI	Memory data 26	Input/output	SSTL/LVTTL
B18	MA2	EMI	Memory address 2	Output	SSTL/LVTTL
B19	MCLK0_N	EMI	Memory clock 0 N	Output	SSTL/LVTTL
B20	MD32	EMI	Memory data 32	Input/output	SSTL/LVTTL
B21	DQS4	EMI	Data strobe 4	Input/output	SSTL/LVTTL
B22	BA0	EMI	Bank address 0	Output	SSTL/LVTTL
B23	MD39	EMI	Memory data 39	Input/output	SSTL/LVTTL
C4	MD5	EMI	Memory data 5	Input/output	SSTL/LVTTL
C5	MD1	EMI	Memory data 1	Input/output	SSTL/LVTTL
C6	MD6	EMI	Memory data 6	Input/output	SSTL/LVTTL
C7	MA13	EMI	Memory address 13	Output	SSTL/LVTTL
C8	MD12	EMI	Memory data 12	Input/output	SSTL/LVTTL
C9	MD14	EMI	Memory data 14	Input/output	SSTL/LVTTL
C10	MD15	EMI	Memory data 15	Input/output	SSTL/LVTTL
C11	MD20	EMI	Memory data 20	Input/output	SSTL/LVTTL
C12	MD21	EMI	Memory data 21	Input/output	SSTL/LVTTL
C13	DQM2	EMI	Data mask 2	Output	SSTL/LVTTL
C14	MA8	EMI	Memory address 8	Output	SSTL/LVTTL
C15	MA6	EMI	Memory address 6	Output	SSTL/LVTTL
C16	MD29	EMI	Memory data 29	Input/output	SSTL/LVTTL
C17	MA3	EMI	Memory address 3	Output	SSTL/LVTTL
C18	MD31	EMI	Memory data 31	Input/output	SSTL/LVTTL
C19	MCLKIN	EMI	Memory clock input	Input	SSTL/LVTTL
C20	MA10	EMI	Memory address 10	Output	SSTL/LVTTL
C21	MD36	EMI	Memory data 36	Input/output	SSTL/LVTTL
C22	DQM4	EMI	Data mask 4	Output	SSTL/LVTTL
C25	MD44	EMI	Memory data 44	Input/output	SSTL/LVTTL
D6	MD2	EMI	Memory data 2	Input/output	SSTL/LVTTL
D7	MA14	EMI	Memory address14	Output	SSTL/LVTTL

Table 18: PBGA ballout

Pin No.	Name	Module	Function	Type	Note
D8	DQS1	EMI	Data strobe 1	Input/output	SSTL/LVTTL
D10	MD10	EMI	Memory data 10	Input/output	SSTL/LVTTL
D11	CKE0	EMI	Clock enable 0	Output	SSTL/LVTTL
D12	MD17	EMI	Memory data 17	Input/output	SSTL/LVTTL
D13	MA9	EMI	Memory address 9	Output	SSTL/LVTTL
D14	MA7	EMI	Memory address 7	Output	SSTL/LVTTL
D15	MA5	EMI	Memory address 5	Output	SSTL/LVTTL
D16	MD25	EMI	Memory data 25	Input/output	SSTL/LVTTL
D17	MA4	EMI	Memory address 4	Output	SSTL/LVTTL
D18	MD27	EMI	Memory data 27	Input/output	SSTL/LVTTL
D19	MCLKOUT	EMI	Memory clock out	Output	SSTL/LVTTL
D20	MA0	EMI	Memory address 0	Output	SSTL/LVTTL
D21	MD33	EMI	Memory data 33	Input/output	SSTL/LVTTL
D22	MD34	EMI	Memory data 34	Input/output	SSTL/LVTTL
D23	GND	EMI	GND	Supply	0V
D24	MD40	EMI	Memory data 40	Input/output	SSTL/LVTTL
D25	MWE_N	EMI	Memory write enable	Output	SSTL/LVTTL
D26	RAS_N	EMI	Row address strobe	Output	SSTL/LVTTL
E24	MD45	EMI	Memory data 45	Input/output	SSTL/LVTTL
E25	MD41	EMI	Memory data 41	Input/output	SSTL/LVTTL
E26	MCS0_N	EMI	Memory chip select 0	Output	SSTL/LVTTL
F23	CAS_N	EMI	Column address strobe	Output	
F24	MCS1_N	EMI	Memory chip select 1	Output	SSTL/LVTTL
F25	DQS5	EMI	Data strobe 5	Input/output	SSTL/LVTTL
F26	DQM5	EMI	Data mask 5	Output	SSTL/LVTTL
G23	MD42	EMI	Memory data 42	Input/output	SSTL/LVTTL
G24	MD46	EMI	Memory data 46	Input/output	SSTL/LVTTL
G25	MD43	EMI	Memory data 43	Input/output	SSTL/LVTTL
G26	MD47	EMI	Memory data 47	Input/output	SSTL/LVTTL
H23	MD48	EMI	Memory data 48	Input/output	SSTL/LVTTL
H24	MD52	EMI	Memory data 52	Input/output	SSTL/LVTTL
H25	MD49	EMI	Memory data 49	Input/output	SSTL/LVTTL
H26	MD53	EMI	Memory data 53	Input/output	SSTL/LVTTL
J23	DQS6	EMI	Data strobe 6	Input/output	SSTL/LVTTL

Table 18: PBGA ballout

Pin No.	Name	Module	Function	Type	Note
J24	DQM6	EMI	Data mask 6	Output	SSTL/LVTTL
J25	MCLK2_N	EMI	Memory clock 2 N	Output	SSTL/LVTTL
J26	MCLK2	EMI	Memory clock 2	Output	SSTL/LVTTL
K23	MD50	EMI	Memory data 50	Input/output	SSTL/LVTTL
K24	MD54	EMI	Memory data 54	Input/output	SSTL/LVTTL
K25	MD51	EMI	Memory data 51	Input/output	SSTL/LVTTL
K26	MD55	EMI	Memory data 55	Input/output	SSTL/LVTTL
L23	MD56	EMI	Memory data 56	Input/output	SSTL/LVTTL
L24	MD60	EMI	Memory data 60	Input/output	SSTL/LVTTL
L25	MD57	EMI	Memory data 57	Input/output	SSTL/LVTTL
L26	MD61	EMI	Memory data 61	Input/output	SSTL/LVTTL
M23	DQS7	EMI	Data strobe 7	Input/output	SSTL/LVTTL
M24	DQM7	EMI	Data mask 7	Output	SSTL/LVTTL
M25	MD58	EMI	Memory data 58	Input/output	SSTL/LVTTL
M26	MD62	EMI	Memory data 62	Input/output	SSTL/LVTTL
N23	MD59	EMI	Memory data 59	Input/output	SSTL/LVTTL
N24	MD63	EMI	Memory data 63	Input/output	SSTL/LVTTL
D1	DATA2	FEMI	Data 2	Input/output	LVTTL
D2	DATA1	FEMI	Data 1	Input/output	LVTTL
D3	DATA0	FEMI	Data 0	Input/output	LVTTL
E1	DATA6	FEMI	Data 6	Input/output	LVTTL
E2	DATA5	FEMI	Data 5	Input/output	LVTTL
E3	DATA4	FEMI	Data 4	Input/output	LVTTL
E4	DATA3	FEMI	Data 3	Input/output	LVTTL
F1	DATA10	FEMI	Data 10	Input/output	
F2	DATA9	FEMI	Data 9	Input/output	
F3	DATA8	FEMI	Data 8	Input/output	
F4	DATA7	FEMI	Data 7	Input/output	
G1	DATA14	FEMI	Data 14	Input/output	
G2	DATA13	FEMI	Data 13	Input/output	
G3	DATA12	FEMI	Data 12	Input/output	
G4	DATA11	FEMI	Data 11	Input/output	
H1	ADDR2	FEMI	Address 2	Output	LVTTL
H2	ADDR1	FEMI	Address 1	Output	LVTTL

Table 18: PBGA ballout

Pin No.	Name	Module	Function	Type	Note
H3	ADDR0	FEMI	Address 0	Output	LVTTL
H4	DATA15	FEMI	Data 15	Input/output	LVTTL
J1	ADDR6	FEMI	Address 6	Output	LVTTL
J2	ADDR5	FEMI	Address 5	Output	LVTTL
J3	ADDR4	FEMI	Address 4	Output	LVTTL
J4	ADDR3	FEMI	Address 3	Output	LVTTL
K1	ADDR10	FEMI	Address 10	Output	LVTTL
K2	ADDR9	FEMI	Address 9	Output	LVTTL
K3	ADDR8	FEMI	Address 8	Output	LVTTL
K4	ADDR7	FEMI	Address 7	Output	LVTTL
L1	ADDR14	FEMI	Address 14	Output	LVTTL
L2	ADDR13	FEMI	Address 13	Output	LVTTL
L3	ADDR12	FEMI	Address 12	Output	LVTTL
L4	ADDR11	FEMI	Address 11	Output	LVTTL
M1	ADDR18	FEMI	Address 18	Output	LVTTL
M2	ADDR17	FEMI	Address 17	Output	LVTTL
M3	ADDR16	FEMI	Address 16	Output	LVTTL
M4	ADDR15	FEMI	Address 15	Output	LVTTL
N1	ADDR22	FEMI	Address 22	Output	LVTTL
N2	ADDR21	FEMI	Address 21	Output	LVTTL
N3	ADDR20	FEMI	Address 20	Output	LVTTL
N4	ADDR19	FEMI	Address 19	Output	LVTTL
P1	CS0_N	FEMI	Chip select 0 N	Input/output	LVTTL
P2	ADDR25	FEMI	Address 25	Output	LVTTL
P3	ADDR24	FEMI	Address 24	Output	LVTTL
P4	ADDR23	FEMI	Address 23	Output	LVTTL
R1	CS4_N	FEMI	Chip select 4 N	Input/output	LVTTL
R2	CS3_N	FEMI	Chip select 3 N	Input/output	LVTTL
R3	CS2_N	FEMI	Chip select 2 N	Input/output	LVTTL
R4	CS1_N	FEMI	Chip select 1 N	Input/output	LVTTL
T1	WE3_N	FEMI	Write enable 3 N	Output	LVTTL
T2	WE2_N	FEMI	Write enable 2 N	Output	LVTTL
T3	WE1_N	FEMI	Write enable 1 N	Output	LVTTL
T4	WE0_N	FEMI	Write enable 0 N	Output	LVTTL

Table 18: PBGA ballout

Pin No.	Name	Module	Function	Type	Note
U1	BS_N	FEMI	Bus start	Input/output	LVTTL
U2	RDWR	FEMI	Read/write	Input/output	LVTTL
V1	RDY_N	FEMI	Wait state request	Input/output	LVTTL
V2	WP_N	FEMI	Write protect	Output	LVTTL
W1	RDFRM_N	FEMI	Read/frame signal	Input/output	LVTTL
Y4	DATA16	FEMI	Data 16	Input/output	LVTTL
AA1	DATA17	FEMI	Data 17	Input/output	LVTTL
AA2	DATA18	FEMI	Data 18	Input/output	LVTTL
AA3	DATA19	FEMI	Data 19	Input/output	LVTTL
AB3	CKO	FEMI	FEMI clock out	Output	LVTTL
AB4	DATA21	FEMI	Data 21	Input/output	LVTTL
AB7	BREQ_N	FEMI	Bus request	Input	LVTTL
AC3	DATA22	FEMI	Data22	Input/output	LVTTL
AC5	DATA26	FEMI	Data26	Input/output	LVTTL
AC6	DATA30	FEMI	Data30	Input/output	LVTTL
AC7	CMD0	FEMI	Command0	Input/output	LVTTL
AD4	DATA23	FEMI	Data23	Input/output	LVTTL
AD5	DATA27	FEMI	Data27	Input/output	LVTTL
AD6	DATA31	FEMI	Data31	Input/output	LVTTL
AD7	CMD1	FEMI	Command1	Input/output	LVTTL
AD8	BACK_N	FEMI	Bus acknowledge	Output	LVTTL
AE4	DATA24	FEMI	Data24	Input/output	LVTTL
AE5	DATA28	FEMI	Data28	Input/output	LVTTL
AE6	CMD4	FEMI	Command4	Input/output	LVTTL
AE7	CMD2	FEMI	Command2	Input/output	LVTTL
AF4	DATA25	FEMI	Data25	Input/output	LVTTL
AF5	DATA29	FEMI	Data29	Input/output	LVTTL
AF6	CMD5	FEMI	Command5	Input/output	LVTTL
AF7	CMD3	FEMI	Command3	Input/output	LVTTL
P25	IRL0	INTC	Interrupt 0	Input	LVTTL
R25	IRL1	INTC	Interrupt 1	Input	LVTTL
T23	IRL3	INTC	Interrupt level 3	Input	LVTTL
T25	IRL2	INTC	Interrupt level 2	Input	LVTTL
U23	NMI	INTC	NMI	Input	LVTTL

Table 18: PBGA ballout

Pin No.	Name	Module	Function	Type	Note
AB17	PCICKSEL	PCI	PCI clock select	Input	DC
AB21	HOSTEN	PCI	PCI host enable	Input	DC
AC9	AD5	PCI	Address/data5	Input/output	LVTTL
AC10	AD8	PCI	Address/data8	Input/output	LVTTL
AC11	AD12	PCI	Address/data12	Input/output	LVTTL
AC12	CBE1_N	PCI	Command/byte enable1	Input/output	LVTTL
AC13	LOCK_N	PCI	Lock	Input/output	LVTTL
AC14	TRDY_N	PCI	Target ready	Input/output	LVTTL
AC15	AD16	PCI	Address/data16	Input/output	LVTTL
AC16	AD20	PCI	Address/data20	Input/output	LVTTL
AC17	IDSEL	PCI	Initialization device select	Input	LVTTL
AC18	AD26	PCI	Address/data26	Input/output	LVTTL
AC19	AD29	PCI	Address/data29	Input/output	LVTTL
AC20	AD31	PCI	Address/data31	Input/output	LVTTL
AC21	GNT3_N	PCI	Grant3	Output	LVTTL
AC22	INTD_N	PCI	Interrupt D	Input	LVTTL
AD9	AD4	PCI	Address/data4	Input/output	LVTTL
AD10	CBE0_N	PCI	Command/byte enable0	Input/output	LVTTL
AD11	AD11	PCI	Address/data11	Input/output	LVTTL
AD12	AD15	PCI	Address/data15	Input/output	LVTTL
AD14	DEVSEL_N	PCI	Device select	Input/output	LVTTL
AD15	CBE2_N	PCI	Command/byte enable2	Input/output	LVTTL
AD16	AD19	PCI	Address/data19	Input/output	LVTTL
AD17	AD23	PCI	Address/data23	Input/output	LVTTL
AD18	AD25	PCI	Address/data25	Input/output	LVTTL
AD20	AD30	PCI	Address/data30	Input/output	LVTTL
AD21	REQ2_N	PCI	Request 2	Input	LVTTL
AD22	GNT2_N	PCI	Grant 2	Output	LVTTL
AD23	INTC_N	PCI	Interrupt C	Input	LVTTL
AE8	AD1	PCI	Address/data1	Input/output	LVTTL
AE9	AD3	PCI	Address/data3	Input/output	LVTTL
AE10	AD7	PCI	Address/data7	Input/output	LVTTL
AE11	AD10	PCI	Address/data10	Input/output	LVTTL
AE12	AD14	PCI	Address/data14	Input/output	LVTTL

Table 18: PBGA ballout

Pin No.	Name	Module	Function	Type	Note
AE13	SERR_N	PCI	System error	Input/output	LVTTL
AE14	STOP_N	PCI	Stop	Input/output	LVTTL
AE15	FRAME_N	PCI	Cycle frame	Input/output	LVTTL
AE16	AD18	PCI	Address/data18	Input/output	LVTTL
AE17	AD22	PCI	Address/data22	Input/output	LVTTL
AE18	AD24	PCI	Address/data24	Input/output	LVTTL
AE19	AD28	PCI	Address/data28	Input/output	LVTTL
AE20	REQ3_N	PCI	Request3	Input	LVTTL
AE21	REQ1_N	PCI	Request1	Input	LVTTL
AE22	GNT1_N	PCI	Grant1	Output	LVTTL
AE23	INTB_N	PCI	Interrupt B	Input	LVTTL
AE24	INTA_N	PCI	Interrupt A	Input/output	LVTTL
AF8	AD0	PCI	Address/data0	Input/output	LVTTL
AF9	AD2	PCI	Address/data2	Input/output	LVTTL
AF10	AD6	PCI	Address/data6	Input/output	LVTTL
AF11	AD9	PCI	Address/data9	Input/output	LVTTL
AF12	AD13	PCI	Address/data13	Input/output	LVTTL
AF13	PAR	PCI	Parity	Input/output	LVTTL
AF14	PERR_N	PCI	Parity error	Input/output	LVTTL
AF15	IRDY_N	PCI	Initiator ready	Input/output	LVTTL
AF16	AD17	PCI	Address/data17	Input/output	LVTTL
AF17	AD21	PCI	Address/data21	Input/output	LVTTL
AF18	CBE3_N	PCI	Command/byte enable3	Input/output	LVTTL
AF19	AD27	PCI	Address/data27	Input/output	LVTTL
AF20	PME_N	PCI	Power management event	Input/output	LVTTL
AF21	REQ0_N	PCI	Request 0	Input/output	LVTTL
AF22	GNT0_N	PCI	Grant0	Input/output	LVTTL
AF23	PCICLK	PCI	PCI clock	Input	LVTTL
P26	TRSTN	PMU	Test reset	Input	LVTTL
R26	TCK	PMU	Test clock	Input	LVTTL
A1	VCC_2.5	Power	EMI I/O power	Supply	2.5v/3.3v
A2	VCC_VREF	Power	VREF power	Supply	2.5v/3.3v
A24	VCC_2.5	Power	EMI I/O power	Supply	2.5v/3.3v
A25	VCC_2.5	Power	EMI I/O power	Supply	2.5v/3.3v

Table 18: PBGA ballout

Pin No.	Name	Module	Function	Type	Note
A26	VCC_2.5	Power	EMI I/O power	Supply	2.5v/3.3v
B1	NC	Power	-	-	-
B2	VCC_2.5	Power	EMI I/O power	Supply	2.5v/3.3v
B3	GND_VREF	Power	VREF GND	Supply	0v
B24	VCC_2.5	Power	EMI I/O power	Supply	2.5v/3.3v
B25	VCC_2.5	Power	EMI I/O power	Supply	2.5v/3.3v
B26	VDD_DLL	Power	EMI DLL power	Supply	1.5v
C1	VPP	Power	VPP (use EMI)	Supply	1.5v
C2	VCC_3.3	Power	FEMI I/O power	Supply	3.3v
C3	VCC_2.5	Power	EMI I/O power	Supply	2.5v/3.3v
C23	VCC_2.5	Power	EMI I/O power	Supply	2.5v/3.3v
C24	VCC_2.5	Power	EMI I/O power	Supply	2.5v/3.3v
C26	GND_DLL	Power	EMI DLL GND	Supply	0V
D4	GND	Power	GND	Supply	0V
D5	VCC_2.5	Power	EMI I/O power	Supply	2.5v/3.3v
E5	VCC_2.5	Power	EMI I/O power	Supply	2.5v/3.3v
E6	VCC_2.5	Power	EMI I/O power	Supply	2.5v/3.3v
E7	GND	Power	GND	Supply	0V
E8	VDD_1.5	Power	Core power	Supply	1.5v
E9	GND	Power	GND	Supply	0V
E10	VCC_2.5	Power	EMI I/O power	Supply	2.5v/3.3v
E11	VCC_2.5	Power	EMI I/O power	Supply	2.5v/3.3v
E12	GND	Power	GND	Supply	0V
E13	GND	Power	GND	Supply	0V
E14	VDD_1.5	Power	Core power	Supply	1.5v
E15	GND	Power	GND	Supply	0V
E16	VCC_2.5	Power	EMI I/O power	Supply	2.5v/3.3v
E17	VCC_2.5	Power	EMI I/O power	Supply	2.5v/3.3v
E18	GND	Power	GND	Supply	0V
E19	VDD_1.5	Power	Core power	Supply	1.5v
E20	GND	Power	GND	Supply	0V
E21	VCC_2.5	Power	EMI I/O power	Supply	2.5v/3.3v
E22	VCC_2.5	Power	EMI I/O power	Supply	2.5v/3.3v
E23	VCC_2.5	Power	EMI I/O power	Supply	2.5v/3.3v

Table 18: PBGA ballout

Pin No.	Name	Module	Function	Type	Note
F5	VCC_3.3	Power	3.3V I/O power	Supply	
F22	VCC_2.5	Power	EMI I/O power	Supply	
G5	GND	Power	GND	Supply	
G22	GND	Power	GND	Supply	
H5	VDD_1.5	Power	Core power	Supply	1.5V
H22	VDD_1.5	Power	Core power	Supply	1.5V
J5	GND	Power	GND	Supply	0V
J22	GND	Power	GND	Supply	0V
K5	VCC_3.3	Power	3.3V I/O power	Supply	3.3V
K22	VCC_2.5	Power	EMI I/O power	Supply	2.5v/3.3v
L5	VCC_3.3	Power	3.3V I/O power	Supply	3.3V
L11	GND	Power	GND	Supply	0V
L12	GND	Power	GND	Supply	0V
L13	GND	Power	GND	Supply	0V
L14	GND	Power	GND	Supply	0V
L15	GND	Power	GND	Supply	0V
L16	GND	Power	GND	Supply	0V
L22	VCC_2.5	Power	EMI I/O power	Supply	2.5v/3.3v
M5	GND	Power	GND	Supply	0V
M11	GND	Power	GND	Supply	0V
M12	GND	Power	GND	Supply	0V
M13	GND	Power	GND	Supply	0V
M14	GND	Power	GND	Supply	0V
M15	GND	Power	GND	Supply	0V
M16	GND	Power	GND	Supply	0V
M22	GND	Power	GND	Supply	0V
N5	VDD_1.5	Power	Core power	Supply	1.5V
N11	GND	Power	GND	Supply	0V
N12	GND	Power	GND	Supply	0V
N13	GND	Power	GND	Supply	0V
N14	GND	Power	GND	Supply	0V
N15	GND	Power	GND	Supply	0V
N16	GND	Power	GND	Supply	0V
N22	GND	Power	GND	Supply	0V

Table 18: PBGA ballout

Pin No.	Name	Module	Function	Type	Note
P11	GND	Power	GND	Supply	0V
P12	GND	Power	GND	Supply	0V
P13	GND	Power	GND	Supply	0V
P14	GND	Power	GND	Supply	0V
P15	GND	Power	GND	Supply	0V
P16	GND	Power	GND	Supply	0V
P22	VDD_1.5	Power	Core power	Supply	1.5V
R5	GND	Power	GND	Supply	0V
R11	GND	Power	GND	Supply	0V
R12	GND	Power	GND	Supply	0V
R13	GND	Power	GND	Supply	0V
R14	GND	Power	GND	Supply	0V
R15	GND	Power	GND	Supply	0V
R16	GND	Power	GND	Supply	0V
R22	GND	Power	GND	Supply	0V
T5	VCC_3.3	Power	3.3v I/O power	Supply	3.3V
T11	GND	Power	GND	Supply	0V
T12	GND	Power	GND	Supply	0V
T13	GND	Power	GND	Supply	0V
T14	GND	Power	GND	Supply	0V
T15	GND	Power	GND	Supply	0V
T16	GND	Power	GND	Supply	0V
U5	VCC_3.3	Power	3.3v I/O power	Supply	LVTTL
V5	GND	Power	GND	Supply	0v
W5	VDD_1.5	Power	Core power	Supply	1.5V
W22	VDD_1.5	Power	Core power	Supply	1.5V
Y5	GND	Power	GND	Supply	0v
AB5	VCC_3.3	Power	3.3v I/O power	Supply	3.3v
AB6	VCC_3.3	Power	3.3v I/O power	Supply	3.3v
AB8	VDD_1.5	Power	Core power	Supply	1.5v
AB9	GND	Power	GND	Supply	0v
AB10	VCC_3.3	Power	3.3v I/O power	Supply	3.3v
AB11	VCC_3.3	Power	3.3v I/O power	Supply	3.3v
AB12	GND	Power	GND	Supply	0v

Table 18: PBGA ballout

Pin No.	Name	Module	Function	Type	Note
AB13	VDD_1.5	Power	Core power	Supply	1.5v
AB14	GND	Power	GND	Supply	0v
AB15	GND	Power	GND	Supply	0v
AB16	VCC_3.3	Power	3.3v I/O power	Supply	3.3v
AB18	GND	Power	GND	Supply	0v
AB19	VDD_1.5	Power	Core power	Supply	1.5v
AB20	GND	Power	GND	Supply	0v
AB22	VCC_3.3	Power	3.3v I/O power	Supply	3.3v
AB26	VCC_CPG	Power	Core oscillator power	Supply	3.3v
AC4	GND	Power	GND	Supply	0v
AC23	GND	Power	GND	Supply	0v
AD1	GND_RTC	Power	RTC oscillator GND pin	Supply	0v
AD2	VBGN	Power	3.3v I/O power	Supply	3.3v
AD3	VBGP	Power	3.3v I/O power	Supply	3.3v
AD24	VCC_3.3	Power	3.3v I/O power	Supply	3.3v
AD25	VCC_3.3	Power	3.3v I/O power	Supply	3.3v
AE1	VCC_RTC	Power	RTC oscillator VCC pin	Supply	3.3v
AE2	VCC_3.3	Power	3.3v I/O power	Supply	3.3v
AE3	VCC_3.3	Power	3.3v I/O power	Supply	3.3v
AE25	VCC_3.3	Power	3.3v I/O power	Supply	3.3v
AE26	VCC_3.3	Power	3.3v I/O power	Supply	3.3v
AF1	VCC_3.3	Power	3.3v I/O power	Supply	3.3v
AF2	VCC_3.3	Power	3.3v I/O power	Supply	3.3v
AF3	VCC_3.3	Power	3.3v I/O power	Supply	3.3v
AF24	VDD_PLL	Power	System PLL power	Supply	1.5v
AF25	VCC_3.3	Power	3.3v I/O power	Supply	3.3v
AF26	VCC_3.3	Power	3.3v I/O power	Supply	3.3v
AC1	XTAL2	RTC	Connects crystal to RTC oscillator	Output	32.768kHz
AC2	EXTAL2	RTC	Connects crystal to RTC oscillator	Input	32.768kHz
P23	RTS	SCI	RTS	Input/output	SSTL/LVTTL
P24	SCK2	SCI	SCK	Input/output	SSTL/LVTTL
R23	CTS	SCI	CTS	Input/output	LVTTL
R24	TXD2	SCI	TXD	Output	LVTTL
T24	RXD2	SCIF	RXD2	Input	LVTTL

Table 18: PBGA ballout

Pin No.	Name	Module	Function	Type	Note
N25	MRESET_N	SYSTEM	Manual reset	Input	DC
N26	PRESET_N	SYSTEM	Power on reset	Input	DC
W26	STATUS1	SYSTEM	Status 1	Output	LVTTL
Y22	MODE3	SYSTEM	Selects use/non-use of crystal resonator	Input	DC
Y26	STATUS0	SYSTEM	Status0	Output	LVTTL
AB23	MODE7	SYSTEM	FEMI CS0 size	Input	DC
AB24	MODE6	SYSTEM	FEMI CS0 bus type	Input	DC
AB25	MODE5	SYSTEM	FEMI CS area merge	Input	DC
AC8	BWSEL	SYSTEM	BWSEL	Input	DC
AC24	MODE8	SYSTEM	FEMI CS0 size	Input	DC
AC25	EXTAL	SYSTEM	Connects crystal resonator	Input	System clock
AC26	XTAL	SYSTEM	Connects crystal resonator	Output	System clock
AB2	TCLK	TMU	Timer clock in/RTC clock out	Input/output	LVTTL

Table 18: PBGA ballout

9 Package

9.1 Package layout

Physical properties

- 456 pin BGA package
- Other parameters refer to *Table 46*.

Figure 45 is a diagram of the pin disposition on the package.

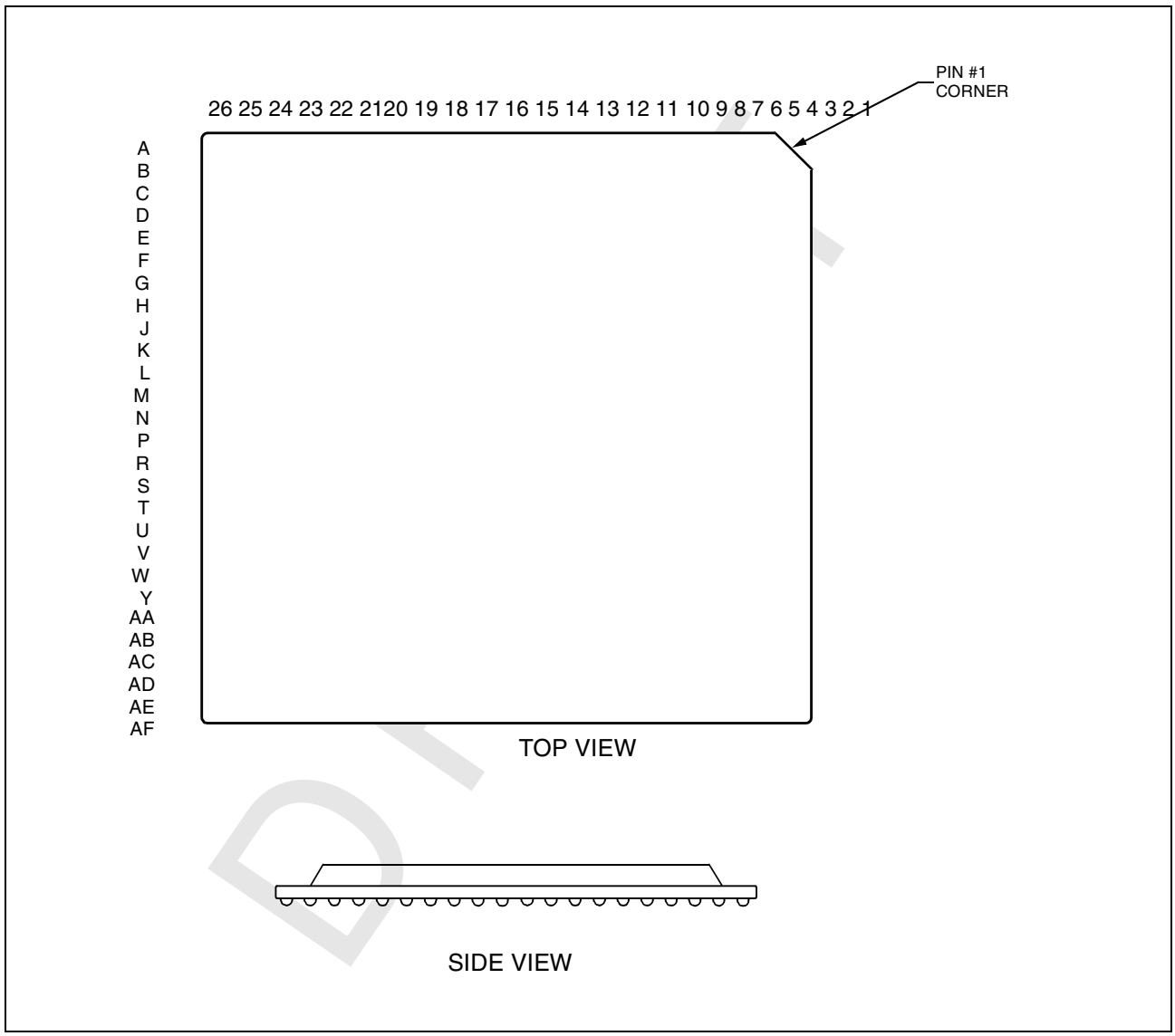


Figure 45: Package layout (viewed through package)

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PACKAGE OUTLINE ASSEMBLY

TITLE: PBGA 35x35x2.59 420 & 420+36 5R26x26 1.27

PACKAGES CODE: HS = 420 – 2 Layers
Not codified yet = 420 – 4 Layers
HQ = 420+36 – 2 Layers
UK = 420+36 – 4 Layers

JEDEC/EIAJ REFERENCE NUMBER: JEDEC STANDARD NO.95-1 SECTION 14
(Ball Grid Array Package Design Guide)

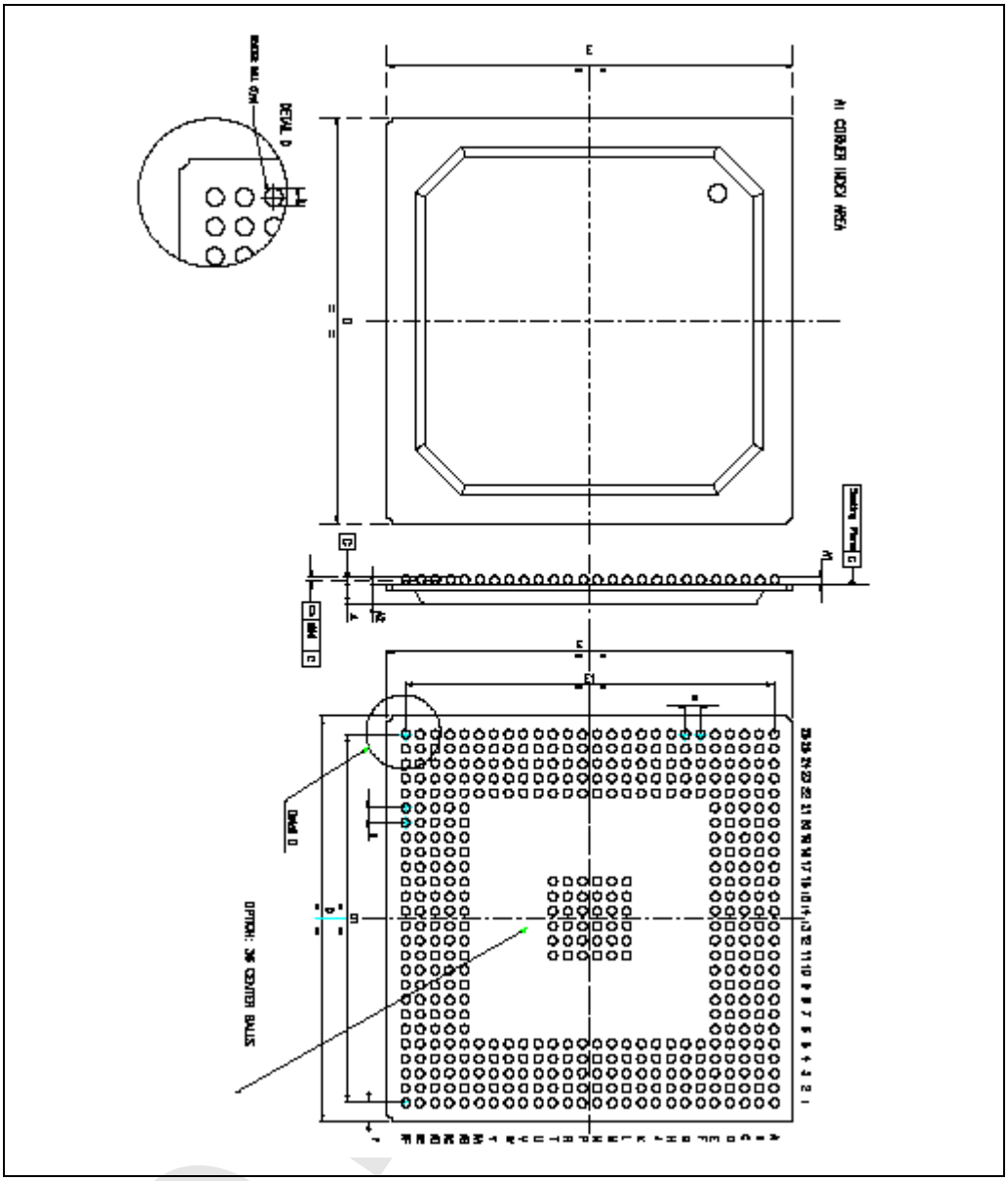
	DIMENSIONS					
	DATABOOK (mm)			DRAWING (mm)		
REF.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.590			2.590
A1	0.360			0.500	0.600	0.700
A2			1.890			1.890
b	0.600	0.750	0.900	0.600	0.760	0.900
D	34.800	35.000	35.200	34.800	35.000	35.200
D1		31.750			31.750	
E	34.800	35.000	35.200	34.800	35.000	35.200
E1		31.750			31.750	
e	1.195	1.270	1.345	1.195	1.270	1.345
f	1.475	1.625	1.775	1.475	1.625	1.775
ddd			0.200			0.200

NOTES:

(1) - PBGA stands for **P**lastic **B**all **G**rid **A**rray.

(2) - The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heatslug.
- A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner.
- Exact shape of each corner is optional.

Figure 46: Package outline assembly



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