

RENESAS TECHNICAL UPDATE

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
RenesasTechnology Corp.

Product Category	MPU&MCU		Document No.	TN-SH7-501A/EA	Rev.	1.0
Title	Notice of the DMA transmission of A/D converter		Information Category	Usage Limitation		
Applicable Product	SH7760	Lot No.	Reference Document	SH7760 hardware manual (ADE-602-291)		
		All				

The A/D Converter (ADC) of SH7760 has following notice.

1. Condition

When DMAC selection bit (DMASL) of ADCSR is set to 1, the value of ADC register read by CPU is unknown.
Then, ADC registers can't be read during ADC DMA transmission. But writing register is possible.
And while ADC execute DMA transmission, if CPU read MFI register, the value may not be correct.
Furthermore, DMA transmitted value of ADC also may not be correct.

2. Workaround

Please apply one of following 1) or 2) workarounds.

- 1) Do not read ADC registers by CPU during ADCSR.DMASL=1.
- 2) Use ADCSR.DMASL=0.