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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-SH7-528A/EA	Rev.	1.0
Title	SH7750 series The revision about power-on and power-off procedure.		Information Category	Correction or Supplement of Document		
Applicable Product	SH7750/ SH7750S/ SH7750R	Lot No. ALL	Reference Document	SH7750 series Hardware Manual ADE-602-124		

SH7750 series Power-On and Power-Off Procedures.

1. Power-on Procedure

(1)Please turn on the power supply of I/O, RTC, PLL1/2 and CPG to the same timing as a power supply VDDQ.

(2)After turning on a power supply to VDDQ or simultaneously, the input of a signal line (RESET, MRESET, MD0-MD10, external clock, and etc) must be input. If the signal lines are entered first, the LSI may be damaged.

(i)Please make a RESET signal into a Low level at the power supply VDDQ.

(ii)Input high level to MRESET in compliance with the voltage level of the I/O, PLL1/2, RTC, CPG power supply voltage.

(3)It recommends that a power supply to VDDQ is in advance, and a power supply to VDD is behind.

(4)In addition to the above (1), (2), (3) and following (i)(ii), please follow “3. The ratings for power-on and power-off”.

(i) In the case of this LSI simple substance, the power supply sequence of a power supply to VDDQ and VDD does not have time restrictions. Please refer to Figure H {Fig. H1}. In addition, it recommends performing a power-on procedure at the shortest possible time.

(ii)When this LSI is connected with other elements on the mounting board, please keep that

-0.3V < Vin < VDDQ+0.3V.

Moreover, as shown in figure H {Fig. H2}, restrictions time until it goes up from GND [0V] to a operation voltage value {VDDQ (min), VDD (min)} is 100ms (max). It is exceeded, a product may be damaged. In addition, it recommends performing a power-on procedure at the shortest possible time.

2 . Power-off Procedure

(1) Please turn off the power supply of I/O, RTC, PLL1/2 and CPG to the same timing as a power supply VDDQ.

(2) There is no timing regulation of a signal line (RESET and MRESET).

(3) The input level to the pin must be lowered in compliance with the I/O, PLL1/2, RTC, CPG power supply voltage.

(4) It recommends that turning off the I/O, PLL1/2, RTC, CPG power supply voltage after (or at the same time as) turning off the internal power supply voltage (VDD).

(5) In addition to the above (1), (2), (3), (4) and following (i)(ii), please follow “3. The ratings for power-on and power-off”.

(i) In the case of this LSI simple substance, the power supply sequence of a power supply to VDDQ and VDD does not have time restrictions. Please refer to Figure H {Fig. H1}. In addition, it recommends performing a power off at the shortest possible time.

(ii)When this LSI is connected with other elements on the mounting board, please keep that

-0.3V < Vin < VDDQ+0.3V.

Moreover, as shown in figure H {Fig. H2}, restrictions time until it goes down from a operation voltage value {VDDQ (min), VDD (min)} to GND [0V] is 150ms (max). It is exceeded, a product may be damaged. In addition, it recommends performing shortest possible time.

3. The ratings for power-on and power-off

A product may be damaged when not satisfying the conditions of (1), (2), and (3) below.

(1) VDDQ = VDD-CPG=VDD-RTC=VDD-PLL1/2.

VDD-RTC in the hardware standby mode is to follow the content 9.8.5 of the SH4-SH7750 hardware manual in the case of SH7750S.

(2) -0.3V < VDD < VDDQ+0.3V.

(3)VSS = VSSQ = VSS-PLL1/2 = VSS-CPG=VSS-RTC = GND [0V].

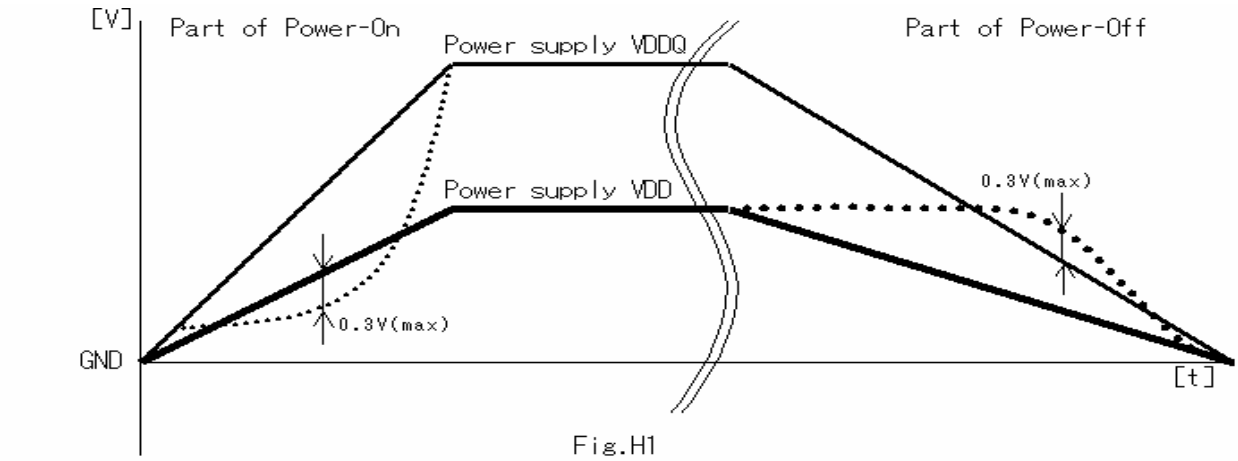

Fig.H1

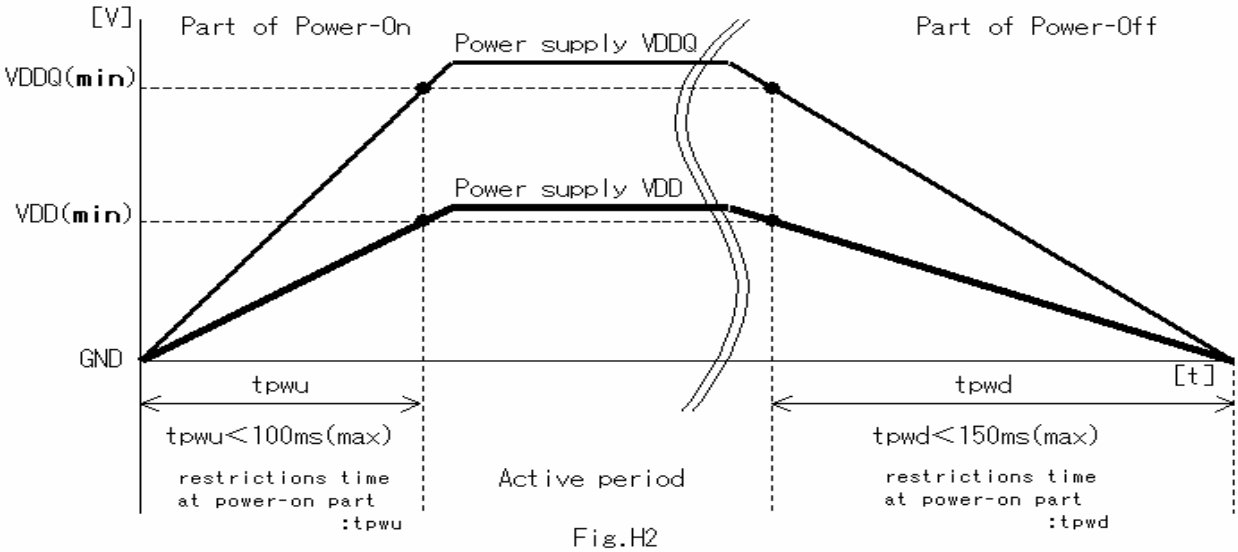

Fig.H2

Fig.H Power-On and Power-off Procedures.