date: 2003/11/28

RENESAS TECHNICAL UPDATE

Classification of Production	MPU&MCU		No	TN-SH7-494A/E	Rev	1
THEME	SH7760 type number change due to logical modification.	Classification of Information	1. Spec change 2. Supplement of Documents 3. Limitation of Use (4.) Change of Mask 5. Change of Production Line			
PRODUCT NAME	HD6417760BP200D HD6417760BP200DV	Lot No. All	Reference Documents	SH7760 hardware manual Rev 1.0 (ADE-602-291)	Effective Date Eternity	

The mask of SH7760(HD6417760) is changed due to logical modifications described below. Please see the following new type number.

1. Product Type Number

The type numbers of HD6417760BP200D and HD6417760BP200DV were changed.

Table 1 Product Type Number

Current Type Number	New Type Number (A Mask)	Note
HD6417760BP200D	HD6417760BP200AD	Non-Pb free solder.
HD6417760BP200DV	HD6417760BP200ADV	Pb free solder.

2. Fixed Bugs

"A Mask" products fixed following 4 points :

2.1 USB Host Controller Incorrect Disconnection Detection

[Outline]

SH7760 USB Host Controller detects SE0(*1) incorrectly in Full Speed communicating, and consequently it may detect a device disconnect event in spite of NOT disconnected.

(*1) : SE0

USB transmission is proceeded with D+/D- differential signals, and the D+/D- are opposite signal levels each other in ordinary. And for a special case, both D+/D-: "Low" status is defined as SE0. USB Host Controller detects a device disconnection event when it detected SE0 for a certain period(2.5μsec) or more.

[Resolution]
(1) Please use Low speed(1.5Mbps) mode. At Low Speed mode, incorrect disconnection detection does not occur.
(2) At Full Speed (12Mbps) mode, please work around the following a) or b) to avoid the incorrect detection.
a) Cross over voltage level of D+, D- from USB Function Device shall be more than SH7760 V_{DDQ} x 0.65 (V).
b) "0" shall not continue more than 28 bits in a received data packet (*2).

(*2) : "0" bit series should be counted in all bits of the packet,
SYNC + PID + DATA + CRC16 + EOP
counting EOP as 2 bits.

[Modification Result]
HD6417760BP200AD/ADV : Because this bug was fixed, there is no need to apply the resolution .

2.2 Modification for the Restrictions Related to HAC

HD6417760BP200AD/ADV also fixed "25.5.5 Restrictions Related to HACTCR.CMDAMT", which was described in the SH7760 Hardware manual Rev 1.0.

+ About Section 25.5.5 (1) "Writing a codec register address to HACCSAR" :
[Text of Hardware manual Rev 1.0]
Write a codec register address to HACCSAR twice with an interval of 100ns(*3)
((*3):Waiting time can be set from 90nsec to 20µsec.)

[Modification Result]
HD6417760BP200AD/ADV : There is no need to apply this restriction. Please see Figure 1 and 2.

+ About Section 25.5.5 (2) Writing data to a codec register
[Text of Hardware manual Rev 1.0]
After writing data to a codec register, verify the write data by reading this codec register. If the write is unsuccessful, carry out writing again.

[Modification Result]
HD6417760BP200AD/ADV : There is no need to apply this restriction.

+ About Section 25.5.5 (3) Reading from a codec register

[Text of Hardware manual Rev 1.0]

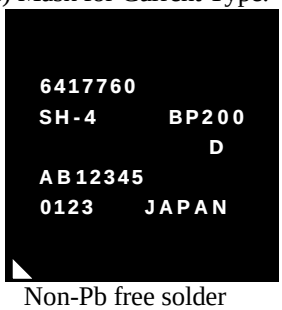
When HACTSR.CMDAMT is accidentally set to 1, a read access to the codec register is not performed and therefore neither HACRSR.STARY nor HACRSR.STDRY is set to 1 to indicate data reception. If HACRSR.STARY and HACRSR.STDRY stay 0 for a longer time than expected in normal read operation, it should be regarded as timeout. Carry out reading again.

[Modification Result]

HD6417760BP200AD/ADV : There is no need to apply this restriction.

3. Marking Specification

(1) Mask for Current Type.



Non-Pb free solder

Pb free solder

(2) Mask for New Type (Mask A).

Non-Pb free solder

Pb free solder

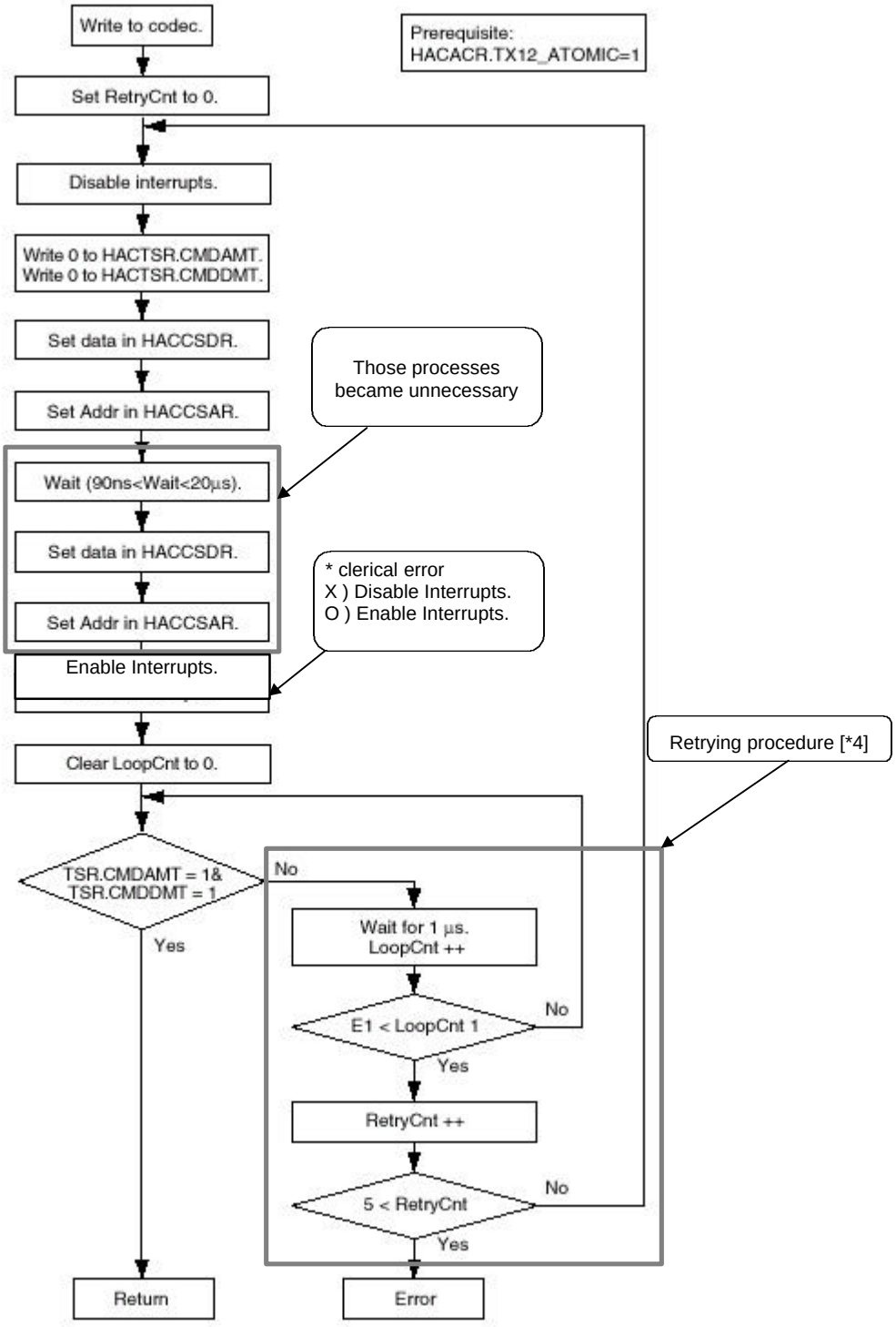


Figure 1. Modification for Figure 25.4 in Hardware Manual Rev 1.0

(*4) : Some CODEC devices may not complete accessing CODEC register within 1 slot time.
In this case, please execute this retrying procedure.

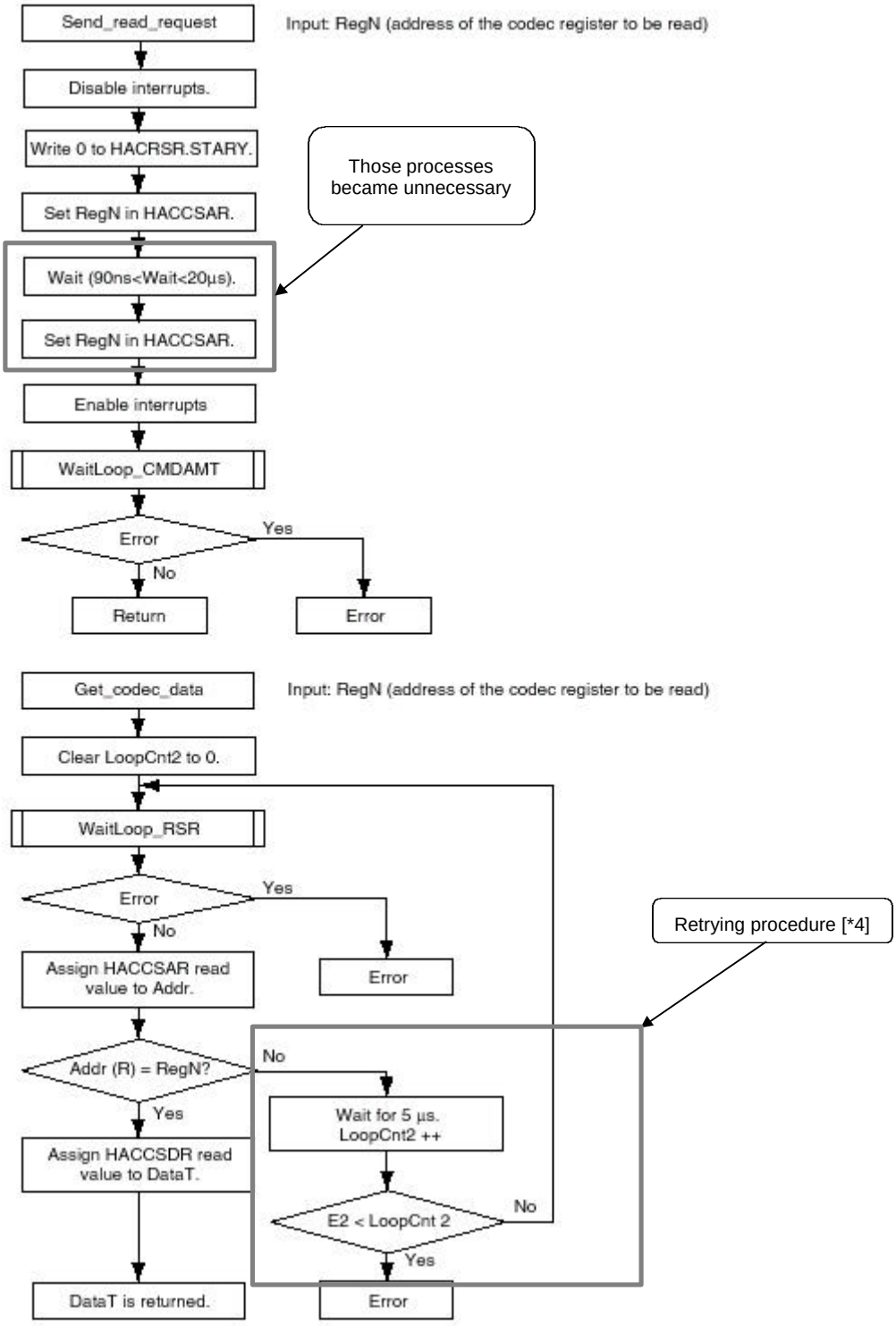


Figure 2. Modification for Figure 25.6 in Hardware Manual Rev 1.0