SH7000 Series

Remainder of 32 Bit ÷ 32 Bit (Unsigned)

Label: DIVU32R

Functions Used: DIV0U Instruction
DIV1 Instruction

Contents

1. Function

Divides the dividend (unsigned 32 bits) by the divisor (unsigned 32 bits), and determines the remainder (unsigned 32 bits). Also indicates errors (division by 0) in the T bit.

2. Arguments

Description		Storage Location	Data Length (Bytes)
Input	Dividend (unsigned 32 bits)	R1	4
	Divisor (unsigned 32 bits)	R0	4
Output	Remainder (unsigned 32 bits)	R2	4
	Error (division by 0) generated/not generated (generated: T = 1, not generated: T = 0)	T bit (SR)	4

3. Internal Register Changes and Flag Changes

	(Before Execution) → (After Execution)
R0	Divisor (unsigned 32 bits) → No change
R1	Dividend (unsigned 32 bits) → Change
R2	Undefined → Remainder (unsigned 32 bits)
R3	
R4	
R5	
R6	
R7	
R8	
R9	
R10	
R11	
R12	
R13	
R14	
R15	(SP)

T bit | * |

— : No change
* : Change
0 : Fixed 0
1 : Fixed 1

4. Programming Specifications

Program memory (bytes)
148
Data memory (bytes)
0
Stack (bytes)
0
Number of states
74
Reentrant
Yes
Relocation
Yes
Intermediate interrupt
Yes

5. Notes

The number of states indicated in the programming specifications is the value when H'FFFFFFFF ÷ H'FFFFFFFE is calculated.

6. Description

(1) Function

Details of the arguments are as follows.

R0: Set the divisor (unsigned 32 bits) as the input argument.

R1: Set the dividend (unsigned 32 bits) as the input argument.

R2: Holds the remainder (unsigned 32 bits) as the output argument.

T bit (SR): Indicates whether an error (division by 0) has occurred.
T bit = 1: Indicates an error (division by 0) has occurred.
T bit = 0: Indicates no error (division by 0) has occurred.

Figure 1 shows a software DIVU32R execution example.

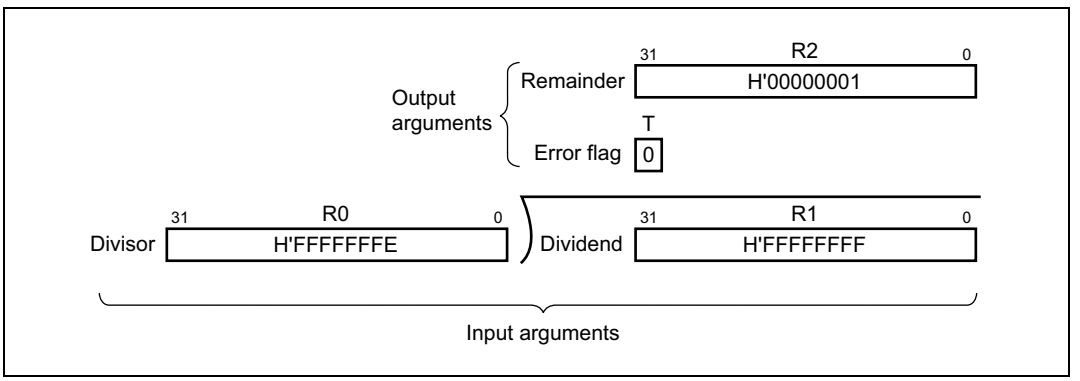


Figure 1 Software DIVU32R Execution Example

(2) Usage Notes

The value of R1, which is set to the dividend, is changed when software instruction DIVU32R is executed. If the value for the dividend will be needed after the software DIVU32R instruction is executed, it should be saved beforehand.

(3) RAM Used

No RAM is used by the software DIVU32R instruction.

(4) Usage Example

After the dividend and divisor are set in the input arguments, the software instruction DIVU32R is executed by a subroutine call.

```
          MOV.L   DATA1,R1     ... Sets dividend (unsigned 32 bits) in input argument (R1)
          BSR     DIVU32R      ... Subroutine call to software instruction DIVU32R
          MOV.L   DATA2,R0     ... Sets divisor (unsigned 32 bits) in input argument (R0)
          BT      ERROR        ... Branches to error processing subroutine if error (division by 0) occurs
                .
                .
                .
                .
        .align   4
DATA1   .data.l  H'FFFFFFFF
DATA2   .data.l  H'FFFFFFFE
```

(5) Operating Principle

(a) Before division, the following initial settings are carried out.

(i) R2 is used for the upper 32 bits to zero-extend the dividend to 64 bits. (Figure 2-(1))

(ii) The M, Q, and T bits used in one-step division are set to division values. (Figure 2-(2))

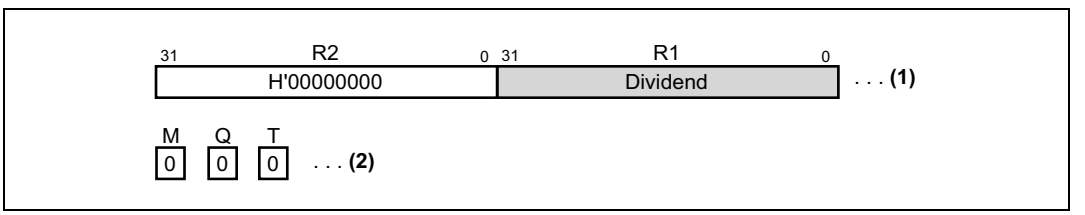


Figure 2 Initial Settings

(b) As shown in figure 3, the division operation is repeated through the number of divisor bits (32 times) using the ROCTL and DIV1 instructions.

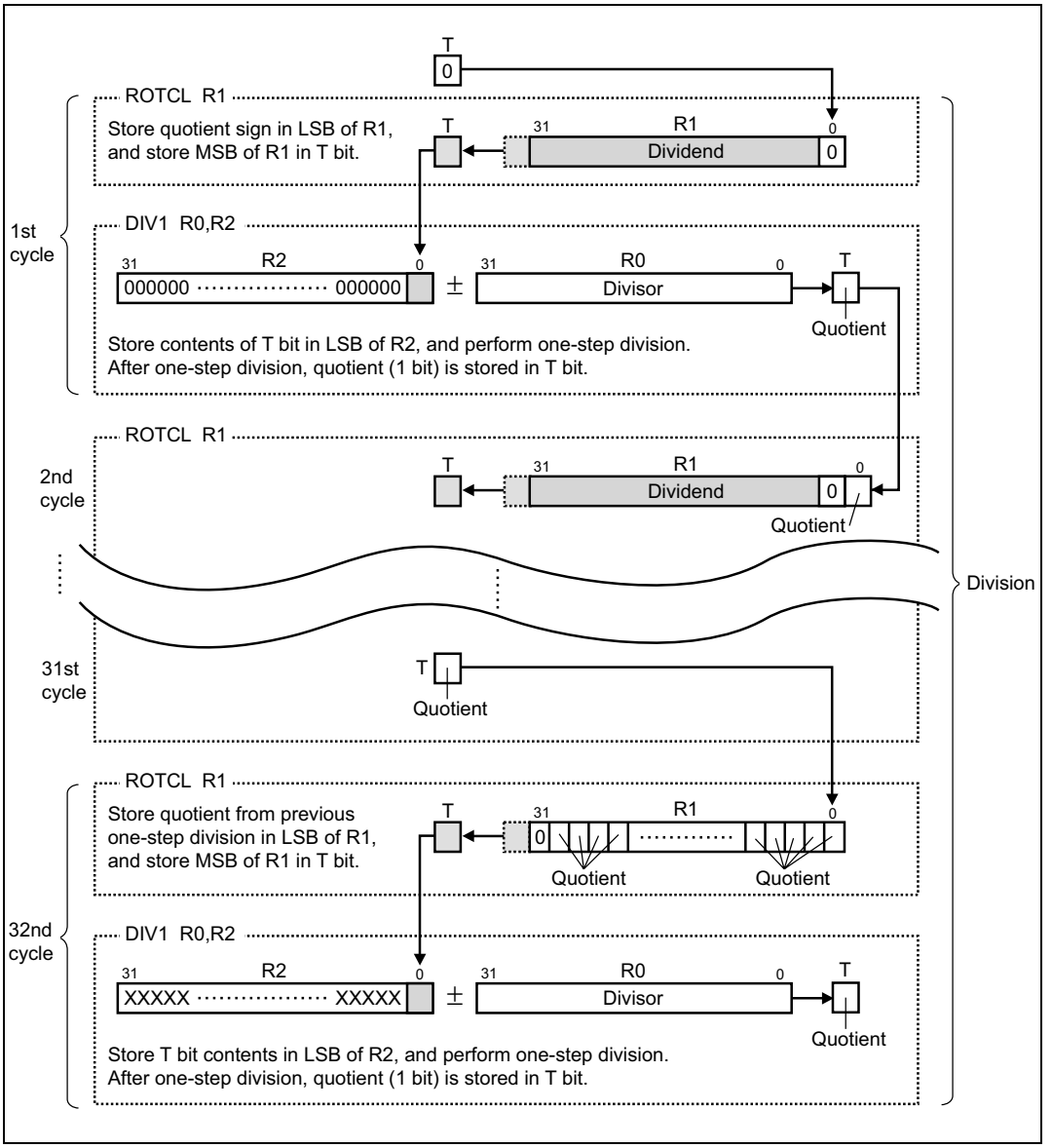


Figure 3 Division

(c) As shown in figure 4, the way of determining the remainder differs depending on the value of the T bit (quotient of 32nd one-step division) at the end of division.

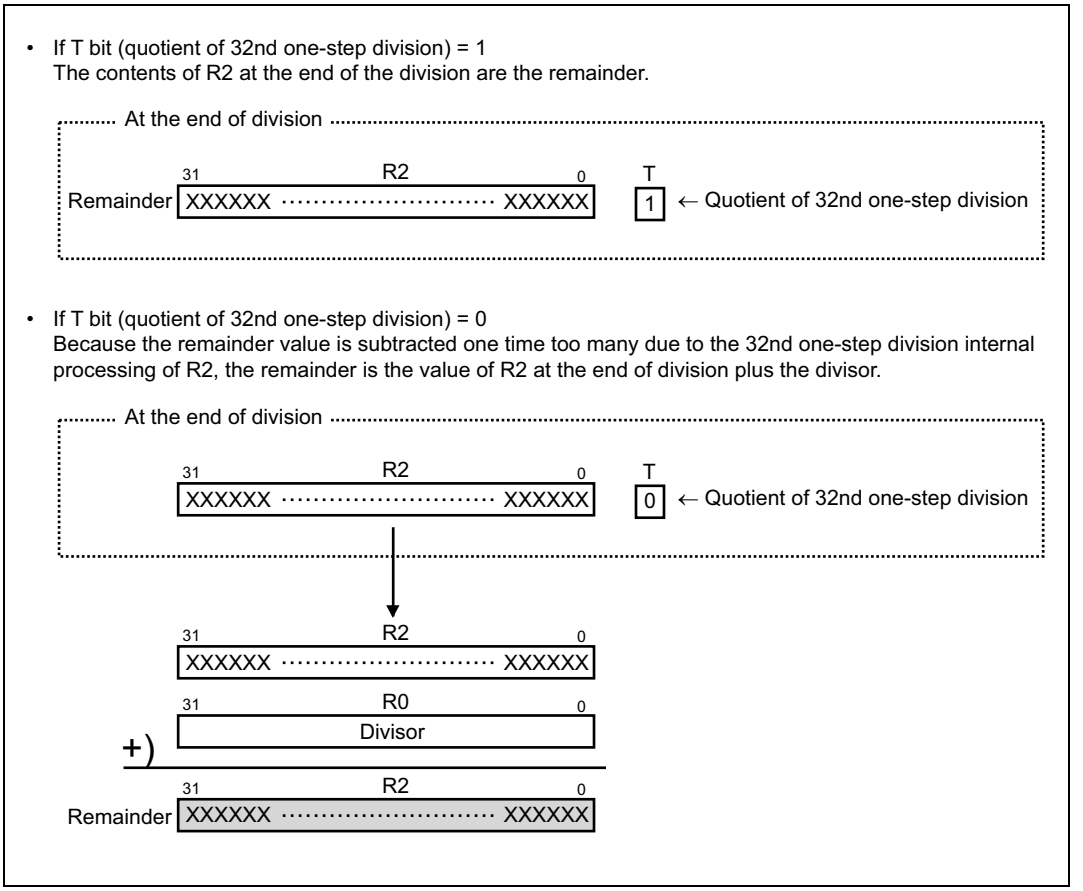
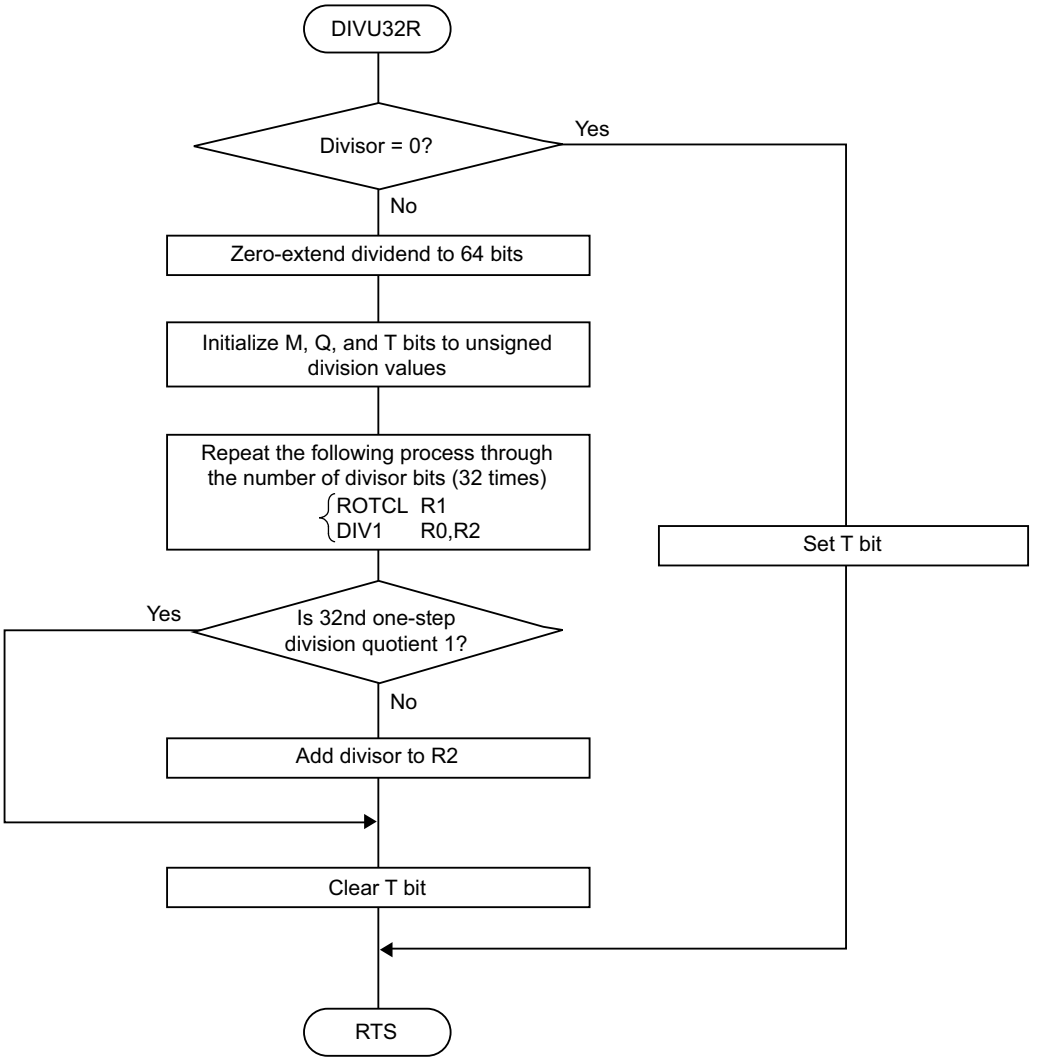


Figure 4 Remainder

7. Flowchart


DIVU32R
Divisor = 0?
Yes
No
Zero-extend dividend to 64 bits
Initialize M, Q, and T bits to unsigned division values
Repeat the following process through the number of divisor bits (32 times)
ROTCL R1
DIV1 R0,R2
Set T bit
Yes
Is 32nd one-step division quotient 1?
No
Add divisor to R2
Clear T bit
RTS

8. Program Listing

```
 1                          1  ;*************************************************************
 2                          2  ;*                                                           *
 3                          3  ;*      NAME ; RESIDUAL OF 32 BIT UNSIGNED DIVISION (DIVU32R) *
 4                          4  ;*                                                           *
 5                          5  ;*************************************************************
 6                          6  ;*                                                           *
 7                          7  ;*      ENTRY : R1 (DIVIDEND)                                *
 8                          8  ;*              R0 (DIVISOR)                                 *
 9                          9  ;*    RETURNS : R2 (RESIDUAL)                                *
10                         10  ;*              T BIT (ERROR -> TRUE;T=1,FALSE;T=0           *
11                         11  ;*                                                           *
12                         12  ;*************************************************************
13 00001000                13          .SECTION A,CODE,LOCATE=H'1000
14          00001000       14  DIVU32R .EQU    $           ; Entry point
15 00001000 2008           15          TST     R0,R0       ; Divisor = 0 ?
16 00001002 8945           16          BT      DIVU32R2    ; Yes
17 00001004 222A           17          XOR     R2,R2       ; R2 <- H'00000000
18 00001006 0019           18          DIV0U               ; Divide as unsigned
19                         19                              ;
20 00001008 4124           20          ROTCL   R1          ; Divide 1 step
21 0000100A 3204           21          DIV1    R0,R2       ;
22 0000100C 4124           22          ROTCL   R1          ;
23 0000100E 3204           23          DIV1    R0,R2       ;
24 00001010 4124           24          ROTCL   R1          ;
25 00001012 3204           25          DIV1    R0,R2       ;
26 00001014 4124           26          ROTCL   R1          ;
27 00001016 3204           27          DIV1    R0,R2       ;
28 00001018 4124           28          ROTCL   R1          ;
29 0000101A 3204           29          DIV1    R0,R2       ;
30 0000101C 4124           30          ROTCL   R1          ;
31 0000101E 3204           31          DIV1    R0,R2       ;
32 00001020 4124           32          ROTCL   R1          ;
33 00001022 3204           33          DIV1    R0,R2       ;
34 00001024 4124           34          ROTCL   R1          ;
35 00001026 3204           35          DIV1    R0,R2       ;
36                         36                              ;
37 00001028 4124           37          ROTCL   R1          ;
38 0000102A 3204           38          DIV1    R0,R2       ;
39 0000102C 4124           39          ROTCL   R1          ;
40 0000102E 3204           40          DIV1    R0,R2       ;
41 00001030 4124           41          ROTCL   R1          ;
42 00001032 3204           42          DIV1    R0,R2       ;
43 00001034 4124           43          ROTCL   R1          ;
44 00001036 3204           44          DIV1    R0,R2       ;
45 00001038 4124           45          ROTCL   R1          ;
46 0000103A 3204           46          DIV1    R0,R2       ;
47 0000103C 4124           47          ROTCL   R1          ;
48 0000103E 3204           48          DIV1    R0,R2       ;
49 00001040 4124           49          ROTCL   R1          ;
```

```
 50 00001042 3204          50          DIV1    R0,R2       ;
 51 00001044 4124          51          ROTCL   R1          ;
 52 00001046 3204          52          DIV1    R0,R2       ;
 53                        53                              ;
 54 00001048 4124          54          ROTCL   R1          ;
 55 0000104A 3204          55          DIV1    R0,R2       ;
 56 0000104C 4124          56          ROTCL   R1          ;
 57 0000104E 3204          57          DIV1    R0,R2       ;
 58 00001050 4124          58          ROTCL   R1          ;
 59 00001052 3204          59          DIV1    R0,R2       ;
 60 00001054 4124          60          ROTCL   R1          ;
 61 00001056 3204          61          DIV1    R0,R2       ;
 62 00001058 4124          62          ROTCL   R1          ;
 63 0000105A 3204          63          DIV1    R0,R2       ;
 64 0000105C 4124          64          ROTCL   R1          ;
 65 0000105E 3204          65          DIV1    R0,R2       ;
 66 00001060 4124          66          ROTCL   R1          ;
 67 00001062 3204          67          DIV1    R0,R2       ;
 68 00001064 4124          68          ROTCL   R1          ;
 69 00001065 3204          69          DIV1    R0,R2       ;
 70                        70                              ;
 71 00001068 4124          71          ROTCL   R1          ;
 72 0000106A 3204          72          DIV1    R0,R2       ;
 73 0000106C 4124          73          ROTCL   R1          ;
 74 0000106E 3204          74          DIV1    R0,R2       ;
 75 00001070 4124          75          ROTCL   R1          ;
 76 00001072 3204          76          DIV1    R0,R2       ;
 77 00001074 4124          77          ROTCL   R1          ;
 78 00001076 3204          78          DIV1    R0,R2       ;
 79 00001078 4124          79          ROTCL   R1          ;
 80 0000107A 3204          80          DIV1    R0,R2       ;
 81 0000107C 4124          81          ROTCL   R1          ;
 82 0000107E 3204          82          DIV1    R0,R2       ;
 83 00001080 4124          83          ROTCL   R1          ;
 84 00001082 3204          84          DIV1    R0,R2       ;
 85 00001084 4124          85          ROTCL   R1          ;
 86 00001086 3204          86          DIV1    R0,R2       ;
 87                        87                              ;
 88 00001086 8900          88          BT      DIVU32R1    ; T bit = 1 ?
 89 0000108A 320C          89          ADD     R0,R2       ; Clear oversub
 90 0000108C               90   DIVU32R1                   ;
 91 0000108C 000B          91          RTS                 ;
 92 0000108E 0008          92          CLRT                ; T bit <- No error
 93 00001090               93   DIVU32R2                   ;
 94 00001090 000B          94          RTS                 ;
 95 00001092 0018          95          SETTT               ; T bit <- Error
 96                        96          .END
*****TOTAL ERRORS    0
*****TOTAL WARNINGS  0
```

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