HITACHI MICROCOMPUTER TECHNICAL UPDATE

DATE	12 April 2000	No.	TN-SH7-224A/E
THEME	BSC WCR1 usage notice		
CLASSIFICATION	☐ Spec change ☐ Limitation on Use ■ Supplement of Documents		
PRODUCTNAME	HD6417750, HD6417750S	Lot No.etc.	All
REFERENCE DOCUMENTS	SH7750 Hardware Manual	Rev. 1 - 3	EffectiveDate Eternity From

1. Contents

If the related control bits of WCR1 are cleared to 0, no cycle is inserted between write access and MPX address output cycle of the following access (both read and write) to a different area.

Table1. Idle Insertion between Accesses

Following Cycle / Preceding Cycle	Same Area				Different Area				Same Area	Different Area
	Read		Write		Read		Write		MPX	MPX
	CPU	DMA	CPU	DMA	CPU	DMA	CPU	DMA	Address Output	Address Output
Read			M	M	M	M	M	M	M(1)	M(1)
Write					M	M	M	M	Note 2	M
DMA Read (memory→device)			M	M	M	M	M	M		M(1)
DMA Write (device→memory)	D	D	D	D*	D	D	D	D		D(1)

M, D : WCR1 wait insertion
(M(1) : One cycle inserted in MPX access even if WCR1 is cleared to 0)
M : Idle cycles are inserted by setting AnIW2-AnIW0 (area0 to area6)
D : Idle cycles are inserted by setting DMAIW2-DMAIW0
* : No insertion in consecutive accesses to the same device
In this table, “DMA” means DMA single address transfer. DMA dual address transfer case is same as “CPU”.

Notes: 1. When synchronous DRAM is used in RAS down mode, set bits DMAIW2-DMAIW0 to 000 and bits A3IW2-A3IW0 to 000.

Notes: 2. The condition that idle cycles are inserted between write access and MPX address output of the following access (both read and write) to the same area is as follows.

(a)Synchronous DRAM is used in RAS down mode,

(b)Internal DMAC accesses synchronous DRAM.

Idle cycles are inserted except in the above condition ((a) and (b)). If under the above condition, Idle cycles are occasionally inserted depending on the synchronous DRAM pipeline access internal status. If the related control bits of WCR1 are cleared to 0, no idle cycle is inserted between accesses. WCR1 is initialized to maximum cycles (15) by power-on-reset, so WCR1 should be set to an appropriate value.