HITACHI MICROCOMPUTER TECHNICAL UPDATE

DATE	5 November 2001	No.	TN-SH7-372A/E
THEME	Clock wiring between SH-4 and Synchronous DRAM		
CLASSIFICATION	☐ Spec change ☐ Limitation on Use ☑ Supplement of Documents		
PRODUCT NAME	SH7750, SH7750S		Lot No. etc. : All
REFERENCE DOCUMENTS	SH7750 series Hardware manual	Rev.	Effective Date
			Eternal

[Abstract] Clock wiring between SH-4 and Synchronous DRAM

SH-4 provides with interface capability which can be connected directly to Synchronous DRAM of 100MHz operation, but it is necessary to consider the proper PCB layout. When performing the mounting layout for wiring which connects SH-4 CKIO pin to Synchronous DRAM clock input pin, the following two items need to be considered.

1. Control clock distortion on the Synchronous DRAM receiving point, and make Synchronous DRAM normal operation.
2. Control clock distortion on the SH-4 sending point, and make the PLL circuit 2 normal operation.

As follows, examples for clock wiring are shown to satisfy these two items. Moreover, SH-4 has the CKIO2 pin to distribute the load. The direction of the pin is explained in Chapter 3.

[Contents]

1. To control clock distortion on the Synchronous DRAM receiving point, and make Synchronous DRAM normal operation

To transmit 100MHz clock signal which is drove by SH-4 CKIO pin to Synchronous DRAM properly, it needs to note for wiring system and its structure. As an example, Figure 1 shows SH-4 and Synchronous DRAM layout and clock wiring when four 16-bit width Synchronous DRAM are connected in parallel to SH-4 external bus. In this example, four-layer-board is used and two of the inside layers are assumed to be a power supply and a ground layer. But, clock wiring termination at the ending point using resistance etc. is not used. Main points are the following three points.

(1) Arrangement of SH-4 and Synchronous DRAM

SH-4 D0 to D63 pins are arranged on the both sides of chip centered on CKIO in 16 bits. Therefore, the compact arrangement and wiring can be done when four 16-bit width in Synchronous DRAM are arranged shown on Figure 1(four-layer-board is used). Here, two out of four Synchronous DRAM are mounted on the soldered side.

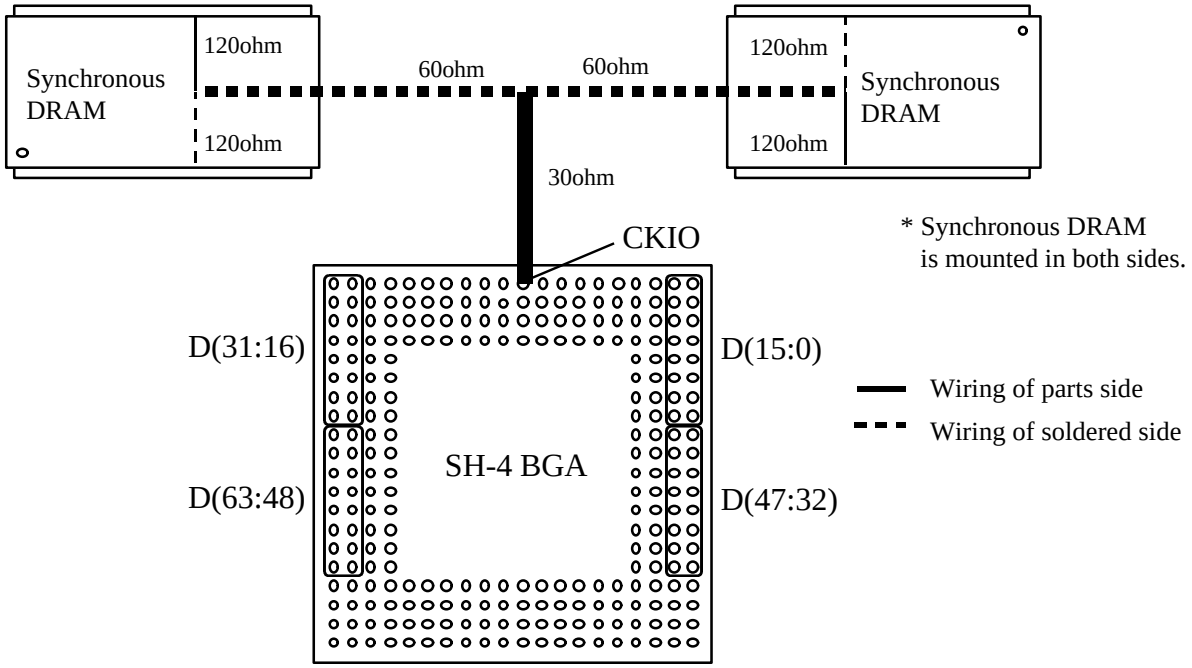

Figure 1: SH-4 and Synchronous DRAM layout and clock wiring example

(2) Matching between SH-4 output impedance and wiring characteristic impedance.

To control waveform distortion, in general, impedance matching should be taken at sending or ending point of wiring and signal multirefrection should be controlled. This example uses a method that match the characteristic impedance of wiring (reference value : 30ohm at rising edge / 10ohm at falling down) to SH-4 output impedance. This method has following advantages.

- Rising edge of signal became sharp because the characteristic impedance of wiring with 100ohm or more can decrease to 30ohm even regular four-layer PCB 1.6mm in thickness.
- Additional parts for the impedance matching are not needed at all.

Concrete impedance value is decided by the following method. First, the wiring characteristic impedance between CKIO and a turning point is matched to 30ohm, which is output impedance at the time for SH-4 rising edge. Then, it makes the characteristic impedance twice about 60ohm after branch to avoid impedance mismatch at the turning point. As the same reason, it is matched to 120ohm after the second branch. Figure 1 shows clock wiring and characteristic impedance value for every branch wiring.

Impedance for each branch wiring is matched by changing wiring width for each branch wiring.

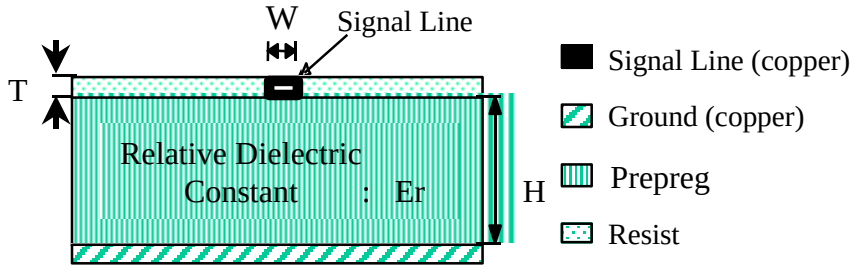

Figure 2: Microstrip Wiring Length Structure

Case of Microstrip wiring is shown by Figure 2. Assuming the wiring characteristic impedance Z_o is possible to disregard resist, the following equation is shown(*1).

$$Z_0 = \frac{87}{\sqrt{E_r + 1.414}} \ln\left(\frac{5.98H}{0.8W + T}\right)$$

It is understood that the parameter which can be matched to each branch wiring is only W, because Er, H and T are constant by the entire PCB in variables of the above equation. Moreover, characteristic impedance which includes the influence of resist or wiring characteristic impedance which has structures excluding Microstrip can calculate at a variety of emulators (Apsim/ RLGC(*2), Avant!/Star-HSPECE(*3) and etc.).

(3) Equal-Length Wiring

The termination at Synchronous DRAM receiving point is not used, because the impedance is matched at SH-4 sending point in this example. Therefore, the reflection is generated at four Synchronous DRAM receiving points; however, these reflected waves are in phase with at the turning point and return to SH-4 sending point due to equal-length of branch wiring. The reflection does not occur again, because output impedance and wiring characteristic impedance are matched at SH-4 sending point. Equal-length wiring should be within 1mm accuracy in the error despite the length of clock wiring.

* Impedance matching and equal-length wiring which mentioned previously is effective only when executing at the same time.

2. To control clock distortion on SH-4 sending point and make PLL circuit 2 normal operation

SH-4 feeds back the clock output from CKIO to an internal PLL circuit 2 in order to match the phase of internal bus clock (B phi) and CKIO. CKIO needs to have single integrity not only at receiving point, but also at SH-4 sending point. Especially, a stepped voltage waveform at SH-4 sending point has possibility to disturb the operation stability of PLL circuit. To control the stepped waveform, reflected wave from receiving point should be nestled into clock rise time or fall time. Assuming that clock rise time/fall time is t , and signal propagation speed is v, CKIO wiring length l (distance between CKIO and the furthest receiving point) needs to satisfy the following equation.

$$\frac{2\boldsymbol{l}}{\boldsymbol{v}} < t$$

Because minimum value of t is to be 0.7ns for SH-4, the allowed wiring length l should be about 56mm assuming v is about 160mm/ns which is simulation value for this board (simulator is Apsim/RLGC(*2)).

3. Direction for the use of CKIO2

SH-4 provides with CKIO2 pin to reduce the load of CKIO. For the difference of these pins, CKIO2 output is not fed back while CKIO output is fed back to PLL circuit 2. Therefore, it is guaranteed to match the phase of CKIO and internal bus clock (B phi), but not guaranteed to match the phase of CKIO2 and (B phi). Please note the following matter when CKIO/CKIO2 is connected to a device such as Synchronous DRAM which need to match the phase of B phi.

- Please connect to CKIO when you need only one within CKIO and CKIO2.
- Please adjust for the load of CKIO and CKIO2 to be equal, when you use CKIO and CKIO2 and need to match the phase of B phi and CKIO2.

Reference: CKIO and CKIO2 output block diagram is shown in “SH7750 series Hardware Manual, Appendix D”

4. Workaround on the PCB

When PCB may not be designed with the above clock pattern method, there may be the following 2 problems.

(1) The clock waveform on the Synchronous DRAM receiving point may be distorted.
(The impedance is unmatched on the CKIO line.)
(2) The PLL circuit2 may not oscillate correctly by the distortion of the CKIO on the SH-4 sending point.

If the dumping resistance can be inserted to the CKIO line near the CKIO sending point , it can be achieved to avoid the above problem.
The recommended value of the dumping resistance is form 20ohm to 40ohm, because the reference value of the CKIO output impedance is 30ohm.
The best value for the PCB depends on the pattern or the load condition, so the value should be selected to avoid a stepped voltage waveform at the sending point near the threshold voltage (Vddq/2) .

5. Reference Document

(*1) Mark I. Montrose, Printed Circuit Board Design Techniques for EMC Compliance,
Chapter4: IEEE Press
(*2) http://www.edac.org/Apsim/rlgc.html
(*3) http://www.avanticorp.com/pdt/hspice.pdf