Date: Mar.22.2004

RENESAS TECHNICAL UPDATE

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan RenesasTechnology Corp.

Product Category	MPU&MCU		Document No.	TN-SH7-518A/EA	Rev.	1.0
Title	Watchdog Timer may cause an illegal manual reset		Information Category	Usage Limitation		
Applicable Product	SH7750 SH7750S SH7751	Lot No.	Reference Document	SH7750 series hardware manual (ADE-602-124) SH7751 series hardware manual (ADE-602-201)		

Watchdog Timer (WDT) may cause an illegal manual reset. The condition and the workaround are described below.

1. Condition

When the following conditions 1 – 4 are satisfied at the same time, the WDT may cause an illegal manual reset.

- 1. After the WDT overflows regardless of the WT/IT# bit's and RSTS bit's value in WTCSR register.
- 2. Before the watchdog counter (WTCNT) is counted up according to the CKS bits in WTCSR register.
- 3. At least one of the TME bit, WT/IT# bit and RSTS bit in WTCSR register is 0.
- 4. The TME bit, WT/IT# bit and RSTS bit in WTCSR register are all set to 1.

2. Workaround

It is possible to avoid this problem to count up the WTCNT register prior to writing all 1 value to the TME bit, WT/IT# bit and RSTS bit in WTCSR register. The sample program is described below.

Sample: Insert the following program before the TME bit, WT/IT# bit and RSTS bit in WTCSR register are all set to 1.

MOV.L #WTCNT,R7 MOV.W #H'5A00,R8 MOV.W R8,@R7

MOV.L #WTCSR,R9 MOV.W #H'A580,R10 MOV.W R10,@R9

LOOP_WDT:

MOV.B @R7,R0 CMP/EQ #H'00, R0 BT LOOP_WDT

