date: 2002/09/11

## HITACHI SEMICONDUCTOR TECHNICAL UPDATE

Classification of Production	MPU			No	TN-SH7-424A/E	Rev	1
ТНЕМЕ	SH7751/SH7751R MD pin status		Classification of Information	<ol> <li>Spec change</li> <li>Supplement of Documents</li> <li>Limitation of Use</li> <li>Change of Mask</li> <li>Change of Production Line</li> </ol>			
PRODUCT NAME	SH7751, SH7751R	Lot No	Reference Documents			tive Date	

There are notes about MD9 and MD10 pins in Appendix D Pin Functions in the SH7751 series hardware manual. Please refer the following tables.

Table D.2. Pin States in Reset, Power-Down State, and Bus-Released State (PCI Enable)

Pin name	I/O	Reset(Power on)	
		HOST	non HOST
PCIREQ2#/MD9	I/O	I*19	I *19
PCIREQ3#/MD10	I/O	I *19	I *19

<sup>\*19:</sup>Pullup by on-chip pullup resistor. Note that this cannot be used for pullup of the mode pin during a power-on reset. Pullup or pulldown should be performed externally to the SH-4.

Table D.3. Pin States in Reset, Power-Down State, and Bus-Released State (PCI Disable)

Pin name	I/O	Reset(Power on)
PCIREQ2#/MD9	I/O	I *19
PCIREQ3#/MD10	I/O	I *19

<sup>\*19:</sup>Pullup by on-chip pullup resistor. Note that this cannot be used for pullup of the mode pin during a power-on reset. Pullup or pulldown should be performed externally to the SH-4.