

# RENESAS TECHNICAL UPDATE

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Product Category	Development Environment		Document No.	TN-CSX-057A/EA	Rev.	1.0
Title	Update of the SuperH™ RISC engine C/C++ Compiler Package Ver. 7.1.04		Information Category	Specification Change		
Applicable Product	P0700CAS7-MWR P0700CAS7-SLR P0700CAS7-H7R	Lot No.	Reference Document	SuperH RISC engine C/C++ Compiler, Assembler, Optimizing Linkage Editor User's Manual ADE-702-372A Rev.2.0		
		Ver. 7.x				

We have updated the SuperH™ RISC engine C/C++ compiler package to be Ver. 7.1.04. For details on this update, see P0700CAS7-031113E attached to this technical update.

If you have the compiler package of the Windows® version, download the update tool from the following URL:  
<http://www.renesas.com/eng/products/mpumcu/tool/index.html>

If you have the compiler package of the UNIX version, request an update to an authorized product distributor.

Attached document: P0700CAS7-031113E  
SuperH™ RISC engine C/C++ Compiler Package Ver. 7.1.04 Update

## **SuperH™ RISC engine C/C++ Compiler Package Ver. 7.1.04 Update**

We have updated the SuperH™ RISC engine C/C++ compiler to be Ver. 7.1.04.

Details on this update (problems fixed) are listed below.

Note, however, that section 1, and 3 only apply to the compiler package of the Windows® version.

### **1. High-performance Embedded Workshop**

#### **1.1 HEW Network Database Message Box on Windows® Me**

Display of the network database error message box on Windows® Me is prevented.

#### **1.2 Addition and Modification for Data Generated by the Project Generator**

The I/O definition file (iodefine.h) of the following CPUs has been modified:

SH7020, SH7021, SH7032, SH7034, SH7040, SH7041, SH7042, SH7043, SH7044, SH7045, SH7052, SH7055F, SH7144 (F), SH7145 (F), SH7604, SH7615, SH7616, SH7705, SH7706, SH7707, SH7709, SH7709A, SH7709S, SH7727, SH7729R, SH7750, and SH7751

### **2. Compiler**

#### **2.1 Fixed Problems Listed in SuperH RISC engine C/C++ Compiler ver.7 Failures Found in This Release (9)**

For details, refer to the technical update TN-CSX-054A.

#### **2.2 Fixed Problems Listed in SuperH RISC engine C/C++ Compiler ver.7 Failures Found in This Release (10)**

For details, refer to the technical update TN-CSX-056A.

### **3. SuperH™ RISC engine Simulator/Debugger**

#### **3.1 Fixed Problem Regarding the Little Endian (SH3-DSP, SH3-DSP (Core), and SH4AL-DSP)**

When little endian is in use, displaying the X/Y memory contents in 8-byte units causes the byte order to be incorrect.

#### **3.2 Fixed Problem Regarding an LDRC Instruction (SH3-DSP (Core))**

If instructions LDRE @ (disp,PC) and LDRC have been executed in this order, the least significant bit of the RE register will not be 1 when EX of LDRC and WB of LDRE are executed at the same time.

#### **3.3 Fixed Problem Regarding a Repeat (SH3-DSP (Core))**

If a DSP stall occurs when the instruction at the address eight bytes ahead from the top of a repeat is fetched, a compatible repeat that has four instructions or more will not work correctly.

### 3.4 Fixed Problem Regarding Delayed Slot Instructions (SH-4, SH-4 with BSC, and SH-4 (SH7750R))

Stepping in instruction units will not be completed when a double-precision FMUL instruction is placed at the slot of a delayed branch instruction.