SH7000 Series

64 Bit + 64 Bit = 64 Bit (Unsigned)

Label: ADDU64

Functions Used: ADDC Instruction

Contents

1. Function

Adds the augend (unsigned 64 bits) and addend (unsigned 64 bits), and determines the sum (unsigned 64 bits). At this time, whether or not any carry is generated is set in the T bit.

2. Arguments

Description		Storage Location	Data Length (Bytes)
Input	Upper 32 bits of augend (unsigned 64 bits)	R0	4
	Lower 32 bits of augend (unsigned 64 bits)	R1	4
	Upper 32 bits of addend (unsigned 64 bits)	R2	4
	Lower 32 bits of addend (unsigned 64 bits)	R3	4
Output	Upper 32 bits of sum (unsigned 64 bits)	R0	4
	Lower 32 bits of sum (unsigned 64 bits)	R1	4
	With/without carry (with: T = 1, without: T = 0)	T bit (SR)	4

3. Internal Register Changes and Flag Changes

	(Before Execution) → (After Execution)
R0	Upper 32 bits of augend → Upper 32 bits of sum
R1	Lower 32 bits of augend → Lower 32 bits of sum
R2	Upper 32 bits of addend → No change
R3	Lower 32 bits of addend → No change
R4	
R5	
R6	
R7	
R8	
R9	
R10	
R11	
R12	
R13	
R14	
R15	(SP)

T bit | * |

— : No change
* : Change
0 : Fixed 0
1 : Fixed 1

4. Programming Specifications

Program memory (bytes)
8
Data memory (bytes)
0
Stack (bytes)
0
Number of states
5
Reentrant
Yes
Relocation
Yes
Intermediate interrupt
Yes

5. Description

(1) Function

Details of the arguments are as follows.

R0: Set the upper 32 bits of the augend (unsigned 64 bits) as the input argument.
Holds the upper 32 bits of the sum (unsigned 64 bits) as the output argument.

R1: Set the lower 32 bits of the augend (unsigned 64 bits) as the input argument.
Holds the lower 32 bits of the sum (unsigned 64 bits) as the output argument.

R2: Set the upper 32 bits of the addend (unsigned 64 bits) as the input argument.

R3: Set the lower 32 bits of the addend (unsigned 64 bits) as the input argument.

T bit (SR): Indicates the presence or absence of a carry after execution of the software instruction ADDU64.
T bit = 1: Indicates a carry was generated.
T bit = 0: Indicates no carry was generated.

Figure 1 shows a software ADDU64 execution example.

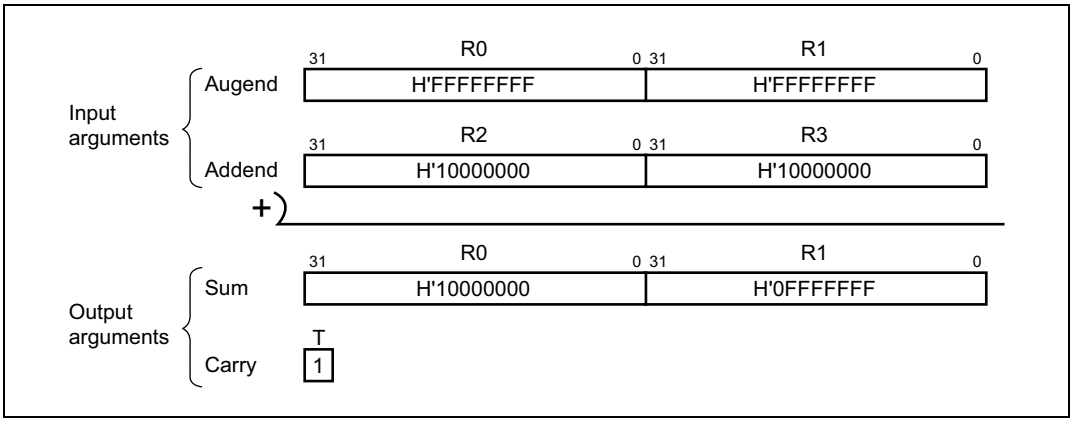


Figure 1 Software ADDU64 Execution Example

(2) Usage Notes

Since the sum is set in R1 and R2, which contained the augend settings, the augend data is destroyed. If the value for the augend will be needed after the software ADDU64 instruction is executed, it should be saved beforehand.

(3) RAM Used

No RAM is used by the software ADDU64 instruction.

(4) Usage Example

After the augend and addend are set in input arguments, the software instruction ADDU64 is executed by a subroutine call.

```
        MOV.L   DATA1,R0     .... Sets augend (upper 32 bits) in input argument
        MOV.L   DATA2,R1     .... Sets augend (lower 32 bits) in input argument
        MOV.L   DATA3,R2     .... Sets addend (upper 32 bits) in input argument
        BSR     ADDU64       .... Subroutine call to ADDU64
        MOV.L   DATA4,R3     .... Sets addend (lower 32 bits) in input argument
        BT      ERROR        .... Branches to error-processing subroutine if carry occurs
              .
              .
              .
              .
      .align    4
DATA1 .data.l   H'FFFFFFFF
DATA2 .data.l   H'FFFFFFFF
DATA3 .data.1   H'10000000
DATA4 .data.1   H'10000000
```

(5) Operating Principle

As shown in figure 2, the add with carry instruction (ADDC) is used repeatedly to perform addition in 32-bit units, starting from the LSB.

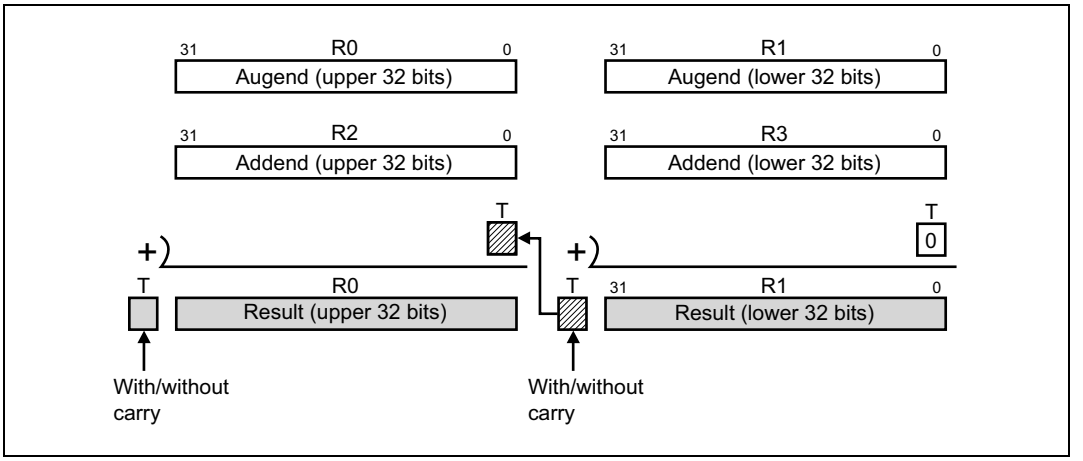
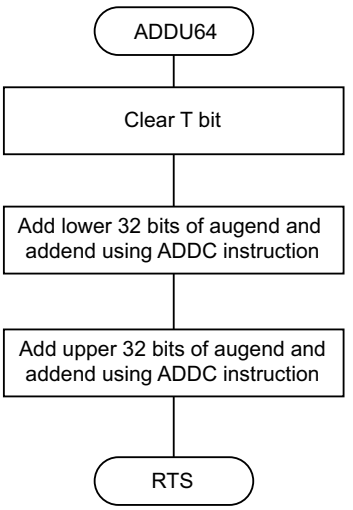


Figure 2 Unsigned Addition

6. Flowchart



7. Program Listing

```
 1                      1   ;*************************************************************
 2                      2   ;*                                                           *
 3                      3   ;*        NAME ; 64 BIT UNSIGNED BINARY ADDITION (ADDU64)    *
 4                      4   ;*                                                           *
 5                      5   ;*************************************************************
 6                      6   ;*                                                           *
 7                      7   ;*      ENTRY : R0    (UPPER 32 BIT AUGEND)                  *
 8                      8   ;*              R1    (LOWER 32 BIT AUGEND)                  *
 9                      9   ;*              R2    (UPPER 32 BIT ADDEND)                  *
10                     10   ;*              R3    (LOWER 32 BIT ADDEND)                  *
11                     11   ;*    RETURNS : R0    (UPPER 32 BIT SUM)                     *
12                     12   ;*              R1    (LOWER 32 BIT SUM)                     *
13                     13   ;*              T BIT (CARRY -> TRUE;T=1,FALSE;T=0)          *
14                     14   ;*                                                           *
15                     15   ;*************************************************************
16 00001000            16           .SECTION A,CODE,LOCATE=H'1000
17          00001000   17   ADDU64  .EQU    $               ; Entry point
18 00001000 0008       18           CLRT                    ; Clear T bit
19 00001002 313E       19           ADDC    R3,R1           ; Lower 32 bit augend + Lower
                                                            ; 32 bit addend
20 00001004 000B       20           RTS                     ;
21 00001006 302E       21           ADDC    R2,R0           ; Upper 32 bit augend + Upper
                                                            ; 32 bit addend
22                     22           .END
*****TOTAL ERRORS    0
*****TOTAL WARNINGS  0
```

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