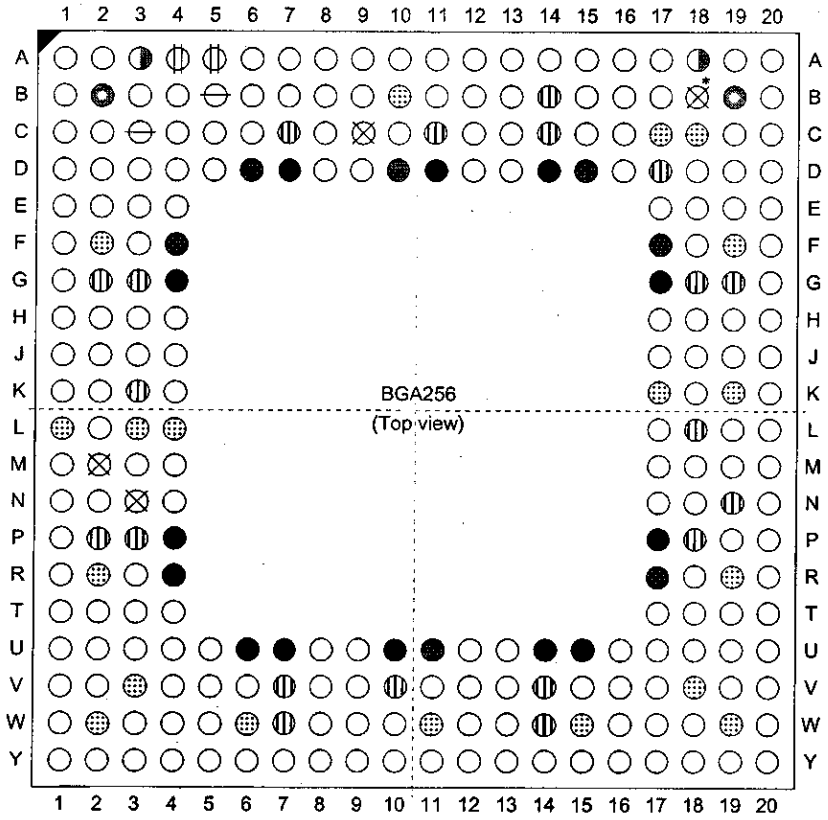
HITACHI MICROCOMPUTER TECHNICAL UPDATE

DATE	8 November 2001	No.	TN-SH7-376A/E
THEME	Amendment of the Pin Arrangement		
CLASSIFICATION	☐ Spec change ☐ Limitation on Use ■ Supplement of Documents		
PRODUCT NAME	SH7751		Lot No. etc. All
REFERENCE DOCUMENTS	SH7751 Hardware Manual	Rev.	Effective Date Eternity
		2.0	From

Please be advised that we revised the Pin Arrangement of BGA Package.

Please find attached amendment.



Note: Power must be supplied to the on-chip PLL power supply pins (VDD-PLL1, VDD-PLL2, VSS-PLL1, VSS-PLL2, VDD-CPG, VSS-CPG, VDD-RTC, and VSS-RTC) regardless of whether or not the PLL circuits, crystal resonator, and RTC are used.

* VSSQ also possible

Figure 1 Pin Arrangement (256-Pin BGA)

Table 1 Pin Functions

						Memory Interface				
No.	Pin Number	Pin Name	I/O	Function	Reset	SRAM	DRAM	SDRAM	PCMCIA	MPX
1	B3	TMS	I	Mode (H-UDI)						
2	C4	TCK	I	Clock (H-UDI)						
3	G3	VDDQ	Power	IO VDD						
4	F2	VSSQ	Power	IO GND						
5	D4	TDI	I	Data in (H-UDI)						
6	B1	$\overline{\text{CS0}}$	O	Chip select 0		$\overline{\text{CS0}}$				$\overline{\text{CS0}}$
7	C2	$\overline{\text{CS1}}$	O	Chip select 1		$\overline{\text{CS1}}$				$\overline{\text{CS1}}$
8	C1	$\overline{\text{CS4}}$	O	Chip select 4		$\overline{\text{CS4}}$				$\overline{\text{CS4}}$
9	D3	$\overline{\text{CS5}}$	O	Chip select 5		$\overline{\text{CS5}}$			$\overline{\text{CE1A}}$	$\overline{\text{CS5}}$
10	D2	$\overline{\text{CS6}}$	O	Chip select 6		$\overline{\text{CS6}}$			$\overline{\text{CE1B}}$	$\overline{\text{CS6}}$
11	D1	$\overline{\text{BS}}$	O	Bus start		($\overline{\text{BS}}$)	($\overline{\text{BS}}$)	($\overline{\text{BS}}$)	($\overline{\text{BS}}$)	($\overline{\text{BS}}$)
12	E4	$\overline{\text{WE0}}$/ $\overline{\text{REG}}$	O	D7–D0 select signal		$\overline{\text{WE0}}$			$\overline{\text{REG}}$	
13	E3	$\overline{\text{WE1}}$	O	D15–D8 select signal		$\overline{\text{WE1}}$			$\overline{\text{WE1}}$	
14	E2	D0	I/O	Data						A0
15	G2	VDDQ	Power	IO VDD						
16	L4	VSSQ	Power	IO GND						
17	G4	VDD	Power	Internal VDD						
18	F4	VSS	Power	Internal GND						
19	E1	D1	I/O	Data						A1
20	F3	D2	I/O	Data						A2
21	F1	D3	I/O	Data						A3
22	G1	D4	I/O	Data						A4
23	H4	D5	I/O	Data						A5
24	H3	D6	I/O	Data						A6
25	H2	D7	I/O	Data						A7
26	H1	D8	I/O	Data						A8
27	J4	D9	I/O	Data						A9

Table 1 Pin Functions (cont)

						Memory Interface				
No.	Pin Number	Pin Name	I/O	Function	Reset	SRAM	DRAM	SDRAM	PCMCIA	MPX
28	J3	D10	I/O	Data						A10
29	K3	VDDQ	Power	IO VDD						
30	L3	VSSQ	Power	IO GND						
31	J2	D11	I/O	Data						A11
32	J1	D12	I/O	Data						A12
33	K4	D13	I/O	Data						A13
34	K2	D14	I/O	Data						A14
35	K1	D15	I/O	Data						A15
36	L2	$\overline{\text{CAS0}}$/ DQM0	O	D7–D0 select signal			$\overline{\text{CAS0}}$	DQM0		
37	M4	$\overline{\text{CAS1}}$/ DQM1	O	D15–D8 select signal			$\overline{\text{CAS1}}$	DQM1		
38	M3	RD/$\overline{\text{WR}}$	O	Read/write			RD/$\overline{\text{WR}}$	RD/$\overline{\text{WR}}$		RD/$\overline{\text{WR}}$
39	M1	CKIO	O	Clock output				CKIO		
40	M2	NC		Do not connect						
41	P3	VDDQ	Power	IO VDD						
42	L1	VSSQ	Power	IO GND						
43	N3	NC		Do not connect						
44	P1	$\overline{\text{RD}}$/ $\overline{\text{CASS}}$/ $\overline{\text{FRAME}}$	O	Read/$\overline{\text{CAS}}$/ $\overline{\text{FRAME}}$		$\overline{\text{OE}}$		$\overline{\text{CAS}}$	$\overline{\text{OE}}$	$\overline{\text{FRAME}}$
45	N2	CKE	O	Clock output enable				CKE		
46	N1	$\overline{\text{RAS}}$	O	$\overline{\text{RAS}}$			$\overline{\text{RAS}}$	$\overline{\text{RAS}}$		
47	P4	VDD	Power	Internal VDD						
48	R4	VSS	Power	Internal GND						
49	N4	$\overline{\text{CS2}}$	O	Chip select 2		$\overline{\text{CS2}}$	($\overline{\text{CS2}}$)	$\overline{\text{CS2}}$		$\overline{\text{CS2}}$
50	R3	$\overline{\text{CS3}}$	O	Chip select 3		$\overline{\text{CS3}}$	($\overline{\text{CS3}}$)	$\overline{\text{CS3}}$		$\overline{\text{CS3}}$
51	R1	A0	O	Address						
52	T4	A1	O	Address						
53	T3	A2	O	Address						
54	T2	A3	O	Address						
55	P2	VDDQ	Power	IO VDD						

Table 1 Pin Functions (cont)

						Memory Interface				
No.	Pin Number	Pin Name	I/O	Function	Reset	SRAM	DRAM	SDRAM	PCMCIA	MPX
56	R2	VSSQ	Power	IO GND						
57	T1	A4	O	Address						
58	U4	A5	O	Address						
59	U3	A6	O	Address						
60	U2	A7	O	Address						
61	U1	A8	O	Address						
62	V2	A9	O	Address						
63	V1	A10	O	Address						
64	W1	A11	O	Address						
65	Y1	A12	O	Address						
66	Y2	A13	O	Address						
67	V7	VDDQ	Power	IO VDD						
68	V3	VSSQ	Power	IO GND						
69	W3	A14	O	Address						
70	Y3	A15	O	Address						
71	V4	A16	O	Address						
72	W4	A17	O	Address						
73	Y4	$\overline{\text{CAS2}}$/ DQM2	O	D23–D16 select signal			$\overline{\text{CAS2}}$	DQM2		
74	U5	$\overline{\text{CAS3}}$/ DQM3	O	D31–D24 select signal			$\overline{\text{CAS3}}$	DQM3		
75	V5	D16	I/O	Data						A16
76	W5	D17	I/O	Data						A17
77	Y5	D18	I/O	Data						A18
78	V6	D19	I/O	Data						A19
79	W7	VDDQ	Power	IO VDD						
80	W2	VSSQ	Power	IO GND						
81	U7	VDD	Power	Internal VDD						
82	U6	VSS	Power	Internal GND						
83	Y6	D20	I/O	Data						A20
84	Y7	D21	I/O	Data						A21
85	U8	D22	I/O	Data						A22
86	V8	D23	I/O	Data						A23

Table 1 Pin Functions (cont)

						Memory Interface				
No.	Pin Number	Pin Name	I/O	Function	Reset	SRAM	DRAM	SDRAM	PCMCIA	MPX
87	W8	D24	I/O	Data						A24
88	Y8	D25	I/O	Data						A25
89	U9	D26	I/O	Data						
90	V9	D27	I/O	Data						
91	W9	D28	I/O	Data						
92	Y9	D29	I/O	Data						ACCSIZE0
93	V10	VDDQ	Power	IO VDD						
94	W6	VSSQ	Power	IO GND						
95	W10	D30	I/O	Data						ACCSIZE1
96	Y10	D31	I/O	Data						ACCSIZE2
97	U10	VDD	Power	Internal VDD						
98	U11	VSS	Power	Internal GND						
99	V11	A18	O	Address						
100	Y11	A19	O	Address						
101	U12	A20	O	Address						
102	V12	A21	O	Address						
103	W12	A22	O	Address						
104	Y12	A23	O	Address						
105	V14	VDDQ	Power	IO VDD						
106	W11	VSSQ	Power	IO GND						
107	U13	A24	O	Address						
108	V13	A25	O	Address						
109	W13	$\overline{\text{WE2}}$/ $\overline{\text{ICIORD}}$	O	D23–D16 select signal		$\overline{\text{WE2}}$			$\overline{\text{ICIORD}}$	
110	Y13	$\overline{\text{WE3}}$/ $\overline{\text{ICIOWR}}$	O	D31–D24 select signal		$\overline{\text{WE3}}$			$\overline{\text{ICIOWR}}$	
111	U14	VDD	Power	Internal VDD						
112	U15	VSS	Power	Internal GND						
113	Y14	$\overline{\text{SLEEP}}$	I	Sleep						
114	V15	$\overline{\text{PCIGNT4}}$	O	Bus grant (host function)						
115	Y15	$\overline{\text{PCIGNT3}}$	O	Bus grant (host function)						

Table 1 Pin Functions (cont)

						Memory Interface				
No.	Pin Number	Pin Name	I/O	Function	Reset	SRAM	DRAM	SDRAM	PCMCIA	MPX
116	U16	$\overline{\text{PCIGNT2}}$	O	Bus grant (host function)						
117	V16	$\overline{\text{PCIREQ4}}$	I/O	Bus request (host function)						
118	W16	$\overline{\text{PCIREQ3}}$ /MD10	I/O	Bus request (host function)/ mode	MD10					
119	W14	VDDQ	Power	IO VDD						
120	W15	VSSQ	Power	IO GND						
121	Y16	$\overline{\text{PCIREQ2}}$ /MD9	I/O	Bus request (host function)/ mode	MD9					
122	U17	IDSEL	I	Configuration device select						
123	V17	$\overline{\text{INTA}}$	O	Interrupt (async)						
124	W17	$\overline{\text{PCIRST}}$	O	Reset output						
125	Y17	PCICLK	I	PCI input clock						
126	W18	$\overline{\text{PCIGNT1}}$ /$\overline{\text{REQOU}}$ $\overline{\text{T}}$	O	Bus grant (host function)/ bus request						
127	Y18	$\overline{\text{PCIREQ1}}$ /$\overline{\text{GNTIN}}$	I	Bus request (host function) /bus grant						
128	Y19	$\overline{\text{SERR}}$	I/O	System error						
129	Y20	AD31	I/O	PCI address/ data/port		(Port)	(Port)	(Port)	(Port)	(Port)
130	W20	AD30	I/O	PCI address/ data/port		(Port)	(Port)	(Port)	(Port)	(Port)
131	P18	VDDQ	Power	IO VDD						
132	V18	VSSQ	Power	IO GND						
133	V19	AD29	I/O	PCI address/ data/port		(Port)	(Port)	(Port)	(Port)	(Port)
134	V20	AD28	I/O	PCI address/ data/port		(Port)	(Port)	(Port)	(Port)	(Port)

Table 1 Pin Functions (cont)

No.	Pin Number	Pin Name	I/O	Function	Reset	Memory Interface				
						SRAM	DRAM	SDRAM	PCMCIA	MPX
135	U18	AD27	I/O	PCI address/ data/port		(Port)	(Port)	(Port)	(Port)	(Port)
136	U20	AD26	I/O	PCI address/ data/port		(Port)	(Port)	(Port)	(Port)	(Port)
137	T17	AD25	I/O	PCI address/ data/port		(Port)	(Port)	(Port)	(Port)	(Port)
138	T18	AD24	I/O	PCI address/ data/port		(Port)	(Port)	(Port)	(Port)	(Port)
139	U19	C/$\overline{BE3}$	I/O	PCI address/ data/port						
140	T20	AD23	I/O	PCI address/ data/port		(Port)	(Port)	(Port)	(Port)	(Port)
141	R18	AD22	I/O	PCI address/ data/port		(Port)	(Port)	(Port)	(Port)	(Port)
142	T19	AD21	I/O	PCI address/ data/port		(Port)	(Port)	(Port)	(Port)	(Port)
143	N19	VDDQ	Power	IO VDD						
144	W19	VSSQ	Power	IO GND						
145	P17	VDD	Power	Internal VDD						
146	R17	VSS	Power	Internal GND						
147	R20	AD20	I/O	PCI address/ data/port		(Port)	(Port)	(Port)	(Port)	(Port)
148	P20	AD19	I/O	PCI address/ data/port		(Port)	(Port)	(Port)	(Port)	(Port)
149	P19	AD18	I/O	PCI address/ data/port		(Port)	(Port)	(Port)	(Port)	(Port)
150	N20	AD17	I/O	PCI address/ data/port		(Port)	(Port)	(Port)	(Port)	(Port)
151	N17	AD16	I/O	PCI address/ data/port		(Port)	(Port)	(Port)	(Port)	(Port)
152	N18	C/$\overline{BE2}$	I/O	Command/ byte enable						
153	M20	$\overline{PCIFRAME}$	I/O	Bus cycle						
154	M19	$\overline{IRDY}$	I/O	Initiator ready						
155	M18	$\overline{TRDY}$	I/O	Target read						

Table 1 Pin Functions (cont)

						Memory Interface				
No.	Pin Number	Pin Name	I/O	Function	Reset	SRAM	DRAM	SDRAM	PCMCIA	MPX
156	M17	$\overline{\text{DEVSEL}}$	I/O	Device select						
157	L18	VDDQ	Power	IO VDD						
158	R19	VSSQ	Power	IO GND						
159	L20	$\overline{\text{PCISTOP}}$	I/O	Transaction stop						
160	L19	$\overline{\text{PCILOCK}}$	I/O	Exclusive access						
161	L17	PERR	I/O	Parity error						
162	K20	PAR	I/O	Parity						
163	K18	C/$\overline{\text{BE1}}$	I/O	Command/ byte enable						
164	J20	AD15	I/O	PCI address/ data/port		(Port)	(Port)	(Port)	(Port)	(Port)
165	J19	AD14	I/O	PCI address/ data/port		(Port)	(Port)	(Port)	(Port)	(Port)
166	J18	AD13	I/O	PCI address/ data/port		(Port)	(Port)	(Port)	(Port)	(Port)
167	J17	AD12	I/O	PCI address/ data/port		(Port)	(Port)	(Port)	(Port)	(Port)
168	H20	AD11	I/O	PCI address/ data/port		(Port)	(Port)	(Port)	(Port)	(Port)
169	G18	VDDQ	Power	IO VDD						
170	K17	VSSQ	Power	IO GND						
171	H19	AD10	I/O	PCI address/ data/port		(Port)	(Port)	(Port)	(Port)	(Port)
172	G20	AD9	I/O	PCI address/ data/port		(Port)	(Port)	(Port)	(Port)	(Port)
173	H18	AD8	I/O	PCI address/ data/port		(Port)	(Port)	(Port)	(Port)	(Port)
174	H17	C/$\overline{\text{BE0}}$	I/O	Command/ byte enable						
175	G17	VDD	Power	Internal VDD						
176	F17	VSS	Power	Internal GND						
177	F18	AD7	I/O	PCI address/ data/port		(Port)	(Port)	(Port)	(Port)	(Port)
178	F20	AD6	I/O	PCI address/ data/port		(Port)	(Port)	(Port)	(Port)	(Port)

Table 1 Pin Functions (cont)

No.	Pin Number	Pin Name	I/O	Function	Reset	Memory Interface				
						SRAM	DRAM	SDRAM	PCMCIA	MPX
179	E20	AD5	I/O	PCI address/ data/port		(Port)	(Port)	(Port)	(Port)	(Port)
180	E19	AD4	I/O	PCI address/ data/port		(Port)	(Port)	(Port)	(Port)	(Port)
181	E18	AD3	I/O	PCI address/ data/port		(Port)	(Port)	(Port)	(Port)	(Port)
182	D20	AD2	I/O	PCI address/ data/port		(Port)	(Port)	(Port)	(Port)	(Port)
183	G19	VDDQ	Power	I/O VDD						
184	K19	VSSQ	Power	I/O GND						
185	D19	AD1	I/O	PCI address/ data/port		(Port)	(Port)	(Port)	(Port)	(Port)
186	D18	AD0	I/O	PCI address/ data/port		(Port)	(Port)	(Port)	(Port)	(Port)
187	E17	$\overline{\text{IRL0}}$	I	Interrupt 0						
188	C20	$\overline{\text{IRL1}}$	I	Interrupt 1						
189	C19	$\overline{\text{IRL2}}$	I	Interrupt 2						
190	B20	$\overline{\text{IRL3}}$	I	Interrupt 3						
191	B18	NC*[6]		Do not connect						
192	D17	VDDQ	Power	I/O VDD						
193	A20	XTAL2	O	RTC crystal resonator pin						
194	A19	EXTAL2	I	RTC crystal resonator pin						
195	A18	VDD-RTC	Power	RTC VDD						
196	B19	VSS-RTC	Power	RTC GND						
197	B17	CA	I	Hardware standby						
198	A17	$\overline{\text{RESET}}$	I	Reset					$\overline{\text{RESET}}$	
199	C16	$\overline{\text{TRST}}$	I	Reset (H-UDI)						
200	B16	$\overline{\text{MRESET}}$	I	Manual reset						
201	D16	NMI	I	Nonmaskable interrupt						

Table 1 Pin Functions (cont)

						Memory Interface				
No.	Pin Number	Pin Name	I/O	Function	Reset	SRAM	DRAM	SDRAM	PCMCIA	MPX
202	A16	$\overline{\text{BACK}}$/ $\overline{\text{BSREQ}}$	O	Bus acknowledge/ bus request						
203	B15	$\overline{\text{BREQ}}$/ $\overline{\text{BSACK}}$	I	Bus request/bus acknowledge						
204	C15	MD6/ $\overline{\text{IOIS16}}$	I	Mode/$\overline{\text{IOIS16}}$ (PCMCIA)	MD6				$\overline{\text{IOIS16}}$	
205	A15	$\overline{\text{RDY}}$	I	Bus ready		$\overline{\text{RDY}}$			$\overline{\text{RDY}}$	$\overline{\text{RDY}}$
206	A14	TXD	O	SCI data output						
207	B14	VDDQ	Power	IO VDD						
208	F19	VSSQ	Power	IO GND						
209	D14	VDD	Power	Internal VDD						
210	D15	VSS	Power	Internal GND						
211	D13	MD2/RXD 2	I	Mode/SCIF data input	MD2	RXD2	RXD2	RXD2	RXD2	RXD2
212	C13	RXD	I	SCI data input						
213	B13	TCLK	I/O	RTC/TMU clock						
214	A13	MD8/ $\overline{\text{RTS2}}$	I/O	Mode/SCIF data control (RTS)	MD8	RTS2	RTS2	RTS2	RTS2	RTS2
215	D12	SCK	I/O	SCI clock						
216	B11	MD1/ TXD2	I/O	Mode/SCIF data output	MD1	TXD2	TXD2	TXD2	TXD2	TXD2
217	C12	MD0/ SCK2	I/O	Mode/SCIF clock	MD0	SCK2	SCK2	SCK2	SCK2	SCK2
218	A12	MD7/ $\overline{\text{CTS2}}$	I/O	Mode/SCIF data control (CTS)	MD7	CTS2	CTS2	CTS2	CTS2	CTS2
219	B12	AUDSYNC		AUD sync						
220	A11	AUDCK		AUD clock						
221	C14	VDDQ	Power	IO VDD						
222	C18	VSSQ	Power	IO GND						
223	C10	AUDATA0		AUD data						
224	A10	AUDATA1		AUD data						

Table 1 Pin Functions (cont)

						Memory Interface				
No.	Pin Number	Pin Name	I/O	Function	Reset	SRAM	DRAM	SDRAM	PCMCIA	MPX
225	D11	VDD	Power	Internal VDD						
226	D10	VSS	Power	Internal GND						
227	B9	AUDATA2		AUD data						
228	D9	AUDATA3		AUD data						
229	C9	NC		Do not connect						
230	A9	MD3/$\overline{\text{CE2A}}$	I/O	Mode/ PCMCIA-CE	MD3				$\overline{\text{CE2A}}$	
231	D8	MD4/$\overline{\text{CE2B}}$	I/O	Mode/ PCMCIA-CE	MD4				$\overline{\text{CE2B}}$	
232	C8	MD5	I	Mode	MD5					
233	C11	VDDQ	Power	IO VDD						
234	C17	VSSQ	Power	IO GND						
235	B8	DACK0	O	DMAC0 bus acknowledge						
236	A8	DACK1	O	DMAC1 bus acknowledge						
237	B7	DRAK0	O	DMAC0 request acknowledge						
238	A7	DRAK1	O	DMAC1 request acknowledge						
239	D7	VDD	Power	Internal VDD						
240	D6	VSS	Power	Internal GND						
241	C6	STATUS0	O	Status						
242	B6	STATUS1	O	Status						
243	A6	$\overline{\text{DREQ0}}$	I	Request from DMAC0						
244	C5	$\overline{\text{DREQ1}}$	I	Request from DMAC1						
245	D5	$\overline{\text{ASEBRK}}$/ BRKACK	I/O	Pin break/ acknowledge (H-UDI)						
246	B4	TDO	O	Data out (H-UDI)						
247	C7	VDDQ	Power	IO VDD						
248	B10	VSSQ	Power	IO GND						

Table 1 Pin Functions (cont)

No.	Pin Number	Pin Name	I/O	Function	Reset	Memory Interface				
						SRAM	DRAM	SDRAM	PCMCIA	MPX
249	A5	VDD-PLL2	Power	PLL2 VDD						
250	B5	VSS-PLL2	Power	PLL2 GND						
251	A4	VDD-PLL1	Power	PLL1 VDD						
252	C3	VSS-PLL1	Power	PLL1 GND						
253	A3	VDD-CPG	Power	CPG VDD						
254	B2	VSS-CPG	Power	CPG GND						
255	A2	XTAL	O	Crystal resonator						
256	A1	EXTAL	I	External input clock/crystal resonator						

I: Input
O: Output
I/O: Input/output
Power: Power supply

Notes:
1. Except in hardware standby mode, supply power to all power pins. In hardware standby mode, supply power to RTC as a minimum.
2. Power must be supplied to VDD-PLL1/2 and VSS-PLL1/2 regardless of whether or not the on-chip PLL circuits are used.
3. Power must be supplied to VDD-CPG and VSS-CPG regardless of whether or not the on-chip crystal resonator is used.
4. Power must be supplied to VDD-RTC and VSS-RTC regardless of whether or not the on-chip RTC is used.
5. When using in PCI-disabled mode, refer to Table D.4 in Appendix D for handling of pins.
6. This pin can be connected to V_{SSQ} (I/O GND (0 V)).

Table D.4 Handling of Pins When PCI is Not Used

signals	I/O	Handling
AD31 - AD0	I/O	Pull up to 3.3 V [*1]
$\overline{\text{CBE3}}$ - $\overline{\text{CBE0}}$	I/O	Pull up to 3.3 V
PAR	I/O	Pull up to 3.3 V
$\overline{\text{SERR}}$	I/O	Pull up to 3.3 V
$\overline{\text{PERR}}$	I/O	Pull up to 3.3 V
$\overline{\text{PCILOCK}}$	I/O	Pull up to 3.3 V
$\overline{\text{PCISTOP}}$	I/O	Pull up to 3.3 V
$\overline{\text{DEVSEL}}$	I/O	Pull up to 3.3 V
$\overline{\text{TRDY}}$	I/O	Pull up to 3.3 V
$\overline{\text{IRDY}}$	I/O	Pull up to 3.3 V
$\overline{\text{PCIFRAME}}$	I/O	Pull up to 3.3 V
$\overline{\text{PCIREQ4}}$ - $\overline{\text{PCIREQ2}}$	I/O	Pull up to 3.3 V
$\overline{\text{PCIREQ1}}$	I	Pull up to 3.3 V
$\overline{\text{PCIGNT4}}$ - $\overline{\text{PCIGNT2}}$	O	Pull up to 3.3 V
$\overline{\text{PCIGNT1}}$	O	Pull up to 3.3 V
PCICLK	I	Pull up to 3.3 V
$\overline{\text{PCIRST}}$	O	Leave unconnected
IDSEL	I	Pull up to 3.3 V
$\overline{\text{INTA}}$	O	Leave unconnected

Notes: 1. When pins are not used as general-purpose I/O port.