HITACHI SEMICONDUCTOR TECHNICAL UPDATE

DATE	7th June, 1999	No.	TN-SH7-157 A /E
THEME	Setting Synchronous DRAM Mode register.		
CLASSIFICATION	☐ Spec. change ☐ Supplement of Documents	☑ Limitation on Use	
PRODUCT NAME	HD6417750BP200, HD6417750F167, HD6417750VF128		
REFERENCE DOCUMENTS	SH7750 Hardware Manual, SH7750 Programming Manual	Effective Date From	eternity

1. Setting Synchronous DRAM Mode register

1.1 Contents

(1) When setting Synchronous DRAM Mode register and DMA transfer request occurs simultaneously, Mode register setting or DMA transfer is not executed correctly.

(2) When setting Synchronous DRAM Mode register request occurs just after setting register in Peripheral modules*1, register setting in Peripheral module is not executed correctly.

2. Workaround

Do not use any DMA transfer until setting Synchronous DRAM Mode register is completed.
Do not write to registers in Peripheral modules until setting Synchronous DRAM Mode register is completed.

Setting Synchronous DRAM Mode register should be executed only once after power-on-reset before starting to access Synchronous DRAM.

*1) Peripheral modules in this document is as follows.
CPG, RTC, INTC, TMU, SCI, SCIF, and Hitachi-UDI
(See Hardware manual Appendix A, Table A.1)