PowerVR M2VX

The PowerVR M2VX family of cores are complete standard-definition and high-definition MPEG-2 video decoders developed as IP cores for use in a range of applications including set-top box, Digital TV, DVD playback, video on demand and mobile entertainment systems.

PowerVR M2VX can be programmed to operate synchronously to the display output as required in a set-top box or asynchronously as required in a PDA or PC device. For synchronous operation the memory requirement for decode is only 3 frames. For asynchronous operation a total of 5 frame buffers can be used to achieve maximum frame display.

PowerVR M2VX is designed for high reliability and low-power. Features include:

- MPEG-2 (ISO/IEC 13818-2)
- MPEG-1 (ISO/IEC 11172-2)
- MP@ML or MP@HL decode:
  M2VX - MP@ML (SDTV)
  M2VX-H - MP@HL (HDTV)
  M2VX-HM - MP@HL or multiple streams of MP@ML
- Full hardware video elementary stream decode
- Picture display, sequence display and copyright extensions
- Process portable
- Single clock operation and high testability
- Power minimization
- Simple synchronous register and input data interfaces
- Sustained input rate of 80 Mbits/sec
- Process portable design: 0.18µm, 0.13µm, 90nm and beyond
- Up to 150 MHz clock speed in 0.18µm.

The M2VX IP core is a full scan design and is provided complete with management software for the video decoder and either hardware or software Transport Stream Demux and Section Filtering Options depending on system requirements.

PowerVR M2VX-H

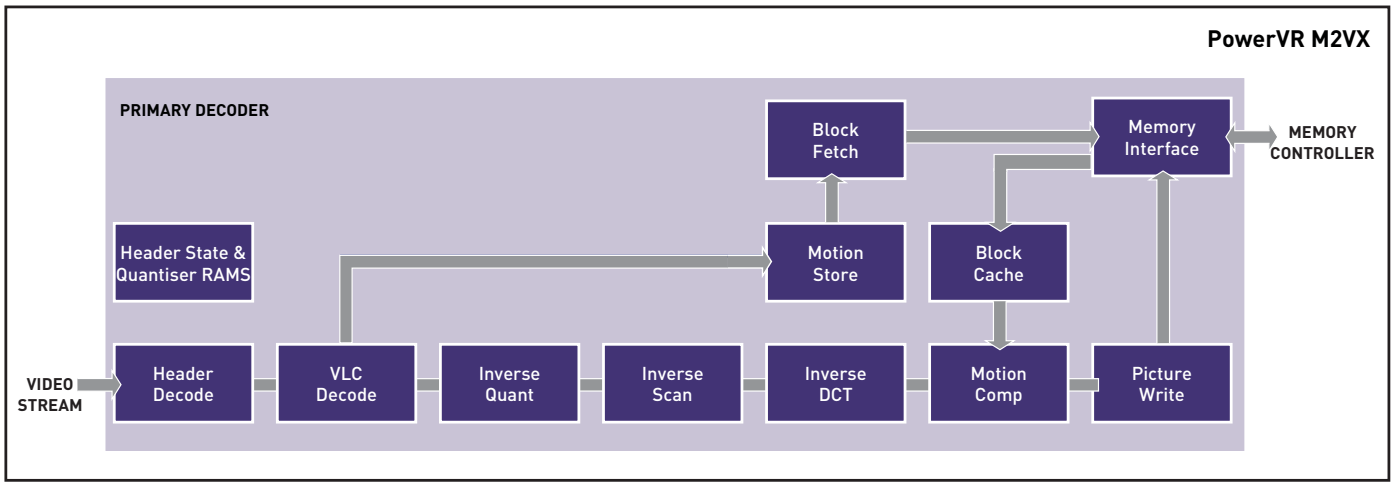
The M2VX-H combines the functionality of M2VX, with the performance to decode MP@MH for HDTV.

PowerVR M2VX-HM

The M2VX-HM provides all the functionality and HDTV performance of the M2VX-H, but with the additional flexibility to support decode of of up to 2 MP@HL or 4 MP@ML video streams.

Performance

M2VX-H and M2VX-HM can achieve full MP@HL decode by running the decoder at 75 MHz. However, as the M2VX family is designed for SoC solutions with a Unified Memory Architecture (UMA), it is expected that the core would be clocked faster to guarantee sufficient dedicated bandwidth for the video stream. The M2VX family will synthesize at speeds up to 150 MHz in 0.18µm.



Power Requirements

Power requirements are optimized by sophisticated power management techniques using register-level clock gating to ensure the lowest active and standby power.

Related System Solution IP

- Metagence META™ IP core is a multi-threaded embedded DSP/RISC processor core ideally suited for audio decoding and signal reception as well as General Purpose processing, which when used with PowerVR M2VX provides a full MPEG-2 solution including audio decode, TS (transport stream) and PS (program stream) decode.
- Ensigma UCC (Universal Communications Coprocessor) increases the level of integration of Imagination Technologies SoC solutions, requiring only a tuner to provide the complete decode solution for digital video broadcasting.
- PowerVR Pixel Display Pipeline (PDP) is a multi-layer display controller, designed to support modern layered user interfaces. Configurable for up to 6 planes with support for YUV and RGB, scaling is available on 2 planes, and the PDP has configurable alpha-blending and chroma key support.
- PowerVR graphics cores: MBX Pro for high-end 3D graphics acceleration for consumer electronics devices including set-top boxes, consoles and home entertainment systems. MBX for best area/performance 3D graphics acceleration for handheld devices and mainstream set-top boxes. MBX Lite for entry level 3D graphics acceleration for mobile devices.
- PowerVR TVE is a digital TV encoder which outputs PAL or NTSC encoded composite video and simultaneous S-video, RGBS or YUV component video for TV display when connected to a pixel display pipeline such as PowerVR PDP.

Related Software IP

- Dolby® Digital
- MPEG-2 audio
- MPEG audio layer-3 (MP3)

M2VX Core Design Package

M2VX is available as soft IP or as hard IP and ships with:

- Synthesis scripts
- Extensive verification test suite to ensure correct implementation of the design in an SoC
- Behavioural simulator written in ANSI C
- Hardware implementation guides
- Programmer's reference manuals

PowerVR
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