Intel® 2700G7 Multimedia Accelerator

Datasheet

November 2004

Document Number: 304430-001

Contents

Figures

Tables

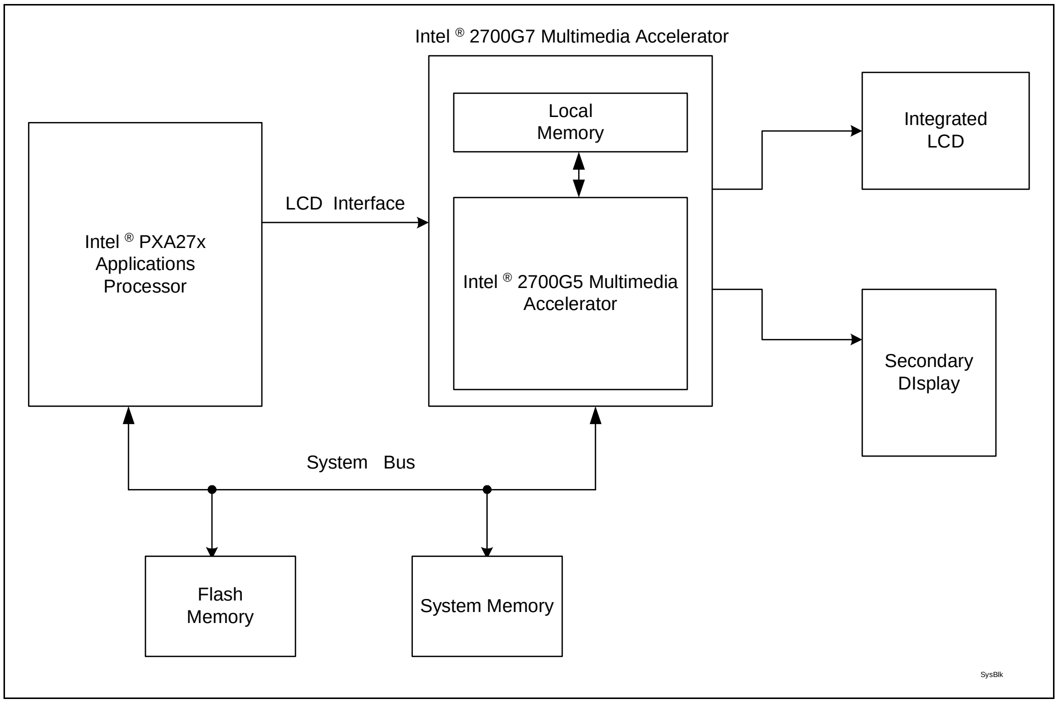
Revision History

Rev. No.	Description	Rev. Date
-001	Initial Release.	November 2004

Intel® 2700G7 Multimedia Accelerator Family Features

- Advanced Packaging
  - 14 mm x 14 mm, 0.65 mm ball pitch, 364 ball BGA package optimized for space constrained handheld devices
- Low Power
  - Up to VGA (640x480x16 bpp) refresh from integrated frame buffer
  - Extensive clock gating
  - Low voltage core (1.2 V)
  - Optional low voltage I/O (1.8 V)
  - 0.13 micron process technology
  - Partial and one-shot display refresh support
- Low Power, High Performance Video Acceleration
  - Accelerated MPEG2* video decode, 720 x 480 resolution, 30+ fps
  - Accelerated MPEG4* video decode, 640 x 480, 30+ fps
  - Accelerated WMV* video decode, 640 x 480, 30+ fps
  - Hardware accelerated Inverse Discrete Cosine Transforms (IDCT)
  - Hardware accelerated motion compensation
  - Hardware accelerated color space conversion
  - Hardware accelerated scaling
- Low Power, High Performance Graphics Acceleration
  - 2D and 3D acceleration
  - Up to 75 MHz, 32-bit graphics engine
  - 150M pixels per second (pps) fill rate for 2D
  - 831K triangles per second (tps) processing capability for 3D
- Packaged Memory Solutions
  - Integrated 704 KB on die memory
  - Stacked high-speed SDRAM for local memory
    - 16 MB SDRAM at 100 MHz
    - 1.8 V SDRAM support
    - Low-power SDRAM support
- Accelerated Dual Display
  - Simultaneous displays with independent images and independent resolutions
  - Integrated LCD switch provides high quality dual display
    - Intel® 2700G7 Multimedia Accelerator can drive either display up to 1024 x 768
    - Intel® PXA27x Processor graphics engine can drive either display up to 800 x 600
    - Dynamic, programmable assignment of graphics engine to each display
- Flexible Architecture
  - Easy design transition to the 2700G7 Multimedia Accelerator from 2700G3/2700G5 Multimedia Accelerator
- Intel® PXA27x Processor Optimized
  - Complementary feature set
  - Wireless MMX* optimized drivers
  - PXA27x Processor IPPs and GPPs
  - Uses both Variable Latency I/O (VLIO) and SRAM protocols
- Broad Display Support
  - TFT LCDs up to 1024x768x24bpp
  - Accelerated dual display
  - Low power display refresh using on-die memory
  - Advanced LCD Support
  - Supports external displays such as analog CRTs and projectors, TVs or digital flat panels when paired with an encoder chip

System Architecture Block Diagram



1 Introduction

The Intel® 2700G Multimedia Accelerator family contains three components:

- The Intel® 2700G5 Multimedia Accelerator. This component incorporates a 704 KB on-die frame buffer for performance.
- The Intel® 2700G3 Multimedia Accelerator. This component incorporates a 384 KB on-die frame buffer for value.
- Intel® 2700G7 Multimedia Accelerator. This component stacks the Intel® 2700G5 Multimedia Accelerator with 16 MB of local memory running at 100 MHz.

This document is the datasheet for the Intel® 2700G7 Multimedia Accelerator and includes device overview, capabilities, performance estimates, signal description, functional description, register description, package characteristics, and ballout. For information on the 2700G3/2700G5 Multimedia Accelerator components, refer to the *Intel® 2700G Multimedia Accelerator Multimedia Datasheet*.

This document assumes a working knowledge of the Intel® XScale® technology applications processor family, and specifically the PXA27x processors. Contact your Intel representative for more documentation regarding these processors.

1.1 Reference Documentation

Document Title	Location / Document Number
Intel® 2700G7 Multimedia Accelerator Design Guide	304431
Intel® 2700G Multimedia Accelerator Design Guide	300949
Intel® 2700G Multimedia Accelerator Datasheet	300948

1.2 Overview

As the multimedia capabilities of handheld devices increase to include higher resolutions, high-quality displays, complete graphical user interfaces (GUIs), multimedia, 3D capabilities, and video playback, it is necessary to include a graphics accelerator in many handheld devices. The 2700G7 Multimedia Accelerator component is low-power, full-featured graphics accelerator optimized for Intel® Personal Client Architecture solutions and support the PXA27x processor family. The 2700G7 Multimedia Accelerator provides high-performance 2D, 3D, MPEG2, MPEG4, and Windows* Media Video (WMV) acceleration as well as dual-display capabilities.

The 2700G7 Multimedia Accelerator supports resolutions up to XGA (1024 x 768 x 24 bpp) color. The 2700G7 Multimedia Accelerator 3D acceleration provides a complete hardware 3D rendering pipeline. This includes 831K triangles per second processing capability and 84 million pixels-per-second fill rate. Advanced 3D hardware acceleration includes features such as texture and light mapping, point, bilinear, trilinear and anisotropic filtering, alpha blending, dual texturing support, deferred texturing, screen tiling, texture compression and full-screen anti-aliasing.

The 2700G7 Multimedia Accelerator 2D acceleration includes support for clipping, anti-aliasing, alpha blending as well as a variety of BLT functions. All 256 raster operations (Source, Pattern, and Destination) defined by Microsoft are supported.

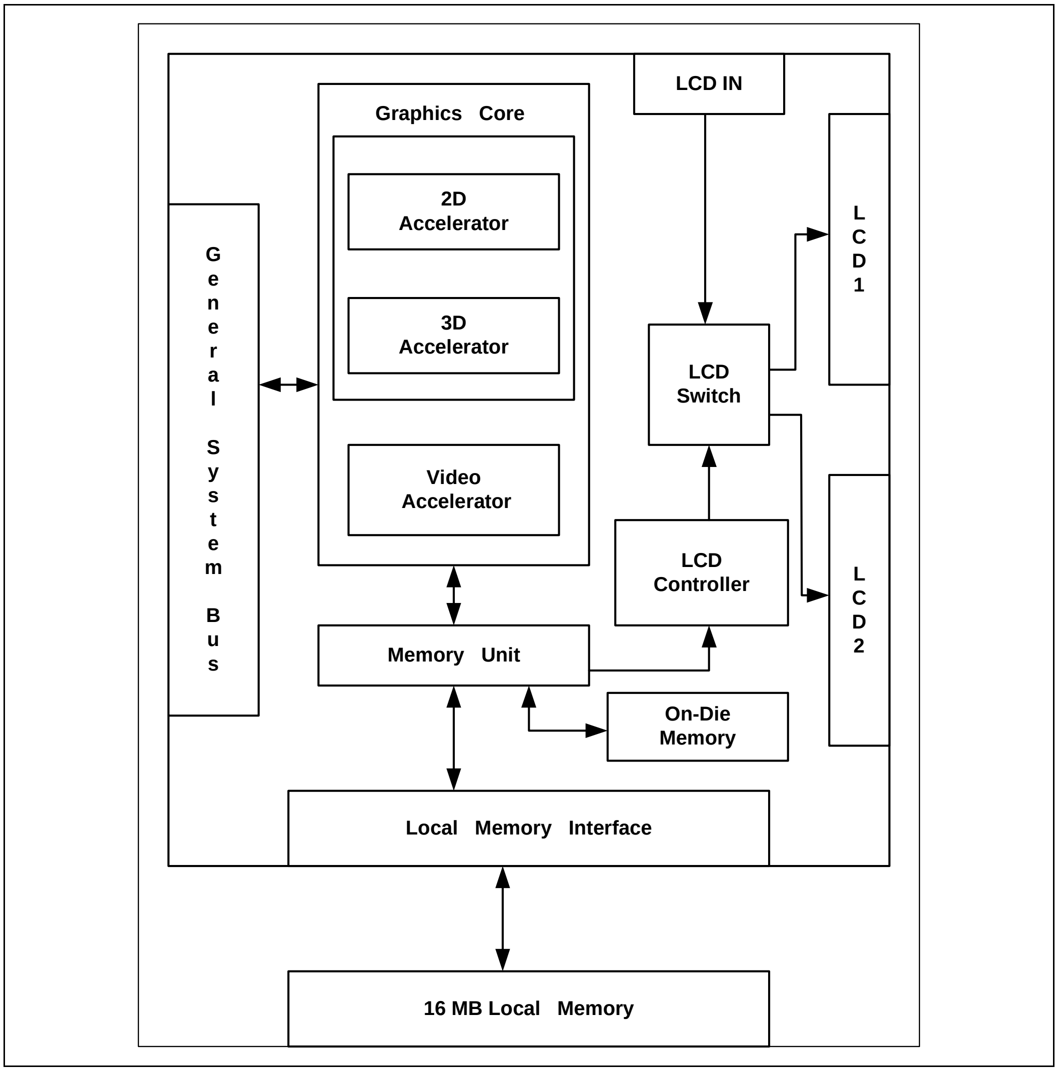
The 2700G7 Multimedia Accelerator accelerates MPEG4, MPEG2, and WMV video decode. For optimal performance and lowest power, the following video-decode capabilities are accelerated in the 2700G7 Multimedia Accelerator hardware: Inverse Zig-Zag (IZZ), Inverse Discrete Cosine Transforms (IDCT), Motion Compensation (MC), Color Space Conversion (CSC), and Scaling. The 2700G7 Multimedia Accelerator hardware will perform Inverse Zig-Zag, Inverse Discrete Cosine Transform, and Motion Compensation for MPEG-1*/2*/4* and Motion Compensation for WMV* video streams.

The 2700G7 Multimedia Accelerator also provides flexibility to a system’s display capabilities. With this device, a system can use a wide variety of displays, including integrated LCDs of various resolutions, color depths, and refresh rates, as well as external displays (e.g., analog CRTs, TVs, or digital flat panels). When paired with the applications processor, the 2700G7 Multimedia Accelerator is capable of simultaneously driving separate display streams to two separate displays.

The 2700G7 Multimedia Accelerator makes it the ideal solution for space-constrained designs like smart phones, personal digital assistants (PDAs), wireless communicators, and telematics devices.

Figure 1-1 shows a high-level block diagram of the 2700G7 Multimedia Accelerator.

Figure 1-1. Intel® 2700G7 Multimedia Accelerator Block Diagram



§

2 Signal Description

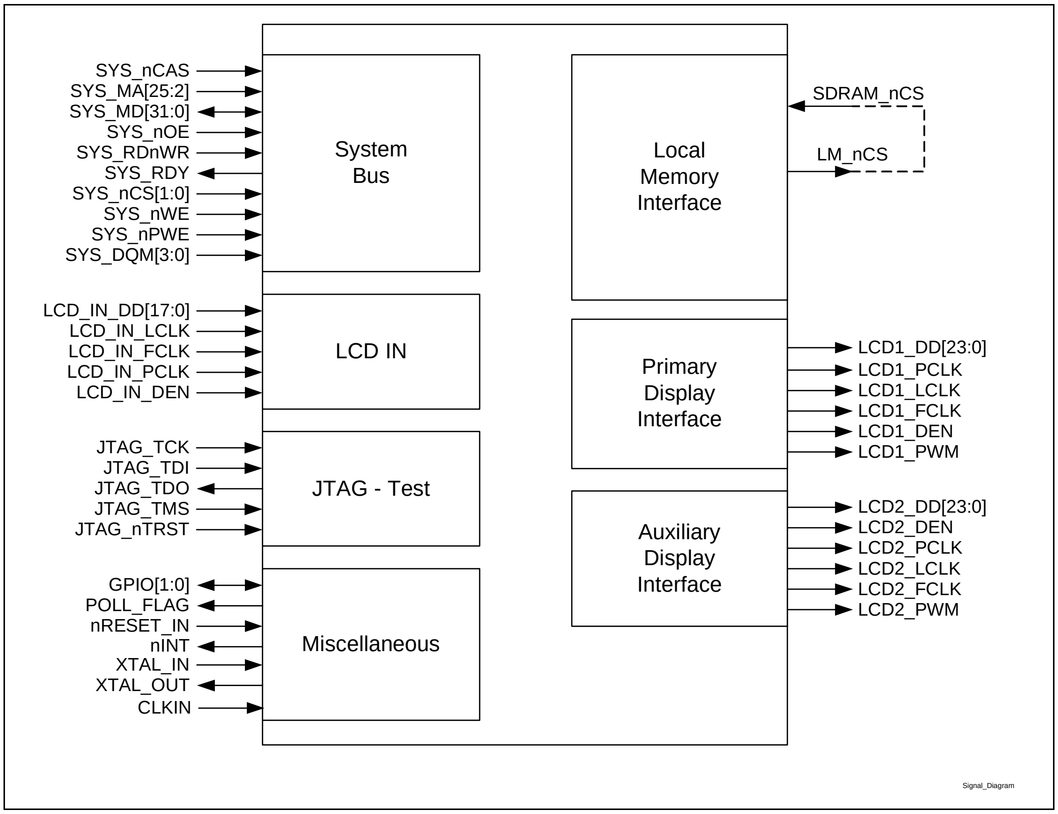
This chapter provides a detailed description of the 2700G7 Multimedia accelerator signals. The signals are arranged in functional groups according to their associated interface. The states of all of the signals during reset are provided in Section 2.10.

The lower case "n" character in a signal name indicates that the active, or asserted, state occurs when the signal is at a low voltage level. When "n" is not present in a signal name, the signal is asserted when at the high voltage level. Note that for the SYS_RDnWR signal, the "n" in front of the WR indicates that only the write function is active low (read function is active high).

The following notations are used to describe the signal type:

I	Input pin
O	Output pin
I/O	Bi-directional Input/Output pin

Figure 2-1. Signal Diagram



2.1 System Bus Interface

The I/O voltage of these signals is set by VCC_SYS.

Table 2-1. General System Bus Signals

Signal Name	Type	Description
SYS_nCAS	I	**System Bus Address Strobe:** This signal is the address valid strobe for SRAM interface (SYS_nCS1).
SYS_MA[25:2]	I	**System Bus Address:** These signals are the address pins for the system bus. They are used with both VLIO and SRAM protocols.
SYS_MD[31:0]	I/O	**System Bus Data:** These signals are the bi-directional data pins for the system bus. They are used with both VLIO and SRAM protocols.
SYS_nOE	I	**System Bus Output Enable:** SYS_nOE enables the 2700G7 Multimedia Accelerator's SYS_MD[31:0] drivers. This signal is for use with SRAM protocol.
SYS_RDnWR	I	**System Bus Read/Write:** SYS_RDnWR defines the transaction type. High = Read; Low = Write
SYS_RDY	O	**System Bus Ready:** SYS_RDY low indicates the VLIO target (2700G7 Multimedia Accelerator) not ready. A high indicates VLIO target (2700G7 Multimedia Accelerator) ready. For reads, this signal indicates readiness to provide data. For writes, this signal indicates readiness to accept data.
SYS_nCS[1:0]	I	**System Bus Chip Select:** SYS_nCS0 indicates the 2700G7 Multimedia Accelerator is the target of a VLIO protocol transaction (read or write) on the GSB interface. SYS_nCS1 indicates the 2700G7 Multimedia Accelerator is the target of an SRAM protocol transaction (write only) on the GSB interface.
SYS_nWE	I	**System Bus SRAM Write Enable:** SYS_nWE qualifies valid write data for SRAM protocol transactions.
SYS_nPWE	I	**System Bus VLIO Write Enable:** SYS_nPWE qualifies valid write data for VLIO protocol transactions.
SYS_DQM[3:0]	I	**System Bus Data Byte Masks:** SYS_DQM[3:0] are used to mask byte lanes on the GSB. Masked byte lanes do not carry valid data and are ignored. • SYS_DQM[X] **High** = Mask Byte X (data not valid) • SYS_DQM[X] **Low** = Do Not Mask Byte X (data valid) **SYS_DQM** **Byte Lane** 0 MD[7:0] 1 MD[15:8] 2 MD[23:16] 3 MD[31:24]

NOTE: Total number of system bus signals is 68.

2.2 Local Memory Interface

The I/O voltage of these signals is set by VCC_LM.

Table 2-2. Local Memory Interface Signals

Signal Name	Type	Description
LM_RSVD	O	**Local Memory Reserved:** There are a total of 55 LM_RSVD signals. These signals must be left as no connects.
LM_nCS	O	**Local Memory Chip Select:** This signal must be connected to SDRAM_nCS via a short, direct trace on the board.
SDRAM_nCS	I	**SDRAM Chip Select:** SDRAM_nCS is the chip select pin for the stacked SDRAM local memory. This signal must be connected to LM_nCS via a short, direct trace on the board.

NOTE: Total number of local memory interface signals is 57.

2.3 LCD Input Interface

The I/O voltage of these signals is set by VCC_LCD_IN.

Table 2-3. LCD Input Signals

Signal Name	Type	Description
LCD_IN_DD[17:0]	I	**LCD Data Inputs:** These signals carry LCD data from application processor to the 2700G7 Multimedia Accelerator.
LCD_IN_PCLK	I	**Pixel Clock Input:** This signal is the pixel clock for the LCD input used to clock LCD_IN_DD[17:0].
LCD_IN_LCLK	I	**Line Clock Input:** This signal is the line clock for the LCD input and indicates the end of a line.
LCD_IN_FCLK	I	**Frame Clock Input:** This signal is the frame clock for the LCD input and indicates the end of a frame.
LCD_IN_DEN	I	**LCD Data Enable Input:** LCD data enable indicates valid data on the LCD input interface.

NOTE: Total number of LCD Input signals is 22.

2.4 Primary LCD Interface

The I/O voltage of these signals is set by VCC_LCD1.

Table 2-4. Primary Display Interface Signals

Signal Name	Type	Description
LCD1_DD[23:0]	O	**Primary LCD Data:** These signals carry LCD data from the 2700G7 Multimedia Accelerator to the LCD module (or intermediate display device).
LCD1_PCLK	O	**Primary LCD Pixel Clock:** LCD1_PCLK is the pixel clock for the LCD interface and is used to clock LCD1_DD[23:0].
LCD1_LCLK	O	**Primary LCD Line Clock:** LCD1_LCLK is the line clock for the LCD interface and indicates the end of a line.
LCD1_FCLK	O	**Primary LCD Frame Clock:** LCD1_FCLK is the frame clock for the LCD interface and indicates the end of a frame.
LCD1_DEN	O	**Primary LCD Data Enable:** LCD1_DEN is the LCD data enable and indicates valid data on the primary LCD interface.
LCD1_PWM	O	**Primary LCD Pulse Width Modulator:** LCD1_PWM allows control of the primary LCD backlight independent of the state of the application processor.

NOTE: Total number of Primary LCD signals is 29.

2.5 Auxiliary LCD Interface

The I/O voltage of these signals is set by VCC_LCD2.

Table 2-5. Auxiliary Display Interface Signals

Signal Name	Type	Description
LCD2_DD[23:0]	O	**Auxiliary LCD Data:** These signals carry LCD data from the 2700G7 Multimedia Accelerator to the auxiliary LCD module (or intermediate display device).
LCD2_PCLK	O	**Auxiliary LCD Pixel Clock:** LCD2_PCLK is the pixel clock for the auxiliary LCD interface and is used to clock LCD2_DD[23:0].
LCD2_LCLK	O	**Auxiliary LCD Line Clock:** LCD2_LCLK is the line clock for auxiliary LCD interface and indicates the end of a line.
LCD2_FCLK	O	**Auxiliary LCD Frame Clock:** LCD2_FCLK is the frame clock for auxiliary LCD interface and indicates the end of a frame.
LCD2_DEN	O	**Auxiliary LCD Data Enable:** LCD2_DEN is the LCD data enable and indicates valid data on the auxiliary LCD interface.
LCD2_PWM	O	**Auxiliary LCD Pulse Width Modulator:** LCD2_PWM allows control of the auxiliary LCD backlight independent of the state of the application processor.

NOTES: Total number of Auxiliary LCD signals is 29.

2.6 JTAG Interface

Table 2-6. Test (JTAG) Signals

Signal Name	Type	Description
JTAG_TCK	I	**JTAG Test Clock:** This signal is the clock input for the 2700G7 Multimedia Accelerator's JTAG interface.
JTAG_TDI	I	**JTAG Test Data In:** This signal is the serial data input and is sampled on the rising edge of JTAG_TCK. This signal must be pulled high when not being driven.
JTAG_TDO	O	**JTAG Test Data Out:** This signal is the serial data output and is clocked on the falling edge of JTAG_TCK. This signal is tri-stated when not being driven to allow for parallel TDO connections at the board level.
JTAG_TMS	I	**JTAG Test Mode Select:** This signal controls functionality of the 2700G7 Multimedia Accelerator's JTAG interface and is sampled on the rising edge of JTAG_TCK.
JTAG_nTRST	I	**JTAG Test Reset:** This signal provides asynchronous initialization of the JTAG test logic. An external source must drive JTAG_nTRST before or at the same time as nRESET_IN for correct JTAG and the 2700G7 Multimedia Accelerator operation.

NOTE: Total number of JTAG signals is 5.

2.7 Miscellaneous Signals

Table 2-7. Miscellaneous Signals

Signal Name	Type	Description
XTAL_IN	I	**Clock XTAL in (13 MHz):** XTAL_IN is the crystal input for clock generation. If used, the external crystal is connected between XTAL_IN and XTAL_OUT. If an external reference clock is provided via CLKIN, a crystal is not required on this signal.
XTAL_OUT	O	**Clock XTAL out (13 MHz):** This signal drives the crystal. If an external reference clock is provided via CLKIN, a crystal is not required on this signal.
CLKIN	I	**Reference Clock Input:** This signal may be used as an alternate 13 MHz source for the 2700G7 Multimedia Accelerator's PLL reference clock. If used, XTAL_IN and XTAL_OUT should not be connected to a crystal. If an external crystal is connected between XTAL_IN and XTAL_OUT, this signal should not be connected to an external clock reference.
GPIO[1:0]	I/O	**General Purpose I/O:** These signals are software controllable GPIO signals that can be programmed using the 2700G7 Multimedia Accelerator registers as either inputs (GPIs) or outputs (GPOs). In GPO mode, these GPIO signals can be programmed to drive high, drive low, or tri-state via a system register. In GPI mode, the state of the GPIO signals will be reflected in a system register.
POLL_FLAG	O	**Polling Flag:** This signal is the polling flag connected to applications processor GPIO. This signal can be used for flow control observations within the 2700G7 Multimedia Accelerator.
nRESET_IN	I	**Hard Reset Input:** All internal logic is reset when nRESET_IN is low.

Signal Name	Type	Description
nINT	O	**Interrupt:** This signal is an interrupt output used to interrupt the application processor.
RSVD	I/O	**Reserved:** There are 3 RSVD signals. Each signal requires a 100 kΩ pull-down resistor to ground.
NC	-	**No Connects:** These signals have no function.

NOTE: Total number of miscellaneous signals is 13.

2.8 Power and Ground

Table 2-8. Power Signals

Signal Name	# of Signals	Type	Description
VCC_CORE	28	P	Core Power Supply. 1.2 V
VCC_SYS	9	P	General System Bus Power Supply. 1.8 V, 2.5 V
VCC_LM	10	P	Local Memory Bus Power Supply. 1.8 V
VCC_SDRAM	13	P	SDRAM Device supply. 1.8 V
VCC_LCD_IN	2	P	LCD Input Power Supply. 1.8 V, 2.5 V
VCC_LCD1	4	P	Primary LCD Interface Power Supply. 1.8 V, 2.5 V, 3.3 V
VCC_LCD2	4	P	Auxiliary LCD Interface Power Supply. 1.8 V, 2.5 V, 3.3 V
VCC_IO	15	P	Miscellaneous I/O Power Supply. 3.3 V
GND	50	G	Common Ground. Gnd
VCCA_CORE_PLL	1	P	Core PLL Analog Power. 2.5 V
VSSA_CORE_PLL	1	G	Core PLL Analog Ground. Gnd
VCCA_DISP_PLL	1	P	Display PLL Analog Power. 2.5 V
VSSA_DISP_PLL	1	G	Display PLL Analog Ground. Gnd
VAA_XTAL	1	P	Crystal Oscillator Analog Power. 2.5 V
VSSA_XTAL	1	G	Crystal Oscillator Analog Ground. Gnd

NOTE: Total number of power and ground pins is 141.

2.8.1 Power Sequencing

The following 2700G7 Multimedia Accelerator-specific power sequencing requirements must be observed:

- Any I/O rail that is powered at 3.3 V (e.g., VCC_LCD1) must be tied to VCC_IO to ensure identical sequencing.
- Typical design practice has all power rails applied/removed as close in time as practical. If the 2700G7 Multimedia Accelerator's rails can be brought up at roughly the same time, there are no specific sequencing requirements. However, if design limitations require significant delays between the application of power rails, then the 2700G7 Multimedia Accelerator's core power should be applied first. Additionally, the 3.3 V rail should be brought up no later than the other I/O rails.

2.9 Pin Straps and Pull-up/Pull-down Resistors

Table 2-9 lists the strapping options for the 2700G7 Multimedia Accelerator.

Table 2-9. Strapping Options

Signal Name	Strap Function	Strap High Option	Strap Low Option	Recommendation
LCD1_DD0	Clock source	XTAL	CLKIN	If using crystal: 100 kΩ pull-up to V_{CC_LCD1} If using external reference clock: 100 kΩ pull-down to ground
LCD1_DD1	SYS_RDY drive strength	High buffer strength	Low buffer strength	100 kΩ pull-down to ground. Dependent on system bus loading; refer to the *Intel® 2700G7 Multimedia Accelerator Design Guide*.
LCD1_DD2	Reserved	Required	N/A	A 100 kΩ pull-up to V_{CC_LCD1} is required.

Table 2-10 lists the pull-up (PU) or pull-down (PD) resistors required externally or integrated internally in the 2700G7 Multimedia Accelerator. The system designer must implement external PU and PD values on the main board. Signals with internal PU and PD values do **not** require external PU/PD resistors and are shown for reference only.

Table 2-10. Pull-up and Pull-down Resistors

Signal Name	External PU	Internal PU	External PD	Internal PD
RSVD (3 signals)	—	—	100 kΩ to GND	—
CLKIN[1]	—	—	100 kΩ to GND	—
JTAG_TCK	—	—	100 kΩ to GND	—
JTAG_TDI	—	~61 kΩ	—	—
JTAG_TMS	—	~61 kΩ	—	—
JTAG_nTRST	—	~61 kΩ	—	—
GPIO0	—	—	100 kΩ to GND	—
GPIO1	—	—	100 kΩ to GND	—

NOTES:

1. Only if clock source is provided by XTAL (refer to Table 2-9). If external reference clock is provided via this pin, 100 kΩ PD should be applied to XTAL_IN instead.

2.10 Signal States in Reset

Table 2-11 lists the state of the 2700G7 Multimedia Accelerator signals during reset.

Table 2-11. Signal States in Reset

Signal Name	Reset State
System Bus	
SYS_nCS[1:0]	Input Only
SYS_MA[23:0]	Input Only
SYS_MD[31:0]	Tri-State
SYS_nOE	Input Only
SYS_RDnWR	Input Only
SYS_nPWE	Input Only
SYS_nWE	Input Only
SYS_nCAS	Input Only
SYS_DQM[3:0]	Input Only
SYS_RDY	Tri-State
Local Memory Interface	
LM_nCS	High
SDRAM_nCS	Input Only
LCD Input	
LCD_IN_PCLK	Input Only
LCD_IN_FCLK	Input Only
LCD_IN_LCLK	Input Only
LCD_IN_DEN	Input Only
LCD_IN_DD[17:0]	Input Only
Primary LCD Output	
LCD1_PCLK	Low
LCD1_FCLK	Low
LCD1_LCLK	Low
LCD1_DEN	Low
LCD1_DD[23:3]	Low
LCD1_DD[2:0][(1)]	Tri-State [2]
LCD1_PWM	Low
GPIO[1:0]	Tri-State [2]
Secondary LCD Output	
LCD2_PCLK	Low
LCD2_FCLK	Low
LCD2_LCLK	Low
LCD2_DEN	Low
LCD2_DD[23:0]	Low
LCD2_PWM	Low
Miscellaneous	
nRESET_IN	Input Only
nINT	High
POLL_FLAG	Low
Test	
CLKIN	Input Only
JTAG_nTRST	Input Only
JTAG_TDI	Input Only
JTAG_TDO	Tri-State
JTAG_TMS	Input Only
JTAG_TCK	Input Only
Crystal Oscillator	
XTAL_IN	N/A
XTAL_OUT	N/A

NOTES:
1. Four XTAL or CLKIN cycles, after nRESET_IN pin is de-asserted, these pins will be driven low (0x0).
2. External pull-up (PU)/pull-down (PD) required. Refer to Table 2-10 for more details.

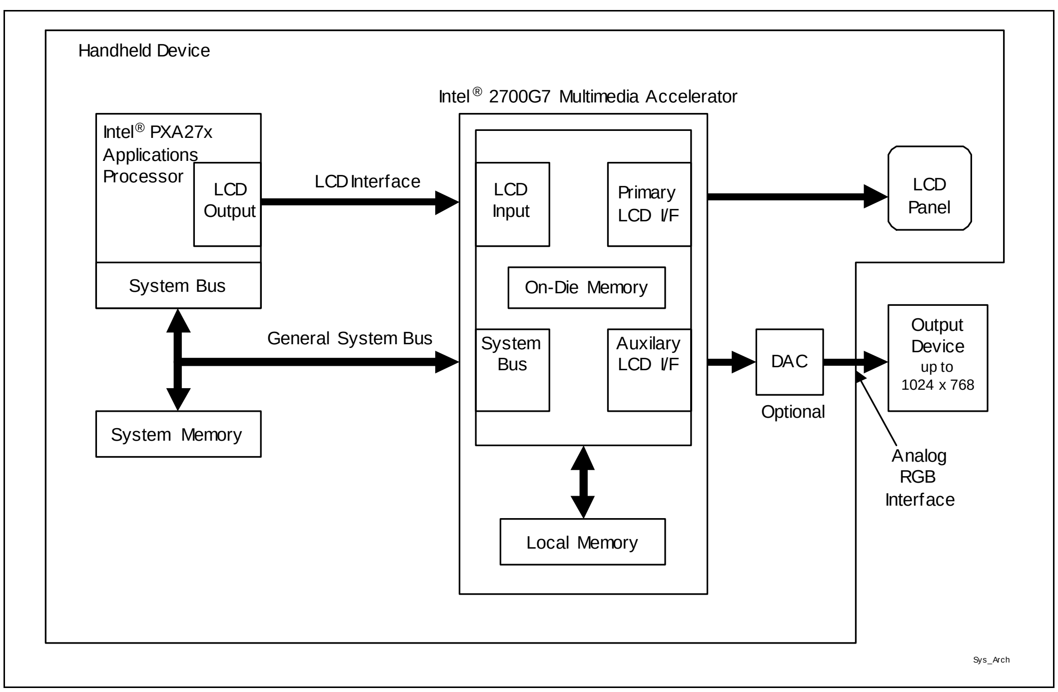
3 System Architecture

3.1 High-Level System Architecture

The 2700G7 Multimedia Accelerator has five major interfaces:

- General System Bus
  - Used to connect to the application processor
- LCD Input
  - LCD input from applications processor for dual display
- Local memory
  - 16 MB stacked SDRAM memory for graphics data.
- Primary LCD Interface
  - For connection to an LCD display
- Auxiliary LCD Interface
  - For connection to a second LCD, DAC, or other display output

Figure 3-1. Typical High-Level Intel® 2700G7 Multimedia Accelerator Package System Architecture



3.2 Intel® XScale® Technology General System Bus Support

The 2700G7 Multimedia Accelerator interfaces with the Intel XScale® technology application processor via the general system bus. This 32-bit, 100 MHz bus provides up to 400 MB/s maximum theoretical bandwidth. Additionally, the general system bus operates at either 1.8 V or 2.5 V.

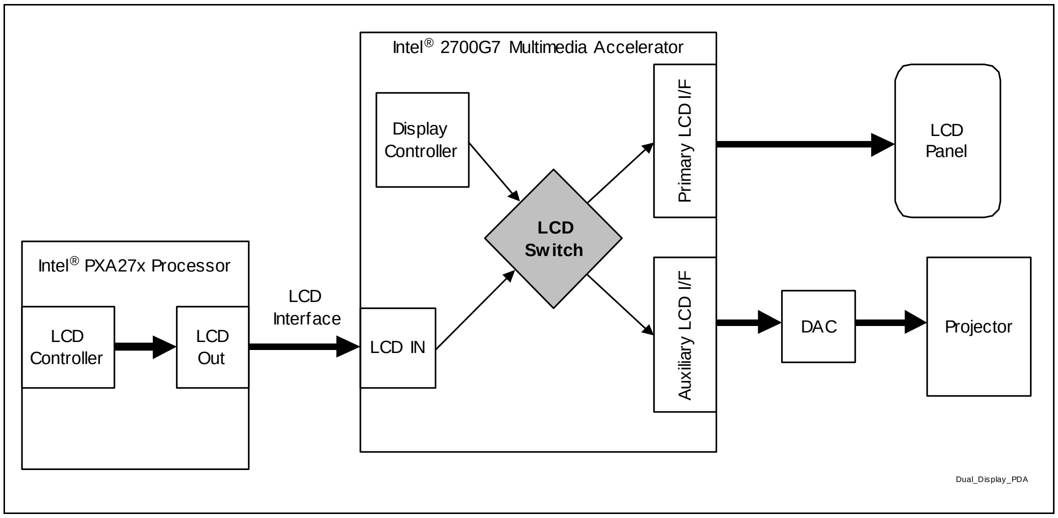
There are several protocols that run on the general system bus. The applications processor uses two of these protocols to communicate with the 2700G7 Multimedia Accelerator: *SRAM Protocol* is strictly used for writes and *Variable Latency I/O* (VLIO) can be used for reads and writes. SRAM protocol is used for optimum write performance.

3.3 Accelerated Dual Display

A 2700G7 Multimedia Accelerator -based system has two display engines: the 2700G7 Multimedia Accelerator display controller and the applications processor's built-in display controller. Refer to Section 3.6 for more detailed information regarding the 2700G7 Multimedia Accelerator display controller. The 2700G7 Multimedia Accelerator's accelerated dual-display capability allows designers to take full advantage of the graphics acceleration capabilities of the 2700G7 Multimedia Accelerator and the integrated display controller in the applications processor. A 2700G7 Multimedia Accelerator -based system is capable of driving two separate displays, with either identical display content and timings, or independent content and timings.

To ensure optimum display performance, the 2700G7 Multimedia Accelerator provides two LCD outputs (primary and auxiliary); one to drive each of the displays. Either display controller (the 2700G7 Multimedia Accelerator or the applications processor) can drive either the primary or auxiliary output. In most cases, the designer will want the best display to be driven by the 2700G7 Multimedia Accelerator and the lower resolution display to be driven by the applications processor. However, this decision is left to the system designer and is controlled via software. The 2700G7 Multimedia Accelerator can drive displays up to 1024 x 768 and the applications processor can drive displays up to 800x600, if needed. Connecting a PDA to a digital projector is one potentially common usage model for dual display. Other potential usage models include connecting a handheld device to a television set or external monitor, communicators with dual TFT displays, etc.

Figure 3-2. Accelerated Dual-Display Implementation for PDA/Digital Projector



In the single display case (e.g., PDA being used without external monitor), the single display (i.e., LCD) would typically be driven by the 2700G7 Multimedia Accelerator multimedia engine. When the device is placed in dual-display mode (e.g., PDA with external projector), the original display (i.e., LCD) could be driven by the applications processor's display controller and the external display (i.e., projector) could be driven by the 2700G7 Multimedia Accelerator's graphics engine (assuming the external device has higher resolution and display quality than the internal display). Refer to Figure 3-3 and Figure 3-4 for details on this implementation.

Figure 3-3. Accelerated Dual Display / Single Display Example

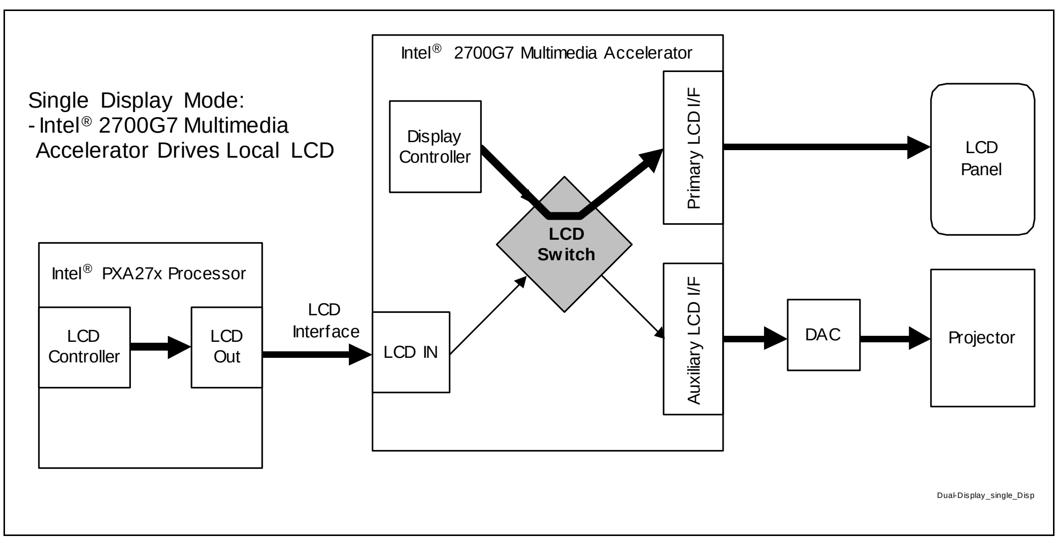
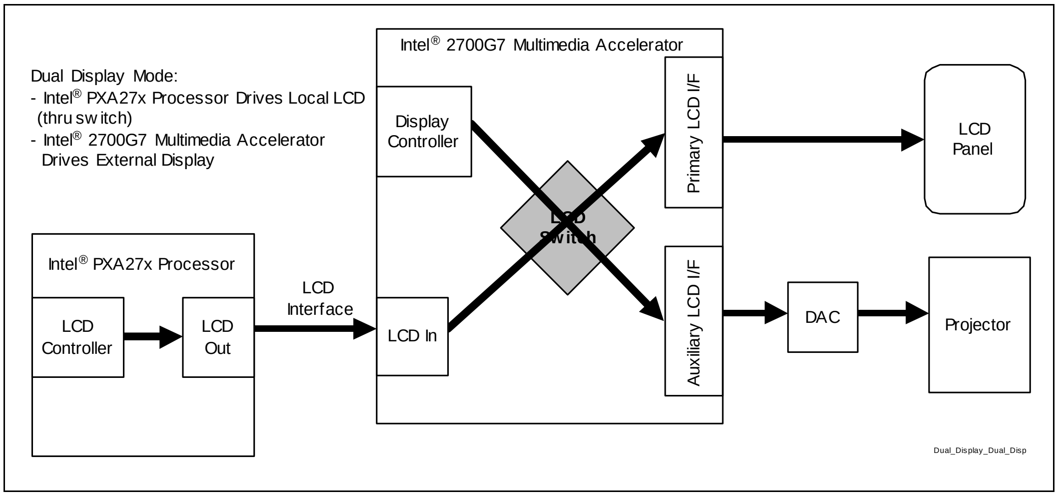


Figure 3-4. Accelerated Dual Display / Dual Display Example



The LCD cross-bar switch ensures that the most appropriate display controller is always driving each display. This implementation allows accelerated graphics on the LCD panel, when in single display mode, and still allows accelerated resolutions up to 1024x768 for a projector when in dual-display mode. The LCD switch is controlled via a register write. To avoid display artifacts, both displays will be blanked before switching occurs.

Additionally, the LCD switch allows either the 2700G7 Multimedia Accelerator display controller, or the PXA27x processor LCD controller to drive BOTH the primary and auxiliary outputs simultaneously with the same data at the same resolution and frame rate.

3.4 Graphics and Video Acceleration

3.4.1 Graphics and Video Features

This section documents the 2D, 3D, and video acceleration capabilities of the 2700G7 Multimedia Accelerator. More detailed descriptions of these capabilities are in Section 3.4.2.

3.4.1.1 2D Features

- 32-bit, up to 75 MHz Graphics Core
- ROP2, 3 and 4 Support
- Per-Pixel Alpha Blending
- Colorkey
- Full Scene Anti-Aliasing
- Alpha Test
- BitBLT, StretchBLT, CSCBLT
- 150M Pixels/Second Fill Rate
- 16, 18, and 24 bits per Pixel Support
  — Low color depth support for power savings
- Hardware pixel doubling and decimation

3.4.1.2 3D Features

- Up to 75 MHz 3D Graphics Core
- Deferred Texturing
- Screen Tiling
- Flat and Gouraud Shading
- Perspective Correct Texturing
- Specular Highlights
- 32-bit Z Buffer
- 32-bit ARGB Internal Rendering
- Full Tile Blend Buffer
- Z Load/Store Mode
- Per Vertex Fogging
- 16 and 32-bit RGB Textures
- YUV 4:2:2 Textures
- OpenGL-ES* Compatible 2-bit and 4-bit Runtime Texture Compression
- Point, Bilinear, Trilinear, and Anisotropic Filtering
- Dot3 Bump Mapping
- Backface Culling
- Small Object Culling
- Fixed-Point to Floating-Point Conversion
- Accelerated Rendering of Triangle Lists, Strips and Fans
- Per-Pixel Alpha Blending
- Full Scene Anti-Aliasing
- Hardware Clipping
- 831K Triangles/Second Rendering

3.4.1.3 Video Acceleration Features

- Up to 75 MHz Video Core
- Scalable Video Overlay
- High quality 8x4 Programmable Tap Filter for Scaling and Decimation
- Independent Gamma Correction
- 640x480 (VGA) MPEG4 Decode @ greater than 30 fps (Simple Profile)
- 640x480 and 720x480 MPEG2 Decode @ greater than 30 fps (Main Profile)
- Hardware Windows Media Video (WMV) Acceleration
- Hardware Video Decode
  - Inverse Zig-Zag (iZZ)
  - Inverse Discrete Cosine Transform (iDCT)
  - Hardware Motion Compensation
  - Color Space Conversion
  - Hardware Video Scaling
- Half- and Quarter-Sample Accuracy
- YUV 4:2:2 and 4:2:0
- Video Scaled up to 1024x768 (XGA) with no performance impact
- Maximum source width = 768

3.4.2 Graphics and Video Acceleration Capabilities

3.4.2.1 2D Capabilities

2D Clipping Operation

The 2700G7 Multimedia Accelerator supports 2D clipping to a scissor rectangle within the drawing window. Objects are clipped to the rectangle that has the benefit of not processing pixels that fall outside the rectangle. Clipping in hardware reduces the need for software to clip objects; thus, improving performance. A scissor rectangle accelerates the clipping process by allowing the driver to clip to a bigger region, and allowing the hardware to clip to the exact window.

Anti-Aliasing

Aliasing is one of the artifacts that degrades image quality. In its simplest manifestation, aliasing causes the jagged staircase effects on sloped lines and polygon edges. Another artifact is the Moiré pattern that occurs as a result of a very small number of pixels available on the screen to contain the data of a high resolution texture map. More subtle effects are observed in animation, where very small primitives blink in and out of view. The 2700G7 Multimedia Accelerator supports Anti-Aliasing to reduce these effect.

Alpha Blending

The 2700G7 Multimedia Accelerator supports Alpha Blending which adds the property of transparency or opacity to an object. Alpha blending combines a source pixel color (RsGsBs) and alpha (As) component with a destination pixel color (RdGdBd) and alpha (Ad) component. Thus, a glass surface, for example, on top (source) of a red surface (destination) would allow much of the red base color to show through.

2D BLT Engine

The 2700G7 Multimedia Accelerator provides 2D hardware acceleration for block transfers of data (BLTs). The BLT engine provides the ability to copy a source block of data to a destination and perform operations on the data. For example, the StretchBLT engine is used to move source data to a destination that need not be the same size. Performing these common tasks in hardware reduces processor load which improves performance.

Using this BLT engine accelerates Graphical User Interfaces (GUIs). The 32-bit 2700G7 Multimedia Accelerator BLT Engine provides hardware acceleration for block transfers of pixel data for many common graphics operations. The term BLT refers to a block transfer of pixel data between memory locations.

As an example, the BLT engine could be used for the following:

- Move rectangular blocks of data between memory locations.
- Data alignment.
- Perform logical operations (raster operations – ROPs)

BLTs can be either opaque or transparent. Opaque transfers move the specified data to the destination. Transparent BLTs compare destination color to source color and write each location according to the mode of transparency selected.

Hardware is included for all 256 raster operations (Source, Pattern, and Destination) defined by Microsoft, including transparent BLT.

3.4.2.2 3D Capabilities

The 2700G7 Multimedia Accelerator is a tile-based rendering device. The screen is divided into tiles. After being transformed and lit by the processor, 3D object data (triangles) are sent to the 2700G7 Multimedia Accelerator. The 2700G7 Multimedia Accelerator tile accelerator determines the visibility of each triangle and arranges the triangles into tiles. The texturing engine then textures, blends, fogs and applies other effects to the 3D object data, and writes the final pixels to the frame buffer for each tile.

The 2700G7 Multimedia Accelerator offloads the processor and system bus of the compute and bandwidth intensive operations required for 3D texturing including: Z buffer compare, small object culling, off-screen and backface culling, tiling, texturing, filtering, and anti-aliasing.

Screen Tiling

The triangles from the processor are not sent to the graphics accelerator in any particular spatial order (e.g., the triangles are not sent from the upper left triangle to the lower right triangle – they are essentially sent in a random order). Tiling divides each scene into blocks, and processes each block independently. This allows the graphics controller to process spatially local triangles together. This allows the graphics accelerator to process a much smaller data set (e.g., one tile at a time, as opposed to the whole scene). The graphics accelerator can therefore perform much of the triangle processing internally for each tile; improving performance and reducing memory bandwidth requirements.

Figure 3-5. Tiling Example

Deferred Texturing

Deferred texturing improves performance by texturing only those pixels that are visible. Because the graphics controller is working with a smaller data set (a tile), it can perform the Z-compares for each pixel, before texturing that pixel (e.g., for each pixel, the texture engine will *first* determine which triangle is going to be visible, and then apply the appropriate texture). This prevents pixels from being textured twice. For α-blended textures, more than one triangle may be visible.

Fixed to Floating Conversion

The 2700G7 Multimedia Accelerator can accept fixed-point or floating-point object data; however, some of the internal calculations are processed using floating-point format. As such, if the 2700G7 Multimedia Accelerator is programmed to accept fixed-point object data, it will internally convert that data to floating-point format.

Small Object Culling

On a screen, the smallest visible element is a pixel. If a triangle fails to intersect with a pixel, it will not be drawn on the screen. Many triangles like this can occur in an image due to complex models that may be scaled, rotated, and transformed. The tile accelerator removes these unused triangles, reducing the number of triangles to be processed by the 3D core.

Off-Screen Culling

Not all triangles are inside the display area. Triangles outside of the screen area are not visible, and are removed.

Backface Culling

The 2700G7 Multimedia Accelerator discards triangles from further processing if they are facing away from the user's viewpoint. This operation, referred to as "Back Face Culling," is accomplished based on the "clockwise" or "counter-clockwise" orientation of the vertices on a primitive.

Perspective Correct Texture Support

A textured polygon is generated by mapping a 2D texture pattern onto each pixel of the polygon. A texture map is like wallpaper pasted onto the polygon. Since polygons are rendered in perspective, it is important that texture be mapped in perspective as well.

Texture Compression

Texture Compression reduces the bandwidth and power required to deliver textures. With larger textures, higher color depth, and multiple textures, it becomes increasingly important to provide a mechanism to compress textures and reduce system memory bus use. The 2700G7 Multimedia Accelerator uses a high-performance texture compression format compatible with OpenGL-ES*.

Mipmapping

Rather than providing a single texture, in a single resolution, that would be ideal for an object of a certain size being textured at a specific distance (Z), mipmapping allows an application to store several textures at varying resolutions. The graphics accelerator will pick the most appropriate texture from the mipmap for each pixel, based on the texture resolution required. This exact texture selected, and the resulting color of the pixel is dependent on the filtering mode being used.

Texture Mapping and Filtering

Many texture mapping modes are supported. Perspective correct mapping is always performed. As the map is fitted across the triangle, the map will be tiled. The way a texture is combined with other object attributes is also definable.

The 2700G7 Multimedia Accelerator supports up to twelve Levels-of-Detail (LODs) ranging in size from 2048x2048 to 1x1 texels. (A texel is defined as a texture map element). Textures do not have to be square.

The 2700G7 Multimedia Accelerator supports seven types of texture filtering:

- *Point Sampling:* Texel with coordinates nearest to the desired pixel is used. This mode only requires one level-of-detail to be present.
- *Bilinear Filtering:* A weighted average of the texels in a 2x2 area surrounding the desired pixel is used. This mode only requires one level-of-detail to be present.
- *Point Mipmapping:* This is used if many LODs are present. The nearest LOD is chosen and the texel with coordinates nearest to the desired pixel are used.
- *Bilinear Mipmapping*: This is used if many LODs are present. The nearest LOD is chosen and a weighted average of the texels in a 2x2 area surrounding the desired pixel is used.
- *Point Mipmapping Linear:* This is used if many LODs are present. Two appropriate LODs are selected and within each LOD, the texel with coordinates nearest to the desired pixel are selected. The final texture value is generated by linear interpolation between the two texels selected from each of the LODs.
- *Trilinear Mipmapping:* This is used if many LODs are present. Two appropriate LODs are selected and a weighted average of a 2x2 area of texels surrounding the desired pixel in each LOD is generated (four texels per LOD). The final texture value is generated by linear interpolation between the two texels generated for each of the LODs. Trilinear mipmapping is used to minimize the visibility of LOD transitions across an object.
- *Anisotropic Filtering:* This is used if many LODs are present. The nearest LOD-1 level will be determined for each of four sub-samples for the desired pixel. These four sub-samples are then bilinear filtered and averaged together.

Per Vertex Fogging

Fogging is used to create atmospheric effects (e.g., low visibility conditions), typically in simulator type applications. It adds another level of realism to computer-generated scenes. Fog can be used for depth cueing or hiding distant objects. With fog, distant objects can be rendered with fewer details (e.g., triangles), thereby improving the rendering speed or frame rate. Fog is simulated by attenuating the color of an object with the fog color as a function of distance; the greater the distance, the higher the density (lower visibility for distant objects).

3.4.2.3 Video Acceleration Capabilities

The 2700G7 Multimedia Accelerator has integrated the most computationally intensive portions of the video decode solution. The 2700G7 Multimedia Accelerator will perform Inverse Zig-Zag, Inverse Discrete Cosine Transform, and Motion Compensation for MPEG2*/MPEG4* video streams and also Motion Compensation for WMV*. The integration of these capabilities provides low power video decode while significantly reducing system bus traffic. Additionally, for higher resolutions, the hardware decode provides optimum performance.

Due to the nature of video signals, it is possible to highly compress video, transmit or store the compressed video, and then decompress the video without losing significant image quality. The very high compression ratios achievable with video, combined with the high-quality of the decompressed video, lead to the proliferation of compressed video formats that are common today. Examples of these video formats are MPEG2*, MPEG4*, and WMV*.

These formats primarily take advantage of two characteristics of video data. Video data tends to have low entropy within a frame. That is, pixels that are located adjacent to each other typically have similar color values. Additionally, subsequent video frames have significant redundancy. That is, frame *n* and frame *n+1* are typically similar.

To take advantage of low entropy within a frame, each frame is divided into blocks (usually 8 pixels x 8 pixels) and encoded using a discrete cosine transform. Then, the result of this transform is rearranged in a zig-zag format. The cosine transform is referred to as *DCT* (discrete cosine transform). The reversal of these processes (during decode) are *IDCT* (inverse discrete cosine transform) and *IZZ* (inverse zig-zag).

In addition to low entropy within a frame, the redundancy between frames is used to obtain higher compression. As an object moves across the screen in a video, approximately the same image appears at different locations. For example, a car moving across the screen to the right, first appears on the left of the screen, then in the center, then on the right. Rather than re-encode the entire object for each frame, a motion vector can be sent that describes the movement of the object. This process (both encoding and decoding) is referred to as *motion compensation* (MC).

Finally, each frame is not independently encoded. Rather, there are three types of frames:

I-Frames
I-frames (intra-coded frames) are completely encoded frames that can be decoded independently (e.g., no information from other frames is required).

P-Frames
P-frames (predicted frames) encode the difference between a single previous frame and the current P-frame. P-frames can be based on either I-frames or other P-frames.

B-Frames
B-frames (bi-directionally predicted frames) are based on two additional frames (one previous frame and one future frame). These frames can be either P-frames or I-frames. B-frames will never be used as the basis for another frame.

The details of the MPEG compression techniques are beyond the scope of this document. Refer to Scott Janus' *Video in the 21st Century*, Intel Press, 2002 (ISBN 0-9712887-5-5) for a detailed description of MPEG encode and decode.

The 2700G7 Multimedia Accelerator performs Inverse Zig-Zag (IZZ), Inverse Discrete Cosine Transforms (IDCT), and Motion Compensation in hardware to deliver MPEG video playback at 720 x 480 pixels (DVD quality) at greater than 30 frames/sec.

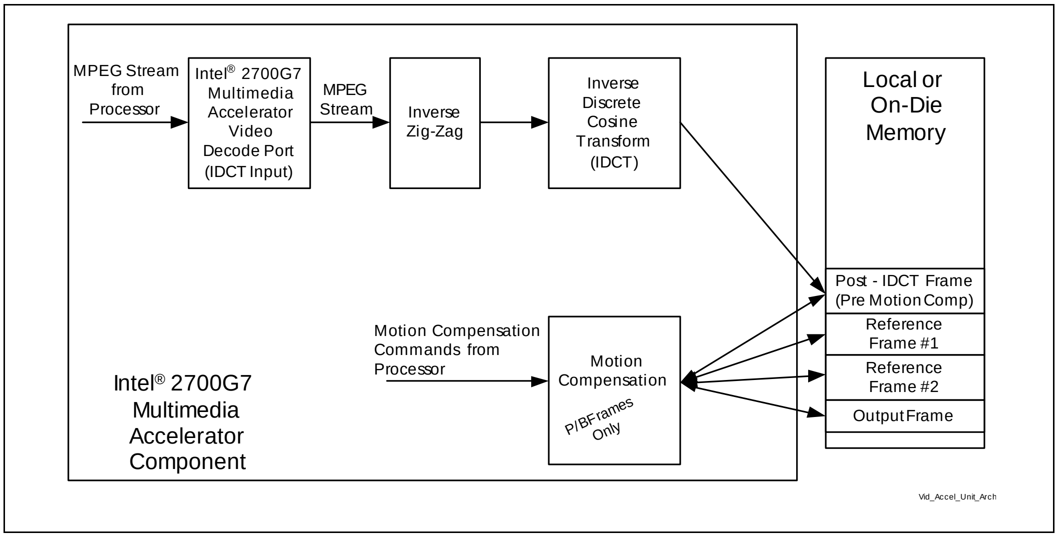
In addition to significantly reducing processor workload and power consumption, the hardware implementation of IZZ and IDCT in the 2700G7 Multimedia Accelerator reduces system bus bandwidth requirements by up to 95%. When using the 2700G7 Multimedia Accelerator, IZZ and IDCT are completed "on-the-fly".

Additionally, the Motion Compensation operations are performed in the local graphics memory, and, therefore, completely relieve the system bus of this traffic. The system bus bandwidth used by the 2700G7 Multimedia Accelerator for MPEG/WMV decode is approximately 4.5 MB/s for VGA resolution MPEG-4 decode at 30 frames per second.

After completing Motion Compensation, the resulting YUV 4:2:0 video can be converted to YUV 4:2:2 in the 2700G7 Multimedia Accelerator video decode unit. The YUV 4:2:2 data could be used as a video texture by the 2700G7 Multimedia Accelerator's 2D and 3D accelerator unit, as it is capable of texturing with YUV 4:2:2 textures.

Refer to Figure 3-6 for an architectural diagram of the 2700G7 Multimedia Accelerator's Video Acceleration Unit.

Figure 3-6. Intel® 2700G7 Multimedia Accelerator Video Acceleration Unit Architecture



3.4.3 2D and 3D Graphics Accelerator and Video Accelerator Data Formats

Table 3-1 describes the input and output formats from the 2D and 3D graphics accelerator and the video decode accelerator.

Table 3-1. 2D and 3D Graphics and Video Accelerator Formats

Format Type	Graphics Accelerator		Video Decode Accelerator
	2D	3D	
Input Formats	**(A)RGB** 4:4:4:4 5:5:5 5:5:5:1 5:6:5 8:8:8 8:8:8:8 **Palletized** 8-bit	**RGB Textures** 1:5:5:5 5:6:5 4:4:4:4 8:3:3:2 8:8:8 **YUV Textures** YUV 4:2:2	YUV 4:2:0
Output Formats	**RGB** 4:4:4:4 5:5:5 5:5:5:1 5:6:5 8:8:8 8:8:8:8 **Palletized** 8-bit	**RGB** 4:4:4:4 5:5:5 5:5:5:1 5:6:5 8:8:8 8:8:8:8 **Palletized** 8-bit	YUV 4:2:0 YUV 4:2:2 RGB 8:8:8

3.5 On-Die Frame Buffer

The 2700G7 Multimedia Accelerator has 704 KB of on-die memory that supports resolutions up to VGA (640 x 480 x 16 bpp, single buffered). When driving resolutions higher than those supported in the on-die memory, the 2700G7 Multimedia Accelerator uses a frame buffer stored in its stacked local memory. Additionally, video decode and 3D rendering will make use of the stacked local memory when needed. Using the on-die frame buffer saves significant power when refreshing the display (as compared to using the stacked, but off-die local memory).

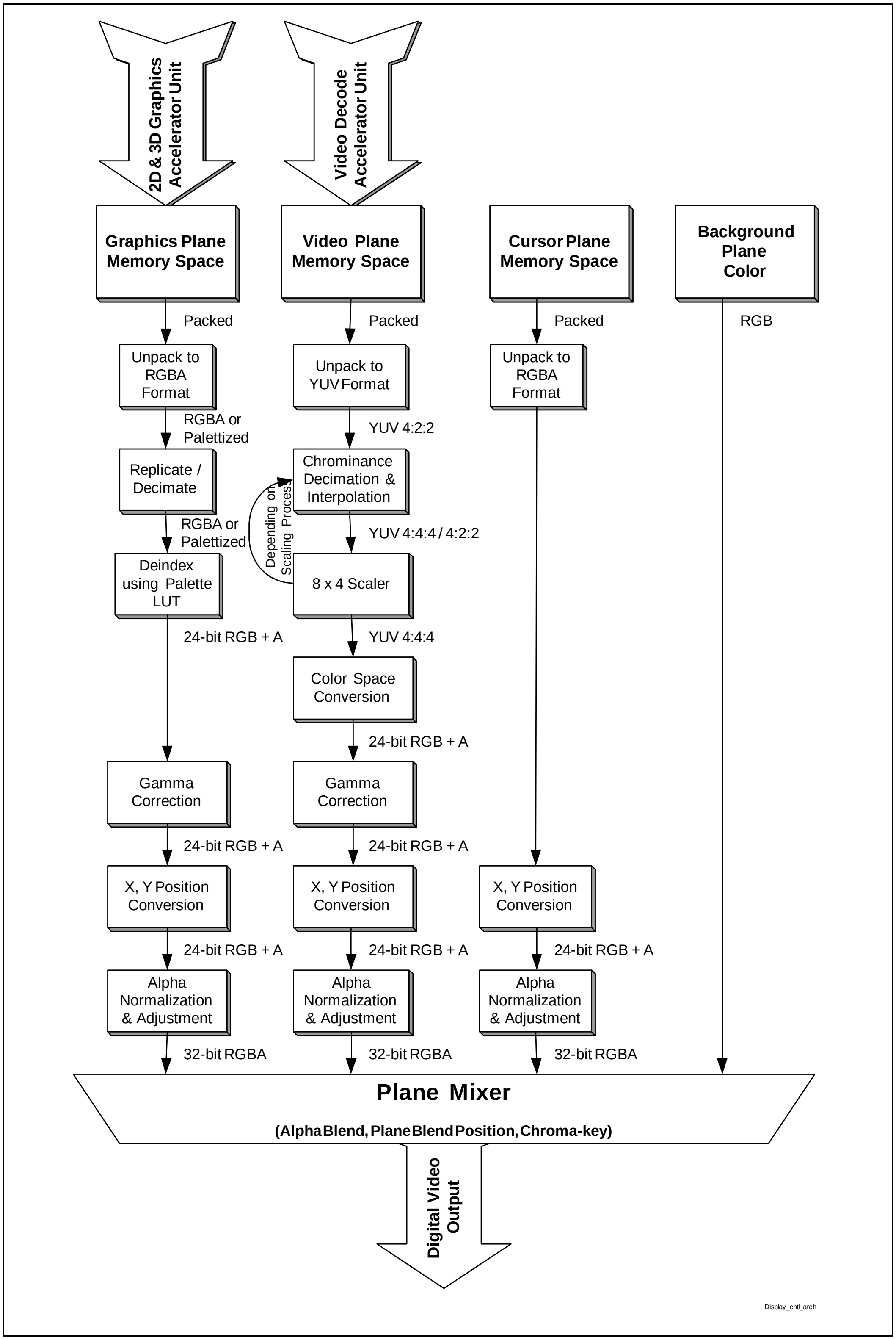
3.6 Intel® 2700G7 Multimedia Accelerator Display Controller

The integrated 2700G7 Multimedia Accelerator display controller is intended to support active LCDs as well as CRTs, TVs, and external digital displays (with external encoders). The display controller supports a graphics plane, a video plane, a cursor plane, and a background color. Data for the graphics plane is generated by the 2D and 3D accelerator functional blocks within the 2700G7 Multimedia Accelerator, while data for the video plane is driven by the video decode accelerator functional block within the 2700G7 Multimedia Accelerator.

3.6.1 Display Plane Architecture

Figure 3-7 shows the architecture of the 2700G7 Multimedia Accelerator display controller.

Figure 3-7. Intel® 2700G7 Multimedia Accelerator Display Controller Architecture



In addition to a solid color opaque background plane, there are three input streams (planes) that determine the color of each pixel that is sent to the display: graphics, video, and cursor. Each plane has a unique path through the display controller, tailored to the type of data represented in that plane. The four streams are combined by the mixer to create the final image that appears on the display. The mixer combines the streams based on their blend position (top, middle, bottom, background), alpha values, and chroma-key.

The graphics plane processes the RGB data delivered by the 2D and 3D graphics acceleration functional block within the 2700G7 Multimedia Accelerator. The display controller can replicate or decimate the graphics data, de-index a palletized image using the palette lookup table (LUT), perform gamma correction, and finally setup the data for combining by the mixer.

The video plane processes the YUV data delivered by the video decode accelerator functional block within the 2700G7 Multimedia Accelerator. YUV 4:2:2 data is converted to YUV 4:4:4 and scaled. After scaling, the YUV 4:4:4 data is color space converted to RGB. A global alpha value is added to allow alpha blending of the video if required. Finally, the data is setup for combining in the mixer.

The cursor plane allows for hardware cursor support. A cursor image can be placed in the cursor plane memory space, and the image will be combined with the other planes in the mixer. The cursor plane simply takes the cursor image and performs the setup for combining in the mixer.

The background color plane is used only if none of the other three planes fill a given pixel opaquely. The background plane is a solid color, with no alpha value (i.e., opaque) and always has the lowest blend position (i.e., below graphics, video, and cursor). Because the background plane has the lowest blend position, if any other plane fills a pixel opaquely, the background color will not be used when calculating the final color of that pixel.

3.6.2 Display Plane Formats and Capabilities

Each display plane accepts data formats based on the data type being delivered. Table 3-2 lists these data formats and the processing capabilities of each plane.

Table 3-2.Display Plane Formats and Capabilities

Parameter	Planes			
	2D and 3D Graphics Acceleration	Video	Cursor	Background
Default Position (programmable)	1 (bottom)	2 (middle)	3 (top)	4 (background)
Maximum Resolution	2048 x 2048	2048 x 2048	64 x 64	1 Color
RGB Formats	8 (palletized) 4:4:4:4 5:5:5:1 5:6:5 8:8:8 8:8:8:8	No	3:3:2 4:4:4:4 5:5:5:1	8:8:8
YUV Formats	No	4:2:0 4:2:2	No	No
Bits Per Pixel	8 16 24 32	12 16	8 16	24
Horizontal / Vertical Decimation / Replication	Yes	No	No	NA
Horizontal / Vertical Scaling	No	8 x 4 - Tap Programmable	No	NA
Palette LUT	24-bit x 256 LUT	No	No	NA
CSC	No	3 x 3 Matrix Programmable	No	No
Gamma Correction	Yes	Yes	No	No
Per-pixel α–Blending	1-Bit 4-Bit 8-Bit	No	1 Bit 4 Bit	No
Global α–Blending	8 Bit	8 Bit	8 Bit	No
Destination Color key	Yes	Yes	Yes	No

3.6.3 Graphics and Video Plane Gamma Correction

The graphics and video display planes include hardware RGB gamma correction. Refer to Figure 3-7 for a diagram of the display controller architecture. Gamma correction is performed separately for each color.

The gamma correction uses a programmable 17-entry lookup table (LUT). Table 3-3 provides an example LUT for gamma correction values of 1.0 (no correction) and 1.4. The upper-nibble (κ_G) of a color is used as the index into the LUT. The correction value corresponding to κ_G, and the value corresponding to κ+1 are interpolated based on the lower nibble of the original color value (α_G).

Table 3-3. LUT Example for Gamma Correction of 1.0 and 1.4

LUT index	Gamma = 1.0	Gamma = 1.4
0	0	0
1	16	35
2	32	57
3	48	77
4	64	95
5	80	111
6	96	127
7	112	141
8	128	156
9	144	169
10	160	182
11	176	195
12	192	208
13	208	220
14	224	232
15	240	244
16	255	255

The gamma corrected color value (for R, G, and B) is calculated by:

1) Lookup κ_G+1 in the LUT index column of Table 3-3.
2) Select the gamma value in the right columns of Table 3-3.
   This is T[κ_G+1].
3) Lookup κ_G in the LUT index column of Table 3-3.
4) Select the gamma value in the right columns of Table 3-3.
   This is T[κ_G].
5) Interpolate T[κ_G] and T[κ_G+1] using α_G.

As an example, assume an RGB color of R=135, G=222, and B=053 (all values are decimal) being gamma corrected using the gamma = 1.4 values in Table 3-3.

RED

1) κ_G = upper nibble of 135 = 8
2) α_G = lower nibble of 135 = 7
3) $T[\kappa_G]$ = 156
4) $T[\kappa_G+1]$ = 169
5) Interpolate $T[\kappa_G]$ & $T[\kappa_G+1]$

$$R' = T[\kappa_G] + (T[\kappa_G + 1] - T[\kappa_G]) \times \frac{\alpha_G}{16}$$

$$R' = 156 + (169 - 156) \times \frac{7}{16}$$

6) Resulting red value is: 162

The same process can be applied to the original G and B values to obtain the gamma corrected pixel color.

3.6.4 8 x 4-tap Video Scaler

The video plane has 8-tap horizontal and 4-tap vertical scalers. The horizontal scaler is fixed at 8-tap. The vertical scaler is programmable to either 2-tap or 4-tap. The vertical filter should be set to 2-tap when scaling down to less than 1/3 the height of the source image, but should otherwise be set to 4-tap for the best image quality.

Horizontal scaling factors of 8 down to 0.25 are supported (increase up to 8X or shrink by 4X). Horizontal scaling down to 0.125 can be achieved using horizontal decimation. Source images up to 768 pixels wide can be scaled. The maximum width of the output image is 1024 pixels.

Video Scaler Summary

Maximum Input Width:	768 pixels
Maximum Output Width:	1024 pixels
Maximum Upscale:	8X
Maximum Downscale:	4X (8X with decimation)

3.6.5 Video Plane Color Space Conversion

The video display plane includes a hardware color space converter. Refer to Figure 3-7 for a diagram of the display controller architecture. This color space conversion is fully programmable using a 3 x 3 matrix. The 2700G7 Multimedia Accelerator can yield accurate color replication on a wide range of displays, because the 2700G7 Multimedia Accelerator can adjust for the color primaries of any given display. The formulas used for color space conversion are:

R' = (Cry*(Y–16)/64 + Crv*(V–128)/64 + Cru*(U–128)/64)/4

G' = (Cgy*(Y–16)/64 + Cgv*(V–128)/64 + Cgu*(U–128)/64)/4

B' = (Cby*(Y–16)/64 + Cbv*(V–128)/64 + Cbu*(U–128)/64)/4

C(r,g,b)(y,u,v) are 11-bit signed integers. HDTV and SDTV conversion recommendations are listed in Table 3-4 and Table 3-5.

Table 3-4. HDTV YUV to R'G'B' Coefficient Example

Coefficient	Y	V	U
R	0x12A	0x1CB	0x000
G	0x12A	0x777	0x7C9
B	0x12A	0x000	0x21D

Table 3-5. SDTV YUV to R'G'B' Coefficient Example

Coefficient	Y	V	U
R	0x12A	0x199	0x000
G	0x12A	0x730	0x79C
B	0x12A	0x000	0x205

3.6.6 Plane Mixer Chroma-Key and α-Blend

The Plane Mixer (Refer to Figure 3-7) performs chroma-key and α-blend for the four display planes (graphics, video, cursor, and background).

The 24-bit chroma-key value is programmed independently for the graphics, video, and cursor planes (background does not support chroma-key). Chroma-key can be programmed using two different methods.

In the first method, the chroma-key value for a certain plane (e.g., graphics) is compared against each pixel in that plane. If a match is found, the previous plane’s pixel color is displayed (e.g., the pixel from the plane *below* the current plane). For example, this would allow for a “hole” in the middle of the graphics plane, in which a video was playing from the video plane (video plane behind graphics plane, graphics plane chroma-key = color of hole in graphics plane).

In the second method, the chroma-key value for a certain plane (e.g., graphics) is compared against each pixel in the previous plane (the plane below the current plane). If a match is found, the current plane's pixel color is displayed. For example, this would allow for every green pixel of the video plane to be replaced by the corresponding pixel in the graphics plane (video plane behind graphics plane, graphics plane chroma-key = green).

Additionally, a chroma-key mask is provided that allows certain bits of the chroma-key (and the color it is being compared to) to be ignored. This could, for example, be used to mask the least significant digits of the chroma-key to select a color range.

The plane mixer also performs α-blending on the display planes. The graphics, video, and cursor planes support global α values, and the graphics and cursor planes also support per-pixel α values. A single global α value is applied to all the pixels in a plane, while per-pixel α values vary for each pixel. Prior to α-blending the planes, the per-pixel α values for each pixel in the graphics and cursor planes are adjusted to account for the global alpha value for that plane.

The plane mixer blends based on the adjusted α value. Pixels with a α value of 0xFFh are opaque (the output pixel matches the current stream's pixel). Pixels with a α value of 0x00h are transparent (the output pixel matches the previous plane's pixel).

3.6.7 Display Controller Sync Control

The 2700G7 Multimedia Accelerator display controller has a fully programmable sync controller. The sync controller drives x_LCLK (HSYNC), x_FCLK (VSYNC), and x_DEN (Data Enable). The timing and polarity of these signals are programmable.

As with most displays, the 2700G7 Multimedia Accelerator display controller drives pixels in horizontal lines, starting in the upper-left corner of the display. The x_LCLK signal indicates the beginning of a new line, and the x_FCLK signal indicates the beginning of a new frame (reset to the upper-left corner).

There are three types of horizontal lines:

- Vertical Sync / Blanking Line
- Vertical Border Line
- Active Pixel Data Line

Each horizontal line is one of these types. The transitions between the three line types are timed, and based on the x_FCLK (VSYNC). Refer to Figure 3-8 for a diagram of display sync and data generation. Figure 3-9 details the timing of each horizontal line type with respect to x_FCLK. Refer to Figure 3-10, Figure 3-11, and Figure 3-12 for examples of each line type.

Each horizontal line may contain horizontal blanking, horizontal porch, horizontal border, and/or active display data types. Horizontal lines, other than vertical blanking lines, will contain more than one data type.

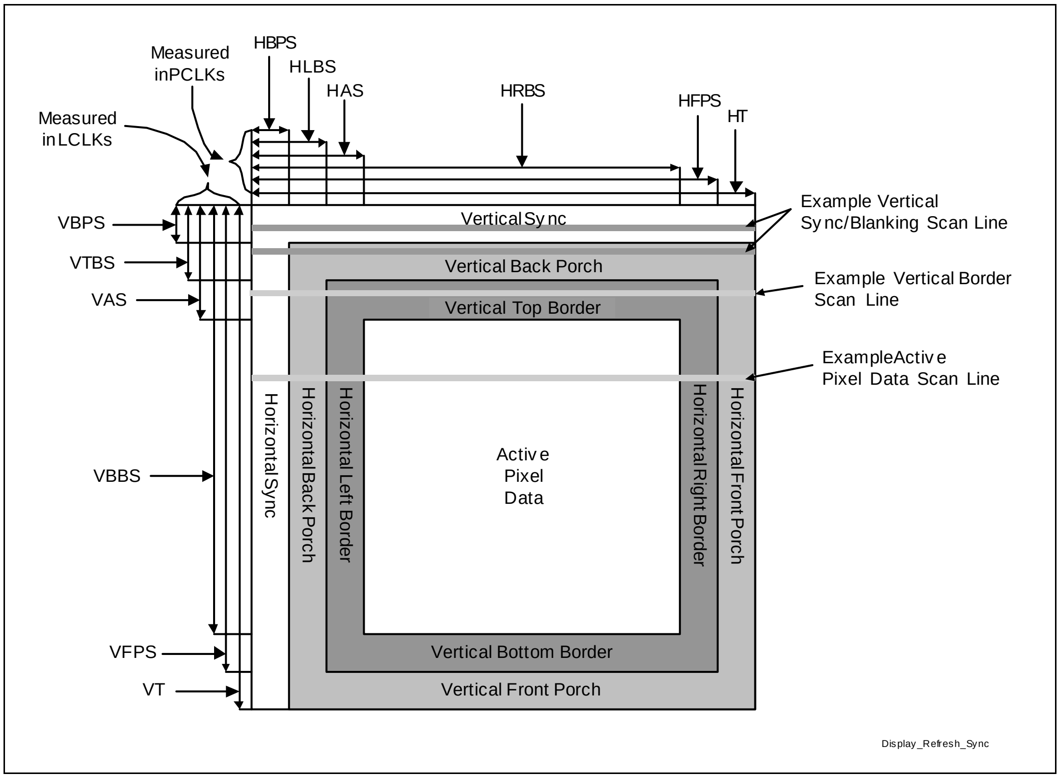
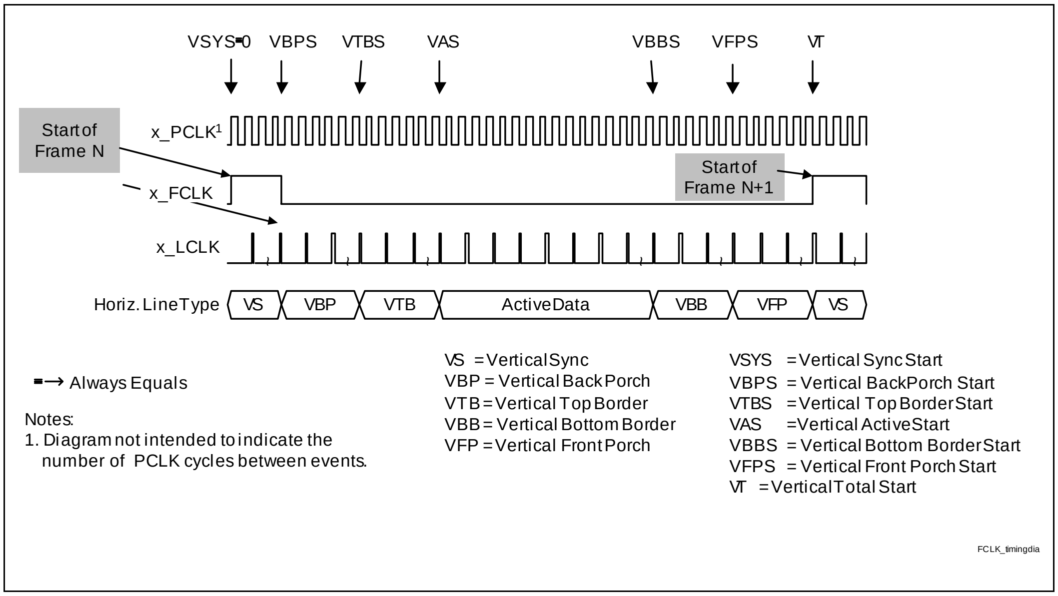


Figure 3-8. Display Refresh Sync / Data Generation

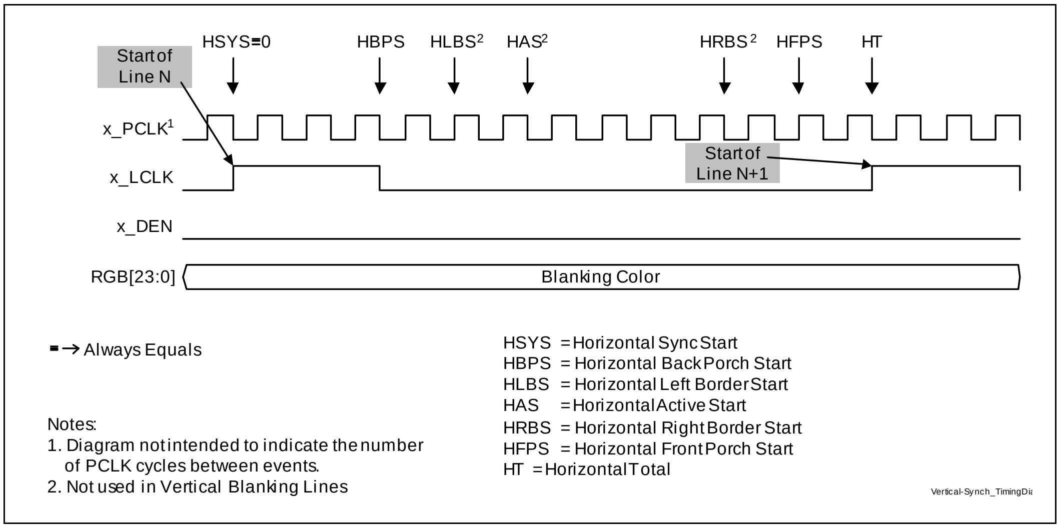
Note: Figure 3-9 thru Figure 3-12 assume x_FCLK, x_LCLK, and x_DEN are programmed as active high signals.

Figure 3-9. x_FCLK (VSYNC) Timing and Horizontal Line Types



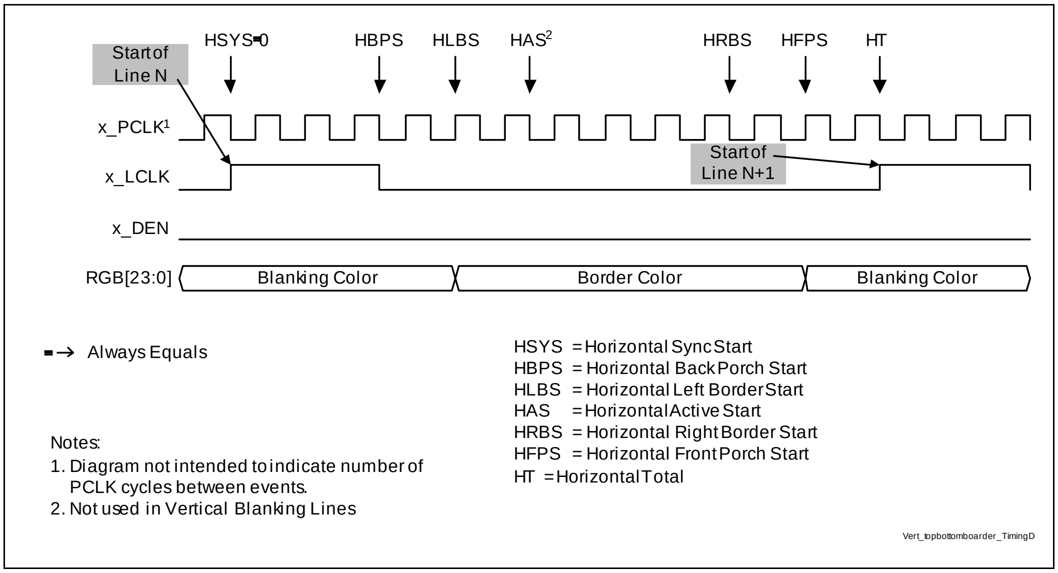
NOTE: All vertical and horizontal LCD timing parameters (e.g., VBPS, VTBS, VAS, VBBS, VFPS, VT) are cumulative. For the Vertical Top Border (VTB) to be zero lines, VTBS must equal VAS. The difference between VTBS and VAS is the width of the Vertical Top Border in lines.

Figure 3-10. Vertical Sync / Blanking Horizontal Line Draw (VS, VBP, VFP)



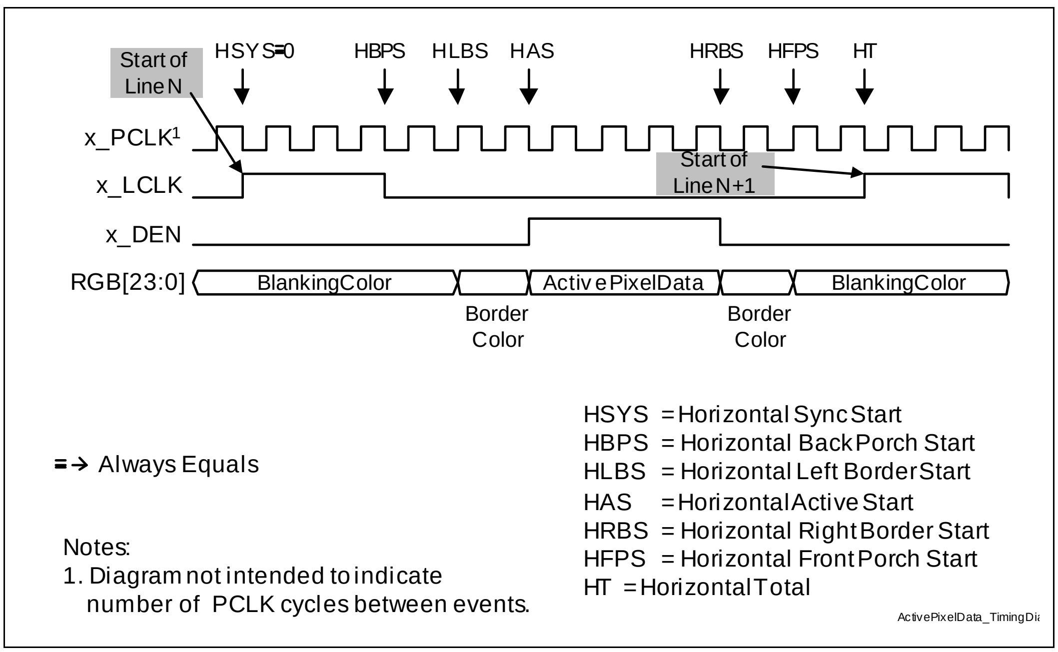
NOTE: All vertical and horizontal LCD timing parameters (e.g., HBPS, HLBS, HAS, HRBS, HFPS, HT) are cumulative. For the Horizontal Back Porch to be zero pixels, HBPS must equal HLBS. The difference between HBPS and HLBS is the width of the Horizontal Back Porch in pixels.

Figure 3-11. Vertical Top/Bottom Border Horizontal Line Draw



NOTE: All vertical and horizontal LCD timing parameters (e.g., HBPS, HLBS, HAS, HRBS, HFPS, HT) are cumulative. For the Horizontal Back Porch to be zero pixels, HBPS must equal HLBS. The difference between HBPS and HLBS is the width of the Horizontal Back Porch in pixels.

Figure 3-12. Active Pixel Data Horizontal Line Draw



NOTE: All vertical and horizontal LCD timing parameters (e.g., HBPS, HLBS, HAS, HRBS, HFPS, HT) are cumulative. For the Horizontal Back Porch to be zero pixels, HBPS must equal HLBS. The difference between HBPS and HLBS is the width of the Horizontal Back Porch in pixels.

VBPS, VTBS, VAS, VBBS, VFPS, VT, HBPS, HLBS, HAS, HRBS, HFPS, and HT are all controlled by registers programmable from 0 to 4095.

3.6.8 Display Controller Power Saving Features

In addition to supporting advanced internal power savings techniques (e.g., extensive, automatic clock gating) the 2700G7 Multimedia Accelerator display controller supports advanced refresh capabilities to reduce power consumption within the 2700G7 Multimedia Accelerator as well as the power consumption of the LCD interface and the LCD module. These modes are described in Sections 3.6.8.1 thru 3.6.8.7.

3.6.8.1 Reduced Refresh Rate

The 2700G7 Multimedia Accelerator display controller refresh rate can be reduced to 10 Hz (or lower). Reducing the refresh rates will save I/O power in the LCD interface as well as power consumption of the LCD module. The refresh rates supported by the LCD being used should be verified with the LCD vendor.

3.6.8.2 Reduced Color Mode

In reduced color mode, the least significant bits of each color are masked. The value placed in these bits can be programmed to be high or low. Each bit can be individually masked; however, the most common implementation would be to mask only the least significant bits.

3.6.8.3 Programmable Partial Display Refresh

The display controller can be programmed to only refresh a portion of the display. This would allow for a clock, or similar information, to be displayed without refreshing the entire display. This partial refresh can be set to refresh any rectangular portion of the display. The rest of the display would be driven with the blanking or border color. This will reduce the 2700G7 Multimedia Accelerator device power consumption, the interface power consumption, and the LCD module power consumption. This does not require a special LCD module.

3.6.8.4 Single-Shot, Software Initiated Display Refresh

Single-shot display refresh can be programmed to operate in two modes. A single display refresh can be initiated directly under software control via a register write to the 2700G7 Multimedia Accelerator. When not outputting a frame, RGB outputs will be set to the blanking level and the 2700G7 Multimedia Accelerator can be programmed to hold sync signals (x_FCLK and x_LCLK) in their inactive state.

Alternatively, the 2700G7 Multimedia Accelerator can be programmed to output one frame of every *n* frames. For example, the 2700G7 Multimedia Accelerator could be programmed to output every other frame. When not outputting frames, RGB outputs will be set to the blanking level and the 2700G7 Multimedia Accelerator can be programmed to hold sync signals (x_FCLK and x_LCLK) in their inactive state. In this mode (output 1 of *n* frames), sync related interrupts can be issued as if every frame was being output, as the timing is maintained internally for frames not being displayed (but the outputs are gated).

3.6.8.5 Reduced Blanking Display Refresh

The 2700G7 Multimedia Accelerator can operate with displays that use reduced blanking intervals. As seen in Figure 3-9, only a portion of the data sent out the display port is active display data. Reduced blanking displays reduce the amount of non-active data required. This improves the efficiency of the display interface, reducing the power needed for its operation.

3.6.8.6 Sync-Only Display Refresh

In sync-only display refresh mode, black or white (programmable) pixels will be substituted for the pixel data. All pixels (blanking, border and active) will be black or white. Valid sync signals will be driven.

3.6.8.7 Display Controller Power-Down Mode

In power-down mode, no display controller outputs will be driven. Pixel data, pixel clock, and sync signals will be stopped.

3.7 Primary and Auxiliary LCD Display Interface

The primary and auxiliary LCD display interfaces on the 2700G7 Multimedia Accelerator are functionally and electrically interchangeable. The LCD display interfaces will support active TFT LCDs with resolutions up to 1024 x 768 x 24 bpp @ 60 Hz. The 2700G7 Multimedia Accelerator can interface with 16-, 18-, or 24-bit displays.

The 2700G7 Multimedia Accelerator contains a programmable internal timing generator to supply the pixel clock, line clock (horizontal sync), frame clock (vertical sync), and data enable. The 2700G7 Multimedia Accelerator should be programmed to provide the correct timings to the display that is being driven by the 2700G7 Multimedia Accelerator LCD controller. In Accelerated Dual-Display Mode, the timings for the display being driven by the applications processor’s LCD controller should be programmed in the applications processor. The 2700G7 Multimedia Accelerator will pass these timings though to the display.

The intent is for the primary LCD display (e.g., the LCD on a PDA) to be connected to the primary LCD display interface, and the drivers will be written to support this configuration.

3.7.1 LCD Clocking

LCD data outputs can be switched on either the rising or the falling edge of the associated PCLK. Note that this does not directly correspond to the clocking requirements at the receiver side. If the receiver (e.g., LCD) latches incoming data on the rising edge of PCLK, the 2700G7 Multimedia Accelerator should be programmed to switch its LCD data outputs on the falling edge of PCLK. This allows the data to be centered (with proper setup and hold times) with respect to PCLK.

3.7.2 Pulse Width Modulators

To allow control of the LCD backlight independent of the state of the application processor, the 2700G7 Multimedia Accelerator provides two independently programmable pulse width modulators (PWMs). While one PWM is intended for the primary LCD output and the second

PWM is intended for the auxiliary LCD output, they are functionally and electrically interchangeable.

The pulse width modulator frequency is based on the 13 MHz external input clock. The PWM output waveform is configured via three registers:

- 6-bit reference clock pre-divider
- 10-bit period counter
- 10-bit pulse with counter

The period counter and pulse width counter will be incremented by the divided reference clock. The frequency range supported is 198.3 Hz to 6.5 MHz.

The intent is for LCD1_PWM to be used with the primary LCD output (e.g., the LCD on a PDA) and for LCD2_PWM to be used with the auxiliary LCD output, and the drivers will be written to support this configuration.

3.8 Local Memory Support

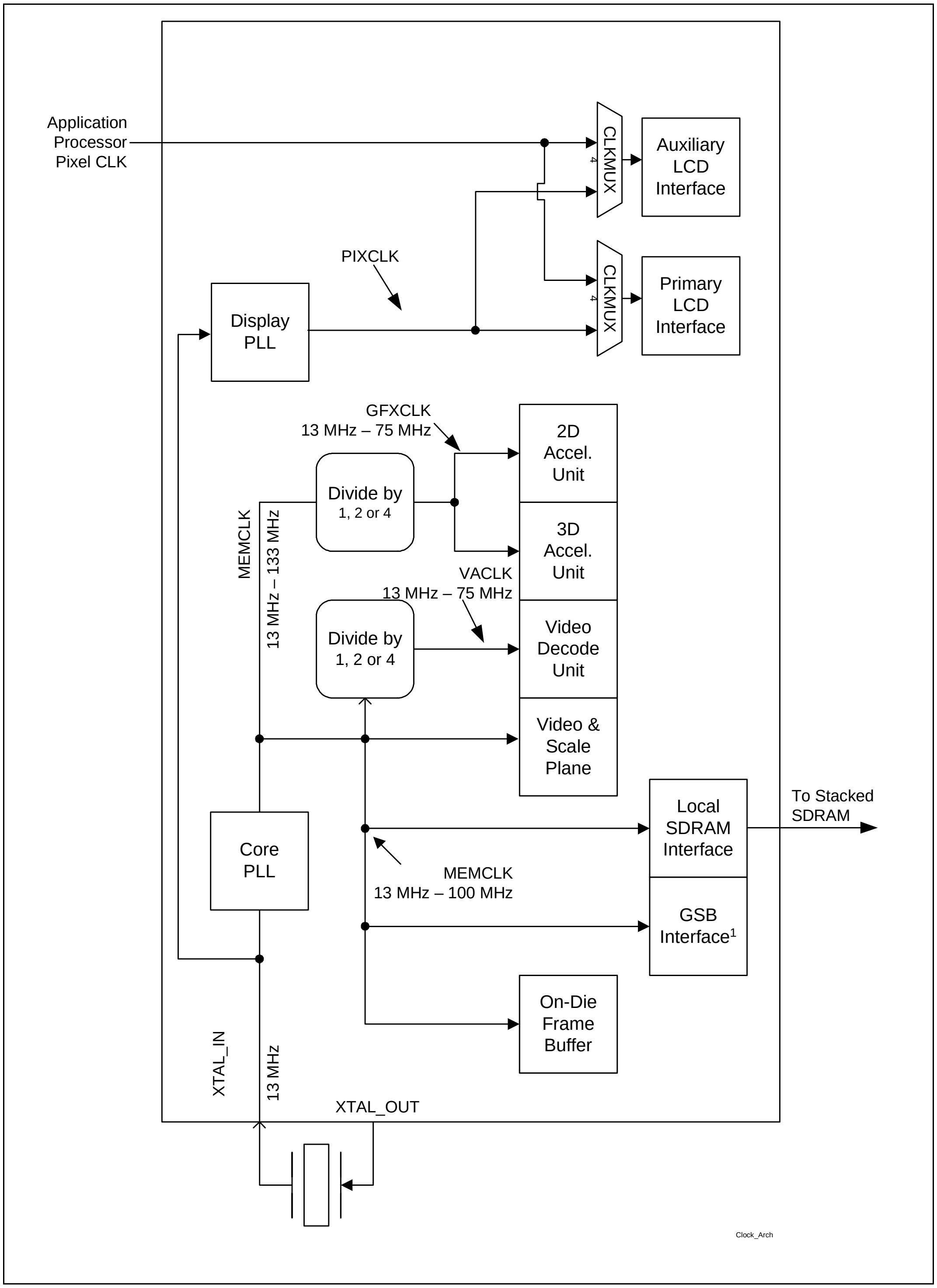
The 2700G7 Multimedia Accelerator’s stacked 16 MB local memory of SDRAM has the following characteristics:

- 100 MHz LP-SDRAM device
- 13 MHz – 100 MHz dynamic interface frequency
- 1.8 V core and I/O voltage (VCC_SDRAM)
- 32-bit data interface
  - Two x16 devices
- 16 MB stacked memory
- 2-bit bank address, 12-bit row address, 8-bit column address
- SDRAM self-refresh mode, partial refresh mode, power down and deep power down

3.9 Clock Generation

Figure 3-13 shows the clocking solution internal to the 2700G7 Multimedia Accelerator component.

Figure 3-13. Intel® 2700G7 Multimedia Accelerator Component Clocking



NOTES:

1. Clock can be gated to each functional block, except GSB which is required for wake.
2. Each PLL can be disabled.
3. Each clock divider can be set to divide by 1, 2 or 4.
4. The applications processor's pixel clock is used when LCD data driven by application processor; PXLCLK used when LCD data driven by the 2700G7 Multimedia Accelerator.

Table 3-6 shows some example clock frequency options based on the clocking architecture documented in Figure 3-13. Table 3-6 is an example only, many more combinations are achievable.

Table 3-6. Example Intel® 2700G7 Multimedia Accelerator Clock Frequency Options

SDRAMCLK (MHz)	2D Unit (MHz)	3D Unit (MHz)	Video Unit (MHz)
100	50	50	50
100	Gated	Gated	50
100	50	50	Gated
100	50	Gated	Gated
75	75	75	75
75	Gated	Gated	75
75	75	75	Gated
75	37.5	Gated	Gated
75	18.75	Gated	Gated
66	66	66	66
66	33	Gated	33
66	Gated	Gated	66
50	Gated	Gated	50
50	50	Gated	Gated
50	25	Gated	Gated
13	13	Gated	Gated

In addition, the pixel clock from the 2700G7 Multimedia Accelerator's display PLL is highly programmable and should be set based on the display resolution, refresh rate, and blanking intervals required.

3.10 General Purpose I/O Signals (GPIOs)

The 2700G7 Multimedia Accelerator has two software controllable GPIO signals. Using a system register, these pins are programmable as either input-only (GPIs) or input/output (GPIOs). In GPIO mode, these signals can be programmed to drive high, drive low, or tri-state via a system register. In both GPI and GPIO modes, the state of the GPIO signals will be reflected in the 2700G7 Multimedia Accelerator register.

3.11 JTAG

The 2700G7 Multimedia Accelerator includes a JTAG port and controller for boundary scan purposes. The 2700G7 Multimedia Accelerator has integrated internal pull-ups on the JTAG_nTRST, JTAG_TDI, and JTAG_TMS signals, per the IEEE 1149.1 standard. JTAG_TCK requires an external pull-down, whether the 2700G7 Multimedia Accelerator's JTAG interface is being used or not. For BSDL files to run boundary scan on the 2700G7 Multimedia Accelerator, contact your Intel field representative.

4 Register Description

The Intel 2700G7 Multimedia Accelerator contains sets of configuration registers for local memory, clocks, LCD port control, frame buffer control, GPIO control, pulse width modulator control, and device identification. This chapter provides detailed bit field descriptions of these registers.

4.1 Register Terminology

Term	Description
RO	Read Only. If a register is read only, writes to this register location have no effect.
WO	Write Only. If a register is write only, reads to this register location return undefined data.
R/W	Read/Write. A register with this attribute can be read and written.
Reserved Bits	Some of the registers described in this chapter contain reserved bits. These bits are labeled Reserved. Software must deal correctly with fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions, and then written back.
Default Value upon Reset	Upon reset, the 2700G7 Multimedia Accelerator sets all of its internal configuration registers to predetermined default states. Some register values at reset are determined by external strapping options. The default state represents the minimum functionality feature set required to successfully bring up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software to properly determine the SDRAM configurations, operating parameters, and optional system features that are applicable, and to program the 2700G7 Multimedia Accelerator registers accordingly.

4.2 Register Memory Address Map

The 2700G7 Multimedia Accelerator and its stacked local memory are mapped to an address range of 64 MB. The registers used to control the 2700G7 Multimedia Accelerator reside in the highest 128 KB of the 64 MB space, at offsets of 0x03FE_0000 thru 0x03FF_FFFF. To allow the 2700G7 Multimedia Accelerator to work with a single 64 MB range the on-die frame buffer and registers are overlaid on the external (system) SDRAM within the memory space at offsets 0x0 thru 0x03FE_0000.

The full 64 MB range is visible to the application processor. The 2700G7 Multimedia Accelerator itself has a 32 MB address range and so is only able to access the bottom 32 MB of the map. The on-die frame buffer may be disabled and accesses routed out to external (system) SDRAM.

All accesses are 32 bit accesses. All addresses in this chapter are byte addresses.

Figure 4-1. Intel® 2700G7 Multimedia Accelerator Memory Map

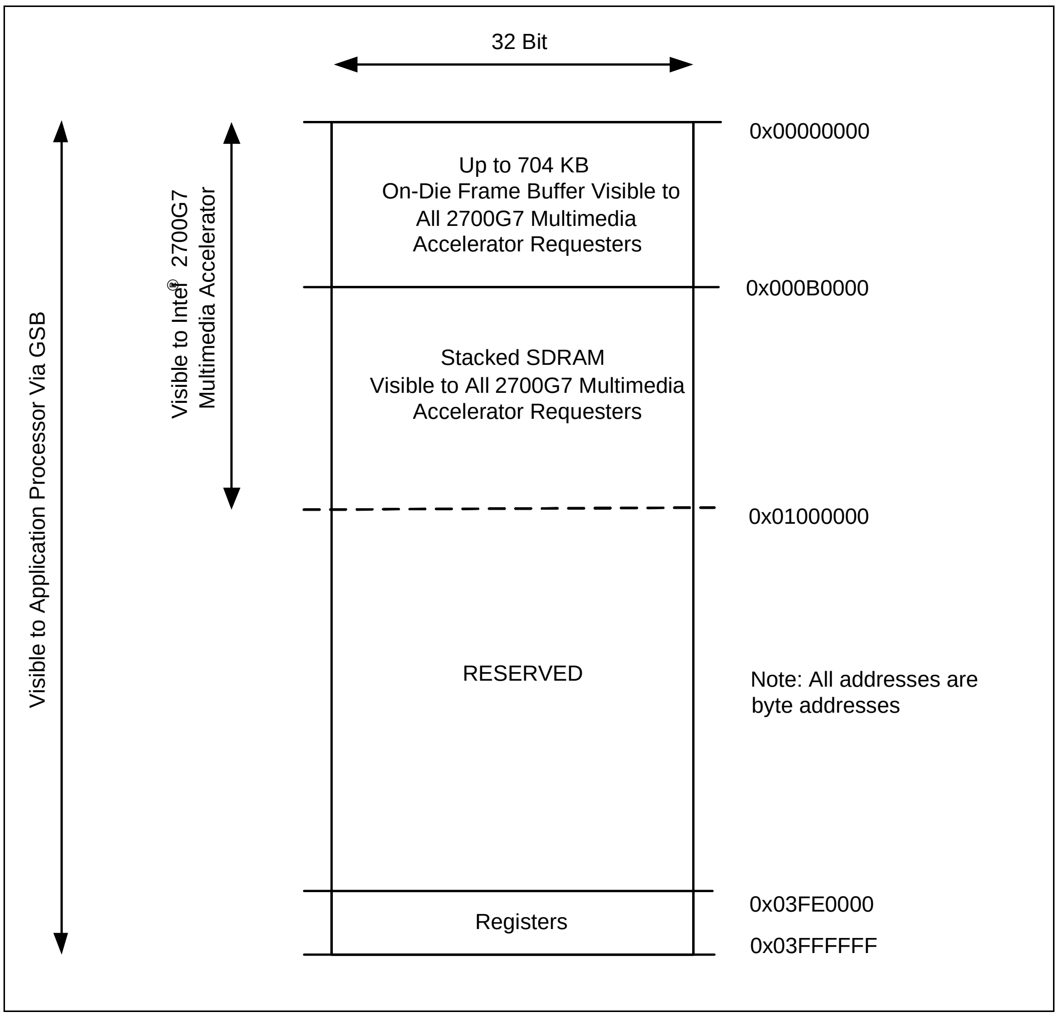


Table 2. Memory Mapped Registers

Address Offset	Symbol	Description	Section
System Configuration Registers (0x03FE_0000 – 0x03FE_0010)			
0x03FE_0000	SYSCFG	General System Bus Configuration	4.3.1
0x03FE_0004	PFBASE	Pre-Fetch Ahead Base Address	4.3.2
0x03FE_0008	PFCEIL	Pre-Fetch Ceiling Address	4.3.3
0x03FE_000C	POLLFLAG	POLL_FLAG Pin Control	4.3.4
0x03FE_0010	SYSRST	System Reset Control	4.3.5
Interrupt Control Registers (0x03FE_0014 – 0x03FE_002F)			
0x03FE_0014	NINTPW	NINT Pulse Width Configuration	4.4.1
0x03FE_0018	MINTENABLE	Master interrupt Enable	4.4.2
0x03FE_001C	MINTSTAT	Mater Interrupt Status	4.4.3
0x03FE_0020	SINTENABLE	System interrupt Enable	4.4.4
0x03FE_0024	SINTSTAT	System Interrupt Status	4.4.5
0x03FE_0028	SINTCLR	System Interrupt Clear	4.4.6
Clock Control Registers (0x03FE_00u2C – 0x03FE_005F)			
0x03FE_002C	SYSCLKSRC	SYSCLK Source Control	4.5.1
0x03FE_0030	PIXCLKSRC	PIXCLK Source Control	4.5.2
0x03FE_0034	CLKSLEEP	Clock Disable	0
0x03FE_0038	COREPLL	CORE PLL Configuration	4.5.4
0x03FE_003C	DISPPLL	Display PLL Configuration	4.5.5
0x03FE_0040	PLLSTAT	PLL Status	4.5.6
0x03FE_0044	VOVRCLK	Video and Scale Clock Control	4.5.7
0x03FE_0048	PIXCLK	LCD Pixel Clock Control	4.5.8
0x03FE_004C	MEMCLK	Memory Clock Control	4.5.9
0x03FE_0058	SDCLK	SDRAM Clock Control	4.5.10
0x03FE_005C	PIXCLKDIV	PIXCLK Divisor	4.5.11
LCD Port Control Register (0x03FE_0060 – 0x03FE_006F)			
0x03FE_0060	LCD_CONFIG	LCD Configuration	4.6.1
On-Die Frame Buffer Registers (0x03FE_0064 – 0x03FE_006B)			
0x03FE_0064	ODFBPWR	On-Die Frame Buffer Power Control	4.7.1
0x03FE_0068	ODFBSTAT	On-Die Frame Buffer Power Status	4.7.2

Address Offset	Symbol	Description	Section
GPIO Registers (0x03FE_006C – 0x03FE_007F)			
0x03FE_006C	GPIOCGF	GPIO Configuration	4.8.1
0x03FE_0070	GPIOHI	GPIO High Output	4.8.2
0x03FE_0074	GPIOLO	GPIO Low Output	4.8.3
0x03FE_0078	GPIOSTAT	GPIO Input Status	4.8.4
Pulse Width Modulator (PWM) Registers (0x03FE_0200 – 0x03FE_02FF)			
0x03FE_0200	PWMRST	PWM Soft Reset Control	4.9.1
0x03FE_0204	PWMCFG	PWM Configuration	4.9.2
0x03FE_0210	PWM0DIV	PWM 0 Pre-Scale Divisor	4.9.3
0x03FE_0214	PWM0DUTY	PWM 0 Duty Cycle Control	4.9.4
0x03FE_0218	PWM0PER	PWM Period Control	4.9.5
0x03FE_0220	PWM1DIV	PWM 1 Pre-Scale Divisor	4.9.6
0x03FE_0224	PWM1DUTY	PWM 1 Duty Cycle Control	4.9.7
0x03FE_0228	PWM1PER	PWM 1 Period Control	4.9.8
Identification (ID) Registers (0x03FE_0300 – 0x03FE_0FFF)			
0x03FE_0FF0	ID	Identification	4.10.1
Local Memory (SDRAM) Registers (0x03FE_1000 – 0x03FE_1FFF)			
0x03FE_1000	LMRST	Local Memory (SDRAM) Reset	4.11.1
0x03FE_1004	LMCFG	Local Memory (SDRAM) Configuration	4.11.2
0x03FE_1008	LMPWR	Local Memory (SDRAM) Power Control	4.11.3
0x03FE_100C	LMPWRSTAT	Local Memory (SDRAM) Power Status	4.11.4
0x03FE_1010	LMCEMR	Local Memory (SDRAM) EMR Control	4.11.5
0x03FE_1014	LMTYPE	Local Memory (SDRAM) Type	4.11.6
0x03FE_1018	LMTIM	Local Memory (SDRAM) Timing	4.11.7
0x03FE_101C	LMREFRESH	Local Memory (SDRAM) t_{REF} Control	4.11.8
0x03FE_1020	LMPROTMIN	Local Memory (SDRAM) Protection Minimum Address	4.11.9
0x03FE_1024	LMPROTMAX	Local Memory (SDRAM) Protection Maximum Address	4.11.10
0x03FE_1028	LMPROTCFG	Local Memory (SDRAM) Protection Configuration	4.11.11
0x03FE_102C	LMPROTERR	Local Memory (SDRAM) Protection Error Status	4.11.12

Address Offset	Symbol	Description	Section
Plane Controller Registers (0x03FE_2000 – 0x03FE_2FFF)			
0x03FE_2000	GSCTRL	Graphics Surface Control	4.12.1.1
0x03FE_2004	VSCTRL	Video Surface Control	4.12.2.1
0x03FE_2020	GBBASE	Graphics Blending Base	4.12.1.2
0x03FE_2024	VBBASE	Video Blending Base	4.12.2.2
0x03FE_2040	GDRCTRL	Graphics Decimation Replication Control	4.12.1.3
0x03FE_2044	VCMSK	Video Color Key Mask	4.12.2.3
0x03FE_2060	GSCADR	Graphics Stream Control Address	4.12.1.4
0x03FE_2064	VSCADR	Video Stream Control Address	4.12.2.4
0x03FE_2084	VUBASE	Video U Base	4.12.2.5
0x03FE_20A4	VVBASE	Video V Base	4.12.2.6
0x03FE_20C0	GSADR	Graphics Stride Address	4.12.1.5
0x03FE_20C4	VSADR	Video Stride Address	4.12.2.7
0x03FE_2100	HCCTRL	Hardware Cursor Control	4.12.4.1
0x03FE_2110	HCSIZE	Hardware Cursor Size	4.12.4.2
0x03FE_2120	HCPOS	Hardware Cursor Position	4.12.4.3
0x03FE_2130	HCBADR	Hardware Cursor Blend Address	4.12.4.4
0x03FE_2140	HCCKMSK	Hardware Cursor Color Key Mask	4.12.4.5
0x03FE_2150	GPLUT	Graphics Palette LUT	4.12.1.6
0x03FE_2154	DSCTRL	Display Sync Control	4.13.1
0x03FE_2158	DHT01	Display Horizontal Timing Register 01	4.13.3
0x03FE_215C	DHT02	Display Horizontal Timing Register 02	4.13.4
0x03FE_2160	DHT03	Display Horizontal Timing Register 03	4.13.5
0x03FE_2164	DVT01	Display Vertical Timing Register 01	4.13.6
0x03FE_2168	DVT02	Display Vertical Timing Register 02	4.13.7
0x03FE_216C	DVT03	Display Vertical Timing Register 03	4.13.8
0x03FE_2170	DBCOL	Display Border Color	4.13.13
0x03FE_2174	BGCOLOR	Background Color	4.12.3.1
0x03FE_2178	DINTRS	Display Interrupt Status	4.13.17
0x03FE_217C	DINTRE	Display Interrupt Enable	4.13.18
0x03FE_2180	DINTRCNT	Display Interrupt Control	4.13.19
0x03FE_2184	DSIG	Display Signature	4.13.14
0x03FE_2188	DMCTRL	Display Memory Control	4.13.16
0x03FE_218C	CLIPCTRL	Clipping Control	4.14.1
0x03FE_2190	SPOCTRL	Scale Pitch/Order Control	4.14.2

Address Offset	Symbol	Description	Section
0x03FE_2194	SVCTRL	Scale Vertical Control	4.14.3
0x03FE_2198–0x03FE_21A8	VSCOEFF[0:4]	Video Scalar Vertical Coefficient [0:4]	4.14.5
0x03FE_21B0	SHCTRL	Scale Horizontal Control	4.14.4
0x03FE_21B4–0x03FE_21D4	HSCOEFF[0:8]	Video Scalar Horizontal Coefficient [0:8]	4.14.7
0x03FE_21D8	SSSIZE	Scale Surface Size	4.14.6
0x03FE_2200–0x03FE_2240	VIDGAM[0:16]	Video Gamma LUT Index [0:16]	4.15.2
0x03FE_2250–0x03FE_2290	GFXGAM[0:16]	Graphics Gamma LUT Index [0:16]	4.15.3
0x03FE_2300	DLSTS	Display Load Status	4.13.20
0x03FE_2304	DLLCTRL	Display List Load Control	4.13.21
0x03FE_2308	DVLNUM	Display Vertical Line Number	4.13.15
0x03FE_230C	DUCTRL	Display Update Control	4.13.2
0x03FE_2310	DVECTRL	Display Vertical Event Control	4.13.9
0x03FE_2314	DHDET	Display Horizontal DE Timing	4.13.10
0x03FE_2318	DVDET	Display Vertical DE Timing	4.13.11
0x03FE_231C	DODMSK	Display Output Data Mask	4.13.12
0x03FE_2330	CSC01	Color Space Coefficient Register 01	4.16.2
0x03FE_2334	CSC02	Color Space Coefficient Register 02	4.16.3
0x03FE_2338	CSC03	Color Space Coefficient Register 03	4.16.4
0x03FE_233C	CSC04	Color Space Coefficient Register 04	4.16.5
0x03FE_2340	CSC05	Color Space Coefficient Register 05	4.16.6

4.3 System Configuration Registers

These registers allow the 2700G7 Multimedia Accelerator to be configured for use in a specific design.

4.3.1 SYSCFG—General System Bus Configuration Register

Offset:	0x03FE_0000
Default Value:	0x00000000
Access:	R/W, RO
Size:	32 bits

This register is used to configure the general system bus, including drive strength and read prefetch for acceleration of burst read transactions. This register also allows the nINT and POLL_FLAG outputs to be tri-stated. SYSRDY and SYSMD are automatically tri-stated when the device is not selected via SYSCS0 or SYSCS1.

Bits	Access	Name	Description
31:8	R/W	SYS_TO_CNT	**System Timeout Count.** This bit is a general system bus timeout count. Number of SYSCLK cycles before GSB access is aborted. 000000000000000000000000b = timeout disabled any other value = timeout enabled when the specified number of SYSCLK cycles occurs
7:4	R/W	RSVD	Reserved
3	R/W	MISC_DS	**nINT and POLL_FLAG Drive Strength.** 0b = 3 mA at all I/O voltages (default) 1b = 6 mA at 1.8 V or 10 mA at 2.5 V / 3.3 V
2	R/W	SYSD_DS	**General System Bus (Data) Drive Strength.** 0b = 3 mA at all I/O voltages (default) 1b = 6 mA at 1.8 V or 10 mA at 2.5V / 3.3 V
	RO	SYSR_DS	**SYSRDY Drive Strength.** Read-only; writes to this bit have no effect. This is set using a hardware strap on Pin LDC1_DD1. See the *Intel® 2700G7 Multimedia Accelerator Design Guide* for more information. 0b = Drive strength power up configuration is 3 mA at all I/O voltages 1b = Drive strength power up configuration is 6 mA at 1.8 V or 10 mA at 2.5 V / 3.3 V
0	R/W	PREFET_EN	**Prefetch Enable.** This bit defines the prefetch on read behavior. The prefetching performs address wrapping for cache-line fill operations. 0b = Disabled (default) 1b = Enabled

4.3.2 PFBASE— Pre-Fetch Ahead Base Address Register

Offset:	0x03FE_0004
Default Value:	0x00000000
Access:	R/W
Size:	32 bits

This register defines the base of the region for pre-fetching. This register is meaningful only when the PREFETCH_MODE is enabled. Note that bits 4:0 will always read as zero and will always write as zero, since pre-fetch accesses to and from the 2700G7 Multimedia Accelerator local memory must be 32 byte aligned. The base address can be set in the range 0x0 to 0x03FDFFDF (i.e., within the local memory region but excluding the 2700G7 Multimedia Accelerator registers). The default base address is 0x0.

Bits	Access	Name	Description
31:26	R/W	RSVD	Reserved
25:0	R/W	PREFET_ BASE	**Prefetch Base Address.**

4.3.3 PFCEIL— Pre-Fetch Ceiling Address Register

Offset:	0x03FE_0008
Default Value:	0x03FDFFE0
Access:	R/W
Size:	32 bits

This register defines the ceiling of the region for pre-fetching. This register is meaningful only when the PREFETCH_MODE is enabled. Note that bits 4:0 will always read as zero and will always write as zero, since pre-fetch accesses to and from 2700G7 Multimedia Accelerator local memory must be 32 byte aligned. The ceiling address can be set in the range 0x20 to 0x03FDFFF0 (i.e., within the local memory region but excluding the 2700G7 Multimedia Accelerator registers). The address must be greater than PREFETCH_BASE. The default ceiling address is 0x03FDFFE0.

Bits	Access	Name	Description
31:26	R/W	RSVD	Reserved
25:0	R/W	PREFET_ BASE	**Prefetch Ceiling Address.**

4.3.4 POLLFLAG—POLL_FLAG Pin Control Register

Offset:	0x03FE_000C
Default Value:	0x00000000
Access:	R/W
Size:	32 bits

This register enables the slave port FIFO level of each module to be monitored via an external signal (POLL_FLAG). The POLL_FLAG pin is always low if disabled. The signal asserts high when the selected FIFO goes above the threshold level set.

Bits	Access	Name	Description
31:17	R/W	RSVD	Reserved
16:8	R/W	PFLG_ THRHLD	**POLL_FLAG Threshold.** This field sets the threshold level at which the POLL_FLAG pin will assert. The legal range is dependant on PFLG_SEL field. 0 to 64 DWords for Video Decode command buffer 0 to 64 DWords 0 to 64 DWords for Video Decode IDCT buffer 0 to 64 DWords for Video Decode IZZ buffer 0 to 512 DWords for TA buffer (Control, Data, and 2D combined)
7:3	R/W	RSVD	Reserved
2:0	R/W	PFLG_SEL	**POLL_FLAG Select.** This field selects the source for the POLL_FLAG pin: 000b = POLL_FLAG disabled (default) 001b = Video Decode command buffer 010b = Video Decode IDCT buffer 011b = Video Decode IZZ buffer 100b = TA buffer (Control, Data and 2D combined) 101b = Reserved 110b = Reserved 111b = Reserved

4.3.5 SYSRST—System Reset Control Register

Offset: 0x03FE_0010
Default Value: 0x00000000
Access: R/W
Size: 32 bits

This is the overall system soft reset register. All modules are reset when this register is set, including the general system bus (GSB) interface. Write a 1 to reset the whole device. No register reads or writes are allowed for 32 REFCLK cycles after writing to this register. All registers will be set to their default “reset” value. This is equivalent to a hard reset via the nRESET_IN pin.

Bits	Access	Name	Description
31:1	R/W	RSVD	Reserved
0	R/W	SYS_RST	**System Reset.** 0b = Device active (default) 1b = Reset activated for 32 REFCLK cycles

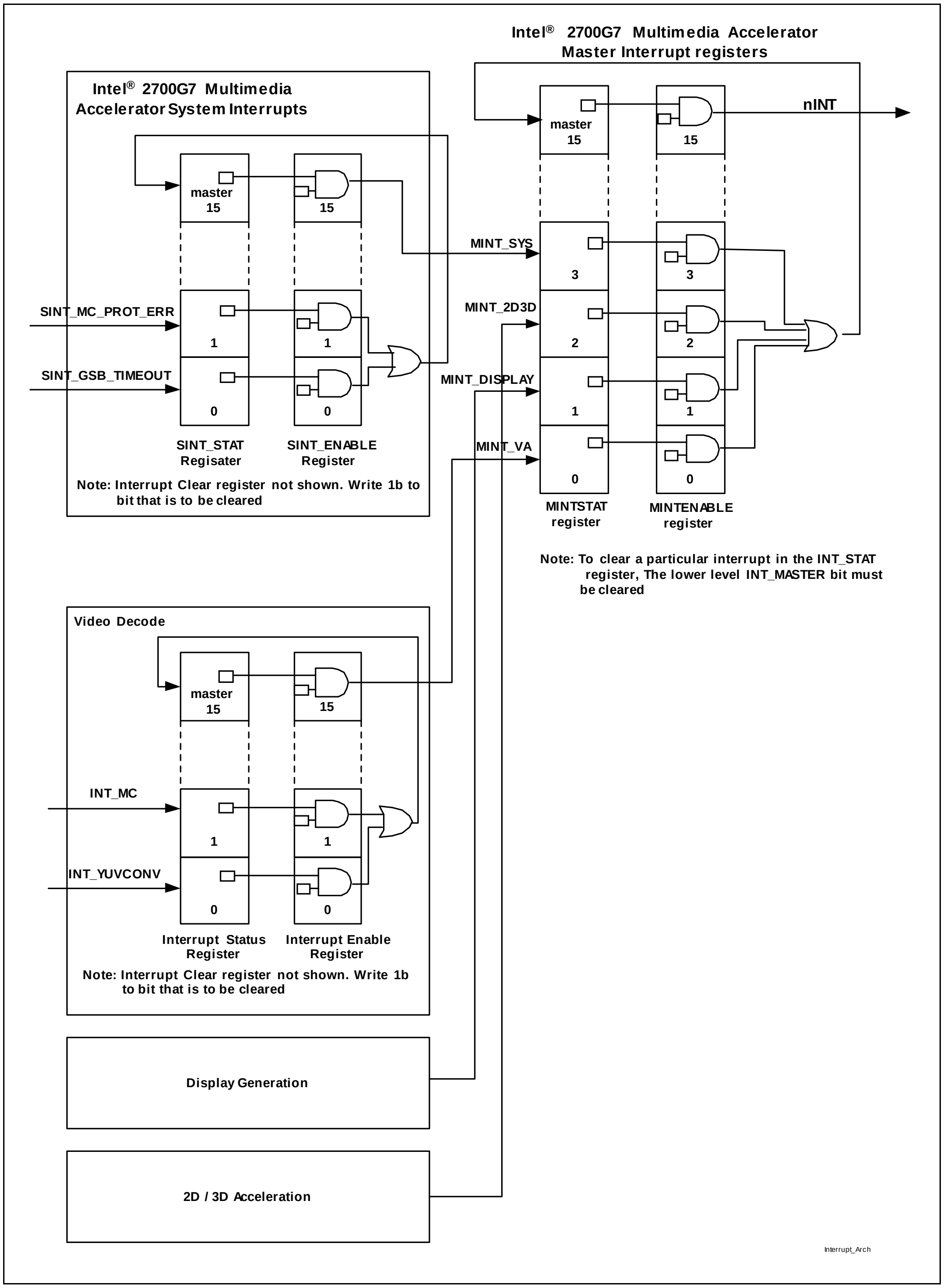
4.4 Interrupt Control Registers

The 2700G7 Multimedia Accelerator provides a single interrupt output. There are a number of interrupt sources within the 2700G7 Multimedia Accelerator. The display, video decode, and 2D/3D acceleration components may all assert an interrupt. Within each of the components, there are a number of possible interrupt sources. Each component provides its own local interrupt enable, status, and clear control.

The 2700G7 Multimedia Accelerator also has a number of system interrupts. These are controlled by the SINTENABLE, SINTSTAT, and SINTCLR registers.

The interrupts from the display, video decode, and 2D/3D acceleration components are combined with the system interrupt in the master interrupt register and applied to the nINT pin. Refer to the MINTENABLE and MINTSTAT registers. The pulse width of the nINT signal is controlled by the NINTCRTL register.

Figure 4-2. Intel® 2700G7 Multimedia Accelerator Interrupt Architecture



4.4.1 NINTPW—NINT Pulse Width Configuration Register

Address Offset:	0x03FE_0014
Default Value:	0x00000096
Access:	R/W
Size	32 bits

This register controls the pulse width of the nINT interrupt pin.

Bits	Access	Name	Description
31:8	R/W	RSVD	Reserved
7:0	R/W	INT_MINPW	**Interrupt Minimum Pulse Width.** Minimum number of SYSCLK periods required during nINT assertion and de-assertion. The default gives a minimum nINT pulse width of greater than 1 us for the maximum 2700G7 Multimedia Accelerator SYSCLK frequency.

4.4.2 MINTENABLE—Master Interrupt Enable Register

Address Offset:	0x03FE_0018
Default Value:	0x00000000
Access:	R/W
Size	32 bits

The Master Interrupt Enable register enables individual interrupts from each core to be masked by writing a 0 to the respective bit. All of the bit fields correspond exactly to those in the Master Interrupt Status register. A 0 in the MINTE_MASTER field will prohibit an external interrupt to the host system. Disabling a particular interrupt bit does not affect that interrupt's status bit. The status of an interrupt may be read at any time.

Note: There is no MINTCLR register, since these interrupts will deactivate when the interrupt is cleared by writing to the CLEAR register in the corresponding core or the SINTCLEAR register.

Bits	Access	Name	Description
31:16	R/W	RSVD	Reserved
15	R/W	MINTE_ MASTER	**Master Interrupt Enable.** This bit controls generation of interrupts to the host. If it is 1 and the MINT_MASTER bit in the interrupt status register is set, then an interrupt is generated.
14:4	R/W	RSVD	Reserved
3	R/W	MINTE_SYS	**System Interrupt Enable.** This bit enables interrupts in the SINT_STAT register to generate interrupts to the host
2	R/W	MINTE_2D3D	**2D/3D Interrupt Enable.** This bit enables interrupts from the 2D/3D acceleration core to generate interrupts to the host
1	R/W	MINTE_ DISPLAY	**Display Interrupt Enable.** This bit enables interrupts from the display core to generate interrupts to the host
0	R/W	MINTE_VA	**Video Acceleration Interrupt Enable.** This bit enables interrupts from the video decode core to generate interrupts to the host

4.4.3 MINTSTAT—Master Interrupt Status Register

Address Offset: 0x03FE_001C
Default Value: 0x00000000
Access: RO
Size 32 bits

The Master Interrupt Status register indicates the source of the top-level master interrupts. The interrupt structure is hierarchical and four sub-level interrupt controller feed into this one. When all bits of this register are cleared the interrupt to the host system will be de-activated.

Note: There is no MINT_CLEAR register, since these interrupts will deactivate when the interrupt is cleared by writing to the CLEAR register in the corresponding core or the SINT_CLEAR register.

Bits	Access	Name	Description
31:16	RO	RSVD	Reserved
15	RO	MINT_ MASTER	**Master Interrupt Status.** This bit reflects status of external nINT interrupt pin. 0b = Interrupt pin is inactive (high) 1b = Interrupt pin is active (low)
14:4	RO	RSVD	Reserved
3	RO	MINT_SYS	**Interrupt from System Interrupt Controller (SINT_* registers).** 0b = There are no system interrupts 1b = A system interrupt is active (see SINT_STAT register)
2	RO	MINT_2D3D	**Interrupt from 2D/3D Interrupt Controller.** 0b = There are no interrupts from 2D/3D accelerator portion of the 2700G7 Multimedia Accelerator 1b = A 2D/3D interrupt is active
1	RO	MINT_ DISPLAY	**Interrupt from Display Interrupt Controller.** 0b = There are no interrupts from Display stream portion of the 2700G7 Multimedia Accelerator 1b = A display interrupt is active
0	RO	MINT_VA	**Interrupt from Video Decode Interrupt Controller.** 0b = There are no interrupts from Video Decode portion of the 2700G7 Multimedia Accelerator 1b = A video decode interrupt is active

4.4.4 SINTENABLE—System Interrupt Enable Register

Address Offset:	0x03FE_0020
Default Value:	0x00000000
Access:	R/W
Size	32 bits

The System Interrupt Enable register allows individual interrupts to be masked by writing a 0 to the respective bit. All of the bit fields correspond exactly to those in the Interrupt Status register. A 0 in the SINTE_MASTER field will prohibit an interrupt from reaching the Master Interrupt status register (MINTSTAT). Disabling a particular interrupt bit does not affect that interrupt's status bit. The status of an interrupt may be read at any time.

Bits	Access	Name	Description
31:16	R/W	RSVD	Reserved
15	R/W	SINTE_ MASTER	**Master Mask.** This bit controls propagation of interrupts to the master interrupt controller. If it is 1 and the SINT_MASTER bit in the interrupt status register is set, then an interrupt will be active in the MINT_STAT register.
14:4	R/W	RSVD	Reserved
3	R/W	SINTE_GSB_ SPOVER FLOW	**GSB Slave Port Overflow Mask.** This bit masks the GSB Slave port overflow interrupt.
2	R/W	SINTE_GSB_ SPBADADD	**GSB Slave Port Bad Address Mask.** This bit masks the GSB Slave port bad address interrupt.
1	R/W	SINTE_MC_ PROT_ERR	**Memory Controller Protection Mask.** This bit masks the memory controller protection interrupt.
0	R/W	SINTE_GSB_ TIMEOUT	**Read Timeout General System Bus Mask.** This bit masks the read timeout General system bus interrupt.

4.4.5 SINTSTAT— System Interrupt Status Register

Address Offset: 0x03FE_0024
Default Value: 0x00000000
Access: R/W
Size 32 bits

The System Interrupt Status register indicates the source of the system interrupts. These interrupts feed into the master interrupt status register (MINT_STAT) only if the relevant bit in the system interrupt mask (SINT_ENABLE) register is set. When all enabled bits are cleared, the MINT_SYS bit in the MINT_STAT register will be cleared. This SINTSTAT register is writeable, allowing interrupts to be generated by software for the purposes of testing and debug.

Bits	Access	Name	Description
31:16	R/W	RSVD	Reserved
15	R/W	SINT_ MASTER	**Master Interrupt Status.** This bit reflects overall status of system interrupt controller: 0b = Interrupt is inactive 1b = Interrupt is active
14:4	R/W	RSVD	Reserved
3	R/W	SINT_GSB_ SPOVER FLOW	**GSB Slave Port Overflow Status.** This bit indicates when an overflow has occurred while trying to write to one of the core's slave ports in SRAM mode. 0b = No slave port overflow 1b = An overflow occurred while writing to a slave port in SRAM mode
2	R/W	SINT_GSB_ SPBADADD	**GSB Bad Address Status.** A bad address was received while writing to a slave port in SRAM mode. 0b = No bad addresses were received 1b = A bad address was received while writing to a slave port in SRAM mode
1	R/W	SINT_MC_ PROT_ERR	**Memory Controller Protection Error Status.** This bit becomes set if the memory controller performs an illegal access as defined by the MC_PROT_RNW, MC_MAX_ADDRESS, and MC_MIN_ADDRESS registers. 0b = No memory controller error 1b = Memory controller protection error
0	R/W	SINT_GSB_ TIMEOUT	**GSB Read Timeout.** This bit indicates when a read timeout has occurred on the general system bus. 0b = No GSB timeout 1b = General system bus recently timed-out during a read

4.4.6 SINTCLR—System Interrupt Clear Register

Address Offset: 0x03FE_0028
Default Value: 0x00000000
Access: R/W
Size 32 bits

The System Interrupt Clear register enables individual interrupts in the System Interrupt Status register to be cleared by writing 1s to the respective bits. When all unmasked bits are cleared, the MINT_SYS bit in the MINTSTAT register will be cleared. Writes of 0 have no affect. Reads return 0.

Bits	Access	Name	Description
31:4	R/W	RSVD	Reserved
3	R/W	SINTC_GSB_ SPOVER FLOW	**GSB Slave Port Overflow Interrupt Clear.** This bit clears the GSB Slave port overflow interrupt.
2	R/W	SINTC_GSB_ SPBADADD	**GSB Slave Port Bad Address Interrupt Clear.** This bit clears the GSB Slave port bad address interrupt.
1	R/W	SINTC_MC_ PROT_ERR	**Memory Controller Protection Error Clear.** This bit clears the memory controller protection error status.
0	R/W	SINTC_GSB_ TIMEOUT	**GSB Read Timeout Interrupt Clear.** This bit clears the GSB read timeout interrupt.

4.5 Clock Control Registers

The 2700G7 Multimedia Accelerator Graphics controller contains multiple clock domains with various programmable capabilities.

4.5.1 SYSCLKSRC—SYSCLK Source Control Register

Address Offset:	0x03FE_002C
Default Value:	0x00000000
Access:	R/W
Size	32 bits

This register allows the SYSCLK to be switched between the REFCLK, CORE_PLL or DISP_PLL in a glitch-free manner. The clock source will be updated immediately after writing to this register. Completion of switch over requires 32 REFCLK cycles.

Bits	Access	Name	Description
31:2	R/W	RSVD	Reserved
1:0	R/W	SCLK_SEL	**System Clock Selection.** 00b = SYSCLK is supplied from REFCLK (default) 01b = SYSCLK is supplied from DISP_PLL 10b = SYSCLK is supplied from CORE_PLL 11b = Reserved

4.5.2 PIXCLKSRC—PIXCLK Source Control Register

Address Offset:	0x03FE_0030
Default Value:	0x00000000
Access:	R/W
Size	32 bits

This register allows the PIXCLK to be switched between the REFCLK and DISP_PLL in a glitch-free manner. The clock source will be updated immediately after writing to this register. Completion of switch over requires 32 REFCLK cycles.

Bits	Access	Name	Description
31:2	R/W	RSVD	Reserved
1:0	R/W	PCLK_SEL	**Pixel Clock Selection.** 00b = PIXCLK is supplied from REFCLK (default) 01b = PIXCLK is supplied from DISP_PLL 10b = Reserved 11b = Reserved

4.5.3 CLKSLEEP—Clock Disable Register

Address Offset:	0x03FE_0034
Default Value:	0x00000000
Access:	R/W
Size	32 bits

This register allows the device to be put into full power-down mode with all clocks disabled. After activating deep sleep, no general system bus accesses are allowed. A hard reset is required to wake up the device.

Bits	Access	Name	Description
31:1	R/W	RSVD	Reserved
0	R/W	DP_SLP	**Deep Sleep.** 0b = Normal mode (default) 1b = Activate deep sleep mode

4.5.4 COREPLL— CORE PLL Configuration Register

Address Offset:	0x03FE_0038
Default Value:	0x00000FC4
Access:	R/W
Size	32 bits

This register configures the core PLL. This is the PLL that provides the clock source for graphics processing components in the 2700G7 Multimedia Accelerator, including the 2D, 3D, video decode, scaling, local memory, GSB interface, and on-die memory.

The PLL output frequency is defined as (Frefclk*M)/(N*2^P).
Default Frequency is 25.1875 MHz. Writes to this register take immediate effect.

Bits	Access	Name	Description
31:13	R/W	RSVD	Reserved
12:7	R/W	CORE_PLL_M	**CORE_PLL M Divider Configuration.** 1 to 63 (Default 31)
6:4	R/W	CORE_PLL_N	**CORE_PLL N Divider Configuration.** 1 to 7 (Default 4)
3:1	R/W	CORE_PLL_P	**CORE_PLL P Divider Configuration.** 0 to 7 (Default 2)
0	R/W	CORE_PLL_EN	**CORE_PLL Enable/Power Down.** 0b = Standby/Power down mode - output clock is REFCLK (default) 1b = Normal operation

4.5.5 DISPPLL—Display PLL Configuration Register

Address Offset:	0x03FE_003C
Default Value:	0x00000FC4
Access:	R/W
Size	32 bits

This register configures the display PLL. This is the PLL that controls the rate of the pixel clock (MPXLCLK) output the LCD interfaces.

The PLL output frequency is defined as (Frefclk*M)/(N*2^P). Default Frequency is 25.1875MHz. Writes to this register take immediate effect.

Bits	Access	Name	Description
31:13	R/W	RSVD	Reserved
12:7	R/W	DISP_PLL_M	**DISP_PLL M Divider Configuration.** Range = 1 to 63 (Default = 31)
6:4	R/W	DISP_PLL_N	**DISP_PLL N Divider Configuration.** Range = 1 to 7 (Default = 4)
3:1	R/W	DISP_PLL_P	**DISP_PLL P Divider Configuration.** Range = 0 to 7 (Default = 2)
0	R/W	DISP_PLL_EN	**DISP_PLL Enable/Power Down.** 0b = Standby/Power down mode - output clock is REFCLK (default) 1b = Normal operation

4.5.6 PLLSTAT—PLL Status Register

Address Offset:	0x03FE_0040
Default Value:	0x00000000
Access:	R/W, RO
Size	32 bits

The PLL Status register indicates the lock status of each PLL. Both the current status and history for each PLL is available. Writing a zero to the CORE_PLL_LOST_L or DISP_PLL_LOST_L status bits will clear them.

Bits	Access	Name	Description
31:4	R/W	RSVD	Reserved
3	R/W	CORE_PLL_LOST_L	**CORE_PLL Lost Lock.** This bit indicates if the CORE_PLL lost lock previously. 0b = CORE_PLL has never lost lock 1b = CORE_PLL has previously lost lock
2	RO	CORE_PLL_LSTS	**CORE_PLL Lock Status.** This bit is the CORE_PLL lock status. 0b = CORE_PLL is not locked 1b = CORE_PLL is locked
1	R/W	DISP_PLL_LOST_L	**DISP_PLL Lost Lock.** This bit indicates if the DISP_PLL lost lock previously. 0b = DISP_PLL has never lost lock 1b = DISP_PLL has previously lost lock
0	RO	DISP_PLL_LSTS	**DISP_PLL Lock Status.** This bit is the DISP_PLL lock status. 0b = DISP_PLL is not locked 1b = DISP_PLL is locked

4.5.7 VOVRCLK—Video and Scale Clock Control Register

Address Offset:	0x03FE_0044
Default Value:	0x00000000
Access:	R/W
Size	32 bits

Video overlay clock gating is controlled by this register. Writing a 1 enables the clock, while a 0 disables the clock. Changes take immediate effect.

Bits	Access	Name	Description
31:1	R/W	RSVD	Reserved
0	R/W	VCLK_EN	**Video Overlay Clock Enable.** 0b = Disabled (default) 1b = Enabled

4.5.8 PIXCLK— LCD Pixel Clock Control Register

Address Offset:	0x03FE_0048
Default Value:	0x00000000
Access:	R/W
Size	32 bits

Pixel clock gating is controlled by this register.

Bits	Access	Name	Description
31:1	R/W	RSVD	Reserved
0	R/W	PCLK_EN	**Pixel Overlay Clock Enable.** 0b = Disabled (default) 1b = Enabled

4.5.9 MEMCLK—Memory Clock Control Register

Address Offset:	0x03FE_004C
Default Value:	0x00000000
Access:	R/W
Size	32 bits

MEMCLK clock gating is controlled by this register.

Bits	Access	Name	Description
31:1	R/W	RSVD	Reserved
0	R/W	MCLK_EN	**Memory Clock Enable.** 0b = Disabled (default) 1b = Enabled

4.5.10 SDCLK—SDRAM Clock Control Register

Address Offset: 0x03FE_0058
Default Value: 0x00000000
Access: R/W
Size 32 bits

SDRAM clock gating is controlled by this register.

Bits	Access	Name	Description
31:1	R/W	RSVD	Reserved
0	R/W	SDCLK_EN	**SDRAM Clock Enable.** 0b = Disable (default) 1b = Enable

4.5.11 PIXCLKDIV—PIXCLK Divisor Register

Address Offset: 0x03FE_005C
Default Value: 0x00000001
Access: R/W
Size 32 bits

There is a post divider for the PIXCLK which is configured using the PIX_PD field.

Bits	Access	Name	Description
31:9	R/W	RSVD	Reserved
8:0	R/W	PIX_PD	**PIXCLK Post Divider Configuration.** Range = 1 to 511 (Default 1) Note: a value of 0 is mapped to 1.

4.6 LCD Port Control Registers

The 2700G7 Multimedia Accelerator contains one LCD input port and two LCD output ports that have configurable interfaces. The input port (LCD_IN) may be configured to pass thru the 2700G7 Multimedia Accelerator to one of the LCD output ports. Refer to Section 3.6 for more information about Dual-Display capabilities.

4.6.1 LCD_CONFIG—LCD Configuration Register

Address Offset:	0x03FE_0060
Default Value:	0x00000001
Access:	R/W
Size	32 bits

The LCD switch and drive strength is configured using this register. This register also allows the LCD outputs to be tri-stated. In addition, the clock polarity of the incoming data can be configured. Incoming data to the LCD switch is registered on either the rising or falling edge of the pixel clock, configured via the X_POL register bits.

Bits	Access	Name	Description
31	R/W	RSVD	Reserved
30:28	R/W	LCDIN_FMT	**LCD Input Format.** This field defines the format of the RGB data presented to the LCD_IN interface. 000b = 5:5:5 001b = 5:5:6 010b = 5:6:5 011b = 6:5:5 100b = 6:6:5 101b = 6:6:6 110b = Reserved 111b = Reserved
27	R/W	LCD1DEN_POL	**LCD1 DEN Source Clock Polarity.** This input is registered on either rising or falling edge of the active clock (MPXLCLK/LCD_IN_PCLK). 0 = rising edge of active clock 1 = falling edge of active clock
26	R/W	LCD1FCLK_POL	**LCD1 FCLK Source Clock Polarity.** This input is registered on either rising or falling edge of the active clock (MPXLCLK/LCD_IN_PCLK). 0 = rising edge of active clock 1 = falling edge of active clock
25	R/W	LCD1LCLK_POL	**LCD1 LCLK Source Clock Polarity.** This input is registered on either rising or falling edge of the active clock (MPXLCLK/LCD_IN_PCLK). 0 = rising edge of active clock 1 = falling edge of active clock

Bits	Access	Name	Description
24	R/W	LCD1D_POL	**LCD1 Data Source Clock Polarity.** This input is registered on either rising or falling edge of the active clock (MPXLCLK/LCD_IN_PCLK). 0 = rising edge of active clock 1 = falling edge of active clock
23	R/W	LCD2DEN_POL	**LCD2 DEN Source Clock Polarity.** This input is registered on either rising or falling edge of the active clock (MPXLCLK/LCD_IN_PCLK). 0 = rising edge of active clock 1 = falling edge of active clock
22	R/W	LCD2FCLK_POL	**LCD2 FCLK Source Clock Polarity.** Input is registered on either rising or falling edge of the active clock (MPXLCLK/LCD_IN_PCLK). 0 = rising edge of active clock 1 = falling edge of active clock
21	R/W	LCD2LCLK_POL	**LCD2 LCLK Source Clock Polarity.** Input is registered on either rising or falling edge of the active clock (MPXLCLK/LCD_IN_PCLK). 0 = rising edge of active clock 1 = falling edge of active clock
20	R/W	LCD2D_POL	**LCD2 DATA Source Clock Polarity.** Input is registered on either rising or falling edge of the active clock (MPXLCLK/LCD_IN_PCLK). 0 = rising edge of active clock 1 = falling edge of active clock
19	R/W	LCD1_TS	**LCD1 Tri-state Outputs.** 0b = Outputs are tri-stated (default) 1b = Outputs are actively driven
18	R/W	LCD1D_DS	**LCD1D Drive Strength.** This bit is the drive strength for Primary LCD interface data (LCD1FCLK, LCD1LCLK, LCD1DEN, LCD1D). 0b = Drive strength is 3 mA at all IO voltages (default) 1b = Drive strength is 6 mA at 1.8 V or 10 mA at 2.5/3.3 V
17	R/W	LCD1C_DS	**LCD1C Drive Strength.** This bit is the drive strength for Primary LCD interface clock (LCD1PCLK). 0b = Drive strength is 3 mA at all IO voltages (default) 1b = Drive strength is 6 mA at 1.8 V or 10 mA at 2.5/3.3 V
16	R/W	LCD1_IS_LCD_IN	0b = LCD1 is the 2700G7 Multimedia Accelerator-generated display. (default) 1b = LCD1 is LCD_IN
15:4	R/W	RSVD	Reserved
3	R/W	LCD2_TS	**LCD2 Tri-state Outputs**. 0b = Outputs are tri-stated (default) 1b = Outputs are actively driven

Bits	Access	Name	Description
2	R/W	LCD2D_DS	**LCD2D_DS Drive Strength**. This bit is the drive strength for Secondary LCD interface data (LCD2FCLK, LCD2LCLK, LCD2DEN, LCD2D). 0b = Drive strength is 3 mA at all IO voltages (default) 1b = Drive strength is 6 mA at 1.8 V or 10 mA at 2.5/3.3 V
1	R/W	LCD2C_DS	**LCD2C_DS Drive Strength.** This bit is the drive strength for Secondary LCD interface clock (LCD2PCLK). 0b = Drive strength is 3 mA at all IO voltages (default) 1b = Drive strength is 6 mA at 1.8 V or 10 mA at 2.5/3.3 V
0	R/W	LCD2_IS_LCD_IN	0b = LCD2 is the 2700G7 Multimedia Accelerator-generated display. 1b = LCD2 is LCD_IN. (default).

4.7 On-Die Frame Buffer Control Registers

The 2700G7 Multimedia Accelerator components have on-die frame buffers. The configuration of the on-die frame buffer is controlled by the ODFBPWR register, while the current power state of the buffer is available in the ODFBSTAT register. Refer to Section 3.5 for more information about the on-die frame buffer.

4.7.1 ODFBPWR—On-Die Frame Buffer Power Control Register

Address Offset: 0x03FE_0064
Default Value: 0x00000007
Access: R/W
Size 32 bits

The power mode of the on-die frame buffer is controlled using this register. Writing to this register takes immediate effect. The MEMCLK frequency provided must be calculated and the ODFB_SLOW field set appropriately when putting the on-die frame buffer into active mode.

Bits	Access	Name	Description
31:3	R/W	RSVD	Reserved
2	R/W	FBP_SLOW	**System Clock Frequency.** 0b = High frequency 66 – 133 MHz 1b = Low frequency 13 – 66 MHz (default)
1:0	R/W	FBP_MODE	**Frame Buffer Power Mode.** 00b = Active at all times 01b = Active low power. Automatically placed in retentive standby mode when inactive. 10b = Forced Sleep - retentive standby mode 11b = Shutdown - non-retentive shutdown mode (default)

4.7.2 ODFBSTAT— On-Die Frame Buffer Power State Status Register

Address Offset: 0x03FE_0068
Default Value: 0x00000001
Access: RO
Size 32 bits

The current power mode of the on-die frame buffer is reflected in this register.

Bits	Access	Name	Description
31:3	RO	RSVD	Reserved
2	RO	FBP_ACT	**Frame Buffer Power State Active.** 0b = Active 1b = Not active
1	RO	FBP_SLP	**Frame Buffer Power State Sleep Mode** (retentive standby). 0b = Active 1b = Not active
0	RO	FBP_SDN	**Frame Buffer Power State Shutdown Mode** (non-retentive standby) 0b = Active 1b = Not active

4.8 GPIO Control Registers

4.8.1 GPIOCFG—GPIO Configuration Register

Address Offset:	0x03FE_006C
Default Value:	0x00000000
Access:	R/W
Size	32 bits

The GPIO configuration register controls direction and drive strength when configured as outputs. Output drivers of GPIOs are tri-state when configured as an input.

Bits	Access	Name	Description
31:4	R/W	RSVD	Reserved
3	R/W	GPIO1_DS	**GPIO1 Drive Strength.** 0b = 3 mA at all I/O voltages (default) 1b = 6 mA at 1.8 V or 10 mA at 2.5/3.3 V
2	R/W	GPIO0_DS	**GPIO0 Drive Strength.** 0b = 3 mA at all I/O voltages (default) 1b = 6 mA at 1.8 V or 10 mA at 2.5/3.3 V
1	R/W	GPIO1_DIR	**GPIO1 Pin Direction.** 0b = Input (default) 1b = Output
0	R/W	GPIO0_DIR	**GPIO0 Pin Direction.** 0b = Input (default) 1b = Output

4.8.2 GPIOHI—GPIO High Output Register

Address Offset: 0x03FE_0070
Default Value: 0x00000000
Access: WO
Size 32 bits

This GPIOHI register allows the state of pins configured as outputs to be set high.

Bits	Access	Name	Description
31:2	WO	RSVD	Reserved
1	WO	GPIO1_PH	**GPIO 1 Pin High.** 0b = GPIO1 pin level is unaffected (default). 1b = If configured as an output, GPIO1 pin level is set high.
0	WO	GPIO0_PH	**GPIO 0 Pin High.** 0b = GPIO0 pin level is unaffected (default). 1b = If configured as an output, GPIO0 pin level is set high.

4.8.3 GPIOLO—GPIO Low Output Register

Address Offset: 0x03FE_0074
Default Value: 0x00000000
Access: WO
Size 32 bits

This GPIOLO register allows the state of pins configured as outputs to be set low.

Bits	Access	Name	Description
31:2	WO	RSVD	Reserved
1	WO	GPIO1_PL	**GPIO 1 Pin Low.** 0b = GPIO1 pin level is unaffected (default) 1b = If configured as an output, GPIO1 pin level is set low
0	WO	GPIO0_PL	**GPIO 0 Pin Low.** 0b = GPIO0 pin level is unaffected (default) 1b = If configured as an output, GPIO0 pin level is set low

4.8.4 GPIOSTAT—GPIO Input State Register

Address Offset:	0x03FE_0078
Default Value:	0x00000000
Access:	RO
Size	32 bits

The GPIO Level register indicates the current value of each GPIO pin.

Bits	Access	Name	Description
31:2	RO	RSVD	Reserved
1	RO	GPIO1_PS	**GPIO1 Pin State.** 0b = Low 1b = High
0	RO	GPIO0_PS	**GPIO0 Pin State.** 0b = Low 1b = High

4.9 Pulse Width Modulator Control Registers

The 2700G7 Multimedia Accelerator contains two controllable pulse modulators (PWMs) that can be used to control LCD backlights. Refer to Section 3.7.2 for more information on PWMs.

4.9.1 PWMRST—PWM Soft Reset Control Register

Address Offset:	0x03FE_0200
Default Value:	0x00000000
Access:	R/W
Size	32 bits

Write a 1 to reset the PWM controller module and write a 0 to bring it out of reset. A hard system reset also resets this block listed below and overrides the values within this register.

Bits	Access	Name	Description
31:1	R/W	RSVD	Reserved
0	R/W	PWM_RST	**PWR Controller Reset State.** 0b = Inactive (default) 1b = Active

4.9.2 PWMCFG— PWM Configuration Register

Address Offset: 0x03FE_0204
Default Value: 0x00000000
Access: R/W
Size 32 bits

The drive strength of the PWM outputs can be controlled from this register. This register also allows the outputs to be tri-stated.

Bits	Access	Name	Description
31:4	R/W	RSVD	Reserved
3	R/W	PWM_DS1	**PWM1 Output Drive Strength.** 0b = 3 mA at all I/O voltages (default) 1b = 6 mA at 1.8 V or 10 mA at 2.5/3.3 V
2	R/W	PWM_DS0	**PWM0 Output Drive Strength.** 0b = 3 mA at all I/O voltages (default) 1b = 6 mA at 1.8 V or 10 mA at 2.5/3.3 V
1	R/W	PWM_TS1	**Tri-state local PWM1.** 0b = Outputs are tri-stated (default) 1b = Outputs are actively driven
0	R/W	PWM_TS0	**Tri-state local PWM0.** 0b = Outputs are tri-stated (default) 1b = Outputs are actively driven

4.9.3 PWM0DIV— PWM 0 Pre-Scale Divisor Register

Address Offset: 0x03FE_0210
Default Value: 0x00000000
Access: R/W
Size 32 bits

The PWM0DIV register contains a 6-bit pre-scale counter load field. This field determines the relationship between REFCLK and PSCLK_PWM0. PSCLK_PWM0 is REFCLK divided by between 1 and 64.

Note: The value of the divisor is one greater than the value programmed into the PWM0_PSD field.

Bits	Access	Name	Description
31:6	R/W	RSVD	Reserved
5:0	R/W	PWM0_PSD	**PWM0 Pre-scale Divisor.** This field determines the frequency of the PWM pre-scaled clock. 0x0 = divide by 1 … 0x3F = divide by 64 PSCLK_PWM0 = REFCLK / (PWM0_PRESCALE + 1).

4.9.4 PWM0DUTY— PWM 0 Duty Cycle Control Register

Address Offset: 0x03FE_0214
Default Value: 0x00000000
Access: R/W
Size 32 bits

The PWM0_DUTY register contains a 10-bit duty-cycle load field. This field allows the duty-cycle to be varied, where the high time can be from 1 to 1023 scaled clock cycles. If this field is cleared to zero, the channel is turned off and PWM0 remains in a low state.

Bits	Access	Name	Description
31:10	R/W	RSVD	Reserved
9:0	R/W	PWM0_DCYC	**PWM0 Duty Cycle.** This field provides the duty cycle of PWM0. (i.e., the number of PSCLK_PWM cycles PWM0 is asserted within one cycle of PWM0). 0x0 = Off and tied low 0x1 = High time is 1 PSCLK_PWM0 cycle … 0x3FF = High time is 1023 PSCLK_PWM0 cycles

4.9.5 PWM0PER— PWM 0 Period Control Register

Address Offset:	0x03FE_0218
Default Value:	0x00000004
Access:	R/W
Size	32 bits

The PWM0PER register contains a 10-bit field called PWM0_PC. This field determines the period of the PWM0 waveform referenced to PSCLK_PWM0. For any non-zero value written to the PWM0_PC field, the output frequency of PWM0 is the frequency of PSCLK_PWM0 divided by the value of (PWM_PC + 1).

Note: If PWM0_PC = 0x0, the PWM0 clock (PWM0) is set high and does not toggle.

Note: The value of the PWM0_PC field must never be less than the PWM0_DCYCLE field for normal operation; otherwise, the output will remain constantly high.

Bits	Access	Name	Description
31:10	R/W	RSVD	Reserved
9:0	R/W	PWM0_PC	**PWM0 Period Control.** (PWM0_PC+1) is the number of PSCLK_PWM0 cycles that comprise one PWM0 cycle. 0x0 = Off and tied high 0x1 = Period is 2 PSCLK_PWM0 cycles … 0x3FF = Period is 1024 PSCLK_PWM0 cycles

4.9.6 PWM1DIV— PWM 1 Pre-Scale Divisor Register

Address Offset:	0x03FE_0220
Default Value:	0x00000000
Access:	R/W
Size	32 bits

The PWM1DIV register contains the 6-bit pre-scale counter load field. This field determines the relationship between REFCLK and PSCLK_PWM1. PSCLK_PWM1 is REFCLK divided by between 1 and 64.

Note: The value of the divisor is one greater than the value programmed into the PWM1_PSD field.

Bits	Access	Name	Description
31:6	R/W	RSVD	Reserved
5:0	R/W	PWM1_PSD	**PWM1 Pre-scale Divisor.** This field determines the frequency of the PWM pre-scaled clock. 0x0 = divide by 1 … 0x3F = divide by 64 PSCLK_PWM1 = REFCLK / (PWM1_PRESCALE + 1).

4.9.7 PWM1DUTY—PWM 1 Duty Cycle Control Register

Address Offset: 0x03FE_0224
Default Value: 0x00000000
Access: R/W
Size 32 bits

The PWM1DUTY register contains the 10-bit duty-cycle load field. This field allows the duty-cycle to be varied, where the high time can be from 1 to 1023 scaled clock cycles. If this field is cleared to zero, the channel is turned off and PWM1 remains in a low state.

Bits	Access	Name	Description
31:10	R/W	RSVD	Reserved
9:0	R/W	PWM1_DCYC	**PWM0 Duty Cycle.** This field provides the duty cycle of PWM1. (i.e., the number of PSCLK_PWM cycles PWM0 is asserted within one cycle of PWM1). 0x0 = Off and tied low 0x1 = High time is 1 PSCLK_PWM1 cycle … 0x3FF = High time is 1023 PSCLK_PWM1 cycles

4.9.8 PWM1PER— PWM 1 Period Control Register

Address Offset: 0x03FE_0228
Default Value: 0x00000004
Access: R/W
Size 32 bits

The PWM1PER register contains a 10-bit field called PWM1_PC. This field determines the period of the PWM1 waveform referenced to PSCLK_PWM1. For any non-zero value written to the PWM1_PC field, the output frequency of PWM1 is the frequency of PSCLK_PWM1 divided by the value of (PWM1_PC + 1).

Note: If PWM1_PC = 0x0, the PWM1 clock (PWM1) is set high and does not toggle.

Note: The value of the PWM1_PC field must never be less than the PWM1_DCYCLE field; otherwise, the output will remain constantly high.

Bits	Access	Name	Description
31:10	R/W	RSVD	Reserved
9:0	R/W	PWM1_PC	**PWM1 Period Control.** (PWM1_PC+1) is the number of PSCLK_PWM1 cycles that comprise one PWM1 cycle. 0x0 = Off and tied high 0x1 = Period is 2 PSCLK_PWM1 cycles … 0x3FF = Period is 1024 PSCLK_PWM1 cycles

4.10 Device Identification Registers

The 2700G7 Multimedia Accelerator can be identified in software by reading the ID register.

4.10.1 ID— Identification Register

Address Offset:	0x03FE_0FF0
Default Value:	0x01727189
Access:	RO
Size	32 bits

Bits	Access	Name	Description
31:24	RO	RID	**Revision Identification.** This field contains product stepping information. 0x01 = A1' stepping
23:8	RO	DID	**Device Identification.** This field contains a 16-bit value assigned to the 2700G7 Multimedia Accelerator graphics core. 0x7271 = Device ID
7:0	RO	VID	**Vendor Identification.** This field contains the 8-bit Intel vendor ID. 0x89 = Vendor ID

4.11 Local Memory (SDRAM) Interface Registers

The 2700G7 Multimedia Accelerator contains 16 MB of SDRAM stacked within the package that can be used as graphics memory. Throughout this section, the term "Local Memory" refers to this stacked memory within the 2700G7 Multimedia Accelerator package.

Note: Since the stacked SDRAM package within the 2700G7 Multimedia Accelerator cannot be changed or replaced, the values that are programmed by Intel's drivers to these registers should not be changed. Contact your Intel representative for the latest drivers for the 2700G7 Multimedia Accelerator.

4.11.1 LMRST—Local Memory (SDRAM) Reset

Address Offset:	0x03FE_1000
Default Value:	0x00000000
Access:	R/W
Size	32 bits

This is the memory controller soft reset register. Write a 1 to reset the memory controller module and write a 0 to bring it out of reset. A hard system reset also resets this block and overrides the values within this register.

Bits	Access	Name	Description
31:1	R/W	RSVD	Reserved
0	R/W	MC_RST	**Memory Controller Reset.** 0b = Inactive (default) 1b = Active

4.11.2 LMCFG—Local Memory (SDRAM) Configuration Register

Address Offset:	0x03FE_1004
Default Value:	0x00000000
Access:	R/W
Size	32 bits

The drive strength of the memory controller outputs can be controlled from this register via the *_DS fields. This register also allows the outputs to be tri-stated via the *_TS fields.

Bits	Access	Name	Description
31:6	R/W	RSVD	Reserved
5	R/W	LMC_DS	**Local Memory Clock Drive Strength.** This bit selects the drive strength of the local (SDRAM) memory clock output. 0b =3 mA at all I/O voltages (default) 1b = 6 mA at 1.8 V or 10 mA at 2.5/3.3 V
4	R/W	LMD_DS	**Local Memory Data Drive Strength.** This bit selects the drive strength of the local (SDRAM) memory data outputs. 0b = 3 mA at all I/O voltages (default) 1b = 6 mA at 1.8 V or 10 mA at 2.5/3.3 V
3	R/W	LMA_DS	**Local Memory Address/Control Drive Strength.** This bit selects the drive strength of the local (SDRAM) memory control outputs (CKE, NCS, NCAS, NRAS, NWE, NDQM, BA, A). 0b = 3 mA at all I/O voltages (default) 1b = 6 mA at 1.8 V or 10 mA at 2.5/3.3 V
2	R/W	LMC_TS	**Local Memory Clock Tri-state Control.** This bit tri-states the local (SDRAM) memory clock output. 0b = Outputs are tri-stated (default) 1b = Outputs are actively driven
1	R/W	LMD_TS	**Local Memory Data Tri-state Control.** This bit tri-states local (SDRAM) memory data outputs. 0b = Outputs are tri-stated (default) 1b = Outputs are actively driven
0	R/W	LMA_TS	**Local Memory Address/Control Tri-state Control.** This bit tri-states local (SDRAM) memory control outputs (CKE, NCS, NCAS, NRAS, NWE, NDQM, BA, A). 0b = Outputs are tri-stated (default) 1b = Outputs are actively driven

4.11.3 LMPWR—Local Memory (SDRAM) Power Control Register

Address Offset:	0x03FE_1008
Default Value:	0x00000000
Access:	R/W
Size	32 bits

This register controls the state of the memory devices. The controller must be in Active mode when any read or write accesses are required. In Self Refresh mode no R/W accesses are allowed, but the contents of the SDRAM are maintained. In Deep Power Down mode maximum power saving is achieved by shutting off the power to the entire memory array power island of the external SDRAM device. The data contents of the SDRAM will not be retained once Deep Power Down mode is executed. The LMPWRSTAT register indicates when the desired state has been achieved.

Bits	Access	Name	Description
31:2	R/W	RSVD	Reserved
1:0	R/W	MC_PWR_CNT	**Memory Controller Powerdown Control.** 00b = Active (default) 01b = Self Refresh Mode 10b = Reserved 11b = Deep Power Down

4.11.4 LMPWRSTAT—Local Memory (SDRAM) Power Status Register

Address Offset:	0x03FE_100C
Default Value:	0x00000000
Access:	RO
Size	32 bits

This register shows that the indicated state has been achieved by the memory devices.

Bits	Access	Name	Description
31:2	RO	RSVD	Reserved
1:0	RO	MC_PWR_STA	**Memory Controller Powerdown Status.** 00b = Active 01b = Self Refresh Mode 10b = Reserved 11b = Deep Power Down

4.11.5 LMCEMR—Local Memory (SDRAM) EMR Control Register

Address Offset:	0x03FE_1010
Default Value:	0x00000000
Access:	R/W
Size	32 bits

This register programs the Extended Mode Register (EMR) in the external SDRAM devices. The EMR controls the Driver Strength (DS), Temperature Compensation Self Refresh (TCSR) control, and Partial Array Self Refresh (PASR). Support for Drive Strength control can vary from one SDRAM vendor to another. Non-default settings of PASR can result in lost data in the banks that are not refreshed.

Bits	Access	Name	Description
31:8	R/W	RSVD	Reserved
7	R/W	MC_EMR_EN	**Memory Extended Mode Enable.** This bit enables use of the Extended Mode register. 0b = EMR programming disabled (default) 1b = EMR programming enabled
6:5	R/W	MC_ EMR_DS	**Memory Drive Strength Control.** This field controls the DS bits 6:5 of the EMR. Possible values for Driver Strength are: 00b = Full Strength (default) 01b = Half Strength 10b = Quarter Strength (optional) 11b = Reserved
4:3	R/W	MC_EMR_TEMP	**Memory Temperature Refresh Control.** This field controls the TCSR bits (4:3) of the EMR. The register should be set to the highest case temperature expected. Possible values are: 00b = 70 °C (default) 01b = 45 °C 10b = 15 °C 11b = 85 °C
2:0	R/W	MC_EMR_PREF	**Memory Array Partial Refresh Control.** This field controls the PASR bits (2:0) of the EMR. Possible values for self refresh coverage are: 000b = Four banks (default) 001b = Two banks (lowest 1/2 of memory) 010b = One bank (lowest 1/4 of memory) 011b = Reserved 100b = Reserved 101b = Half bank (lowest 1/8th of memory) 110b = Quarter bank (lowest 1/16th of memory) 111b = Reserved

4.11.6 LMTYPE—Local Memory (SDRAM) Type Register

Address Offset: 0x03FE_1014
Default Value: 0x00000EC9
Access: R/W
Size 32 bits

Bits	Access	Name	Description
31:13	R/W	RSVD	Reserved
12:10	R/W	MC_CASLAT	**Memory CAS Latency.** This field defines the CAS latency of the memory devices. The value must be set according to the specification of the memory devices being used. 000b = Reserved 001b = 1 010b = 2 011b = 3 (default) 100b = Reserved 101b = Reserved 110b = Reserved 111b = Reserved
9:8	R/W	MC_BKSZ	**Memory Bank Size.** This field controls the number of bank address bits on the memory device. Supported values are: 01b = 1 bank address bit (2 banks) 10b = 2 bank address bits (4 banks) (default)
7:4	R/W	MC_ROWSZ	**Memory Row Size.** This field controls the row width of the memory device. Supported values are: 1011b = 11 rows 1100b = 12 rows (default) 1101b = 13 rows
3:0	R/W	MC_COLSZ	**Memory Row Size.** This field controls the column width of the memory device. Supported values are: 0111b = 7 columns 1000b = 8 columns 1001b = 9 columns (default) 1010b = 10 columns 1011b = 11 columns 1100b = 12 columns

4.11.7 LMTIM—Local Memory (SDRAM) Timing Register

Address Offset: 0x03FE_1018
Default Value: 0x00052272
Access: R/W
Size 32 bits

The t_{RAS} value is the Activate to Precharge time of the memory device. This value should be calculated directly from the memory vendor's datasheet. For example, at 150 MHz (a period of 6.67 ns) a t_{RAS} of 10 ns is between 1 and 2 clock cycle times. A value of 2 would, therefore, be inserted in this register.

The t_{RP} value is the Precharge command period of the memory device. This value should be calculated directly from the memory vendor's datasheet. For example, at 150 MHz (a period of 6.67 ns) a t_{RP} of 10 ns is between 1 and 2 clock cycle times. A value of 2 would, therefore, be inserted in this register.

The t_{RCD} value is the Activate to Read time of the memory device. This value should be calculated directly from the memory vendor's datasheet. For example, at 150 MHz (a period of 6.67 ns) a t_{RCD} of 10 ns is between 1 and 2 clock cycle times. A value of 2 would, therefore, be inserted in this register.

The t_{RC} value is the minimum Active to Active command period of the memory device. This value should be calculated directly from the memory vendor's datasheet. For example, at 150 MHz (a period of 6.67 ns) a t_{RC} of 75 ns is between 11 and 12 clock cycle times. A value of 12 would, therefore, be inserted in this register.

The t_{DPL} value is the Data-in to Precharge command period of the memory device. This value should be calculated directly from the memory vendor's datasheet (sometimes it is referred to as t_{WR} or t_{RDL}). For example, at 150 MHz (a period of 6.67 ns) a t_{DPL} of 10 ns is between 1 and 2 clock cycle times. A value of 2 would, therefore, be inserted in this register.

Note: The following restriction must be met. MC_TRP + MC_TRAS ≥ MC_TRC.

Bits	Access	Name	Description
31:20	R/W	RSVD	Reserved
19:16	R/W	MC_TRAS	**Memory Controller Activate to Precharge Delay (t_{RAS}).** This field is the minimum t_{RAS} time in clock cycles.
15:12	R/W	MC_TRP	**Memory Controller Precharge Command Period (t_{RP}).** This field selects the minimum t_{RP} time in clock cycles.
11:8	R/W	MC_TRCD	**Memory Controller Activate to Read Time (t_{RCD}).** This field selects the minimum t_{RCD} (Activate to R/W) time in clock cycles.
7:4	R/W	MC_TRC	**Memory Controller Min Active to Active Command (t_{RC}).** This field selects the minimum t_{RC} (Refresh to Activate) time in clock cycles.
3:0	R/W	MC_TDPL	**Memory Controller Data-in to Precharge (t_{DPL}).** This field selects the minimum t_{DPL} (Last data-in to Precharge) time in clock cycles.

4.11.8 LMREFRESH—Local Memory (SDRAM) t_{REF} Control Register

Address Offset: 0x03FE_101C
Default Value: 0x00000610
Access: R/W
Size 32 bits

This register contains the minimum t_{REF} of the memory devices attached to the system. The t_{REF} value is the average periodic refresh interval of the memory device. This value should be calculated directly from the memory vendor's datasheet. If there are 4096 rows in a device and these rows must be refreshed in 32 ms, this value would be $(32^{10-3}/4096)/(6.67^{10-9})$=1171 clock cycles.

Bits	Access	Name	Description
31:2	R/W	RSVD	Reserved
1:0	R/W	MC_TREF	**Memory Controller Periodic Refresh Time.** This field provides the minimum t_{REF} time in clock cycles. (default = 1552 clocks)

4.11.9 LMPROTMIN—Local Memory (SDRAM) Protection Minimum Address Register

Address Offset: 0x03FE_1020
Default Value: 0x00000000
Access: R/W
Size 32 bits

If an area of memory needs to be protected against reads/writes, this register is programmed with the lowest address to be accessed. The SINT_MC_PROT_ERR interrupt (see SINT_STAT register) is asserted if an access occurs outside the window defined by the LMPROTMAX and LMPROTMIN registers. This can be used in a system that populates 32 MB of SDRAM to flag an illegal access to the unpopulated region of local memory. The default is 0x0.

Bits	Access	Name	Description
31:26	R/W	RSVD	Reserved
25:2	R/W	MC_MINADR	**Memory Controller Minimum Address.** The minimum address that the memory controller is allowed to be addressed by the memory controller. Accesses outside of this range produce a protection error.
1:0	R/W	RSVD	Reserved

4.11.10 LMPROTMAX— Local Memory (SDRAM) Protection Maximum Address Register

Address Offset:	0x03FE_1024
Default Value:	0x03FDFFFF
Access:	R/W
Size	32 bits

If an area of memory needs to be protected against reads/writes, this register is programmed with the highest address to be accessed. The SINT_MC_PROT_ERR interrupt (see SINT_STAT register) is asserted if an access occurs outside the window defined the LMPROTMAX and LMPROTMIN registers. This can be used in a system that populates 32 MB of SDRAM to flag an illegal access to the unpopulated region of local memory. The default is 0x03FDFFFF

Bits	Access	Name	Description
31:26	R/W	RSVD	Reserved
25:2	R/W	MC_MAXADR	**Memory Controller Maximum Address.** The maximum address that the memory controller is allowed to be addressed by the memory controller. Accesses outside of this range produce a protection error.
1:0	R/W	RSVD	Reserved

4.11.11 LMPROTCFG—Local Memory (SDRAM) Protection Configuration Register

Address Offset:	0x03FE_1028
Default Value:	0x00000000
Access:	R/W
Size	32 bits

The protection window is defined by the LMPROTMIN and LMPROTMAX registers.

Bits	Access	Name	Description
31:1	R/W	RSVD	Reserved
0	R/W	MC_PR_RW	**Memory Controller Protection Read and Write.** 0b = Generate a protection error if either a read or write occur outside of the protection window (default) 1b = Generate a protection error if a write occurs outside of the protection window

4.11.12 LMPROTERR—Local Memory (SDRAM) Protection Error Status Register

Address Offset: 0x03FE_102C
Default Value: 0x00000000
Access: RO
Size 32 bits

Bits	Access	Name	Description
31:1	RO	RSVD	Reserved
0	RO	MC_PR_ERR	**Memory Controller Protection Error.** This bit is set if the memory controller performs an illegal access as defined by the LMPROTCFG register

4.12 Plane Control

This section describes the 2700G7 Multimedia Accelerator's Plane Control registers. For a description of the four graphics planes in the 2700G7 Multimedia Accelerator's architecture, refer to Chapter 3.

4.12.1 Graphics Display Registers

The Graphics Display plane registers configure the RGB stream used by the 2D and 3D Graphics Accelerator Unit.

4.12.1.1 GSCTRL—Graphics Surface Control Register

Address Offset: 0x03FE_2000
Default Value: 0x00000000
Access: R/W
Size: 32 bits

Bits	Access	Name	Description
31	R/W	LUT_EN	**LUT Enable**. 0 = LUT inactive (grayscale in indexed color modes) 1 = LUT active (indexed color modes only)
30:27	R/W	GPIXFMT	**Graphics Pixel format**. 0000b = 8-bit indexed (grayscale if LUT turned off) [RGB] 0100b = 4-bit alpha + 12-bit rgb444 [ARGB] 0101b = 1-bit alpha + 15-bit rgb555 [ARGB] 0110b = 24-bit rgb888 [RGB] 0111b = 16-bit rgb565 [RGB] 1000b = 8-bit alpha + 24-bit rgb888 [ARGB]
26	R/W	GAMMA_EN	**Gamma LUT Interpolation Enable.** 0 = Gamma LUT interpolation inactive 1 = Gamma LUT interpolation active
25:22	R/W	RSVD	Reserved
21:11	R/W	GSWIDTH	**Graphics Surface Width.** Width of surface in pixels = 1 (maximum of 2047, giving maximum width of 2048) Notes: This field represents the width of the surface in memory, rather than displayed plane, the resultant width of which is affected by pixel doubling/halving.
10:0	R/W	GSHEIGHT	**Graphics Surface Height.** Height of surface in lines = 1 (maximum of 2047, giving maximum height of 2048) Notes: Must be halved if address generator 'intfield' mode is set, as represents height for field rather than frame.

4.12.1.2 GBBASE—Graphics Blending Base Register

Address Offset: 0x03FE_2020
Default Value: 0x00000000
Access: R/W
Size: 32 bits

Bits	Access	Name	Description
31:24		GLALPHA	**Global Alpha** (least significant bits reserved if less than 8-bits). all 0 = Entirety of previous surface(s) displayed all 1 = Entirety of this surface displayed
23:0		COLKEY	**Color Key for Stream.** The color key must be in the unpacked (and de-palletized) RGB data format or YUV format (note that chroma components will have been interpolated).

4.12.1.3 GDRCTRL—Graphics Decimation Replication Control Register

Address Offset: 0x03FE_2040
Default Value: 0x00000000
Access: R/W
Size: 32 bits

Bits	Access	Name	Description
31	R/W	PIXDBL	**Pixel Doubling.** 0 = No pixel doubling 1 = Pixel doubling is performed
30	R/W	PIXHLV	**Pixel Halving.** 0 = No pixel halving 1 = Pixel halving is performed (alternate pixels dropped)
29	R/W	LNDBL	**Line Doubling.** 0 = No line doubling 1 = Line doubling is performed
28	R/W	LNHLV	**Line Halving.** 0 = No line halving 1 = Line halving is performed (alternate lines dropped)
27:24	R/W	RSVD	Reserved
23:0	R/W	COLKEYM	**Color Key Mask for Stream.** Set these bits to zero to mask from color key comparison. The mask is logically AND'ed with the data to be compared against the color key. For example, to match red values in the range 8 to 11, the mask would be 0xFCFFFF, and the key would be 0x080000.

4.12.1.4 GSCADR—Graphics Stream Control Address Register

Address Offset: 0x03FE_2060
Default Value: 0x00000000
Access: R/W
Size: 32 bits

Bits	Access	Name	Description
31	R/W	STR_EN	**Stream Enable.** 0 = Stream disabled (no memory fetches or blending with other planes) 1 = Stream enabled
30	R/W	COLKEY_EN	**Color Key Enable.** 0 = Color keying disabled 1 = Color keying enabled
29	R/W	COLKEYSCR	**Color Key Source.** 0 = Current plane's color key compared against pixel from previous plane, and current plane's pixel displayed if match (else pixels are optionally alpha blended). (i.e., destination color key match selects source pixels). 1 = Current plane's color key compared against pixel from current plane, and previous plane's pixel displayed if match (else pixels are optionally alpha blended). i.e. source color key match selects destination pixels.
28:27	R/W	BLEND_M	**Blend Mode.** 00 = No alpha blending 01 = Inversion for formats with more than 1 bit of pixel alpha. Zero alpha gives transparency, full alpha gives opaque, and intermediate pixel alpha values give inversion of the lower surface pixels. 10 = Global alpha blending 11 = Pixel alpha blending
26	R/W	RSVD	Reserved
25:24	R/W	BLEND_POS	**Plane/Cursor Position.** 00 = Position 0 (bottom) – desktop graphics in architecture diagram 01 = Position 1 – video in architecture diagram 10 = Position 2 (top) – cursor in architecture diagram Note: It is vital that a unique position is programmed for each plane/cursor, even if that plane/cursor is disabled. Failure to do so results in display corruption.
23	R/W	RSVD	Reserved
22:0	R/W	GBASE_ADR	**Graphics Base Address.** Bits 26:4 of the Base Address of the Surface (Y in 4:2:0 for video, left-hand side of screen if Split Background). 128MB range on 16-byte boundaries. Takes effect immediately

4.12.1.5 GSADR—Graphics Stride Address Register

Address Offset: 0x03FE_20C0
Default Value: 0x00000000
Access: R/W
Size: 32 bits

Bits	Access	Name	Description
31:22	R/W	SRCSTRIDE	**Surface Stride.** This field provides the stride of the surface in 16 byte words – 1 (max (4095 + 1)*16 = 64 KB) Note: For planar 4:2:0 video, the stride relates to Y only. The stride for U/V is calculated in hardware to be half or equal to the Y plane rounded up to whole 16 byte words. It is necessary for the host to pad lines to ensure each starts on a 16 byte word boundary.
21:11	R/W	XSTART	**X Position Start.** X position of top left corner of plane in pixels (maximum of 2047)
10:0	R/W	YSTART	**Y Position Start.** Y position of top left corner of plane in pixels (maximum of 2047)

4.12.1.6 GPLUT—Graphics Palette LUT Registrer

Address Offset: 0x03FE_2150
Default Value: 0x00000000
Access: R/W
Size: 32 bits

Bits	Access	Name	Description
31:24	R/W	LUTADR	**LUT Address**. Set LUT address to read or write
23:0	R/W	LUTDATA	**LUT Data**. Data to read or write to LUT in RGB666 format

4.12.2 Video Display Registers

The Graphics Display plane registers configure the YUV stream used by the Video Decode (MPEG) Accelerator Unit.

4.12.2.1 VSCTRL—Video Surface Control Register

Address Offset: 0x03FE_2004
Default Value: 0x00000000
Access: R/W
Size: 32 bits

Bits	Access	Name	Description
31	R/W	RSVD	Reserved
30:27	R/W	VPIXFMT	**Video Pixel Format.** 1001b = 16-bit YUV 4:2:0 Planar [YUV12] 1100b = 16-bit YUV 4:2:2 UY0VY1 (U lsb) [UYVY / UYNV] 1101b = 16-bi t YUV 4:2:2 VY0UY1 (V lsb) 1110b = 16-bit YUV 4:2:2 Y0UY1V (Y0 lsb) [YUY2 / YUNV / V422] 1111b = 16-bit YUV 4:2:2 Y0VY1U (Y0 lsb) [YVYU]
26	R/W	GAMMA_EN	**Gamma LUT Interpolation Enable.** 0 = Gamma LUT interpolation inactive 1 = Gamma LUT interpolation active
25	R/W	CSC_EN	**Color Space Conversion Enable.** 0 = Color space conversion inactive 1 = Color space conversion active
24:23	R/W	RSVD	Reserved
22	R/W	COSITED	Selects whether source chroma samples are co-sited with luma, or offset. 0 = Chroma samples are horizontally offset from luma 1 = Chroma samples are horizontally co-sited with luma Note: If co-sited, odd chroma samples are output directly, with even interpolated. If offset, output is always interpolation of input samples.
21:11	R/W	VSWIDTH	**Video Surface Width.** Width of surface in pixels – 1 (max 2047, giving max width 2048) Notes: Represents width of surface in memory, rather than displayed plane, the resultant width of which is affected by scaling.
10:0	R/W	VSHEIGHT	**Video Surface Height.** Height of surface in lines – 1 (max 2047, giving max height 2048) Notes: Must be halved if address generator ‘intfield’ mode is set, as represents height for field rather than frame.

4.12.2.2 VBBASE—Video Blending Base Register

Address Offset: 0x03FE_2024
Default Value: 0x00000000
Access: R/W
Size: 32 bits

Bits	Access	Name	Description
31:24	R/W	GLALPHA	**Global Alpha** (least significant bits reserved if less than 8-bits): all 0 = Entirety of previous surface(s) displayed all 1 = Entirety of this surface displayed
23:0	R/W	COLKEY	**Color Key for Stream.** The color key must be in the unpacked (and de-palletized) RGB data format or YUV format (note that chroma components will have been interpolated).

4.12.2.3 VCMSK—Video Color Key Mask Register

Address Offset: 0x03FE_2044
Default Value: 0x00000000
Access: R/W
Size: 32 bits

Bits	Access	Name	Description
31:24	R/W	RSVD	Reserved
23:0	R/W	COLKEY_M	**Color Key Mask for Stream.** Set bits to zero to mask from color key comparison. The mask is logically AND'ed with the data to be compared against the color key. For example, to match red values in the range 8 to 11, the mask would be 0xFCFFFF, and the key would be 0x080000.

4.12.2.4 VSCADR—Video Stream Control Address Register

Address Offset: 0x03FE_2064
Default Value: 0x01000000
Access: R/W
Size: 32 bits

Bits	Access	Name	Description
31	R/W	STR_EN	**Stream Enable.** 0 = Stream disabled (no memory fetches or blending with other planes) 1 = Stream enabled
30	R/W	COLKEY_EN	**Color Key Enable.** 0 = Color keying disabled 1 = Color keying enabled
29	R/W	COLKEYSRC	**Color Key Source**. 0 = Current plane's color key compared against pixel from previous plane, and current plane's pixel displayed if match (else pixels are optionally alpha blended). i.e. destination color key match selects source pixels. 1 = Current plane's color key compared against pixel from current plane, and previous plane's pixel displayed if match (else pixels are optionally alpha blended). i.e. source color key match selects destination pixels.
28:27	R/W	BLEND_M	**Blend Mode.** 00 = No alpha blending 01 = Inversion for formats with more than 1 bit of pixel alpha. Zero alpha gives transparency, full alpha gives opaque, and intermediate pixel alpha values give inversion of the lower surface pixels. 10 = Global alpha blending 11 = Pixel alpha blending
26	R/W	RSVD	Reserved
25:24	R/W	BLEND_POS	**Plane/Cursor Position.** 00 = Position 0 (bottom) – desktop graphics in architecture diagram 01 = Position 1 – video in architecture diagram 10 = Position 2 (top) – cursor in architecture diagram Note: It is vital that a unique position is programmed for each plane/cursor, even if that plane/cursor is disabled. Failure to do so results in display corruption.
23	R/W	RSVD	Reserved
22:0	R/W	VBASE_ADR	**Base Address.** This field provides bits 26:4 of the base address of the surface (Y in 4:2:0 for video, left-hand side of screen if Split Background); 128 MB range on 16-byte boundaries. This action takes effect immediately.

4.12.2.5 VUBASE—Video U Base Register

Address Offset: 0x03FE_2084
Default Value: 0x00000000
Access: R/W
Size: 32 bits

Bits	Access	Name	Description
31	R/W	UVHALFSTR	**UV Half Stride.** 0 = UV stride equal to Y stride 1 = UV stride half Y stride
30:24	R/W	RSVD	Reserved
23:0	R/W	UBASE_ADR	**U Base Address.** This field provides bits 26:3 of the base address of the 4:2:0 video U plane; 128 MB range on 8-byte boundaries. This action takes effect immediately.

4.12.2.6 VVBASE—Video V Base Register

Address Offset: 0x03FE_20A4
Default Value: 0x00000000
Access: R/W
Size: 32 bits

Bits	Access	Name	Description
31:24	R/W	RSVD	Reserved
23:0	R/W	VBASE_ADR	**V Base Address**. This field provides bits 26:3 of the base address of the 4:2:0 video V plane; 128 MB range on 8-byte boundaries. This action takes effect immediately.

4.12.2.7 VSADR—Video Stride Address Register

Address Offset: 0x03FE_20C4
Default Value: 0x00000000
Access: R/W
Size: 32 bits

Bits	Access	Name	Description
31:22	R/W	SRCSTRIDE	**Source Stride**. Stride of surface in 16 byte words – 1 (max (4095 + 1)*16 = 64 KB) Note: For planar 4:2:0 video, the stride relates to Y only. The stride for U/V is calculated in hardware to be half or equal to the Y plane rounded up to whole 16 byte words. It is necessary for the host to pad lines to ensure each starts on a 16 byte word boundary.
21:11	R/W	XSTART	**X Position Start.** X position of top left corner of plane in pixels (maximum of 2047)
10:0	R/W	YSTART	**Y Position Start.** Y position of top left corner of plane in pixels (maximum of 2047)

4.12.3 Background Control Registers

The Background plane registers configure the RGB value used if the 2D/3D, Video, and Cursor Planes are not used.

4.12.3.1 BGCOLOR—Background Color Register

Address Offset: 0x03FE_2174
Default Value: 0x00000000
Access: R/W
Size: 32 bits

Bits	Access	Name	Description
31:24	R/W	RSVD	Reserved
23:0	R/W	BGNDCOL	**Background Color.** Color of background in RGB888

4.12.4 Hardware Cursor Registers

The Hardware Cursor plane registers configure how the RGB hardware cursor is displayed over all other planes.

4.12.4.1 HCCTRL—Hardware Cursor Control Register

Address Offset: 0x03FE_2100
Default Value: 0x00000000
Access: R/W
Size: 32 bits

Bits	Access	Name	Description
31	R/W	CUR_EN	**Cursor Enable.** 0 = Cursor disabled 1 = Cursor enabled
30	R/W	RSVD	Reserved
29	R/W	COLKEY_EN	**Color Key Enable.** 0 = Color keying disabled 1 = Color keying enabled
28	R/W	COLKEYSCR	**Color Key Source.** 0 = Current plane's color key compared against pixel from previous plane, and current plane's pixel displayed if match (else pixels are optionally alpha blended). That is, destination color key match selects source pixels. 1 = Current plane's color key compared against pixel from current plane, and previous plane's pixel displayed if match (else pixels are optionally alpha blended). That is, source color key match selects destination pixels.
27:26	R/W	BLEND_M	**Blend Mode.** 00 = No alpha blending 01 = Inversion for formats with more than 1 bit of pixel alpha. Zero alpha gives transparency, full alpha gives opaque, and intermediate pixel alpha values give inversion of the lower surface pixels. 10 = Global alpha blending 11 = Pixel alpha blending
25:23	R/W	CPIXFMT	**Cursor Pixel Format.** 011b = 8-bit rgb332 [RGB] 100b = 4-bit alpha + 12-bit rgb444 + [ARGB] 101b = 1-bit alpha + 15-bit rgb555 [ARGB]
22:0	R/W	CBASE_ADR	**Cursor Base Address.** Bits 26:4 of the base address of the cursor; 128 MB range on 16-byte boundaries. This action takes effect immediately.

4.12.4.2 HCSIZE—Hardware Cursor Size Register

Address Offset: 0x03FE_2110
Default Value: 0x00000000
Access: R/W
Size: 32 bits

Bits	Access	Name	Description
31	R/W	RSVD	Reserved
30:29	R/W	BLEND_POS	**Blend Position.** 00 = Position 0 (bottom) – desktop graphics in architecture diagram 01 = Position 1 – video in architecture diagram 10 = Position 2 (top) – cursor in architecture diagram Note: It is vital that a unique position is programmed for each plane/cursor, even if that plane/cursor is disabled. Failure to do so results in display corruption.
28:19	R/W	RSVD	Reserved
18:16	R/W	CWIDTH	**Cursor Width.** Width of cursor in (pixels / 8) – 1 (maximum of 7, giving max width (7 + 1) * 8 = 64)
15:3	R/W	RSVD	Reserved
2:0	R/W	CHEIGHT	**Cursor Height.** Height of cursor in (lines / 8) – 1 (maximum of 7, giving max height (7 + 1) * 8 = 64) Note: Must be halved if address generator 'intfield' mode set, as represents height for field rather than frame.

4.12.4.3 HCPOS—Hardware Cursor Position Register

Address Offset:	0x03FE_2120
Default Value:	0x00000000
Access:	R/W
Size:	32 bits

Bits	Access	Name	Description
31	R/W	RSVD	Reserved
30	R/W	SWITCHSRC	**Switch Cursor Source**. This bit is for the switch cursor source data base address. When alternating, the second address is "CBASE_ADR + 64*64/8" irrespective of the programmed cursor dimensions. 0 = Always display same cursor data 1 = Alternate between cursor base addresses when blinking
29:24	R/W	CURBLINK	**Cursor Blink**. This field provides the number of frames between cursor update. If greater than 0, causes cursor to blink or alternate between cursor data.
23:12	R/W	XSTART	**X Position Start**. Signed X position of top left corner of cursor in pixels (maximum is ±2047)
11:0	R/W	YSTART	**Y Position Start**. Signed Y position of top left corner of cursor in pixels (maximum is ±2047)

4.12.4.4 HCBADR—Hardware Cursor Blend Address Register

Address Offset:	0x03FE_2130
Default Value:	0x00000000
Access:	R/W
Size:	32 bits

Bits	Access	Name	Description
31:24	R/W	GLALPHA	**Global Alpha**. (least significant bits reserved if less than 8-bits): all 0 = Entirety of previous surface(s) displayed all 1 = Entirety of this surface displayed
23:0	R/W	COLKEY	**Color key for Stream**. The color key must be in the unpacked (and de-palletized) RGB data format.

4.12.4.5 HCCKMSK—Hardware Cursor Color Key Mask Register

Address Offset:	0x03FE_2140
Default Value:	0x00000000
Access:	R/W
Size:	32 bits

Bits	Access	Name	Description
31:24	R/W	RSVD	Reserved
23:0	R/W	COLKEY_M	**Color Key Mask for Stream**. Set bits to zero to mask from color key comparison. The mask is logically AND'ed with the data to be compared against the color key. For example, to match red values in the range 8 to 11, the mask would be 0xFCFFFF, and the key would be 0x080000.

4.13 Display Synchronization Registers

This section describes the 2700G7 Multimedia Accelerator's Display Synchronization registers.

4.13.1 DSCTRL—Display Sync Control Register

Address Offset:	0x03FE_2154
Default Value:	0x00000000
Access:	R/W
Size:	32 bits

Bits	Access	Name	Description
31	R/W	SYNCGEN_EN	**Sync Generator Enable**. This bit starts the sync generator. This bit must be set to generate syncs, and should be set after starting pixel fetches. 0 = Disabled 1 = Enabled
30	R/W	RSVD	Reserved
29	R/W	DPL_RST	**Display Software Reset**. 0 = Normal operation. 1 = Software reset.
28	R/W	PWRDN_M	**Power Down Mode**. 0 = Normal operation. 1 = Output valid sync signals, and substitute active data with black pixels.
27	R/W	RSVD	Reserved
26	R/W	UPDSYNCNT	**Display Update Sync Control**. 0 = Generate SYNCs at full free-running field rate, irrespective of reduced DE/DATA field update rate. 1 = Generate SYNCs at reduced DE/DATA field update rate.
25	R/W	UPDINTCNT	**Display Update Interrupt Control**. 0 = Generate interrupts at full free-running field rate. 1 = Generate interrupts only for fields displayed at reduced rate.
24	R/W	UPDCNT	**Display Update Control**. 0 = Free-running or reduced update mode – fields only fetched for display when updwait counter is zero. 1 = Single-shot mode – fields only fetched for display when updfield = 1.
23:20	R/W	RSVD	Reserved
19:16	R/W	UPDWAIT	**Display Update Wait**. This field provides the number of displayed fields to wait before fetching another for update on a flat panel display. Set to zero for normal free-running operation with fetches for all fields.
15:12	R/W	RSVD	Reserved

Bits	Access	Name	Description
11	R/W	CLKPOL	**Pixel Clock Polarity**.
10	R/W	CSYNC_EN	**Composite Output Enable**: 0 = VSYNC outputs vertical sync 1 = VSYNC outputs composite sync (VSYNC OR HSYNC)
9:8	R/W	RSVD	Reserved
7	R/W	VS_SLAVE	**Vertical Sync Master/Slave Control**. 0 = Vertical sync generated internally (vsync master) 1 = Locked to externally provided vertical sync (vsync slave)
6	R/W	HS_SLAVE	**Horizontal Sync Master/Slave Control**. 0 = Horizontal sync generated internally (vsync master) 1 = Locked to externally provided horizontal sync (vsync slave)
5	R/W	BLNK_POL	**Blanking Polarity**. This bit controls blanking signal polarity. 0 = Blanking signal is active high 1 = Blanking signal is active low
4	R/W	BLNK_DIS	**Blank Signal Disable**. Blank also known as data enable for digital displays. When set the blank signal is disabled and the output level is determined by BLNK_POL (0 low, 1 high) 0 = Enable 1 = Disable
3	R/W	VS_POL	**Vertical Sync Polarity**. This bit controls the vertical sync polarity. 0 = Vertical Sync is active high 1 = Vertical Sync is active low
2	R/W	VS_DIS	**Vertical Sync Disable**. When set the vertical syncs are disabled and the output level is determined by VS_POL (0 low, 1 high)
1	R/W	HS_POL	**Horizontal Sync**. This bit controls the horizontal sync polarity. 0 = Horizontal Sync is active high 1 = Horizontal Sync is active low
0	R/W	HS_DIS	**Horizontal Sync Disable**. When set, the horizontal syncs are disabled and the output level is determined by HS_POL (0 low, 1 high). 0 = Enable 1 = Disable

4.13.2 DUCTRL—Display Update Control Register

Address Offset: 0x03FE_230C
Default Value: 0x00000000
Access: R/W
Size: 32 bits

Bits	Access	Name	Description
31:1	R/W	RSVD	Reserved
0	R/W	UPFIELD	**Update Field**. Set to 1 to update next field for display when UPDCNT = 1. Automatically cleared to 0 after the update has occurred.

4.13.3 DHT01—Display Horizontal Timing Register 01

Address Offset: 0x03FE_2158
Default Value: 0x00000000
Access: R/W
Size: 32 bits

Bits	Access	Name	Description
31:28	R/W	RSVD	Reserved
27:16	R/W	HBPS	**Horizontal Back Porch Start.** (HBPS – max 4095). The number of pixels from start of horizontal sync to start of the horizontal back porch (region of blanking which follows Horizontal Sync)
15:12	R/W	RSVD	Reserved
11:0	R/W	HT	**Horizontal Total** (HT – max 4095). The total number of pixels in a line.

4.13.4 DHT02—Display Horizontal Timing Register 02

Address Offset: 0x03FE_215C
Default Value: 0x00000000
Access: R/W
Size: 32 bits

Bits	Access	Name	Description
31:28	R/W	RSVD	Reserved
27:16	R/W	HAS	**Horizontal Active Start** (HAS – max 4095). The number of pixels from start of horizontal sync to first active pixel.
15:12	R/W	RSVD	Reserved
11:0	R/W	HLBS	**Horizontal Left Border Start** (HLBS – max 4095). The number of pixels from start of horizontal sync to start of left border (region between end of blanking and start of active video). The border may be used to center a smaller image in a screen (e.g., 800x600 display onto 1024x768 LCD timings).

4.13.5 DHT03—Display Horizontal Timing Register 03

Address Offset: 0x03FE_2160
Default Value: 0x00000000
Access: R/W
Size: 32 bits

Bits	Access	Name	Description
31:28	R/W	RSVD	Reserved
27:16	R/W	HFPS	**Horizontal Front Porch Start** (HFPS – max 4095). The number of pixels from start of horizontal sync to first pixel of blanking after active video.
15:12	R/W	RSVD	Reserved
11:0	R/W	HRBS	**Horizontal Right Border Start** (HRBS – max 4095). The number of pixels from start of horizontal sync to start of the right border (region between end of active video and start of blanking). The border may be used to center a smaller image in a screen (e.g., 800x600 display onto 1024x768 LCD timings).

4.13.6 DVT01—Display Vertical Timing Register 01

Address Offset: 0x03FE_2164
Default Value: 0x00000000
Access: R/W
Size: 32 bits

Bits	Access	Name	Description
31:28	R/W	RSVD	Reserved
27:16	R/W	VBPS	**Vertical Back Porch Start** (VBPS – max 4095). The number of lines from start of vertical sync to start of the vertical back porch (region of blanking which follows vertical sync).
15:12	R/W	RSVD	Reserved
11:0	R/W	VT	**Vertical Total** (VT – max 4095). The total number of lines in a field.

4.13.7 DVT02—Display Vertical Timing Register 02

Address Offset: 0x03FE_2168
Default Value: 0x00000000
Access: R/W
Size: 32 bits

Bits	Access	Name	Description
31:28	R/W	RSVD	Reserved
27:16	R/W	VAS	**Vertical Active Start** (VAS – max 4095). The number of lines from start of vertical sync to first active line.
15:12	R/W	RSVD	Reserved
11:0	R/W	VTBS	**Vertical Top Border Start** (VTBS – max 4095). The number of lines from start of vertical sync to start of the top border (region between end of blanking and start of active video). The border may be used to center a smaller image in a screen (e.g., 800x600 display onto 1024x768 LCD timings).

4.13.8 DVT03—Display Vertical Timing Register 03

Address Offset: 0x03FE_216C
Default Value: 0x00000000
Access: R/W
Size: 32 bits

Bits	Access	Name	Description
31:28	R/W	RSVD	Reserved
27:16	R/W	VFPS	**Vertical Front Porch Start** (VFPS – max 4095). The number of lines from start of vertical sync to first line of blanking after active video.
15:12	R/W	RSVD	Reserved
11:0	R/W	VBBS	**Vertical Bottom Border Start** (VBBS – max 4095). The number of lines from start of vertical sync to start of the bottom border (region between end of active video and start of blanking). The border may be used to center a smaller image in a screen (e.g., 800x600 display onto 1024x768 LCD timings).

4.13.9 DVECTRL—Display Vertical Event Control Register

Address Offset: 0x03FE_2310
Default Value: 0x00000000
Access: R/W
Size: 32 bits

Bits	Access	Name	Description
31:28	R/W	RSVD	Reserved
27:16	R/W	VEVENT	**Vertical Event Start** (VEVENT – max 4095). Vertical line on which to indicate that registers can be updated without visual artifacts – causes generation of VEVENT interrupt (refer to Interrupts section). Normally set to 0, but should be increased above vertical bottom border start (VBBS) when operating with reduced blanking displays to allow line stores and buffers to fill in time for display. The time between VEVENT and VFETCH must be sufficient for the number of registers that need to be updated.
15:12	R/W	RSVD	Reserved
11:0	R/W	VFETCH	**Vertical Fetch Start** (VFETCH – max 4095). Vertical line number before memory fetches and pixel generation commences. Normally set to vertical back porch start (VBPS), but should be reduced when operating with reduced blanking displays to allow line stores and buffers to fill in time for display. The time between VEVENT and VFETCH must be sufficient for the number of registers that need to be updated.

4.13.10 DHDET—Display Horizontal DE Timing Register

Address Offset: 0x03FE_2314
Default Value: 0x00000000
Access: R/W
Size: 32 bits

Bits	Access	Name	Description
31:28	R/W	RSVD	Reserved
27:16	R/W	HDES	**Horizontal Data Enable Start** (HDES – max 4095). The start position for active pixels enabled on a flat panel display. Set to HLBS if all pixels including border are being displayed, since pixels with all bits set to the blank level are substituted when DE is inactive.
15:12	R/W	RSVD	Reserved
11:0	R/W	HDEF	**Horizontal Data Enable Finish** (HDEF – max 4095). The finish position for active pixels enabled on a flat panel display. Set to HFPS if all pixels including border are being displayed, since pixels with all bits set to the blank level are substituted when DE is inactive.

4.13.11 DVDET—Display Vertical DE Timing Register

Address Offset: 0x03FE_2318
Default Value: 0x00000000
Access: R/W
Size: 32 bits

Bits	Access	Name	Description
31:28	R/W	RSVD	Reserved
27:16	R/W	VDES	**Vertical Data Enable Start** (VDES – max 4095). The start position for active pixels enabled on a flat panel display. Set to VTBS if all lines including border are being displayed, since black pixels are substituted when DE is inactive.
15:12	R/W	RSVD	Reserved
11:0	R/W	VDEF	**Vertical Data Enable Finish** (VDEF – max 4095). The finish position for active pixels enabled on a flat panel display. Set to VFPS if all lines including border are being displayed, since black pixels are substituted when DE is inactive.

4.13.12 DODMSK—Display Output Data Mask Register

Address Offset:	0x03FE_231C
Default Value:	0x00000000
Access:	R/W
Size:	32 bits

Bits	Access	Name	Description
31	R/W	MASK_LVL	**Mask Level.** This bit controls the level that the output bits are tied to when masked. 0 = Masked output bits tied low. 1 = Masked output bits tied high.
30	R/W	BLNK_LVL	**Blank Level.** This bit controls the level that the output bits are tied to when DE is inactive. 0 = Blanked output bits tied low. 1 = Blanked output bits tied high.
29:24	R/W	RSVD	Reserved
23:16	R/W	MASK_B	**Mask Channel B.** This field provides an output data mask for channel B. Masked bits are tied to level set using MASK_LVL control bit in this register.
15:8	R/W	MASK_G	**Mask Channel G.** This field provides an output data mask for channel G. Masked bits are tied to level set using MASK_LVL control bit in this register.
7:0	R/W	MASK_R	**Mask Channel R.** This field provides an output data mask for channel R. Masked bits are tied to level set using MASK_LVL control bit in this register.

4.13.13 DBCOL—Display Border Color Register

Address Offset: 0x03FE_2170
Default Value: 0x00000000
Access: R/W
Size: 32 bits

Bits	Access	Name	Description
31:24	R/W	RSVD	Reserved
23:0	R/W	BORDCOL	**Border Color**. Color of border in RGB888

4.13.14 DSIG—Display Signature Register

Address Offset: 0x03FE_2184
Default Value: 0x00000000
Access: RO
Size: 32 bits

Bits	Access	Name	Description
31:0	RO	DSIG	**Display Signature.** This field provides the signature for the active display area (excludes border and syncs)

4.13.15 DVLNUM—Display Vertical Line Number Register

Address Offset: 0x03FE_2308
Default Value: 0x00000000
Access: RO
Size: 32 bits

Bits	Access	Name	Description
31:12	RO	RSVD	Reserved
11:0	RO	VLINE	**Vertical Line**. This field provides the current line number.

4.13.16 DMCTRL—Display Memory Control Register

Address Offset: 0x03FE_2188
Default Value: 0x18383808
Access: R/W
Size: 32 bits

Bits	Access	Name	Description
31:30	R/W	MEM_REF	**Memory Refresh**. This field selects enable flag generation for memory refresh controller. 00 = Always enabled, memory refreshes can occur during active video. 01 = Memory refreshes enabled during horizontal blanking only. 10 = Memory refreshes enabled during vertical blanking only. 11 = Memory refreshes enabled during horizontal and vertical blanking.
29:24	R/W	UV_THRHLD	**UV Threshold**. This field specifies the threshold below which U/V buffer requests are issued.
23	R/W	RSVD	Reserved
22:16	R/W	V_THRHLD	**V Threshold**. This field specifies the threshold below which Y buffer requests are issued.
15	R/W	RSVD	Reserved
14:8	R/W	D_THRHLD	**V Threshold**. This field specifies the threshold below which buffer requests are issued.
7:6	R/W	RSVD	Reserved
5:0	R/W	BURSTLN	**Burst Length**. This field specifies the number of consecutive words issued from the current base address before moving onto the next. In the case of planar 420 data, the U and V requests are of the length specified in this register, with two Y bursts generated for every UV request.

4.13.17 DINTRS—Display Interrupt Status Register

Address Offset: 0x03FE_2178
Default Value: 0x00000000
Access: R/W
Size: 32 bits

The interrupt status register indicates the source of any interrupt caused by the display pipeline. These interrupts only generate an external interrupt if the relevant enable bit in the interrupt enable register is set. Setting bits to 0 clears the respective bit in the Interrupt Status register. When all enabled bits are cleared, the display pipeline de-asserts its interrupt to the core. If any bits are written to this register as a 1, they are set in the Interrupt Status register, causing an interrupt to be generated (this is intended for debug purposes only).

Bits	Access	Name	Description
31:19	R/W	RSVD	Reserved
18	R/W	CUR_OR_S	**Cursor Overrun Status.** This bit indicates over-run for stream curs.
17	R/W	STR2_OR_S	**Stream 2 Overrun Status.** This bit indicates over-run for stream str2.
16	R/W	STR1_OR_S	**Stream 1 Overrun Status.** This bit indicates over-run for stream str1.
15:7	R/W	RSVD	Reserved
6	R/W	CUR_UR_S	**Cursor Underrun Status.** This bit indicates under-run for stream curs.
5	R/W	STR2_UR_S	**Stream 2 Underrun Status.** This bit indicates under-run for stream str2.
4	R/W	STR1_UR_S	**Stream 1 Underrun Status.** This bit indicates under-run for stream str1.
3	R/W	VEVENT1_S	**Visual Event 1 Status.** This bit indicates start of region when safe to update registers without visual artifacts for second field.
2	R/W	VEVENT0_S	**Visual Event 0 Status.** This bit indicates start of region when safe to update registers without visual artifacts for first field.
1	R/W	HBLNK1_S	**Horizontal Blanking 1 Status.** This bit indicates start of horizontal blanking for second field.
0	R/W	HBLNK0_S	**Horizontal Blanking 0 Status**. This bit indicates start of horizontal blanking for frame or first field.

4.13.18 DINTRE—Display Interrupt Enable Register

Address Offset:	0x03FE_217C
Default Value:	0x00000000
Access:	R/W
Size:	32 bits

This register enables display interrupts. Writing a 1 to a bit field enables the relevant interrupt. All the bit fields correspond exactly to those in the Interrupt Status register.

Bits	Access	Name	Description
31:19	R/W	RSVD	Reserved
18	R/W	CUR_OR_EN	**Cursor Overrun Enable.** This bit enables over-run interrupt for stream curs.
17	R/W	STR2_OR_EN	**Stream 2 Overrun Enable.** This bit enables over-run interrupt for stream str2.
16	R/W	STR1_OR_EN	**Stream 1 Overrun Enable.** This bit enables over-run interrupt for stream str1.
15:7	R/W	RSVD	Reserved
6	R/W	CUR_UR_ EN	**Cursor Underrun Enable.** This bit enables under-run interrupt for stream curs.
5	R/W	STR2_UR_ EN	**Stream 2 Underrun Enable.** This bit enables under-run interrupt for stream str2.
4	R/W	STR1_UR_ EN	**Stream 1 Underrun Enable.** This bit enables under-run interrupt for stream str1.
3	R/W	VEVENT1_ EN	**Visual Event 1 Enable.** This bit enables interrupt indicating start of region when safe to update registers without visual artifacts for second field.
2	R/W	VEVENT0_ EN	**Visual Event 0 Enable.** This bit enables interrupt indicating start of region when safe to update registers without visual artifacts for first field.
1	R/W	HBLNK1_ EN	**Horizontal Blanking 1 Enable.** This bit enables the start of the horizontal blanking interrupt for second field.
0	R/W	HBLNK0_ EN	**Horizontal Blanking 0 Enable**. This bit enables the start of the horizontal blanking interrupt for frame or first field.

4.13.19 DINTRCNT—Display Interrupt Control Register

Address Offset: 0x03FE_2180
Default Value: 0x00000000
Access: R/W
Size: 32 bits

Bits	Access	Name	Description
31:17	R/W	RSVD	Reserved
16	R/W	HBLNK_LN	**Horizontal Blanking Line Enable**. This bit enables horizontal blanking interrupt for specific line: 0 = Horizontal blanking interrupt generated for all lines. (default) 1 = Horizontal blanking interrupt generated for specified line.
15:12	R/W	RSVD	Reserved
11:0	R/W	HBLNK_LNNO	**Horizontal Blanking Line Number**. This field provides a horizontal line number on which to generate horizontal blanking interrupt.

4.13.20 DLSTS—Display Load Status Register

Address Offset: 0x03FE_2300
Default Value: 0x08000000
Access: RO
Size: 32 bits

Bits	Access	Name	Description
31:24	RO	RSVD	Reserved
23	RO	RLD_ADONE	**Register Load Address Done.** 0 = Actively processing list. 1 = Ready to process another list of register address/data held in memory.
22:0	RO	RLD_ADOUT	**Register Load Address Out.** This field represents bits 26:4 of the register list being processed; 128 MB range on 16-byte boundaries. Updated at the start of VSYNC, when the register list address and length are taken for processing.

4.13.21 DLLCTRL—Display List Load Control Register

Address Offset: 0x03FE_2304
Default Value: 0x00000000
Access: R/W
Size: 32 bits

Bits	Access	Name	Description
31:24	R/W	RLD_ADRLN	**Register Load Address Length.** This field provides the length of the list of register address/data list held in memory, in number of address/data pairs (8-bytes).
23	R/W	RLD_VAL	**Register Load Valid.** This bit, when set, indicates that the address, and length, of the memory register list is valid. This flag is cleared at the start of VSYNC, when the register list address and length are taken for processing.
22:0	R/W	RLD_ADRIN	**Register Load Address In.** This field represents bits 26:4 of the base address for the next list of register address/data held in memory ready to be processed; 128 MB range on 16-byte boundaries.

4.14 Clipping and Scaling Registers

This section describes the 2700G7 Multimedia Accelerator’s Clipping and Scaling registers.

4.14.1 CLIPCTRL—Clipping Control Register

Address Offset: 0x03FE_218C
Default Value: 0x00000000
Access: R/W
Size: 32 bits

Bits	Access	Name	Description
31:27	R/W	RSVD	Reserved
26:16	R/W	HSKIP	**Horizontal Skip.** Number of pixels to skip from left hand side before scaling. If displaying MPEG2 video, and external panning is enabled, Hskip should be set to center the region passed to the scaler within the source image.
15:11	R/W	RSVD	Reserved
10:0	R/W	VSKIP	**Vertical Skip.** Number of lines to skip from top of field before scaling.

4.14.2 SPOCTRL—Scale Pitch/Order Control Register

Address Offset:	0x03FE_2190
Default Value:	0x00000000
Access:	R/W
Size:	32 bits

Bits	Access	Name	Description
31	R/W	H_SC_BP	**Horizontal Video Scaler Bypass.** 0 = No Bypass 1 = Bypass
30	R/W	V_SC_BP	**Vertical Video Scaler Bypass.** 0 = No Bypass 1 = Bypass
29	R/W	HV_SC_OR	**Horizontal/Vertical Scaling Order.** 0 = Vertical scaling performed prior to horizontal scaling. 1 = Horizontal scaling performed prior to vertical scaling.
28	R/W	RSVD	Reserved
27	R/W	VS_UR_C	**Vertical Scaling Underrun Control.** 0 = Acknowledge under-run, and treat in same manner as unscaled planes. 1 = Ignore under-run. Gives better results in many situations due to scaler FIFO.
26:18	R/W	RSVD	Reserved
17:16	R/W	VORDER	**Vertical Filter Order.** Should be set to 2-tap when scaling down to less than one third of the height of the source image; otherwise, can be set to 4-tap. 00 = 1-tap (decimation/replication). 01 = 2-tap (bilinear). 11 = 4-tap.
15:0	R/W	VPITCH	**Vertical Pitch.** This field is the vertical pitch (1/Scale Factor) for HQ video filter. 5.11 fixed point binary

4.14.3 SVCTRL—Scale Vertical Control Register

Address Offset: 0x03FE_2194
Default Value: 0x00000000
Access: R/W
Size: 32 bits

Bits	Access	Name	Description
31:16	R/W	INITIAL1	**Initial 1.** This field provides the initial vertical position of field 1 for HQ video filter. 5.11 fixed point binary. If using the vertical scaler to generate fields on an interlaced display, this field should be set to half of the vertical pitch (vpitch/2).
15:0	R/W	INITIAL0	**Initial 0.** This field provides the initial vertical position of field 0 for HQ video filter. 5.11 fixed point binary

4.14.4 SHCTRL—Scale Horizontal Control Register

Address Offset: 0x03FE_21B0
Default Value: 0x00000000
Access: R/W
Size: 32 bits

Bits	Access	Name	Description
31:16	R/W	HINITIAL	**Horizontal Initial.** This field provides the initial horizontal position for HQ video filter. 5.11 fixed point binary. Should be set to center tap position – for 8 taps, set to 4.000.
15	R/W	HDECIM	**Horizontal Decimation.** If set, the number of pixels are halved by decimation prior to scaling.
14:0	R/W	HPITCH	**Horizontal Pitch.** This field provides the horizontal scale pitch (1/Scale Factor) for HQ video filter. If scaling down to less than a quarter of the source image size, the pitch should be halved and horizontal decimation activated. 4.11 fixed point binary

4.14.5 VSCOEFF[0:4]—Video Scalar Vertical Coefficient Registers

Address Offset: 0x03FE_2198 – 0x03FE_21A8
Default Value: 0x00000000
Access: R/W

Number of 2.6-bit 2’s complement fraction coefficients for vertical filter,

N = (no. interpolation points)x(max no. taps)/2 + 1 = 17 for 4 taps; 9 for 2 taps

<table>
<tr><th>Offset</th><th>Symbol</th><th>Bit</th><th>Coeff</th><th>Description</th><th>Default Value</th></tr>
<tr><td>0x03FE_2198</td><td>VSCOEFF 0</td><td>31:24, 23:16, 15:8, 7:0</td><td>3:0</td><td>Four 2.6-bit 2’s complement fractions</td><td>0x00000000</td></tr>
<tr><td>0x03FE_219C</td><td>VSCOEFF 1</td><td>31:24, 23:16, 15:8, 7:0</td><td>7:4</td><td>Four 2.6-bit 2’s complement fractions</td><td>0x00000000</td></tr>
<tr><td>0x03FE_21A0</td><td>VSCOEFF 2</td><td>31:24, 23:16, 15:8, 7:0</td><td>11:8</td><td>Four 2.6-bit 2’s complement fractions</td><td>0x00000000</td></tr>
<tr><td>0x03FE_21A4</td><td>VSCOEFF 3</td><td>31:24, 23:16, 15:8, 7:0</td><td>15:12</td><td>Four 2.6-bit 2’s complement fractions</td><td>0x00000000</td></tr>
<tr><td rowspan="2">0x03FE_21A8</td><td rowspan="2">VSCOEFF 4</td><td>31:24</td><td>16</td><td>One 2.6-bit 2’s complement fraction</td><td rowspan="2">0x00000000</td></tr>
<tr><td colspan="2">23:0</td><td>Reserved</td></tr>
</table>

4.14.6 SSIZE—Scale Surface Size Register

Address Offset: 0x03FE_21D8
Default Value: 0x00000000
Access: R/W
Size: 32 bits

Bits	Access	Name	Description
31:27	R/W	RSVD	Reserved
26:16	R/W	SC_WIDTH	**Scaled Width.** Width of surface after scaling in pixels – 1 (maximum is 2047, giving max width of 2048) This is the width of the scaled surface when blended with other planes, and must exclude skipped horizontal pixels. If the scaler setup generates fewer pixels than specified by this width, it will continue to filter the last input data in order to meet the specified width. Likewise, if this width is less than the number of pixels created by the scaler, pixels at the end of the line will be discarded. Every attempt should be made to ensure that the scaler generates as close to the required number of pixels as possible, as significantly fewer will lead to a noticeable visual artifact at the end of line, and with more there is the possibility of having insufficient time to discard pixels before the next start of line.
15:11	R/W	RSVD	Reserved
10:0	R/W	SC_HEIGHT	**Scaled Height.** Height of surface after scaling in lines – 1 (maximum is 2047, giving max height of 2048) This is the height of the scaled surface when blended with other planes. If the scaler setup generates fewer lines than specified by this height, it will continue to filter the last input data in order to meet the specified height. Likewise, if this height is less than the number of pixels created by the scaler, lines at the end of the frame will be discarded. Every attempt should be made to ensure that the scaler generates as close to the required number of lines as possible, as significantly fewer will lead to a noticeable visual artifact at the end of frame. Must be halved if address generator ‘intfield’ mode set, as represents height for field rather than frame.

4.14.7 HSCOEFF[0:8]—Video Scalar Horizontal Coefficient Register

Address Offset: 0x03FE_21B4 – 0x03FE_21D4
Default Value: 0x00000000
Access: R/W

Number of 2.6-bit 2’s complement fraction coefficients for horizontal filter,

N = (no. interpolation points)x(max no. taps)/2 + 1 = 33 for 8 taps

Offset	Symbol	Bit	Coeff	Description	Default Value
0x03FE_21B4	HSCOEFF0	31:24, 23:16, 15:8, 7:0	3:0	Four 2.6-bit 2’s complement fractions	0x00000000
0x03FE_21B8	HSCOEFF1	31:24, 23:16, 15:8, 7:0	7:4	Four 2.6-bit 2’s complement fractions	0x00000000
0x03FE_21BC	HSCOEFF2	31:24, 23:16, 15:8, 7:0	11:8	Four 2.6-bit 2’s complement fractions	0x00000000
0x03FE_21C0	HSCOEFF3	31:24, 23:16, 15:8, 7:0	15:12	Four 2.6-bit 2’s complement fractions	0x00000000
0x03FE_21C4	HSCOEFF4	31:24, 23:16, 15:8, 7:0	19:16	Four 2.6-bit 2’s complement fractions	0x00000000
0x03FE_21C8	HSCOEFF5	31:24, 23:16, 15:8, 7:0	23:20	Four 2.6-bit 2’s complement fractions	0x00000000
0x03FE_21CC	HSCOEFF6	31:24, 23:16, 15:8, 7:0	27:24	Four 2.6-bit 2’s complement fractions	0x00000000
0x03FE_21D0	HSCOEFF7	31:24, 23:16, 15:8, 7:0	31:28	Four 2.6-bit 2’s complement fractions	0x00000000
0x03FE_21D4	HSCOEFF8	31:24	32	One 2.6-bit 2’s complement fraction	0x00000000
		23:0		Reserved	

4.15 Gamma Adjustment

4.15.1 Gamma Adjustment Description

The Gamma adjustment registers allow the RGB values generated by the Video and Graphics Display Streams to be adjusted. Refer to Chapter 3 for more information about Gamma Correction.

4.15.2 VIDGAM[0:16]—Video Gamma LUT Index Registers

Address Offset: 0x03FE_2200 – 0x03FE_2240
Default Value: See table below
Access: R/W

Bits 31:24 of the following registers are reserved:

Offset	Symbol	Bit	Symbol	Format	Default Value
0x03FE_2200	VIDGAM0	23:0	Gamma Index 0	RGB888	0x00000000
0x03FE_2204	VIDGAM1	23:0	Gamma Index 1	RGB888	0x00101010
0x03FE_2208	VIDGAM2	23:0	Gamma Index 2	RGB888	0x00202020
0x03FE_220C	VIDGAM3	23:0	Gamma Index 3	RGB888	0x00303030
0x03FE_2210	VIDGAM4	23:0	Gamma Index 4	RGB888	0x00404040
0x03FE_2214	VIDGAM5	23:0	Gamma Index 5	RGB888	0x00505050
0x03FE_2218	VIDGAM6	23:0	Gamma Index 6	RGB888	0x00606060
0x03FE_221C	VIDGAM7	23:0	Gamma Index 7	RGB888	0x00707070
0x03FE_2220	VIDGAM8	23:0	Gamma Index 8	RGB888	0x00808080
0x03FE_2224	VIDGAM9	23:0	Gamma Index 9	RGB888	0x00909090
0x03FE_2228	VIDGAM10	23:0	Gamma Index 10	RGB888	0x00A0A0A0
0x03FE_222C	VIDGAM11	23:0	Gamma Index 11	RGB888	0x00B0B0B0
0x03FE_2230	VIDGAM12	23:0	Gamma Index 12	RGB888	0x0C0C0C0
0x03FE_2234	VIDGAM13	23:0	Gamma Index 13	RGB888	0x00D0D0D0
0x03FE_2238	VIDGAM14	23:0	Gamma Index 14	RGB888	0x00E0E0E0
0x03FE_223C	VIDGAM15	23:0	Gamma Index 15	RGB888	0x00F0F0F0
0x03FE_2240	GFXGAM16	23:0	Gamma Index 16	RGB888	0x00FFFFFF

4.15.3 GFXGAM[0:16]—Graphics Gamma LUT Index Registers

Address Offset:	0x03FE_2250 – 0x03FE_2290
Default Value:	
Access:	R/W
Size	32 bits

Bits 31:24 of the following registers are reserved:

Offset	Symbol	Bit	Symbol	Format	Default Value
0x03FE_2250	GFXGAM0	23:0	Gamma Index 0	RGB888	0x00000000
0x03FE_2254	GFXGAM1	23:0	Gamma Index 1	RGB888	0x00101010
0x03FE_2258	GFXGAM2	23:0	Gamma Index 2	RGB888	0x00202020
0x03FE_225C	GFXGAM3	23:0	Gamma Index 3	RGB888	0x00303030
0x03FE_2260	GFXGAM4	23:0	Gamma Index 4	RGB888	0x00404040
0x03FE_2264	GFXGAM5	23:0	Gamma Index 5	RGB888	0x00505050
0x03FE_2268	GFXGAM6	23:0	Gamma Index 6	RGB888	0x00606060
0x03FE_226C	GFXGAM7	23:0	Gamma Index 7	RGB888	0x00707070
0x03FE_2270	GFXGAM8	23:0	Gamma Index 8	RGB888	0x00808080
0x03FE_2274	GFXGAM9	23:0	Gamma Index 9	RGB888	0x00909090
0x03FE_2278	GFXGAM10	23:0	Gamma Index 10	RGB888	0x00A0A0A0
0x03FE_227C	GFXGAM11	23:0	Gamma Index 11	RGB888	0x00B0B0B0
0x03FE_2280	GFXGAM12	23:0	Gamma Index 12	RGB888	0x0C0C0C0
0x03FE_2284	GFXGAM13	23:0	Gamma Index 13	RGB888	0x00D0D0D0
0x03FE_2288	GFXGAM14	23:0	Gamma Index 14	RGB888	0x00E0E0E0
0x03FE_228C	GFXGAM15	23:0	Gamma Index 15	RGB888	0x00F0F0F0
0x03FE_2290	GFXGAM16	23:0	Gamma Index 16	RGB888	0x00FFFFFF

4.16 Color Space Conversion Registers

This section describes the 2700G7 Multimedia Accelerator's color conversion registers.

4.16.1 Color Space Conversion Coefficients

YUV-to-RGB color space conversion coefficients are a fully programmable 3x3 matrix as follows:

R' = (Cry*(Y-16)/64 + Crv*(V-128)/64 + Cru*(U-128)/64)/4

G' = (Cgy*(Y-16)/64 + Cgv*(V-128)/64 + Cgu*(U-128)/64)/4

B' = (Cby*(Y-16)/64 + Cbv*(V-128)/64 + Cbu*(U-128)/64)/4

where C(r,g,b)(y,u,v) = 11 bit signed integers.

4.16.2 CSC01—Color Space Coefficient Register 01

Address Offset: 0x03FE_2330
Default Value: 0x0000012A
Access: R/W
Size: 32 bits

Bits	Access	Name	Description
31:22	R/W	RSVD	Reserved
21:11	R/W	COEF_UR	**U CSC Coefficient for R Channel.**
10:0	R/W	COEF_YR	**Y CSC Coefficient for R Channel.**

4.16.3 CSC02—Color Space Coefficient Register 02

Address Offset: 0x03FE_2334
Default Value: 0x000951CB
Access: R/W
Size: 32 bits

Bits	Access	Name	Description
31:22	R/W	RSVD	Reserved
21:11	R/W	COEF_GY	**Y CSC Coefficient for G Channel.**
10:0	R/W	COEF_RV	**V CSC Coefficient for R Channel.**

4.16.4 CSC03—Color Space Coefficient Register 03

Address Offset: 0x03FE_2338
Default Value: 0x003BBFC9
Access: R/W
Size: 32 bits

Bits	Access	Name	Description
31:22	R/W	RSVD	Reserved
21:11	R/W	COEF_GV	**V CSC Coefficient for G Channel.**
10:0	R/W	COEF_GU	**U CSC Coefficient for G Channel.**

4.16.5 CSC04—Color Space Coefficient Register 04

Address Offset: 0x03FE_233C
Default Value: 0x0010E92A
Access: R/W
Size: 32 bits

Bits	Access	Name	Description
31:22	R/W	RSVD	Reserved
21:11	R/W	COEF_BU	**U CSC Coefficient for B Channel.**
10:0	R/W	COEF_BY	**Y CSC Coefficient for B Channel.**

4.16.6 CSC05—Color Space Coefficient Register 05

Address Offset: 0x03FE_2340
Default Value: 0x00000000
Access: R/W
Size: 32 bits

Bits	Access	Name	Description
31:11	R/W	RSVD	Reserved
10:0	R/W	COEF_BV	**V CSC Coefficient for B Channel.**

§

5 Electrical Characteristics

This chapter contains the DC and AC electrical characteristics for the 2700G7 Multimedia Accelerator.

5.1 Signal Configuration

The 2700G7 Multimedia Accelerator graphics accelerator interfaces have flexibility in setting I/O voltages and drive buffer strengths. The voltage options for interfaces are as shown in Table 5-1.

Table 5-1. Interface Voltage Options

Symbol	Interface	Voltage	Max. Frequency[1]
V_{CC}_SYS	General System Bus[2]	1.8 V	100 MHz
		2.5 V	
V_{CC}_LCD_IN	LCD Input	1.8 V, 2.5 V	46 MHz
V_{CC}_LCD1	Primary LCD	1.8 V, 2.5 V, 3.3 V	100 MHz[3]
V_{CC}_LCD2	Secondary LCD	1.8 V, 2.5 V, 3.3 V	100 MHz[3]
V_{CC}_LM	Local Memory Bus	1.8 V	100 MHz
V_{CC}_SDRAM	Local Memory Device	1.8 V	100 MHz
V_{CC}_IO[4]	Misc. I/O Power Supply	3.3 V	—-

NOTES:

1. Actual operating frequencies are dependent on required clocking relationships.
2. The general system bus frequencies specified refer to the internal GSB clock only. Since VLIO and SRAM protocols are asynchronous, actual interface transfers rates are dependent on both the PXA27x processor and the 2700G7 Multimedia Accelerator internal general system bus frequencies.
3. Based on 1024x768 resolution, 60 Hz refresh rate (VESA DMT timings).
4. V_{CC_IO} should always be 3.3 V for ESD purposes. Any other I/O voltage rail that uses 3.3 V should be connected to the V_{CC_IO} rail.

In addition to voltage flexibility, the 2700G7 Multimedia Accelerator graphics accelerator I/O buffers have flexibility in programming the drive strengths for different interfaces. The I/Os can be programmed (on an interface by interface basis) to have a weak or a strong drive strength.

5.2 DC Parameters

The V_{DDO} symbol in Table 5-2 and Table 5-3 is used to collectively denote the voltage rail for different interfaces. For example, $V_{DDO1.8}$ denotes an interface operating at 1.8 V I/O voltage.

Table 5-2 lists operating conditions of the I/O power supply and the crystal oscillator interfaces. The general DC characteristics of the interfaces are given in Table 5-3.

Note: All voltage references are with respect to V_{SS}.

Table 5-2. Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC_CORE}	Core Power Supply	1.14	1.2	1.296	V
T_J	Junction Temperature under BIAS[1, 2]	-25	—	85	°C
$V_{DDO1.8}$	I/O Power Supplies	1.71	1.8	2.16	V
$V_{DDO2.5}$		2.25	2.5	2.75	V
$V_{DDO3.3}$		3.0	3.3	3.6	V
Analog Power Supplies					
V_{AA_XTAL}	Crystal Oscillator	2.25	2.5	2.75	V
$V_{CCA\_CORE\_PLL}$	Core PLL	2.25	2.5	2.75	V
$V_{CCA\_DISP\_PLL}$	Display PLL	2.25	2.5	2.75	V

NOTES:

1. The die temperature range is also known as the junction temperature range.
2. System design must ensure that the device case temperature is maintained within the specified limits. In some system applications it may be necessary to use external thermal management (for example, a package-mounted heat spreader) or configure the device to limit power consumption and maintain acceptable case temperatures.

Table 5-3. General DC Characteristics

Symbol	Description	Min	Max	Units
V_{IH}	Input High Voltage	0.8 * V_{DDO}	—	V
V_{IL}	Input Low Voltage	—	0.2 * V_{DDO}	V
I_{IN}	Input Leakage (VI – VDDO or GND)	—	±1	µA
V_{OH}	Output High Voltage	0.85 * V_{DDO}	V_{DDO}	V
V_{OL}	Output Low Voltage	V_{SS}	0.15 * V_{DDO}	V
I_{oh_s10}	Output High Current (DRIVE = STRONG for 2.5 V or 3.3 V I/O mode)	10	—	mA
I_{ol_s10}	Output Low Current (DRIVE= STRONG for 2.5 V or 3.3 V I/O mode)	-10	—	mA
I_{oh_s6}	Output High Current (DRIVE = STRONG for 1.8 V I/O mode)	6	—	mA
I_{ol_s6}	Output Low Current (DRIVE= STRONG for 1.8 V I/O mode)	-6	—	mA
I_{oh_w3}	Output High Current (DRIVE = WEAK for all I/O modes)	3	—	mA
I_{ol_w3}	Output Low Current (DRIVE = WEAK for all I/O modes)	-3	—	mA
C_{in}	Input Capacitance	—	4	pF
Overshoot	Maximum Overshoot for 1 ns	—	1	V

5.3 AC Parameters

This section provides the AC timing diagrams and associated AC parameters for the various interfaces and functions of the 2700G7 Multimedia Accelerator.

5.3.1 General System Bus Timing

Figure 5-1. VLIO Write Timing (see Table 5-4)

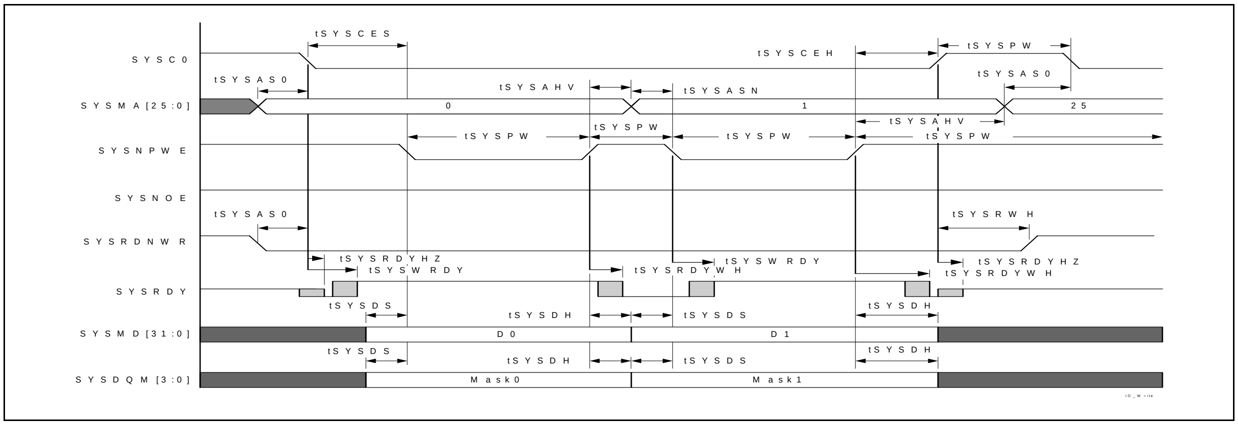


Figure 5-2. VLIO Read Timing (see Table 5-4)

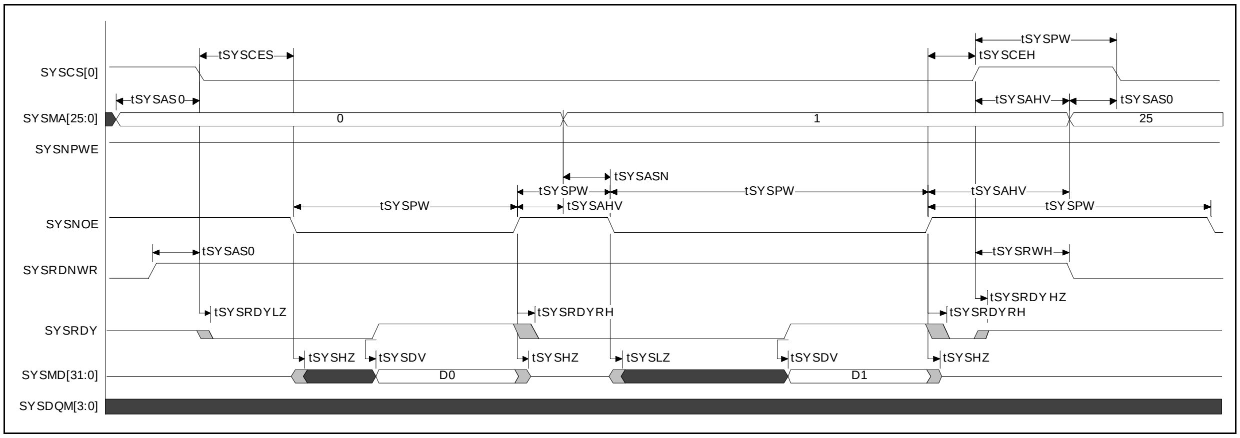


Figure 5-3. SRAM Write Timing (see Table 5-4)

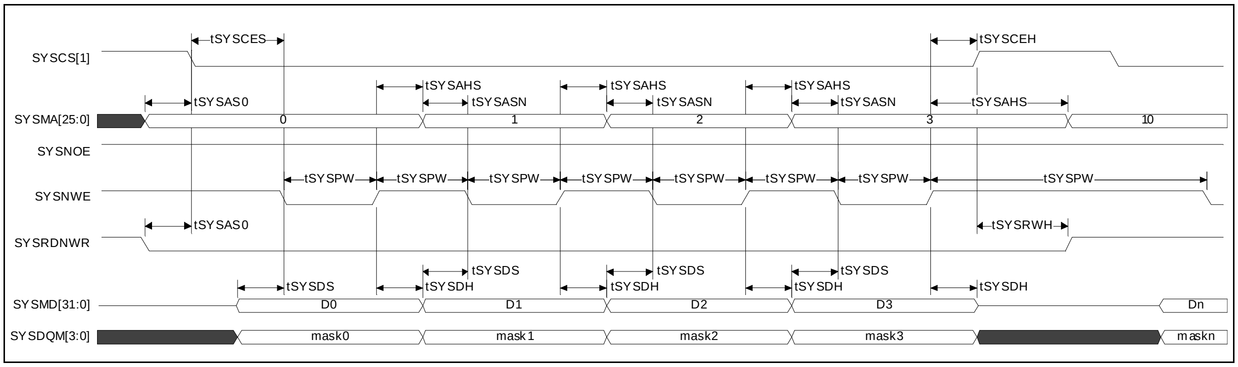


Table 5-4. General System Bus Timing

Name	Description	Min	Max	Units
tSYSCLK[1]	2700G7 Multimedia Accelerator clock period	7.5	—	ns
tSYSAS0	SYS_MA and SYS_RDnWR setup to SYS_nCS0 or SYS_nCS1 active	0	—	ns
tSYSASN	SYS_MA setup to SYS_nPWE, SYS_nWE, or SYS_nOE asserted	0	—	ns
tSYSCES	SYS_nCS0 or SYS_nCS1 setup to SYS_nPWE, SYS_nWE, or SYS_nOE asserted	0	—	ns
tSYSCEH	SYS_nCS0 or SYS_nCS1 active to SYS_nPWE, SYS_nWE, or SYS_nOE asserted	0	—	ns
tSYSAHV	SYS_MA hold from SYS_nPWE, SYS_nWE, SYS_nOE, SYS_nCS0 de-asserted	4	—	ns
tSYSRWH	SYS_RDnWR hold from SYSCS0 or SYSCS1 de-asserted	5	—	ns
tSYSAHS	SYS_MA hold from SYS_nWE de-asserted	4	—	ns
tSYSRDYWH	SYS_RDY hold from SYS_nPWE de-asserted	2*tSYSCLK	4*tSYSCLK	ns
tSYSRDYRH	SYS_RDY hold from SYS_nOE de-asserted	0	2*tSYSCLK	ns
tSYSRDYHZ	SYS_nCS0 de-asserted to SYSRDY tri-state	0	10	ns
tSYSRDYLZ	SYS_nCS0 de-asserted to SYSRDY driven	0	10	ns
tSYSDS	SYS_MD and SYS_DQM setup to SYS_nPWE or SYS_nWE asserted	0	—	ns
tSYSDH	SYS_MD and SYS_DQM hold from SYS_nPWE or SYS_nWE de-asserted	4	—	ns
tSYSPW	SYS_nOE, SYS_nPWE, and SYS_nWE asserted or de-asserted time	tSYSCLK+7.5	—	ns
tSYSLZ	SYS_nOE asserted to SYS_MD driven	3	—	ns
tSYSHZ	SYS_nOE de-asserted to SYS_MD tri-state	3	—	ns
tSYSWRDY	SYS_nCS0 asserted to SYS_RDY asserted	2*tSYSCLK	3*tSYSCLK	ns
tSYSDV	SYS_RDY asserted to SYS_MD valid	0	—	ns
tRISE/tFALL	20/80 transition rise and fall time	—	1	ns

NOTES:

1. The 2700G7 Multimedia Accelerator internal system bus frequency. This is not measurable.

5.3.2 Local Memory SDRAM Interface Timing

The only Local Memory signals that are accessible outside of the 2700G7 Multimedia Accelerator Package are the LM_nCS and the SDRAM_nCS signals. The LM_nCs signal should be connected to the SDRAM_nCS signal via a short, direct trace on the main board.

The 55 LM_RSVD signals should be left as no connects.

5.3.3 LCD Input Interface Timing

Figure 4-5. LCD_IN Timing

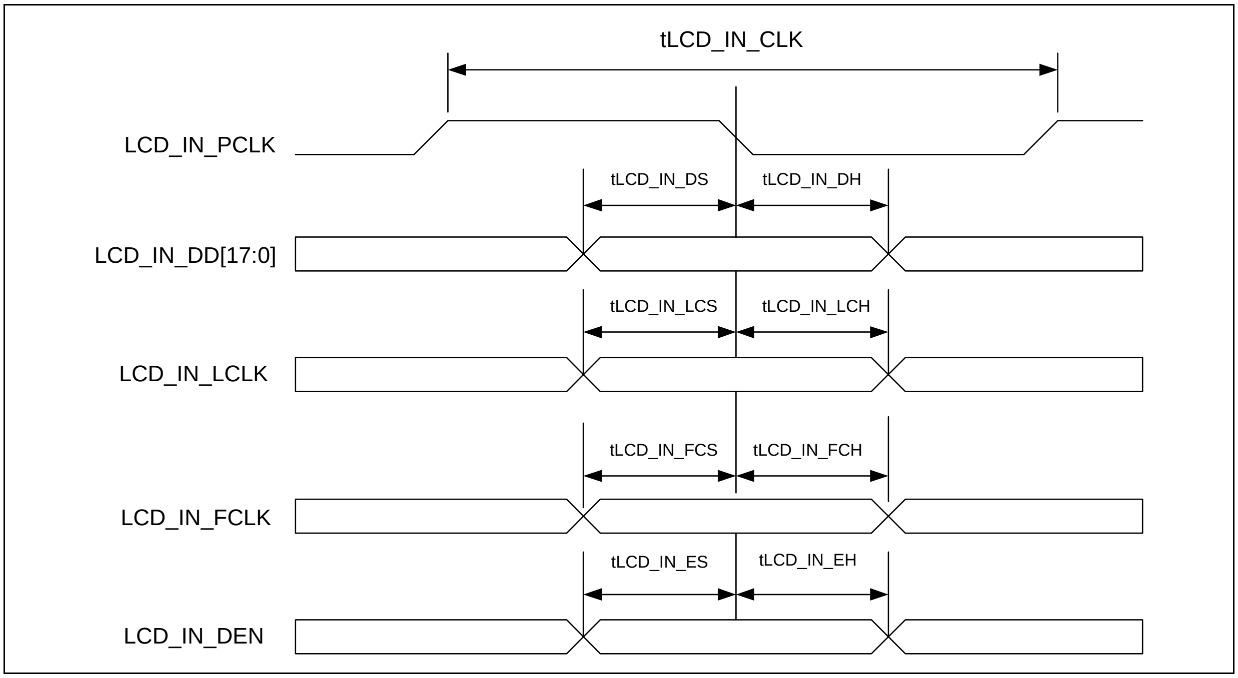


Table 4-5. LCD Input Interface Timing

Name	Description	Min	Max	Units
tLCD_IN_CLK	LCD_IN clock period.	21	—	ns
tLCD_IN_DS	LCD_IN data set up time	3	—	ns
tLCD_IN_DH	LCD_IN data hold time	3	—	ns
tLCD_IN_LCS	LCD_IN line clock set up time	3	—	ns
tLCD_IN_LCH	LCD_IN line clock hold time	3	—	ns
tLCD_IN_FCS	LCD_IN frame clock setup time	3	—	ns
tLCD_IN_FCH	LCD_IN frame clock hold time	3	—	ns
tLCD_IN_ES	LCD_IN data enable setup time	3	—	ns
tLCD_IN_EH	LCD_IN data enable hold time	3	—	ns

5.3.4 LCD1/LCD2 Interface Timing

LCD data outputs can be switched on either the rising or the falling edge of the associated PCLK. Note that this does not directly correspond to the clocking requirements at the receiver side. If the receiver (e.g., LCD) latches incoming data on the rising edge of PCLK, the 2700G7 Multimedia Accelerator should be programmed to switch its LCD data outputs on the falling edge of PCLK. This allows the data to be centered (with proper setup and hold times) with respect to PCLK.

Note: Figure 5-4 shows timings for LCD data transfers using both the rising and the falling edge of the PCLK. In a system implementation, data will switch either on PCLK rising or PCLK falling edges (but not both).

Figure 5-4. LCD1/LCD2 Timing

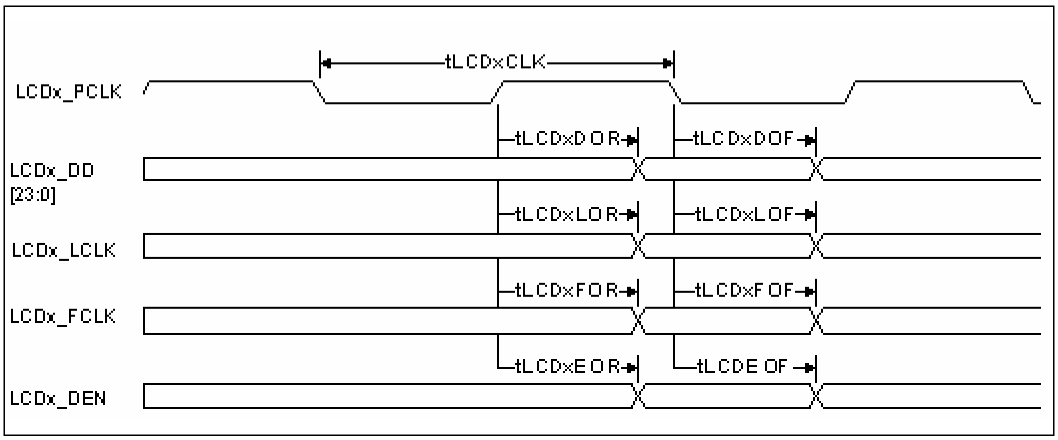


Table 4-6. LCD1/2 Interface Timing

Symbol	Parameter	Min	Max	Units
tLCDxCLK	LCD interface clock period.	7.5	—	ns
tLCDxDOR	Data out valid time, driven from rising edge PCLK	0	3	ns
tLCDxLOR	Line clock valid time, driven from rising edge PCLK	0	3	ns
tLCDxFOR	Frame clock valid time, driven from rising edge PCLK	0	3	ns
tLCDxEOR	Data enable valid time, driven from rising edge PCLK	0	3	ns
tLCDxDOF	Data out valid time, driven from falling edge PCLK	0	3	ns
tLCDxLOF	Line clock valid time, driven from falling edge PCLK	0	3	ns
tLCDxFOF	Frame clock valid time, driven from falling edge PCLK	0	3	ns
tLCDEOF	Data enable valid time, driven from falling edge PCLK	0	3	ns
tRISE/tFALL	20/80 transition rise and fall time	—	1	ns

5.3.5 PWM Interface Timing

Figure 5-5. PWM Timing

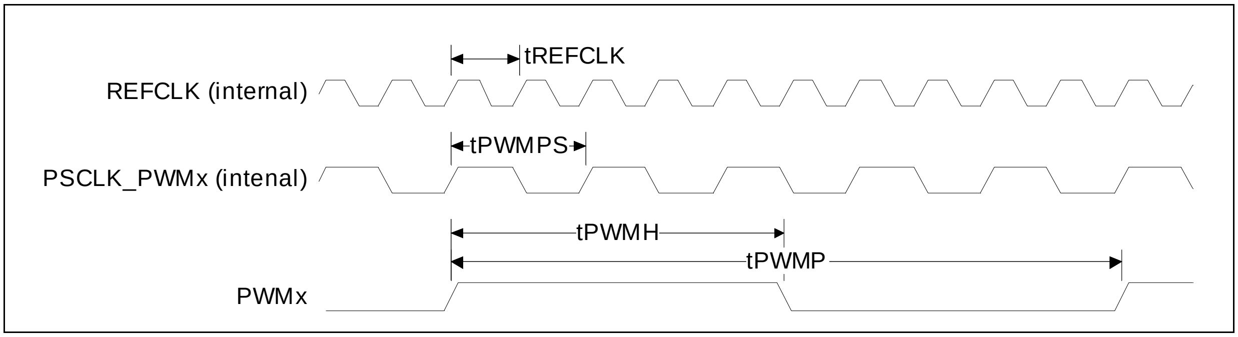


Table 5-5. PWM Interface Timing

Name	Description	Min	Max	Units
tREFCLK	REFCLK frequency. In normal operation REFCLK is 13 MHz.	7.5	77	ns
tPWMPS	tPWMPS = tREFCLK * (PWMCRx_PRESCALE + 1)	1	64	REFCLK Cycles
tPWMH	tPWMH = tPWMPS * PWMDCRx_DCYCLE	1	1023	PSCLK_PWMx Cycles
tPWMP	tPWMP = tPWMP * PWMPCRx_PV	2	1023	PSCLK_PWMx Cycles
tRISE/tFALL	20/80 transition rise and fall time	—	1	ns

5.3.6 JTAG Timing

Figure 5-6. JTAG Interface Timing

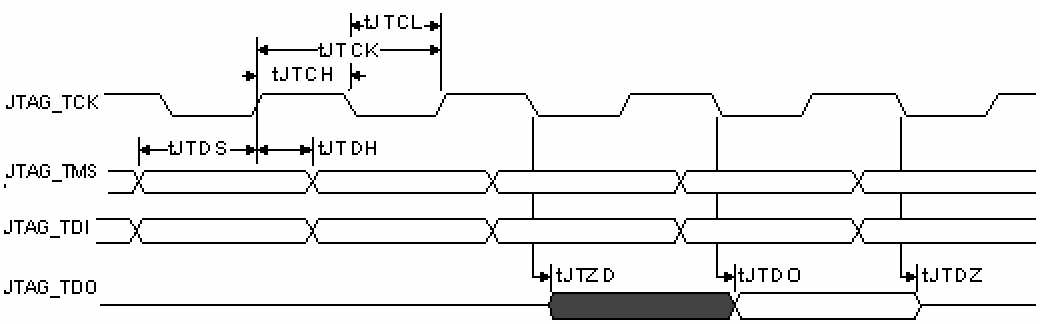


Table 4-8. JTAG Interface Timing

Name	Description	Min	Max	Units
tJTCK	JTAG Clock period	75	—	ns
tJTCH	JTAG Clock high time	33	—	ns
tJTCL	JTAG Clock low time	33	—	ns
tJTDS	JTAG Data In setup time	10	—	ns
tJTDH	JTAG Data In hold time	10	—	ns
tJTZD	JTAG Data Out tri-state to data valid time	—	10	ns
tJTD0	JTAG Data Out clock to data valid time	2	10	ns
tJTDZ	JTAG Data Out data valid to tri-state time	—	10	ns
tRISE/tFALL	20/80 transition rise and fall time	—	1	ns

Figure 5-7. JTAG Reset Timing

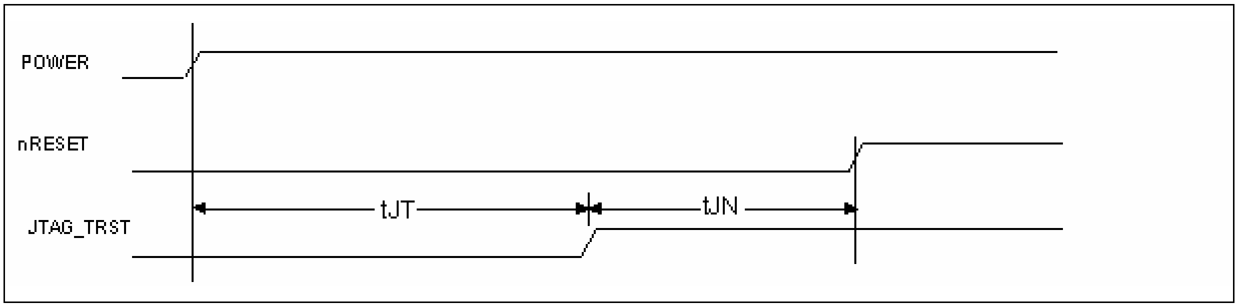


Table 5-6. JTAG Reset Timing

Name	Parameter	Min	Max	Units
tJT	Minimum Pulse Width of JTAG_RST	5	—	ns
tJN	JTAG de-assertion to nRESET de-assertion	5	—	ns
tRISE/tFALL	20/80 transition rise and fall time	—	1	ns

5.3.7 Reset Timings

Figure 5-8. nRESET_IN Timing for XTAL OSC REFCLK Source

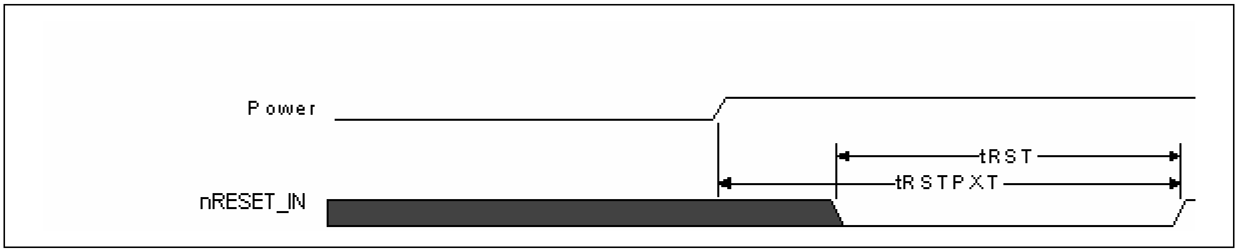


Table 5-7. nRESET_IN Timing for the XTAL OSC REFCLK Source

Symbol	Parameter	Min	Max	Units
tRSTPXT	All power rails valid to nRESET_IN de-assertion	100	—	ms
tRST	nRESET_IN active period	256	—	REFCLK cycles
tST	Start-up time	100	—	ms

Figure 5-9. nRESET_IN Timing for CLKIN REFCLK Source

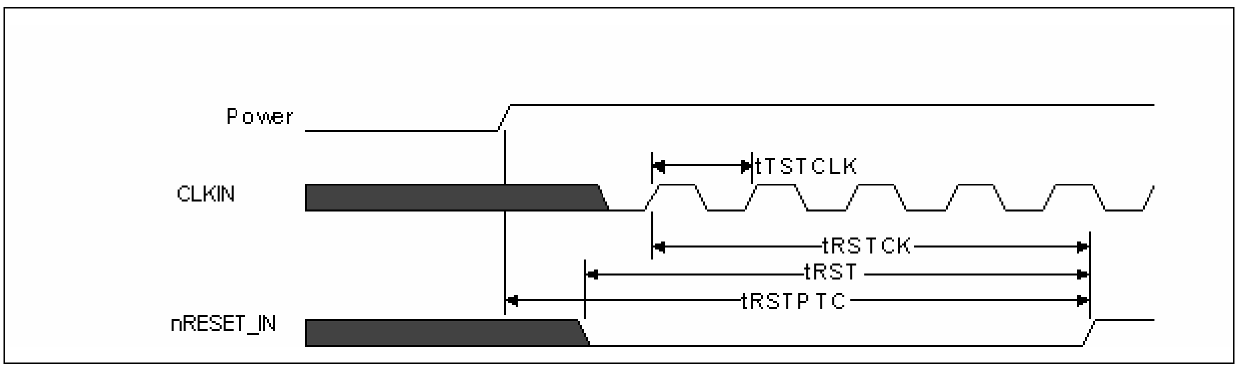


Table 5-8. nRESET_IN Timing for CLKIN REFCLK Source

Symbol	Parameter	Min	Max	Units
tRSTTCK	nRESET_IN active after stable CLKIN	256	—	REFCLK cycles
tRSTPTC	All power rails valid to nRESET_IN de-assertion	256	—	REFCLK cycles
tRST	nRESET_IN active period	256	—	REFCLK cycles
tTSTCLK	Test Clock Timing	77	—	ns

6 Ballout and Package

This chapter provides the ballout and package information for the 2700G7 Multimedia Accelerator.

6.1 Ballout Information

Table 6-1 provides a signal count summary.

Table 6-1. Signal Count Summary

Signal Name	# of Signals
Total I/O	221
NC	2
VCC_CORE	28
VCC_SYS	9
VCC_LM	10
VCC_SDRAM	13
VCC_LCD_IN	2
VCC_LCD1	4
VCC_LCD2	4
VCC_IO	15
GND	50
VCCA_CORE_PLL	1
VSSA_CORE_PLL	1
VCCA_DISP_PLL	1
VSSA_DISP_PLL	1
VAA_XTAL	1
VSSA_XTAL	1
Total	**364**

Figure 6-1 and Figure 6-2 show the 2700G7 Multimedia Accelerator ballout footprint viewed from the top of the package. Table 6-2 provides the ballout listed alphabetically by signal name and Table 6-3 provides the ballout listed sequentially by ball number.

Figure 6-1. Intel® 2700G7 Multimedia Accelerator Ballout (Top View, Left Side)

	1	2	3	4	5	6	7	8	9	10
A	GND	SYS_ MA18	SYS_ MA22	SYS_MA24	LCD_IN_DEN	LCD_IN_FCLK	LCD_IN_DD1	LCD_IN_DD3	LCD_IN_DD7	LCD_IN_DD11
B	SYS_MA11	SYS_ MA12	SYS_ MA17	SYS_MA23	SYS_MA25	LCD_IN_LCLK	LCD_IN_PCLK	LCD_IN_DD5	LCD_IN_DD9	LCD_IN_DD13
C	SYS_MA7	SYS_ MA9	SYS_ MA13	SYS_MA14	SYS_MA16	SYS_MA20	LCD_IN_DD2	LCD_IN_DD0	LCD_IN_DD4	LCD_IN_DD8
D	SYS_MA4	SYS_ MA5	SYS_ MA10	SYS_MA15	SYS_MA19	SYS_MA21	VCC_IO	LCD_IN_DD6	LCD_IN_DD10	VCC_IO
E	SYS_MA2	SYS_ MA3	SYS_ MA8	VCC_SYS	VCC_CORE	VCC_CORE	VCC_CORE	VCC_CORE	VCC_CORE	GND
F	SYS_MD30	SYS_ MD31	SYS_ MA6	VCC_IO	VCC_IO					
G	SYS_MD27	SYS_ MD28	SYS_ MD29	VCC_SYS	GND		VCC_CORE	VCC_CORE	GND	GND
H	SYS_MD23	SYS_ MD24	SYS_ MD26	SYS_MD25	VCC_SYS		VCC_CORE	VCC_CORE	GND	GND
J	SYS_MD19	SYS_ MD20	SYS_ MD22	SYS_MD21	VCC_SYS		VCC_CORE	VCC_CORE	GND	GND
K	SYS_MD15	SYS_ MD16	SYS_ MD18	SYS_MD17	VCC_SYS		GND	GND	GND	GND
L	SYS_MD14	SYS_ MD13	SYS_ MD10	VCC_SYS	VCC_SYS		GND	GND	GND	GND
M	SYS_MD12	SYS_ MD11	SYS_ MD7	SYS_MD9	VCC_SYS		GND	GND	GND	GND
N	SYS_MD8	SYS_ MD6	SYS_ MD3	VCC_SYS	GND		VCC_CORE	VCC_CORE	VCC_CORE	GND
P	SYS_MD4	SYS_ MD2	SYS_ MD1	SYS_MD5	VCC_CORE		VCC_CORE	VCC_CORE	VCC_CORE	GND
R	SYS_MD0	SYS_ nCS1	SYS_ DQM1	SYS_nCS0	VCC_CORE					
T	SYS_DQM3	SYS_ DQM2	SYS_ nWE	SYS_nCAS	GND	VCC_ LM	VCC_ LM	GND	VCC_SDRAM	VCC_SDRAM
U	SYS_DQM0	SYS_ nOE	SYS_ RDY	VCC_IO	LM_RSVD	LM_RSVD	LM_RSVD	VCC_SDRAM	LM_RSVD	VCC_ LM
V	SYS_RDnWR	SYS_ nPWE	LM_RSVD	LM_RSVD	LM_RSVD	LM_RSVD	LM_RSVD	LM_RSVD	LM_RSVD	LM_RSVD
W	LM_RSVD	LM_RSVD	LM_RSVD	LM_RSVD	LM_RSVD	LM_RSVD	LM_RSVD	LM_RSVD	LM_RSVD	LM_RSVD
Y	GND	LM_RSVD	LM_RSVD	LM_RSVD	VCC_ LM	LM_RSVD	LM_RSVD	LM_RSVD	LM_RSVD	VCC_SDRAM
	1	2	3	4	5	6	7	8	9	10

Figure 6-2. Intel® 2700G7 Multimedia Accelerator Ballout (Top View, Right Side)

11	12	13	14	15	16	17	18	19	20	
VCC_ LCD_IN	LCD_IN _ DD16	GPIO1	LCD1_DD2	LCD1_DD4	LCD1_DD6	LCD1_DD8	LCD1_DD14	LCD1_DD16	NC	A
VCC_ LCD_IN	LCD_IN_ DD17	LCD1_ DD1	LCD1_DD3	LCD1_DD5	LCD1_DD7	LCD1_DD12	LCD1_DD17	LCD1_DD18	LCD1_DD23	B
LCD_IN_ DD12	GPIO0	LCD_IN_ DD15	LCD1_DD0	LCD1_DD9	LCD1_DD11	LCD1_DD15	LCD1_DD19	LCD1_DD20	LCD1_DEN	C
LCD_IN_ DD14	VCC_ LCD1	VCC_ CORE	VCC_ IO	LCD1_DD10	LCD1_DD13	LCD1_DD21	LCD1_PWM	LCD1_LCLK	LCD1_FCLK	D
GND	VCC_ LCD1	VCC_ CORE	VCC_ IO	VCC_ CORE	VCC_ LCD1	LCD1_DD22	LCD2_DD0	LCD1_PCLK	LCD2_DD1	E
					VCC_ LCD1	VCC_ IO	LCD2_DD2	LCD2_DD3	LCD2_DD4	F
GND	VCC_ CORE	VCC_ CORE	VCC_ CORE		GND	LCD2_DD8	LCD2_DD6	LCD2_DD5	LCD2_DD7	G
GND	VCC_ CORE	VCC_ CORE	VCC_ CORE		GND	VCC_ IO	LCD2_DD10	LCD2_DD9	LCD2_DD11	H
GND	GND	GND	GND		VCC_ LCD2	LCD2_DD16	LCD2_DD13	LCD2_DD12	LCD2_DD14	J
GND	GND	GND	GND		VCC_ LCD2	LCD2_DD17	LCD2_DD18	LCD2_DD15	VCC_ LCD2	K
GND	GND	GND	GND		VCC_ LCD2	LCD2_DD21	LCD2_DD19	LCD2_DD22	LCD2_DD20	L
GND	VCC_SDRAM	VCC_SDRAM	VCC_SDRAM		GND	VCC_ IO	LCD2_DEN	LCD2_PWM	LCD2_DD23	M
GND	VCC_SDRAM	VCC_SDRAM	VCC_SDRAM		VCC_ IO	LCD2_LCLK	LCD2_PCLK	nRESET _IN	LCD2_FCLK	N
GND	VCC_SDRAM	VCC_SDRAM	VCC_SDRAM		VCC_ IO	nINT	VAA_ XTAL	RSVD	POLL_FLAG	P
					GND	VCC_ IO	VSSA_XTAL	XTAL_ IN	XTAL_OUT	R
VCC_ LM	VCC_ LM	GND	VCC_ LM	VCC_ LM	VCC_ LM	VCCA_ CORE_PLL	JTAG_TMS	CLKIN	JTAG_TCK	T
VCC_ IO	RSVD	SDRAM_nCS	VCC_ IO	LM_RSVD	LM_RSVD	LM_RSVD	VSSA_ CORE_PLL	JTAG_TDO	JTAG_ nTRST	U
LM_RSVD	LM_ nCS	LM_RSVD	LM_RSVD	LM_RSVD	LM_RSVD	LM_RSVD	VSSA_ DISP_ PLL	VCCA_ DISP_ PLL	JTAG_TDI	V
LM_RSVD	RSVD	LM_RSVD	LM_RSVD	LM_RSVD	LM_RSVD	LM_RSVD	LM_RSVD	LM_RSVD	LM_RSVD	W
LM_RSVD	LM_RSVD	LM_RSVD	LM_RSVD	VCC_ LM	LM_RSVD	LM_RSVD	LM_RSVD	LM_RSVD	NC	Y
11	12	13	14	15	16	17	18	19	20	

Table 6-2. Intel® 2700G7 Multimedia Accelerator Ballout by Signal Name

Signal Name	Ball #	Signal Name	Ball #	Signal Name	Ball #
CLKIN	T19	GND	M7	LCD_IN_DD12	C11
GND	A1	GND	M8	LCD_IN_DD13	B10
GND	E10	GND	M9	LCD_IN_DD14	D11
GND	E11	GND	M10	LCD_IN_DD15	C13
GND	G5	GND	M11	LCD_IN_DD16	A12
GND	G9	GND	M16	LCD_IN_DD17	B12
GND	G10	GND	N5	LCD_IN_DEN	A5
GND	G11	GND	N10	LCD_IN_FCLK	A6
GND	G16	GND	N11	LCD_IN_LCLK	B6
GND	H9	GND	P10	LCD_IN_PCLK	B7
GND	H10	GND	P11	LCD1_DD0	C14
GND	H11	GND	R16	LCD1_DD1	B13
GND	H16	GND	T5	LCD1_DD2	A14
GND	J9	GND	T8	LCD1_DD3	B14
GND	J10	GND	T13	LCD1_DD4	A15
GND	J11	GND	Y1	LCD1_DD5	B15
GND	J12	GPIO0	C12	LCD1_DD6	A16
GND	J13	GPIO1	A13	LCD1_DD7	B16
GND	J14	JTAG_TCK	T20	LCD1_DD8	A17
GND	K7	JTAG_TDI	V20	LCD1_DD9	C15
GND	K8	JTAG_TDO	U19	LCD1_DD10	D15
GND	K9	JTAG_TMS	T18	LCD1_DD11	C16
GND	K10	JTAG_nTRST	U20	LCD1_DD12	B17
GND	K11	LCD_IN_DD0	C8	LCD1_DD13	D16
GND	K12	LCD_IN_DD1	A7	LCD1_DD14	A18
GND	K13	LCD_IN_DD2	C7	LCD1_DD15	C17
GND	K14	LCD_IN_DD3	A8	LCD1_DD16	A19
GND	L7	LCD_IN_DD4	C9	LCD1_DD17	B18
GND	L8	LCD_IN_DD5	B8	LCD1_DD18	B19
GND	L9	LCD_IN_DD6	D8	LCD1_DD19	C18
GND	L10	LCD_IN_DD7	A9	LCD1_DD20	C19
GND	L11	LCD_IN_DD8	C10	LCD1_DD21	D17
GND	L12	LCD_IN_DD9	B9	LCD1_DD22	E17
GND	L13	LCD_IN_DD10	D9	LCD1_DD23	B20
GND	L14	LCD_IN_DD11	A10	LCD1_DEN	C20

Signal Name	Ball #
LCD1_FCLK	D20
LCD1_LCLK	D19
LCD1_PCLK	E19
LCD1_PWM	D18
LCD2_DD00	E18
LCD2_DD1	E20
LCD2_DD2	F18
LCD2_DD3	F19
LCD2_DD4	F20
LCD2_DD5	G19
LCD2_DD6	G18
LCD2_DD7	G20
LCD2_DD8	G17
LCD2_DD9	H19
LCD2_DD10	H18
LCD2_DD11	H20
LCD2_DD12	J19
LCD2_DD13	J18
LCD2_DD14	J20
LCD2_DD15	K19
LCD2_DD16	J17
LCD2_DD17	K17
LCD2_DD18	K18
LCD2_DD19	L18
LCD2_DD20	L20
LCD2_DD21	L17
LCD2_DD22	L19
LCD2_DD23	M20
LCD2_DEN	M18
LCD2_FCLK	N20
LCD2_LCLK	N17
LCD2_PCLK	N18
LCD2_PWM	M19
LM_nCS	V12
LM_RSVD	U5

Signal Name	Ball #
LM_RSVD	U6
LM_RSVD	U7
LM_RSVD	U9
LM_RSVD	U15
LM_RSVD	U16
LM_RSVD	U17
LM_RSVD	V3
LM_RSVD	V4
LM_RSVD	V5
LM_RSVD	V6
LM_RSVD	V7
LM_RSVD	V8
LM_RSVD	V9
LM_RSVD	V10
LM_RSVD	V11
LM_RSVD	V13
LM_RSVD	V14
LM_RSVD	V15
LM_RSVD	V16
LM_RSVD	V17
LM_RSVD	W1
LM_RSVD	W2
LM_RSVD	W3
LM_RSVD	W4
LM_RSVD	W5
LM_RSVD	W6
LM_RSVD	W7
LM_RSVD	W8
LM_RSVD	W9
LM_RSVD	W10
LM_RSVD	W11
LM_RSVD	W13
LM_RSVD	W14
LM_RSVD	W15
LM_RSVD	W16

Signal Name	Ball #
LM_RSVD	W17
LM_RSVD	W18
LM_RSVD	W19
LM_RSVD	W20
LM_RSVD	Y2
LM_RSVD	Y3
LM_RSVD	Y4
LM_RSVD	Y6
LM_RSVD	Y7
LM_RSVD	Y8
LM_RSVD	Y9
LM_RSVD	Y11
LM_RSVD	Y12
LM_RSVD	Y13
LM_RSVD	Y14
LM_RSVD	Y16
LM_RSVD	Y17
LM_RSVD	Y18
LM_RSVD	Y19
NC	A20
NC	Y20
nINT	P17
nRESET_IN	N19
POLL_FLAG	P20
RSVD	P19
RSVD	U12
RSVD	W12
SDRAM_nCS	U13
SYS_DQM0	U1
SYS_DQM1	R3
SYS_DQM2	T2
SYS_DQM3	T1
SYS_MA2	E1
SYS_MA3	E2
SYS_MA4	D1

Signal Name	Ball #
SYS_MA5	D2
SYS_MA6	F3
SYS_MA7	C1
SYS_MA8	E3
SYS_MA9	C2
SYS_MA10	D3
SYS_MA11	B1
SYS_MA12	B2
SYS_MA13	C3
SYS_MA14	C4
SYS_MA15	D4
SYS_MA16	C5
SYS_MA17	B3
SYS_MA18	A2
SYS_MA19	D5
SYS_MA20	C6
SYS_MA21	D6
SYS_MA22	A3
SYS_MA23	B4
SYS_MA24	A4
SYS_MA25	B5
SYS_MD0	R1
SYS_MD1	P3
SYS_MD2	P2
SYS_MD3	N3
SYS_MD4	P1
SYS_MD5	P4
SYS_MD6	N2
SYS_MD7	M3
SYS_MD8	N1
SYS_MD9	M4
SYS_MD10	L3
SYS_MD11	M2
SYS_MD12	M1
SYS_MD13	L2

Signal Name	Ball #
SYS_MD14	L1
SYS_MD15	K1
SYS_MD16	K2
SYS_MD17	K4
SYS_MD18	K3
SYS_MD19	J1
SYS_MD20	J2
SYS_MD21	J4
SYS_MD22	J3
SYS_MD23	H1
SYS_MD24	H2
SYS_MD25	H4
SYS_MD26	H3
SYS_MD27	G1
SYS_MD28	G2
SYS_MD29	G3
SYS_MD30	F1
SYS_MD31	F2
SYS_nCAS	T4
SYS_nCS0	R4
SYS_nCS1	R2
SYS_nOE	U2
SYS_nPWE	V2
SYS_nWE	T3
SYS_RDnWR	V1
SYS_RDY	U3
VAA_XTAL	P18
VCC_CORE	D13
VCC_CORE	E5
VCC_CORE	E6
VCC_CORE	E7
VCC_CORE	E8
VCC_CORE	E9
VCC_CORE	E13
VCC_CORE	E15

Signal Name	Ball #
VCC_CORE	G7
VCC_CORE	G8
VCC_CORE	G12
VCC_CORE	G13
VCC_CORE	G14
VCC_CORE	H7
VCC_CORE	H8
VCC_CORE	H12
VCC_CORE	H13
VCC_CORE	H14
VCC_CORE	J7
VCC_CORE	J8
VCC_CORE	N7
VCC_CORE	N8
VCC_CORE	N9
VCC_CORE	P5
VCC_CORE	P7
VCC_CORE	P8
VCC_CORE	P9
VCC_CORE	R5
VCC_IO	D7
VCC_IO	D10
VCC_IO	D14
VCC_IO	E14
VCC_IO	F4
VCC_IO	F5
VCC_IO	F17
VCC_IO	H17
VCC_IO	M17
VCC_IO	N16
VCC_IO	P16
VCC_IO	R17
VCC_IO	U4
VCC_IO	U11
VCC_IO	U14

Signal Name	Ball #
VCC_LCD_IN	A11
VCC_LCD_IN	B11
VCC_LCD1	D12
VCC_LCD1	E12
VCC_LCD1	E16
VCC_LCD1	F16
VCC_LCD2	K20
VCC_LCD2	L16
VCC_LCD2	J16
VCC_LCD2	K16
VCC_LM	T6
VCC_LM	T7
VCC_LM	T11
VCC_LM	T12
VCC_LM	T14
VCC_LM	T15
VCC_LM	T16

Signal Name	Ball #
VCC_LM	U10
VCC_LM	Y5
VCC_LM	Y15
VCC_SDRAM	M12
VCC_SDRAM	M13
VCC_SDRAM	M14
VCC_SDRAM	N12
VCC_SDRAM	N13
VCC_SDRAM	N14
VCC_SDRAM	P12
VCC_SDRAM	P13
VCC_SDRAM	P14
VCC_SDRAM	T9
VCC_SDRAM	T10
VCC_SDRAM	U8
VCC_SDRAM	Y10
VCC_SYS	E4

Signal Name	Ball #
VCC_SYS	G4
VCC_SYS	H5
VCC_SYS	J5
VCC_SYS	K5
VCC_SYS	L4
VCC_SYS	L5
VCC_SYS	M5
VCC_SYS	N4
VCCA_CORE_PLL	T17
VCCA_DISP_PLL	V19
VSSA_CORE_PLL	U18
VSSA_DISP_PLL	V18
VSSA_XTAL	R18
XTAL_IN	R19
XTAL_OUT	R20

Table 6-3. Intel® 2700G7 Multimedia Accelerator Ballout by Ball Number

Ball #	Signal Name	Ball #	Signal Name	Ball #	Signal Name
A1	GND	B15	LCD1_DD5	D9	LCD_IN_DD0
A2	SYS_MA18	B16	LCD1_DD7	D10	VCC_IO
A3	SYS_MA22	B17	LCD1_DD12	D11	LCD_IN_DD14
A4	SYS_MA24	B18	LCD1_DD17	D12	VCC_LCD1
A5	LCD_IN_DEN	B19	LCD1_DD18	D13	VCC_CORE
A6	LCD_IN_FCLK	B20	LCD1_DD23	D14	VCC_IO
A7	LCD_IN_DD1	C1	SYS_MA7	D15	LCD1_DD10
A8	LCD_IN_DD3	C2	SYS_MA9	D16	LCD1_DD13
A9	LCD_IN_DD7	C3	SYS_MA13	D17	LCD1_DD21
A10	LCD_IN_DD11	C4	SYS_MA14	D18	LCD1_PWM
A11	VCC_LCD_IN	C5	SYS_MA16	D19	LCD1_LCLK
A12	LCD_IN_DD16	C6	SYS_MA20	D20	LCD1_FCLK
A13	GPIO1	C7	LCD_IN_DD2	E1	SYS_MA2
A14	LCD1_DD2	C8	LCD_IN_DD0	E2	SYS_MA3
A15	LCD1_DD4	C9	LCD_IN_DD4	E3	SYS_MA8
A16	LCD1_DD6	C10	LCD_IN_DD8	E4	VCC_SYS
A17	LCD1_DD8	C11	LCD_IN_DD12	E5	VCC_CORE
A18	LCD1_DD14	C12	GPIO0	E6	VCC_CORE
A19	LCD1_DD16	C13	LCD_IN_DD15	E7	VCC_CORE
A20	NC	C14	LCD1_DD0	E8	VCC_CORE
B1	SYS_MA11	C15	LCD1_DD9	E9	VCC_CORE
B2	SYS_MA12	C16	LCD1_DD11	E10	GND
B3	SYS_MA17	C17	LCD1_DD15	E11	GND
B4	SYS_MA23	C18	LCD1_DD19	E12	VCC_LCD1
B5	SYS_MA25	C19	LCD1_DD20	E13	VCC_CORE
B6	LCD_IN_LCLK	C20	LCD1_DEN	E14	VCC_IO
B7	LCD_IN_PCLK	D1	SYS_MA4	E15	VCC_CORE
B8	LCD_IN_DD5	D2	SYS_MA5	E16	VCC_LCD1
B9	LCD_IN_DD9	D3	SYS_MA10	E17	LCD1_DD22
B10	LCD_IN_DD13	D4	SYS_MA15	E18	LCD2_DD0
B11	VCC_LCD_IN	D5	SYS_MA19	E19	LCD1_PCLK
B12	LCD_IN_DD17	D6	SYS_MA21	E20	LCD2_DD1
B13	LCD1_DD1	D7	VCC_IO	F1	SYS_MD30
B14	LCD1_DD3	D8	LCD_IN_DD6	F2	SYS_MD31

Ball #	Signal Name
F3	SYS_MA6
F4	VCC_IO
F5	VCC_IO
F16	VCC_LCD1
F17	VCC_IO
F18	LCD2_DD2
F19	LCD2_DD3
F20	LCD2_DD4
G1	SYS_MD27
G2	SYS_MD28
G3	SYS_MD29
G4	VCC_SYS
G5	GND
G7	VCC_CORE
G8	VCC_CORE
G9	GND
G10	GND
G11	GND
G12	VCC_CORE
G13	VCC_CORE
G14	VCC_CORE
G16	GND
G17	LCD2_DD8
G18	LCD2_DD6
G19	LCD2_DD5
G20	LCD2_DD7
H1	SYS_MD23
H2	SYS_MD24
H3	SYS_MD26
H4	SYS_MD25
H5	VCC_SYS
H7	VCC_CORE
H8	VCC_CORE
H9	GND
H10	GND

Ball #	Signal Name
H11	GND
H12	VCC_CORE
H13	VCC_CORE
H14	VCC_CORE
H16	GND
H17	VCC_IO
H18	LCD2_DD10
H19	LCD2_DD9
H20	LCD2_DD11
J1	SYS_MD19
J2	SYS_MD20
J3	SYS_MD22
J4	SYS_MD21
J5	VCC_SYS
J7	VCC_CORE
J8	VCC_CORE
J9	GND
J10	GND
J11	GND
J12	GND
J13	GND
J14	GND
J16	VCC_LCD2
J17	LCD2_DD16
J18	LCD2_DD13
J19	LCD2_DD12
J20	LCD2_DD14
K1	SYS_MD15
K2	SYS_MD16
K3	SYS_MD18
K4	SYS_MD17
K5	VCC_SYS
K7	GND
K8	GND
K9	GND

Ball #	Signal Name
K10	GND
K11	GND
K12	GND
K13	GND
K14	GND
K16	VCC_LCD2
K17	LCD2_DD17
K18	LCD2_DD18
K19	LCD2_DD15
K20	VCC_LCD2
L1	SYS_MD14
L2	SYS_MD13
L3	SYS_MD10
L4	VCC_SYS
L5	VCC_SYS
L7	GND
L8	GND
L9	GND
L10	GND
L11	GND
L12	GND
L13	GND
L14	GND
L16	VCC_LCD2
L17	LCD2_DD21
L18	LCD2_DD19
L19	LCD2_DD22
L20	LCD2_DD20
M1	SYS_MD12
M2	SYS_MD11
M3	SYS_MD7
M4	SYS_MD9
M5	VCC_SYS
M7	GND
M8	GND

Ball #	Signal Name
M9	GND
M10	GND
M11	GND
M12	VCC_SDRAM
M13	VCC_SDRAM
M14	VCC_SDRAM
M16	GND
M17	VCC_IO
M18	LCD2_DEN
M19	LCD2_PWM
M20	LCD2_DD23
N1	SYS_MD8
N2	SYS_MD6
N3	SYS_MD3
N4	VCC_SYS
N5	GND
N7	VCC_CORE
N8	VCC_CORE
N9	VCC_CORE
N10	GND
N11	GND
N12	VCC_SDRAM
N13	VCC_SDRAM
N14	VCC_SDRAM
N16	VCC_IO
N17	LCD2_LCLK
N18	LCD2_PCLK
N19	nRESET_IN
N20	LCD2_FCLK
P1	SYS_MD4
P2	SYS_MD2
P3	SYS_MD1
P4	SYS_MD5
P5	VCC_CORE
P7	VCC_CORE
P8	VCC_CORE
P9	VCC_CORE
P10	GND
P11	GND
P12	VCC_SDRAM
P13	VCC_SDRAM
P14	VCC_SDRAM
P16	VCC_IO
P17	nINT
P18	VAA_XTAL
P19	RSVD
P20	POLL_FLAG
R1	SYS_MD0
R2	SYS_nCS1
R3	SYS_DQM1
R4	SYS_nCS0
R5	VCC_CORE
R16	GND
R17	VCC_IO
R18	VSSA_XTAL
R19	XTAL_IN
R20	XTAL_OUT
T1	SYS_DQM3
T2	SYS_DQM2
T3	SYS_nWE
T4	SYS_nCAS
T5	GND
T6	VCC_LM
T7	VCC_LM
T8	GND
T9	VCC_SDRAM
T10	VCC_SDRAM
T11	VCC_LM
T12	VCC_LM
T13	GND
T14	VCC_LM
T15	VCC_LM
T16	GND
T17	VCCA_CORE_PL L
T18	JTAG_TMS
T19	CLKIN
T20	JTAG_TCK
U1	SYS_DQM0
U2	SYS_nOE
U3	SYS_RDY
U4	VCC_IO
U5	LM_RSVD
U6	LM_RSVD
U7	LM_RSVD
U8	VCC_SDRAM
U9	LM_RSVD
U10	VCC_LM
U11	VCC_IO
U12	RSVD
U13	SDRAM_nCS
U14	VCC_IO
U15	LM_RSVD
U16	LM_RSVD
U17	LM_RSVD
U18	VSSA_CORE_PLL
U19	JTAG_TDO
U20	JTAG_nTRST
V1	SYS_RDnWR
V2	SYS_nPWE
V3	LM_RSVD
V4	LM_RSVD
V5	LM_RSVD
V6	LM_RSVD
V7	LM_RSVD

Ball #	Signal Name
V8	LM_RSVD
V9	LM_RSVD
V10	LM_RSVD
V11	LM_RSVD
V12	LM_nCS
V13	LM_RSVD
V14	LM_RSVD
V15	LM_RSVD
V16	LM_RSVD
V17	LM_RSVD
V18	VSSA_DISP_PLL
V19	VCCA_DISP_PLL
V20	JTAG_TDI
W1	LM_RSVD
W2	LM_RSVD
W3	LM_RSVD
W4	LM_RSVD
W5	LM_RSVD

Ball #	Signal Name
W6	LM_RSVD
W7	LM_RSVD
W8	LM_RSVD
W9	LM_RSVD
W10	LM_RSVD
W11	LM_RSVD
W12	RSVD
W13	LM_RSVD
W14	LM_RSVD
W15	LM_RSVD
W16	LM_RSVD
W17	LM_RSVD
W18	LM_RSVD
W19	LM_RSVD
W20	LM_RSVD
Y1	GND
Y2	LM_RSVD
Y3	LM_RSVD

Ball #	Signal Name
Y4	LM_RSVD
Y5	VCC_LM
Y6	LM_RSVD
Y7	LM_RSVD
Y8	LM_RSVD
Y9	LM_RSVD
Y10	VCC_SDRAM
Y11	LM_RSVD
Y12	LM_RSVD
Y13	LM_RSVD
Y14	LM_RSVD
Y15	VCC_LM
Y16	LM_RSVD
Y17	LM_RSVD
Y18	LM_RSVD
Y19	LM_RSVD
Y20	NC

6.2 Package Information

The 2700G7 Multimedia Accelerator is packaged in a 14 mm x 14 mm BGA. The package has 364 balls spaced on a 0.65 mm ball grid (pitch) and a maximum Z height (above the PCB) of 1.52 mm. Figure 6-3 shows the package specifications. All dimensions and tolerances conform to ANSI Y14.5M – 1982. All dimensions, unless otherwise specified, are in millimeters.

Figure 6-3. Package Dimensions