HITACHI SEMICONDUCTOR TECHNICAL UPDATE

DATE	20th May, 1999	No.	TN-SH7-156 A/E
THEME	DMAC external request mode		
CLASSIFICATION	☐ Spec. change ☑ Supplement of Documents	☐ Limitation on Use	
PRODUCT NAME	HD6417750BP200, HD6417750F167, HD6417750VF128		
REFERENCE DOCUMENTS	SH7750 Hardware Manual, SH7750 Programming Manual	Effective Date From	

1. Conditions of detection of DREQ in external request mode

1.1 Contents

(1) Even when either DMAOR.DME or CHCR.DE is 0 and DMAOR.NMIF, DMAOR.AE and CHCR.TE are 0, the DMA transfer request with DREQ from external device is accepted and kept until DMA transfer starts or the DMA transfer request is canceled.
But DMA transfer doesn't start because of DMAOR.DME=0 or CHCR.DE=0. And DMA transfer starts after setting DMAOR.DME and CHCR.DE to 1.

(2) If DMA transfer is enabled (DMAOR.DME=1, CHCR.DE=1, CHCR.TE=0, DMAOR.NMIF=0, DMAOR.AE=0), DMA transfer starts when DREQ is input. (Hardware manual ver1.0 sec.14.3.2)

(3) During CHCR.TE=1, DMAOR.NMIF=1, DMAOR.AE=1, power on reset, manual reset, deep sleep mode, standby mode or module standby mode of DMAC, DREQ is ignored.

(4) Detected DREQ inputs are canceled by NMI (DMAOR.NMI=1), address error (DMAOR.AE=1), power-on reset or manual reset.

1.2 Usage Notes

As DREQ is detected at low level or falling edge, keep the DREQ pin high level if there is no DMA transfer request after reset.
At restarting DMA transfer, please note whether DMA transfer request is kept or not.