PowerVR M24VA

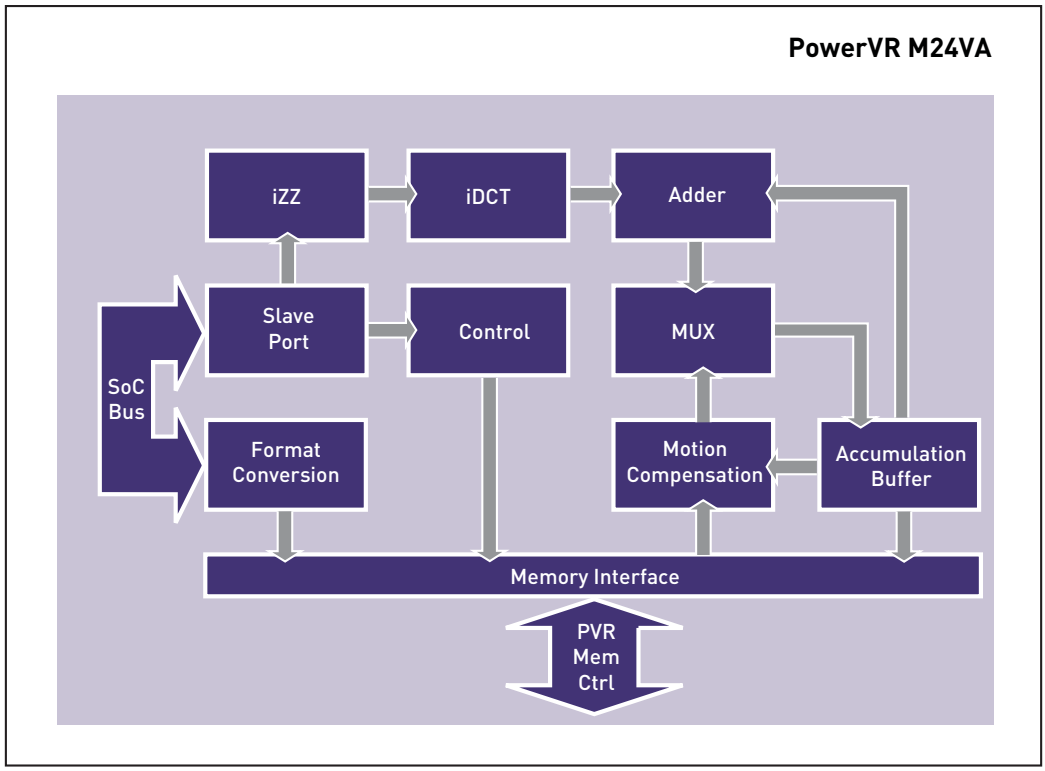
PowerVR M24VA is a multi-standard video decode accelerator developed as an IP core for use in a wide range of applications including mobile and handheld multimedia, internet appliances and in-car infotainment. M24VA accelerates the decode of MPEG-2, MPEG-4, WMV8 and WMV9 video streams, offloading inverse Zig-Zag, inverse Discret Cosine Transform (iDCT) and Motion Compensation, the most costly stages in video decoding, from the CPU.

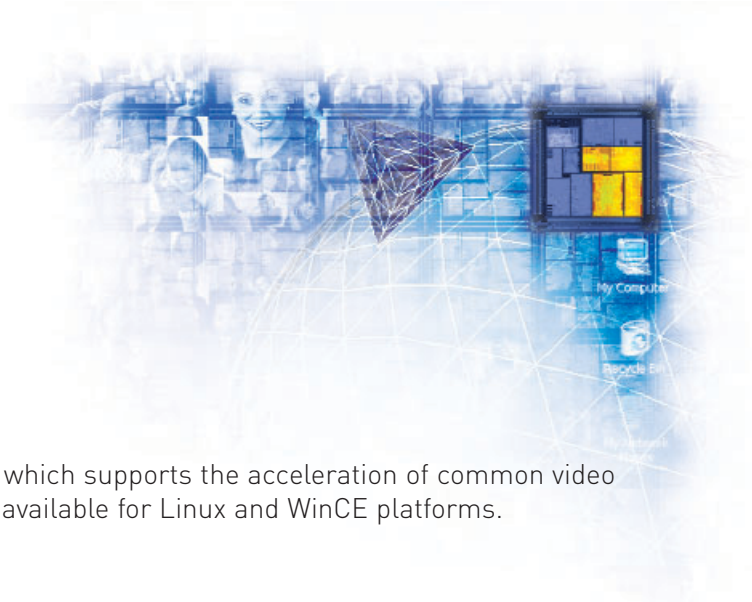
By performing the most CPU intensive parts of the video decode task from the CPU, M24VA reduces the CPU load required for decode by at least 40%, thereby allowing the system designer to target lower cost and lower power systems. The reduction in CPU computing requirements is of increased importance when performing quarter-pel motion compensation as used in modern video compression standards.

M24VA is also configurable to support colour space conversion from native YUV 4:2:0 video format to either RGB or YUV 4:2:2 formats. This colour space conversion runs concurrently with motion compensation enabling effective pipelining of the process for maximum efficiency.

M24VA Features

- MPEG-4 (ISO/IEC 14496-2) Simple Profile
- MPEG-4 (ISO/IEC 14496-2) Advanced Simple Profile (except GMC)
- MPEG-2 (ISO/IEC 13818-2) Main Profile
- WMV 9 simple profile
- iDCT for MPEG2 and MPEG4
- iDCT accuracy to ISO 14496-2
- Inverse Zig-Zag with programmable scan ordering
- Full bi-directional prediction
- Quarter-pel motion compensation
- Full support for unrestricted motion vectors
- 8x8, 8x4, 4x8 or 4x4 block size support
- Automated calculation of prediction address from vector
- Configurable image conversion to YUV 4:2:2 or 16/24-bit RGB
- Reduces CPU load by at least 40%
- Full scan circuitry





Software Support

M24VA is available with a video decode acceleration driver which supports the acceleration of common video codes through a single easy to use interface. The driver is available for Linux and WinCE platforms.

Configurability

The M24VA core is configurable at synthesis time to optimize the core for specific system requirements. Support can be added to motion compensation, for colour space conversion from YUV 4:2:0 to YUV 4:2:2 or RGB formats.

Power Requirements

Power requirements are optimized by sophisticated power management techniques using register-level clock gating to ensure the lowest active and standby power.

Performance

A full rate MPEG-2 MP@ML stream decode requires the core to run at less than 50 MHz.

Related System Solution IP

- Metagence META™ multi-threaded core offers an extremely efficient embedded DSP/RISC processing engine for modern multi-function consumer products.
- Ensigma UCC (Universal Communications Coprocessor) increases the level of integration of Imagination Technologies SoC solutions, requiring only a tuner to provide the complete decode solution for digital video broadcasting.
- PowerVR Pixel Display Pipeline (PDP) is a multi-layer display controller, designed to support modern layered user interfaces. Configurable for up to 6 planes with support for YUV and RGB, scaling is available on 2 planes, and the PDP has configurable alpha-blending and chroma key support.
- PowerVR graphics cores: MBX for best area/performance 3D graphics acceleration for handheld devices and mainstream set-top boxes. MBX Lite for entry level 3D graphics acceleration for mobile devices.
- PowerVR TVE is a digital TV encoder which outputs PAL or NTSC encoded composite video and simultaneous S-video, RGBS or YUV component video for TV display when connected to a pixel display pipeline such as PowerVR PDP.

M24VA Core Design Package

PowerVR M24VA is available as soft IP, and ships with

- Synthesis scripts
- Extensive verification test suite to ensure correct implementation of the design in a SoC
- Hardware implementation guide
- Programmer's reference manual

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PowerVR is a division of Imagination Technologies Ltd.