PowerVR MBX

The MBX graphics processor is an IP core specifically developed to meet the growing multimedia needs of low power, low cost system-on-chip (SoC) applications such as handheld gaming systems, in-car infotainment devices, handheld Internet appliances and entry-level set-top boxes. When used with embedded microprocessor cores, MBX enables the migration of complex 3D/2D graphics and video content to such platforms.

MBX has all the inherent benefits of the PowerVR architecture, including low memory bandwidth, exceptional performance, market leading image quality and low power demands. Other features include:

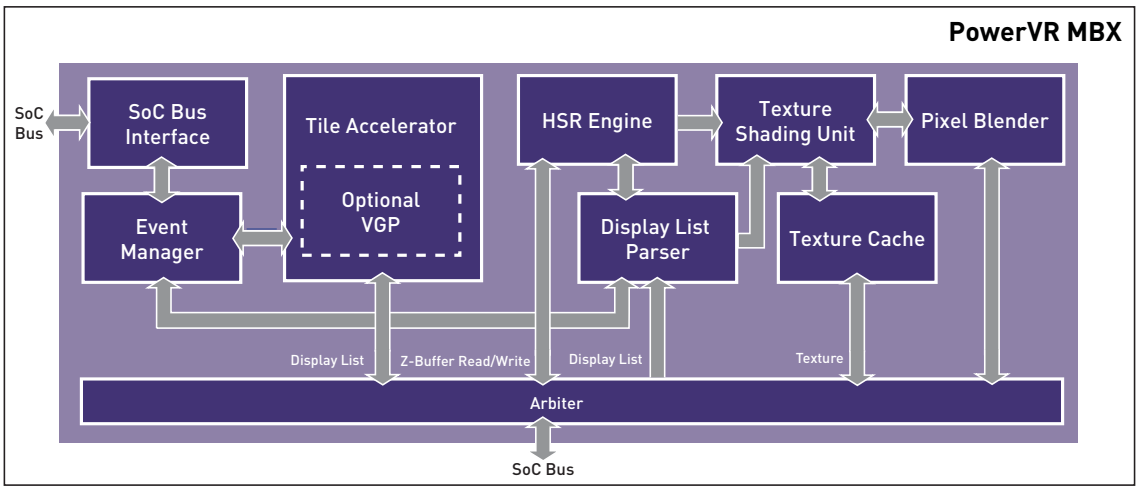
- Small die size
- Easy SoC integration using standard synchronous bus interfaces, e.g., AMBA AHB
- Synthesizable soft IP package
- Optional companion Vertex Geometry Processor for enhanced transformation and lighting performance
- 2Dvia3D™ - 2D operations, including ROPs, scaled BLTs and colour space conversion, integrated into 3D pipeline, removing requirement for separate engine.
- Performance optimized for Unified Memory Architectures (UMA).
- Process portable design: 0.18µm, 0.13µm, 90nm and beyond
- Full scan design
- Synthesizable up to 80 MHz clock speed in 0.18µm and 120 MHz in 0.13µm.
- Patent protected algorithms

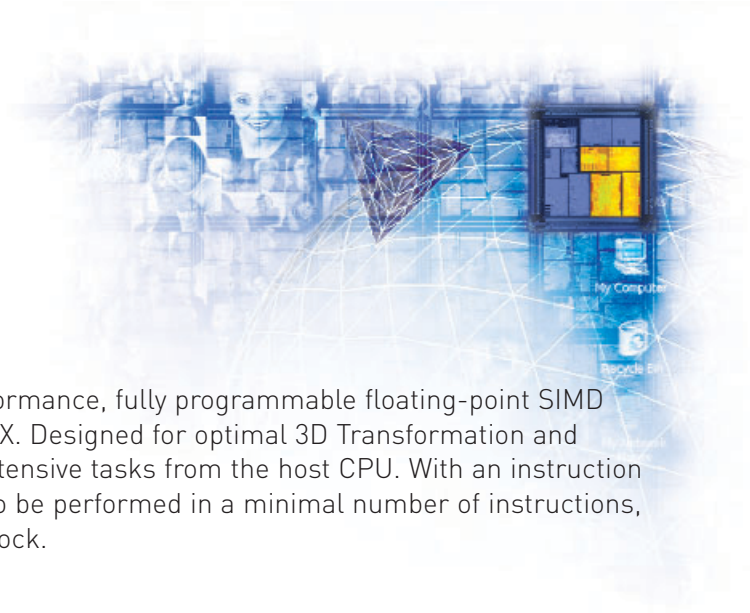
3D Features

- Tile-based rendering - enables on-chip processing of costly hidden-surface removal and pixel blending, and enables deferred texturing, eliminating all unnecessary accesses to off-chip memory.
- Scene Manager™ - seamless scene complexity management to support arbitrarily complex scenes in limited memory footprints.
- ITC™ - PowerVR Internal True Colour. Colour operations are performed on-chip at 32-bpp for superior colour precision.
- FSAA4Free™ - full screen anti-aliasing with no performance loss delivering smoother more realistic graphics at mobile display resolutions.
- PVR-TC™ - PowerVR texture compression for small memory footprints.

All key 3D features are included, including: flat and Gouraud shading; perspective texturing; specular highlights; 2 layer multitexturing; floating-point Z support; full tile blend buffer; effective fill rates that increase with 3D scene complexity; per vertex fog; comprehensive texture format support for compressed 2-bit and 4-bit textures, 16-bit and 32-bit textures and YUV video textures; point, bilinear, trilinear and anisotropic filtering; full range of blend modes; alpha test; and full-scene anti-aliasing.

PowerVR MBX is fully compatible with all industry-standard graphics APIs. Reference implementations are available for the following: OpenGL ES on SymbianOS and Linux; Direct3D on Windows CE; and MGL (PowerVR's native API) on SymbianOS and Linux.





Vertex Geometry Processor

PowerVR Vertex Geometry Processor (VGP) is a high-performance, fully programmable floating-point SIMD coprocessor carefully matched to the requirements of MBX. Designed for optimal 3D Transformation and Lighting (T&L), the VGP offloads these highly computer intensive tasks from the host CPU. With an instruction set carefully designed to allow common T&L operations to be performed in a minimal number of instructions, the VGP is capable of four floating-point operations per clock.

Performance

MBX provides the graphics performance, feature set and display quality to enable the migration of modern content to mobile platforms. MBX provides fill rates in excess of 360 million pixels/sec and throughput of 2.5 million triangles/sec, from a very small, very power-efficient core.

Size and Power

PowerVR MBX's unique patent-protected technologies enable it to deliver class-leading performance from a very small core, and its sophisticated power management techniques exploit both module and register-level clock gating to ensure the lowest possible active and standby power dissipation.

Related System Solution IP

PowerVR provides a wide range of complementary IP for use with MBX in SoC Designs including:

- PowerVR M2VX is a famaily of MPEG-2 video decoders for MP@ML, MP@HL or multiple stream decode.
- PowerVR M24VA is an efficient multi-standard video decode accelerator, designed to accelerate the decode of MPEG-2, MPEG-4, WMV8 and WMV9 video streams. It offloads iZZ, iDCT and motion compensation decode steps from the CPU for lower clock rate and power solutions.
- PowerVR Pixel Display Pipeline (PDP) is a highly configurable display controller which supports display solutions from simple graphics displays to complex systems requiring multiple video and graphics layers. The PDP is configurable for up to 6 planes with support scaling, blending and cursors.
- PowerVR TVE, a companion to the PDP, is a digital TV encoder, designed to output PAL or NTSC encoded video with simultaneous SVideo, RGBS or YUV component video for TV display.
- PowerVR De-interlacing. Motion adaptive and full motion compensation video de-interlacing cores are also available for the highest quality interlace to progressive processing available.

MBX Core Design Package

MBX is available as soft IP and ships with:

- Synthesis scripts
- Extensive verification test suite to ensure correct implementation of the design in an SoC
- Behavioural simulator written in ANSI C
- Hardware implementation guides and programmer's reference manuals

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