PowerVR TVE

The PowerVR TVE digital TV encoder outputs PAL or NTSC encoded Composite video and simultaneous S-Video, or RGBS or YUV component video for TV display when connected to a pixel display pipeline such as PowerVR PDP.

The PowerVR TVE is one of a range of PowerVR cores developed to meet the needs of the growing consumer multimedia market. PowerVR TVE is designed for use in low power, high performance system-on-chip (SoC) video applications including set-top boxes, games consoles and video cameras.

PowerVR TVE benefits include:

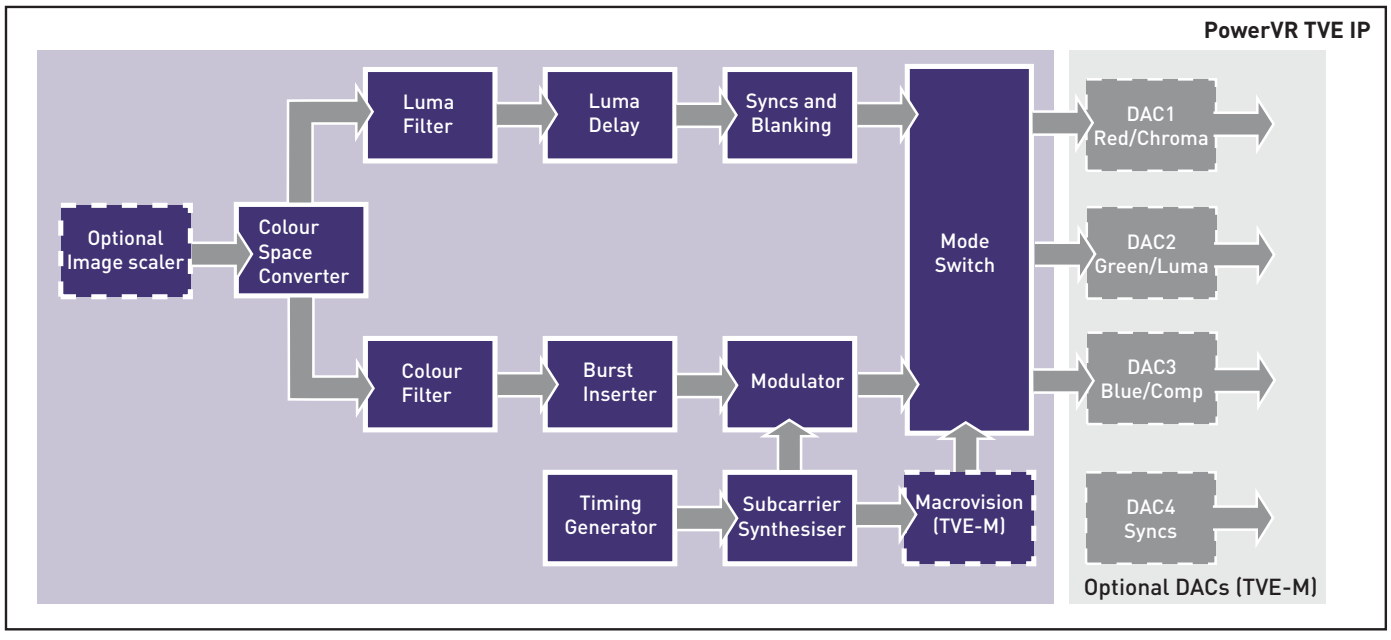
- Compliance with worldwide TV standards
- Composite and S-Video, RGB SCART or YUV outputs
- 10-bit video resolution
- High quality, selectable flicker filter eliminates interlace flicker on horizontal edges and fine detail
- Digital input for direct connection to PowerVR PDP display pipeline
- Load detection
- Small die size
- Synthesizable soft IP package
- Process portable design: 0.18µm, 0.13µm, 90nm and beyond

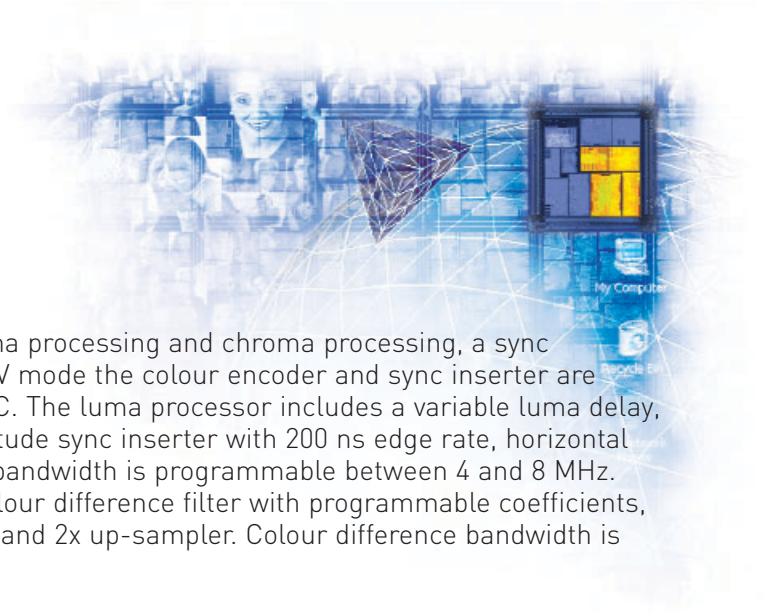
TVE features

- RGB or YCrCb digital input
- Programmable band-limiting filters optimize image quality for Composite or S-Video display
- Programmable timing and subcarrier generators support all PAL/NTSC variants
- Adjustments for brightness, contrast, saturation and luma/chroma differential delay
- Compatible with graphics resolutions from 320 x 200 to 800 x 600. Optional back-end scaler extends graphics resolution to 1024 x 768
- Provides overscanned or underscanned image size
- Oversampling reduces post-DAC filter cost and complexity
- Wide bandwidth RGB output
- Load detection assists with mode setting and power management
- Full scan design
- ATSC modes 480i, 480p, 720p, 1080i, YPbPr with tri-level syncs
- VBI data insertion for CC (Closed Caption), XDS (eXtended Data Service), CGMS-A (Copy Generation Management System - Analog) and WSS (Wide Screen Signalling)

PowerVR TVE-M

The PowerVR TVE-M core package adds integrated video DACs and Macrovision™ encoding for industry-standard analogue copy protection.





Architecture

PowerVR TVE consists of two colour space converters, luma processing and chroma processing, a sync generator, VBID inserter and optional DACs. In RGB or YUV mode the colour encoder and sync inserter are bypassed and mixed sync is generated from the fourth DAC. The luma processor includes a variable luma delay, 7 tap filter with programmable coefficients, variable amplitude sync inserter with 200 ns edge rate, horizontal blanking with 300 ns edge rate and 2x up-sampler. Luma bandwidth is programmable between 4 and 8 MHz. The chroma processor includes a burst inserter, 15 tap colour difference filter with programmable coefficients, programmable subcarrier synthesizer, chroma modulator and 2x up-sampler. Colour difference bandwidth is programmable between 0.6 and 2 MHz.

Compatibility

The timing generator has programmable horizontal timing to support ITU-601 and square pixel modes, and predefined 525/60 and 625/50 vertical timing to CCIR 624 specifications. Compliant with: PAL B, D, G, H, I, M and N, NTSC and NTSC-J. PowerVR TVE can be used with any suitable DACs up to 10-bit resolution. An accurate reference clock at two or four times pixel rate (or up to eight times with optional back-end downscaling) is required.

Optional Scaler

The optional multi-tap scaler allows individual horizontal and vertical resizing from any suitable graphics resolution to TV overscan or underscan image sizes.

Power Requirements

Power requirements are optimized by sophisticated power management techniques using register-level clock gating to ensure lowest active and standby power.

Related System Solution IP

- PowerVR graphics cores: MBX Pro for high-end 3D graphics acceleration for consumer electronics devices including set-top boxes, consoles and home entertainment systems. MBX for best area/performance 3D graphics acceleration for handheld devices and mainstream set-top boxes. MBX Lite for entry level 3D graphics acceleration for mobile devices.
- PowerVR M24VA is an efficient multi-standard video decode accelerator, designed to accelerate the decode of MPEG-2, MPEG-4, WMV8 and WMV9 video streams. It offloads iZZ, iDCT and motion compensation decode steps from the CPU for lower clock rate and power solutions.
- PowerVR Pixel Display Pipeline (PDP) is a multi-layer display controller, designed to support modern layered user interfaces. Configurable for up to 6 planes with support for YUV and RGB, scaling is available on two planes, and the PDP has configurable alpha-blending and chroma key support.

TVE Core Design Package

TVE is available as soft IP and ships with:

- Synthesis scripts
- Extensive verification test suite to ensure correct implementation of the design in an SoC
- Behavioural simulator written in ANSI C
- Hardware implementation guide
- Programmer's reference manual

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