HITACHI SEMICONDUCTOR TECHNICAL UPDATE

Classification of Production	Microprocessor			No	TN-SH7-466A/E	Rev	1
THEME	Supplement of programming manuals regarding SH-4 Pipeline Operation		Classification of Information	1. Spec change (2.) Supplement of Documents 3. Limitation of Use 4. Change of Mask 5. Change of Production Line			
PRODUCT NAME	SH-4	Lot No. ALL	Reference Documents	SH-4 Programming Manual (ADE-602-156D)		Effective Date Eternity	

This is the supplementary explanation regarding Pipeline operation and the number of Ick cycles.

The number of states (Ick cycles) which needs for the pipeline stages containing external memory accesses, is basically the number of states which is set by Bus State Controller (BSC) for the external memory.
But, there is the possibility that idle cycles are added to the pipeline stages containing external memory accesses.

Namely, there is the possibility that

1) the data transmission between Logical Address Bus and Physical Address Bus

and

2) the data transmission between different clock frequency Buses

become the cause to occur the idle cycles.

The pipeline stages containing external memory accesses, are a part of Instruction Fetch (I), and a part of Memory Access (MA).