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HITACHI SEMICONDUCTOR TECHNICAL UPDATE

Classification of Production	MPU		No	TN-SH7-465A/E	Rev	1
THEME	Manual correction about the Pin Functions	Classification of Information	1. Spec change (2.) Supplement of Documents 3. Limitation of Use 4. Change of Mask 5. Change of Production Line			
PRODUCT NAME	SH7750,SH7750S, SH7750R	Lot No. All	Reference Documents	SH7750Series Hardware Manual (ADE-602-124E)	Effective Date Eternal	

It corrects about Appendix E Pin Functions E.1 Pin States. Please refer to the following.

Table 1 Pin States in Reset, Power-Down State, and Bus-Released State

Signal Name	I/O	Reset (Power-On)		Reset (Manual)		Standby	Bus Released	Hard-Ware Standby	notes
		Master	Slave	Master	Slave				
D0 to D7	I/O	Z	Z	Z*21	Z*21	Z*21	Z*21	Z	
D8 to D15	I/O	Z	Z	Z*21	Z*21	Z*21	Z*21	Z	
D15 to D23	I/O	Z	Z	Z*21	Z*21	Z*21	Z*21	Z	
D24 to D31	I/O	Z	Z	Z*21	Z*21	Z*21	Z*21	Z	
D32 to D51	I/O	Z	Z	Z*21 K*20	Z*21 K*20	Z*21 K*20	Z*21 K*20	Z	
D52 to D55	I/O	Z	Z	Z*21	Z*21	Z*21	Z*21	Z	
D56 to D63	I/O	Z	Z	Z*21	Z*21	Z*21	Z*21	Z	
A0,A1,A18 to A25	O	PZ	PZ	Z*14 O*17	Z*14	Z*14 O*7	Z*14	Z	
A2 to A17	O	PZ	PZ	Z*14 O*9	Z*14	Z*14 O*7	Z*14	Z	
RESET#	I	I	I	I	I	I	I	I	
BACK#/BSREQ#	O	H	H	H	H	H	O	Z	
BREQ#/BSACK#	I	PI	PI	I*13	I*13	I*13	I*13	Z	
BS#	O	H	PZ	H	Z*14	Z*14 H*7	Z*14	Z	
CKE	O	H	H	O	O	L	O	Z	
CS0# to CS6#	O	H	PZ	H	Z*14	Z*14 H*7	Z*14	Z	
RAS#	O	H	PZ	O	Z*14	Z*14 O*5	Z*14 O*5	Z	
RD#/CASS#/FRAME#	O	H	PZ	O	Z*14	Z*14 O*5	Z*14 O*5	Z	
RD/WR#	O	H	PZ	H	Z*14	Z*14 H*7	Z*14	Z	
RDY#	I	PI	PI	I*13	I*13	Z*13	I*13	Z	
WE7#/CAS7#/DQM7	O	H	PZ	O	Z*14	Z*14 O*5	Z*14 O*5	Z	
WE6#/CAS6#/DQM6	O	H	PZ	O	Z*14	Z*14 O*5	Z*14 O*5	Z	
WE5#/CAS5#/DQM5	O	H	PZ	O	Z*14	Z*14 O*5	Z*14 O*5	Z	
WE4#/CAS4#/DQM4	O	H	PZ	O	Z*14	Z*14 O*5	Z*14 O*5	Z	
WE3#/CAS3#/DQM3	O	H	PZ	O	Z*14	Z*14 O*5	Z*14 O*5	Z	
WE2#/CAS2#/DQM2	O	H	PZ	O	Z*14	Z*14 O*5	Z*14 O*5	Z	
WE1#/CAS1#/DQM1	O	H	PZ	O	Z*14	Z*14 O*5	Z*14 O*5	Z	
WE0#/CAS0#/DQM0	O	H	PZ	O	Z*14	Z*14 O*5	Z*14 O*5	Z	
DACK0 to DACK1	O	L	L	L	L	Z*12O*8	O	Z	
MD7/TXD	I/O	PI*16	PI*16	Z*12	Z*12	Z*12 K*20O*8	Z*12 K*20O*8	Z	
MD6/IOIS16#	I	PI*16	PI*16	I*13	I*13	Z*13	I*13	Z	

Table 1 Pin States in Reset, Power-Down State, and Bus-Released State(cont)

Signal Name	I/O	Reset (Power-On)		Reset (Manual)		Standby	Bus Released	Hard-Ware Standby	notes
		Master	Slave	Master	Slave				
MD5/RAS2#	I/O[*1]	PI[*16]	PI[*16]	Z[*14] O[*6]	Z[*14]	Z[*14] O[*5]	Z[*14] O[*5]	Z	
MD4/CE2B#	I/O[*3]	PI[*16]	PI[*16]	Z[*14] H[*7]	Z[*14]	Z[*14] H[*7]	Z[*14]	Z	
MD3/CE2A#	I/O[*2]	PI[*16]	PI[*16]	Z[*14] H[*7]	Z[*14]	Z[*14] H[*7]	Z[*14]	Z	
CKIO	O	O	O	O[*11] Z[*11]	O[*11] Z[*11]	PZ	O[*11] Z[*11]	Z	
STATUS1	O	O	O	O	O	O	O	Z O[*18]	
IRL0# to IRL3#	I	PI	PI	I[*13]	I[*13]	I[*13]	I[*13]	I	
NMI	I	PI	PI	I[*13]	I[*13]	I[*13]	I[*13]	I	
DREQ0# to DREQ1#	I	PI	PI	I[*12]	I[*12]	Z[*12]	I[*12]	Z	
DRAK0 to DRAK1	O	L	L	L	L	Z[*12] O[*8]	O	Z	
MD0/SCK	I/O	PI[*16]	PI[*16]	I[*12]	I[*12]	Z[*12] K[*20] O[*8]	I[*12] O K[*20]	Z	
RXD	I	PI	PI	I[*12]	I[*12]	Z[*12]	I[*12]	Z	
SCK2/MRESET#	I	PI	PI	I[*12]	I[*12]	I[*12]	I[*12]	Z	
MD1/TXD2	I/O	PI[*16]	PI[*16]	Z[*12]	Z[*12]	Z[*12] K[*20] O[*8]	Z[*12] K[*20] O[*8]	Z	
MD2/RXD2	I	PI[*16]	PI[*16]	I[*12]	I[*12]	Z[*12]	I[*12]	Z	
CTS2#	I/O	PI	PI	I[*12]	I[*12]	Z[*12] K[*20]	I[*12] K[*20]	Z	
MD8/RTS2#	I/O	PI[*16]	PI[*16]	I[*12]	I[*12]	Z[*12] K[*20]	I[*12] K[*20]	Z	
TCLK	I/O	PI	PI	I[*12]	I[*12]	Z[*12] O[*19]	I[*12] O[*19]	Z	
TDO	O	O	O	O	O	O	O	Z	
TMS	I	PI	PI	PI	PI	PZ	PI	Z	
TCK	I	PI	PI	PI	PI	PZ	PI	Z	
TDI	I	PI	PI	PI	PI	PZ	PI	Z	
TRST#	I	PI	PI	PI	PI	PZ	PI	Z	
CKIO2[*23]	O	PZ[*22] O[*10]	PZ[*22] O[*10]	PZ[*22] O[*10*22]	PZ[*22] O[*10*22]	PZ	PZ[*22] O[*10*22]	Z	
RD2#[*23]	O	Z[*22] H[*10*22]	Z[*22] PZ[*10]	Z[*14*22] O[*10]	Z[*10*14]	Z[*10*14] O[*5]	Z[*10*14] O[*5]	Z	
RD/WR2#[*23]	O	Z[*22] H[*10*22]	Z[*22] PZ[*10]	Z[*14*22] H[*10]	Z[*10*14]	Z[*10*14] H[*5]	Z[*10*14]	Z	
CKIO2ENB#[*23]	I	PI	PI	PI	PI	PI	PI	Z	
CA	I	I	I	I	I	I	I	I	
ASEBRK#/BRKACK#	I/O	PI[*24] O[*24]	PI[*24] O[*24]	PI[*24] O[*24]	PI[*24] O[*24]	PI[*24] O[*24]	PI[*24] O[*24]	Z	

Notes:

I : Input(not Pulled Up)
O : Output
Z : High-impedance(not Pulled Up)
H : High-level output
L : Low-level output
K : Output state held
PI : Input(Pulled Up)
PZ: High-impedance (not Pulled Up)

*1: Output when area 2 is used as DRAM.
*2: Output when area 5 is used as PCMCIA.
*3: Output when area 6 is used as PCMCIA.
*4: Depends on refresh and DMAC operations.
*5: Z(I) or O on refresh operations, depending on register setting(BCR1.HIZCNT).
*6: Depends on refresh operations.
*7: Z(I) or H(state held), depending on register setting (BCR1. HIZMEM).
*8: Z or O, depending on register setting (STBCR.PHZ).
*9: Output when refreshing is set.
*10: Operation in respective state when CKIO2ENB# = 0(SH7750/SH7750S)(High-level outputs at SH7750R).

*11: PZ or O, depending on register setting (FRQCR.CKOEN).
*12: Pulled up or not pulled up, depending on register setting (STBCR.PPU).
*13: Pulled up or not pulled up, depending on register setting (BCR1.IPUP).
*14: Pulled up or not pulled up, depending on register setting (BCR1.OPUP).
*15: Not pulled up.
*16: Pulled up with a built-in pull-up resistance. However, it cannot use for fixation of an input MD pin at the time of power-on reset. Pulled up or down outside the SH-4
*17: Output when refreshing is set (SH7750R only).
*18: Z or O, depending on register setting (STBCR2.STHZ)(SH7750R only).
*19: Z or O, depending on register setting (TOCR.TCOE)
*20: Output state held when used as port.
*21: Pulled up or not pulled up, depending on register setting (BCR1.DPUP) (SH7750R only).
*22: Z when CKIO2ENB# = 1
*23: BGA Package only.
*24: Depends on Emulator operations.

Changed parts:

1.Since a pull-up is not carried out by having no built-in pull-up, the description Z*16 is changed to Z. The notes about SH7750R are added by *21.
2. Since a pull-up is carried out by built-in pull-up, the description PI*16, and I*16 are changed to PI, and Z*16 is changed to PZ. However, notes addition which is *16 about MD pin pulled up.
3. Notes at the time of a port setup are added by *20.
4. Since it outputs also at the time of refresh, the description O*6 is changed to O.
5. DACK1-DACK0, and DRAK1-DRAK0 at the time of standby and Bus-released, the description O*12 is changed to O.
6. Notes about SH7750R are added by *18.
7. It adds about ASEBRK#/BRKACK.
8. BREQ#/BSACK# at the time of hardware standby is corrected to Z from I.
9. MD6/IOIS16#, DREQ1#-DREQ0#, MD0/SCK, RXD, MD2/RXD2, and RDY# at the time of standby, are corrected to Z from I.
10. TCLK, TMS, TCK, TDI and TRST# at the time of standby, are corrected to PZ from I.
11. *13 of MD5/RAS2#, MD4/CE2B#, and MD3/CE2A# are corrected to *14, and *7 are added.
12. CKIO, and CKIO2 at the time of standby are corrected to PZ from ZO.
13. O*18 is added to STATUS1-STATUS0 at the time of hardware standby.
14. K*20 is added to MD1/TXD2, andMD7/TXD at the time of standby and Bus-released.
15. I at the time of standby of CTS2#, and MD8/RTS2# is deleted, and O at the time of standby and Bus-released is corrected to K.
16. The value at the time of CKIOENB# setup is indicated to CKIO2, RD2#, and RD/WR2#.