HITACHI SEMICONDUCTOR TECHNICAL UPDATE

DATE	1 February 2000	No.	TN -SH7-203A /E
THEME	Limitation on Store Queue instructions due to incapability of cancellation		
CLASSIFICATION	☐ Spec. change ■ Limitation on Use ☐ Supplement of Documents		
PRODUCT NAME	HD6417750, HD6417750S, HD6417751		
REFERENCE DOCUMENTS	SH-4 Series Hardware Manual, SH-4 Programming Manual	Effective Date: Eternity Lot#: All	

1.Contents

When an exception occurs by an instruction located from 0 to 3 instructions before a store instructions into Store Queue (SQ), the execution of the store instruction into SQ, which should be canceled on the occurrence of the exception, is possibly completed on the branch to the exception handling routine.

In an application program, there is a possibility of incorrect behavior shown as 1.1 and 1.2 below:

1.1 SQ data transfer to the external memory in the normal program

When a PREF instruction is located from 0 to 3 instructions before a store instructions into SQ, the execution of the store instruction into SQ, which should be canceled on the occurrence of the exception, is possibly completed and SQ is updated on the branch to the exception handling routine. After return from the exception handling routine, the PREF instruction is re-executed and the incorrect data are transferred to the external memory in result.

1.2 SQ data transfer to the external memory in the exception handling routine

When a PREF instruction is executed in the exception handling program, incorrect data are possibly transferred to the external memory.

(Ex.1) PREF to SQ for the transfer to external memory followed by a store to the same SQ

```
PREF instruction ; to transfer SQ data to the external memory
                 ; SPC holds an address of this instruction on the occurrence of exception.
                 ; Inst1, Inst2, or Inst3 may be executed on the return from the exception
                 ; handling routine.
Instruction 1    ; may be executed when this is a store instruction to SQ.
Instruction 2    ; may be executed when this is a store instruction to SQ.
Instruction 3    ; may be executed when this is a store instruction to SQ.
Instruction 4    ; not executed even when this is a store instruction to SQ.
```

(Ex.2) An exception occurs at a branch instruction whose branch condition is true

```
Instruction 1 (branch instruction)
                ; SPC holds an address of this instruction on the occurrence of exception.
Instruction 2   ; may be executed when this is a delay slot of Instruction 1
                ;     and a store instruction to SQ.
Instruction 3   ;
Instruction 4   ;
Instruction 5 (target of the branch by Instruction1)
                ; may be executed when this is a store instruction to SQ.
Instruction 6   ; may be executed when this is a store instruction to SQ.
```

(Ex.3) An exception occurs at a branch instruction whose branch condition is false

```
Instruction 1 (branch instruction)
              ; SPC holds an address of this instruction on the occurrence of exception.
Instruction 2 ; may be executed when this is a store instruction to SQ.
Instruction 3 ; may be executed when this is a store instruction to SQ.
Instruction 4 ; may be executed when this is a store instruction to SQ.
Instruction 5 ; not executed even when this is a store instruction to SQ.
```

2. Workaround

Both 2.1 and 2.2 shown below should be satisfied:

2.1 When a PREF instruction which transfers SQ data to the external memory is followed by a store instruction accessing to the same SQ, both (1) and (2) below should be satisfied:

(1) 3 NOP instructions (*****1) are required between the two instructions.
(2) PREF instruction transferring SQ data into the external memory should not be located in the delay slot of any branch instructions.

(*****1) If there are other instructions between the two instructions, 3 instructions (including NOP's) satisfy this workaround.

2.2 PREF instruction transferring SQ data into external memory should not be executed inside the exception handling program.
If this is executed and if a store instructions into SQ is located in the address specified by SPC,SPC+2,SPC+4, or SPC+6 (*2), the data transferred from SQ are possibly updated by the store instruction.

(*2) If a branch instruction is located in the address specified by SPC, target two instructions by the branch instruction are included instead of the instructions located in SPC+4 and SPC+6.