HITACHI SEMICONDUCTOR TECHNICAL UPDATE

DATE	9th August, 1999	No.	TN-SH7-179A /E
THEME	Revision of BCR1 description		
CLASSIFICATION	☐ Spec. change ☑ Supplement of Documents	☐ Limitation on Use	
PRODUCT NAME	HD6417750BP200, HD6417750F167, HD6417750VF128		
REFERENCE DOCUMENTS	SH7750 Hardware Manual	Effective Date	eternity
		From	

1. Revision of SH7750 Hardware Manual

Description of BCR1

Bit:30 Master
0 : In a power-on reset, the master/slave setting external pin (MD7) is high, designating master mode for the SH7750
1 : In a power-on reset, the master/slave setting external pin (MD7) is low, designating slave mode for the SH7750

Bit 29 : A0MPX
0 : In a power-on reset, the external pin specifying the area 0 memory type (MD6) is high, designating the area 0 memory type as normal memory
1 : In a power-on reset, the external pin specifying the area 0 memory type (MD6) is low, designating the area 0 memory type as MPX