RP56LD, RP336LU, and RP336LD Modem Data Pumps

Designer's Guide (Preliminary)

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NOTICE

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1. INTRODUCTION

1.1 SUMMARY

The Rockwell RP56LD, RP336U, and RP336D Modem Data Pump (MDP) families support high speed data, high speed fax, AudioSpan, voice coding/decoding (optional), and full-duplex speakerphone (optional) functions depending upon model (Table 1-1). Low voltage and low power consumption support portable applications. Downloadable architecture allows upgrading of MDP code from the host/DTE.

The RP56LD supports Rockwell K56flex data modem operation. The RP336LD and RP336LU support V.34 data modem operation. The RP336LU can be optionally upgraded to RP56LD capability. Otherwise, the MDPs are identical within like models, e.g., SP models operate the same. Unless otherwise noted, descriptions in this document apply to all MDP models.

K56flex™ models can receive data at speeds up to 56 kbps from a digitally connected K56flex-compatible central site modem, such as a Rockwell RC56CSM modem. K56flex modems take advantage of the PSTN which is primarily digital except for the client modem to central office local loop and are ideal for applications such as remote access to an Internet service provider (ISP), on-line service, or corporate site. The MDP can send data at speeds up to V.34 rates.

In V.34 data mode, the MDP can operate in 2-wire, full-duplex, synchronous/asynchronous modes at rates up to 33600 bps. Using V.34 techniques to optimize modem configuration for line conditions, the MDP can connect at the highest data rate that the channel can support from 33600 bps to 2400 bps with auto-fallback to V.32 bis.

Internal HDLC support eliminates the need for an external serial input/output (SIO) device in the DTE for products incorporating error correction and T.30 protocols.

Voice mode includes an Adaptive Differential Pulse Code Modulation (ADPCM) voice coder and decoder (codec). The codec compresses and decompresses voice signals for efficient digital storage of voice messages. The codec operates at 28.8k, 21.6k, or 14.4k bps (4-bit, 3-bit, or 2-bit quantization, respectively) with a 7.2 kHz sample rate.

A voice pass-through mode in all models allows the host to transmit and receive uncompressed audio signals.

SP models support position-independent full-duplex speakerphone (FDSP) operation using a dual internal integrated analog circuit to interface with the telephone line and the audio input/out (i.e., a headset, handset, or a microphone with external speaker).

AudioSpan (analog simultaneous audio/voice and data) operation supports a data rate of 4.8 kbps with audio.

The MDP operates over the public switched telephone network (PSTN) through the appropriate line termination.

Table 1-1. Modem Models and Functions

Modem/Part Number[1]		Package and Package Options				Supported Functions[2]		
Model Number	Part No.	Package	Power	Crystal/Clock Input	Analog Interface Voltage	K56flex Data, Voice/Audio	V.34 Data, V.17 Fax, AudioSpan	FDSP
RP56LD/SP	R6764-11	100-Pin PQFP	Low Power	Clock	+3.3V	Y	Y	Y
RP56LD	R6764-13	100-Pin PQFP	Low Power	Clock	+3.3V	Y	Y	–
RP336LU/SP	R6764-14	100-Pin PQFP	Low Power	Clock	+3.3V	Upgrade	Y	Y
RP336LU	R6764-15	100-Pin PQFP	Low Power	Clock	+3.3V	Upgrade	Y	–
RP336LD/SP	R6764-16	100-Pin PQFP	Low Power	Clock	+3.3V	–	Y	Y
RP336LD	R6764-17	100-Pin PQFP	Low Power	Clock	+3.3V	–	Y	–
RP56LD/SP	R6785-11	144-Pin TQFP	Low Power	Clock/Crystal	+3.3V/+5V	Y	Y	Y
RP56LD	R6785-13	144-Pin TQFP	Low Power	Clock/Crystal	+3.3V/+5V	Y	Y	–
RP336LU/SP	R6785-14	144-Pin TQFP	Low Power	Clock/Crystal	+3.3V/+5V	Upgrade	Y	Y
RP336LU	R6785-15	144-Pin TQFP	Low Power	Clock/Crystal	+3.3V/+5V	Upgrade	Y	–
RP336LD/SP	R6785-16	144-Pin TQFP	Low Power	Clock/Crystal	+3.3V/+5V	–	Y	Y
RP336LD	R6785-17	144-Pin TQFP	Low Power	Clock/Crystal	+3.3V/+5V	–	Y	–

Notes:

1. Model/part number options:
   - L Low power
   - U Upgradable and downloadable
   - D Downloadable
   - SP Speakerphone.
2. Supported functions (Y = Supported; – = Not supported):
   - FDSP Full-duplex speakerphone
   - Voice/Audio Voice and audio
   - AudioSpan Analog simultaneous voice and data

1.2 FEATURES

- Downloadable MDP code from the host/DTE
- 2-wire full-duplex
  - K56flex™ (RP56LD models)
  - V.34 (33.6 kbps), V.32 bis, V.32, V.22 bis, V.22, V.23, and V.21
  - Bell 212 and 103
- 2-wire half-duplex
  - ITU-T V.17, V.33, V.29, V.27 ter, and V.21 channel 2
  - Bell 208
  - Short train option in V.17 and V.27 ter
- Serial synchronous and asynchronous data
- Parallel synchronous and asynchronous data
- Parallel synchronous SDLC/HDLC support
- In-band secondary channel (V.34 and V.32 bis)
- Automatic mode selection (AMS)
- Automatic rate adaption (ARA)
- Digital near-end and far-end echo cancellation
- Bulk delay for satellite transmission
- Auto-dial and auto-answer
- AudioSpan (simultaneous audio/voice and data)
  - ITU-T V.61 modulation (4.8 kbps data plus audio)
  - Handset, headset, or half-duplex speakerphone
- ADPCM voice mode
- Voice pass-through mode
- Full-duplex speakerphone (optional)
  - Acoustic and line echo cancellation
  - Programmable microphone AGC
  - Microphone volume selection and muting
  - Speaker volume control and muting; room monitor
- TTL and CMOS compatible DTE interface
  - ITU-T V.24 (EIA/TIA-232-E) (data/control)
  - Microprocessor bus (data/configuration/control)
- Dynamic range: -9 dBm to -43 dBm
- Adjustable speaker output to monitor received signal
- DMA support interrupt lines
- Two (16+128)-byte FIFO data buffers for burst data transfer
- NRZI encoding/decoding
- 511 pattern generation/detection
- Diagnostic capability
- V.8, V.8 bis signaling
- V.13 signaling
- V.54 inter-DCE signaling
- V.54 local analog and remote digital loopback
- +3.3V operation
  - +5V input voltage tolerance
  - +5V or +3.3V analog operation
- Low power consumption:
  - Normal Mode 250 mW
  - Sleep Mode 33 mW
  - Stop Mode <1 mW
- Low profile, small footprint package meets PCMCIA Type II envelope requirements for PC Cards
  - 100-pin PQFP or 144-pin TQFP

1.3 TECHNICAL DESCRIPTION

Configurations and Rates

The selectable MDP configurations, signaling rates, and data rates are listed in Table 1-2.

Automatic Mode Selection

When automatic mode selection (AMS) is enabled, the MDP configures itself to the highest compatible data rate supported by the remote modem (AUTO bit). Automode operation is supported in K56flex, V.34, V.32 bis, V.32 V.22 bis, V.22, V.21, V.23, Bell 212A, and Bell 103 modes.

NOTE: Bit names refer to data, control, and/or status bits in the MDP interface memory (see Table 3-1).

Automatic Rate Adaption (ARA)

In K56flex, V.34, and V.32 bis modes, automatic rate adaption (ARA) can be enabled to select the highest data rate possible based on the measured eye quality monitor (EQM) (EARC bit). This selection occurs during handshake/retrain and rate renegotiation.

Tone Generation

The MDP can generate single or dual voice-band tones from 0 Hz to 3600 Hz with a resolution of 0.15 Hz and an accuracy of ± 0.01%. Tones over 3000 Hz are attenuated. DTMF tone generation allows the MDP to operate as a programmable DTMF dialer.

Data Encoding

The data encoding conforms to ITU-T recommendations V.34, V.32 bis, V.32, V.17, V.33, V.29, V.27 ter, V.22 bis, V.22, V.23, or V.21, and is compatible with Bell 208, 212A, or 103, depending on the configuration.

RTS - CTS Response Time

The response times of CTS relative to a corresponding transition of RTS are listed Table 1-3.

Transmit Level

The transmitter output level is selectable from -4 dBm to -19 dBm (VAA = +3.3V) or 0 dBm to -15 dBm (VAA = +5V) in 1 dB steps and is accurate to ±0.5 dB when used with an external hybrid. The output level can also be fine tuned by changing a gain constant in MDP DSP RAM. The maximum V.34/V.32 bis/V.32 transmit level for acceptable receive performance should not exceed -9 dBm.

Note: In V.34 mode, the transmit level may be automatically changed during the handshake. This automatic adjustment of the transmit level may be disabled via a parameter in DSP RAM.

Transmitter Timing

Transmitter timing is selectable between internal (±0.01%), external, or slave.

Scrambler/Descrambler

A self-synchronizing scrambler/descrambler is used in accordance with the selected configuration.

Answer Tone

When the NV25 bit is a zero, the MDP generates a 2100 Hz answer tone at the beginning of the answer handshake for 5.0 seconds (V.8) or 3.6 seconds (V.32 bis, V.32, V.22 bis, V.22, V.23, and V.21). The answer tone has 180° phase reversals every 0.45 second to disable network echo cancellers (V.8, V.32 bis, V.32).

Table 1-2. Configurations, Signaling Rates, and Data Rates

Configuration	Modulation	Carrier Frequency (Hz) ±0.01%	Data Rate (bps) ±0.01%	Symbol Rate (Symbols/Sec.)	Bits/Symbol - Data	Bits/Symbol - TCM	Constellation Points
K56flex PCM	PCM	–	56000R/V.34ratesT[4]	8000	Dynamic	–	–
V.34 33600 TCM	TCM	Note 2	33600	Note 2	Note 2	Note 2	Note 2
V.34 31200 TCM	TCM	Note 2	31200	Note 2	Note 2	Note 2	Note 2
V.34 28800 TCM	TCM	Note 2	28800	Note 2	Note 2	Note 2	Note 2
V.34 26400 TCM	TCM	Note 2	26400	Note 2	Note 2	Note 2	Note 2
V.34 24000 TCM	TCM	Note 2	24000	Note 2	Note 2	Note 2	Note 2
V.34 21600 TCM	TCM	Note 2	21600	Note 2	Note 2	Note 2	Note 2
V.34 19200 TCM	TCM	Note 2	19200	Note 2	Note 2	Note 2	Note 2
V.34 16800 TCM	TCM	Note 2	16800	Note 2	Note 2	Note 2	Note 2
V.34 14400 TCM	TCM	Note 2	14400	Note 2	Note 2	Note 2	Note 2
V.34 12000 TCM	TCM	Note 2	12000	Note 2	Note 2	Note 2	Note 2
V.34 9600 TCM	TCM	Note 2	9600	Note 2	Note 2	Note 2	Note 2
V.34 7200 TCM	TCM	Note 2	7200	Note 2	Note 2	Note 2	Note 2
V.34 4800 TCM	TCM	Note 2	4800	Note 2	Note 2	Note 2	Note 2
V.34 2400 TCM	TCM	Note 2	2400	Note 2	Note 2	Note 2	Note 2
V.32 bis 14400 TCM	TCM	1800	14400	2400	6	1	128
V.32 bis 12000 TCM	TCM	1800	12000	2400	5	1	64
V.32 bis 9600 TCM	TCM	1800	9600	2400	4	1	32
V.32 bis 7200 TCM	TCM	1800	7200	2400	3	1	16
V.32 bis 4800	QAM	1800	4800	2400	2	0	4
V.32 9600 TCM	TCM	1800	9600	2400	4	1	32
V.32 9600	QAM	1800	9600	2400	4	0	16
V.32 4800	QAM	1800	4800	2400	2	0	4
V.22 bis 2400	QAM	1200/2400	2400	600	4	0	16
V.22 bis 1200	DPSK	1200/2400	1200	600	2	0	4
V.22 1200	DPSK	1200/2400	1200	600	2	0	4
V.22 600	DPSK	1200/2400	600	600	1	0	4
V.23 1200/75	FSK	1700/420	1200/75	1200	1	0	–
V.21	FSK	1080/1750	0–300	300	1	0	–
Bell 208 4800	DPSK	1800	4800	1600	3	0	8
Bell 212A	DPSK	1200/2400	1200	600	2	0	4
Bell 103	FSK	1170/2125	0–300	300	1	0	–
V.23 1200/75	FSK	1700/420	1200/75	1200	1	0	–
V.21	FSK	1080/1750	0–300	300	1	0	–
V.17 14400 TCM/V.33[3]	TCM	1800	14400	2400	6	1	128
V.17 12000 TCM/V.33[3]	TCM	1800	12000	2400	5	1	64
V.17 9600 TCM[3]	TCM	1800	9600	2400	4	1	32
V.17 7200 TCM[3]	TCM	1800	7200	2400	3	1	16
V.29 9600[3]	QAM	1700	9600	2400	4	0	16
V.29 7200[3]	QAM	1700	7200	2400	3	0	8
V.29 4800[3]	QAM	1700	4800	2400	2	0	4
V.27 4800[3]	DPSK	1800	4800	1600	3	0	8
V.27 2400[3]	DPSK	1800	2400	1200	2	0	4
V.21 Channel 2[3]	FSK	1750	300	300	1	0	–
Tone Transmit	–	–	–	–	–	–	–

Notes:

1. Modulation legend: TCM: Trellis-Coded Modulation; QAM: Quadrature Amplitude Modulation; FSK: Frequency Shift Keying; DPSK: Differential Phase Shift Keying

2. Adaptive; established during handshake:

	Carrier Frequency (Hz)	
Symbol Rate (Baud)	V.34 Low Carrier	V.34 High Carrier
2400	1600	1800
2800	1680	1867
3000	1800	2000
3200	1829	1920
3429	1959	1959

3. Models with fax support only.
4. Maximum data rate.

Table 1-3. RTS-CTS Response Times

Configuration	RTS-CTS Response[1]		Turn-Off Sequence[3]
	Constant Carrier	Controlled Carrier	
K56flex, V.34, V.32 bis, V.32	± 2 ms	N/A	N/A
V.33/V.17 Long	N/A	1393 ms[2]	15 ms[4]
V.33/V.17 Short	N/A	142 ms[2]	15 ms[4]
V.29	N/A	253 ms[2]	12 ms
V.27 4800 Long	N/A	708 ms[2]	7 ms[4]
V.27 4800 Short	N/A	50 ms[2]	7 ms[4]
V.27 2400 Long	N/A	943 ms[2]	10 ms[4]
V.27 2400 Short	N/A	67 ms[2]	10 ms[4]
V.22 bis, V.22, Bell 212A	± 2 ms	270 ms	N/A
V.21	500 ms	500 ms	N/A
V.23, Bell 103	210 ms	210 ms	N/A

Notes:

1. Times listed are CTS turn-on. The CTS OFF-to-ON response time is host programmable in DSP RAM. (Full-duplex modes only.)
2. Add echo protector tone duration plus 20 ms when echo protector tone is used during turn-on.
3. Turn-off sequence consists of transmission of remaining data and scrambled ones for controlled carrier operation. CTS turn-off is less than 2 ms for all configurations.
4. Plus 20 ms of no transmitted energy.
5. N/A = not applicable.

Receive Level

The MDP satisfies performance requirements for received line signal levels from –9 dBm to –43 dBm measured at the Receiver Analog (RXA) (TIP and RING) input (-15 dBm at RIN).

Note: A 6 dB pad is required between TIP and RING and the RIN input.

Receiver Timing

The timing recovery circuit can track a frequency error in the associated transmit timing source of ±0.035% (V.22 bis) or ±0.01% (other configurations).

Carrier Recovery

The carrier recovery circuit can track a ±7 Hz frequency offset in the received carrier.

Clamping

Received Data (RXD) is clamped to a constant mark whenever the Received Line Signal Detector (~RLSD) is off. ~RLSD can be clamped off (RLSDE bit).

Echo Canceller

A data echo canceller with near-end and far-end echo cancellation is included for 2-wire full-duplex V.34/V.32 bis/V.32 operation. The combined echo span of near and far cancellers can be up to 40 ms. The proportion allotted to each end is automatically determined by the MDP. The delay between near-end and far-end echoes can be up to 1.2 seconds.

K56flex echo cancellation is also provided.

AudioSpan Mode

AudioSpan provides full-duplex analog simultaneous audio/voice and data over a single telephone line at a data rate with audio of 4800 bps using V.61 modulation. AudioSpan can send any type of audio waveform, including music. Data can be sent with or without error correction. The audio/voice interface can be in the form of a headset, handset, or a microphone and speaker (half-duplex speakerphone). Handset echo cancellation is provided.

Speakerphone Voice/Audio Paths (/SP Model)

The MDP incorporates a dual integrated analog interface. The voice/audio transmit and receive signals can be routed through several paths. The voice/audio paths are available in the speakerphone mode configuration and are selected through DSP RAM.

The voice/audio input can be taken from one of four different sources: telephone line input (RIN), handset (TELIN), microphone (MICM or MICV).

The speaker output (SPK) can originate from one of five different sources: RIN, TELIN, MICM or MICV or from the MDP's internal voice playback mode.

The voice/audio output may be routed to the telephone line output (TXA1 and TXA2) or handset (TELOUT).

The voice paths can be switched to allow an audio input to be routed to the telephone line output through a variable gain for applications such as music-on-hold.

The "room monitor" mode allows the MDP to receive audio from its surroundings and concurrently transmit the audio to a remote site.

ADPCM Voice Mode (V Models)

Transmit Voice. 16-bit compressed transmit voice can be sent to the MDP ADPCM codec for decompression then to the digital-to-analog converter (DAC) by the host.

Receive Voice. 16-bit received voice samples from the MDP analog-to-digital converter (ADC) can be sent to the ADPCM codec for compression, and then be read by the host.

Voice Pass-Through Mode

Transmit Voice. 16-bit transmit voice samples can be sent to the MDP DAC from the host.

Receive Voice. 16-bit received voice samples from the MDP ADC can be read by the host.

Data Formats

Serial Synchronous Data

Data rate: 300-56000 bps ±0.01%.

Selectable clock: Internal, external, or slave.

Serial Asynchronous Data

Data rate: 300-56000 bps +1% (or +2.3%), -2.5%;
0-300 bps (V.21 and Bell 103);
1200/75 bps (V.23).

Bits per character: 7, 8, 9, 10, or 11.

Parallel Synchronous Data

Normal sync: 8-bit data for transmit and receive

Data rate: 300-56000 bps ±0.01%.

SDLC/HDLC support:

Transmitter: Flag generation, 0 bit stuffing, CRC-16 or CRC-32 generation.

Receiver: Flag detection, 0 bit deletion, CRC-16 or CRC-32 checking.

Parallel Asynchronous Data

Data rate: 300-56000 bps +1% (or 2.3%), -2.5%;
1200, 300, or 75 bps (FSK).

Data bits per character: 5, 6, 7, or 8.

Parity generation/checking: Odd, even, or 9th data bit.

Async/Sync and Sync/Async Conversion

An asynchronous-to-synchronous converter is provided in the transmitter and a synchronous-to-asynchronous converter is provided in the receiver. The converters operate in both serial and parallel modes. The asynchronous character format is 1 start bit, 5 to 8 data bits, an optional parity bit, and 1 or 2 stop bits. Valid character size, including all bits, is 7, 8, 9, 10, or 11 bits per character. Two ranges of signaling rates are provided:

- Basic range: +1% to –2.5%
- Extended overspeed range: +2.3% to –2.5%

When the transmitter's converter is operating at the basic signaling rate, no more than one stop bit will be deleted per 8 consecutive characters. When operating at the extended rate, no more than one stop bit will be deleted per 4 consecutive characters. Break handling is performed as described in V.14.

Asynchronous characters are accepted on the TXD serial input and are issued on the RXD serial output.

V.54 Inter-DCE Signaling

The MDP supports V.54 inter-DCE signaling procedures in synchronous and asynchronous configurations. Transmission and detection of the preparatory, acknowledgment, and termination phases as defined in V.54 are provided. Three control bits in the transmitter allow the host to send the appropriate bit patterns (V54T, V54A, and V54P bits). Three control bits in the receiver are used to enable one of three bit pattern detectors (V54TE, V54AE, and V54PE bits). A status bit indicates when the selected pattern detector has found the corresponding bit pattern (V54DT bit).

V.13 Remote RTS Signaling

The MDP supports V.13 remote RTS signaling. Transmission and detection of signaling bit patterns in response to a change of state in the RTS bit or the ~RTS input signal are provided. The RRTSE bit enables V.13 signaling. The RTSDE bit enables detection of V.13 patterns. The RTSDT status bit indicates the state of the remote RTS signal. This feature may be used to clamp/unclamp the local ~RLSD and RXD signals in response to a change in the remote RTS signal in order to simulate controlled carrier operation in a constant carrier environment. The MDP automatically clamps and unclamps ~RLSD.

Auto-Dialing and Auto-Answering Control

The host can perform auto-dialing and auto-answering. These functions include DTMF or pulse dialing, ringing detection, and a comprehensive supervisory tone detection scheme. The major parameters are host programmable.

Supervisory Tone Detection

Three parallel tone detectors (A, B, and C) are provided for supervisory tone detection. The signal path to these detectors is separate from the main received signal path.

Each tone detector consists of two cascaded second order IIR biquad filters. The coefficients are host programmable. Each fourth order filter is followed by a level detector which has host programmable turn-on and turn-off thresholds allowing hysteresis. Tone detector C is preceded by a prefilter and squarer. This circuit is useful for detecting a tone with frequency equal to the difference between two tones that may be simultaneously present on the line. The squarer may be disabled by the SQDIS bit causing tone detector C to be an eighth order filter. The tone detectors are disabled in data mode.

The tone detection sample rate is 9600 Hz in V.8 and V.34 modes and is 7200 Hz in non-V.34 modes. The default call progress filter coefficients are based on a 7200 Hz sampling rate and apply to non-V.34 modes only. The maximum detection bandwidth is equal to one-half the sample rate.

The default bandwidths and thresholds of the tone detectors are:

Tone Detector	Bandwidth	Turn-On Threshold	Turn-Off Threshold
A	245 – 650 Hz	–25 dBm	–31 dBm
B	360 – 440 Hz	–25 dBm	–31 dBm
C Prefilter	0 – 500 Hz	N/A	N/A
C	50 – 110 Hz	*	*
* Tone Detector C will detect a difference tone within its bandwidth when the two tones present are in the range –1 dBm to –26 dBm.			

511 Pattern Generation/Detection

In a synchronous mode, a 511 pattern can be generated and detected (control bit S511). Use of this bit pattern during self-test eliminates the need for external test equipment.

In-Band Secondary Channel

A full-duplex in-band secondary channel is provided in V.34 (all speeds) and V.32 bis/V.32 (7200 bps and above) modes. Control bit SECEN enables and disables the secondary channel operation. The secondary channel operates in parallel data mode with independent transmit and receive interrupts and data buffers. The main channel may operate in parallel or serial mode.

In V.34 modes, the secondary channel rate is 200 bps.

In V.32 bis/V.32 modes, the secondary channel rate is 150 bps. This rate is also host programmable in V.32 bis/V.32 modes.

Transmit and Receive FIFO Data Buffers

Two (16+128)-byte first-in first-out (FIFO) data buffers allow the DTE/host to rapidly output up to 144 bytes of transmit data and input up to 144 bytes of accumulated received data. The receiver FIFO is always enabled. The transmitter FIFO is enabled by the FIFOEN control bit. TXHF and RXHF bits operate off the lower 16 bits and indicate the corresponding FIFO buffer half full (8 or more bytes loaded) status. TXFNF and RXFNE bits indicate the TXFIFO buffer not full and RXFIFO buffer not empty status, respectively. An interrupt mask register allows an interrupt request to be generated whenever the TXFNF, RXFNE, RXHF, or TXHF status bit changes state. The 128-byte FIFO extensions are enabled by default and can be disabled by clearing a bit in RAM. (See Section 4, Function 74.)

DMA Support Interrupt Request Lines

DMA support is available in synchronous, asynchronous, and HDLC parallel data modes. Control bit DMAE enables and disables DMA support. When DMA support is enabled, the MDP ~RI and ~DSR lines are assigned to Transmitter Request (TXRQ) and Receiver Request (RXRQ) hardware output interrupt request lines, respectively. The TXRQ and RXRQ signals follow the assertion of the TDBE and RDBF interrupt bits thus allowing the DTE/host to respond immediately to the interrupt request without masking out status bits to determine the interrupt source.

NRZI Encoding/Decoding

NRZI data encoding/decoding may be selected in synchronous and HDLC modes instead of the default NRZ (control bit NRZIEN). In NRZ encoding, a 1 is represented by a high level and a 0 is represented by a low level. In NRZI encoding, a 1 is represented by no change in level and a 0 is represented by a change in level.

ITU-T CRC-32 Support

ITU-T CRC-32 generation/checking may be selected instead of the default ITU-T CRC-16 in HDLC mode using DSP RAM access.

Caller ID Demodulation

Caller ID information can be demodulated in V.23 1200 receive configuration and presented to the host/DTE in serial (RXD) and parallel (RBUFFER) form.

Relay Control. Direct control of the off-hook and talk/data relays is provided. Internal relay drivers allow direct connection to the off-hook (RLYA) and talk/data (RLYB) relays. The talk/data relay output can optionally be used for pulse dial.

Speaker Interface

An analog speaker output (SPK) is provided with on/off and volume control logic incorporated in the MDP. An external amplifier is recommended if driving non-amplified speakers.

A digital speaker output (SPKMD) is provided which reflects the received analog input signal digitized to TTL high or low level by an internal comparator to create a PC Card (PCMCIA)-compatible signal.

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2. HARDWARE INTERFACE

2.1 HARDWARE INTERFACE SIGNALS

The functional interconnect diagram in Figure 2-1 show the typical MDP connections in a system. In these diagrams, any point that is active low is represented by a small circle at the signal point.

Edge triggered inputs are denoted by a small triangle (e.g., TDCLK). An active low signal is indicated by a tilde preceding the signal name (e.g., ~RESET).

A clock intended to activate logic on its rising edge (low-to-high transition) is called active low (e.g., ~RDCLK), while a clock intended to activate logic on its falling edge (high-to-low transition) is called active high (e.g., TDCLK). When a clock input is associated with a small circle, the input activates on a falling edge. If no circle is shown, the input activates on a rising edge.

The 144-pin TQFP MDP hardware interface signals are shown Figure 2-2.

The 144-pin TQFP MDP signal pin assignments are shown Figure 2-3 and are listed in Table 2-1.

The 100-pin PQFP MDP hardware interface signals are shown Figure 2-4.

The 100-pin PQFP MDP signal pin assignments are shown Figure 2-5 and are listed in Table 2-2.

The MDP hardware interface signals are described in Table 2-3.

The digital interface characteristics are defined in Table 2-4.

The analog interface characteristics are defined Table 2-5.

The power requirements are defined in Table 2-6.

The absolute maximum ratings are defined in Table 2-7.

The timing for DTE host microprocessor interface bus waveforms is shown in Table 2-8. The host bus waveforms are illustrated in Figure 2-6.

The DTE serial interface waveforms are illustrated in Figure 2-7.

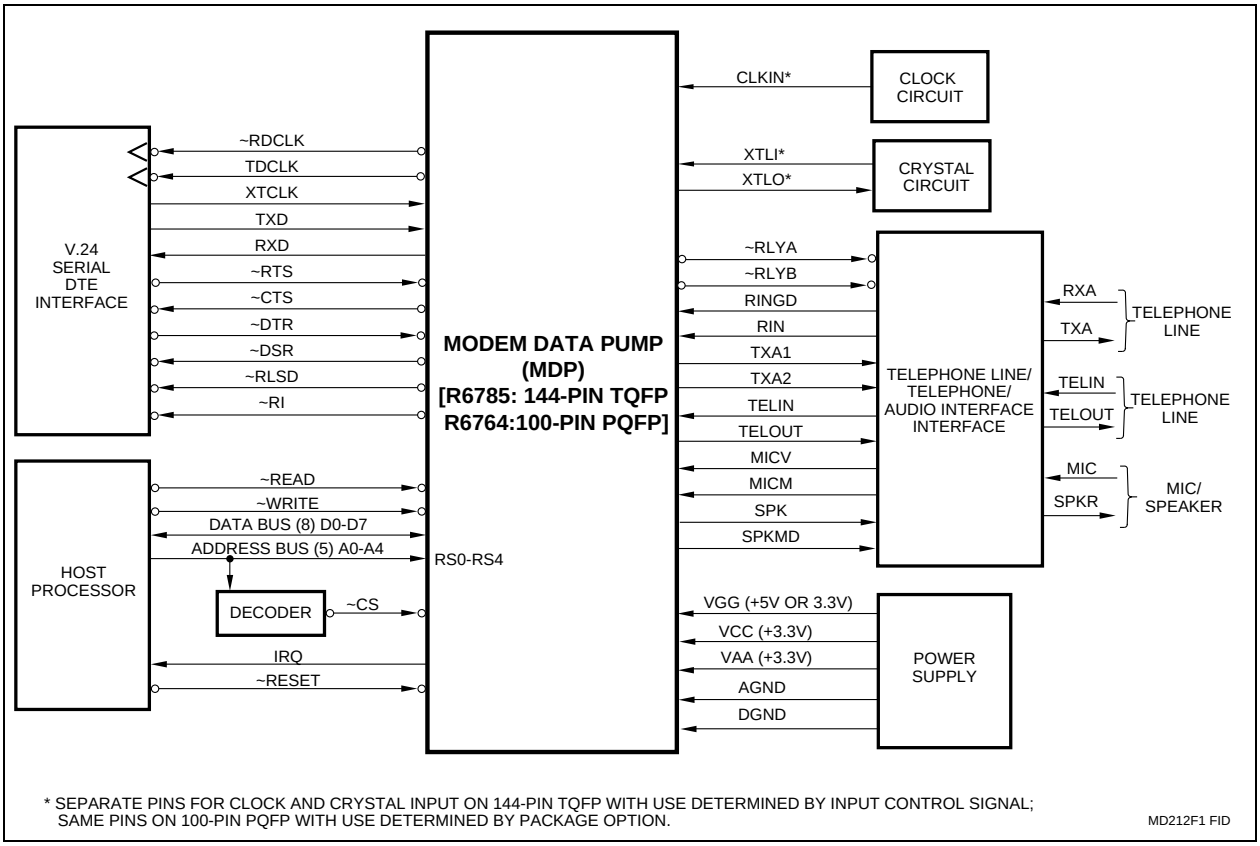


Figure 2-1. MDP Functional Interface Signals

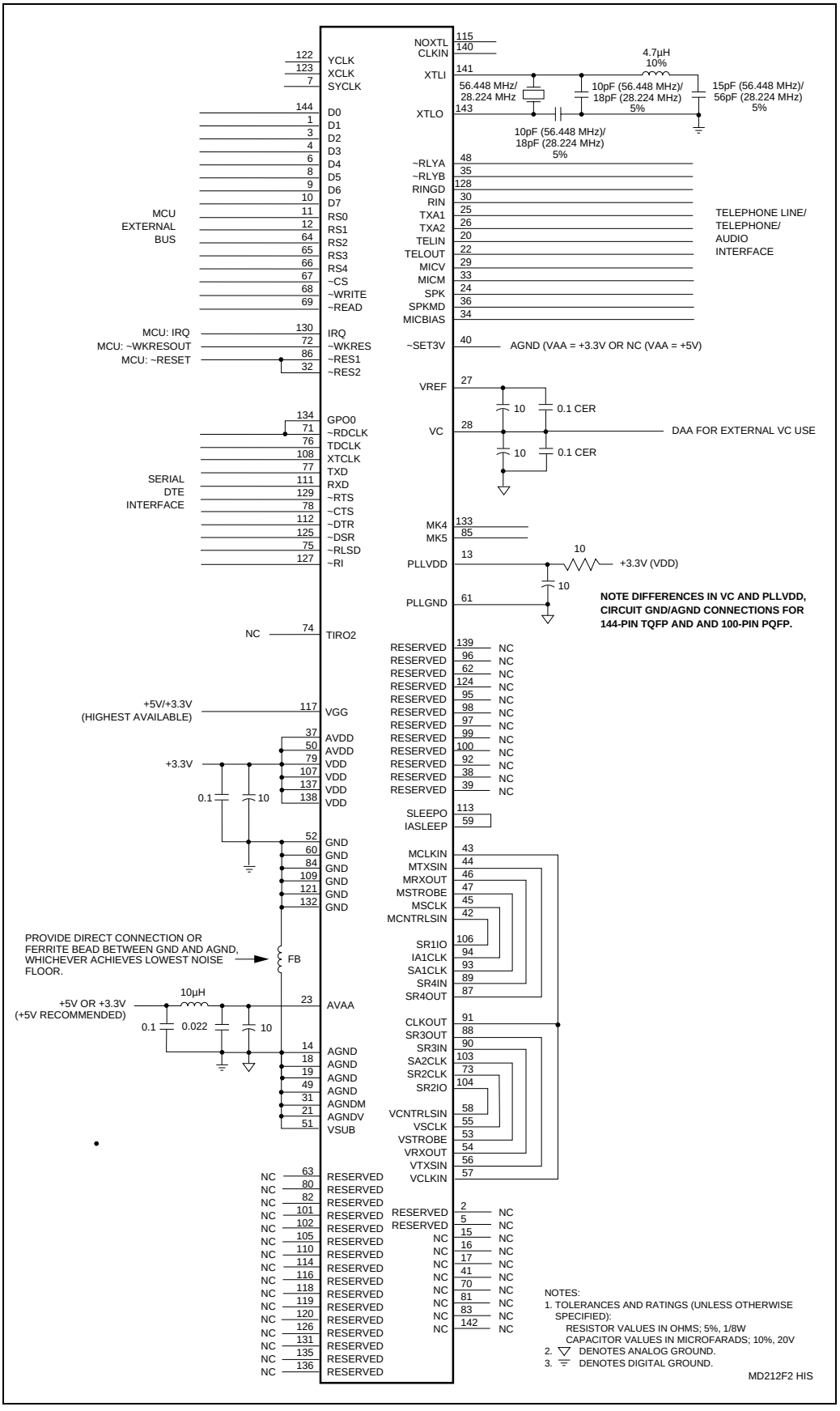


Figure 2-2. MDP Hardware Interface Signals-144-Pin TQFP

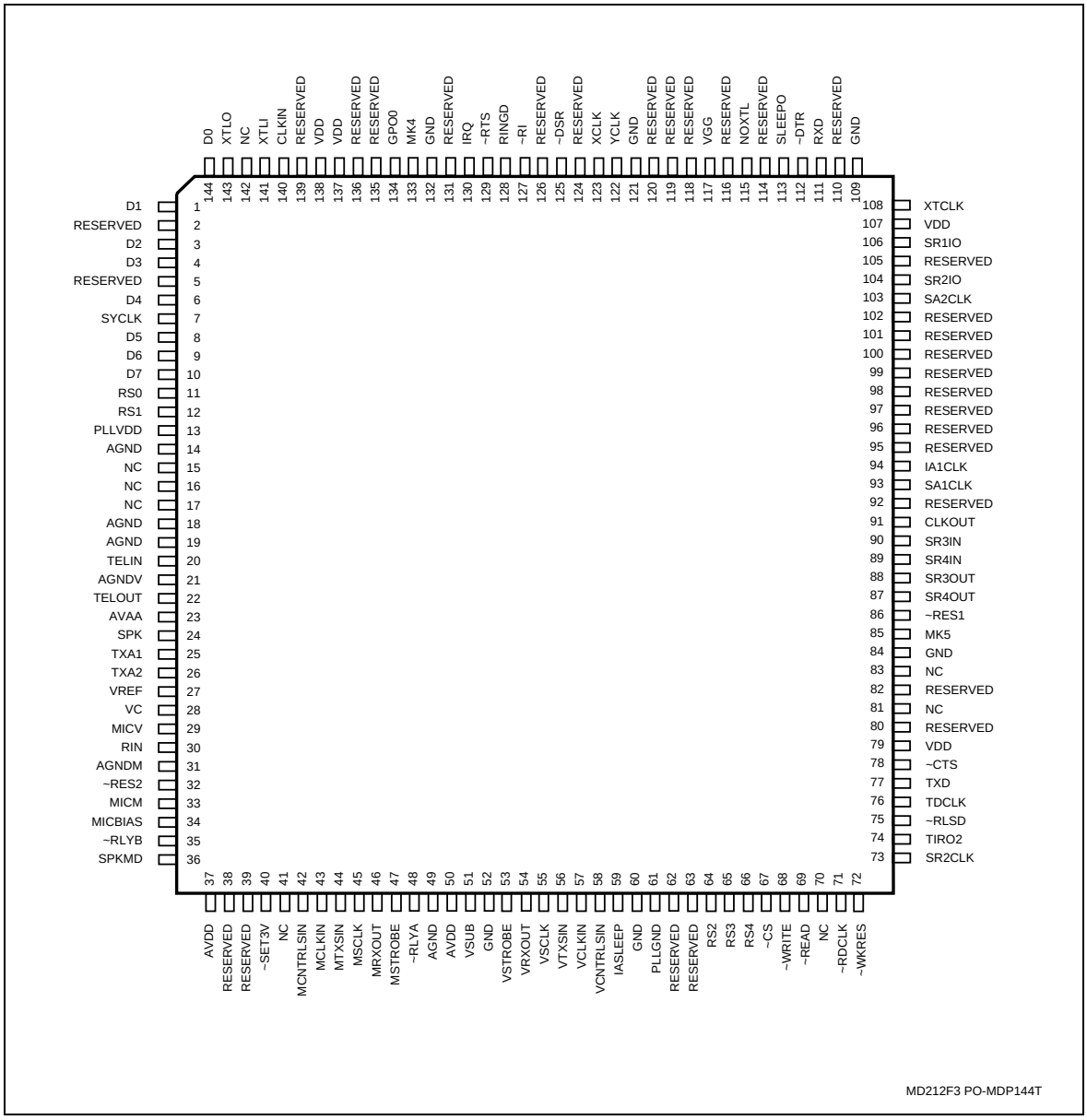


Figure 2-3. MDP Pin Signals - 144-Pin TQFP

Table 2-1. MDP Pin Signals - 144-Pin TQFP

Pin	Signal Label	I/O Type	Interface[3]	Pin	Signal Label	I/O Type	Interface
1	D1	IA/OB	Host Parallel Interface	73	SR2CLK	DI	To VSCLK (55)
2	RESERVED		NC	74	TIRO2	IA	NC
3	D2	IA/OB	Host Parallel Interface	75	~RLSD	OA	DTE Serial Interface
4	D3	IA/OB	Host Parallel Interface	76	TDCLK	OA	DTE Serial Interface
5	RESERVED		NC	77	TXD	IA	DTE Serial Interface
6	D4	IA/OB	Host Parallel Interface	78	~CTS	OA	DTE Serial Interface
7	SYCLK	OA	Controller	79	VDD	PWR	+3.3V
8	D5	IA/OB	Host Parallel Interface	80	RESERVED		NC
9	D6	IA/OB	Host Parallel Interface	81	NC		NC
10	D7	IA/OB	Host Parallel Interface	82	RESERVED		NC
11	RS0	IA	Host Parallel Interface	83	NC		NC
12	RS1	IA	Host Parallel Interface	84	GND	GND	DGND
13	PLLVDD	PLL	To +3.3 (VDD) through 10 Ω and to AGND though10 µF	85	MK5	IA	PLL Circuit Select (Note 4)
14	AGND	GND	AGND	86	~RES1		PIF: ~RESET SIF: Reset circuit
15	NC		NC	87	SR4OUT	DI	To MTXSIN (44)
16	NC		NC	88	SR3OUT	DI	To VTXSIN (56)
17	NC		NC	89	SR4IN	DI	To MRXOUT (46)
18	AGND	GND	AGND	90	SR3IN	DI	To VRXOUT (54)
19	AGND	GND	AGND	91	CLKOUT	DI	To MCLKIN (43) & VCLKIN (57)
20	TELIN	I(DA)	Line/Audio Interface	92	RESERVED		NC
21	AGNDV	GND	AGND	93	SA1CLK	DI	To MSTROBE (47)
22	TELOUT	O(DD)	Line/Audio Interface	94	IA1CLK	DI	To MSCLK (45)
23	AVAA	PWR	+3.3VA or +5VA	95	RESERVED		NC
24	SPK	O(DF)	Line/Audio Interface	96	RESERVED		NC
25	TXA1	O(DD)	Line/Audio Interface	97	RESERVED		NC
26	TXA2	O(DD)	Line/Audio Interface	98	RESERVED		NC
27	VREF	REF	VC through capacitors	99	RESERVED		NC
28	VC	REF	DAA; AGND through capacitors	100	RESERVED		NC
29	MICV	I(DA)	Line/Audio Interface	101	RESERVED		NC
30	RIN	I(DA)	Line/Audio Interface	102	RESERVED		NC
31	AGNDM	GND	AGND	103	SA2CLK	DI	To VSTROBE (53)
32	~RES2		PIF: ~RESET SIF: Reset circuit	104	SR2IO	DI	To VCNTRLSIN (58)
33	MICM	I(DA)	Line/Audio Interface	105	RESERVED		NC
34	MICBIAS		MICBIAS circuit	106	SR1IO	DI	To MCNTRLSIN (42)
35	~RLYB	OD	Line/Audio Interface	107	VDD	PWR	+3.3V
36	SPKMD	OA	Line/Audio Interface	108	XTCLK	IA	DTE Serial Interface
37	AVDD	PWR	+3.3V	109	GND	GND	DGND
38	RESERVED		NC	110	RESERVED		NC
39	RESERVED		NC	111	RXD	OA	DTE Serial Interface
40	~SET3V	IA	AGND (VAA = +3.3V) or NC (VAA = +5V)	112	~DTR	IA	DTE Serial Interface
41	NC		NC	113	SLEEPO	DI	To IASLEEP (59)
42	MCNTRLSIN	DI	To SR1IO (106)	114	RESERVED		NC
43	MCLKIN	DI	To CLKOUT (91)	115	NOXTL	IA	VCC or GND
44	MTXSIN	DI	To SR4OUT (87)	116	RESERVED		NC
45	MSCLK	DI	To IA1CLK (94)	117	VGG	REF	+5V or +3.3V
46	MRXOUT	DI	To SR4IN (89)	118	RESERVED		NC
47	MSTROBE	DI	To SA1CLK (93)	119	RESERVED		NC
48	~RLYA	OD	Line/Audio Interface	120	RESERVED		NC
49	AGND	GND	AGND	121	GND	GND	DGND
50	AVDD	PWR	+3.3V	122	YCLK	OA	NC
51	VSUB	GND	AGND	123	XCLK	OA	NC
52	GND	GND	DGND	124	RESERVED		NC
53	VSTROBE	DI	To SA2CLK (103)	125	~DSR	OA	DTE Serial Interface
54	VRXOUT	DI	To SR3IN (90)	126	RESERVED		NC
55	VSCLK	DI	To SR2CLK (73)	127	~RI	OA	DTE Serial Interface
56	VTXSIN	DI	To SR3OUT (88)	128	RINGD	IA	Line/Audio Interface
57	VCLKIN	DI	To CLKOUT (91)	129	~RTS	IA	DTE Serial Interface
58	VCNTRLSIN	DI	To SR2IO (104)	130	IRQ	IA	Host Parallel Interface
59	IASLEEP	DI	To SLEEPO (113)	131	RESERVED		NC
60	GND	GND	DGND	132	GND	GND	DGND

Table 2-1. MDP Pin Signals - 144-Pin TQFP (Cont'd)

Pin	Signal Label	I/O Type	Interface3	Pin	Signal Label	I/O Type	Interface
61	PLLGND	PLL	AGND	133	MK4	IA	PLL Circuit Select (Note 4)
62	RESERVED		NC	134	GPO0	DI	To ~RDCLK (71)
63	RESERVED		NC	135	RESERVED		NC
64	RS2	IA	Host Parallel Interface	136	RESERVED		NC
65	RS3	IA	Host Parallel Interface	137	VDD	PWR	+3.3V
66	RS4	IA	Host Parallel Interface	138	VDD	PWR	+3.3V
67	~CS	IA	Host Parallel Interface	139	RESERVED		NC
68	~WRITE	IA	Host Parallel Interface	140	CLKIN	IA	Clock Circuit
69	~READ	IA	Host Parallel Interface	141	XTLI	I	Crystal Circuit
70	NC		NC	142	NC		NC
71	~RDCLK	OA	DTE Serial Interface	143	XTLO	O	Crystal Circuit
72	~WKRES	IA	MCU: READY/~WKRESOUT	144	D0	IA/OB	Host Parallel Interface

Notes:

1. I/O types:
   IA, IB = Digital input; OA, OB = Digital output.
   I(DA) = Analog input; O(DD), O(DF) = Analog output.
   DI = Device interconnect.
2. NC or RESERVED = No external connection allowed (may have internal connection).
3. Interface Legend:
   MDP = Modem Data Pump
   DTE = Data Terminal Equipment
   PIF = Parallel host interface
   SIF = Serial DTE interface.
4. An internal 55 kΩ pullup resistor is connected to this pin.

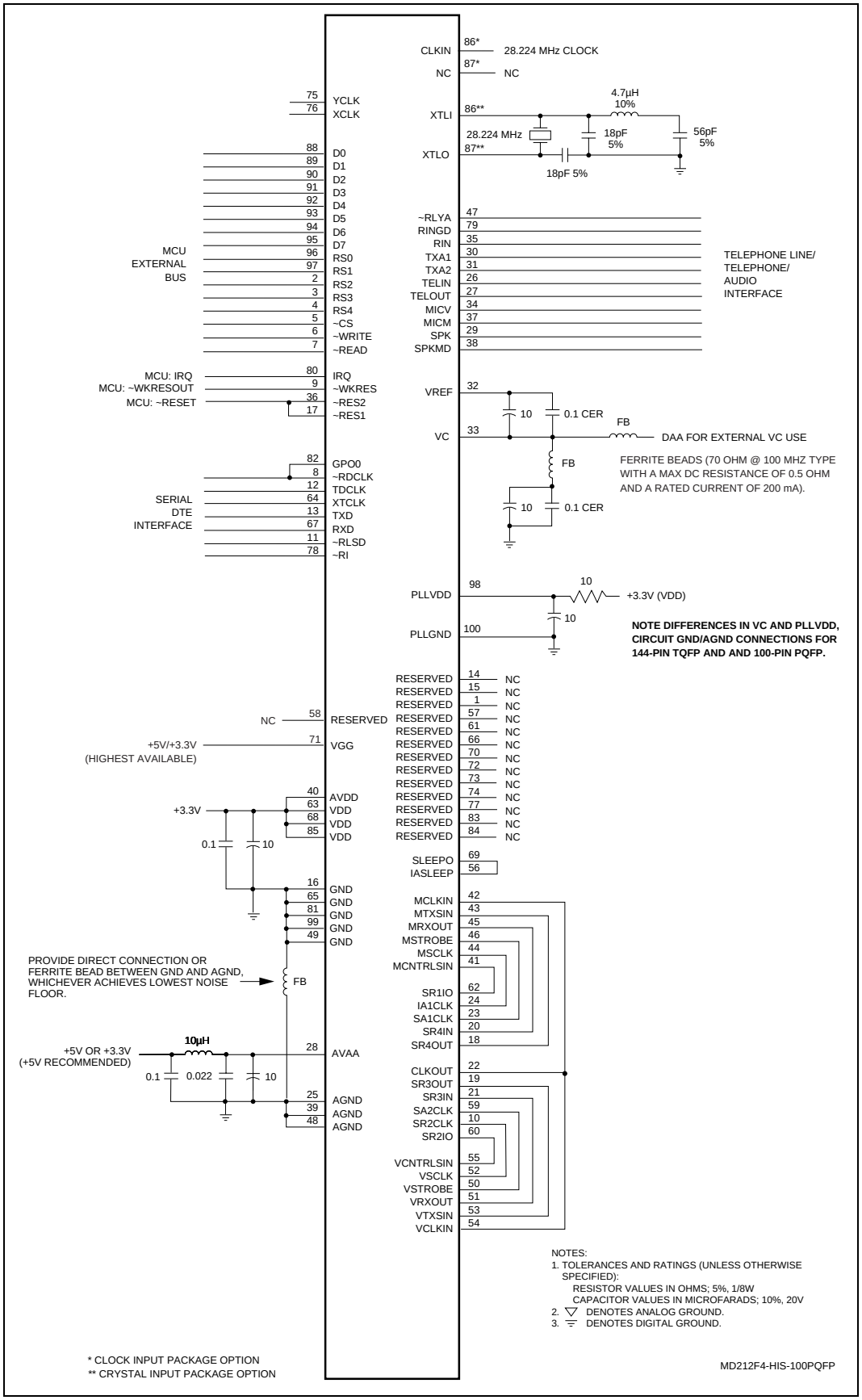


Figure 2-4. MDP Hardware Interface Signals-100-Pin PQFP

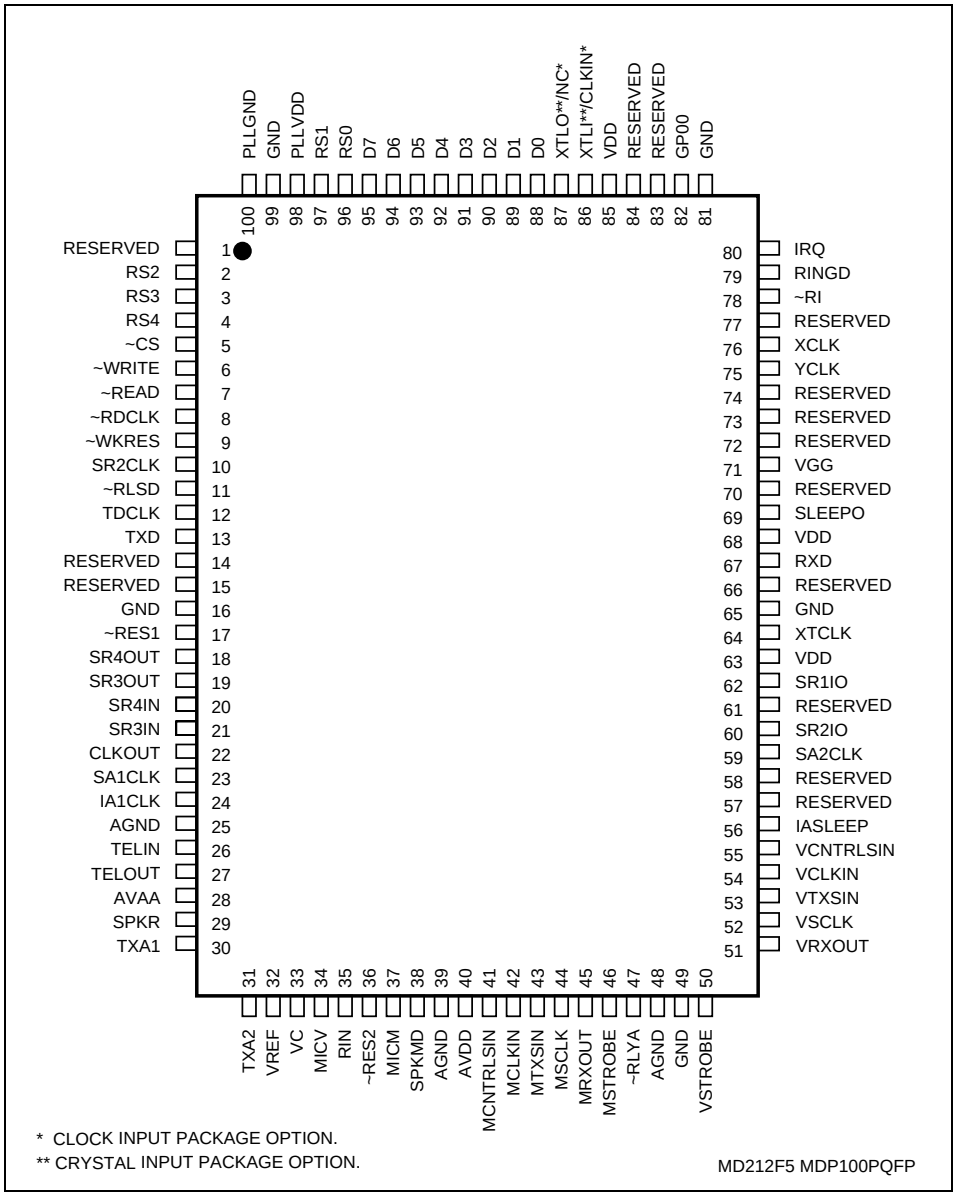


Figure 2-5. MDP Pin Signals - 100-Pin PQFP

Table 2-2. MDP Pin Signals - 100-Pin PQFP

Pin	Signal Label	I/O Type	Interface[3]	Pin	Signal Label	I/O Type	Interface
1	RESERVED		NC	51	VRXOUT	DI	To SR3IN (21)
2	RS2	IA	Host Parallel Interface	52	VSCLK	DI	To SR2CLK (10)
3	RS3	IA	Host Parallel Interface	53	VTXSIN	DI	To SR3OUT (19)
4	RS4	IA	Host Parallel Interface	54	VCLKIN	DI	To CLKOUT (22)
5	~CS	IA	Host Parallel Interface	55	VCNTRLSIN	DI	To SR2IO (60)
6	~WRITE	IA	Host Parallel Interface	56	IASLEEP	DI	To SLEEPO (69)
7	~READ	IA	Host Parallel Interface	57	RESERVED		NC
8	~RDCLK	OA	DTE Serial Interface	58	RESERVED		NC
9	~WKRES	IA	MCU: READY/~WKRESOUT	59	SA2CLK	DI	To VSTROBE (50)
10	SR2CLK	DI	To VSCLK (52)	60	SR2IO	DI	To VCNTRLSIN (55)
11	~RLSD	OA	DTE Serial Interface	61	RESERVED		NC
12	TDCLK	OA	DTE Serial Interface	62	SR1IO	DI	To MCNTRLSIN (41)
13	TXD	IA	DTE Serial Interface	63	VDD	PWR	+3.3V
14	RESERVED		NC	64	XTCLK	IA	DTE Serial Interface
15	RESERVED		NC	65	GND	GND	DGND
16	GND	GND	DGND	66	RESERVED		NC
17	~RES1		PIF: ~RESET SIF: Reset circuit	67	RXD	OA	DTE Serial Interface
18	SR4OUT	DI	To MTXSIN (43)	68	VDD	PWR	+3.3V
19	SR3OUT	DI	To VTXSIN (53)	69	SLEEPO	DI	To IASLEEP (56)
20	SR4IN	DI	To MRXOUT (45)	70	RESERVED		NC
21	SR3IN	DI	To VRXOUT (51)	71	VGG	REF	+5V or +3.3V
22	CLKOUT	DI	To MCLKIN (42) & VCLKIN (54)	72	RESERVED		NC
23	SA1CLK	DI	To MSTROBE (46)	73	RESERVED		NC
24	IA1CLK	DI	To MSCLK (44)	74	RESERVED		NC
25	AGND	GND	Analog Ground	75	YCLK	OA	NC
26	TELIN	I(DA)	Line/Audio Interface	76	XCLK	OA	NC
27	TELOUT	O(DD)	Line/Audio Interface	77	RESERVED		NC
28	AVAA	PWR	+3.3VA or +5VA	78	~RI	OA	DTE Serial Interface
29	SPK	O(DF)	Line/Audio Interface	79	RINGD	IA	Line/Audio Interface
30	TXA1	O(DD)	Line/Audio Interface	80	IRQ	IA	Host Parallel Interface
31	TXA2	O(DD)	Line/Audio Interface	81	GND	GND	DGND
32	VREF	REF	VC through capacitors	82	GPO0	DI	To ~RDCLK (8)
33	VC	REF	DAA through FB; GND through capacitors and FB	83	RESERVED		NC
34	MICV	I(DA)	Line/Audio Interface	84	RESERVED		NC
35	RIN	I(DA)	Line/Audio Interface	85	VDD	PWR	+3.3V
36	~RES2		PIF: ~RESET SIF: Reset circuit	86	XTLI/CLKIN (Note 4)	I	Crystal Circuit/Clock Circuit
37	MICM	I(DA)	Line/Audio Interface	87	XTLO/NC (Note 4)	O/NC	Crystal Circuit/NC
38	SPKMD	OA	Line/Audio Interface	88	D0	IA/OB	Host Parallel Interface
39	AGND	GND	Analog Ground	89	D1	IA/OB	Host Parallel Interface
40	AVDD	PWR	+3.3V	90	D2	IA/OB	Host Parallel Interface
41	MCNTRLSIN	DI	To SR1IO (62)	91	D3	IA/OB	Host Parallel Interface
42	MCLKIN	DI	To CLKOUT (22)	92	D4	IA/OB	Host Parallel Interface
43	MTXSIN	DI	To SR4OUT (18)	93	D5	IA/OB	Host Parallel Interface
44	MSCLK	DI	To IA1CLK (24)	94	D6	IA/OB	Host Parallel Interface
45	MRXOUT	DI	To SR4IN (20)	95	D7	IA/OB	Host Parallel Interface
46	MSTROBE	DI	To SA1CLK (23)	96	RS0	IA	Host Parallel Interface
47	~RLYA	OD	NC	97	RS1	IA	Host Parallel Interface
48	AGND	GND	AGND	98	PLLVDD	PLL	To +3.3 (VDD) through 10 Ω and to DGND through 10 µF.
49	GND	GND	DGND	99	GND	GND	DGND
50	VSTROBE	DI	To SA2CLK (59)	100	PLLGND	PLL	DGND

Table 2-2. MDP Pin Signals - 100-Pin PQFP (Cont'd)

Notes:

1. I/O types:
   IA, IB = Digital input; OA, OB = Digital output;
   I(DA) = Analog input; O(DD), O(DF) = Analog output.
   DI = Device interconnect.
2. NC = No external connection allowed (may have internal connection).
3. Interface Legend:
   MDP = Modem Data Pump
   DTE = Data Terminal Equipment
   PIF = Parallel host interface
   SIF = Serial DTE interface.
4. Package option.

Table 2-3. MDP Signal Definitions

Label	I/O Type	Signal/Definition
OVERHEAD SIGNALS		
CLKIN	IA	**Clock In (144-Pin TQFP).** If external clock is selected (NOXTL = low), connect to an external 56.448 MHz or 28.224 MHz clock circuit. The clock frequency is selected by the MK4 and MK5 inputs.
XTLI	I	**Crystal In (144-Pin TQFP).** If external crystal is selected (NOXTL = high), connect to an external 56.448 MHz or 28.224 MHz crystal circuit. The clock frequency is selected by the MK4 and MK5 inputs.
XTLO	O	**Crystal Out (144-Pin TQFP).** If external crystal is selected (NOXTL = high), connect to the external crystal circuit return.
NOXTL	IA	**No Crystal Circuit (144-Pin TQFP).** Selects external crystal (NOXTL = high, i.e., leave open or connect to VDD through 10kΩ) or clock (NOXTL = low, i.e., connect to GND) circuit. Internal pull-up provided.
XTLI/CLKIN	I	**Crystal In/Clock In (100-Pin PQFP).** Connect to an external 56.448 MHz/28.224 MHz crystal circuit (crystal input option) or to an external 56.448 MHz/28.224 MHz clock circuit (clock input option).
XTLO/NC	O	**Crystal Out/NC (100-Pin PQFP).** Connect to the external crystal circuit return (crystal input option) or leave open (clock input option).
~RES1, ~RES2	IA	**Reset.** ~RESET low holds the MDP in the reset state. ~RESET going high releases the MDP from the reset state and initiates normal operation using power turn-on (default) values. ~RESET must be held low for at least 3 µs. The MDP is ready to use 400 ms after the low-to-high transition of ~RESET. ~RES1 and ~RES2 are typically connected to the MCU ~RESET input and to the host bus ~RESET (or RESET through an inverter) line (parallel host) or reset circuit (serial DTE interface) which resets both the MCU and MDP upon power turn-on. ~RES1 and ~RES2 have active internal pull-up resistors.
~WKRES	IA	**Wake-up Reset.** ~WKRES is connected internally to ~RESET but will not drive the MDP ~RESET pins. Asserting ~WKRES performs the same reset function as the MDP ~RESET and typically used by the MCU to wake up the MDP from SLEEP Mode when the MDP ~RESET lines cannot be asserted (because they are also connected to the MCU ~RESET input). For a serial DTE or parallel host MCU configuration, connect ~WKRES to the MCU ~WKRESOUT output. ~WKRES has an active internal pull-up resistor.
VDD	PWR	**+3.3V Digital Circuit Power Supply.** Connect to +3.3V through digital circuit power supply filter.
AVDD	PWR	**+3.3V Analog Circuit Digital Power Supply.** Connect to +3.3V through digital circuit power supply filter
AVAA	PWR	**Analog Circuit Analog Power Supply.** Connect to +3.3V or +5V (preferred) through analog circuit power supply filter. **Note:** When operating the analog circuitry at +3.3V, the transmit level is 4 dB lower and the converted receive level is 4 dB higher when compared to operating the analog circuitry at +5V. The transmit level must be adjusted accordingly using TLVL or other means.
VGG	REF	**Input Reference Voltage.** Reference voltage for +5V tolerant input pins. Connect to the highest of +3.3V or +5V available on the circuit board. A connection to +5V allows +5V or +3.3V input levels. A connection to +3.3V allows +3.3V input levels only.
GND	GND	**Digital Ground.** Connect to digital ground.
AGND	GND	**Analog Ground.** Connect to analog ground.
XCLK	OA	**X Clock.** Output clock at 56.448 MHz which runs during MDP Normal Mode and is turned off during Sleep Mode.
YCLK	OA	**Y Clock.** Output clock at 28.224 MHz which runs during MDP Normal Mode and is turned off during Sleep Mode.
SYCLK	OA	**System Clock.** Output clock at 28.224 MHz which runs during MDP Normal Mode and during Sleep Mode.
PLLVDD	PLL	**PLLVDD Connection.** For the 144-pin TQFP, connect to +3.3V (VDD) through 10 Ω and to AGND through 10 (+) µF, For the 100-pin PQFP, connect to +3.3V (VDD) through 10 Ω and to DGND through 10 (+) µF.
PLLGND	PLL	**PLLGND Connection.** For the 144-pin TQFP, connect to AGND. For the 100-pin PQFP, connect to DGND.
~SET3V	IA	**Set Integrated Analog +3.3V Reference.** Selects analog circuit voltage reference: High (NC) = +5V, low (AGND) = +3.3V.
MK4	IA	**PLL Circuit Enable/Disable (144-Pin TQFP).** This pin disables (MK4 = high) or enables (MK4 = low) the internal PLL circuit. Connect this pin to GND to enable the PLL circuit. Internal pull-up provided. See MK5. Note: The 100-pin PQFP is internally bonded to enable the internal PLL.
MK5	IA	**PLL Circuit Frequency Select (144-Pin TQFP).** This pin selects the input frequency (MK5 high = 28.224 MHz, MK5 low = 56.448 MHz) when the internal PLL circuit is enabled (MK4 = low). MK5 has no effect when the PLL circuit is disabled (MK4 = high). Internal pull-up provided. See MK4. Note: The 100-pin PQFP is internally bonded to select a 28.224 MHz input frequency.

Table 2-3. MDP Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
PARALLEL HOST INTERFACE		
Address, data, control, and interrupt hardware interface signals allow MDP connection to an 8086-compatible microprocessor bus. With the addition of external logic, the interface can be made compatible with a wide variety of other microprocessors such as the 6502, 8086 or 68000. The microprocessor interface allows a microprocessor to change MDP configuration, read or write channel and diagnostic data, and supervise MDP operation by writing control bits and reading status bits.		
D0–D7	IA/OB	**Data Lines.** Eight bidirectional data lines (D0–D7) provide parallel transfer of data between the host and the MDP. The most significant bit is D7. Data direction is controlled by the Read Enable and Write Enable signals.
RS0–RS4	IA	**Register Select Lines.** The five active high register select lines (RS0–RS4) address interface memory registers within the MDP interface memory. These lines are typically connected to the five least significant lines (A0–A4) of the address bus. The MDP decodes RS0 through RS4 to address one of 32 internal interface memory registers (00–1F). The most significant address bit is RS4, while the least significant address bit is RS0. The selected register can be read from or written into via the 8-bit parallel data bus (D0–D7). The most significant data bit is D7, while the least significant data bit is D0.
~CS	IA	**Chip Select.** ~CS selects the MDP for microprocessor bus operation. ~CS is typically generated by decoding host address bus lines.
~READ	IA	**Read Enable.** During a read cycle (~READ asserted), data from the selected interface memory register is gated onto the data bus by means of three-state drivers in the MDP. These drivers force the data lines high for a one bit, or low for a zero bit. When not being read, the three-state drivers assume their high-impedance (off) state.
~WRITE	IA	**Write Enable.** During a write cycle (~WRITE asserted), data from the data bus is copied into the selected MDP interface memory register, with high and low bus levels representing one and zero bit states, respectively.
IRQ	OA	I**nterrupt Request.** The MDP IRQ output may be connected to the host processor interrupt request input in order to interrupt host program execution for immediate MDP service. The IRQ output can be enabled in the MDP interface memory to indicate immediate change of conditions. The use of IRQ is optional depending upon MDP application. The IRQ output is driven by a TTL-compatible CMOS driver.

Table 2-3. MDP Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
DTE SERIAL INTERFACE		
Timing, data, control, and status signals provide a V.24-compatible serial interface. These signals are TTL compatible in order to drive the short wire lengths and circuits normally found within a printed circuit board, stand-alone modem enclosures, or equipment cabinets. For driving longer cables, these signals can be easily converted to EIA/RS-232-D voltage levels.		
TXD	IA	**Transmitted Data.** The MDP obtains serial data to be transmitted from the local DTE on the Transmitted Data (TXD) input.
RXD	OA	**Received Data.** The MDP presents received serial data to the local DTE on the Received Data (RXD) output.
~RTS	IA	**Request to Send.** Activating ~RTS causes the MDP to transmit data on TXD when ~CTS becomes active. The ~RTS pin is logically ORed with the RTS bit.
~CTS	OA	**Clear To Send.** ~CTS active indicates to the local DTE that the MDP will transmit any data present on TXD. CTS response times from an active condition of RTS are shown in **Error! Reference source not found.**.
~RLSD	OA	**Received Line Signal Detector.** ~RLSD active indicates to the local DTE that energy above the receive level threshold is present on the receiver input, and that the energy is not a training sequence. One of four ~RLSD receive level threshold options can be selected (RTH bits). A minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold level and hysteresis action are measured with a modulated signal applied to the Receiver Analog (RXA) input. Note that performance may be degraded when the received signal level is less than -43 dBm. The ~RLSD on and off thresholds are host programmable in DSP RAM.
~DTR	IA	**Data Terminal Ready.** In V.8, K56flex, V.34, V.32 bis, V.32, V.22 bis, V.22, or Bell 212A configuration, activating ~DTR initiates the handshake sequence. The DATA bit must be set to complete the handshake. In V.21, V.23, or Bell 103 configuration, activating ~DTR causes the MDP to enter the data state provided that the DATA bit is a 1. If in answer mode, the MDP immediately sends answer tone. In these modes, if controlled carrier is enabled, carrier is controlled by RTS. During the data mode, deactivating ~DTR causes the transmitter and receiver to turn off and return to the idle state. The ~DTR input and the DTR control bit are logically ORed.
~DSR	OA	**Data Set Ready.** ~DSR ON indicates that the MDP is in the data transfer state. ~DSR OFF indicates that the DTE is to disregard all signals appearing on the interchange circuits except Ring Indicator (~RI). ~DSR is OFF when the MDP is in a test mode (i.e., local analog or remote digital loopback). The DSR status bit reflects the state of the ~DSR output.
~RI	OA	**Ring Indicator.** ~RI output follows the ringing signal present on the line with a low level (0 V) during the ON time, and a high level (+3.3V) during the OFF time coincident with the ringing signal. The RI status bit reflects the state of the ~RI output.
TDCLK	OA	**Transmit Data Clock.** The MDP outputs a synchronous Transmit Data Clock (TDCLK) for USRT timing. The TDCLK frequency is the data rate (±0.01%) with a duty cycle of 50±1%. The TDCLK source can be internal, external (input on XTCLK), or slave (to ~RDCLK) as selected by TXCLK bits in interface memory.
XTCLK	IA	**External Transmit Clock.** In synchronous communication, an external transmit data clock can be connected to the MDP XTCLK input. The clock supplied at XTCLK must exhibit the same characteristics as TDCLK. The XTCLK input is then reflected at the TDCLK output.
~RDCLK	OA	**Receive Data Clock.** The MDP outputs a synchronous Receive Data Clock (~RDCLK) for USRT timing. The ~RDCLK frequency is the data rate (±0.01%) with a duty cycle of 50±1%. The ~RDCLK low-to-high transitions coincide with the center of the received data bits.

Table 2-3. MDP Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
TELEPHONE LINE/TELEPHONE/AUDIO INTERFACE SIGNALS AND REFERENCE VOLTAGE		
TXA1, TXA2	O(DF)	**Transmit Analog 1 and 2 Output.** The TXA1 and TXA2 outputs are differential outputs 180 degrees out of phase with each other. Each output can drive a 300 Ω load. Typically, TXA1 and TXA2 are connected to the telephone line interface or an optional external hybrid circuit.
RIN	I(DA)	**Receive Analog Input.** RIN is a single-ended input with 70K Ω input impedance. Typically, RIN is connected to telephone line interface or an optional external hybrid circuit. **NOTE: If not used, do not tie directly to ground; this input has a bias voltage of +1.35V (VAA = +3.3V) or +2.5V (VAA = +5V).**
RINGD	IA	**Ring Detect.** The RINGD input is monitored for pulses in the range of 15 Hz to 68 Hz. The frequency detection range may be changed by the host in DSP RAM. The circuit driving RINGD should be a 4N35 optoisolator or equivalent. The circuit driving RINGD should not respond to momentary bursts of ringing less than 125 ms in duration, or less than 40 VRMS (15 Hz to 68 Hz) across TIP and RING. Detected ring signals are reflected on the ~RI output signal as well as the RI bit.
~RLYA (~OHRC, ~CALLID)	OD	**Relay A Control.** The ~RLYA open drain output can directly drive a reed relay coil with a minimum resistance of 360 ohms (9.2 mA max. @ +3.3V). A clamp diode, such as a 1N4148, should be installed across the relay coil. An external transistor can be used to drive heavier loads (e.g., electro-mechanical relays). ~RLYA is controlled by host setting/resetting of the RA bit. In a typical application, ~RLYA is connected to the normally open Off-Hook relay (~OHRC). In this case, ~RLYA active closes the relay to connect the MDP to the telephone line. Alternatively, in a typical application, ~RLYA is connected to the normally open Caller ID relay (~CALLID). When the MDP detects a Calling Number Delivery (CND) message, the ~RLYA output is asserted to close the Caller ID relay in order to AC couple the CND information to the MDP RIN input (without closing the off-hook relay and allowing loop current flow which would indicate an off-hook condition).
~RLYB (~TALK)	OD	**Relay B Control.** The ~RLYB open drain output can directly drive a reed relay coil with a minimum resistance of 360 ohms (9.2 mA max. @ 3.3V). A clamp diode, such as a 1N4148, should be installed across the relay coil. An external transistor can be used to drive heavier loads (e.g., electro-mechanical relays). ~RLYB is controlled by host setting/resetting of the RB bit. In a typical application, ~RLYB is connected to the normally closed Talk/Data relay (~TALK). In this case, ~RLYB active opens the relay to disconnect the handset from the telephone line.
MICM	I(DA)	**Modem Microphone Input.** MICM is a single-ended microphone input. The input impedance is > 70k Ω. **NOTE: If not used, do not tie directly to ground; this input has a bias voltage of +1.35V (VAA = +3.3V) or +2.5V (VAA = +5V).**
SPK	O(DF)	**Speaker Analog Output.** The SPK analog output can originate from one of five different sources: RIN, TELIN, MICM or MICV or from the MDP's internal voice playback mode. The SPK on/off and three levels of attenuation are controlled by bits in DSP RAM. When the speaker is turned off, the SPK output is clamped to the voltage at the VC pin. The SPK output can drive an impedance as low as 300 ohms. In a typical application, the SPK output is an input to an external LM386 audio power amplifier.
SPKMD	OA	**Modem Speaker Digital Output.** The SPKMD digital output reflects the received analog input signal digitized to TTL high or low level by an internal comparator to create a PC Card (PCMCIA)-compatible signal.
VREF	REF	**High Voltage Reference.** Connect to VC through 10 µF (polarized, + terminal to VREF) and 0.1 µF (ceramic) in parallel.
VC	REF	**Low Voltage Reference.** For the 144-pin TQFP, connect to AGND through 10 µF (polarized, + terminal to VC) and 0.1 µF (ceramic) in parallel. For the 100-pin PQFP, connect to a ferrite bead and connect the other end of the ferrite bead to DGND through 10 µF (polarized, + terminal to VC) and 0.1 µF (ceramic) in parallel.
MICV	I(DA)	**Voice Microphone Input.** MICV is a single-ended microphone input. Typically, MICV is connected to a microphone output for recording voice e.g., in a speakerphone application. **NOTE: If not used, do not tie directly to ground; this input has a bias voltage of +1.35V (VAA = +3.3V) or +2.5V (VAA = +5V).**
TELIN	I(DA)	**Telephone Analog Input.** TELIN is a single-ended input with 70K Ω input impedance. Typically, TELIN is connected to a telephone handset microphone circuit. **NOTE: If not used, do not tie directly to ground; this input has a bias voltage of +1.35V (VAA = +3.3V) or +2.5V (VAA = +5V).**
TELOUT	O(DF)	**Telephone Analog Output.** TELOUT is a single-ended output that can drive a 300 Ω load. Typically, TELOUT is connected to a telephone handset speaker circuit.
MICBIAS	REF	**Microphone Bias.** Microphone bias reference voltage.

Table 2-3. MDP Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
MISCELLANEOUS		
TIRO2	IA	NC
RESERVED		Reserved Function. May be connected to internal circuit. Leave open.
MODEM INTERCONNECT		
GPO0	DI	To ~RDCLK.
SLEEPO	DI	To IASLEEP.
IASLEEP	DI	To SLEEPO.
MSCLK	DI	To IA1CLK.
CLKOUT	DI	To MCLKIN & VCLKIN.
SR1IO	DI	To MCNTRLSIN.
SR3IN	DI	To VRXOUT.
IA1CLK	DI	To MSCLK.
SA1CLK	DI	To MSTROBE.
SR4OUT	DI	To MTXSIN.
MCLKIN	DI	To CLKOUT.
VCLKIN	DI	To CLKOUT.
MSTROBE	DI	To SA1CLK.
VSTROBE	DI	To SA2CLK.
MCNTRLSIN	DI	To SR1IO.
VSCLK	DI	To SR2CLK.
VCNTRLSIN	DI	To SR2IO.
MRXOUT	DI	To SR4IN.
VTXSIN	DI	To SR3OUT.
VRXOUT	DI	To SR3IN
MTXSIN	DI	To SR4OUT.
SR2IO	DI	To VCNTRLSIN.
SR4IN	DI	To MRXOUT.
SR2CLK	DI	To VSCLK.
SA2CLK	DI	To VSTROBE.
SR3OUT	DI	To VTXSIN.

Table 2-4. Digital Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions[1]
Input High Voltage	V_{IH}				Vdc	
Type IA		2.0	–	V_{CC}		
Input High Current	I_{IH}	–	–	40	µA	
Input Low Voltage	V_{IL}	0.3		0.8	VDC	
Input Low Current	I_{IL}	–	–	40	µA	
Input Leakage Current	I_{IN}	–	–	±100	µADC	V_{IN} = 0 to +3.3V, V_{CC} = 3.6V
Output High Voltage	V_{OH}		–	–	VDC	
Type OA		2.4	–	V_{CC}		I_{LOAD} = – 100 µA
Type OD						I_{LOAD} = 0 mA
Output Low Voltage	V_{OL}				VDC	
Type OA		–	–	0.4		I_{LOAD} = 1.6 mA
Type OD		–	–	0.75		I_{LOAD} = 15 mA
Three-State (Off) Current	I_{TSI}			±10	µADC	V_{IN} = 0.4 to V_{CC}-1

Table 2-5. Analog Electrical Characteristics

Signal Name	Type	Characteristic	Value
RIN, TELIN, MICM, MICV	I (DA)	Input Impedance	> 70K Ω
		AC Input Voltage Range	1.1 VP-P
		Reference Voltage	+1.35 VDC (VAA = +3.3V) or +2.5 VDC (VAA = +5V)
TXA1, TXA2, TELOUT	O (DD)	Minimum Load	300 Ω
		Maximum Capacitive Load	0 µF
		Output Impedance	10 Ω
		AC Output Voltage Range	1.4 VP-P (VAA = +3.3V) or 2.2 VP-P (VAA = +5V) (with reference to ground and a 600 Ω load)
		Reference Voltage	+1.35 VDC (VAA = +3.3V) or +2.5 VDC (VAA = +5V)
		DC Offset Voltage	± 200 mV
SPK	O (DF)	Minimum Load	300 Ω
		Maximum Capacitive Load	0.01 µF
		Output Impedance	10 Ω
		AC Output Voltage Range	1.4 VP-P (VAA = +3.3V) or 2.2 VP-P (VAA = +5V)
		Reference Voltage	+1.35 VDC (VAA = +3.3V) or +2.5 VDC (VAA = +5V)
		DC Offset Voltage	± 20 mV

Table 2-6. Current and Power Requirements

Mode	Typical Current (mA)	Maximum Current (mA)	Typical Power (mW)	Maximum Power (mW)	Notes
Normal Mode	75	84	250	300	f = 28.224 MHz
Sleep Mode	10	—	33	—	f = 28.224 MHz
Stop Mode	<0.3	—	<1	—	f = 0 MHz

Notes:

1. Operating voltage: VDD = +3.3V ± 0.3V.
2. Test conditions: VDD = +3.3V for typical values; VDD = +3.6V for maximum values.
3. Input Ripple ≤ 0.1 Vpeak-peak.
4. f = Internal frequency.
5. Stop Mode is the same as Sleep Mode with clocks turned off.

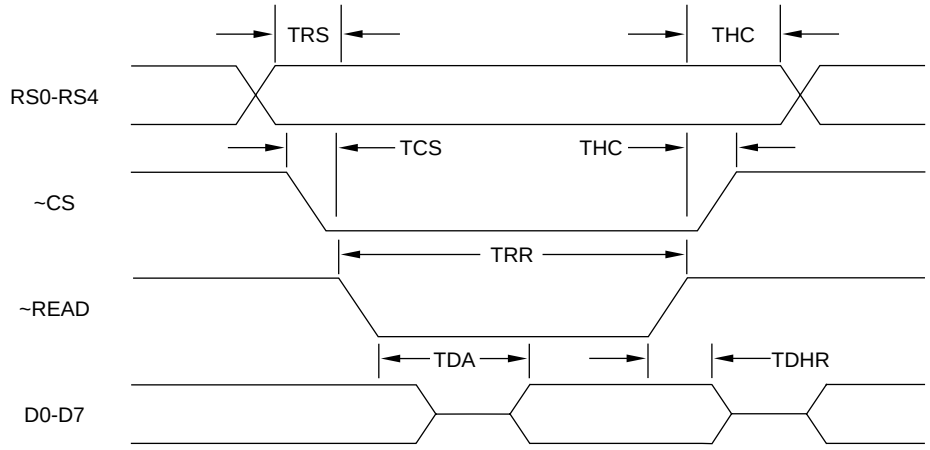
Table 2-7. Absolute Maximum Ratings

Parameter	Symbol	Limits	Units
Supply Voltage	V_{DD}	-0.5 to +4.6	V
Input Voltage	V_{IN}		V
Except XTLI		-0.5 to (VGG +0.5)*	
XTLI		-0.5 to 3.9V	
Operating Temperature Range	T_A	-0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +70	°C
Analog Inputs	V_{IN}	-0.3 to (VAA + 0.5)	V
Voltage Applied to Outputs in High Impedance (Off) State	V_{HZ}	-0.5 to (VGG +0.5)*	V
DC Input Clamp Current	I_{IK}	±20	mA
DC Output Clamp Current	I_{OK}	±20	mA
Static Discharge Voltage (25°C)	V_{ESD}	±2500	V
Latch-up Current (25°C)	I_{TRIG}	±400	mA

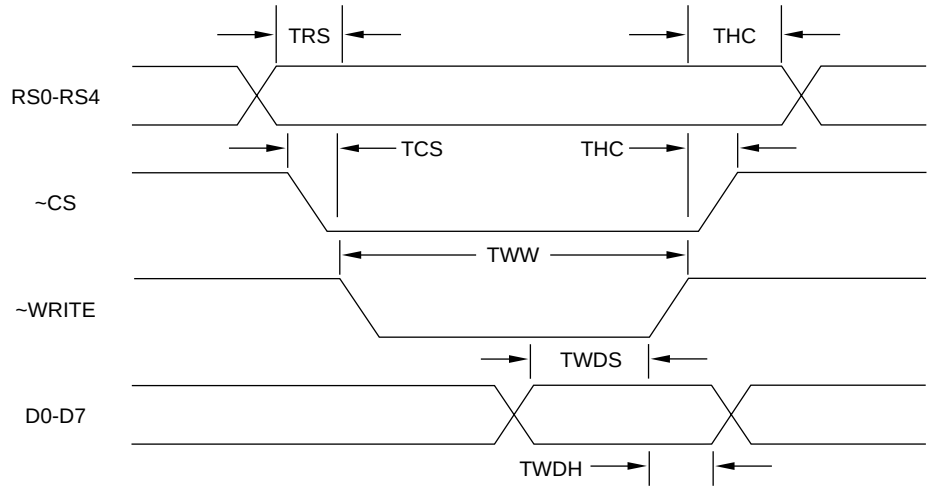
* VGG = +5.0V ± 5% or +3.3V ± 0.3V.

Table 2-8. Host Bus Interface Timing

Parameter	Symbol	Min.	Max.	Units
a. Read				
Address Setup	TRS	10	–	ns
Chip Select Setup	TCS	0	–	ns
Control Hold	THC	10	–	ns
Read Data Access	TDA	-	35	ns
Read Data Hold	TDHR	10	–	ns
Read Pulse Width	TRR	45	–	ns
b. Write				
Address Setup	TRS	10	–	ns
Chip Select Setup	TCS	0	–	ns
Control Hold	THC	10	–	ns
Write Data Setup	TWDS	10	–	ns
Write Data Hold	TWDH	10	–	ns
Write Pulse Width	TWW	45	–	ns



a. Host Bus Read



b. Host Bus Write

* A minimum delay of 3 times the YCLK cycle time is required from the rising edge of ~WRITE to the falling edge of the next selected ~READ or ~WRITE. YCLK = crystal frequency/2.

A minimum delay of 20 ns is required from the rising edge of ~READ to the falling edge of the next selected ~READ or ~WRITE.

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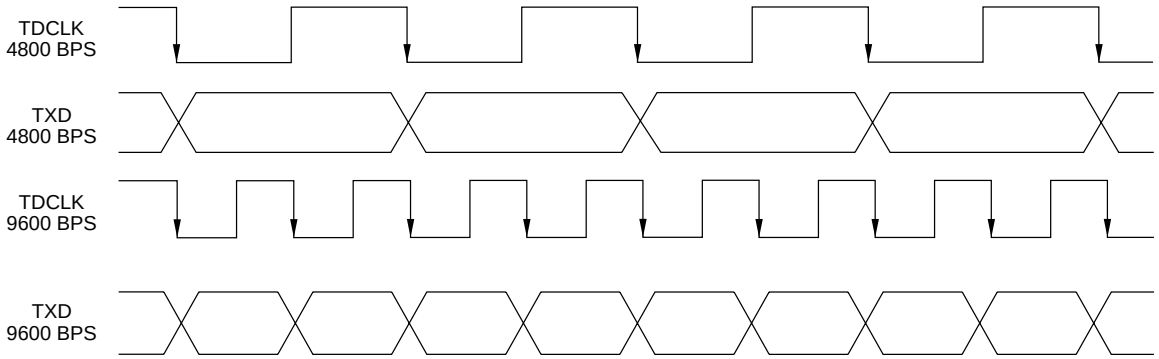
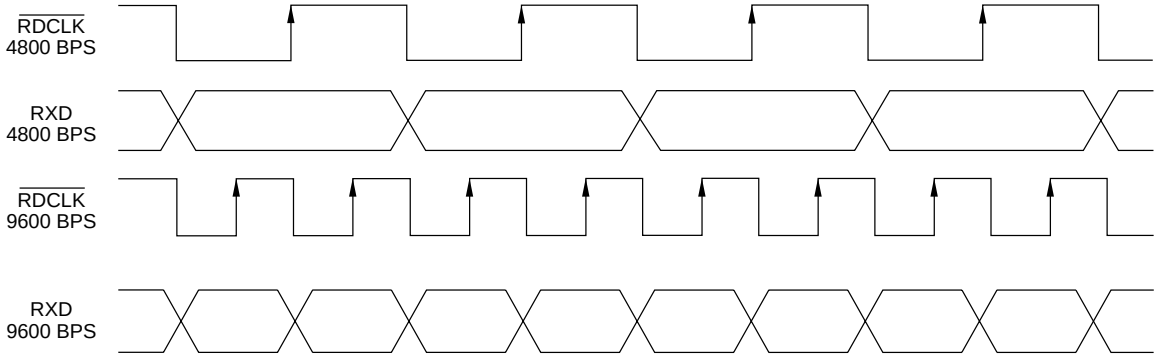
Figure 2-6. Host Bus Interface Waveforms



NOTE: THIS FIGURE IS VALID FOR SYNCHRONOUS MODE ONLY. THERE IS NO RELATIONSHIP BETWEEN TXD AND TDCLK IN ASYNCHRONOUS MODE.

a. Transmit



NOTE: THIS FIGURE IS VALID FOR SYNCHRONOUS MODE ONLY. THERE IS NO RELATIONSHIP BETWEEN RXD AND RDCLK IN ASYNCHRONOUS MODE.

b. Receive

1026F2-8 SIF WF

Figure 2-7. DTE Serial Interface Waveforms

2.2 LINE TRANSFORMER REQUIREMENTS FOR K56flex, V.34/V.32

K56flex/V.34/V.32 bis/V.32 places high requirements upon the Data Access Arrangement (DAA) to the telephone line. Any non-linear distortion generated by the DAA in the transmit direction cannot be canceled by the MDP's echo canceller and interferes with data reception. The designer must, therefore, ensure that the total harmonic distortion seen at the RXA input to the MDP be at least 45 dB (RC336) or 65 dB (RCDL56) below the minimum level of received signal. Due to the wider bandwidth requirements in K56flex and V.34, the DAA must maintain linearity from 10 Hz to 3954 Hz (RC336) or 4000 Hz (RCDL56).

Note that the major source of non-linear distortion in a DAA is the line transformer. A suitable line transformer is the MIDCOM 671-8262 or equivalent.

When designing a DAA, the designer should take into account a worst case subscriber line, giving very poor matching to the DAA hybrid circuit and resulting in a large near-end echo.

3. SOFTWARE INTERFACE

Modem data pump functions are implemented in MDP DSP firmware (code).

3.1 INTERFACE MEMORY

The MDP DSP communicates with the host processor by means of a dual-port, interface memory. The interface memory contains thirty-two 8-bit registers, labeled register 00 through 1F. Each register can be read from, or written into, by both the host and the DSP. The host communicates with the MDP interface memory via the microprocessor bus.

The host can control MDP operation by writing control bits to DSP interface memory and writing parameter values to DSP RAM through the interface memory. The host can monitor MDP operation by reading status bits from DSP interface memory and reading parameter values from DSP RAM through interface memory.

3.1.1 Interface Memory Map

An interface memory map of the 32 addressable registers in the MDP is shown in Figure 3-1. These 8-bit registers may be read or written during any host read or write cycle. In order to operate on a single bit or a group of bits in a register, the host processor must read a register then mask out unwanted data. When writing a single bit or group of bits in a register, the host processor must perform a read-modify-write operation. That is, read the entire register, set or reset the necessary bits without altering the other register bits, then write the unaffected and modified bits back into the interface memory.

3.1.2 Interface Memory Signal Definitions

The individual bits in the interface memory are defined in Table 3-1. The bits in the interface memory are referred to using the format Z:Q. The register number is specified by Z (00 through 1F) and the bit number by Q (0 through 7, 0 = LSB).

Register (Hex)	Bit 7	6	5	4	3	2	1	0
1F	NSIA	NCIA	—	NSIE	NEWS	NCIE	—	NEWC
1E	TDBIA	RDBIA	TDBIE	—	TDBE	RDBIE	—	RDBF
1D	MEACC	—	MEMW	MEMCR	Memory Access Address High B11-B8 (MEADDH)			
1C	Memory Access Address Low B7-B0 (MEADDL)							
1B	EDET	DTDET	OTS	DTMFD	DTMFW			
1A	SFRES	RIEN	RION	DMAE	—	SCOBF	SCIBE	SECEN
19	Memory Access Data MSB B15-B8 (MEDAM)							
18	Memory Access Data LSB B7-B0 (MEDAL)							
17	Secondary Transmit Data Buffer/V.34 Transmit Status(SECTXB)							
16	Secondary Receive Data Buffer/V.34 Receive Status (SECRXB)							
15	SLEEP	—	RDWK	HWRWK	AUTO	RREN	EXL3	EARC
14	ABCODE							
13	TLVL				RTH		TXCLK	
12	Configuration (CONF)							
11	BRKS	PARSL		TXV	RXV	V23HDX	TEOF	TXP
10	Transmit Data Buffer (TBUFFER)/Voice Transmit Buffer (VBUFT)							
0F	RLSD	FED	CTS	DSR	RI	TM	RTSDT	V54DT
0E	RTDET	BRKD	RREDT	SPEED				
0D	P2DET	PNDET	S1DET	SCR1	U1DET	—	TXFNF	—
0C	AADET	ACDET	CADET	CCDET	SDET	SNDET	RXFNE	RSEQ
0B	TONEA	TONEB	TONEC	ATV25	ATBEL	—	DISDET	EQMAT
0A	PNSUC	FLAGDT	PE	FE	OE	CRCS	FLAGS	SYNCD
09	NV25	CC	DTMF	ORG	LL	DATA	RRTSE	DTR
08	ASYN	TPDM	V21S	V54T	V54A	V54P	RTRN	RTS
07	RDLE	RDL	L2ACT	—	L3ACT	—	RA	MHLD
06	—	EXOS	—	HDLC	PEN	STB	WDSZ/DECBITS	
05	—	—	—	TXSQ	CEQ	—	STOFF	—
04	RB	—	—	FIFOEN	—	NRZIEN/ VAGC	—	STRN
03	EPT	SEPT	SRCEN	RLSDE	—	—	GTE	GTS
02	TDE	SQDIS	S511	—	RTSDE	V54TE	V54AE	V54PE
			DCDEN	CDEN	—	—	CODBITS	
01	VOLUME		VPAUSE	—	—	TXHF	RXHF	RXP
00	Receive Data Buffer (RBUFFER)/Voice Receive Data Buffer (VBUFR)							

Notes:

1. — in the "Bit" columns indicates reserved for MDP use only.

Figure 3-1. Modem Interface Memory Map

Table 3-1. Interface Memory Bit Definitions

Mnemonic	Location	Default	Name/Description
AADET	0Ch:7	–	**AA Detector.** When set, status bit AADET indicates that a V.32 bis/V.32 AA sequence has been detected. This bit is reset by the MDP at the start of the CC sequence. This bit is not valid during rate renegotiation. (V.32 bis, V.32)
ABCODE	14h:0–7	00	**Abort Code.** If the handshake fails, an abort code is written into ABCODE. This code indicates the point in the handshake where the failure occurred. The abort code is not cleared by the MDP but may be cleared by the host after it has been read. The abort codes and their meanings are listed in Table 3-2. Refer to ITU-T recommendations for meanings of the signal mnemonics used. (V.8, K56flex, V.34, V.32 bis, V.32)
ACDET	0Ch:6	–	**AC Detector.** When set, status bit ACDET indicates that a V.32 bis/V.32 AC sequence has been detected. This bit is reset by the MDP when a CA sequence or an energy dropout is detected. This bit is not valid during rate renegotiation. Active when DTR = 1 and DATA = X or when DTR = 0 and DATA = 0. (V.32 bis, V.32)
ASYN	08h:7	0	**Asynchronous/Synchronous.** When configuration bit ASYN is set, asynchronous mode is selected; when 0, synchronous mode is selected. When the ASYN bit changes from a 0 to a 1, the asynchronous to synchronous converter is configured according to the EXOS, PEN, STB and WDSZ bits at that time (EXOS, PEN, STB and WDSZ must be configured before ASYN changes from a 0 to a 1.) ASYN may be used to switch between synchronous and asynchronous modes only when RTS is OFF and TDBE = 1 in idle or data mode. Do not set this bit in V.21, V.23, or Bell 103 serial mode. Set this bit in V.21, V.23, or Bell 103 parallel mode. Note that the HDLC bit must be reset to 0 when ASYN is a 1. (K56flex, V.34, V.32 bis, V.32, V.22 bis, V.22, Bell 212A)
ATBEL	0Bh:3	–	**Bell Answer Tone Detector.** When set, status bit ATBEL signifies that the MDP receiver detected a 2225 Hz answer tone. The bit is set when the answer tone is detected, and is reset when the tone ends. ATBEL is active only when the DATA bit is reset and the MDP is in originate mode. [Bell 212A, Bell 103, tone modes (CONF = 80h, 81h, or 83h)]
ATV25	0Bh:4	–	**V25 Answer Tone Detector.** When set, status bit ATV25 signifies that the MDP receiver detected a 2100 Hz answer tone. The bit is set when the answer tone is detected, and is reset when the tone ends. ATV25 is only active when the DATA bit is reset before energy is present at RXA and the MDP is in originate mode. [K56flex, V.8, V.32 bis, V.32, V.22 bis, V.22, V.23, V.21, tone modes (CONF = 80h, 81h, or 83h)]

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
AUTO	15h:3	0	**Automatic Mode Change Enable.** When control bit AUTO is set, the MDP will automatically determine the communication standard of the remote modem and configure itself accordingly. The automode algorithm is based on the EIA/TIA PN-2330 specification. The possible operating modes are: V.32 bis/V.32, V.22 bis, V.22, Bell 212A, Bell 103, V.23 and V.21. Note that TONEB is not available for use by the host when automode function is used in answer mode To operate in automode, the MDP must be configured to V.8, V.32, or V.32 bis in CONF, the AUTO bit must be set, and the DATA bit reset. Setting DTR or activating the DTR pin will then commence the handshake. The AUTO bit will be reset and the DATA bit will be set when the MDP has determined the remote modem type. CONF will then contain the configuration code of the modem type found. It is recommended that the AUTO bit remain reset until answer tone has been detected when in originate mode. The automode function will select V.23 mode only if the remote modem is configured for 1200 receive originate or 75 receive answer. (K56flex, V.8, V.32 bis, V.32)
BRKD	0Eh:6	–	**Break Detected.** When set, status bit BRKD indicates the MDP is receiving continuous space in a synchronous mode. When reset, continuous space is not being received.
BRKS	11h:7	0	**Break Sequence.** When control bit BRKS is set in parallel asynchronous mode, the MDP will send continuous space. When BRKS is reset, the MDP will transmit parallel data from the TBUFFER. (This bit is valid only when TPDM = 1.)
CADET	0Ch:5	–	**CA Detector.** When set, status bit CADET indicates that a CA sequence has been detected. This bit is reset by the MDP when a AC sequence is detected. This bit is not valid during rate renegotiation. (V.32 bis, V.32)
CC	09h:6	0	**Controlled Carrier.** When control bit CC is set and the LL bit is set, the MDP operates in controlled carrier; when bit CC is reset, the MDP operates in constant carrier. Controlled carrier allows the MDP transmitter to be controlled by the RTS pin or the RTS bit (Table 1-3). When the RTS pin is asserted, or the RTS bit set, the transmitter immediately sends scrambled ones for 270 ms and then turns on the ~CTS signal and the CTS bit. (V.22 bis, V.22, V.23, V.21, Bell 212A). (See LL bit description.)
CCDET	0Ch:4	–	**CC Detector.** When set, status bit CCDET indicates that a CC sequence has been detected. This bit is reset by the MDP when an energy dropout is detected. This bit is not valid during rate renegotiation. (V.32 bis, V.32)
CDEN	02h:4	0	**Coder Enable.** In receive voice mode (CONF bits = ACh, 80h, 81h, 83h, or 86h, and RXV = 1), control bit CDEN = 1 selects ADPCM receive mode. In this mode, the MDP performs ADPCM coding and places the coder output into the Voice Receive Buffer (VBUFR). CDEN = 0 selects receive pass-through mode (see RXV bit).
CEQ	05h:3	1	**Compromise Equalizer Enable.** When control bit CEQ is set, the transmitter's digital compromise equalizer is inserted into the transmit path. CEQ should be reset during local analog loopback and in FSK modes (except V.23/1200TX and V.8) to ensure uniform transmit levels for both mark and space frequencies.
CODBITS	02h:1-0	–	**Coder No. of Bits.** Defines the number of bits per sample (2, 3, or 4) used by the ADPCM coder. (ADPCM receive mode only.)

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
CONF	12h:7-0	76	**Modem Configuration.** The CONF control bits select the MDP configuration from the following codes:

Mode	Data Rate	CONF (Hex)	
K56flex	32000-56000		See Section 14
K56flex Cleardown	—	90	See Note 1
V.8		AA	
V.34 TCM	33600	CE	
V.34 TCM	31200	CD	
V.34 TCM	28800	CC	
V.34 TCM	26400	CB	
V.34 TCM	24000	CA	
V.34 TCM	21600	C9	
V.34 TCM	19200	C8	
V.34 TCM	16800	C7	
V.34 TCM	14400	C6	
V.34 TCM	12000	C5	
V.34 TCM	9600	C4	
V.34 TCM	7200	C3	
V.34 TCM	4800	C2	
V.34 TCM	2400	C1	
V.34 Cleardown	—	C0	See Note 1.
V.33 TCM	14400	31	
V.33 TCM	12000	32	
V.33 TCM	9600	34	
V.33 TCM	7200	38	
V.32 bis TCM	14400	76	
V.32 bis TCM	12000	72	
V.32 TCM	9600	74	
V.32	9600	75	
V.32 bis TCM	7200	78	
V.32	4800	71	
V.32 bis/V.32 Cleardown	—	70	See Note 1.
V.17 TCM	14400	B1	
V.17 TCM	12000	B2	
V.17 TCM	9600	B4	
V.17 TCM	7200	B8	
V.29	9600	14	
V.29	7200	12	
V.29	4800	11	
V.27 ter	4800	02	
V.27 ter	2400	01	
V.22 bis	2400	84	
V.22 bis	1200	82	See Note 2.
V.22	1200	52	
V.22	600	51	
V.21	0-300	A0	
V.21 Channel 2	300	A8	
Bell 208	4800	23	
Bell 212A	1200	62	
Bell 103	0-300	60	
V.23	1200 TX/75 RX	A4	
V.23	75 TX/1200 RX	A1	
Transmit Single Tone	—	80	See Notes 3 and 4.
Transmit Dual Tone	—	83	See Notes 3 and 4.
Dialing	—	81	See Note 4.
DTMF Receiver	—	86	See Note 4.
Speakerphone/Voice	—	AC	

(Continued on the next page.)

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
CONF	12h:0–7	76	**Modem Configuration (Cont'd).** **NOTES:** 1. The MDP can transmit a GSTN Cleardown sequence during a retrain (V.32 bis/V.32) or a rate renegotiation (K56flex, V.34/V.32 bis/V.32). In V.32 bis/V.32, the remote modem will automatically detect the Cleardown sequence and both modems will drop carrier at the end of the retrain or rate renegotiation. In V.34, the MDP will indicate the Cleardown detection by writing a 96h in ABCODE. The host must terminate the connection by resetting DTR and setting NEWC (see Function 75 in Section 4). 2. Configuration 82 allows for possible fall forward to 2400 bps. 3. The MDP transmits one or two tones depending upon the selected mode. The tone frequencies and levels are host programmable in DSP RAM. 4. Voice mode can run concurrently; see TXV and RXV bits.
CRCS	0Ah:2	0	**CRC Sending**. When set, status bit CRCS indicates that the transmitter is sending the CRC (2 bytes) in HDLC (SDLC) mode. A 0 indicates that the CRC is not being sent. Either a 16-bit (default) or 32-bit CRC may be sent as selected by the ITU-T CRC32 parameter in RAM (see Section 4.4, Function 52). To disable the CRC transmission in HDLC mode, set bit 0B3h: 6. This is needed for H.324 applications. (See Section 5.1).
CTS	0Fh:5	–	**Clear To Send.** When set, status bit CTS indicates to the DTE that the training sequence has been completed and any data present at TXD (serial mode) or in TBUFFER (parallel mode) will be transmitted (see TPDM). CTS response times from an RTS ON or OFF transition after the MDP has completed a handshake are shown in Table 1-3. The CTS OFF-to-ON response time is programmable in DSP RAM.
DATA	09h:2	1	**Data.** Control bit DATA is used to prevent the transmitter from entering and proceeding with the handshake (start-up) sequence and to ignore all V.24 interface signals. When control bit DATA is reset, the MDP is prevented from entering and proceeding with the handshake (start-up) sequence and will ignore all V.24 interface signals. This bit should be set by the host at a suitable time after completion of dialing or answering. Recommended procedure for originating a call in V.8, V.32 bis/V.32 using DATA: Reset both DATA and DTR. Establish a call. Detect answer tone using ATV25. After receiving answer tone for 1 second, configure to the appropriate mode, set DTR and DATA. (If automode is to be used, set AUTO and leave DATA reset.) The handshake will now proceed. **NOTE:** Set DATA no later than 20 ms after detecting ACDET = 1 for compatibility with V.32 modems which send the minimum allowable AC length of 53.3 ms.
DCDEN	02h:5	0	**Decoder Enable.** In transmit voice mode (CONF bits = ACh, 80h, 81h, 83h, or 86h and TXV = 1), control bit DCDEN = 1 selects ADPCM transmit voice mode. In this mode, the MDP performs ADPCM decoding on the contents of the Voice Transmit Buffer (VBUFT). DCDEN = 0 selects transmit voice pass-through mode (see TXV bit).
DECBITS	06h:1-0	–	**Decoder No. of Bits.** DECBITS defines the number of bits per sample (2, 3, or 4) used by the ADPCM decoder. (ADPCM transmit mode only.)

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
DISDET	0Bh:1	–	**Disconnect Detect.** When set, status bit DISDET indicates that a line disconnection has occurred and the MDP has synchronized onto it's own transmit signal (i.e., EQM acceptable and RLSD still on). The host may then issue a retrain to confirm the disconnection and subsequently drop the line if a response is not detected. Bit DISDET will remain set until reset by the host. (V.32 bis, V.32) **Note:** If RLSD turns off or EQM increases to an unacceptable value due to a disconnection, bit DISDET will not turn on.
DMAE	1Ah:4	0	**DMA Signals Enabled.** When set to a 1, control bit DMAE converts the ~RI and ~DSR output lines to the TXRQ (Transmitter Request) and RXRQ (Receiver Request) output lines, respectively. TXRQ is a high active signal that follows the state of the TDBE bit and the RXRQ is a high active signal that follows the state of the RDBF bit. DMA is available in asynchronous, synchronous and HDLC modes. Bit FIFOEN must be set in asynchronous modes in order to obtain the RXRQ interrupt. (TPDM = 1)
DSR	0Fh:4	–	**Data Set Ready.** Status bit DSR operation is in accordance with circuit 107 of the ITU-T specifications.
DTDET	1Bh:6	–	**Dual Tone Detected.** When configured as a DTMF Receiver, the MDP sets status bit DTDET when a signal is received that satisfies all DTMF criteria except on-time, off-time, and cycle-time. The encoded DTMFW Output Word (1Bh:3-0) value is available when DTDET is set.
DTMF	09h:5	1	**DTMF Select.** When the MDP is configured for dialing mode (CONF = 81h), the MDP will dial using DTMF tones or pulses. When control bit DTMF is set, the MDP will dial using DTMF tones. When DTMF is reset, the MDP will dial using pulses. The DTMF bit can be changed during the dialing process to allow either tone or pulse dialing of consecutive digits. When in dialing mode, the data placed in the Transmit Data Buffer is treated as digits to be dialed. The number to be dialed must be represented by two hexadecimal digits (e.g., if a 9 is to be dialed, then a 09 must be written to the Transmit Data Buffer). Also, see TDBE bit. Dialing timing and power levels are host programmable in DSP RAM (Table 4-1). Pulse dialing defaults to the ~OHRC output. The pulse dialing output is controlled by bit 0D4h:6 [0 = ~OHRC (~RLYA) output; 1 = ~TALK (~RLYB) output] when in dial mode. The output may be selected using RAM access method 1 (see Section 4).
DTMFD	1Bh:4	–	**DTMF Signal Detected.** When configured as a DTMF receiver, the MDP sets status bit DTMFD when a DTMF signal has been detected that satisfies all specified DTMF detect criteria.
DTMFW	1Bh:3-0	–	**DTMF Output Word.** When the MDP is configured as a DTMF receiver and status bit DTDET is set by the MDP, the encoded DTMF output is written into DTMFW. **DTMF Symbol / Encoded Output (Hex) / DTMF Symbol / Encoded Output (Hex)** 0 0 8 8 1 1 9 9 2 2 * A 3 3 # B 4 4 A C 5 5 B D 6 6 C E 7 7 D F The host should wait until the DTMFD bit is set before reading the DTMFW bit.

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
DTR	09h:0	0	**Data Terminal Ready.** In K56flex, V.8, V.34, V.32 bis/V.32, V.22/V.22 bis, and Bell 212A modes, setting control bit DTR initiates a handshake sequence. If in answer mode, the MDP will immediately send answer tone. In V.21, V.23, and Bell 103 modes, DTR must be set for the MDP to enter data state providing DATA bit is set. If in answer mode, the MDP will send answer tone. In these configurations, if controlled carrier is selected, the carrier is controlled by the RTS pin or RTS bit. During the data mode, resetting DTR will cause the transmitter to turn off. The DTR bit parallels the operation of the hardware ~DTR control input. These inputs are ORed by the MDP.
EARC	15h:0	0	**Extended Automatic Rate Change.** Control bit EARC is used to enable automatic rate adaption or automatic rate change during the handshake. When EARC is set, do **not** change the contents of CONF when performing a rate change. This bit is typically used for handshake and retrain only. Turn off EARC once connected. Re-enable EARC if initiating or detecting a retrain. This bit is not advisable for rate negotiation. (See Section 4 for detailed information about auto rate adaption.) (K56flex, V.34, V.32 bis, V.32).
EDET	1Bh:7	–	**DTMF Early Detection.** When configured as a DTMF receiver, the MDP sets status bit EDET to indicate that the received signal is probably a DTMF signal.
EPT	03h:7	0	**Echo Protector Tone Enable.** When control bit EPT is set, an unmodulated carrier is transmitted for 185 ms (SEPT = 0) or 30 ms (SEPT = 1) followed by 20 ms of no transmitted energy prior to the transmission of the training sequence. When EPT is reset, neither the echo protector tone nor the 20 ms of no energy are transmitted prior to the transmission of the training sequence. (V.33, V.17, V.29, V.27) The echo protector tone is typically used in V.27 ter and V.29 over dial-up lines. The tone is sent prior to the training sequence to ensure that the echo suppressors are pointing in the correct direction.
EQMAT	0Bh:0	0	**EQM Above Threshold.** Status bit EQMAT indicates that the measured EQM is above (1) or not above (0) the threshold value programmed in DSP RAM. The default threshold is 3000h. This bit must be cleared by the host. (See Section 4, Function 46.)
EXL3	15h:1	0	**External Loop 3 Selector.** When control bits L3ACT and EXL3 are both set, the signal path for local analog loopback is external to the MDP. When L3ACT is set but EXL3 is reset, the local analog loop signal path is internal to the MDP. This bit is used for measuring the transmit spectrum in V.34, V.32 and V.22 bis modes, without having to connect to a remote modem. V.22 bis/V.22 modes send the low carrier by default. To send the high carrier, write 5555h to location B42h after setting DTR. To send space frequency in FSK modes, use ASYN = 1, TPDM = 1, RTS = 1, and BRKS = 1. BRKS = 0 will cause mark to be sent. (See L3ACT.)
EXOS	06h:6	0	**Extended Overspeed.** When control bit EXOS is set, Extended Overspeed mode is selected in the async-to-sync converter and in the sync-to-async converter. This bit must be configured appropriately before the ASYN bit changes from a 0 to a 1 for asynchronous mode. (K56flex, V.34, V.32 bis, V.32, V.22 bis, V.22, Bell 212A)

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
FE	0Ah:4	0	**Framing Error.** When set, status bit FE indicates that more than 1 in 8 (or 1 in 4 for extended overspeed) characters were received without a Stop bit in asynchronous mode or an ABORT sequence was detected in SDLC/HDLC synchronous mode. When reset, no framing error is detected. In voice receive mode, FE = 1 and PE = 1 denote the first low byte.
FED	0Fh:6	–	**Fast Energy Detector.** When status bit FED is set, energy in the passband above the selected receiver threshold has been detected (see RTH). DTR must be on in order for FED to function in full duplex modes (DATA = 1).
FIFOEN	04h:4	0	**FIFO Enable.** When control bit FIFOEN = 1, the host can input up to 16 bytes of data through TBUFFER, or voice samples through VBUFT, using the TDBE bit as a software interrupt or the TXRQ signal (DMAE = 1) as a DMA request interrupt. In HDLC, by default, if the host underruns the Transmit FIFO, the MDP will append a CRC. If bit 3A5h: 6 is set, the MDP will instead abort the frame and provide an abort code of 41h in ABCODE. The Receive FIFO is always enabled. The host may wait up to 16 byte-times before reading the data in RBUFFER. The RDBF bit or RXRQ signal (DMAE = 1) signals the availability of receive data to the host. The trigger level for RDBF bit/RXRQ signal is host programmable in DSP RAM. (See Section 4 for a detailed description about FIFO operation.) (TPDM = 1)
FLAGDT	0Ah:6	–	**V.21 Channel 2 Flag Detected.** When set, status bit FLAGDT indicates that V.21 Channel 2 Flags (7Eh) are being detected. (V.33, V.17, V.29, V.27 ter)
FLAGS	0Ah:1	0	**Flag Sequence.** When set, status bit FLAGS indicates that the transmitter is sending the Flag sequence in SDLC/HDLC mode, or a constant mark in parallel asynchronous mode. When reset, FLAGS indicates that the transmitter is sending data.
GTE	03h:1	0	**Guard Tone Enable.** When set, control bit GTE causes the specified guard tone to be transmitted (by the answering MDP only) according to the state of the GTS bit. (V.22 bis, V.22)
GTS	03h:0	0	**Guard Tone Select.** When set, control bit GTS selects the 550 Hz tone; when reset, GTE selects the 1800 Hz tone. The selected guard tone will be transmitted only when GTE is enabled. The host must set NEWC after changing the GTS bit. (V.22 bis, V.22)
HDLC	06h:4	0	**HDLC Select.** When control bit HDLC is set, HDLC operation is enabled. When HDLC is reset, HDLC operation is disabled. The ASYN bit must be 0 and the TDBE bit must be 1 prior to setting HDLC to a 1. The HDLC bit is valid only in synchronous parallel data mode (ASYN = 0 and TPDM = 1). Not valid in FSK modes except V.21 channel 2. RTS must be off before switching in or out of HDLC mode while in DATA mode. Note that CRC generation can be disabled by setting bit 6 of RAM location 0B3h (default = CRC generation enabled).
HWRWK	15h:4	1	**Host Write Wake up.** When control bit HWRWK is set and the MDP is in sleep mode, a host write to any register with the exception of 1Dh:7-0, will bring the MDP out of sleep mode. (See SLEEP bit.)

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
L2ACT	07h:5	0	**Loop 2 Activate.** When control bit L2ACT is set, the receiver's digital output is connected to the transmitter's digital input (locally activated remote digital loopback) in accordance with V.54. A V.34 connection must be symmetrical in order to perform Loop 2. (Not valid in K56flex or FSK modes.)
L3ACT	07h:3	0	**Loop 3 Activate.** When control bit L3ACT is set, the transmitter's analog output is coupled internally to the receiver's analog input through an attenuator (local analog loopback) in accordance with ITU-T Recommendation V.54. Optionally, the signal path for loop 3 can also be established externally to the MDP (see EXL3). The MDP may only be placed into loop 3 mode when in idle mode (~DTR signal is OFF and the DTR bit is reset). NEWC must be set after any change in the L3ACT bit. The loopback is then completed (terminated) by asserting ~DTR signal ON (low) or setting the DTR bit. The transmitter's compromise equalizer should be disabled, by resetting CEQ, during local analog loopback. (Not valid in K56flex mode.)
LL	09h:3	0	**Leased Line.** When control bit LL is set, the MDP is in leased line operation; when 0, the MDP is in switched line operation, except as described below. For V.22 bis/V.22, set the LL bit and reset the CC bit. The MDP immediately sends scrambled ones and goes into data mode. A retrain may be required after the initial connection. (V.22 bis, V.22) For V.34, set the LL bit (V.8 should not be used in V.34 leased line). When DTR and DATA bits are set, the MDP continuously sends INFO0 until the remote modem is detected. (V.34) For V.32 bis/V.32, do not set LL bit. When DTR and DATA bits are set, the MDP continuously sends its preamble signal until the remote modem is detected. If desired, set the NV25 bit to prevent answer tone from being sent in answer mode. **Note:** Long term connection may require a retrain every 1-2 days in V.34 and V.32 bis modes in order to maintain connection stability. A rise in EQM will indicate the need for a retrain. Long term connections are not guaranteed to be error free. (Applicable to V.34, V.32 bis/V.32, and V.22 bis/V.22 only.)
MEACC	1Dh:7	0	**Memory Access Enable.** When control bit MEACC is set, the DSP accesses the RAM associated with the address in MEADDH and MEADDL. The MEMW bit determines if a read or write is performed. The DSP resets the MEACC upon RAM access completion.
MEADDL	1Ch: 7-0	00	**Memory Access Address Low (7-0).** MEADDL contains the lower 8 bits (bits 7-0) of the address used to access MDP RAM via the memory access data LSB (18h) and MSB (19h) registers. (See Table 4-1.)
MEADDH	1Dh:3-0	0	**Memory Access Address High (11-8).** MEADDH contains the upper 4 bits (bits 11-8) of the address used to access MDP RAM via the memory access data LSB (18h) and MSB (19h) registers. (See Table 4-1.)
MEDAL	18h:7-0	00	**Memory Data LSB.** MEDAL is the least significant byte (bits 7-0) of the 16-bit data word used in reading or writing data locations in MDP RAM.
MEDAM	19h:7-0	00	**Memory Data MSB.** MEDAM is the most significant byte (bits 15-8) of the 16-bit data word used in reading or writing data locations in MDP RAM.

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
MEMCR	1Dh:4	0	**Memory Continuous Read.** When set to a 1, control bit MEMCR instructs the DSP to automatically update the data in MEDAM and MEDAL based on the RAM address in MEADDH and MEADDL. without the host having to set the MEACC bit. The MDP will set the NEWS bit to a 1 when new data is available.
MEMW	1Dh:5	0	**Memory Write.** When MEMW is set and MEACC is set, the DSP copies data from the interface memory data registers MEDAL (18h) and MEDAM (19h) into the memory location addressed by MEADDL and MEADDH. When control bit MEMW is reset and MEACC is set, the DSP reads memory at the location addressed by MEADDL and MEADDH. The read data is stored into interface memory data registers MEDAL (18h) and MEDAM (19h).
MHLD	07h:0	0	**Mark Hold.** When control bit MHLD is set, the transmitter's digital input data is clamped to a mark. When MHLD is reset, the transmitter's input is taken from TXD or TBUFFER (see TPDM).
NCIA	1Fh:6	–	**NEWC Interrupt Active.** When the new configuration chip 0 interrupt is enabled (NCIE is set) and a new configuration is implemented (NEWC is reset), the MDP asserts IRQ and sets status bit NCIA to indicate that NEWC being reset caused the interrupt. NCIA and the interrupt request due to NEWC are cleared by the host writing a 0 into NCIE. (See NEWC and NCIE.)
NCIE	1Fh:2	0	**NEWC Interrupt Enable.** When control bit NCIE is set (interrupt enabled), the MDP will assert IRQ and set NCIA when the NEWC bit is reset by the MDP. When NCIE is reset (interrupt disabled), NEWC has no effect on IRQ or NCIA. (See NEWC and NCIA.)
NEWC	1Fh:0	0	**New Configuration.** Control bit NEWC must be set by the host after the host changes the configuration code in CONF (12h) or changes any of the following controls bits: CEQ (05h:3), DTMF (09h:5), GTE (03h:1), GTS (03h:0), L3ACT (07h:3), LL (09h:3), ORG(09h:4), RTH (13h:2,3), RXV (11h:3), SFRES (1Ah:7), SLEEP (15h:7), TLVL (13h:7-4), TXCLK (13h:1-0), TXV (11h:4), V21S (08h:5), or V23HDX (11h:2). This informs the MDP to implement the new configuration. The MDP resets the NEWC bit when the configuration change is implemented. A configuration change can also cause IRQ to be asserted. **NOTE:** NEWC should not be set once a connection is being attempted or completed. (See NCIE and NCIA.)
NEWS	1Fh:3	–	**New Status.** When set, status bit NEWS indicates that one or more status bits located in registers 0A–0F, 01, 12, 14, 16-17, 1A, or 1B have changed state (default = interrupt OFF), or a DSP RAM read or write has been completed (default = interrupt ON). This bit can be reset only by the host. The host may mask the effect of individual status bits upon NEWS by writing a mask value to DSP RAM (see Function 17 in Section 4). When set, this bit can cause IRQ to be asserted. (See NSIE and NSIA.) **NOTE:** When read/modifying register 1F, set NEWS = 1 to ensure that the host does not reset NEWS after the MDP DSP has set NEWS during read/modify. If NEWS = 0, setting NEWS to a 1 will not be accepted by the DSP and NEWS will remain a 0.
NRZIEN	04h:2	0	**NRZI Enable.** When set, control bit NRZIEN enables NRZI transmitter encoding and receiver decoding in all synchronous and HDLC modes. When NRZIEN is reset, NRZ encoding and decoding is used.
NSIA	1Fh:7	–	**NEWS Interrupt Active.** When the new status interrupt is enabled (NSIE is set) and a change of status occurs (NEWS is set), the MDP asserts IRQ and sets status bit NSIA to indicate that NEWS being set caused the interrupt. NSIA and the interrupt request due to NEWS are cleared when the host writes a 0 to NEWS. (See NEWS and NSIE.)

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
NSIE	1Fh:4	0	**NEWS Interrupt Enable.** When control bit NSIE is set (interrupt enabled), the MDP will assert IRQ and set NSIA when NEWS is set by the MDP. When NSIE is reset (interrupt disabled), NEWS has no effect on IRQ or NSIA. (See NEWS and NSIA.)
NV25	09h:7	0	**No V.25 Answer Tone.** When control bit NV25 is set, the MDP will not transmit the 2100 Hz ITU-T answer tone when a handshake sequence is initiated and the MDP is in answer mode. (V.32 bis, V.32, V.22 bis, V.22, V.23, V.21) (Not valid in AUTO mode.)
OE	0Ah:3	0	**Overrun Error.** When set, status bit OE indicates that the Receiver Data Buffer (RBUFFER) was loaded from the RXA input before the host read the old data from RBUFFER. When reset, RBUFFER was read before new receive data was loaded into RBUFFER. This is valid for both ASYNC mode (ASYN = 1) and SDLC/HDLC mode. This bit must be reset by the host.
ORG	09h:4	0	**Originate.** When configuration bit ORG is set, the MDP is in originate mode; when reset, the MDP is in answer mode. Since this is a configuration bit, the NEWC bit must be set after any change in the ORG bit. For K56flex, see ORG bit description in Section 14.
OTS	1Bh:5	–	**DTMF On-Time Satisfied.** When configured as a DTMF receiver, the MDP sets status bit OTS after the on-time criteria is satisfied. This bit is reset by the MDP after DTMFD is set or if the received signal fails to satisfy the DTMF off-time criteria.
P2DET	0Dh:7	0	**P2 Sequence Detected.** When status bit P2DET is set, the MDP is detecting the P2 portion of the training sequence. When P2DET is reset, P2 is not being detected. (V.33, V.17, V.29. V.27)
PARSL	11h:6-5	00	**Parity Select. Parity Select.** Control bits PARSL select the method by which parity is generated and checked during the asynchronous parallel data mode (ASYN = 1). The options are: **6 5 Parity Selected** 0 0 Stuff Parity ("9th Data Bit") (see TXP, RXP) 0 1 Space Parity 1 0 Even Parity 1 1 Odd Parity
PE	0Ah:5	0	**Parity Error.** When set, status bit PE indicates that a character with bad parity was received in the asynchronous mode, or bad CRC was detected in the SDLC/HDLC synchronous mode. When reset, a character with good parity was received. In voice receive mode, FE = 1 and PE = 1 denote the first low byte.
PEN	06h:3	0	**Parity Enable.** When control bit PEN is set, parity is enabled in asynchronous mode. This bit must be configured appropriately before the ASYN bit changes from a 0 to a 1 for asynchronous mode. (K56flex, V.34, V.32 bis, V.32, V.22, V.22 bis, Bell 212A)
PNDET	0Dh:6	–	**PN Sequence Detected.** Status bit PNDET indicates that the PN portion of the training sequence is being detected (set) or is not being detected (reset). (V.33, V.17, V.29. V.27 ter)
PNSUC	0Ah:7	0	**PN Success.** When status bit PNSUC is set, the MDP has successfully trained at the end of the PN portion of the high speed training sequence. When PNSUC is reset, a successful training has not occurred. (V.33, V.17, V.29. V.27 ter)
RA	07h:1	0	**Relay A Activate.** When control bit RA is set, the ~OHRC output (~RLYA) is active; when reset, the ~OHRC output is off (high).
RB	04h:7	0	**Relay B Activate.** When control bit RB is set, the ~TALK output (~RLYB) is active; when reset, the ~TALK output is off (high).

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
RBUFFER	00h:7-0	–	**Receive Data Buffer.** The host obtains channel data from the MDP receiver in the parallel data mode by reading a data byte from the RBUFFER. The RBUFFER contains the received data when the RDBF bit is set. (See RDBF, RDBIE, and RDBIA.)
RDBF	1Eh:0	–	**Receive Data Buffer Full.** When set, status bit RDBF signifies that the receiver wrote valid data into RBUFFER (00h). This condition can also cause IRQ to be asserted. The host reading RBUFFER resets the RDBF and RDBIA bits. RDBF will remain set until the Receiver FIFO is emptied. (See RDBIE and RDBIA.)
RDBIA	1Eh:6	–	**Receive Data Buffer Interrupt Active.** When the receive data buffer interrupt is enabled (RDBIE is set) and RBUFFER (00h) is written to by the MDP (RDBF is set), the MDP asserts IRQ and sets RDBIA to indicate that RDBF being set caused the interrupt. The host reading RBUFFER resets the RDBIA bit and clears the interrupt request due to RDBF. (See RDBF and RDBIE.)
RDBIE	1Eh:2	0	**Receive Data Buffer Interrupt Enable.** When control bit RDBIE is set (interrupt enabled), the MDP will assert IRQ and set the RDBIA bit when RDBF is set by the MDP. When RDBIE is reset (interrupt disabled), RDBF has no effect on IRQ or RDBIA. (See RDBF and RDBIA.)
RDL	07h:6	0	**Remote Digital Loopback.** When set, control bit RDL causes the MDP to initiate a V.22 bis request for the remote modem to go into digital loopback; RXD is clamped to a mark and the CTS bit and ~CTS signal will be reset in the local MDP until the loop is established. The RDLE bit should be set before setting the RDL bit. (V.22 bis, V.22, Bell 212A/1200)
RDLE	07h:7	1	**Remote Digital Loopback Response Enable.** When set, control bit RDLE enables the MDP to respond to another modem's V.22 bis remote digital loopback request, thus going into loopback. When this occurs, the MDP clamps RXD to mark; resets the CTS, DSR and RLSD bits, and turns the ~CTS, ~DSR and ~RLSD signals to logic 1. The TM bit is set to inform the host of the test status. When the RDLE bit is reset, no response will be generated. (V.22 bis)
RDWK	15h:5	1	**Ring Detect Wake up.** When control bit RDWK is set and the MDP is in sleep mode, an incoming ring signal on the RINGD pin will bring the MDP out of sleep mode. The RINGD pin must be normally low for the RDWK function to work. (See SLEEP bit).
RI	0Fh:3	–	**Ring Indicator.** When set, status bit RI indicates that a ringing signal is being detected. Ringing is detected if pulses are present on the RINGD input in the 15 Hz–68 Hz frequency range. The RI bit follows the ringing signal with a 1 during the ON time and a 0 during the OFF time coincident with ~RI output signal. The decision bounds are host programmable in DSP RAM. This bit is valid only when DATA bit is reset and is not applicable in tone modes.
RIEN	1Ah:6	0	**RION Enable.** When control bit is a 1, the ~RI output will reflect the RION bit. When a 0, the ~RI output follows the ringing signal on the RINGD input.
RION	1Ah:5	0	**Ring Indicator On.** Control bit RION determines the state of the ~RI output (1 = low; 0 = high) when bit RIEN is set and the DATA bit is reset.
RLSD	0Fh:7	–	**Received Line Signal Detector.** When status bit RLSD is set, the MDP has finished receiving the training sequence or has turned on due to detected energy above threshold, and is receiving data. RLSD is reset when the MDP is in the idle state and during the reception of a training sequence. The RLSD threshold may be adjusted in DSP RAM.
RLSDE	03h:4	1	**RLSD Enable.** When control bit RLSDE is set, the ~RLSD pin reflects the RLSD bit state. When RLSDE is reset, the ~RLSD pin is clamped OFF and data is clamped to a mark regardless of the state of the RLSD bit.
RREDT	0Eh:5	–	**Rate Renegotiation Detected.** When set, status bit indicates a rate renegotiation sequence has been detected. RREDT will remain on until the host resets it. (K56flex, V.34, V.32 bis, V.32)

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
RREN	15h:2	0	**Rate Renegotiation.** If control bit RREN is set in K56flex, V.34 or V.32 bis data mode, a rate negotiation sequence is initiated. RREN resets as soon as the initiation is acknowledged. The RREN bit should be used only if both the local and remote modems are K56flex, V.34 or V.32 bis. The value in CONF indicates the connected mode (9Xh = K56flex, CXh = V.34, and 7Xh = V.32 bis). Fallback or fall-forward rate renegotiations may be accomplished in K56flex/V.34/V.32 bis mode as follows: 1. If EARC = 0, change CONF to the required configuration code. (If EARC = 1, do not change CONF; rate renegotiations are best left to the host, not the MDP's auto rate selection). EARC should be left off once the MDP is connected and only enabled if a retrain is detected and initiated. **NOTE:** Only the data rate within a mode can be changed, not the mode. **Do not** set the NEWC bit. 2. Set the RREN bit. If the remote modem can operate at the requested rate, the configuration will be changed by the MDP to reflect the new rate after the rate renegotiation is completed. The CTS bit will be reset during the rate renegotiation and will be set again upon completion of the rate renegotiation. If the remote modem cannot operate at the new rate and there are no common rates between the two modems, the MDP will send a Cleardown sequence and turn off RLSD in V.32 bis, or present an ABCODE of 96h in K56flex/V.34. The CONF register will contain C0h (K56flex/V.34) or 70h (V.32 bis) to indicate that a Cleardown was accomplished. In order to prevent rate negotiations from colliding, the MDP will first check for a possible incoming retrain or rate renegotiation before allowing the setting of the RREN bit to be processed. This may delay the RREN request by 3-4 ms. If a valid retrain or rate renegotiation is detected, the request for a RREN will be denied and the RREN bit will be reset to 0. The MDP will then proceed with the received retrain or rate renegotiation request. In V.32 bis, if the rate renegotiation fails due to line conditions, the MDP will try to complete the rate change by means of a retrain. In K56flex/V.34, the host must check EQM and issue the retrain manually by setting the RTRN bit.
RRTSE	09h:1	0	**Remote RTS Signaling Enable.** When control bit RRTSE is set and both the RTS bit and the RTS pin are inactive, the transmitter will send a pattern (idle pattern) produced by scrambling a binary 1 with the polynomial $1+x^{-3}+x^{-7}$. If RTS is deactivated and immediately reactivated, the MDP will send approximately 144 bits of idle pattern before acknowledging the reactivation of RTS. When RRTSE is set and the RTS bit or the RTS pin is activated, the transmitter will immediately send a pattern of 8 bits (turn-on pattern) produced by scrambling a binary 0 with the polynomial $1+x^{-3}+x^{-7}$ followed by the user data. CTS is automatically delayed until the end of the 8-bit turn-on pattern. The RTS-CTS delay may be increased to allow the MDP to transmit a period of mark after the 8-bit turn-on pattern in order to give the remote modem ample time to detect the turn-on and unclamp the receive data line. When control bit RRTSE is reset, remote RTS signaling is disabled and the RTS bit and RTS pin operate normally. In V.22 bis/V.22 LL mode, wait until RLSD = 1, set RRTSE, then set the CC bit. (Note that the CC bit must be set in order for V.13 to function in V.22 bis/V.22 LL mode.) This bit is not valid in FSK modes.

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
RSEQ	0Ch:0	0	**Rate Sequence Received.** When status bit RSEQ is set, the 16-bit rate sequence included in the start-up procedure has been received and is available in RAM. RSEQ will remain set until reset by the host. (V.32 bis, V.32)
RTDET	0Eh:7	–	**Retrain Detector.** When set, status bit RTDET indicates that a training sequence has been detected (K56flex, V.34, V.32 bis, V.32 or V.22 bis). This bit parallels the operation of the following: **Mode** — **Detector Bit** V.32 Originate — ACDET V.32 Answer — AADET V.22 bis — S1DET
RTH	13h:3-2	0	**Receiver Threshold.** The RTH control bits select the receiver energy detector threshold according to the following codes: **RTH** — **RLSD ON** — **RLSD OFF** 0 — – 43 dBm — – 48 dBm 1 — – 33 dBm — – 38 dBm 2 — – 26 dBm — – 31 dBm 3 — – 16 dBm — – 21 dBm
RTRN	08h:1	0	**Retrain.** If control bit RTRN is set in K56flex, V.34, V.32 bis, V.32, or V.22 bis data mode, a retrain sequence is initiated. RTRN resets as soon as the initiation is acknowledged. Fallback or fall-forward retrains may be accomplished in K56flex, V.34, V.32 bis, V.32, or V.22 bis modes as follows: 1. If EARC = 0, change CONF to the required configuration code. (If EARC = 1, do not change CONF). **NOTE:** Only the data rate within a mode can be changed, not the mode, e.g., fallback from V.32 to V.22 bis mode is not possible.) **Do not** set the NEWC bit. 2. Set the RTRN bit. If the remote modem can operate at the requested rate, the configuration will be changed by the MDP to reflect the new rate after the retrain is completed. The CTS bit will be reset during the retrain and will be set again upon completion of the retrain. The SPEED bits will also be updated at the end of the retrain. The host may wish to clear the SPEED bits during the retrain and wait for them to be updated to signify the end of retrain. If the remote modem cannot operate at the new rate and there are no common rates between the two modems, the MDP will send a Cleardown sequence and turn off RLSD in V.32 bis or present an ABCODE of 96h in V.34. The CONF register will contain C0h (K56flex/V.34) or 70h (V.32 bis/V.32) to indicate that a Cleardown was accomplished. If the MDP reconfigures from V.22 bis 2400 bps to V.22 1200 bps during a handshake or as a result of a retrain, the CONF register will contain 82h.

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
RTS	08h:0	0	**Request to Send.** When control bit RTS is set, the MDP transmits any data on TXD (TPDM = 0) or TBUFFER (TPDM = 1) when CTS becomes active. In V.22 bis, V.22, V.23, V.21, and Bell 103 constant carrier and in V.34, V.32 bis, and V.32 modes, RTS controls data transmission and DTR controls the carrier. For ease of use, RTS can be turned ON at the same time as DTR. In V.22 bis controlled carrier mode, RTS independently controls the carrier when DTR is ON. When RTS is turned ON, the MDP then transmits 270 ms of scrambled 1s before turning CTS ON. In V.21, V.23, V.23 HDX, and Bell 103 controlled carrier modes, RTS independently controls the carrier when DTR is ON. When RTS is turned ON, CTS is turned ON per Table 1-3. In V.33, V.17, V.29, V.27, and V.21 Ch 2 fax modes, RTS controls the training sequence transmission. The RTS bit parallels the operation of the RTS hardware control input. These inputs are ORed by the MDP. (See descriptions of CTS and DTR bits.)
RTSDE	02h:3	0	**Remote RTS Pattern Detector Enable.** When control bit RTSDE is set, the remote RTS pattern detector is enabled. RTSDE is available in synchronous and asynchronous modes. This bit is not valid in FSK modes. (See RTSDT).
RTSDT	0Fh:1	–	**Remote RTS Pattern Detected.** When set, status bit RTSDT indicates that the remote RTS signal is ON, otherwise it indicates that the remote RTS signal is OFF. This status bit is valid only when RTSDE is set. This status bit should be initialized by the host upon setting RTSDE. The MDP will automatically activate/de-activate the local RLSD signal in response to a change in the remote RTS signal. Detection is available in synchronous and asynchronous modes. This bit is not valid in FSK modes.
RXFNE	0Ch:1	-	**Receiver FIFO Not Empty.** When set, status bit RXFNE indicates that the receiver FIFO contains one or more bytes of data. When reset, bit RXFNE indicates that the receiver FIFO is empty. As long as RXFNE = 1 or RDBF = 1, there is receive data to be read, The host may use either bit. (TPDM = 1, FIFOEN = 1)
RXHF	01h:1	0	**Receiver FIFO Half Full.** When set, status bit RXHF indicates that there are 8 or more bytes in the 16-byte Receiver FIFO buffer. When reset, RXHF indicates that there are less than 8 bytes in the Receiver FIFO buffer. (TPDM = 1) An interrupt mask is available to allow an interrupt request to be generated when RXHF transitions from reset to set or from set to reset (the interrupt will occur as the FIFO fills above the half-full point and as the FIFO empties below the half-full point) (see Function 17 in Section 4).
RXP	01h:0	0	**Received Parity Bit.** This status bit is only valid when parity is enabled (PEN = 1), and word size is set for 8 bits per character (WDSZ = 11). In this case, the parity bit received (or ninth data bit) will be available at this location. The host must read this bit before reading the received data buffer (RBUFFER).
RXV	11h:3	0	**Receive Voice.** In a tone mode or DTMF receive mode (CONF = ACh, 80h, 81h, 83h, or 86h); control bit RXV = 1 selects receive voice ADPCM mode (CDEN = 1) or receive voice pass-through mode (CDEN = 0); RXV = 0 disables receive voice mode. In ADPCM receive mode (CDEN = 1), the MDP performs ADPCM coding. The coder output is placed into the Voice Receive Buffer (VBUFR). In receive voice pass-through mode (CDEN = 0), the host can directly access to the A/D converter. The host can obtain 16-bit voice samples from VBUFR at the selected sample rate (7200 Hz default). VBUFR reflects the receive voice sample when bit RDBF is set. (See VBUFR.)

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
S1DET	0Dh:5	–	**S1 Detector.** When set, status bit S1DET indicates that a V.22 bis S1 sequence has been detected. This bit is reset by the MDP at the end of the S1 sequence. (V.22 bis)
S511	02h:5	0	**Send 511.** When set, control bit S511 instructs the MDP to generate and transmit a 511 pattern in the current configuration. If bit V54T, V54P, or V54A is set while bit S511 is set, the 511 pattern will be temporarily interrupted in order to transmit the chosen V54 sequence. For the MDP to detect the 511 pattern, the host must first set up the sync time-out counter at address 0A5h using RAM access method 1 (see 4.2). The most significant bit enables or disables the 511 detection (1 = on) and bits 0-6 represent the sync time-out in byte times. A value of FFh in this location will enable the 511 detection and allow the maximum sync time-out. The 16-bit value read from address 0A7h contains the error count. Bits V54TE, V54PE, and V54AE must be reset in order for the 511 detection to function. (Synchronous modes only.)
SCIBE	1Ah:1	–	**Secondary Channel Input Buffer Empty.** When set, status bit SCIBE indicates that the secondary channel transmit buffer (SECTXB) is empty and ready for the next byte. The host must reset SCIBE after writing a new byte in SECTXB. See SECEN. (See SECEN.) (V.34, V.32 bis, V.32)
SCOBF	1Ah:2	–	**Secondary Channel Output Buffer Full.** When set, status bit SCOBF indicates that the secondary channel receive buffer (SECRXB) is full. The host must reset SCOBF after reading SECRXB. See SECEN. (V.34, V.32 bis, V.32)
SCR1	0Dh:4	–	**Scrambled Ones Detector.** When set, status bit SCR1 indicates that V.22 bis scrambled 1s have been detected during handshake. This bit is reset at the end of the scrambled 1s sequence. (V.22 bis, V.22, Bell 212)
SDET	0Ch:3	–	**S Detector.** When set, status bit SDET indicates that a S sequence has been detected. This bit is reset by the MDP at the end of the S sequence. (V.34, V.32 bis, V.32)
SECEN	1Ah:0	0	**Secondary Channel Enable.** When control bit SECEN is set the secondary channel is enabled. When SECEN is reset the secondary channel is disabled. Bit SECEN may be set in idle mode or during the V.32 bis/V.32 handshake prior to RLSD turning on. The secondary channel may be turned on or off in data mode by setting or resetting the SECEN bit and performing a retrain. (V.34 or V.32 bis/V.32 at 7200 bps or above.)
SECRXB	16h:7-0	–	**Secondary Receive Buffer.** The host obtains secondary channel data or V.34 receive handshake status information from the MDP receiver by reading a data byte from the SECRXB when bit SCOBF is set. (V.34, V.32 bis, V.32) SECRXB is also used in voice mode (see RXV). Also used to convey V.8, K56flex, and V.34 handshake status (see Section 9.4).
SECTXB	17h:7-0	–	**Secondary Transmit Buffer.** The host conveys secondary channel output data to the transmitter by writing a data byte to the SECTXB or obtains V.8, K56flex, and V.34 transmit handshake status information when bit SCIBE is set. (V.34, V.32 bis, V.32) In the transmit voice mode with the FIFO not enabled, SECTXB contains the low byte and VBUFT contains the high byte of the transmit voice sample. (See TXV and FIFOEN.) (Voice transmit mode).
SEPT	03h:6	0	**Short Echo Protector Tone.** When control bit SEPT is set, the echo protector tone duration is 30 ms; when reset, the echo protector tone duration is 185 ms. (V.33, V.17, V.29, V.27)
SFRES	1Ah:7	0	**Soft Reset.** When control bit SFRES is set to a 1, the MDP will perform power-on reset processing. The NEWC bit will be reset to a 0 by the MDP upon completion of the reset processing. NEWC must be set to initiate the reset. Wait for NEWC to clear plus 10 ms before accessing the MDP.

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
SLEEP	15h:7	0	**Sleep Mode.** When control bit SLEEP is set, the MDP is placed in sleep mode for reduced power consumption and the SLEEP pin is driven low. The MDP can be awakened only if bit RDWK and/or HWRWK is set. If both RDWK and HWRWK are reset, only a power-on-reset will bring the MDP out of sleep mode. The MDP is reset upon wake up.
SNDET	0Ch:2	–	**S Negative Detector.** When set, status bit SNDET indicates that a ~S sequence has been detected. This bit is reset at the end of the ~S sequence. (V.34, V.32 bis, V.32)
SPEED	0Eh:4-0	–	**Speed Indication.** In non-V.34 modes, the SPEED status bits indicate the receiver's and transmitter's data rate at the completion of a handshake. In K56flex and V.34 asymmetric modes, the SPEED status bits indicate the transmitter's data rate and the CONF bits indicate the receiver's data rate at the completion of a handshake. **SPEED (Hex) — Data Rate (bps)** 0 — 0–300 1 — 600 2 — 1200 3 — 2400 4 — 4800 5 — 9600 6 — 12000 7 — 14400 8 — 7200 9 — 16800 A — 19200 B — 21600 C — 24000 D — 26400 E — 28800 F — 31200 10 — 33600 11-1F — Reserved Also, see Function 1 in Section 4 for V.34.
SQDIS	02h:6	0	**Squarer Disable (Tone Detector C).** When control bit SQDIS is set, the squarer in front of tone detector C is disabled; when reset, the squarer is enabled. Disabling the squarer cascades the prefilter and filter C creating an 8th-order filter.

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
SRCEN	03h:5	0	**Secondary Rate Change Enable.** The MDP has a method of performing rate changes in V.34 which causes no interruption of primary data. This is a proprietary method and will only work if both MDPs are Rockwell data pumps. This compatibility is enforced by communicating the seamless rate change capability during the handshake. The rate change request is communicated over the MDP's secondary channel. The method to enable Seamless Rate Changes is: 1. Enable the seamless rate change indicator by setting bits 0 and 1 of address 3A5h. The status indicating remote seamless rate change capability is reflected in bit 103h:7. 2. Set bit SECEN. 3. Enable both asymmetric data rates and Framed Secondary Channel (bits 13Fh:6 and 39Bh:0, respectively). Asymmetric mode must be used for seamless rate change. 4. Make a connection. All RAM accesses are 8 bit. Check bit 103h:7 after the connection is complete. If set, the remote modem is capable of performing seamless rate changes. If not set, seamless rate changes should not be attempted. To invoke a seamless rate change, change CONF to the desired receive data rate and then set SRCEN. The CONF register and speed bits will be updated with the new data rate at the completion of the rate change. This feature should be used at the user's discretion.
STB	06h:2	0	**Stop Bit Number.** When control bit STB is reset, one stop bit is selected in asynchronous mode; when set, two stop bits are selected. This bit must be configured appropriately before the ASYN bit changes from a 0 to a 1 for asynchronous mode. (K56flex, V.34, V.32 bis, V.32, V.22, V.22 bis, Bell 212A)
STOFF	05h:1	0	**Soft Turn Off.** When control bit STOFF is set, the transmitter sends a tone at the end of a transmission in V.23, V.21, and Bell 103 configurations. This tone is detected as a mark frequency at the receiver. The soft turn off tone frequencies and durations are as follows: **Configuration** / **Frequency (Hz)** / **Duration (ms)** V.23/1200 — 900 — 7 V.21 Originate — 880 — 30 V.21 Answer — 1550 — 30 Bell 103 Originate — 1370 — 30 Bell 103 Answer — 2325 — 30
STRN	04h:0	0	**Short Train Select.** When a V.17 or V.27 configuration is selected in CONF, control bit STRN selects the training mode (1 = short train; 0 = long train). (V.17, V.27 ter) STRN may be set only after the completion of a successful long train. STRN may be set or reset during data mode (RLSD on) or anytime before the start of the following training sequence. Setting STRN will inhibit the equalizer taps from being reset during the following short train thus allowing for a fast adaptation. A short train may be received only when STRN is set. Once STRN is set, the DATA bit must remain set and the only allowable configuration between V.17 and V.27 that will not alter the taps is V.21 Channel 2. (V.17, V.27 ter)
SYNCD	0Ah:0	0	**Sync Pattern Detected.** When set, status bit SYNCD indicates that SDLC/HDLC flags (7E pattern) are being detected. When reset, the 7E pattern is not being detected. SYNCD is cleared when the first data byte of the current frame is received in RBUFFER. This bit is valid only in SDLC/HDLC mode (HDLC = 1). In voice receive mode, SYNCD = 1 is used to trigger on the first low byte (see Figure 11-3).

Table 3-1. Interface Memory Bit Definitions (Cont'd)

<table>
<tr><th>Mnemonic</th><th>Location</th><th>Default</th><th>Name/Description</th></tr>
<tr><td>TBUFFER</td><td>10h:7-0</td><td>00</td><td>Transmit Data Buffer. The host conveys output data to the transmitter in the parallel mode by writing a data byte to the TBUFFER. Parallel data mode is available in both synchronous and asynchronous modes. The data is transmitted bit 0 first (see TDBE). NOTE: Do not read TBUFFER during data mode. RTS must = 1.</td></tr>
<tr><td>TDE</td><td>02h:7</td><td>1</td><td>Tone Detectors Enable. When control bit TDE is set, tone detectors A, B, and C are enabled; when reset, tone detectors are disabled.</td></tr>
<tr><td>TDBE</td><td>1Eh:3</td><td>–</td><td>Transmit Data Buffer Empty. When set, status bit TDBE signifies that the MDP has read TBUFFER (10h) and the host can write new data into TBUFFER. This condition can also cause IRQ to be asserted. The host writing to TBUFFER resets the TDBE and TDBIA bits. If the host does not write new data into TBUFFER, the MDP sends mark. TDBE must be a 1 before switching between synchronous, asynchronous, or HDLC modes. CTS must be on before data is loaded into TBUFFER. If FIFOEN is set, TDBE, when set, indicates that the transmit FIFO is empty (128-byte extension disabled) or that more data may continue to be written to TBUFFER (128-byte extension enabled). (See TDBIE and TDBIA.)</td></tr>
<tr><td>TDBIA</td><td>1Eh:7</td><td>–</td><td>Transmit Data Buffer Interrupt Active. When the transmit data buffer interrupt is enabled (TDBIE is set) and register 10 is empty (TDBE is set), the MDP asserts IRQ and sets status bit TDBIA to indicate that TDBE being set caused the interrupt. The host writing to register 10 resets the TDBIA bit and clears the interrupt request due to TDBE. (See TDBIE and TDBE.)</td></tr>
<tr><td>TDBIE</td><td>1Eh:5</td><td>0</td><td>Transmit Data Buffer Interrupt Enable. When control bit TDBIE is set (interrupt enabled), the MDP will assert IRQ and set the TDBIA bit when TDBE is set by the MDP. When TDBIE is reset (interrupt disabled), TDBE has no effect on IRQ or TDBIA. (See TDBE and TDBIA.)</td></tr>
<tr><td>TEOF</td><td>11h:1</td><td>0</td><td>HDLC Transmit End of Frame. When operating in HDLC with FIFOEN = 1, the host must set control bit TEOF to inform the transmitter that the corresponding data is the last byte in a frame. TEOF must be set prior to loading the last byte in TBUFFER. The host must reset TEOF prior to loading the next data byte. In voice transmit mode, TEOF is used to sync the ADPCM decoder (see Section 10). (HDLC = 1, TPDM = 1, FIFOEN = 1)</td></tr>
<tr><td>TLVL</td><td>13h:7-4</td><td>9</td><td>Transmit Level. The TLVL code selects the transmitter analog output level at the TXA pin as follows:
<table>
<tr><th>TLVL Code (Hex)</th><th>TX Output Level (dBm ±0.5 dB) [VAA = +3.3V]</th><th>TX Output Level (dBm ±0.5 dB) [VAA = +5V]</th></tr>
<tr><td>0</td><td>-4.0</td><td>0</td></tr>
<tr><td>1</td><td>-5.0</td><td>-1.0</td></tr>
<tr><td>2</td><td>-6.0</td><td>-2.0</td></tr>
<tr><td>3</td><td>-7.0</td><td>-3.0</td></tr>
<tr><td>4</td><td>-8.0</td><td>-4.0</td></tr>
<tr><td>5</td><td>-9.0</td><td>-5.0</td></tr>
<tr><td>6</td><td>-10.0</td><td>-6.0</td></tr>
<tr><td>7</td><td>-11.0</td><td>-7.0</td></tr>
<tr><td>8</td><td>-12.0</td><td>-8.0</td></tr>
<tr><td>9</td><td>-13.0</td><td>-9.0</td></tr>
<tr><td>A</td><td>-14.0</td><td>-10.0</td></tr>
<tr><td>B</td><td>-15.0</td><td>-11.0</td></tr>
<tr><td>C</td><td>-16.0</td><td>-12.0</td></tr>
<tr><td>D</td><td>-17.0</td><td>-13.0</td></tr>
<tr><td>E</td><td>-18.0</td><td>-14.0</td></tr>
<tr><td>F</td><td>-19.0</td><td>-15.0</td></tr>
</table>
The host can fine tune the transmit level by changing a value in DSP RAM.
Not applicable to Speakerphone Mode (CONF = ACh).</td></tr>
</table>

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
TM	0Fh:2	–	**Test Mode.** When set, status bit TM indicates that the MDP is in RDL test mode. The TM bit will be set when RLSD turns off at the start of RDL, and will reset less than 100 ms prior to RLSD turning back on at the end of RDL. (V.22 bis, V.22, Bell 212A)
TONEA	0Bh:7	–	**Tone A Detected.** When set, status bit TONEA indicates that energy is present on the line within the tone detector A passband and above its threshold. The bandpass filter coefficients are host programmable in DSP RAM.
TONEB	0Bh:6	–	**Tone B Detected.** When set, status bit TONEB indicates that energy is present on the line within the tone detector B passband and above its threshold. The bandpass filter coefficients are host programmable in DSP RAM.
TONEC	0Bh:5	–	**Tone C Detected.** When set, status bit TONEC indicates that energy is present on the line within the tone detector C passband and above its threshold. The bandpass filter coefficients are host programmable in DSP RAM. The TONEC filter is preceded by a squarer in order to facilitate detection of difference tones. This squarer may be disabled with the SQDIS bit (see SQDIS bit).
TPDM	08h:6	0	**Transmitter Parallel Data Mode.** When control bit TPDM is set, the MDP accepts data for transmission from the TBUFFER (10h) rather than the TXD input. (See TDBE and RTS.) **Note:** The TPDM bit must be set to a 1 in HDLC mode (HDLC bit = 1).
TXCLK	13h:1-0	0	**Transmit Clock Select.** The TXCLK control bits designate the origin of the transmitter data clock. NEWC must be set to initiate TXCLK change. The TXCLK encoding is: **TXCLK** **Transmit Clock** 0 Internal 2 External (XTCLK) 3 Slave (~RDCLK) When the external clock is selected, an external clock **must** be supplied to the XTCLK input pin. The external clock signal must have a duty cycle of 50% and must be within ±0.01% of the nominal TDCLK frequency (the actual frequency of TDCLK as measured when internal clock is selected). TDCLK will be phase locked to XTCLK when the external clock option is selected. When the slave clock is selected, the transmitter clock (TDCLK) is phase locked to the receiver clock (~RDCLK).
TXFNF	0Dh:1	-	**Transmitter FIFO Not Full.** When set, status bit TXFNF indicates that the transmitter FIFO is not full and the host may continue to write data to the TBUFFER. When reset, TXFNF indicates that the transmitter FIFO is full. (TPDM = 1, FIFOEN = 1)
TXHF	01h:2	0	**Transmitter FIFO Half Full.** When set, status bit TXHF indicates that there are 8 or more bytes in the 16-byte Transmitter FIFO buffer. When reset, TXHF indicates that there are less than 8 bytes in the Transmitter FIFO buffer. (TPDM = 1, FIFOEN = 1) An interrupt mask is available to allow an interrupt request to be generated when TXHF transitions from reset to set or from set to reset (the interrupt will occur as the FIFO fills above the half-full point and as it empties below the half-full point) (see Section 4, Function 17).
TXP	11h:0	0	**Transmit Parity Bit (or 9th Data Bit).** Control bit TXP contains the stuffed parity bit (or ninth data bit) for transmission when parity is enabled (PEN = 1), stuff parity is selected (PARSL = 00), and word size is set for 8 bits per character (WDSZ = 11). The host must load the stuffed parity bit (or 9th data bit) into TXP before loading the other 8 bits of data in TBUFFER.

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
TXSQ	05h:4	0	**Transmitter Squelch.** When control bit TXSQ is set, the transmitter analog output is squelched. All other transmitter functions continue as normal. When TXSQ is reset, the transmitter output functions normally. It is recommended that TXSQ be set while in the fax receive mode.
TXV	11h:4	0	**Transmit Voice.** In a tone mode or DTMF receive mode (CONF = ACh, 80h, 81h, 83h, or 86h), control bit TXV = 1 selects transmit voice ADPCM mode (DCDEN = 1) or transmit voice pass-through mode (DCDEN = 0); TXV = 0 disables transmit voice mode. In transmit voice ADPCM mode (DCDEN = 1), the MDP performs ADPCM decoding on the contents of the Voice Transmit Buffer (VBUFT). In transmit voice pass-through mode (DCDEN = 0), the host can directly access to the D/A converter. The host may send voice samples to the MDP at the selected sample rate (7200 Hz default). The MDP will accept voice samples from VBUFT when the FIFO is enabled or from VBUFT (high byte) and SECTXB (low byte) when the FIFO is not enabled. (See FIFOEN and VBUFT.)
U1DET	0Dh:3	–	**Unscrambled 1s Detector.** When set, status bit U1DET indicates that V.22 bis unscrambled 1s sequence has been detected. This bit is reset by the MDP at the end of the unscrambled 1s sequence. U1DET is not active when DATA is reset. (V.22 bis)
VAGC	04h:2	0	**Voice AGC.** In receive voice mode (RXV = 1), the host can enable (VAGC = 1) or disable (VAGC = 0) the voice AGC.
V21S	08h:5	0	**V21 Synchronous.** In V.21 configuration (CONF = A0h), control bit V21S selects either synchronous (V21S = 1) or asynchronous (V21S = 0) mode. In V.21 synchronous mode, a synchronous transmit clock is provided on the TDCLK pin and a synchronous receive clock is provided on the ~RDCLK pin. During transmit, synchronous data may be applied in either serial or parallel form depending on the TPDM bit. During receive, synchronous data is output in both serial or parallel form. NEWC must be set immediately after changing the V21S bit to initiate the mode change. **Note:** Do **not** set this bit in V.21 Channel 2 (CONF = A8h).
V23HDX	11h:2	0	**V.23 Half Duplex.** When control bit V23HDX is set, the MDP operates in V.23 /1200 half duplex. The transmitter and receiver must be set to the same V.23 configuration, 1200 bps (CONF = A4h). Carrier is under RTS control and DTR must be on. The RTS-CTS delay is adjustable in RAM.
V54A	08h:3	0	**V.54 Acknowledgment Signaling.** When control bit V54A is set, and provided that CTS is ON, the transmitter will send a pattern of 1948 bits produced by scrambling a binary 1 with the polynomial $1+x^{-4}+x^{-7}$ in accordance with ITU-T Recommendation V.54. The transmission will be at the modem data signaling rate. When transmission of the signaling pattern is complete, V54A is automatically reset by the MDP. V.54 signaling pattern detection is available in both synchronous and asynchronous modes. (Not valid in FSK modes.)
V54AE	02h:1	0	**V.54 Acknowledgment Phase Detector Enable.** When control bit V54AE is set, the V.54 acknowledgment phase detector is enabled in the receiver. V.54 signaling pattern detection is available in both synchronous and asynchronous modes. (See V54DT). (Not valid in FSK modes.)

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
V54DT	0Fh:0	0	**V.54 Pattern Detected.** When set, status bit V54DT indicates that one of the three V.54 patterns is being detected. Only one of the three detector enabling bits (V54PE, V54AE or V54TE) must be set by the host at any given time. V54DT should be reset by the host after detection. V.54 signaling pattern detection is available in both synchronous and asynchronous modes. (Not valid in FSK modes.)
V54P	08h:2	0	**V.54 Preparatory Signaling.** When control bit V54P is set and CTS is ON, the transmitter will send a pattern of 2048 bits produced by scrambling a binary 0 with the polynomial $1+x^{-4}+x^{-7}$ in accordance with ITU-T Recommendation V.54. The transmission will be at the modem data signaling rate. When the transmission of the signaling pattern is complete, V54P is automatically reset by the MDP. V.54 signaling pattern detection is available in both synchronous and asynchronous modes. (Not valid in FSK modes.)
V54PE	02h:0	0	**V.54 Preparatory Phase Detector Enable.** When control bit V54PE is set, the V.54 preparatory phase detector is enabled in the receiver. V.54 signaling pattern detection is available in both synchronous and asynchronous modes. (See V54DT). (Not valid in FSK modes.)
V54T	08h:4	0	**V.54 Termination Signaling.** When control bit V54T is set, and provided that CTS is ON, the transmitter will send a pattern of 8192 bits produced by scrambling a binary 1 with the polynomial $1+x^{-4}+x^{-7}$ followed by 64 binary 1s in accordance with ITU-T Recommendation V.54. The transmission will be at the modem signaling rate. When transmission of the signaling pattern is complete, V54T is automatically reset by the DSP. V.54 signaling pattern detection is available in both synchronous and asynchronous modes. (Not valid in FSK modes.)
V54TE	02h:2	0	**V.54 Termination Phase Detector Enable.** When control bit V54TE is set, the V.54 termination phase detector is enabled in the receiver. V.54 signaling pattern detection is available in both synchronous and asynchronous modes. (See V54DT). (Not valid in FSK modes.)
VBUFR	00h:7-0	–	**Voice Receive Buffer.** In voice receive mode (RXV = 1), VBUFR contains one of two consecutive bytes of the 16-bit output voice sample. The first byte read is the low byte; the second byte read is the high byte. (See RXV.) (Receive voice only.)
VBUFT	10h:7-0	–	**Voice Transmit Buffer.** In voice transmit mode (TXV = 1), VBUFT contains one of two consecutive bytes of the 16-bit input voice sample. The first byte written is the low byte; the second byte written is the high byte. When the FIFO is not enabled in the voice transmit mode, VBUFT contains the high byte of the 16-bit input voice sample while SECTXB contains the low byte of the 16-bit input voice sample. (See TXV and FIFOEN.) (Transmit voice only.)
VOLUME	01h:7-6	0	**Volume Control.** The encoded VOLUME control bits select speaker off or one of three volume attenuation levels (at RIN) as follows: **B7 B6 Description** 0 0 Speaker off 1 0 Speaker attenuation = 0 dB (high volume) 0 1 Speaker attenuation = 6 dB (medium volume) 1 1 Speaker attenuation = 12 dB (low volume)

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
VPAUSE	01h:5	0	**Voice Pause.** Control bit VPAUSE enables (1) or disables (0) the voice "pause." When VPAUSE is enabled, voice data is not output to the host.
WDSZ	06h:1-0	0	**Data Word Size.** he WDSZ field sets the number of data bits per character in asynchronous mode as follows (V.34, V.32 bis, V.32, V.22, V.22 bis, Bell 212A): **B1 B0 Data Bits/Character** 0 0 5 1 0 6 0 1 7 1 1 8 These bits must be configured appropriately before the ASYN bit changes from a 0 to a 1 for asynchronous mode.

Table 3-2. ABCODE Error Code Definitions

Value (Hex)	Description	Mode
01	FED turned off while waiting to get into round trip delay estimate (RTDE)	V.32
10	Unexpected E-sequence, do retrain	V.32
11	Timed out in rate renegotiation	V.34
21	Timed out waiting for INFO0	V.34
22	Checksum error in INFO0	V.34
23	Timed out waiting for tone A or B	V.34
24	Timed out waiting for first phase reversal	V.34
25	Timed out waiting for probing cut-off tone	V.34
26	Timed out waiting for second phase reversal	V.34
27	Timed out waiting for end of probing	V.34
28	Timed out waiting for third phase reversal	V.34
29	Timed out waiting for INFO1	V.34
2A	Checksum error in INFO1	V.34
2B	Send repeated INFO0	V.34
2C	Found unexpected INFO0	V.34
81	FED turned off during RTDE	V.32
82	Lost track of AC/AA/CA/CC during RTDE	V.32
84	Timed out waiting for S sequence, 1st ORG	V.32
85	Timed out waiting for S sequence, 2nd ORG	V.32
86	Timed out waiting for S sequence, 1st ANS	V.32
8C	FED turned off during TRN-sequence, 1st ORG	V.32
8D	FED turned off during TRN-sequence, 2nd ORG	V.32
8E	FED turned off during TRN-sequence, 1st ANS	V.32
90	R1 not detected	V.32
91	R2 not detected	V.32
92	R3 not detected	V.32
93	R4/R5 not detected	V.32
94*	Timed out looking for end of S-seq, 1st ORG	V.32
95*	Timed out looking for end of S-seq, ANS	V.32
96	Received rate sequence called for Cleardown	V.32
97	E-sequence not detected	V.32
C0	Problem with S-sequence in EC-training signal	V.34
C1	FED turned off during S-sequence in EC-training signal	V.34
C2	S-sequence turned off before expected in phase 3	V.34
C3	Timed out waiting for S-Sbar in phase 3	V.34
C4	Timed out waiting for S-Sbar in phase 3	V.34
C5	Timed out waiting for S in phase 3	V.34
C6	J-sequence not detected in phase 3	V.34

Table 3-2. ABCODE Error Code Definitions (Cont'd)

Value (Hex)	Description	Mode
D0	Problem with S-sequence in phase 4	V.34
D1	FED turned off during S-sequence in phase 4	V.34
D2	S-sequence turned off before expected in phase 4	V.34
D3	Timed out waiting for S-Sbar in phase 4	V.34
D4	Timed out waiting for S-Sbar in phase 4	V.34
D5	Timed out waiting for S in phase 4	V.34
D6	Timed out waiting for MP	V.34
D7	Timed out waiting for MP'	V.34
D8	Timed out waiting for E	V.34
D9	JP-sequence not detected	V.34
DA	Timed out in transmitter rate renegotiation	V.34
DB	Reserved	
DC	K56flex timed out looking for energy	K56flex
DD	K56flex timed out in phase 3	K56flex
E2	Retrain detected during phase 2	V.34
E3	Retrain detected during phase 3	V.34
E4	Retrain detected during phase 4	V.34
FE	DTR turned off during training	V.34
FF	Transmitter abort	V.34

4. DSP RAM ACCESS

The MDP DSP contains a 16-bit wide random access memory (RAM). The host processor can access (read or write) the RAM through a 12-bit memory address in registers 1D and 1C.

4.1 INTERFACE MEMORY ACCESS TO DSP RAM

The interface memory acts as an intermediary during host to DSP RAM or DSP RAM to host data exchanges. The address stored in interface memory RAM address registers MEADDH and MEADDL by the host is the DSP RAM address for data access. The data is transferred through data registers MEDAM and MEDAL.

One or two bytes (1 byte = 8 bits) are transferred between DSP RAM and DSP interface memory once each device cycle. The DSP operates at a 7200 Hz sample rate.

The RAM access bit (MEACC) in the interface memory instructs the DSP to access the RAM. The transfer is initiated by the host setting the MEACC bit. The DSP tests this bit each sample period.

RAM can be accessed using one of four methods:

1. 8-bit read - 8-bit write.
2. 16-bit read - 8-bit write.
3. 16-bit read - 16-bit write.
4. 16-bit read only (MDP diagnostics).

Parameters transferred under the first method have only 8 bits of significance. The data is written to and read from MEDAL. Data in MEDAM is ignored.

Parameters transferred using the second method have 16 bits of significance but can be written only 8 bits at a time. These parameters have two access codes associated with them, one for the least significant 8-bits and one for the most significant 8 bits. The host need read only the low address to obtain both the most significant and the least significant bytes of the data if the two access codes are in consecutive order.

Parameters transferred using the third method involve 16-bit read or write operations using one access code.

Finally, all diagnostic read operations using the fourth method use only one access code. Data is read from MEDAM and MEDAL.

The parameters available in DSP RAM are listed in Table 4-1.

Table 4-1. Interface Memory RAM Addresses

No.	Function	Method	Address (Hex)
1	K56flex/V.34 Transmitter and K56flex/V.34 Receiver Speeds		
	K56flex/V.34 Transmitter Speed	1	2E5
	K56flex/V.34 Receiver Speed	1	2E4
2	Rate Sequence		
	Received R	4	208
	Received E	4	20A
	Transmitted R	2 (RO)	205, 204 (see Note 1)
	Transmitted E	2 (RO)	207, 206 (see Note 1)
	V.32/V.32 bis R1 Mask	2	2C1, 2C0 (see Note 1)
	V.32/V.32 bis R2 Mask	2	2C3, 2C2 (see Note 1)
	V.32 bis R4 Mask	2	2C5, 2C4 (see Note 1)
	V.32 bis R5 Mask	2	2C7, 2C6 (see Note 1)
	V.33 R33 Mask	2	2C9, 2C8 (see Note 1)
3	DTMF Tone Duration	2	2DB, 218 (see Note 1)
4	DTMF Interdigit Delay	2	2DC, 219 (see Note 1)
5	DTMF Low Band Power Level	2	29C, 29B (see Note 1)
6	DTMF High Band Power Level	2	29E, 29D (see Note 1)
7	Pulse Relay Make Time	1	22C
8	Pulse Relay Break Time	1	21C
9	Pulse Interdigit Delay	2	21B, 21A
10	Calling Tone On Time	2	2D9, 290 (see Note 1)
11	Calling Tone Off Time	2	2DA, 291 (see Note 1)
12	Transmitter Output Level Gain (G)		
	Transmitter Output Level Gain (G) - All Modes	2	3DB, 3DA
	Transmitter Output Level Gain (G) - FSK Modes	3	B57
13	Dual Tone 1 Frequency	2	281, 280 (see Note 1)
14	Dual Tone 2 Frequency	2	283, 282 (see Note 1)
15	Dual Tone 1 Power Level	2	285, 284 (see Note 1)
16	Dual Tone 2 Power Level	2	287, 286 (see Note 1)
17	New Status (NEWS) Masking Registers		
	Masking Register for 01	1	247
	Masking Register for 0A and 0B	2	246, 245
	Masking Register for 0C and 0D	2	244, 243
	Masking Register for 0E and 0F	2	242, 241
	Masking Register for 12 (set bit 7 to enable interrupt)	1	089:7
	Masking Register for 14	1	38A
	Masking Register for 16	1	370
	Masking Register for 17	1	371
	Masking Register for 1A and 1B	2	27D, 27C
	Masking Register for Memory Access		
	(Set bit 6 to disable interrupt)	1	089:6
22	Far-End Echo Frequency Offset	4	852
23	Far-End Echo Level	4	B52
24	CTS OFF-to-ON Response Time (RTS–CTS Delay)	2	203, 202 (see Note 1)
25	Answer Tone Length	2	229, 228 (see Note 1)
26	Silence after Answer Tone Period	2	22B, 22A (see Note 1)
27	Tone Detector A Bandpass Filter Coefficients	3	See Table 4-6
28	Tone Detector B Bandpass Filter Coefficients	3	See Table 4-6
29	Tone Detector C Bandpass Filter Coefficients	3	See Table 4-6
30	RLSD Drop Out Timer	1	270 and 271
31	RLSD Turn-On Threshold (RLSD_ON)	2	135, 134
32	RLSD Turn-Off Threshold (RLSD_OFF)	2	137, 136
	RLSD Threshold Offset	2	139, 138
	RLSD Overwrite Control	1	10D:2
	Extended RTH Control	1	10D:6

Table 4-1. Interface Memory RAM Addresses (Cont'd)

No.	Function	Method	Address (Hex)
34	V.32 PN Length	2	289, 288 (see Note 1)
36	AGC Gain Word	4	A00
37	Round Trip Far Echo Delay	4	239
45	Equalizer Frequency Correction	4	811
46	Eye Quality Monitor (EQM)	4	20C
47	Maximum Period of Valid Ring Signal	1	21F
48	Minimum Period of Valid Ring Signal	1	21E
49	Phase Jitter Frequency	4	80E
50	Phase Jitter Amplitude	4	80D
51	Guard Tone Level	3	B46
52	ITU-T CRC 32 Select	1	0B3:0
53	Secondary Channel Transmitter Speed Select	1	28E
	Secondary Channel Receiver Speed Select	1	28B
60	V.34 Symbol Rate Value	1	2E3
61	V.34 Baud Rate Mask (BRM)	1	101
62	V.34 Pre-Emphasis Value	4	B44
63	V.34 Pre-Emphasis Override	1	0E6
	V.34 Pre-Emphasis Disable (PREDIS)	1	100:1
64	V.34 Transmit Level Deviation Disable (TLDDIS)	1	100:3
68	EQM Above Threshold	1	133
69	ARA-in-RAM Enable	1	3A5:4
	EQM Scale Factor (Gain)	3	A29
70	V.21/V.23 CTS Mark Qualify	1	10D:3
73	No Automode to FSK	1	13F:0
74	Receive FIFO Trigger Level	1	32C
	Transmit FIFO Extension Enable	1	702:0
	Receive FIFO Extension Enable	1	701:0
81	V.34 Spectral Parameters Control	1	105
82	V.34 Phase 2 Power Reduction	1	0E2
85	V.34 Data Rate Mask	2	383, 382
	K56flex/V.34 Transmitter Maximum Data Rate Mask	1	605
	K56flex/V.34 Receiver Maximum Data Rate Mask	1	604
86	K56flex/V.34 Asymmetric Data Rates Enable	1	13F:6
87	V.34 Remote Mode Data Rate Capability	2 (RO)	209, 208
	V.34 Remote Modem Asymmetric Data Rate Indicator	1 (RO)	209:7
88	V.8 Status Registers - See Section 9		
	V.8 Status Register 1	1	301
	V.8 Status Register 2	1	302
	V.8 Status Register 3	1	303
89	V.8 Control Registers - See Section 9		
	V.8 Control Register 1	1	304
	V.8 Control Register 2	1	305
	V.8 Control Register 3	1	306
	V.8 Control Register 4	1	307
	V.8 Control Register 5	1	308
90	Modulation Modes- See Section 9		
	V.34 Full-Duplex configuration - See Section 9	1	309
	V.32 bis configuration	1	30B
	V.22 bis configuration	1	30C
	V.17 configuration	1	30D
	V.29 configuration	1	30E
	V.27 configuration	1	30F
	Reserved	1	310
	Reserved	1	311
	V.23 Full-Duplex configuration	1	312
	V.23 Half-Duplex configuration	1	313
	V.21 configuration	1	314
91	V.8 MaxFrameByteCount- See Section 9	1	31C
92	V.8 Call Functions- See Section 9	1	32A

Table 4-1. Interface Memory RAM Addresses (Cont'd)

No.	Function	Method	Address (Hex)
93	CM/JM/CI Frame - See Section 9		
	SYNC CM/JM/CI	1	32D
	Data Call Function	1	32E
	Modulation 0	1	32F
	Modulation 1	1	330
	Modulation 2	1	331
	Protocol (optional)	1	332
	GSTN (optional)	1	333
	Frame End	1	334
100	Minimum On Time (DTMF)	3	E96
101	Minimum Off Time (DTMF)	3	C96
102	Minimum Cycle Time (DTMF)	3	D96
103	Minimum Dropout Time (DTMF)	3	F96
104	Maximum Speech Energy (DTMF)	3	E95
105	Frequency Deviation, Low Group (DTMF)	3	C94
106	Frequency Deviation, High Group (DTMF)	3	E94
107	Negative Twist Control, TWIST4 (DTMF)	3	D95
108	Positive Twist Control, TWIST8 (DTMF)	3	C95
109	Maximum Energy Hit Time (DTMF)	3	E87
110	ADC Speech Sample Scaling Parameter, ADCS (ADPCM)	3	F21

Notes:

1. High address = MSB of data; low address = LSB of data.
2. The host may access only the X or Y data on any given read cycle, i.e., X and Y data cannot be accessed simultaneously.
3. RO = read-only.

4.2 HOST DSP READ AND WRITE PROCEDURES

DSP RAM Write Procedure

1. Set MEMW to inform the DSP that a RAM write will occur when MEACC is set.
2. Load the RAM address into the MEADDH and MEADDL registers.
3. Write the desired data into the interface memory RAM data registers MEDAM and/or MEDAL.
4. Set MEACC to signal the DSP to perform the RAM write.
5. When the DSP has transferred the contents of the interface memory RAM data registers into RAM, the MDP resets the MEACC bit and sets the NEWS bit to indicate DSP RAM write completion. If the NSIE bit is a 1, IRQ is asserted and NSIA is set to inform the host that setting of the NEWS bit is the source of the interrupt request.
6. Upon the completion of IRQ servicing, write a 0 into the NEWS bit to clear the NSIA bit and to negate IRQ if no other interrupt requests are pending.

DSP RAM Read Procedure

1. Reset MEMW to inform the DSP that a RAM read will occur when MEACC is set.
2. Load the RAM address code into the MEADDH and MEADDL registers.
3. Set MEACC to signal the DSP to perform the RAM read.
4. When the DSP has transferred the contents of RAM into the interface memory RAM data registers MEDAM and/or MEDAL, the MDP resets the MEACC bit and sets the NEWS bit to indicate DSP RAM read completion. If the NSIE bit is a 1, IRQ is asserted and NSIA is set to inform the host that setting of the NEWS bit is the source of the interrupt request.
5. Upon the completion of IRQ servicing, write a 0 into the NEWS bit to clear the NSIA bit and to negate IRQ if no other interrupt requests are pending.

4.3 RAM READ AND WRITE EXAMPLES

Figure 4-1 shows a flowchart of a procedure to change the DTMF tone duration using method 1.

Figure 4-2 shows a flowchart of a procedure to change the RTS-CTS delay using method 2.

Figure 4-3 shows a flowchart of a procedure to change the THRESHU value for TONEA using method 3.

Figure 4-4 shows a flowchart of a procedure to read EQM using method 4.

4.4 CHANGES TO RAM ADDRESSES

Some previously defined RAM locations were changed to optimize internal RAM usage. The addresses affected are those above CXX (all are 16-bit access):

Old Address (Hex)	New Address (Hex)
CXX	48XX (bit 1Dh:6 is set as an extension to MEADDH)
E00-E1B	C80-C9B
E1C-E7F	C1C-C7F
E80-E9B	D80-D9B
E9C-EFF	D1C-D7F
F00-F1B	E80-E9B
F1C-F7F	E1C-E7F
F80-F9B	F80-F9B (no change)
F9C-FFF	F1C-F7F

Note: Old addresses in the range of CXX were often used in RCV288DPX and RCV336ACF workarounds. The old FXXh and EXXh addresses were found under the voice AGC and DTMF detection parameters.

The method for reading and writing RAM remains unchanged.

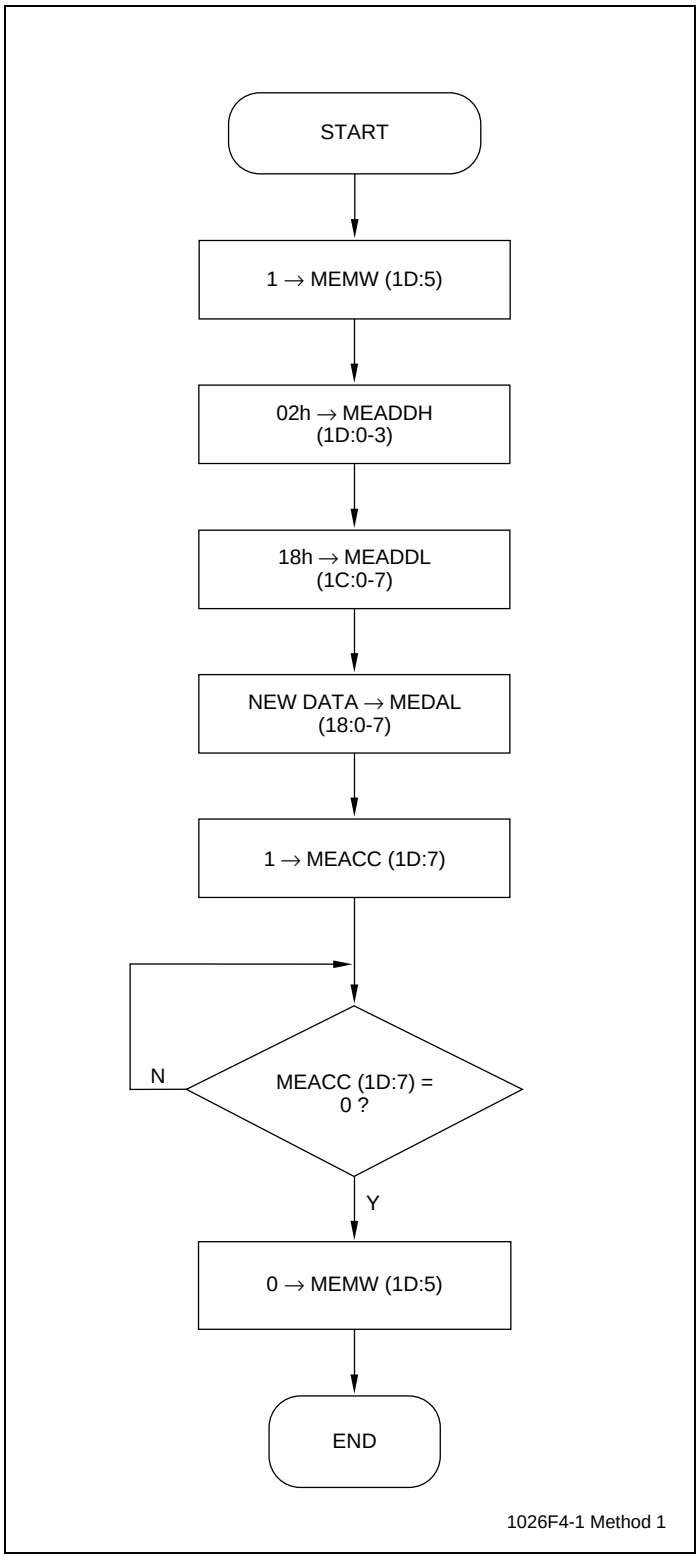


Figure 4-1. Method 1 Example - Changing DTMF Tone Duration (LSB)

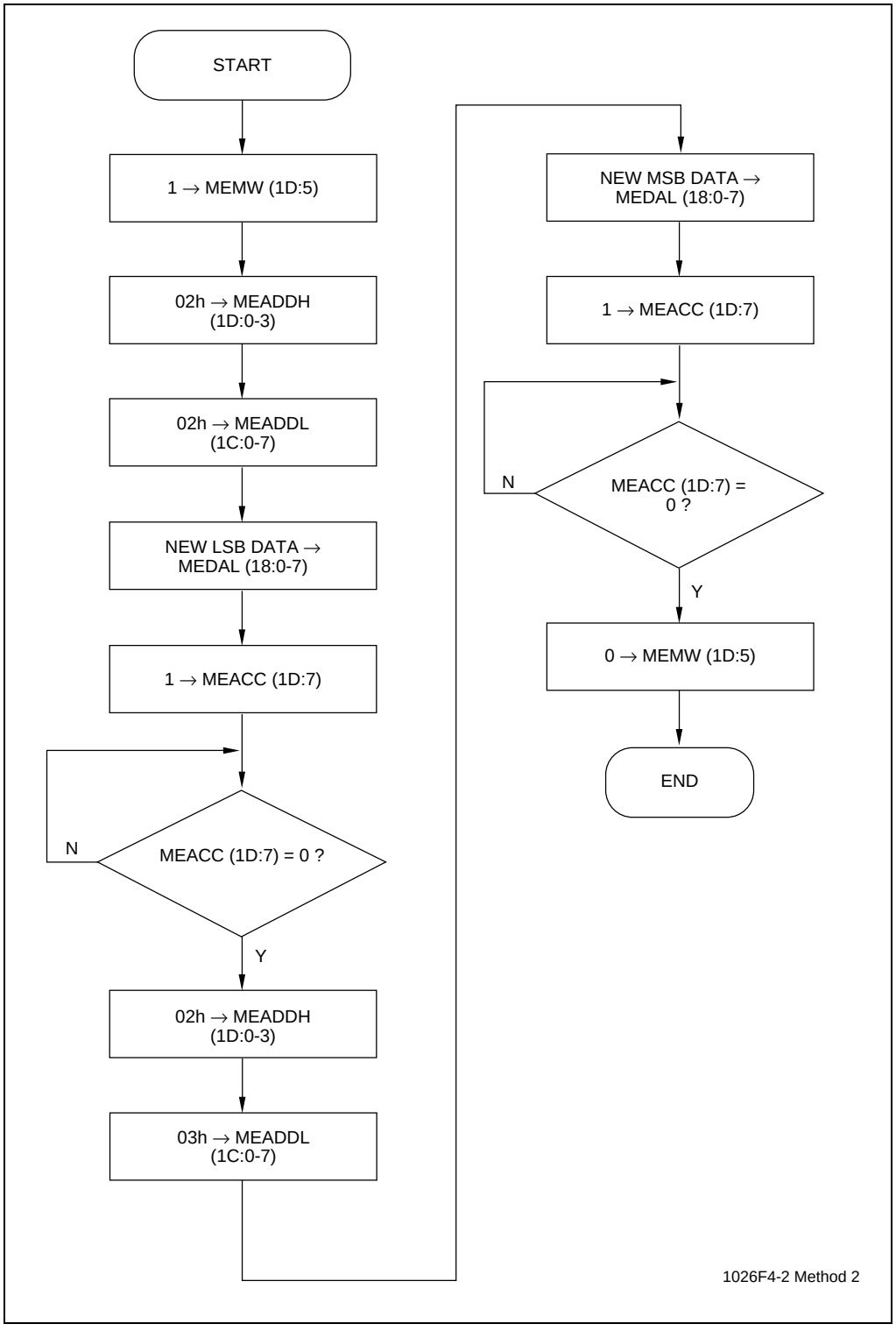


Figure 4-2. Method 2 Example - Changing RTS-CTS Delay

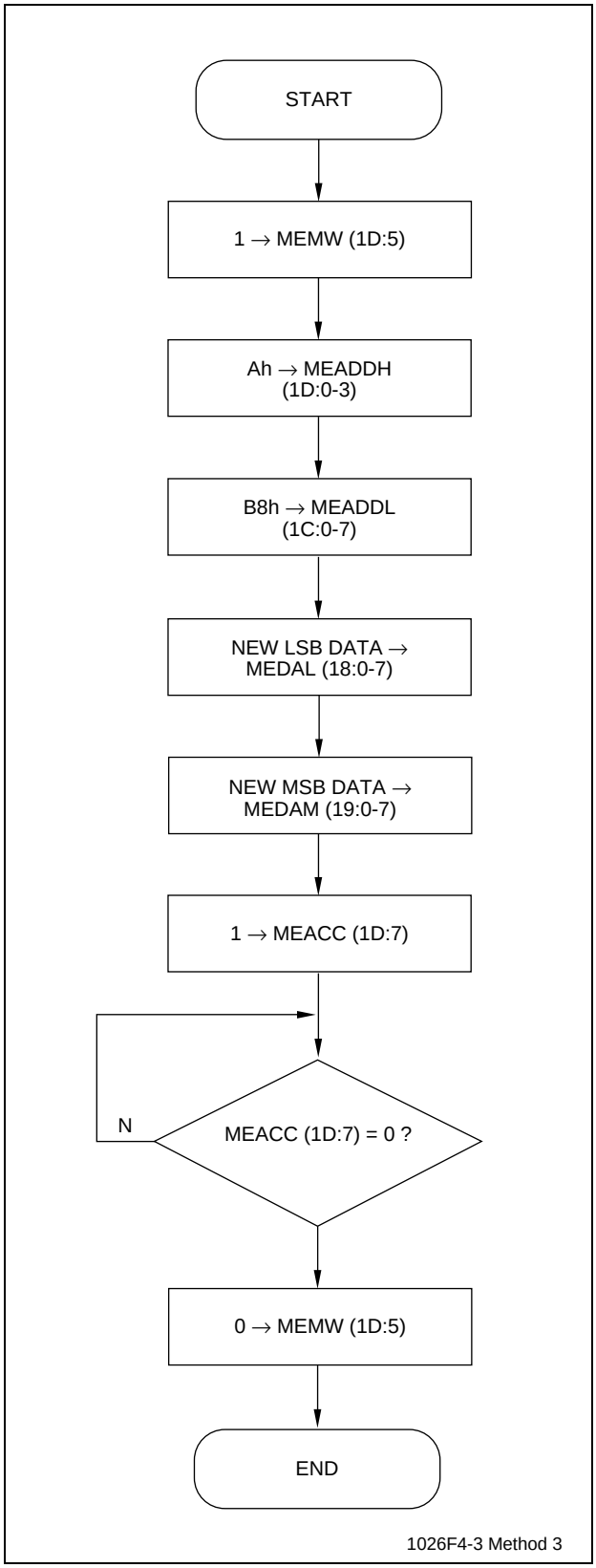


Figure 4-3. Method 3 Example - Changing TONEA THRESHU

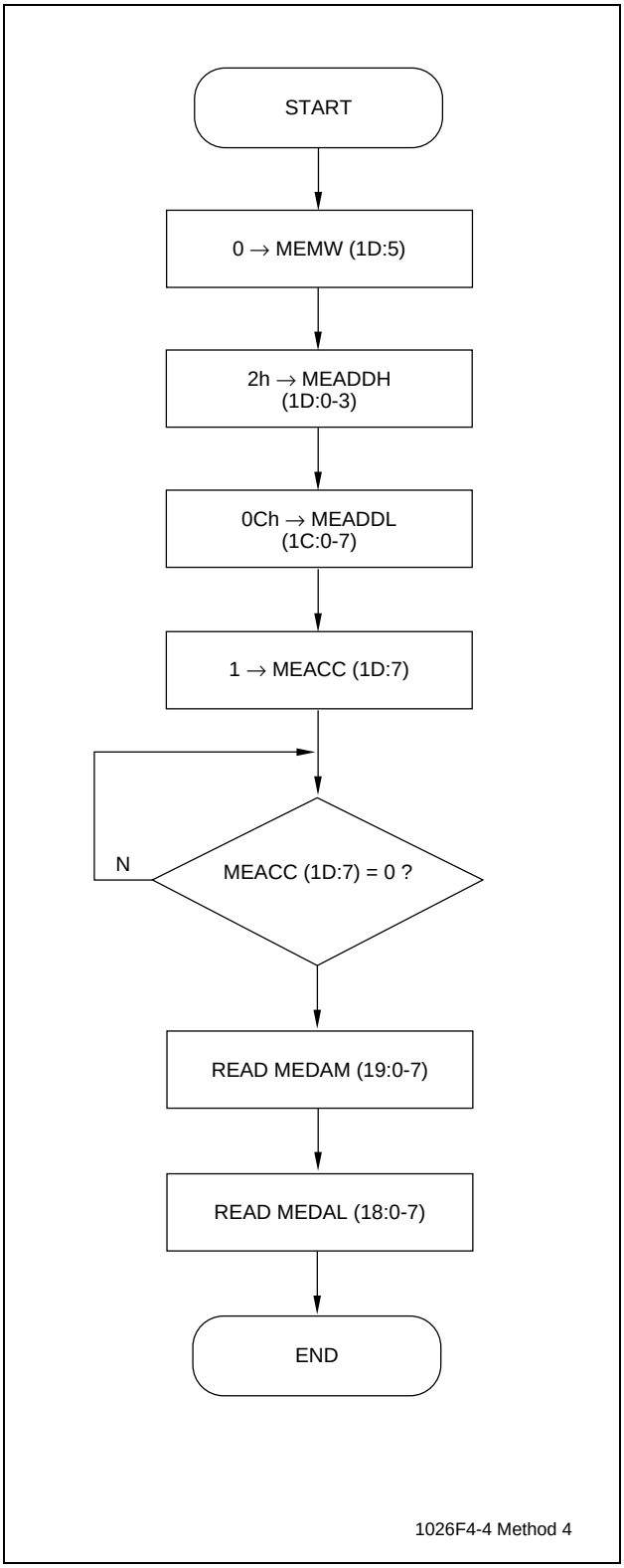


Figure 4-4. Method 4 Example - Reading EQM

4.5 DSP RAM DATA SCALING

Function 1: **K56flex/V.34 Transmitter Speed** **Acc. Method: 1** **Addr.: 2E5h**
K56flex/V.34 Receiver Speed **Acc. Method: 1** **Addr.: 2E4h**

When connected in K56flex or V.34, the current transmitter and receiver speeds may be read from 2E5h and 2E4h, respectively. These locations are updated after each handshake, retrain or rate renegotiation.

The speeds are reported as follows:

2E5h or 2E4h Value	K56flex/V.34 Transmitter Speed (2E5h) or V.34 Receiver Speed (2E4h) (kbps)	K56flex Receiver Speed (2E4h) (kbps)
0E	33.6	Reserved
0D	31.2	56
0C	28.8	54
0B	26.4	52
0A	24.0	50
09	21.6	48
08	19.2	46
07	16.8	44
06	14.4	42
05	12.0	40
04	9.6	38
03	7.2	36
02	4.8	34
01	2.4	32

Function 2: V.32 bis and V.33 Rate Sequence **Acc Method: Table 4-1** **Addr. 208h-2C9h**

V.32 bis Rate Sequence Bits. ITU-T defines the V.32 bis rate sequence bits as follows:

BIT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DATA	0	0	0	0	1	X	X	1	1	X	X	1	X	0	0	1

B0 = MSB; B15 = LSB

Bit	Description
B0-B3, B7, B11, B15	For synchronizing on rate signal
B4	A 1 (Note 1)
B8	A 1 (Note 1)
B5	A 1 denotes the ability to receive at 4800 bps
B6	A 1 denotes the ability to receive at 9600 bps
B9	A 1 denotes the ability to receive at 7200 bps
B10	A 1 denotes the ability to receive at 12000 bps
B12	A 1 denotes the ability to receive at 14400 bps
B13, B14	0,0 (Note 2)

Notes

1. When B4 or B8 is set to zero in a transmitted or received rate signal, then interworking can proceed only in accordance with Recommendation V.32.
2. B13 and B14 shall be set to zero when transmitting and ignored during the reception of a rate signal; they are reserved for future definition by the ITU-T and must not be used by the manufacturers.
3. B4-B6, B9-B10, B12 set to zero calls for a GSTN Cleardown.

V.32 Rate Sequence Bits. ITU-T defines the V.32 rate sequence bits as follows:

BIT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DATA	0	0	0	0	1	X	X	1	1	X	X	1	X	0	0	1

B0 = MSB; B15 = LSB

Bit	Description
B0-B3, B7, B11, B15	For synchronizing on the rate sequence
B4	A 1 denotes the ability to receive at 2400 bps
B5	A 1 denotes the ability to receive at 4800 bps
B6	A 1 denotes the ability to receive at 9600 bps
B4-B6	0 0 0 calls for a GSTN clear down
B8	A 1 denotes the ability of trellis encoding and decoding at the highest data rate indicated in B3-B6.
B9-B14	0 0 1 0 0 0 denotes absence of special operational modes.

Note

When using the MDP in a 7200 bps or 12000 bps proprietary configuration, B9 = 1 denotes the ability to receive at 7200 bps and B10 = 1 denotes the ability to receive at 12000 bps.

V.33 Rate Sequence Bits. ITU-T defines the V.33 rate sequence bits as follows:

For B14 = 0:

BIT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DATA	0	0	0	0	X	X	X	1	X	X	X	1	X	X	0	1

B0 = MSB; B15 = LSB

Bit	Description
B0-B3, B7, B11, B15	For synchronizing on the rate sequence
B4-B6, B10, B12, B13	Not defined
B8	A 1 denotes the ability to receive at 12000 bps
B9	A 1 denotes the ability to receive at 14400 bps

For B14 = 1:

BIT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DATA	0	0	0	0	X	X	X	1	X	X	X	1	X	X	1	1

B0 = MSB; B15 = LSB

Bit	Description
B0-B3, B7, B11, B15	For synchronizing on the rate sequence
B4, B5	A 00 denotes that B6, B10, B12, and B13 define multiplexer configuration selection
B8	A 1 denotes the ability to transmit and receive at 12000 bps
B9	A 1 denotes the ability to transmit and receive at 14400 bps
B6, B10, B12, B13	Multiplexer configuration selection (see the V.33 specification for multiplexer configurations)

The V.32 and V.33 rate sequences contain undefined codes and/or bits. The user can use these bits to convey information to the remote modem during training (e.g., remote configuration, multiplexer configuration, test mode configuration, etc.).

The 16-bit rate sequence word in the MDP's RAM corresponds exactly to the 16-bit rate sequences defined in V.32 and V.33. The MSB of the word in RAM is B0 of the rate sequence and the LSB is B15 of the rate sequence.

V.32/V.32 bis Rate Sequence

The V.32/V.32 bis rate sequence is available in RAM during the handshake when the RSEQ bit is a 1. The RSEQ bit will turn on when the E-sequence is available as well. The rate sequence(s) and E-sequence are read from two different RAM locations (see Table 4-1 Function 2). The RSEQ bit must be reset by the host after reading the rate sequence(s).

The host may modify the rate sequence in one of two ways.

Method 1 Description. The first and simplest method is to use the rate sequence mask (see Table 4-1, Function 2). The rate sequence masks are available for R1, R2, R4, and R5. Rate sequences R1 and R2 are used during the initial handshake and retrains; R4 and R5 are used during rate renegotiations. The mask written to the appropriate RAM location will be logically ANDed to the out-going rate sequence. A power-on-reset will clear the masks to FFFFh.

Example of Method 1. To request or limit the modem speed to 9600 bps, the host would write 0B91h (see page 4-8 for rate sequence bit assignments) to address 2C1h, 2C0h if R1 is to be modified. The same value could be written to address 2C5h, 2C4h if R4 is to be modified to limit the speed during a rate renegotiation. The available rates of the remote must be considered by the host before limiting speeds. If the MDP determines no common rate is available between both modems during a rate change, the MDP will send a clear down and turn off RLSD.

Method 2 Description. The second method for modifying the rate sequence is compatible with the RC144DP and is accomplished through address 205h, 204h. R1 and R3 are sent by the answering modem and R2 is sent by the originating modem.

To modify R1, the host must write a 0 at this address then wait for the value to equal non-zero. The host then has 1.5 seconds to change R1 (through address 205h, 204h) before it is sent.

To modify R2, the host must wait until the RSEQ bit is set to a 1 by the DSP. The host then has 1.5 seconds to modify R2 (through address 205h, 204h).

To modify R3, the host must wait until the RSEQ bit is set to a 1 by the DSP, then change R3 (through address 205h, 204h).

In the case of rate renegotiations, R4 (sent by the requesting modem) is modified in the same manner as R3 after setting the RREN bit. R5 (sent by the responding modem) is also modified in the same manner after RREDT is set. The host has approximately 5 ms to modify R4 or R5 after the value in address 205h, 204h equals zero.

Typical rate sequences and E sequences shown in Table 4-2 (V32BS = 0) and Table 4-3 (V32BS = 1). The ARC bit is set on both modems. R1 and R3 are read on the originating modem, R2 is read on the answering modem. Refer to Section 5.3 of ITU-T Recommendation V.32/V.32 bis for additional information on the V.32/V.32 bis rate sequence.

Table 4-2. R and E Rate Sequences - V.32 to V.32 (V32BS = 0)

Originate Set at	R1 (Hex)	R2 (Hex)	R3 (Hex)	E (Hex) (ANS and ORG)	Answering Configuration	Resulting Configuration
V.32T/9600	0791	0791	0391	F391	V.32T/9600	V.32T/9600
	0711	0711	0311	F311	V.32/9600	V.32/9600
	0511	0511	0511	F511	V.32/4800	V.32/4800
V.32/9600	0791	0711	0311	F311	V.32T/9600	V.32/9600
	0711	0711	0311	F311	V.32/9600	V.32/9600
	0511	0511	0511	F511	V.32/4800	V.32/4800
V.32/4800	0791	0511	0511	F511	V.32T/9600	V.32/4800
	0711	0511	0511	F511	V.32/9600	V.32/4800
	0511	0511	0511	F511	V.32/4800	V.32/4800

Table 4-3. R and E Rate Sequences - V.32 bis to V.32 bis (V32BS = 1)

Originate Set at	R1 (Hex)	R2 (Hex)	R3 (Hex)	E (Hex) (ANS and ORG)	Answering Configuration	Resulting Configuration
V.32T/14400	0FF9	0FF9	0999	F999	V.32T/14400	V.32T/14400
	0FF1	0FF1	09B1	F9B1	V.32T/12000	V.32T/12000
	0FD1	0FD1	0B91	FB91	V.32T/9600	V.32T/9600
	0DD1	0DD1	09D1	F9D1	V.32T/7200	V.32T/7200
	0D91	0D91	0D91	FD91	V.32/4800	V.32/4800
V.32T/12000	0FF9	0FF1	09B1	F9B1	V.32T/14400	V.32T/12000
	0FF1	0FF1	09B1	F9B1	V.32T/12000	V.32T/12000
	0FD1	0FD1	0B91	FB91	V.32T/9600	V.32T/9600
	0DD1	0DD1	09D1	F9D1	V.32T/7200	V.32T/7200
	0D91	0D91	0D91	FD91	V.32/4800	V.32/4800
V.32T/9600	0FF9	0FD1	0B91	FB91	V.32T/14400	V.32T/9600
	0FF1	0FD1	0B91	FB91	V.32T/12000	V.32T/9600
	0FD1	0FD1	0B91	FB91	V.32T/9600	V.32T/9600
	0DD1	0DD1	09D1	F9D1	V.32T/7200	V.32T/7200
	0D91	0D91	0D91	FD91	V.32/4800	V.32/4800
V.32T/7200	0FF9	0DD1	09D1	F9D1	V.32T/14400	V.32T/7200
	0FF1	0DD1	09D1	F9D1	V.32T/12000	V.32T/7200
	0FD1	0DD1	09D1	F9D1	V.32T/7200	V.32T/7200
	0DD1	0DD1	09D1	F9D1	V.32T/7200	V.32T/7200
	0D91	0D91	0D91	FD91	V.32/4800	V.32/4800
V.32/4800	0FF9	0D91	0D91	FD91	V.32T/14400	V.32T/4800
	0FF1	0D91	0D91	FD91	V.32T/12000	V.32T/4800
	0FD1	0D91	0D91	FD91	V.32T/9600	V.32T/4800
	0DD1	0D91	0D91	FD91	V.32T/7200	V.32T/4800
	0D91	0D91	0D91	FD91	V.32/4800	V.32/4800

Functions 3-11: Dialing Parameters **Acc. Method: See Below** **Addr.: See Below**

For Functions 3, 4, 7, 8, and 9, the time T (in ms) is calculated as follows:

Equation: N = T x 2.4 Not in Speakerphone Mode
N = 1.76 In Speakerphone Mode (CONF = ACh)

Where: N is the decimal value of the hex number written to RAM (1-FFh).

A value of 0000 for the DTMF or calling tone on time will cause the MDP to transmit the tone continuously until FFh is written into TBUFFER.

For functions 10 and 11, the time (in ms) is calculated as follows:

Equation: N = T/10

For Functions 5 and 6, the DTMF low band or high band power level (P) in dBm is calculated as follows:

Equation: $N = \log^{-1}(P/20) \times 10143$

Where: N is the decimal value of the hex number written to RAM.

Notes:

1. The compromise equalizer is automatically disabled by the transmitter when sending DTMF tones, single tones, or dual tones. The DTMF levels are not affected by the transmit level bits (TLVL). The calling tones, however, are affected by the TLVL bits.
2. Maximum output power = -0.5 dBm.

The dialing parameters and their default values are:

Function	Parameter	Method	Address (Hex)	Default (Hex)	Default (Dec)
3	DTMF Tone Duration	1	2DB, 218	00DD	92 ms
4	DTMF Interdigit Delay	1	2DC, 219	00AD	72 ms
5	DTMF Low Band Power Level	2	29C, 29B	19C0	-4.0 dBm
6	DTMF High Band Power Level	2	29E, 29D	2085	-2.0 dBm
7	Pulse Relay Make Time	1	22C	56	36 ms
8	Pulse Relay Break Time	1	21C	99	64 ms
9	Pulse Interdigit Delay	2	21B, 21A	0708	750 ms
10	Calling Tone On Time	1	2D9, 290	0032	500 ms
11	Calling Tone Off Time	1	2DA, 291	012C	3 sec

Some DTMF power level values are:

L (dBm)	N (Hex)
–1	2350
–2	1F78
–3	1C0C
–4	1900
–5	1648
–6	13DB

Function 12: Transmitter Output Level Gain-All Modes **Acc. Method: 2** **Addr.: 3DBh, 3DAh**
Transmitter Output Level Gain-FSK Modes **Acc. Method: 3** **Addr.: B57h**

Transmitter Output Level Gain-All Modes (Addr. 3DBh, 3DAh)

The transmitter output level gain constant (G) in dBm is calculated as follows:

Equation: $N = \log^{-1} [G/20] \times 16384$

Where: N is the decimal value of the hex number written to RAM.

Range: 0 - 7FFFh

Default: 4000h

NEWC must be set for the new gain value to take effect. The contents of 3DBh, 3DAh are copied to A48h (16 bits) which may also be used to directly control the transmit level.

The transmitter output level gain constant directly controls the output level of all configurations. It is used for fine tuning the output level which is controlled by the TLVL bits. Therefore,

Output Level = TLVL Setting + Transmitter Output Gain in dBm

Example gain values are:

G (dBm)	N (Hex)	G (dBm)	N (Hex)
+6	7FB2	-8	197A
+5	71CF	-9	16B5
+4	656E	-10	143D
+3	5A67	-11	1209
+2	5092	-12	1013
+1	47CF	-13	0E53
0	4000	-14	0CC5
–1	390A	-15	0B61
–2	32D6	-16	0A24
–3	2D4E	-17	090A
–4	2861	-18	080E
–5	23FD	-19	072E
-6	2013	-20	0666
-7	1C96	-21	05B4

For example, if TLVL is set for -9 dBm and the required level is -30 dBm, the difference is -21 dBm. Therefore, load addresses 3DBh and 3DAh with 05h and B4h, respectively.

The dynamic range of the scale factor is effective from +6 dB down to approximately -60 dB, with a resolution of 0.5E-3 dB.

Transmitter Output Level Gain-FSK Modes (Addr. B57h)

Equation: $N = \log^{-1} [PO/20] \times C$

Where: PO is based on TLVL = 9 and transmit output gain constant (all modes) and A48h = 4000h.

N is the decimal value of the hex number written to RAM.

C = See the following table:

Configuration	CEQ	C (Dec) - Answer	C (Dec) -Originate
V.21	CEQ = 1	9728	10608
	CEQ = 0	8448	8448
Bell 103	CEQ = 1	9072	10496
	CEQ = 0	8704	8352
V.23/1200 TX	CEQ = 1	12800	12800
	CEQ = 0	12544	12544
V.23/75 TX	CEQ = 1	10496	10496
	CEQ = 0	8448	8448

Setting NEWC to a 1 will reset this parameter to the default value.

Function 13: Dual Tone 1 Frequency **Acc. Method: 2** **Addr.: 281h, 280h**
Function 14: Dual Tone 2 Frequency **Acc. Method: 2** **Addr.: 283h, 282h**

Frequency F (in Hz) is calculated as follows:

Equation: N = F/0.109863

Where: N is the decimal value of the hex number written to RAM.

Default = 0

A single or dual tone is transmitted by writing 80h (single tone) or 83h (dual tone) to the CONF register, programming the tone transmit location in RAM, and then activating RTS. The tone will be transmitted as long as RTS is active.

Example values are:

F (Hz)	N (Hex)	F (Hz)	N (Hex)
400	0E39	2100	4AAB
445	0FD2	2250	5000
600	1555	2400	5555
1200	2AAB	3000	6AAB
1800	4000	3600	8000

Function 15: Dual Tone 1 Power Level **Acc. Method: 2** **Addr.: 285h, 284h**
Function 16: Dual Tone 2 Power Level **Acc. Method: 2** **Addr.: 287h, 286h**

Dual tone power level in dBm (PO) is calculated as follows:

Equation: $N = 22304\ [10^{Po/20}]$ (Based on TLVL = 0 and 600 Ω termination.)

Where: N is the decimal value of the hex number written to RAM.

Range: 0 - 7FFFh (Default = 2000h)

Notes:

1. The MDP accepts change only when RTS is off.
2. The Transmit Level bits (TLVL) affect output level.
3. Power out = PO + TLVL setting + transmitter output gain constant.

Function 17A: New Status (NEWS) Masking Registers **Acc. Method: See Table 4-1** **Addr.: See Below**
Function 17B: Memory Access Masking Register **Acc. Method: 1** **Addr.: 089h:6**

Writing a 1 in the bit location corresponding to the desired bit will cause NEWS to go active when a status change occurs for the selected bit. All bits default to 0 at power-on-reset. Figure 4-5 shows the applicable masking register bits.

In addition, bit 089h:6 controls memory access interrupt (set 089h:6 to disable interrupt; reset 089h:6 to enable interrupt).

Register Address	Bit 7	6	5	4	3	2	1	0	Mask Address (Hex)
1B	EDET	DTDET	OTS	DTMFD	DTMFW				27C
1A	—	—	—	—	DTMFW	SCOBF	SCIBE	—	27D
17	Secondary Transmit Data Buffer/V.34 Transmit Status(SECTXB)								371
16	Secondary Receive Data Buffer/V.34 Receive Status (SECRXB)								370
14	ABCODE								38A
12	Configuration (CONF)								089, bit 7 = 1
0F	RLSD	FED	CTS	DSR	RI	TM	RTSDT	V54DT	241
0E	RTDET	BRKD	RREDT	SPEED					242
0D	P2DET	PNDET	S1DET	SCR1	U1DET	—	TXFNF	—	243
0C	AADET	ACDET	CADET	CCDET	SDET	SNDET	RXFNE	RSEQ	244
0B	TONEA	TONEB	TONEC	ATV25	ATBEL	—	DISDET	EQMAT	245
0A	PNSUC	FLAGDT	PE	FE	OE	CRCS	FLAGS	SYNCD	246
01	—		—	—	—	TXHF	RXHF	—	247

Figure 4-5. NEWS Masking Registers

Function 22: Far-End Echo Frequency Offset **Acc. Method: 4** **Addr.: 852h**

Function 22 provides the far-end echo frequency offset (FO), sometimes known as phase roll, in V.34/V.32 configurations.

Equation: $FO = (N * SYMBOL\ RATE)/2^{22}$

Where: SYMBOL RATE = 2400, 2800, 3000, 3200, or 3429 (V.34) (See Function 60.)

2400 (V.32 bis)

N is the decimal value of the hex number read from RAM.

Function 22 is a 16-bit 2s complement number. It is not valid until rate sequence R3 is detected in the originate modem, or rate sequence R2 is detected in the answer modem for V.32 or until RLSD = 1 for V.34.

Function 23: Far-End Echo Level **Acc. Method: 4** **Addr.: B52h**

Function 23 provides the far-end echo power level at RXA in V.34/V.32 configurations.

The following table lists average values read from RAM and the corresponding far end echo level in dBm:

Echo Level (dBm)	V.34 Average Value (Hex)	V.32 bis Average Value (Hex)
-8	1100	1300
-9	0F00	1100
-10	0D00	0F00
-11	0C00	0D00
-12	0A00	0C00
-13	0900	0A00
-15	0700	0800
-20	0400	0500
-25	0250	0300
-30	0150	0180
-35	00C0	00D0
-40	0070	0080
-45	0045	0040

Note: Function 23 is not valid until RLSD is ON.

Function 24: CTS OFF-to-ON Response Time (RTS-CTS Delay) **Acc. Method: 2** **Addr.: 203h, 202h**

Function 24 determines the CTS off-to-on response time in 2-wire full-duplex configurations.

The response time equations and default values are:

Configuration	Equation	Default Value (Hex)	Default Value (Dec)
K56flex, V.34, V.32	N = (Response time x 2.4 ms) –1	0000	0.4 ms
V.22 bis, V.22, Bell 212A	N = (Response time x 0.6 ms) –1	0000	3 ms
Bell 103	N = (Response time x 0.298 ms) –1	003F	215 ms
V.21	N = (Response time x 0.298 ms) –1	0098	525 ms
V.23/1200Tx	N = Response time x 1.2 ms	00FC	210 ms
V.23/75Tx	N = Response time x 0.072 ms	0010	235 ms
Where: N is the decimal value of the hex number written to RAM.			

Example: For an RTS-CTS delay of 20 ms in V.22 bis, N = [(20)(0.6)]-1 = 11 = 000Bh.

Notes:

1. Response time may vary by ± 2 baud times.
2. Function 24 is not applicable in V.33, V.17, V.29, V.27 and V.21 Ch 2.

Function 25: Answer Tone Length **Acc. Method: 2** **Addr.: 229h, 228h**
Function 26: Silence After Answer Tone Period **Acc. Method: 2** **Addr.: 22Ah, 22Bh**

The ITU-T 2100 Hz answer tone length and silence after answer tone are calculated as follows:

Configuration	Equation
V.8, V.32, V.21, Bell 103	N = T x 300 (V.32 silence: N = T x 2400)
V.22 bis, V.22, Bell 212	N = T x 600
V.23/75Tx, V.23/1200Rx	N = T x 75
V.23/1200Tx, V.23/75Rx	N = T x 1200
Where: N is the decimal value of the hex number written to RAM and T is the time is seconds.	

The MDP will rewrite the default values when DTR is turned off or the NEWC bit is set.

The end of answer tone transmission may be determined by monitoring bit 051h:3. This bit will be set to a 1 when the answer has finished and the silence period has commenced. Unless a power-on reset is performed, this bit must be reset by the host if it is to be monitored again on the following connection.

Note: Address 229h, 228h lengthens individual phase reversal times in V.8/V.32 bis/V.32. The answer tone length may be adjusted by increasing or decreasing the number of phase reversals at address 04Bh. The default value at address 04Bh is 08h (8 phase reversals). This value may be changed only after DTR is set.

Functions 27 - 29: Tone Detector Bandpass Filter Coefficients **Acc. Method: 3** **Addr.: See Table 4-4**

A block diagram of the three tone detectors is shown in Figure 4-6. Tone detector C is preceded by a prefilter and a squarer. The purpose of the prefilter and squarer is to allow dual tones to be detected while rejecting the main channel energy. For example, TONEC can be programmed to detect a difference frequency generated by the squarer for detection of 350 Hz and 440 Hz. The prefilter would be designed to reject the energy in the 600 to 3000 Hz band. If the dual tone pair of 350 and 440 Hz appeared (or any other frequency pair in the range of 300 to 600 Hz with a difference of 90 Hz) TONEC would turn on.

The SQDIS bit (02h:6) allows the squarer in front of tone detector C to be disabled. If the squarer is disabled then tone detector C will have four cascaded biquads (since there is a prefilter consisting of two biquads), forming an 8-order IIR filter with user programmable coefficients. To make the prefilter transparent (to use TONEC as a 4th order filter), write 7FFFh in coefficients A1 and write 0000 to all other biquad coefficients.

The implementation of the filters allows user definition of the characteristics of the prefilter and the three tone detectors. Table 4-4 provides the DSP RAM address codes for the filter coefficients. Table 4-5 shows the default values. Figure 4-6 shows that the prefilter and the main filter sections of the tone detectors are fourth order (two second-order biquads in cascade), thereby allowing a wide variety of filter characteristics to be synthesized. The only limitation on these user-definable shapes is that their gain should be around unity at the pass frequencies to avoid problems of saturation at one extreme (gain too high) and digital noise at the other (gain too low). Computation of the filter coefficients can be performed by any infinite impulse response (IIR) filter design program which outputs the coefficients in cascaded second-order sections.

The default sample rate is 7200 Hz, however, in the V.8/V.34 mode, the sample rate is changed to 9600 Hz and all filter coefficients are changed by the MDP. A soft or hard reset is recommended after a V.34 connection to restore default filter coefficients.

The level detector in each of the tone detectors flags the detection of a tone if it is in the tone detector passband and if it is above an upper threshold defined by THRESHU. The tone detected flag will remain set until, or unless, the tone falls below a lower threshold defined by THRESHL.

The tone detectors are preceded by an AGC. The gain of the AGC may be read at address 8B9h (DUGAIN). By default, DUGAIN reaches its maximum gain, at a value of 7FFFh, when the receive level is -26 dBm or lower. Signal levels below -26 dBm are thus not affected by the AGC, therefore, the threshold comparator will see a decreasing signal level as the input signal is lowered. The THRESHU and THRESHL adjustments are limited to signal levels below the AGC cut-off point (-26 dBm). If the THRESHU value is adjusted to try to limit the detection threshold to -20 dBm, the AGC will not allow it.

To raise the AGC cut-off point, decrease the value in address BBB (DAGCRF). The DAGCRF default value is FF00h, which results in the -26 dBm cut-off. Decreasing DAGCRF to FE00h raises the AGC cut-off to -20 dBm, thus allowing THRESHU to be adjusted for a minimum detection level of -20 dBm or lower.

The AGC may be disabled by first writing 0 to address 9BBh (DSRATE), then writing a 07FFh to address 8B9h (DUGAIN).

The first-order low pass filter in each level detector, defined by the coefficients LPGAIN and LPFBK, controls the response time of each tone detector. Normally, these coefficients will not require alteration, but if, for example, a rapid cadence must be detected on a tone, then the 3 dB cutoff is approximately the reciprocal of the on-time or off-time of the tone, whichever is shorter. Decreasing LPFBK will speed up the response time. If LPFBK is decremented, then LPGAIN should be increase by the same amount. The gain of the filter should be set to unity (LPGAIN + LPFBK Å 7FFFh). The default response time is in the order of 0.01 seconds.

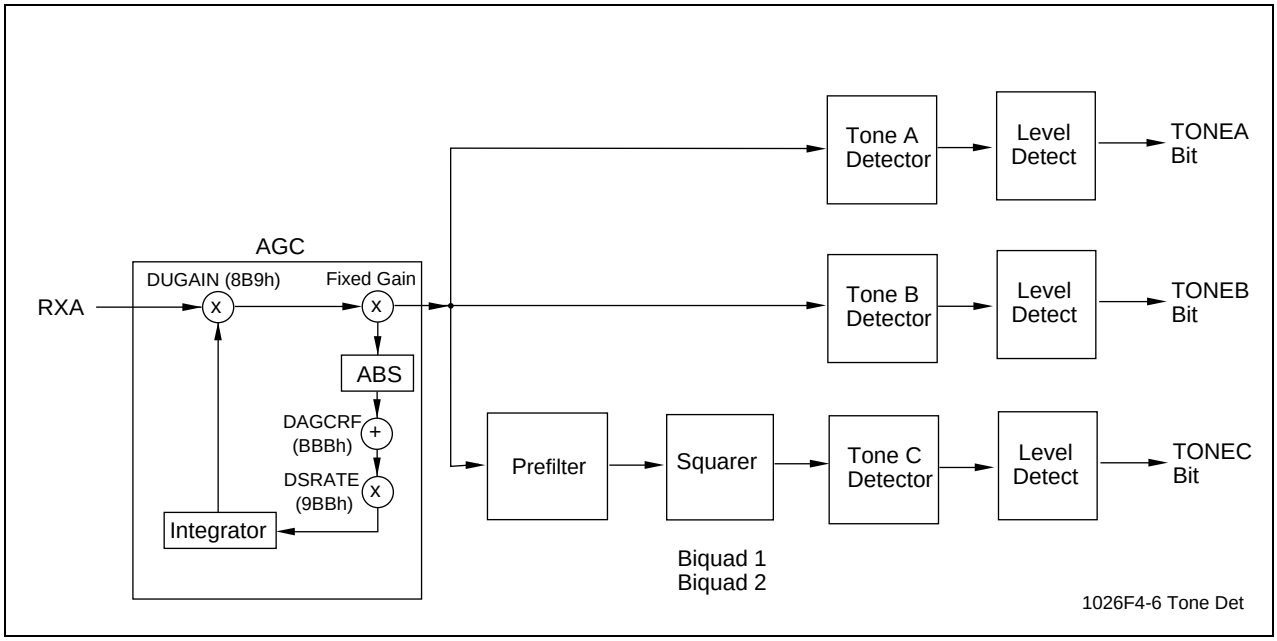


Figure 4-6. Tone Detectors

Table 4-4. TONEA, TONEB, and TONEC DSP RAM Addresses (Hex)

	TONEA		TONEB		TONEC		Prefilter	
Parameter	Biquad1	Biquad2	Biquad1	Biquad2	Biquad1	Biquad2	Biquad1	Biquad2
A3	AA1	BA1	AA7	BA7	AAD	BAD	AB2	BB2
A2	AA2	BA2	AA8	BA8	AAE	BAE	AB3	BB3
A1	AA3	BA3	AA9	BA9	AAF	BAF	AB4	BB4
B2	AA4	BA4	AAA	BAA	AB0	BB0	AB5	BB5
B1	AA5	BA5	AAB	BAB	AB1	BB1	AB6	BB6

Table 4-5. TONEA, TONEB, and TONEC Default Values (Hex)

	TONEA		TONEB		TONEC	
Parameter	Address	Value (Hex)	Address	Value (Hex)	Address	Value (Hex)
LPFBK	BA0	7F30	BA6	7E67	BAC	7F30
LPGAIN	AA0	00CF	AA6	02DF	AAC	00CF
THRESHU	AB8	0880	AB9	2A00	ABA	1600
THRESHL	BB8	0580	BB9	1C00	BBA	0A00

Example:

A call-progress tone detector is required for the US telephone network to detect appropriate tones that exceed –35 dBm.

Solution:

The requirement can be met by detecting tones in the 245 Hz-650 Hz range. A bandpass filter with a passband of 245 Hz-650 Hz must be designed. Any filter up to fourth order can be implemented and, normally, it is best to choose the highest order available, especially for bandpass designs. A biquad filter design package could carry out this function by defining the passband frequencies, the filter order, the filter gain (chose unity), and the filter sampling rate (7200 Hz). An example of suitable coefficients is:

Function	A1	A2	A3	B1	B2
Biquad 1	0.1368	–0.2736	0.1368	1.8281	–0.8835
Biquad 2	0.1368	0.2736	0.1368	1.5716	–0.7920

These values should first be divided by two because coefficients greater than one are unrealized in the actual filter implementation. This division should be done even if none of the coefficients in the design are greater than one. This is because the biquad sections have been implemented as shown in Figure 4-7. The modified values are, therefore:

Function	A1'	A2'	A3'	B1'	B2'
Biquad 1	0.0684	–0.1368	0.0684	0.9140	–0.4418
Biquad 2	0.0684	0.1368	0.0684	0.7858	–0.3960

Next, convert the above numbers to fractional 2s complement numbers. In this case, the default coefficient values for TONEA:

Function	A1'	A2'	A3'	B1'	B2'
Biquad 1	08C2	EE7C	08C2	74FE	C774
Biquad 2	08C2	1184	08C2	6495	CD4F

The second part of the requirement is to detect tones that exceed –35 dBm. The approximate values of THRESHU and the corresponding tone level detected for TONEA at 500 Hz are:

THRESHU (Hex)	Tone Level Detected (dBm)
1100	–29
0C00	–32
0880	–35
0600	–38

THRESHU should be 0880h. If no hysteresis is required in the tone detector, then set THRESHL to 0880h (see Table 4-5). If hysteresis is required, then make THRESHL < THRESHU. Threshold levels stated in the data sheets are measured at the band edges. Other filter designs may require different values to those shown above. Note that changing threshold coefficients may change the bandwidth response of tone detectors.

Table 4-6 shows the filter coefficient values for specific filters. Adjust THRESHL and THRESHU as necessary (see Table 4-5).

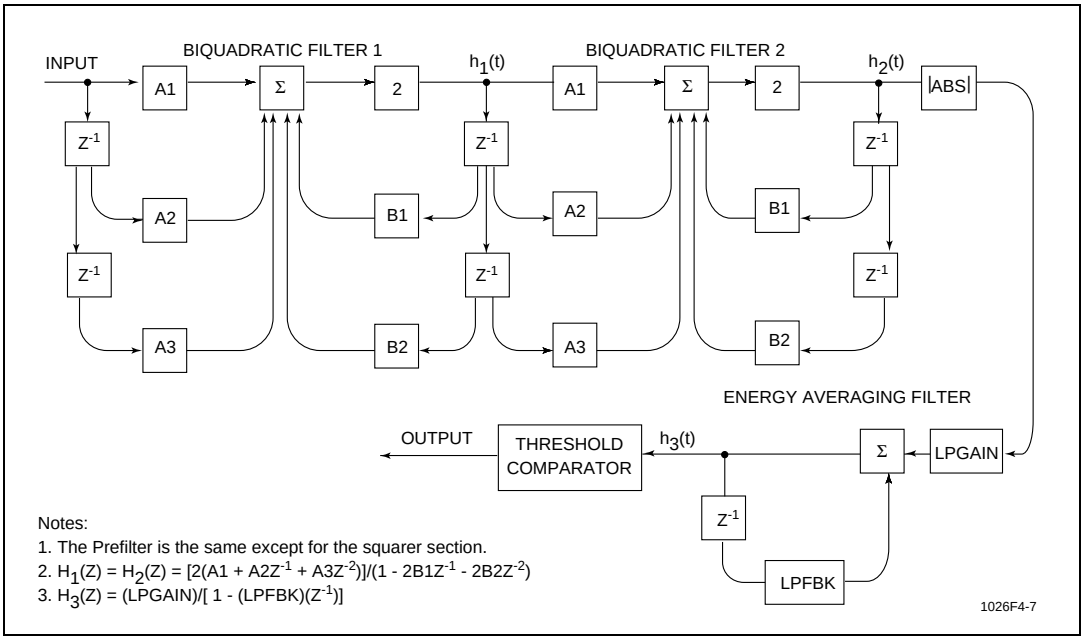


Figure 4-7. Biquad Filter and Level Detector

Table 4-6. Example Tone Detector Filter Coefficients

	Biquad1 Coefficients (Hex)					Biquad2 Coefficients (Hex)				
Sampling Rate/Filter	**A3**	**A2**	**A1**	**B2**	**B1**	**A3**	**A2**	**A1**	**B2**	**B1**
7200 Hz (Non-V.34 Modes)										
1100 Hz	01B3	FC9C	01B4	C147	48C6	01B3	0097	01B4	C147	4897
1800 Hz	0184	FCFB	0185	C147	001C	0184	01BD	0185	C147	FFE4
2250 Hz	0205	FBF9	0206	C147	CF9C	0205	0380	0206	C147	CF68
2100 Hz	01E8	FC32	01E9	C147	DF4F	01E8	034E	01E9	C147	DF19
2225 Hz	0205	FBF9	0206	C147	D22D	0205	0380	0206	C147	D1F8
1270 Hz	02B2	FAA1	02B3	C147	38A4	02B2	00F0	02B3	C147	3871
1650 Hz	0306	F9F9	0307	C147	10A6	0306	010D	0307	C147	106E
980 Hz	0205	FBF9	0206	C147	5337	0205	00B4	0206	C147	530D
1300 Hz	0244	FB7B	0245	C147	35A7	0244	00CA	0245	C147	3574
245-650 Hz[1]	08C2	EE7C	08C2	C774	74FE	08C2	1184	08C2	CD4F	6495
360-440 Hz[2]	0000	FD36	02CA	C63E	7243	02CA	0593	02CA	C63E	7243
9600 Hz (V.8 and V.34 Modes)										
1800 Hz	0372	FEA6	0372	C063	30D6	00C4	FFDA	00C4	C063	30D6
2250 Hz	0119	FE72	0130	C063	0C82	02D9	FEE3	02D9	C063	0C82
2100 Hz	0397	F8D3	0399	C3C9	1905	0397	02C0	0399	C3C9	176D
2225 Hz	0884	EF47	0889	C147	0E90	0884	FE54	0889	C147	0E66
1270 Hz	0123	FDBA	0123	C147	55B6	0123	00DF	0123	C147	5596
1650 Hz	028B	FAEA	028C	C289	3BDA	028B	01F3	028C	C289	3A68
980 Hz	0224	FBB8	0225	C289	64FF	0224	01A4	0225	C289	6403
1300 Hz	0112	FDDB	0113	C147	536D	0112	00D2	0113	C147	533D
245-650 Hz	F8EA	0000	0716	C63E	6FE1	0716	F5FB	0716	C774	7601
360-440 Hz	01AA	FEBC	01AA	C7CD	7438	FF5C	0000	00A4	C148	7A66

Notes:
1. TONEA default.
2. TONEB default.

Function 30: RLSD Drop Out Timer **Acc. Method: 1** **Addr.: 270h, 271h**

V.32 bis, V33, V17, V29, V27, and V.21 channel 2

Address 270, 271 holds the value for a 16-bit counter which decrements at a baud interval when energy is removed from RXA. When the counter reaches 0000, RLSD turns off. The count down may be observed in addresses 389h (value from address 271h) and 388h (value from address 270h). The value in address 271h (MSB), 270h (LSB) may be changed anytime after RLSD = 1. The default time may be read in address 271h, 270h after RLSD = 1. See Table 1-2 for baud rates of individual modes. By prolonging the RLSD on-off time, the MDP can be kept in a freeze mode which can be used to bridge long dropouts. Dropouts of several seconds can be bridged by extending this timer. The default RLSD on-off time for V.32 bis is approximately 500 ms. Note that in V.32 bis mode, it is possible for the receiver to lock onto the local transmit signal when the received signal is lost. (See the DISDET description in Table 3-1.)

V.22 bis, V.22, Bell 212/1200

The 8-bit value in address 270h controls the RLSD on-off time. The value counts down to 0 in address 388h. Once this value starts to decrement, after the signal has been removed from RXA, the host may continuously write a large value in address 388, not allowing the counter to decrement, in order to prolong the RLSD on-off time if the 8-bit counter is not sufficient. This, however, requires the host to monitor address 388 during the connection until it starts to decrement.

The 8-bit value in address 271h controls the time the MDP will wait for energy to return after RLSD has turned off. This value is loaded into address 389h and starts to count up until it reaches a value of 63h. The default value in address 271h is 0 which gives the maximum freeze time of 63h bauds. After RLSD = 0, the host may continuously write 00 in address 389h, not allowing the counter to increment, in order to prolong the freeze time. Both addresses 27h1 and 270h may be written to after RLSD = 1.

Function 31:	**RLSD Turn-On Threshold (RLSD_ON)**	**Acc. Method: 2**	**Addr.: 135h, 134h**
Function 32:	**RLSD Turn-Off Threshold (RLSD_OFF)**	**Acc. Method: 2**	**Addr.: 137h, 136h**
	RLSD Threshold Offset	**Acc. Method: 2**	**Addr.: 139h, 138h**
	RLSD Overwrite Control	**Acc. Method: 1**	**Addr.: 10Dh:2**
	Extended RTH Control	**Acc. Method: 1**	**Addr.: 10Dh:6**

A control bit (10Dh:2) enables or disables the over-writing of the RLSD thresholds by the MDP's own default threshold table [0 = overwriting enabled (default); 1 = overwriting disabled]. The default state is initialized only by power on or a soft reset.

The RLSD thresholds are loaded into memory locations RLSD_ON and RLSD_OFF. During the Idle mode initialization, the 2-byte value stored in RLSD_ON is used as the RLSD on threshold. When the MDP is in Data mode, the 2-byte RLSD_OFF value is used for the RLSD off threshold.

During reset, the respective thresholds for V.32 bis 14400 bps are loaded into RLSD_ON and RLSD_OFF as initial values. After reset, the host may then alter these values using the following procedure:

1. Set 10Dh:2 (to prevent custom values from being overwritten by default values).
2. Load in the custom RLSD values.
3. Set NEWC.

Note: the thresholds can be over-written at any time, but this method ensures that the first connection after a NEWC uses the correct value of ON threshold.

Extended RLSD Threshold Selection:

The Extended RTH bit (XRTH) (10Dh:6) controls the reduction of RLSD thresholds by approximately 5 dBm [0 = disables reduction (default); 1 = enables reduction]. If XRTH is a 1, RTH must be reset to 0. This extended RLSD threshold method affects all configurations while preserving the hysteresis.

The amount of threshold reduction (offset) can be controlled manually by the host writing a 16-bit offset value into address 139, 138. For example, this offset is useful for compensating for any loss or gain that may be introduced by the DAA/hybrid used. Note that if a negative offset is wanted, then the twos complement number should be entered. The maximum amount of offset that can safely be subtracted is 900h (F700h, 2s complement).

Function 34: V.32 PN Length **Acc. Method: 2** **Addr.: 289h, 288h**

The V.32 bis/V.32 handshake and retrain sequence may be shortened or lengthened to meet special applications by adjusting the length of the PN (TRN) sequence. The answering modem sends two TRN sequences during the handshake while the originating modem sends only one.

The TRN time T (in ms) is calculated as follows:

Equation: N = (2.4 x T) - 256

Where: N is the decimal equivalent of the hex number written to RAM and T is the time in ms.

Note: Values of N should be kept within 400h to 1F00h. A power-on reset will clear this location.

Changing the TRN lengths should be reserved for special applications only and is not recommended. Short TRN sequences may jeopardize the success of the handshake or retrain. Consult the ITU-T V.32/V.32 bis specifications for TRN length limitations. Only the originate TRN and the first answer TRN lengths are affected.

Function 36: AGC Gain Word **Acc. Method: 4** **Addr.: A00h**

Function 36 is useful for determining the receive level (RL) at the Receive Analog (RXA) input. The number in RAM is related to the receive level as follows:

Configuration	Equation (AVAA = +5 V)	Equation (AVAA = +3.3 V)
K56flex, V.34, V.33, V.17, V.29, V.27	RL = N/682.7 - 52 dB	RL = N/682.7 - 56 dB
V.32 bis, V.32	RL = N/682.7 - 53 dB	RL = N/682.7 - 57 dB
V.22 bis, V.22, Bell 212, V.23/1200	RL = N/682.7 - 48 dB	RL = N/682.7 - 52 dB
V.21, V.23/75	RL = N/682.7 - 54 dB	RL = N/682.7 - 58 dB
Bell 103	RL = N/682.7 - 51 dB	RL = N/682.7 - 55 dB
Where: N is the decimal value of the hex number read from RAM.		

This formula is valid only if the receive level is above the RLSD off-to-on threshold.

Function 37: Round Trip Far Echo Delay **Acc. Method: 4** **Addr.: 239h**

Function 37 provides the value of the round trip delay measured during the handshake.

Equation: RTD = (N/X) - 3.5 (for V.34)

RTD = (N/2.4) - 29 (for V.32 bis)

Where: RTD = Round Trip Delay in ms

N = Decimal equivalent of value read from RAM

X = symbol rate/1000, i.e., 2.4, 2.8, 3.0, 3.2, or 3.429 (see Function 60).

Function 45: Equalizer Frequency Correction **Acc. Method: 4** **Addr.: 811h**

Function 45 provides the value of the Equalizer Frequency Correction (V.32 bis only).

Equation: F = N/27.3 (for V.32 bis)

Where: F = Carrier frequency offset in Hz

N is the decimal value of the hexadecimal number read from RAM

Function 46: Eye Quality Monitor **Acc. Method: 4** **Addr.: 20Ch**

In V.32 4800 bps, V.29, V.27, V.22 bis, V.22 and Bell 212A modes, EQM is the filtered squared magnitude of the error vector. However, for all TCM modes (V.34, and V.33 modes, and V.32 12000, 9600, and 7200 bps modes), EQM is the filtered minimum trellis path length (or metric). This gives a better indication of signal quality for trellis modes.

The error vector formed by the decision logic can be used to indicate relative signal quality. As signal quality deteriorates, the average error vector increases in magnitude. By calculating the magnitude of the error vector and filter the results, a number inversely proportional to signal quality is derived. This number is called the eye quality monitor (EQM). Because of the filter time constant, EQM should be allowed to stabilize for approximately 700 baud times following RLSD going active.

The EQM value for the non-trellis configurations is the filtered squared magnitude of the error vector and represents the average signal power contained in the error component. The power is directly proportional to the probability of errors occurring in the received data and can be used to implement a discrete Data Signal Quality Detector circuit (circuit 110 of ITU-T Recommendation V.24 or circuit CG of the RS-232-C standard) by comparing the EQM value against experimentally determined criteria (Bit Error Rate curves). Figure 4-8 illustrates the relationship of the EQM number to an eye pattern created by a 4-point signal structure (e.g., V.29/4800 bps) in the presence of high level white noise. The EQM value is proportional to the square of the radius of the disk around any ideal point. The radius increases when signal to noise ratio (SNR) decreases. As the radius approaches the ideal point's boundary values, the bit error rate (BER) increases. Curves of BER as a function of the SNR are used to establish a criteria for determining the acceptability of EQM values. Therefore, from an EQM value, the host processor can determine an approximate BER value. If the BER is found to be unacceptable, the host may cause the MDP to fallback to a lower speed to improve BER.

It should be noted that the meaning of EQM varies with the type of line disturbance present on the line and with the various configurations. A given magnitude of EQM in V.29/9600 does not represent the same BER as in V.27/4800. The former configuration has 16 points that are more closely spaced than the four signal points in the latter, resulting in a greater probability of error for a given level of noise or jitter. Also, the type of line disturbance has a significant bearing on the EQM value. For example, white noise produces an evenly distributed smearing of the eye pattern with about equal magnitude and phase error while phase jitter produces phase error with little error in magnitude.

Since EQM is dependent upon the signal structure of the modulation being used and the type of line disturbance, EQM must therefore be determined empirically in each application.

The relationship of EQM to eye pattern is illustrated in Figure 4-8.

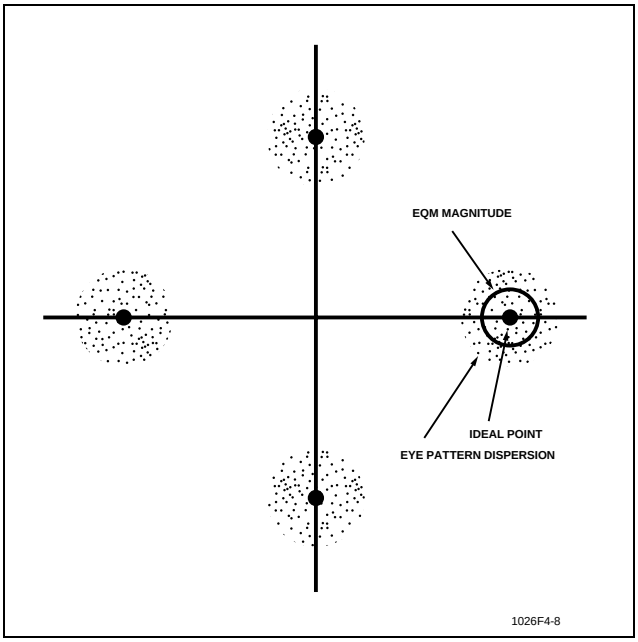


Figure 4-8. Relationship of EQM to Eye Pattern

Function 47: Maximum Period of Valid Ring Signal **Acc. Method: 1** **Addr.: 21Fh**
Function 48: Minimum Period of Valid Ring Signal **Acc. Method: 1** **Addr.: 21Eh**

The ring detector measures the period of pulses on the ring detect input and determines whether the pulses are within the frequency range specified by the Maximum Period of Valid Ring Signal and Minimum Period of Valid Ring Signal functions. Since maximum period corresponds to minimum frequency, the formula for calculating these functions is given in terms of frequency.

Frequency F (in Hz) is calculated as follows:

Equation: N = 2400/F

Where: N is the decimal value of the hex number written to RAM (05h-FFh).

Default: The default values are:

Function	Parameter	Method	Address	Default (Hex)	Default (Dec)
47	Maximum Period of Valid Ring Signal	1	21Fh	A0	15 Hz
48	Minimum Period of Valid Ring Signal	1	21Eh	23	68 Hz

Note: Writing 00 to Function 48 will cause the RI bit state and ~RI output pin level to follow the RINGD input pin level.

Function 49: Phase Jitter Frequency **Acc. Method: 4** **Addr.: 80Eh**

The phase jitter frequency estimate is available in V.34/V.32 bis/V.32 mode only. The phase jitter amplitude must be greater than approximately 6 degrees with a minimum frequency of 10 Hz in order for the MDP to lock on and track the jitter.

Equation: $F = N*\text{Symbol Rate}/2^{16}$ (V.34)

$F = N/27.3$ (V.32 bis/V.32)

Where: F is the frequency in Hz.

N is the decimal equivalent of the hex number read from RAM.

Symbol Rate = 2400, 2800, 3000, 3200, or 3429.

Function 50: Phase Jitter Amplitude **Acc. Method: 4** **Addr.: 80Dh**

The phase jitter amplitude estimate is available in V.34/V.32 bis/V.32 mode only. The phase jitter amplitude must be greater than approximately 6 degrees with a minimum frequency of 10 Hz in order for the MDP to lock on and track the jitter.

Equation: AP = N/90

Where: AP is the amplitude in degrees.

N is the decimal equivalent (absolute value) of the hex number read from RAM

Function 51: Guard Tone Level **Acc. Method: 3** **Addr.: B46h**

Guard tone power in dBm (PO) is calculated as follows (based on TLVL bits = 9 and 600 Ω termination):

Configuration	Equation	Default Value (Hex)
1800 Hz guard tone (GTS bit = 0; CEQ bit = 1)	$N = 4926\ [10^{Po/20}]$	036C
1800 Hz guard tone (GTS bit = 0; CEQ bit = 0)	$N = 8458\ [10^{Po/20}]$	05E0
550 Hz guard tone (GTS bit = 1; CEQ bit = 1)	$N = 5128\ [10^{Po/20}]$	0390
550 Hz guard tone (GTS bit = 1; CEQ bit = 0)	$N = 8458\ [10^{Po/20}]$	05D8

Notes:

1. Setting the NEWC bit will reset the power level to its default level.
2. The power level may be adjusted only after the GTE bit is set.
3. The transmit level bits (TLVL) affect the guard tone power output level.
4. Guard tone power is available in V.22 bis/2400 or V.22/1200 answer mode only.

Function 52: ITU-T CRC 32 Select **Acc. Method: 1** **Addr.: 0B3h(0)**

The type of cyclic redundancy check (CRC) generation and detection can be selected by writing to bit 0B3h:0 [0 = ITU-T CRC 32; 1 = ITU-T CRC 16 (default)].

Function 53: Secondary Channel Transmitter Speed Select (V.32 bis/V.32)
Acc. Method: 1 **Addr.: 28Eh**
Secondary Channel Receiver Speed Select (V.32 bis/V.32)
Acc. Method: 1 **Addr.: 28Bh**

The default data rate for the secondary channel is 150 bps. The rate can be changed by modifying a divide factor in two addresses: 28Eh for the transmitter and 28Bh for the receiver. The following table lists the possible secondary channel speeds for the various main channel speeds and the corresponding RAM value. Reset will clear locations 28Eh and 28Bh.

	Secondary Channel Speed (bps)					
	Transmitter and Receiver RAM Divide Constant Values (Hex)					
Main Channel Speed (bps)	75	150	300	600	1200	2400
14400	8	10				
12000	8	10				
9600 TCM	4	8	10			
9600 QAM	2	4	8	10		
7200	2	4	8	10		

Functions 54 - 59: Not Applicable.

Function 60: V.34 Symbol Rate Value **Acc. Method: 1 (RO)** **Addr.: 2E3h**
Function 61: V.34 Baud Rate Mask (BRM) **Acc. Method: 1** **Addr.: 101h**

During the start-up handshake, the MDP probes the communication channel and determines the available bandwidth. This information helps establish the common symbol rate between the modems. The following data rate ranges are available for a selected symbol rate:

Symbol Rate (baud)	Highest Possible V.34 Data Rate (bps)
2400	21600
2800	26400
3000	28800
3200	31200
3429	33600

If line conditions cannot support the higher symbol rates, the MDP automatically reduces the data rate to match the allowable symbol rate.

The host can control the symbol rate negotiation process via the Baud Mask Register (BMR), located at address 101h. By either setting or resetting one or more of five bits in the BMR, the host can specify if a particular symbol rate is to be supported. In Loop 3 (L3ACT = 1), the baud rate may be selected by writing the desired symbol rate value (0, 2, 3, 4, or 5) to address 2E3h anytime prior to establishing the loopback. The default value is 4 for 3200 baud. The symbol rates and the corresponding bit positions are:

Symbol Rate (baud)	Symbol Rate Value (Addr. 2E3h)	Baud Mask Register (BRM) Enable Bit Position (Addr. 101h)
2400	0	0
Reserved	1	1*
2800	2	2
3000	3	3
3200	4	4**
3429	5	5

* Bit 1 must always be a 1.

** Bit 4 (3200 symbol rate) must be set for K56flex operation.

When the MDP determines, from the bandwidth, the maximum supportable symbol rate, the MDP will enable all symbol rates below that maximum value. For example, if the line probe indicates that the bandwidth is adequate to support 3000 baud, then 2800 and 2400 baud will also be supported. This selection of symbol rates is, however, dependent upon the contents of the BMR. Again, for the same example, if a host does not want to support 2800 baud, the host must reset bit 2 of the BMR. If both modems do not agree during probing, e.g., the originate modem chooses 3000 baud and the answer modem chooses 2800 baud, then the highest common rate will be 2400 baud. In the event there is no common rate, the modems will default to 2400 baud.

Figure 4-9 shows the symbol rate negotiation process. The final symbol rate chosen may be read from address 2E3h after the negotiation is complete. A value of 10h, for example, would indicate a symbol rate of 3200 baud.

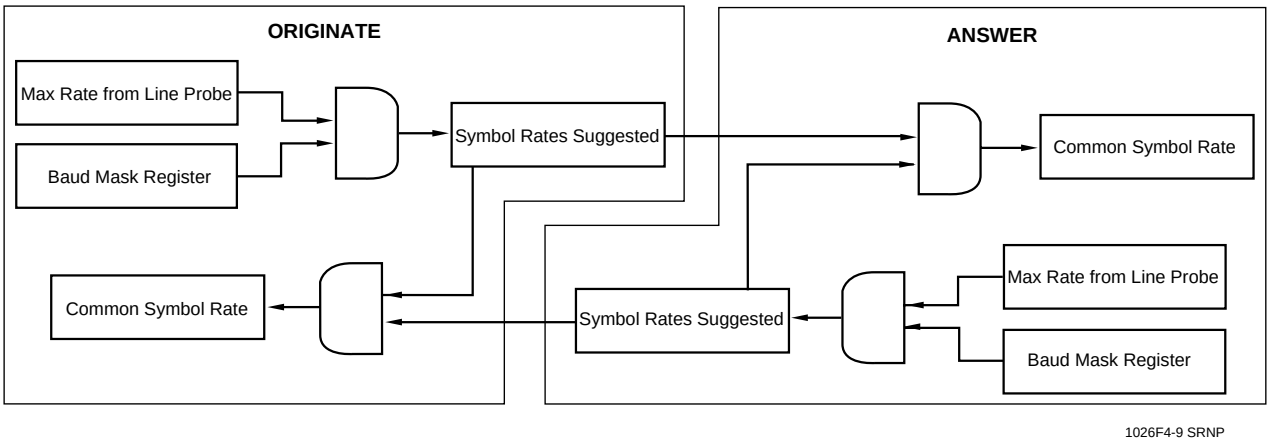


Figure 4-9. V.34 Symbol Rate Negotiation Process

Function 62:	**V.34 Pre-Emphasis Filter Number**	**Acc. Method: 4**	**Addr.: B44h**
Function 63:	**V.34 Pre-Emphasis Filter Override Number**	**Acc. Method: 1**	**Addr.: 0E6h**
	V.34 Emphasis Disable	**Acc. Method: 1**	**Addr.: 100h:1**

There are 11 pre-emphasis filters defined, each matching the templates defined in ITU-T V.34.

The Pre-emphasis filter selected can be read from the V.34 Pre-Emphasis Filter Number (address B44h).

The Pre-emphasis negotiation can be ignored by setting bit 100h:1, Pre-emphasis Disable (PREDIS). This bit does not stop the measurement or the transmission of the suggested pre-emphasis filter, but rather causes the receiver to ignore the suggestion.

Pre-emphasis can also be controlled by using the CEQ bit in the MDP interface memory. If this bit is reset, any selected pre-emphasis or transmit compromise filter will be ignored. In this way, the host can control pre-emphasis by setting/resetting CEQ. However, if the host wishes to use a custom compromise filter, then by using the PREDIS bit, the suggested filter will be ignored and the host's custom defined compromise filter will be used.

The procedure to manually select one of the pre-emphasis filters is:

1. Set the PREDIS bit (100h:1) to override negotiation.
2. Load the Pre-Emphasis Filter Over-Ride Number (address 0E6h) with the Pre-emphasis Filter Suggestion Number from the table above.
3. Ensure that CEQ is on.

Function 64:	**V.34 Transmit Level Deviation Disable**	**Acc. Method: 1**	**Addr.: 100h:3**

During line probing, the MDP measures the receive level of the line signal. If that receive level is high enough, the MDP suggests that the remote modem reduce its own transmit level in order to improve signal-dependent noise performance.

The transmit level power drop does not use receive level alone. Decision is also based on noise and harmonic distortion criteria.

To force the MDP to ignore the suggested transmit level reduction, set the Transmit Level Deviation Disable (TLDDIS) bit (100h:3) to a 1.

Function 65-67: Not Applicable

Function 68: EQM Above Threshold **Acc. Method: 1** **Addr.: 133h**

When the high byte of the EQM reading (address 20Dh) goes above the EQM Above Threshold, the MDP will assert the EQMAT bit (0Bh:1). The host can set up a NEWS interrupt to monitor changes to this bit (see EQMAT in Function 17). The default value of EQM Above Threshold is 30h and is written at POR and is unaffected by NEWC. The MDP does NOT reset the EQMAT bit; the host must reset the EQMAT bit.

Function 69: ARA-in RAM Enable **Acc. Method: 1** **Addr.: 3A5h:4**
EQM Scale Factor (Gain) **Acc. Method: 3** **Addr.: A29h**

The automatic rate adaptation (ARA) algorithm adjusts the data rate based on the level of EQM. The ARA is recommended with the initial train and retrain only. Rate-renegotiation should be performed with ARA off, allowing the host to decide the optimal data rate based on EQM readings. ARA is enabled by setting the EARC bit (15h:0), which defaults off.

Upon initial train and retrain, the EQM is checked during the training, just before the rate negotiation. The 4-point EQM is compared against a table of values representing the necessary levels to achieve the corresponding V.34/V.32 bis data rates with an EQM of around 2000h. Once the maximum achievable rate is determined, the CONF register is changed to reflect the estimate, and is then used to suggest a data rate in the following negotiations.

Modifying the ARA Thresholds in RAM (V.34 Mode only)

The 'ARA-in-RAM' function is enabled by setting bit 3A5h:4 (8-bit access).

Sixteen RAM locations are allocated for the ARA-in-RAM thresholds. These occupy locations 3B0h to 3BFh.

The Search table used for determining the best data rate for a given EQM is uniquely organized. The search through the table starts at the low address first, which represents the lowest data rate*, and progresses through to the higher data rates as the measured EQM value during training decreases. The final measured EQM is compared to the ARA RAM table. The EQM value must be greater than the threshold value in RAM for the corresponding data rate to be selected. For example, in the table below, if the final measured EQM were between 0028 and 0090, the data rate of 26.4k would be selected. If the EQM value were less than 0028, the data rate of 28.8k would be selected. As another example, to allow more aggressive 28.8k connections, the threshold under the 26.4k rate (0028) should be increased. This would require the measured EQM to be slightly worse before falling back to 26.4k.

At the low data rates only the most significant byte of EQM is used in the threshold testing. However, as the thresholds get smaller for the higher data rates, it is necessary to use the least significant byte of EQM for the required resolution. When this transition occurs, the table of thresholds must contain a 0, followed by the appropriate low byte threshold value. The last location to be searched must contain a 0 to stop further searches.

* Normally for symbol rates above 2400 baud, the starting point is at address 3B1h and the initial data rate is 4800 bps. For the case of 2400 baud, the starting point is at 3B0h and the initial data rate is 2400 bps.

The following table of default thresholds against data rates is used in the ARA-in-RAM function.

Data Rate (kbps)	2.4	4.8	7.2	9.6	12.0	14.4	16.8	19.2	21.6	24.0	26.4	28.8	31.2	33.6
Threshold (Hex)	2000	1A00	1200	0C00	0A00	0900	0500	0300	0200	0090	0028	0010	0004	0001

Consequently, the default values written into RAM are:

Address (Hex)	Value (Hex)	Comment
3B0	20	
3B1	1A	
3B2	12	
3B3	0C	
3B4	0A	
3B5	09	
3B6	05	
3B7	03	
3B8	02	
3B9	00	**Note:** This 0 causes the search algorithm to use low byte of EQM
3BA	90	The next threshold (it is equal to 00E0h)
3BB	28	
3BC	10	
3BD	04	
3BE	01	
3BF	00	

Configuring the ARAinRAM Thresholds During the V.34 Handshake

The thresholds are designed for optimum connectivity at symbol rates of 3429 and 3200. Whereas this will cover the vast majority of connections, the user may wish to alter the ARA-in-RAM values when symbol rates of 3000 and below are required. In this situation, the host can read the symbol rate and then load a new set of ARA-in-RAM values into the address range specified. This is to be done at the start of Phase 3 of the handshake.

Method:

1. Monitor the Receive Handshake Status (16h, SECRXB). Wait until it is set to 4X.
2. Read the selected connection symbol rate (address 2E3h, Function No. 60).
3. Write in appropriate ARAinRAM thresholds for that symbol rate in addresses 3B0h through to 3BFh, using the information provided above. (8-bit access).

Forced 2400 Symbol Rate when Probing SNR is Adverse

If the signal-to-noise ratio (SNR) is less than the specified threshold, the data pump overrides the bandwidth evaluation algorithm and forces the Symbol Rate to 2400 baud. This allows the MDP to fallback to 2400 bps if the SNR is poor as defined by this threshold. The threshold is located in RAM at address 3C0 and the bit which enables this feature is bit 3A5:5. The default for this bit is enabled and the default threshold value is 0Dh which approximates to a SNR of 12 dB. All RAM accesses are 8-bit.

Modifying the EQM Gain

A simpler, but less attractive, method to affect these rate adjustments is to increase the EQM gain at address A29h for a more reliable connection or to lower the EQM gain for a less reliable connection. The default value is 1000h. This method affects the EQM reading at address 20Ch.

In V.34, the EQM gain may be changed after the SDET bit is set.

In V.32 bis, the EQM gain may be changed after the DTR bit is set.

Example 1: If a more reliable (lower speed) connection is desired, increase the EQM gain from the normal value of 1000h to 2000h. The rate selected would then be one lower, e.g., 21600 will be selected whereas 24000 would have been selected without the change.

Example 2: If a less reliable (higher speed) connection is desired, decrease the EQM gain from 1000h to 0800h.

See Section 14.1.7for manual ARA adjustments in K56flex and V.34 modes.

Function 70: V.21/V.23 CTS Mark Qualify **Acc Method: 1** **Address: 10Dh:3**

In V.21/V.23 configurations, CTS turn-on qualifying time can be controlled by writing to bit 10Dh:3 [0 = no qualifying time after Mark (default); 1 = qualifying time of 45 ±5 ms after Mark]. This bit is unaffected by the action of NEWC.

Function 71-72: Not Applicable

Function 73: No Automode to FSK **Acc Method: 1** **Address: 13Fh:0**

Automode to FSK modes can be controlled by writing to bit 13Fh:0 [0 = automode to FSK enabled (default); 1 = automode to FSK disabled). This bit remains unaffected by NEWC.

If enabled (0), the automode selection will allow FSK connections. If disabled (1), automode selection will not configure to any FSK mode.

Function 74:	**Receive FIFO Trigger Level**	**Acc Method: 1**	**Address: 32Ch**
	Transmit FIFO Extension Enable	**Acc Method: 1**	**Address: 702h:0**
	Receive FIFO Extension Enable	**Acc Method: 1**	**Address: 701h:0**

Transmitter FIFO (TXFIFO)

The 16-byte TXFIFO is controlled by writing to the FIFOEN bit (04h:4) [0 = TXFIFO disabled; 1 = TXFIFO enabled].

The 128-byte TXFIFO Extension (TXFIFOX) is controlled by writing to the Transmit FIFO Extension Enable bit (702h:0) [0 = TXFIFOX disabled; 1 = TXFIFOX enabled (default)].

When the TXFIFO is enabled (FIFOEN = 1), the host can continuously write to TBUFFER as long as TXFNF status bit (0Dh:1) is set. The TDBE bit (1Eh:3) will be set whenever the TXFIFO is empty (TXFIFOX disabled) or when the TXFIFO can accept more bytes (TXFIFOX enabled). Two control bits, TEOF (11h:1) and TXP (11h:0) are buffered along with the TXFIFO data. The TEOF bit is used in HDLC mode to indicate that the next byte written into TBUFFER is the last byte of the frame. TXP is used in 8-bit, stuff parity asynchronous mode to indicate the parity bit. Also, the TXHF status bit (01h:2) indicates when the TXFIFO is half full.

When the TXFIFO is disabled (FIFOEN = 0), the TXFIFO is one byte in length.

When disabling the FIFO extensions (702h:0 = 0 or 701h:0 = 0), the host must wait until connected in data mode (RLSD = 1) before doing so. If a retrain or rate renegotiation occurs, bits 702h:0 and 701h:0 must again be cleared after completion of the retrain or rate renegotiation (CTS = 1) if disabling the FIFO extensions is desired.

Receiver FIFO (RXFIFO)

The 16-byte RXFIFO is always enabled.

The 128-byte RXFIFO Extension (RXFIFOX) is controlled by writing to the Receive FIFO Extension Enable bit (701h:0) [0 = RXFIFOX disabled; 1 = RXFIFOX enabled (default)].

The lower 16-byte portion of the RXFIFO can be controlled by writing to address 32C. The default value is CBh which gives a trigger level of 14 bytes and a time-out of 17 clock cycles.

Bits 7-6 **Trigger Level.** Selects the trigger level in the 16-byte RXFIFO. For example, setting bits 7 and 6 to 1 selects a trigger level of 14 bytes. That is, RDBF will not become asserted until the receive FIFO is 14 bytes full and the time-out delay has not elapsed (see below). Both RDBF and RXFNE will remain set until the RXFIFO is empty.

Bit 7	Bit 6	Trigger Level (No. of Bytes)
0	0	Trigger level = 1
0	1	Trigger level = 4
1	0	Trigger level = 8
1	1	Trigger level = 14

Bit 5 Must be 0.

Bits 4-2 **Time-out Delay.** Selects the length of idle time that will cause RDBF to be asserted when the RXFIFO is not empty. Idle time is the length of time that elapses without the MDP writing into the RXFIFO or the host reading data from the RXFIFO. This feature prevents data from being "held up" in the RXFIFO.

B4	B3	B2	Idle Time (In Bit Times)
0	0	0	9 bit times
0	0	1	13 bit times
0	1	0	17 bit times
0	1	1	21 bit times
1	0	0	25 bit times
1	0	1	29 bit times
1	1	0	33 bit times
1	1	1	37 bit times

Bit 1 **Idle Time Time-out Enable.** 1 = the time-out enabled; 0 = time out disabled. When Time out is disabled (0), RDBF will be asserted only when the RXFIFO threshold is reached.

Bit 0 **Not Used.**

RXFIFO Error Status Bits

The RXFIFO includes five error status bits: BRKD (0Eh:6), SYNCD (0Ah:1), RXP (01h:0), FE (0Ah:4), and PE (0Ah:5). SYNCD is used for 7E flag detection in HDLC mode only and BRKD indicates that an asynchronous break has been received. FE indicates a framing error in asynchronous mode or an abort condition in HDLC mode. PE indicates an asynchronous parity error or a CRC error in HDLC mode. RXP indicates the received parity bit in 8-bit asynchronous stuff parity mode.

IMPORTANT: The host must read the status bits prior to reading the byte from RBUFFER. Note that this is the opposite of how it should be done using the RC96DPL/RC144DPL or RC96DPi/RC144DPi.)

Also, there are two status bits (RXHF and RXFNE) that the host can use to monitor the RXFIFO operation. RXHF (01h:1) indicates when the receive FIFO is half full and RXFNE (0Ch:1) is set whenever RXFIFO contains data.

Function 75-80: Not Applicable

Function 81: V.34 Spectral Parameters Control Acc Method: 1 Address: 105h

The host can control some of the spectral parameters that the transmitter uses for cases where the local PTT has regulations governing transmission. These control bits should be used in their default state and the host need only alter them if required to meet PTT approval.

Bit 7 **Transmitter Enable for the Low Carrier Frequency for 3200 Baud.** When set, the transmitter can use the low carrier frequency for 3200 baud.

Bit 6 **Transmitter Enable for the High Carrier Frequency for 3200 Baud.** When set, the transmitter can use the high carrier frequency for 3200 baud.

Bit 5 **Transmitter Enable for the Low Carrier Frequency for 3000 Baud.** When set, the can use the low carrier frequency for 3000 baud.

Bit 4 **Transmitter Enable for the High Carrier Frequency for 3000 Baud.** When set, the can use the high carrier frequency for 3000 baud.

Bits 3:0 **Reserved.** Do not alter the contents.

Function 82: V.34 Phase 2 Power Reduction Acc Method: 1 (RO) Address: 0E2h

In V.34 mode, the MDP supports the reduction in transmit power if instructed by the remote modem during the start-up sequence. The amount of power drop from the nominal is 0 to 14 dB. The TLDDIS bit (100h:3, see Function 64) enables the local modem to implement the amount of power drop being suggested by the remote modem or to ignore it and not drop the level at all. Function 82 specifies the amount of power drop in dB after Phase 2.

Function 83-84: Not Applicable

Function 85: V.34 Data Rate Mask **Acc Method: 2** **Address: 383h, 382h**
K56flex/V.34 Transmitter Maximum Data Rate Mask **Acc Method: 1** **Address: 605h**
K56flex/V.34 Receiver Maximum Data Rate Mask **Acc Method: 1** **Address: 604h**

The V.34 data rate masks occupy two bytes in RAM. Locations 382h and 383h represent the lower byte and the upper byte of the mask, respectively (Table 4-7). The bits in the mask represent the enabling of a particular data rate if set or disabled if reset. The definition of the bits are data rate 2400 is at bit 0 (i.e., the LSB of address 382h), 4800 is at bit 1, 7200 at bit 2 and so on up to 33600 bps (in 2400 bps increments) which is bit 13 of the mask (or bit 5 of address 383h. Bits 14-15 are reserved.

Table 4-7. V.34 Rate Sequence Mask Bit Assignments

Data Rate	V.34 Data Rate Mask-MSB (Address 383h)								V.34 Data Rate Mask-LSB (Address 382h)							
(bps)	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
2400	-	-	X	X	X	X	X	X	X	X	X	X	X	X	X	1
4800	-	-	X	X	X	X	X	X	X	X	X	X	X	X	1	X
7200	-	-	X	X	X	X	X	X	X	X	X	X	X	1	X	X
9600	-	-	X	X	X	X	X	X	X	X	X	X	1	X	X	X
12000	-	-	X	X	X	X	X	X	X	X	X	1	X	X	X	X
14400	-	-	X	X	X	X	X	X	X	X	1	X	X	X	X	X
16800	-	-	X	X	X	X	X	X	X	1	X	X	X	X	X	X
19200	-	-	X	X	X	X	X	X	1	X	X	X	X	X	X	X
21600	-	-	X	X	X	X	X	1	X	X	X	X	X	X	X	X
24000	-	-	X	X	X	X	1	X	X	X	X	X	X	X	X	X
26400	-	-	X	X	X	1	X	X	X	X	X	X	X	X	X	X
28800	-	-	X	X	1	X	X	X	X	X	X	X	X	X	X	X
31200	-	-	X	1	X	X	X	X	X	X	X	X	X	X	X	X
33600	-	-	1	X	X	X	X	X	X	X	X	X	X	X	X	X

The rate mask at 383h/382h controls the data rate for both the transmitter and receiver. In other words, if the rate mask is limited to 24k bps, both the transmitter and receiver rates will be limited to 24k bps. If connected in asymmetric mode (see Function 86) the transmitter rate may be further limited by the request of the remote modem's receiver. In symmetric mode, the transmitter and receiver rates cannot differ and will end up at the highest common rate between the two modems, at or below the maximum common data rate specified in both modem's rate mask.

The transmitter and receiver rates can alternatively be limited independently through addresses 605h and 604h, respectively. Note that only the maximum rate can be limited and not specific rates as with the mask at 383h/382h. See Section 14.

The rate masks will limit the data rates during the initial handshake, retrains and rate renegotiations. The rate masks will also limit (but not increase) any speed decision made by the ARA or the manual data rate selection as described in Section 14.

Function 86: K56flex/V.34 Asymmetric Data Rates Enable **Acc Method: 1** **Address: 13Fh:6**

V.34 modes normally operate with asymmetric data rates for the transmitter and receiver. Resetting (default state) bit 13Fh:6 (Function 85) forces the transmitter and receiver data rates to be the same. Setting bit 13Fh:6 allows the transmitter data rate to be different than the receiver data rate. **Note:** This bit must be set in K56flex.

Function 87: V.34 Remote Modem Data Rate Capability **Acc Method: 2** **Address: 209h, 208h**
V.34 Remote Modem Asymmetric Data Rate **Acc Method: 1** **Address: 209h:7**

The data rate capability of the remote modem is reflected in a binary sequence transmitted by the remote modem during Phase 4 of the handshake. This 12-bit received sequence is stored in locations 208h and 209h (Table 4-8). The definition of this field is the same as that described for the V.34 Data Rate Mask (Function 84). Also stored in bit 7 of 209h is the capability of the remote modem to support asymmetric data rates (if set, then capability is enabled). This information is valid after RLSD is ON. The received V.34 rate sequence indicates the remote modem's true speed capabilities as it is masked only by the remote mask sequence register and not by the remote ARA function (EARC bit = 1). For example, the MDP may connect at 24000 bps by request of the remote modem's ARA, yet the received rate sequence may indicate that the remote modem can support 28800 bps. This information may be used for fall forward decisions. Bits 14-15 are reserved.

Table 4-8. V.34 Remote Mode Data Rate Capability Bit Assignments

Data Rate	V.34 Remote Mode Data Rate Capability -MSB (Address 209h)								V.34 Remote Mode Data Rate Capability-LSB (Address 208h)							
(bps)	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
2400	-	-	X	X	X	X	X	X	X	X	X	X	X	X	X	1
4800	-	-	X	X	X	X	X	X	X	X	X	X	X	X	1	X
7200	-	-	X	X	X	X	X	X	X	X	X	X	X	1	X	X
9600	-	-	X	X	X	X	X	X	X	X	X	X	1	X	X	X
12000	-	-	X	X	X	X	X	X	X	X	X	1	X	X	X	X
14400	-	-	X	X	X	X	X	X	X	X	1	X	X	X	X	X
16800	-	-	X	X	X	X	X	X	X	1	X	X	X	X	X	X
19200	-	-	X	X	X	X	X	X	1	X	X	X	X	X	X	X
21600	-	-	X	X	X	X	X	1	X	X	X	X	X	X	X	X
24000	-	-	X	X	X	X	1	X	X	X	X	X	X	X	X	X
26400	-	-	X	X	X	1	X	X	X	X	X	X	X	X	X	X
28800	-	-	X	X	1	X	X	X	X	X	X	X	X	X	X	X
31200	-	-	X	1	X	X	X	X	X	X	X	X	X	X	X	X
33600	-	-	1	X	X	X	X	X	X	X	X	X	X	X	X	X

Function 88: V.8 Status Registers - See Section 9.

Function 89: V.8 Control Registers - See Section 9.

Function 90: Modulation Modes- See Section 9.

Function 91: V.8 MaxFrameByteCount- See Section 9.

Function 92: V.8 Call Functions- See Section 9.

Function 93: CM Frame - - See Section 9.

Function 100: Minimum On Time (DTMF) **Acc Method: 3** **Address: E96h**

The minimum on time is defined as the minimum period of time of the DTMF signal beginning when the signal is detected and ending when the energy is below the turn-off threshold. The on-time parameter cannot be set below 20 ms (0000h). The default on-time parameter is set for 40.0 ±1 ms. The on-time will vary with signal level. To increase or decrease the on-time parameter value, convert the increase/decrease into hexadecimal and add/subtract to/from the current value.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Equation: Minimum On Time ± [(Increase/Decrease)Sample Rate]h

Function 101 Minimum Off Time (DTMF) **Acc Method: 3** **Address: C96h**

The minimum off time is defined as the minimum period of time of the DTMF signal beginning when the energy falls below the turn-off threshold and ending when a gain hit is detected. The off-time parameter is equal to the desired minimum off-time minus the drop out time. The default off time is set for 40.0 ± 1 ms with a default dropout time parameter of 5.0 ms. To increase or decrease the off-time parameter value, convert the increase/decrease into hex and add/subtract to/from the current value.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Equation: Minimum Off Time ± [(Increase/Decrease)Sample Rate]h (dropout time equal to 5.0 ms).

Function 102: Minimum Cycle Time (DTMF) **Acc Method: 3** **Address: D96h**

The minimum cycle time is defined as the minimum period of the DTMF signal beginning when the signal is detected and ending when the next signal begins. The cycle time parameter is equal to the desired minimum cycle-time minus the dropout time. The default cycle time parameter is set for 93.0 ±1 ms with a default drop out time parameter of 5.0 ms. To increase or decrease the cycle time parameter value, convert the increase/decrease into hex and add/subtract to/from the current value.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Equation: Minimum Cycle Time ± [(Increase/Decrease)Sample Rate]h (dropout time equal to 5.0 ms).

Function 103: Minimum Dropout Time (DTMF) **Acc Method: 3** **Address: F96h**

The minimum dropout time is defined as the maximum period of the DTMF signal beginning when the signal energy drops below the turn-off threshold and ending when the signal energy returns that is considered to be part of the on time. The default dropout time parameter is set to 5.0 ms.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Equation: [(Desired time)Sample Rate]h

Function 104: Maximum Speech Energy (DTMF) **Acc Method: 3** **Address: E95h**

This parameter specifies the maximum relative speech energy that may be detected and still receive DTMF signals. The speech energy is measured in the frequency region of second or third harmonics of the DTMF tones. To disable the speech energy detector, set this parameter to its full scale positive value (7FFFh). Decreasing the value of this parameter may degrade signal-to-noise ratio (SNR) performance, but may reduce false settings of status bit EDET due to speech signals. To increase or decrease the maximum speech energy parameter value, convert the increase/decrease into hex and add/subtract to/from the current value.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Equation: Maximum Speech Energy ± (Increase/Decrease)h

Function 105: Frequency Deviation, Low Group (DTMF) Acc Method: 3 Address: C94h

This parameter controls the acceptable frequency range for the low group DTMF tones (697, 770, 852, and 941 Hz). Increasing the value of this parameter increases the frequency range. The frequency range will vary from one DTMF symbol to another. To increase or decrease the parameter value, convert the increase/decrease into hex and add/subtract to/from the current value.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Equation: Frequency Deviation ±(Increase/Decrease)h

Function 106: Frequency Deviation, High Group (DTMF) Acc Method: 3 Address: E94h

This parameter controls the acceptable frequency range for the high group DTMF tones (1209, 1336, 1477, and 1633 Hz). Increasing the value of this parameter increases the frequency range. The frequency range will vary from one DTMF symbol to another. To increase or decrease the parameter value, convert the increase/decrease into hex and add/subtract to/from the current value.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Equation: Frequency Deviation ±(Increase/Decrease)h

Function 107: Negative Twist Control, TWIST4 (DTMF) Acc Method: 3 Address: D95h

This parameter controls the acceptable negative twist for the DTMF signals. Decreasing this parameter increases the acceptable negative twist level. The twist will vary from one DTMF symbol to another. To increase or decrease the parameter value, convert the increase/decrease into hex and add/subtract to/from the default value.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Equation: Negative Twist ±(Increase/Decrease)h

Default: 18CEh

Function 108: Positive Twist Control, TWIST8 (DTMF) Acc Method: 3 Address: C95h

This parameter controls the acceptable positive twist for the DTMF signals. Decreasing this parameter increases the acceptable positive twist level. The twist will vary from one DTMF symbol to another. To increase or decrease the parameter value, convert the increase/decrease into hex and add/subtract to/from the default value.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Equation: Positive Twist ±(Increase/Decrease)h

Default: 1B2Dh

Function 109: Maximum Energy Hit Time (DTMF) Acc Method: 3 Address: E87h

This parameter represents the duration of an allowed energy impulse during the off time measurement. The default value of 0000h means no gain hits will be tolerated during the off time.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Equation: [(Desired Time)(Sample Rate)]h

Function 110: ADC Speech Sample Scaling Parameter, ADCS (ADPCM Rx-coding)
Acc Method: 3 Address: F21h

The received signal sample is scaled by parameter ADCS prior to ADPCM compression by the Rx-coder. Decreasing the value of this parameter attenuates the received speech samples.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Default: 7FF0h

5. HDLC OPERATION

The HDLC (High Level Data Link Control) protocol is a standard procedure used for data communications. SDLC (Synchronous Data Link Control) is a bit-oriented protocol which is a subset of HDLC. The same format is used in both protocols although all SDLC fields must be eight-bit octets. The MDP uses the SDLC protocol but it is referred to as HDLC to avoid confusion.

5.1 HDLC FRAMES

Data and control information on a HDLC link are transmitted via frames. These frames organize the information into a format specified by an ISO standard that enables the transmitting and receiving station to synchronize with each other. This format is shown in Figure 5-1. Flags and the frame check sequence are distinguished from the other fields by status bits in the MDP interface memory.

Flags

All frames start and end with a flag sequence. The beginning flag and the ending flag are defined by the bit pattern 01111110 (7E). The ending flag for one frame can also serve as the beginning flag for the following frame. If separate ending and beginning flags are used, the final zero in the ending flag of one frame may also serve as the first zero of the beginning flag in the following frame. This process is known as "zero-sharing". The zero-sharing bit pattern is 011111101111110.

Address Field

The address field informs the receiver where the information is to go (if the primary station is transmitting) or where the message originated (if a secondary station is transmitting). This field is eight bits in length for the "basic" format.

For the "extended" format, the length is N number of octets, each octet having the first bit a binary zero with the exception of the last octet that begins with a binary one.

Control Field

The control field defines the function of the frame. It may contain a command or response. The control field might also contain send or/and receive sequence numbers. This field can be in one of the following formats:

1. Information Transfer Format
2. Supervisory Format
3. Unnumbered Format

This field is normally eight bits in length. Certain protocols allow for an extended control field of 16 bits in length.

Information Field

The MDP does not distinguish between the address field, the control field, or the information field. The information field does not have a set length; however, this field is in the SDLC protocol format of 8-bit bytes.

Zero Insertion

Since flags mark the beginning and ending of a frame, some method must be implemented to inhibit or alter the transmission of data that appear as flags. The method used is called "zero insertion". HDLC procedures require that a zero be transmitted following any succession of five continuous ones. This includes all data in the address, control, information and Frame Check Sequence (FCS) fields. Use of zero insertion denies any pattern of 01111110 to ever be transmitted between beginning and ending flags.

The MDP transmitter always performs zero insertion when in HDLC mode.

Zero Deletion

When transmitting flags, zero insertion is disabled. During reception of data, after testing for flag recognition, the receiver removes a zero that immediately follows five continuous ones. This is termed "zero deletion". A one that follows five continuous ones signifies either a frame abort (i.e., at least seven ones with no zero insertion) or a flag (i.e., 01111110). The sixth one is, therefore, not removed.

The MDP receiver always performs zero deletion when in HDLC mode.

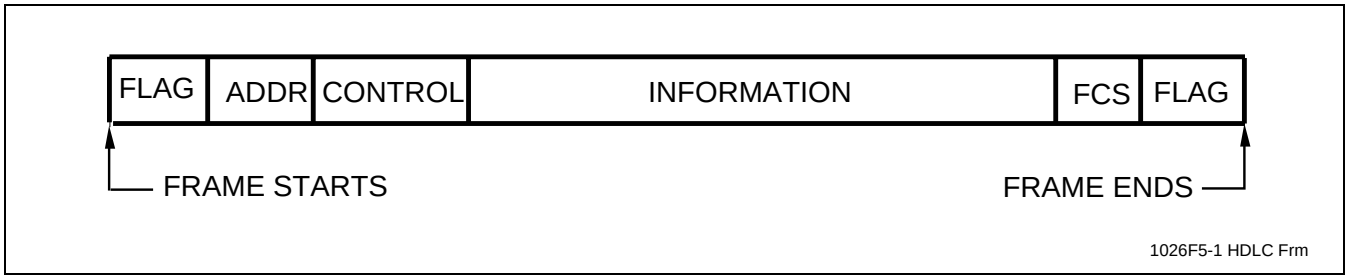


Figure 5-1. HDLC Frame

Frame Check Sequence

The purpose of the Frame Check Sequence (FCS) is to give a shorthand representation of the entire transmitted information field and to compare it to the identically generated shorthand representation of the received sequence. If any difference occurs, the received frame was in error and should be re-transmitted.

The FCS computation is done on all fields within the frame but does not include the flags. A standard Cyclic Redundancy Check (CRC) is used to compute the FCS. Either 16-bit (CRC16) (default) or 32-bit (CRC32) CRC may be selected using the ITU-T CRC32 RAM parameter (see parameter 52 in Section 4.4). The CRC polynomials are:

$$\text{CRC16} = x^{16} + x^{12} + x^5 + 1 \quad \text{(SDLC and X.25)}$$

$$\text{CRC32} = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + 1$$

The FCS is sent as two bytes of data immediately preceding the ending flag of the frame. The FCS register is first preset to all binary ones. The register is then modified by shifting in the data (no flags) contained in the address, control, and information fields. Following the last bit of data, the ones complement of the FCS register is transmitted as the FCS. The FCS is transmitted with the highest order bit first.

To disable the CRC transmission in HDLC mode, set bit 0B3h:6. This is needed for H.324 applications.

Frame Abortion, Frame Idle, and Time Fill

Frame abortion prematurely finishes transmission of a frame. This occurs by sending at least seven consecutive ones with no zero insertion. This abort pattern terminates a frame immediately and does not require a FCS or an ending flag.

An abort pattern followed by a minimum of eight additional consecutive ones idles the data link. Thus, seven to fourteen ones establish the abort pattern; fifteen or more ones constitute an idle pattern.

Interframe time fill is accomplished by transmitting continuous flags.

By default, if the host underruns the Transmit FIFO, the MDP will append a CRC. If bit 3A5h:6 is set, the MDP will instead abort the frame and provide an abort code of 41h in ABCODE.

5.2 OPERATION

5.2.1 Transmitter and Receiver Setup

To select HDLC mode, the host must:

1. Set the CONF bits to the desired MDP configuration. HDLC can be used in all data modes except the full-duplex FSK modes (i.e., V.21, V.23, and Bell 103).
2. Reset the ASYN bit to select synchronous mode, if not already in synchronous mode.
3. Set the TPDM bit to select Transmitter Parallel Data Mode (transmitting only). Setting TPDM is not required when receiving since received data is always available in RBUFFER. Note that HDLC transmission cannot be performed using the serial interface (TPDM = 0).
4. Set the FIFOEN bit to enable the TXFIFO if desired.
5. Set the RTS bit to turn on RTS (transmitting only).
6. Set the HDLC bit to select HDLC mode.
7. Set the NEWC bit.

5.2.2 Transmitter HDLC Operation

The format of the data input to the MDP is in groups of 8-bit bytes. As in the normal synchronous parallel data mode, the least significant bit of the byte is transmitted first.

Flag Transmission and Reception

In HDLC mode, the MDP will send continuous flags with no zero sharing (i.e., 0111111001111..) until the host loads data into the Transmit Data Buffer, TBUFFER (10h). Thus, the MDP defaults to transmitting time-fill and keeps the receiving link station active. The status bit FLAGS (0Ah:1) is set to indicate that the MDP is transmitting the flag sequence.

Information Field Transmission and Reception

If the FIFO is not enabled (FIFOEN bit = 0), if the next byte is not loaded into TBUFFER within the next eight bit times, the MDP interprets this as the end of a frame. If the FIFO is enabled (FIFOEN bit = 1), the TEOF bit must be set by the host to indicate that the next byte to be written into TBUFFER is the last byte in the frame. The host must reset the TEOF bit after writing the last byte of the current frame and before writing the first byte of the next frame.

FCS and Ending Flag Transmission and Reception

Following the detection end of frame, the MDP automatically sends the FCS and ending flag. Status bit CRCS (0Ah:2)is set just before the highest order bit is sent to indicate that the FCS is being transmitted. Once the host sees this bit set, the first byte of the next frame can be loaded. In this case, the ending flag serves as the beginning flag for the next frame. The MDP resets the CRCS bit when the ending flag is transmitted. At the same time, the MDP sets the FLAGS bit.

After the FCS transmission (immediately following bit x0), the MDP sends one flag to signify the end of the current frame and the beginning of the next frame. After the final zero in a flag is transmitted, the MDP looks to see if the host has loaded new data into TBUFFER. If no new data is loaded before this time, another flag is sent. Therefore, if more than one flag between frames is desired, the host must wait N-1 multiples of eight bit times after FLAGS is set by the MDP to load new data into TBUFFER, where N is the number of flags. The host then has seven bit times in which to load new data and thus prevent another flag from being sent. For example, if three flags are desired between frames, the host must wait at least 16 bit times and not more than 23 bit times after FLAGS is set by the MDP.

Abort/Idle Sequence Transmission and Reception

An abort/idle sequence can be sent by the host setting the MHLD bit (07h:0). The MDP stops sending any normal frame transmission, as well as continuous flag transmission, and sends continuous ones. To stop sending continuous ones, the host must reset MHLD. Then, if no new data is loaded into TBUFFER, the MDP sends continuous flags. If new data is loaded into TBUFFER, the MDP sends a beginning flag and then the data in TBUFFER.

5.2.3 Receiver HDLC Operation

The format of the data output to the host is in groups of 8-bit bytes. As in the normal synchronous parallel data mode, the least significant bit of the byte is transmitted first.

Flag Transmission and Reception

The MDP receiver continually searches for the flag data pattern. When one or more flags are detected, status bit SYNCD (0Ah:0) is set. The flags themselves are not presented to the host through the receiver data buffer RBUFFER (00h). The host must service the RDBF interrupt while waiting for the SYNC bit to be set to a 1 in order to clear the Receive FIFO of any unwanted or left- over characters and to ensure the alignment of the SYNCD bit with the received flag.

The MDP can also detect consecutive flags with zero-sharing.

Information Field Transmission and Reception

Received data between flags is passed to the host through the RBUFFER by the use of the handshaking bit RDBF (1Eh:0). The host must wait for RDBF to be set by the MDP before reading the status bits, followed by the received data in RBUFFER. Note that the RBUFFER and Receive FIFO can accumulate 144 bytes before overflowing. If the host does not read the data within 16 byte times, the data in RBUFFER will be overwritten by the next received byte and the Overrun Error bit (0Ah:3) will be set. The flag sequence and abort/idle sequence are not presented to the user. The receiver determines where the FCS field is by detecting the ending flag. There is at least a 16-bit time delay in the reception of data.

FCS and Ending Flag Transmission and Reception

Upon the receipt of an ending flag in the current frame (which may also be the beginning flag of the next frame), the receiver checks the data in the FCS register. If the FCS register remainder is correct, the PE bit (0Ah:5) is left a zero. If the remainder is incorrect, the PE bit is set. The FCS field is also passed to the host, in case the host wishes to do his own CRC checking. The receiver will set the SYNCD bit and the PE bit (if the MDP detected a frame with a bad CRC) after sending the FCS to the host. The MDP presets the FCS register to all ones after one or more flags are received.

After the FCS transmission (immediately following bit x0), one flag is sent to signify the end of the current frame and the beginning of the next frame. After the final zero in a flag is transmitted, the MDP looks to see if the host has loaded new data into TBUFFER. If no new data is loaded before this time, another flag is sent. Therefore, if more than one flag between frames is desired, the host must wait N-1 multiples of eight bit times after FLAGS is set by the MDP to load new data into TBUFFER, where N is the number of flags. The host then has seven bit times in which to load new data and thus prevent another flag from being sent. For example, if three flags are desired between frames, the host must wait at least 16 bit times and not more than 23 bit times after FLAGS is set by the MDP.

Abort/Idle Sequence Transmission and Reception

The MDP receiver not only continually searches for flags, but also continually searches for an abort/idle sequence. When the MDP detects this data pattern, it sets the FE bit (0Ah:4). The reception of data following the abort/idle sequence is treated as invalid data and is not presented to the host. Therefore, to re-establish transmitter and receiver synchronization, the receiver must see at least one flag. If FE is set, the current received data byte (typically FFh) should be discarded.

5.3 EXAMPLE APPLICATION

Refer to Table 3-1 for a description of the bits associated with the HDLC functions. Figure 5-2 illustrates bit timing.

5.3.1 Transmitter Example (Tx FIFO Disabled)

The steps to perform a typical HDLC transmission with the Transmitter FIFO disabled are (Figure 5-2a):

1. Set the MDP configuration in CONF; reset the ASYN and FIFOEN bits; set the HDLC, TPDM, and RTS bits.
2. The MDP starts transmitting flags immediately and continues with flags until the first byte of data is loaded into TBUFFER.
3. Wait for TDBE = 1, then place the first byte of data into TBUFFER. The MDP finishes transmitting the current flag followed by this byte of data.
4. As soon as TDBE is set, load in the next byte of data. This must occur within 2.5 bit times of TDBE being set.
5. After all information but the last byte is given to the MDP, load in the last byte of data in the frame as in step 4.
6. Wait until FLAGS is set to load in the first byte of the next frame. The MDP follows the last byte of the current frame with the FCS and a flag.
7. Repeat steps 4 through 6 for all frames to be transmitted.

5.3.2 Transmitter Example (Tx FIFO Enabled)

The steps to perform a typical HDLC transmission with the Transmitter FIFO enabled are:

1. Set the MDP configuration in CONF; reset the ASYN bit; set the FIFOEN, HDLC, TPDM, and RTS bits.
2. The MDP starts transmitting flags immediately and continues with flags until the first byte of data is loaded into TBUFFER.
3. Place the first byte of data into TBUFFER. The MDP finishes transmitting the current flag followed by this byte of data.
4. Continue to load data in TBUFFER until TXFNF = 0 or the last byte of the frame is reached.
5. After all information but the last byte is given to the MDP, set TEOF, then load in the last byte of data in the frame as in step 4.
6. Reset TEOF to 0.
7. Repeat steps 4 through 6 for all frames to be transmitted.

5.3.3 Receiver Example

The steps to perform a typical HDLC reception are (Figure 5-2b):

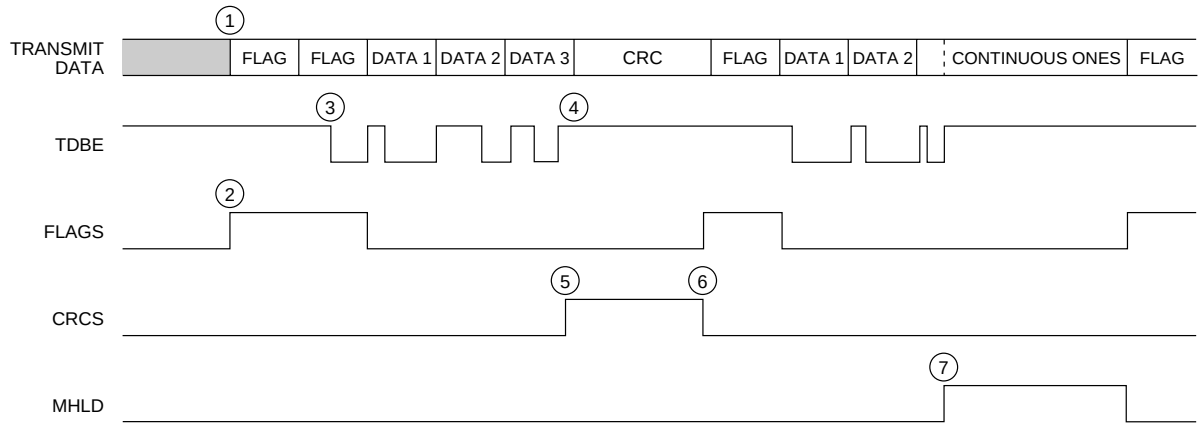
1. Set the MDP configuration in CONF; reset the ASYN bit; set the HDLC bit. Then monitor, through interrupts, the RDBF, OE, SYNCD, PE, and FE status bits.
2. Wait for an interrupt. If it is caused by the MDP setting RDBF (RDBIA is also set by the MDP), if NEWS = 1 or NSIA = 1, read status bits OE, SYNCD, PE, and FE.

   OE indicates that RBUFFER was loaded with new data before the host read the old data.

   SYNCD indicates that the MDP is receiving flags (RBUFFER = 7E).

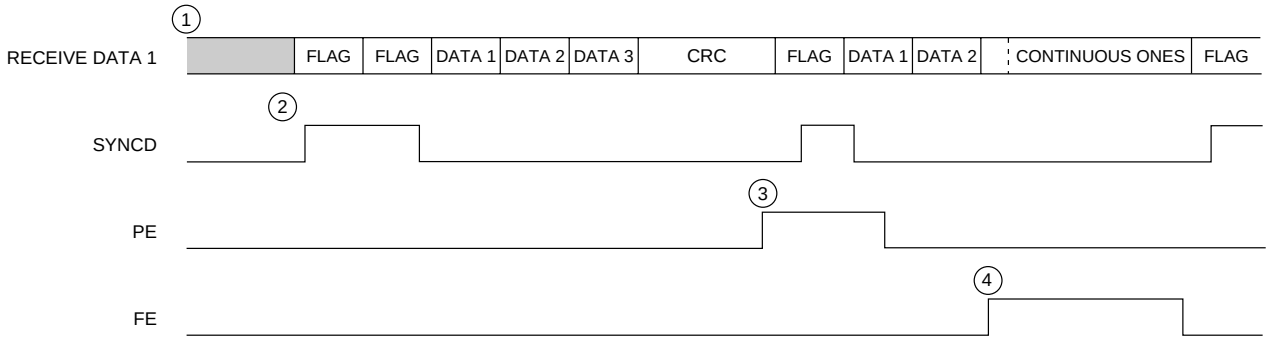
   PE indicates that the FCS had an incorrect CRC.

   FE indicates that an abort/idle sequence is detected (RBUFFER = FF) and the frame that was aborted is invalid. The MDP does not set the PE bit in this case since no FCS checking is done.
3. If NEWS = 0 and RDBF = 1 (or RXFNF = 1), read the received data in RBUFFER. **Note:** The host may continue to read the HDLC status bits followed by RBUFFER until the RXFIFO is empty, i.e., RDBF = 0 (or RXFNE = 0).
4. Continue waiting for interrupts and take appropriate action when the interrupts are received.



1. The host enters HDLC mode by setting HDLC bit.
2. The modem sets FLAGS prior to sending the first bit of the first 7E flag.
3. If the host loads the first data byte into TBUFFER while FLAGS is being sent, the data will not be sent until the flag is completely sent.
4. After TDBE is set, the host has 2.5 bit times to load new data into TBUFFER.
5. CRCS is set as soon as the last bit of the last data byte is sent and prior to sending the first bit of the CRC sequence. As soon as FLAGS is set, a new data byte of the next frame can be loaded.
6. CRCS is reset and FLAGS is set when the last bit of the CRC sequence is sent.
7. If MHLD is set anytime during the data, CRC, or flag transmission, the byte transmitted is interrupted and the abort sequence is started.

a. Transmitter (FIFOEN = 0)



1. Timing refers to when received data is presented to the host. Flags and the abort sequence are not presented to the host.
2. SYNCD will turn on 8-15 bit times after entering HDLC mode, when 7E flags are detected.
3. PE is set only if a bad CRC is detected by the modem.
4. FE will turn on when seven consecutive 1s are detected.

b. Receiver

1026F5-2 HDLC Timing

Figure 5-2. HDLC Signal Timing

6. HOST FUNCTIONS

6.1 INTERRUPT REQUEST HANDLING

DSP interface memory registers 00, 10, 1E, and 1F have unique hardware connections to the interrupt logic. Register 00 is the Receive Buffer (RBUFFER) and register 10 is the Transmit Buffer (TBUFFER). Registers 1E and 1F hold interrupt flag, interrupt enable, and interrupt active bits. When a condition occurs that satisfies an interrupt criteria, the corresponding interrupt flag bit is set. This interrupt flag can be reported to the host either by the host polling the interrupt flag bits (i.e., not using IRQ) or by being interrupted by IRQ. When an interrupt enable bit is a 1, IRQ is asserted and the appropriate interrupt active bit set to a 1 when the corresponding interrupt condition occurs.

The basic sources for IRQ generation are status change detected (status bit changes state, maskable in DSP RAM), configuration change implemented, receive buffer full, transmit buffer empty, and memory access (also maskable in DSP RAM). Each source is individually maskable.

Table 6-1 identifies the interrupt sources and describes the interrupt clearing procedures.

6.2 AUTO DIAL PROCEDURE

The host auto dial procedure is the same as outputting data to be transmitted using TBUFFER (Figure 6-1). The MDP timing accounts for the DTMF tone duration and amplitude, and inter-digit delay. These dialing parameters are host programmable in DSP RAM.

Calling tone on/off times are also programmable in DSP RAM. Calling tone levels are controlled by the Transmit Level bits (TLVL).

The levels of the high band and low band DTMF tones may be modified by the host in DSP RAM. The level of the high band DTMF tone should be 2 dB greater than the level of the low band DTMF tone. Transmit Level bits (TLVL) do not affect DTMF levels.

The auto dialer default parameters are given in Table 6-2.

6.3 AUTO MODE DETECTION

Figure 6-2 and Figure 6-3 show the flowcharts corresponding to the DSP algorithm used in supporting originating and answering automode (AUTO 15h:3), respectively.

Table 6-1. Interrupt Request Bits

Interrupt Active Bit	Interrupt Enable Bit	Interrupt Flag Bit	Interrupt Condition Description	Interrupt Clear Procedure
NSIA	NSIE	NEWS	New status detected (NEWS transitioned from a 0 to 1) a. RAM read or RAM write occurred b. Status bit changed in register 0A-0F, 01, 12, 14, 16-17, 1A, or 1B	Host writes a 0 into NEWS (Clears NSIA to a 0)
NCIA	NCIE	NEWC	New configuration implemented by the MDP (NEWC transitioned from a 1 to a 0).	Host writes a 0 into NCIE (Clears NCIA to a 0)
TDBIA	TDBIE	TDBE	TBUFFER is empty and can be written (TDBE transitioned from a 1 to a 0)	Host writes to BUFFER (10h:7-0) (Clears TDBE and TDBIA to 0)
RDBIA	RDBIE	RDBF	RBUFFER is full and can be read (RDBF transitioned from a 0 to a 1).	Host reads RBUFFER (00h:7-0) Clears RDBF and RDBIA to 0)

Table 6-2. Auto Dial Default Values

Parameter	Default Value
DTMF Tone Duration	92 ms
DTMF Interdigit Delay	72 ms
DTMF Total Output Power Level	0 dBm
DTMF Low Band Power Level	–4 dBm
DTMF High Band Power Level	–2 dBm
Pulse Relay Make Time	36 ms
Pulse Relay Break Time	64 ms
Pulse Interdigit Delay	750 ms
Calling Tone On Time	500 ms
Calling Tone Off Time	2 s

Dial Digits/Tone Pairs

Hex	Dial Digit	Tone Pairs	
		Tone 1	Tone 2
00	0	941	1336
01	1	697	1209
02	2	697	1336
03	3	697	1477
04	4	770	1209
05	5	770	1336
06	6	770	1477
07	7	852	1209
08	8	852	1336
09	9	852	1477
0A	*	941	1209
0B	#	941	1477
0C	A	697	1633
0D	B	770	1633
0E	C	852	1633
0F	D	941	1633
10	1300 Hz Calling Tone		
11	1100 Hz Calling Tone		

NOTE: Calling tone is continuously transmitted with the appropriate on-off time until NEWC is set or FFh is written into TBUFFER.

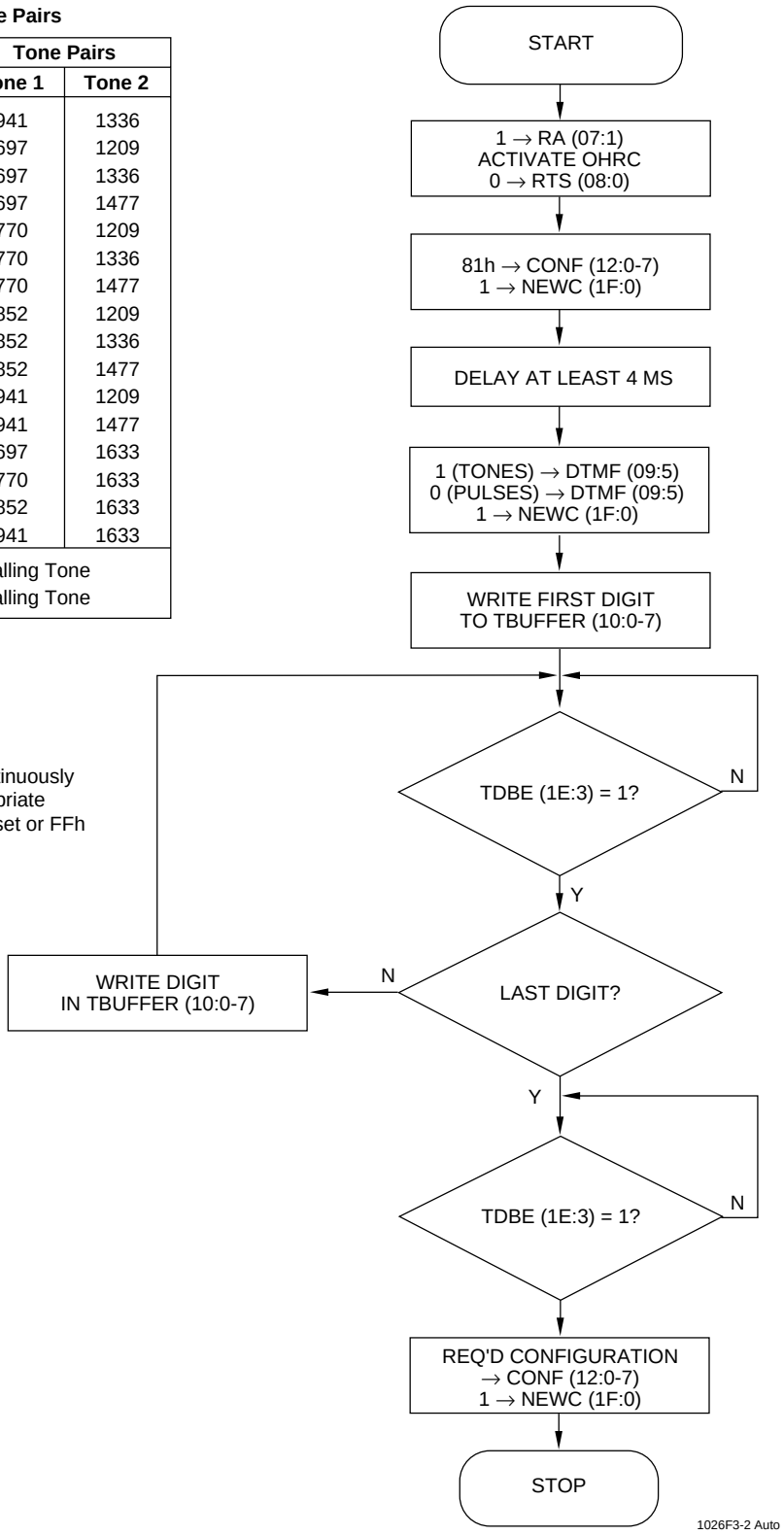


Figure 6-1. Auto Dial Sequence and Dial Digits

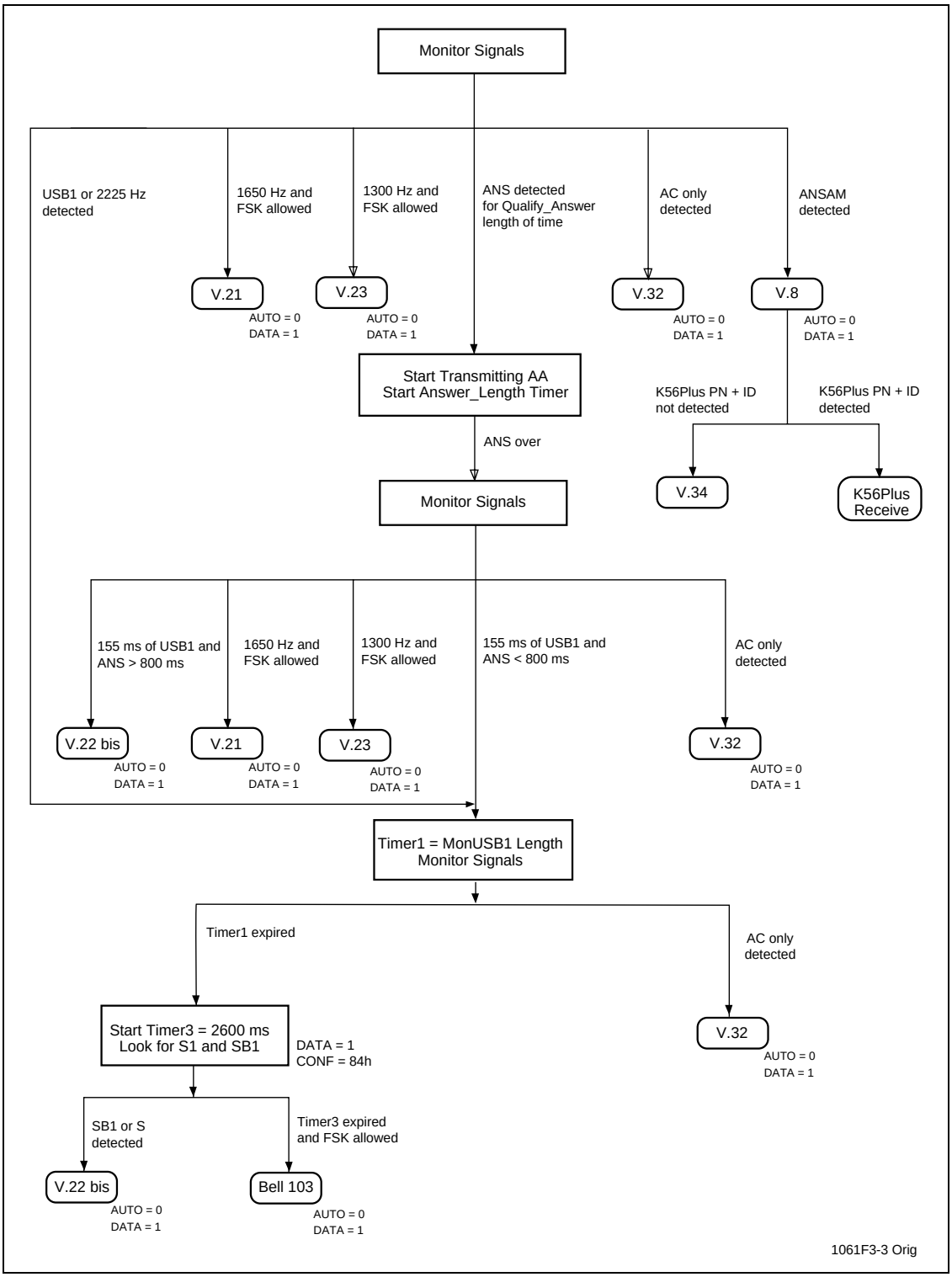


Figure 6-2. Host Flowchart - Originating Automode

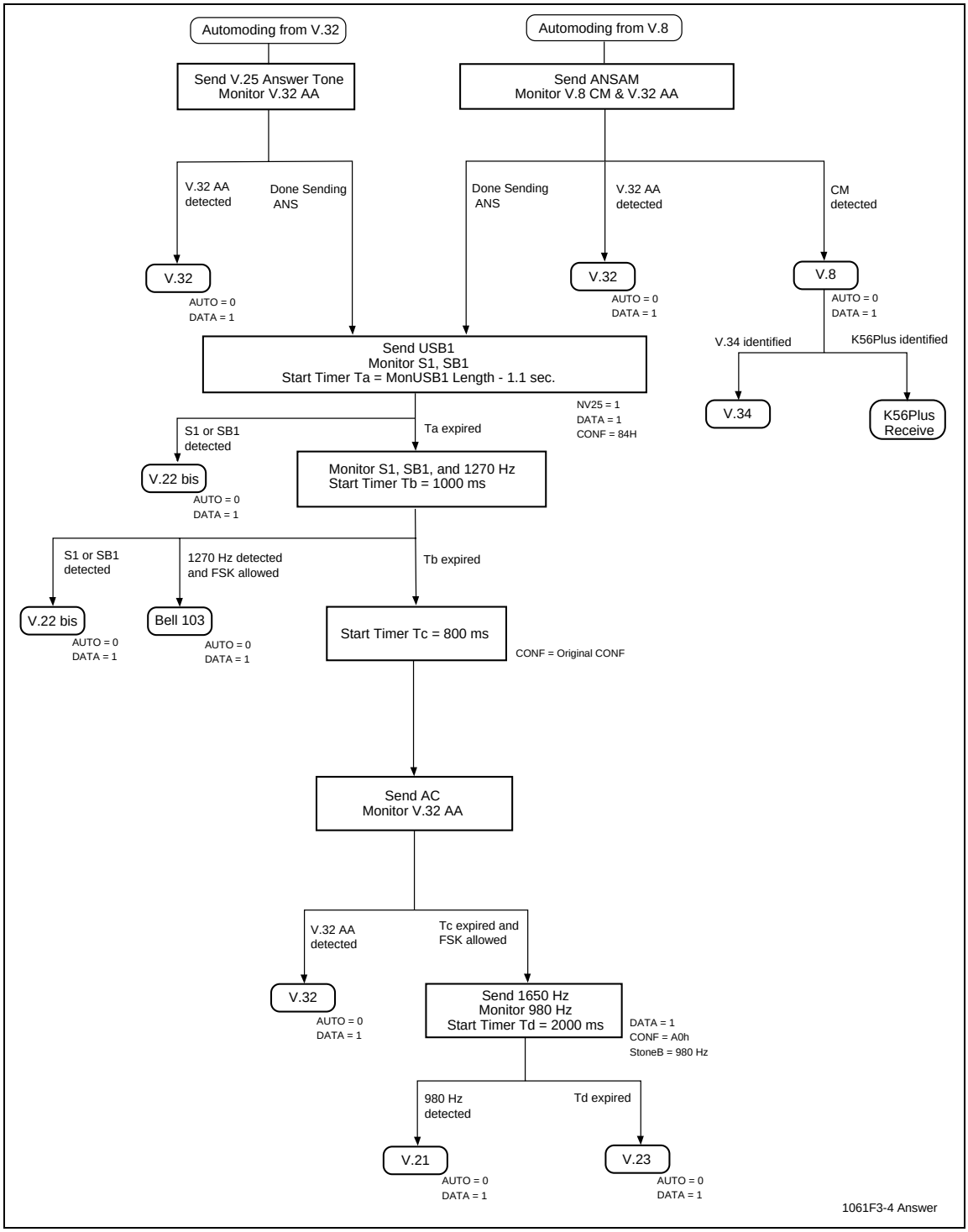


Figure 6-3. Host Flowchart - Answering Automode

6.4 MODEM SELF-TEST INFORMATION

After a power-on reset, the MDP performs a self-test of the internal controller and DSP devices. After each self-test, the test results and configuration information is loaded into interface memory.

Figure 6-4 shows the flowchart for reading the self-test data.

6.4.1 Controller Self-Test

The controller self-test is performed first. Upon test completion, the following test results and configuration information is loaded into interface memory:

Register	Function	Value (Hex)*	Value Type
1D, 1C	RAM1 Checksum	EA3C	Constant
1B, 1A	RAM2 Checksum	5536	Constant
19, 18	ROM1 Checksum	5F4C	Constant
17, 16	ROM2 Checksum	3835	ASCII 82
15, 14	Timer/ROM/RAM	0801	Constant
13, 12	Part Number	3730	ASCII 46
11, 00	Revision Level	4241	ASCII BA
* Values shown are typical and may not reflect the current code release.			

The host should read the test results within 5 ms of the appearance of RAM1 and RAM2 checksums. Register 10 should then be read to reset bit 1Eh:3 (ignore the read value).

When bit 1Eh:3 is reset or 5 ms has expired, the information is cleared and the DSP self-test is performed. If the register 10 is not read by the host, bit 1Eh:3 will not be reset.

6.4.2 DSP Self-Test

Upon completion of DSP self-test, the following test results and configuration information is loaded into interface memory and bit 1Eh:3 is set to a 1:

Register	Function	Value (Hex)*	Value Type
1B, 1A	EC Checksum	F083	Constant
19, 18	Multiplier Checksum	46EE	Constant
17, 16	RAM Checksum	00FA	Constant
15, 14	ROM Checksum	0A09	ASCII 82
13, 12	Part Number	3730	ASCII 46
11, 00	Revision Level	2041	ASCII A
* Values shown are typical and may not reflect the current code release.			

The host should read the test results within 5 ms of bit 1Eh:3 being set.

When bit 1Eh:3 is reset or 5 ms has expired since DSP test completion, the information is cleared and MDP initialization continues.

Soft Reset. If reading the self-test information by performing a soft reset (see SFRES in Table 3-1), set SFRES, then set NEWC (do not wait for NEWC to clear). Proceed as described above. After reading the desired information, wait for NEWC to clear plus 10 ms before accessing the MDP.

NOTE: The reset time for both a hard or soft reset is under 150 ms.

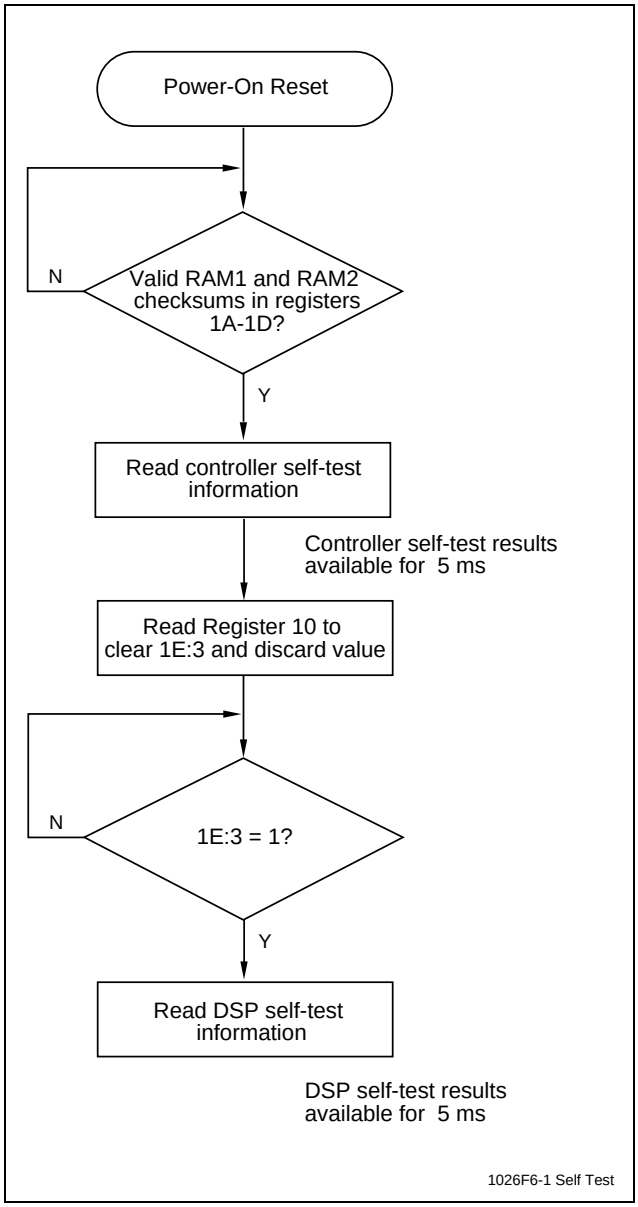


Figure 6-4. Modem Self-Test Results Read Procedure

6.5 EQM AVERAGING

A host-programmable EQM averaging feature helps the host controller with retrain and rate change decisions. A single-pole low-pass filter is used to average the EQM samples. The number of symbol intervals between EQM samples is host-programmable in memory location 26Bh (*EQMBaudInterval*). Also, the host can program the number of EQM samples to be used before the final filtered EQM value (*FilteredEQM*) is determined. The EQMAT bit is set if this final *FilteredEQM* (address 26Fh) is larger than the EQMAT threshold (address 133h). If *EQMBaudInterval* is 0, then the EQM averaging is disabled as is by default. Suitable values for addresses 26Bh and 26Ch are 20h and 64h, respectively. They may be altered as desired. The value obtained at address 26Fh is the same as if the host were to read and average the MSB of EQM read at address 20Ch (Function 46). All RAM accesses are 8-bit.

Parameter Name	Address (Hex)	Default Value	Description
EQM Baud Interval	26B	0	Symbols between EQM samples used as input to LPF.
Num EQM Samples	26C	0	EQM samples to be run through the EQM LPF.
Saved Filtered EQM	26F		Output of EQM filter used for EQMAT determination (MSB value).

6.6 RETRAIN AND AUTOMATIC RATE CHANGE

This section explains how to perform the retrain and rate change.

6.6.1 Retrain Without a Rate Change

K56flex/V.34/V.32/V.32 bis and V.22 bis Configurations

When the RTRN bit is set to a 1, the MDP will initiate the retrain sequence. The modem which detects the retrain sequence will respond with training, and both modems will proceed with the proper training sequence. The retrain process can be monitored by observing the appropriate status bits in the transmitter and receiver.

6.6.2 Retrain With a Rate Change

K56flex/V.34/V.32/V.32 bis and V.22 bis Configurations

The following procedure describes how to obtain a rate change along with a retrain.

1. Store the desired configuration in the CONF register. Use configuration code 82h (V.22 bis/1200) for fall forward or fallback between 2400 bps and 1200 bps. **NOTE:** Do not set the NEWC bit.
2. Set the RTRN bit to a 1.

The MDP will then send the retrain sequence at the correct operating speed as selected in the configuration registers. The rate sequence is automatically changed in the training sequence to tell the other modem at what speed to operate. The status bits will change as mentioned above and the CTS bit will be set to a 1 when the retrain sequence is completed. (See the RREN bit description in Table 3-1 for rate change procedures in K56flex/V.34/V.32 bis modes using a rate renegotiation rather than a retrain. Also, see the SRCEN bit description in Table 3-1 for rate change procedures in V.34 mode using the secondary channel.)

6.7 HANDSHAKE TIME-OUT TIMERS

If any part of the handshake is not detected, the MDP will time out and abort the handshake. In this case, the transmitter will immediately stop sending the training sequence. Also, the MDP, upon timing out, will load an error code into register 14 (ABCODE) of interface memory that indicates that point in the handshake the time-out occurred. The error code is not cleared even if the MDP immediately goes into a new handshake after aborting. The user can observe this register during the handshake to determine if an abort occurred.

The user can progressively observe the handshake detector bits (AADET, ACDET, CCDET, SECTXD, SECRXD, etc.) to determine how the handshake is proceeding. The user can thus be interrupted at each step of the handshake progression.

The K56flex, V.34, and V.32 handshake error codes and their meanings are:

Error Code	Reason For Aborting (Time-out)
00	No error
01- FF	See ABCODE in Table 3-1 and error code definitions in Table 3-2.

6.8 CLEARDOWN

6.8.1 K56flex Cleardown

Sourcing a K56flex Cleardown Request

1. The host loads CONF with 90h.
2. The host sets RREN to 1

Receiving a K56flex Cleardown Request

1. On receiving a Cleardown request, the MDP responds by writing 96h into the ABCODE register and also writing C0h into the CONF register. RAM location 2E4h (see Section 4, Function 1) will also be cleared to zero.

6.8.2 V.34 Cleardown

Sourcing a V.34 Cleardown Request

The Cleardown procedure provided in the V.34 modes is strictly defined, and as such there is now only one method to initiate the Cleardown. The retrain method that has been provided in V.32bis is not supported in V.34. The method used is:

1. The host loads CONF with C0h.
2. The host sets RREN to 1
3. The data pump transmits Cleardown request as per §11.7 of ITU-T Recommendation V.34.

Receiving a V.34 Cleardown Request

1. On receiving a Cleardown request, the MDP responds by writing 96h into the ABCODE register and also writing C0h into the CONF register. RAM location 2E4h (see Section 4, Function 1) will also be cleared to zero.

6.8.3 V.32 bis Cleardown

Sourcing a V.32 bis GSTN Cleardown Request

1. The host loads CONF with 70h.
2. The host sets either RTRN or RREN to a 1.
3. RLSD drops automatically.

Receiving a V.32 bis Cleardown Request

1. The host loads CONF with 70h.
2. RLSD drops automatically.

7. DESIGN CONSIDERATIONS

Good engineering practices must be adhered to when designing a printed circuit board (PCB) containing the MDP. Suppression of noise is essential to the proper operation and performance of the MDP itself and for surrounding equipment.

Two aspects of noise in an OEM board design containing the MDP must be considered: on-board/off-board generated noise that can affect analog signal levels and analog-to-digital conversion (ADC)/digital-to-analog conversion (DAC), and on-board generated noise that can radiate off-board. Both on-board and off-board generated noise that is coupled on-board can affect interfacing signal levels and quality, especially in low level analog signals. Of particular concern is noise in frequency ranges affecting modem performance.

On-board generated electromagnetic interference (EMI) noise that can be radiated or conducted off-board is a separate, but equally important, concern. This noise can affect the operation of surrounding equipment. Most local governing agencies have stringent certification requirements that must be met to allow use in specific environments.

Proper PC board layout (component placement, signal routing, trace thickness and geometry, etc.), component selection (composition, value, and tolerance), interface connections, and shielding are required for the board design to achieve desired modem performance and to attain EMI certification.

All the aspects of proper engineering practices are beyond the scope of this designer's guide. The designer should consult noise suppression techniques described in technical publications and journals, electronics and electrical engineering text books, and component supplier application notes. Seminars addressing noise suppression techniques are often offered by technical and professional associations as well as component suppliers.

7.1 PC BOARD LAYOUT GUIDELINES

1. Provide an adequate ground.
   a) In a 2-layer design, provide a ground grid in all unused space around and under components (judiciously near analog components) on both sides of the board and connect in such a manner as to avoid small islands. A grid is preferred over a plane to improve solderability. Typically, the grid is composed of .012 in. traces and .012 in. spaces on a .025 in. grid. Connect each grid to other grids on the same side at several points and to grids on the opposite side through the board at several points. Connect all MDP DGND and AGND pins to the ground grid.
   b) In a 4-layer design, provide a ground plane covering the entire board. Connect all MDP DGND and AGND pins to the ground plane at a single point.
2. As a general rule, route digital signals on the component side of the PCB and the analog signals on the solder side. The sides may be reversed to match particular OEM requirements. Route the digital traces perpendicular to the analog traces to minimize signal cross coupling.
3. Route the MDP signals to provide maximum isolation between noise sources and noise sensitive inputs. When layout requirements necessitate routing these signals together, they should be separated by neutral signals. The MDP noise source, neutral, and noise sensitive pins are listed in Table 7-1.
4. All power and ground traces should be at least 0.05 inch wide.
5. Keep all traces and component leads connected to crystal input and output pins (e.g., XTLI and XTLO) short in order to reduce induced noise levels and minimize any stray capacitance that could affect the crystal oscillator. Keep the XTLO trace extremely short with no bends greater than 45 degrees and containing no vias since the XTLO pin is connected to a fast rise time, high current driver.
6. Connect crystal can(s) to ground.
7. Locate the MDP and all supporting analog circuitry, including the data access arrangement, on the same area of the PCB.
8. Locate the analog components close to and on the side of board containing the TXA1, TXA2, and RIN signals.
9. Avoid placing noisy components and traces near TXA1, TXA2, RIN, VC, and VREF lines.
10. Locate receivers and drivers for DTE EIA-232 serial interface signals close to the connectors and away from traces carrying high frequency clocks in order to avoid/minimize the addition of noise suppression components (i.e., chokes and capacitors) for each line.
11. Route MDP interconnect signals (e.g., MSCLK to IA1CLK or MSTROBE to SA1CLK) directly to the interfacing by the shortest possible route avoiding all analog components.
12. Provide an RC network on the VAA supply in the immediate proximity of the AVAA pin to filter out high frequency noise above 115 kHz. A tantalum capacitor is recommended (especially in a 2-layer board design) for improved noise immunity with a current limiting series resistor or inductor to the VAA supply which meets the RC filter frequency requirements.

13. Provide a 0.1 µF ceramic decoupling capacitor to ground between the high frequency filter and the AVAA pin.
14. Provide a 0.1 µF ceramic decoupling capacitor to ground between the VCC supply and the VDD pins.

Table 7-1. Modem Pin Noise Characteristics

Device	Function	Noise Source	Neutral	Noise Sensitive
MDP 144-Pin TQFP	VDD, AVDD, AVAA, VGG, PLLVDD		13, 23, 37, 50, 79, 107, 117, 137-138	
	GND, DGND, AGND, PLLGND		14, 18-19, 21, 31, 49, 51-52, 60-61, 84, 109, 121, 132	
	Crystal/Clock	7, 122-123, 140-141, 143		
	Control		32, 40, 59, 72, 85-86, 113, 115, 133	
	Line Interface		35, 48	20, 22, 25-30, 33-34, 128
	Speaker Interface			24, 36
	Serial/LED Interface	71, 76-77, 108, 111, 134	75, 78, 112, 125, 127, 129	
	Host Interface	1, 3-4, 6, 8, 9- 12, 64- 69, 144	130	
	MDP Interconnect	42-47, 53- 58, 73, 87-91, 93-94, 103-104, 106		
	Reserved or NC		2, 5, 15-17, 38-39, 41, 62-63, 70, 74, 80-83, 92, 95-102, 105, 110, 114, 116, 118-120, 124, 126, 131, 135-136, 139, 142	
MDP 100-Pin PQFP	VDD, AVDD, AVAA, VGG, PLLVDD		28, 40, 49, 63, 71, 85, 98	
	GND, DGND, AGND, PLLGND		16, 25 39, 48, 65, 81, 99-100	
	Crystal/Clock	75-76, 86-87		
	Control		9, 17, 36, 56, 69,	
	Line Interface		47	26-27, 30-35, 37, 79
	Speaker Interface			29, 38
	Serial/LED Interface	8, 12-13, 64, 82	11, 67-68, 78,	
	Host Interface	2-7, 88-97	80	
	MDP Interconnect	41-46, 50-55, 59-60, 62		
	Reserved or NC		1, 14-16, 57-58, 61, 66, 70, 72-74, 77, 83-84	

7.2 ELECTROMAGNETIC INTERFERENCE (EMI) CONSIDERATIONS

The following guidelines are offered to specifically help minimize EMI generation. Some of these guidelines are redundant with, or similar to, the general guidelines but are mentioned again to reinforce their importance.

In order to minimize the contribution of the modem-based design to EMI, the designer must understand the major sources of EMI and how to reduce them to acceptable levels.

These guidelines assume a microcontroller unit (MCU) is connected to the MDP.

Crystal Circuit

1. Place the crystal and related components as close as possible to the MCU and MDP devices, and in particular, the XTLI and XTLO pins.
2. For MCU and MDP devices that do not have an internal series resistor in the crystal circuit, place a 100-ohm (typical) resistor between the XTLO pin and the crystal/capacitor node.
3. Connect crystal capacitor ground connections directly to GND pin on the MCU and MDP devices. Do not use common ground plane or ground trace to route the capacitor GND pin to the corresponding MCU or MDP GND pin.

Digital Components

1. Place digital components close together in order to minimize signal trace length.
2. Use decoupling capacitors (0.1 µF) on each digital component.
3. Place one large 10 µF tantalum capacitor between power and ground near digital components.

Circuit Traces

1. Avoid right angle (90 degree) turns on high frequency traces. Use smoothed radiuses or 45 degree corners.
2. Minimize the number of through-hole connections (feedthroughs) on traces carrying high frequency signals.
3. Keep all signal traces away from crystal circuits.
4. Keep digital signals, EIA/TIA-232 signals, and DAA signals separated from each other.
5. Provide a good ground plane or grid. In some cases, a multilayer board may be required with full layers for ground and power distribution.
6. Eliminate ground loops, which are unexpected current return paths to the power source.
7. Locate high frequency circuits in a separate area to minimize capacitive coupling to other circuits.
8. Locate cables and connectors so as to avoid coupling from high frequency circuits.
9. Lay out the highest frequency signal traces next to the ground grid.
10. If a multilayer board design is used, make no cuts in the ground or power planes and be sure the ground plane covers all traces.
11. On 2-layer boards with no ground grid, provide a shadow ground trace on the opposite side of the board to traces carrying high frequency signals. This will be effective as a high frequency ground return if it is three times the width of the signal traces.
12. Distribute high frequency signals continuously on a single trace rather than several traces radiating from one point.

Signal Conditioning

1. Keep traces carrying high frequency signals as short as possible.
2. Condition high frequency, long trace, and digital signals by inserting a series resistor (300 ohm typical) in the signal source.
3. Conditioning the ~READ signal alone may provide adequate EMI reduction.
4. Conditioning the address or data lines might also be necessary.

EIA/TIA-232 Interface Components

1. Place components close to each other and close to the EIA/TIA-232 interface cable connector.
2. Connect power and ground for all RS-232 components to the power and ground source points via separate power and ground traces that are not connected to the digital power and ground "except" at these source points. Power and ground source points are the board input pins or a regulator output if used.
3. Connect RS-232 cable signal ground wire to the ground source point.
4. Connect the EIA/TIA-232 cable shield ground to the ground source point.

Telephone and Local Hand Set Interface

1. Place common mode chokes in series with Tip and Ring for each connector.
2. Decouple the telephone line cables at the telephone line jacks. Typically, use a combination of series inductors, common mode chokes, and shunt capacitors. Methods to decouple telephone lines are similar to decoupling power lines, however, telephone line decoupling may be more difficult and deserves additional attention. A commonly used design aid is to place footprints for these components and populate as necessary during performance/EMI testing and certification.
3. Place high voltage filter capacitors (.001 µF @1KV) from Tip and Ring to Ground.

Stand Alone Modem Chassis

1. Use a metal enclosure.
2. If a plastic enclosure is required, internal metal foil lining the enclosure or conductive spray applied to the top and bottom covers may reduce emissions.

Power and Ground

1. Keep the current paths of separate board functions isolated, thereby reducing the current's travel distance. Separate board functions are: host interface, display, digital (SRAM, EPROM, MCU, MDP), and DAA. Power and ground for each of these functions should be separate islands connected together at the power and ground source points only.
2. Do not place ground or voltage planes beneath the telephone line side of the Tip and Ring chokes.
3. Decouple power from ground with decoupling capacitors as close to the MDP device power pins as possible.
4. Decouple the power cord at the power cord interface with decoupling capacitors. Methods to decouple power lines are similar to decoupling telephone lines.

Optional Configurations

Because fixed requirements of a design may alter EMI performance, guidelines that work in one case may deliver little or no performance enhancement in another. Initial board design should, therefore, include flexibility to allow evaluation of optional configurations. These optional configurations may include:

1. Chokes in Tip and Ring lines replaced with jumper wires as a cost reduction if the design has sufficient EMI margin.
2. Various grounding areas connected by tie points (these tie points can be short jumper wires, solder bridges between close traces, etc.).
3. EIA/TIA-232 cable ground wire or cable shielding connected on the board or floated.
4. Two designs in parallel with one based on a two layer board and the other based on a four layer board. During the evaluation phase, better performance of one design over another may result in quicker time to market.

7.3 CRYSTAL SPECIFICATIONS

Recommended crystal specifications are listed in Table 7-2 (28.224 MHz) and Table 7-3 (56.448 MHz).

Table 7-2. Crystal Specifications - 28.224 MHz

Characteristic	Value	Value
Rockwell Part No.	333R44-011	5333R02-020
Electrical		
Frequency	28.224 MHz nom.	28.224 MHz nom.
Frequency Tolerance	±50 ppm (C_L = 16.5 and 19.5 pF)	±50 ppm (C_L = 16.5 and 19.5 pF)
Frequency Stability		
vs. Temperature	±30 ppm (0°C to 70°C)	±35 ppm (0°C to 70°C)
vs. Aging	±20 ppm/5 years	±15 ppm/4 years
Oscillation Mode	Fundamental	Fundamental
Calibration Mode	Parallel resonant	Parallel resonant
Load Capacitance, C_L	18 pF nom.	18 pF nom.
Shunt Capacitance, C_O	7 pF max.	7 pF max.
Series Resistance, R_1	35 Ω max. @20 nW drive level	60 Ω max. @20 nW drive level
Drive Level	100µW correlation; 500µW max.	100µW correlation; 300µW max.
Operating Temperature	0°C to 70°C	0°C to 70°C
Storage Temperature	–40°C to 85°C	–40°C to 85°C
Mechanical		
Dimensions (L x W x H)	11.05 x 4.65 x 13.46 mm max.	7.5 x 5.2 x 1.3 mm max.
Mounting	Through Hole	SMT
Holder Type	HC-49/U	None
Suggested Suppliers		
	KDS America	KDS America
	ILSI America	ILSI America
	Vectron Technologies, Inc.	Vectron Technologies, Inc.

Notes

1. Characteristics @ 25°C unless otherwise noted.
2. Supplier Information:

KDS America
Fountain Valley, CA 92626
(714) 557-7833

ILSI America
Kirkland, WA 98033
(206) 828 - 4886

Vectron Technologies, Inc.
Lowell, NH 03051
(603) 598-0074

Table 7-3. Crystal Specifications - 56.448 MHz

Characteristic	Value	Value
Rockwell Part No.	333R45-011	5333R02-017
Electrical		
Frequency	56.448 MHz nom.	56.448 MHz nom.
Frequency Tolerance	±40 ppm (C_L = 16.5 and 19.5 pF)	±50 ppm (C_L = 16.5 and 19.5 pF)
Frequency Stability		
vs. Temperature	±45 ppm (0°C to 70°C)	±35 ppm (0°C to 70°C)
vs. Aging	±15 ppm/5 years	±15 ppm/4 years
Oscillation Mode	Third overtone	Third overtone
Calibration Mode	Parallel resonant	Parallel resonant
Load Capacitance, C_L	18 pF nom.	18 pF nom.
Shunt Capacitance, C_O	7 pF max.	7 pF max.
Series Resistance, R_1	35 Ω max. @20 nW drive level	80 Ω max. @20 nW drive level
Drive Level	100µW correlation; 500µW max.	100µW correlation; 300µW max.
Operating Temperature	0°C to 70°C	0°C to 70°C
Storage Temperature	–40°C to 85°C	–40°C to 85°C
Mechanical		
Dimensions (L x W x H)	11.05 x 4.65 x 13.46 mm max.	7.5 x 5.2 x 1.3 mm max.
Mounting	Through Hole	SMT
Holder Type	HC-49/U	None
Suggested Suppliers		
	KDS America	KDS America
	ILSI America	ILSI America
	Vectron Technologies, Inc.	Vectron Technologies, Inc.

Notes

1. Characteristics @ 25°C unless otherwise noted.
2. Supplier Information:

   KDS America
   Fountain Valley, CA 92626
   (714) 557-7833

   ILSI America
   Kirkland, WA 98033
   (206) 828 - 4886

   Vectron Technologies, Inc.
   Lowell, NH 03051
   (603) 598-0074

7.4 RECOMMENDED INTERFACE CIRCUITS

A typical external circuit for connection to the line with no external hybrid and a transmit level to -7 dBm is shown in Figure 7-5.

A typical external circuits for connection to the line with an external hybrid and a transmit level to 0 dBm is shown in Figure 7-6.

A typical external speaker circuit is shown in Figure 7-7.

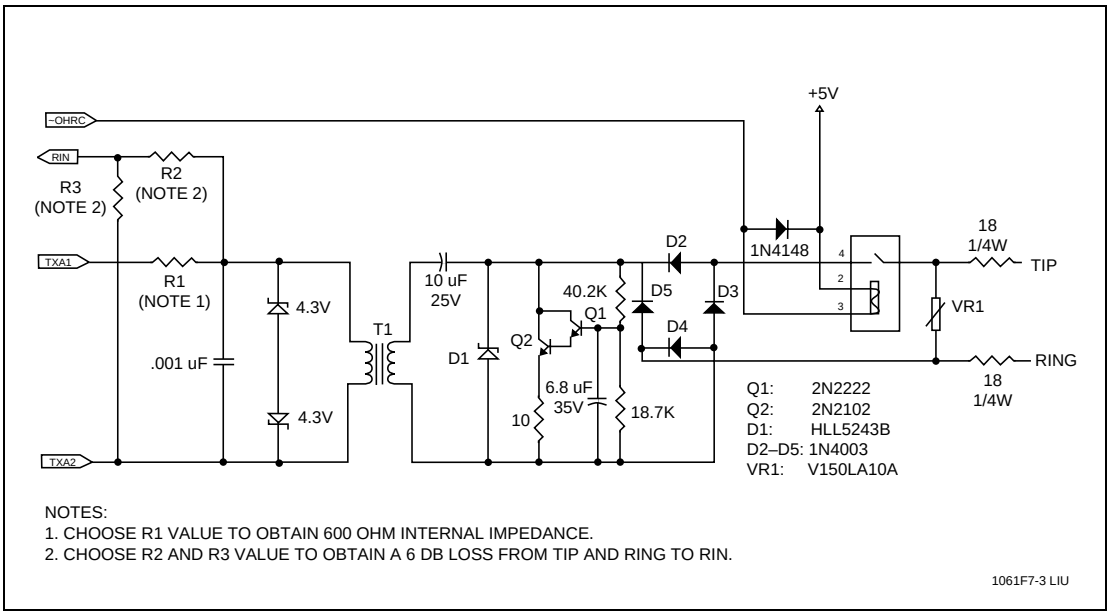


Figure 7-5. Typical Line Interface

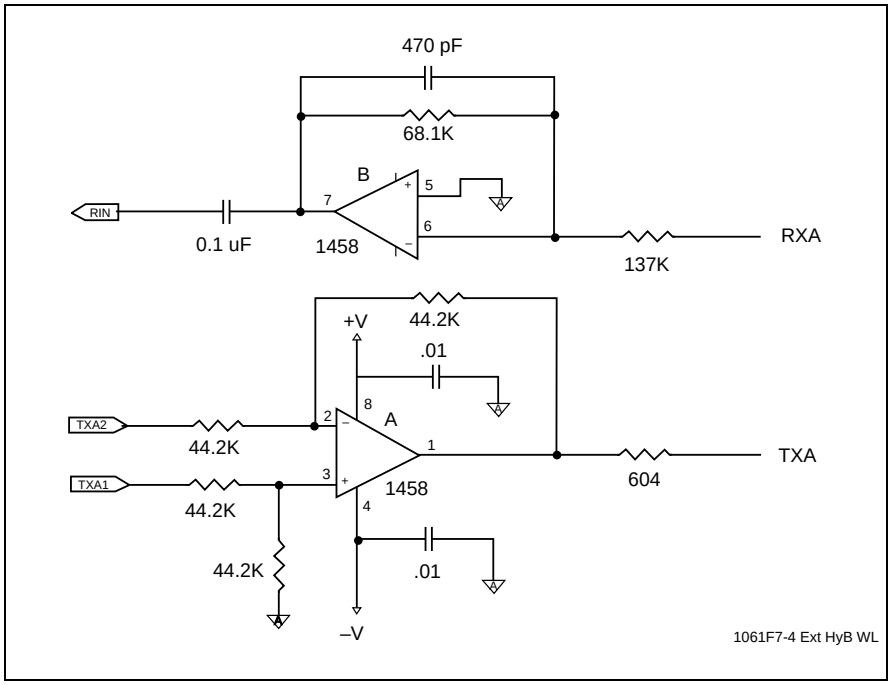


Figure 7-6. Typical Interface to External Hybrid

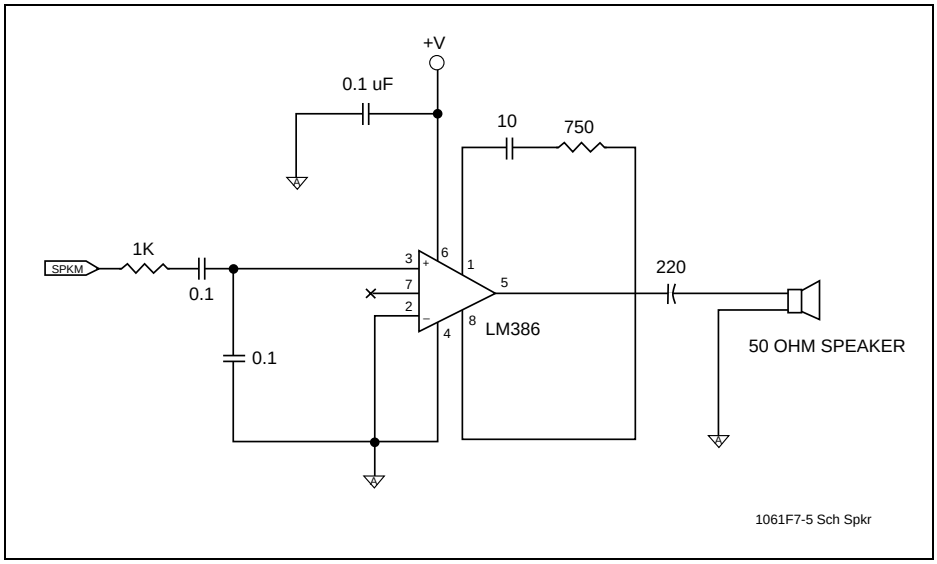
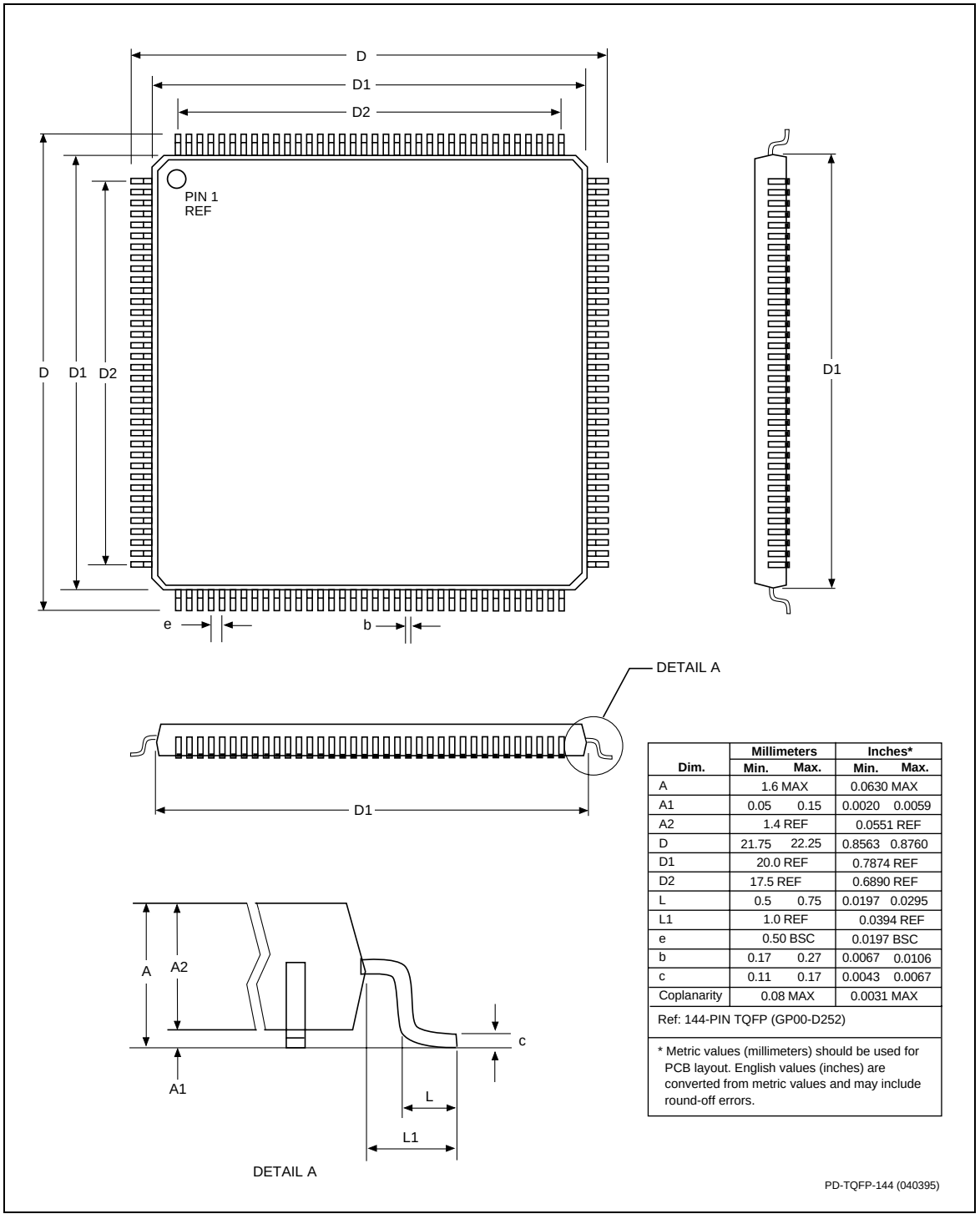


Figure 7-7. Typical External Speaker Circuit

7.5 PACKAGE DIMENSIONS

The 144-pin TQFP package dimensions are shown in Figure 7-8 (144-pin TQFP) and Figure 7-9 (100-pin PQFP).

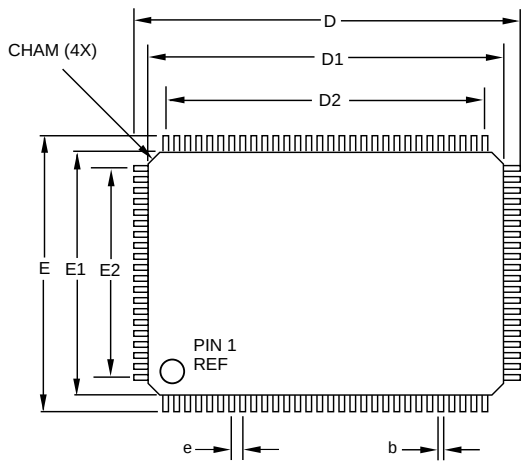


Dim.	Millimeters Min.	Millimeters Max.	Inches* Min.	Inches* Max.
A		1.6 MAX		0.0630 MAX
A1	0.05	0.15	0.0020	0.0059
A2		1.4 REF		0.0551 REF
D	21.75	22.25	0.8563	0.8760
D1		20.0 REF		0.7874 REF
D2		17.5 REF		0.6890 REF
L	0.5	0.75	0.0197	0.0295
L1		1.0 REF		0.0394 REF
e		0.50 BSC		0.0197 BSC
b	0.17	0.27	0.0067	0.0106
c	0.11	0.17	0.0043	0.0067
Coplanarity		0.08 MAX		0.0031 MAX

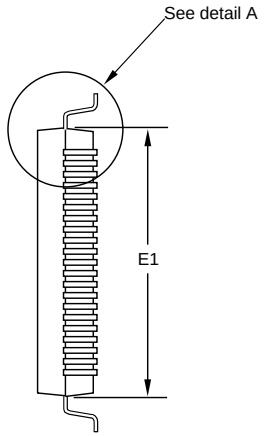
Ref: 144-PIN TQFP (GP00-D252)

* Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may include round-off errors.

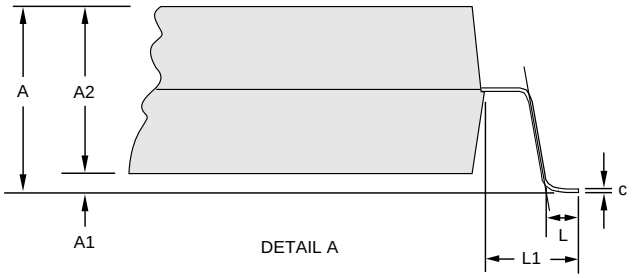
Figure 7-8. Package Dimensions - 144-Pin TQFP



TOP VIEW



SIDE VIEW



Dim.	Millimeters Min.	Millimeters Max.	Inches* Min.	Inches* Max.
A	2.4 MAX		0.0945 MAX	
A1	0.05	0.35	0.0020	0.0138
A2	2.0 REF		0.0787 REF	
D	22.95	23.45	0.9035	0.9232
D1	20.0 REF		0.7874 REF	
D2	18.85 REF		0.7421 REF	
E	16.95	17.45	0.6673	0.6870
E1	14.0 REF		0.5512 REF	
E2	12.35 REF		0.4862 REF	
L	0.73	1.03	0.0287	0.0406
L1	1.6 REF		0.0630 REF	
e	0.65 BSC		0.0256 BSC	
b	0.25	0.45	0.0098	0.0177
c	0.13	0.19	0.0051	0.0075
Coplanarity	0.10 MAX		0.004 MAX	
Ref: 100-PIN PQFP (GP00-D234)				

* Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may include round-off errors.

PD-PQFP-100 (040695)

Figure 7-9. Package Dimensions - 100-Pin PQFP

8. T.30 IMPLEMENTATION

8.1 GENERAL

ITU-T Recommendation T.30 details procedures for facsimile transmission over the PSTN. This standard describes how to initiate, complete, and end a fax transmission. This section describes methods to set up host software to implement T.30 with the modem.

A basic block diagram of a Group 3 facsimile machine is shown in Figure 8-1. The MDP performs the modulation/demodulation process. The fax machine manufacturer must implement the interface between the modem (T.30), the data compression/decompression (T.4), and the interface to the scanner and printer.

There are five phases (A-E) to the T.30 facsimile protocol. Phase A is the call setup, in which both facsimile machines connect to the line. Phase B is a pre-message procedure which consists of identification and command sections. The actual high speed message transmission occurs during Phase C. This is followed by the post-message procedure or Phase D. Both facsimile machines release the line in Phase E.

Figure 8-2 illustrates a typical Group 3 facsimile procedure. This example on T.30 describes a facsimile call where the calling unit (originate) transmits a documents to a called unit (answer). Phase E is not included in this example since it is the call release and both ends hang up.

Figure 8-3 through Figure 8-7 illustrate how to originate a fax call. Figure 8-8 through Figure 8-13 illustrate how to answer a fax call. Figure 8-14 through Figure 8-19 illustrate subroutines for originating or answering a fax call.

8.1.1 Phase A

T.30 specifies that call establishment can be realized one of four ways. The four methods of call establishment are: manual-to-manual, manual-to-automatic, automatic-to-manual, and automatic-to-automatic. Manual corresponds to operator or human intervention while automatic means machine only. The explanation that follows describes an automatic-to-automatic example.

After dialing, the calling unit, or originating fax, first transmits a calling tone (CNG) to indicate it is a non-speech terminal. The called unit, or answering fax, then responds with a called station ID (CED). The end of Phase A is signified after the called unit sends a 2100 Hz (CED) tone and the calling unit has detected this tone. Some facsimile manufacturers do not configure the MDP to detect these tones. In this case, the MDP looks for the preamble of flags (see phase B).

8.1.2 Phase B

The pre-message procedure consists of the following handshake. The answering fax machine sends an identification signal and the originating machine responds with a command signal. A training check is sent at a high speed and the receiving machine informs the transmitting machine if the training check was successful. This usually occurs at V.21 300 bps Frequency Shift Keying (FSK) modulation in HDLC format.

HDLC stands for High level Data Link Control. It is a standard procedure used for data communications. HDLC is a bit-oriented protocol (normally used in synchronous communications) that defines how the data being sent over the data link is organized and arranged.

When using the HDLC protocol, the data is transmitted via frames. These frames organize the data into a format specified by an ISO (International Standards Organization) standard that enables the transmitting and receiving station to synchronize with each other. Figure 8-20 illustrates the HDLC frame structure used for the facsimile protocol.

The preamble is a series of HDLC Flags for one second ±15%. The purpose of the 7E flags is to condition the line. The flag sequence defines the beginning and ending of a frame. The address field is required to provide identification for multi-point addressing. For PSTN the format is 11111111. The control field's purpose is to provide the capability of encoding the commands and responses. The format is 1100X000 (X = 0 non-final frame; X = 1 final frame).

The HDLC information field provides the specific information for the control and message interchange between the two stations. In the fax protocol the format for the information field consists of two parts, the Facsimile Control Field (FCF) and the Facsimile Information Field (FIF).

The FCF contains information regarding the type of information being exchanged and the position in the overall sequence. The acronyms, functions, and format for FCF commands are defined in the T.30 Recommendation. The FIF contains additional information which further clarifies the facsimile procedure. Some examples of information communicated with the FIF are: group capability, data rate, vertical resolution, coding scheme, recording width, recording length, and minimum scan line time.

The Frame Check Sequence (FCS) follows the FIF. The MDP automatically generate the FCS or Cyclic Redundancy Check (CRC). The frame ends with an ending 7E flag. It is recommended that more than one ending flag be transmitted.

After the MDP has been configured for FSK, the Digital Identification Signal (DIS) is transmitted by the called unit. The DIS informs the calling unit about the called unit's capabilities such as group capability (G1, G2, G3), data rate, vertical

resolution, coding scheme (Modified Huffman, Modified Read), recording width, recording length, and minimum scan line time. The calling unit then responds with a Digital Command Signal (DCS) which informs the called unit which options are chosen to complete this facsimile call.

After the DCS is transmitted, both the calling unit and the called unit set up for the high speed configuration that was chosen and transmitted via the DCS. A Training Check (TCF) is transmitted by the calling unit to verify training and give an indication of channel acceptability for the selected data rate. The TCF consists of a series of zeros for 1.5 seconds ±10%. Since the called unit knows it will be receiving 1.5 seconds of zeros, the host can make a decision whether the line is good enough at the chosen data rate or fallback to a slower speed.

After completing the TCF, the calling unit and the called unit re-configure for FSK, HDLC format. The called unit then transmits either a Confirmation to Receive (CFR) or a Failure To Train (FTT). The CFR is a response informing the calling unit of a successful pre-message procedure completion. A FTT informs the calling unit that the training signal was rejected and requests re-training. If a FTT is received by the calling unit, the fax protocol jumps back to the transition of DCS and continues until finally a CFR is received or the calling unit host decides to terminate the call.

8.1.3 Phase C

Phase C occurs after both facsimile machines have set up for the high speed configuration that was decided upon in phase B. The T.30 Error Correction Mode is addressed in a following section. The high speed message information is usually compressed data using a Modified Huffman (MH) or Modified Read (MR) algorithm. The host processor must perform the MH or MR compression before loading the data into the MDP. On the receive end, the host processor must perform the MH or MR decompression.

The start of phase C is denoted by an End Of Line (EOL) 8-bit code. The data follows this first EOL character until the end of the line. Another EOL character is transmitted to indicate a new line. A minimum transmission time of a total coded scan line is measured from the beginning of the EOL to the beginning of the following EOL. If the transmitted data requires less time than the minimum transmission time, fill bits must be transmitted. Six consecutive EOL character constitute a Return To Control (RTC) command meaning end of document transmission. Figure 8-21 illustrates the phase C format.

8.1.4 Phase D

The post-message phase D procedure uses FSK and HDLC format. The calling station will typically send an End Of Message (EOM) signal. This FCF command (EOM) informs the called station that this is the end of the page and return to Phase B. A Multi-Page Signaling (MPS) or End Of Procedure (EOP) signal may be sent instead of EOM. The MPS signal informs the called unit that there are more pages in this facsimile transmission. EOP signals the end of the facsimile transmission. Procedure Interrupt-EOM (PRI-EOM), Procedure Interrupt-MPS (PRI-MPS), and Procedure Interrupt-EOP (PRI-EOP) indicate the same as EOM, MPS, and EOP, respectively, with the additional optional capability of requesting operator intervention. If operator intervention is required, further facsimile procedures commence at the beginning of phase B.

The called station might respond to an EOM, MPS, or EOP signal with a Message Confirmation (MCF) command. This FCF command indicates to the calling unit that the complete message was received. One of the following FCF commands may be sent instead of the MCF: Re-Train Positive (RTP), Re-Train Negative (RTN), Procedure Interrupt Positive (PIP), or Procedure Interrupt Negative (PIN). RTP indicates that a complete message has been received and that additional messages may follow after retransmission of TCF and CFR. RTN indicates that the previous message has not been satisfactorily received, however, further receptions may be possible provided there is a retransmission of TCF and CFR. PIP and PIN indicate that the previous message was received satisfactorily or not satisfactorily, respectively, and operator intervention is required for further transmissions.

8.1.5 Phase E

Call Release, or phase E, occurs after the last post-message signal of the procedure or under certain conditions such as a time-out, procedural interrupt, or a Disconnect (DCN) command.

The DCN command indicates the initiation of phase E. This command requires no response.

8.2 ERROR CORRECTION MODE

8.2.1 General

The revised T.30 contains an Error Correction Mode (ECM) option. The ECM allows the phase C portion of the facsimile transmission to be encoded in a HDLC framing format using a specified number of bits in the information field. The transmitted high speed message is broken up into a number of frames identified by frame numbers. If an error is detected during reception of the message, the called station records the frame number. After all the frames in the message has been received, the called station transmits the frame numbers that were received in error. The calling station then re-transmits only those frames in error. This continues until the entire message is received error free or the calling station decides not to transmit any more frames.

The error detection is performed by comparing the CRC or FCS. Using ECM, the fax data rate can be as fast as 14400 bps, therefore, the host microprocessor may not be able to keep up if implementing HDLC without the use of a serial I/O device.

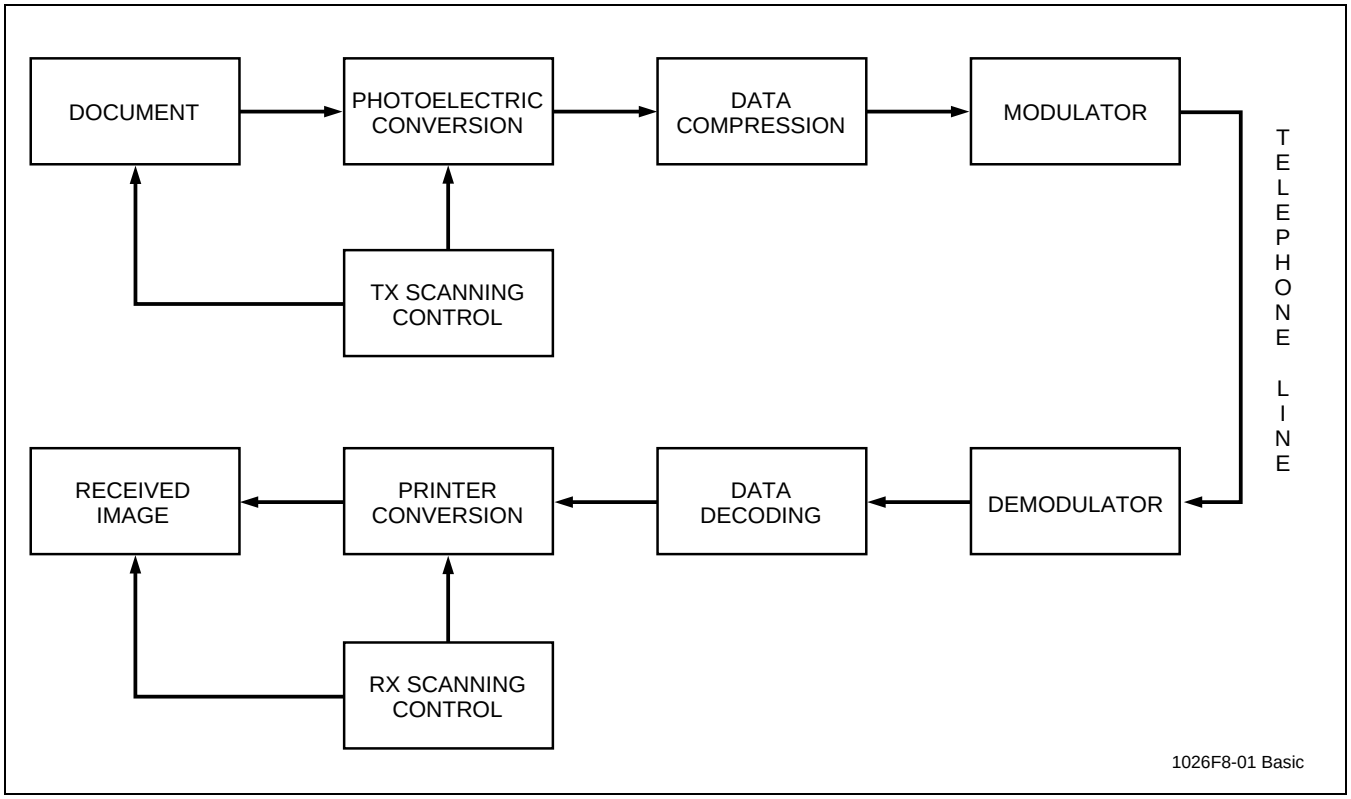


Figure 8-1. Basic Block Diagram of G3 Facsimile

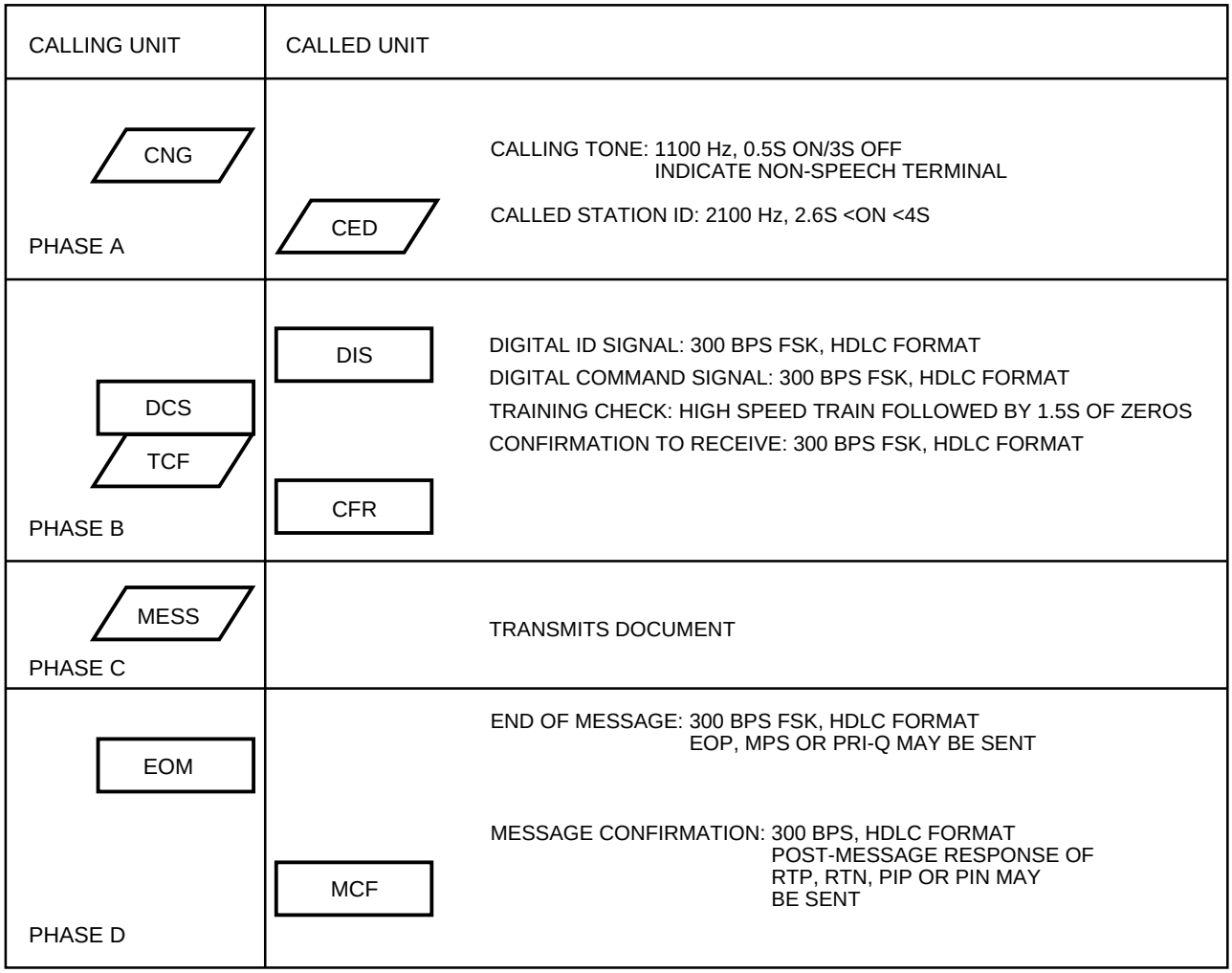


Figure 8-2. G3 Facsimile Procedure

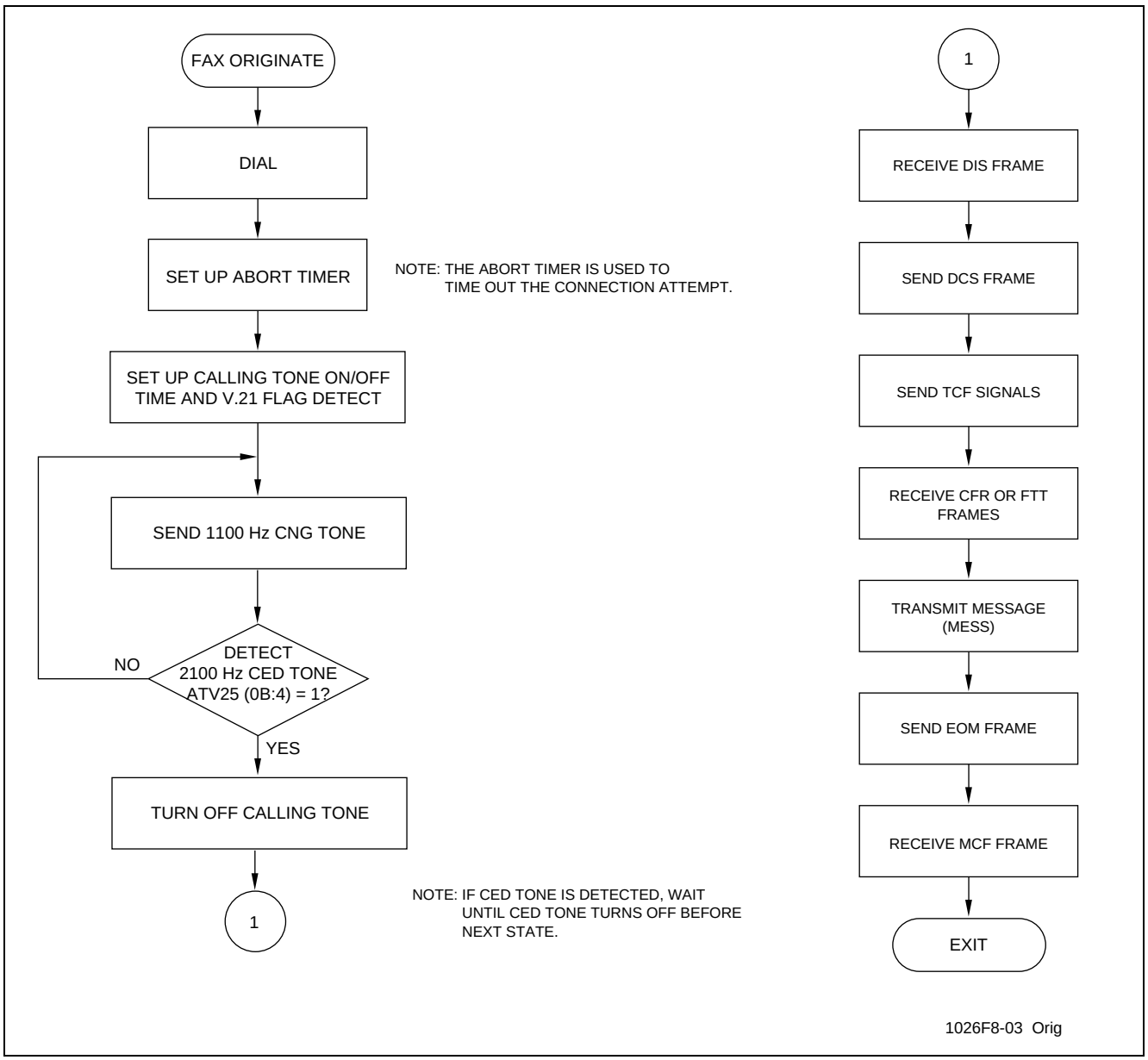


Figure 8-3. Originating a Fax Call - General

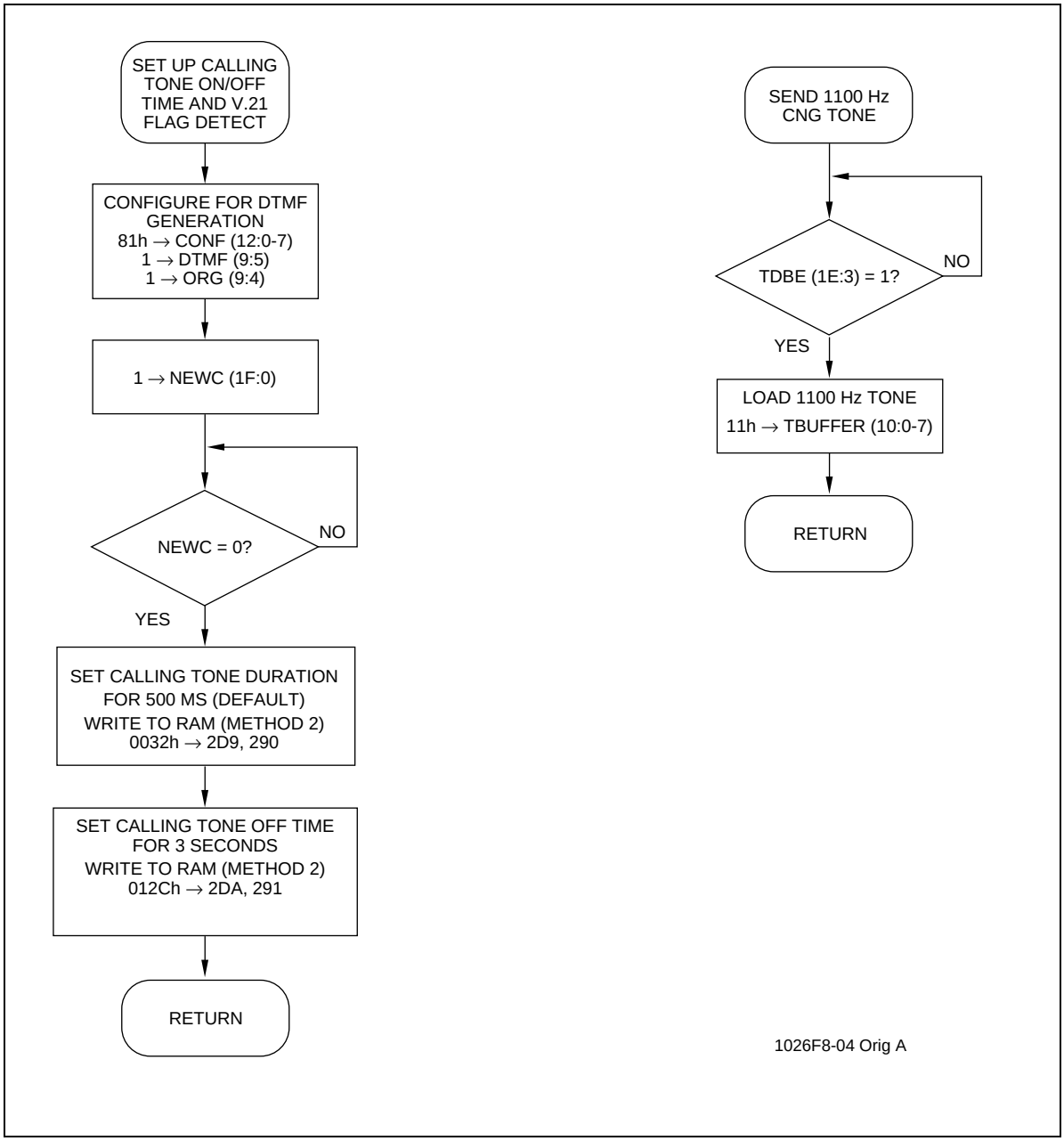


Figure 8-4. Originating a Fax Call - Phase A

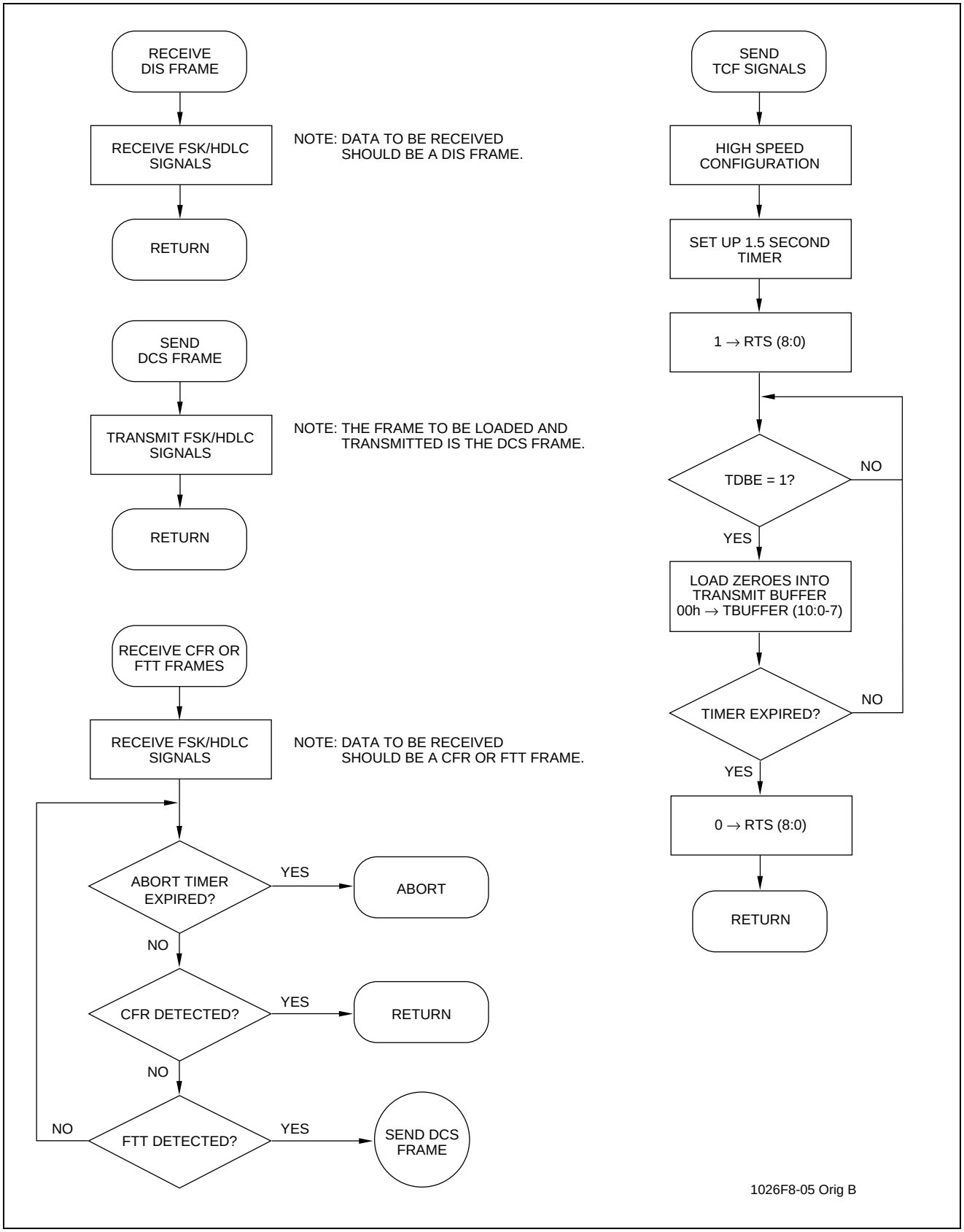


Figure 8-5. Originating a Fax Call - Phase B

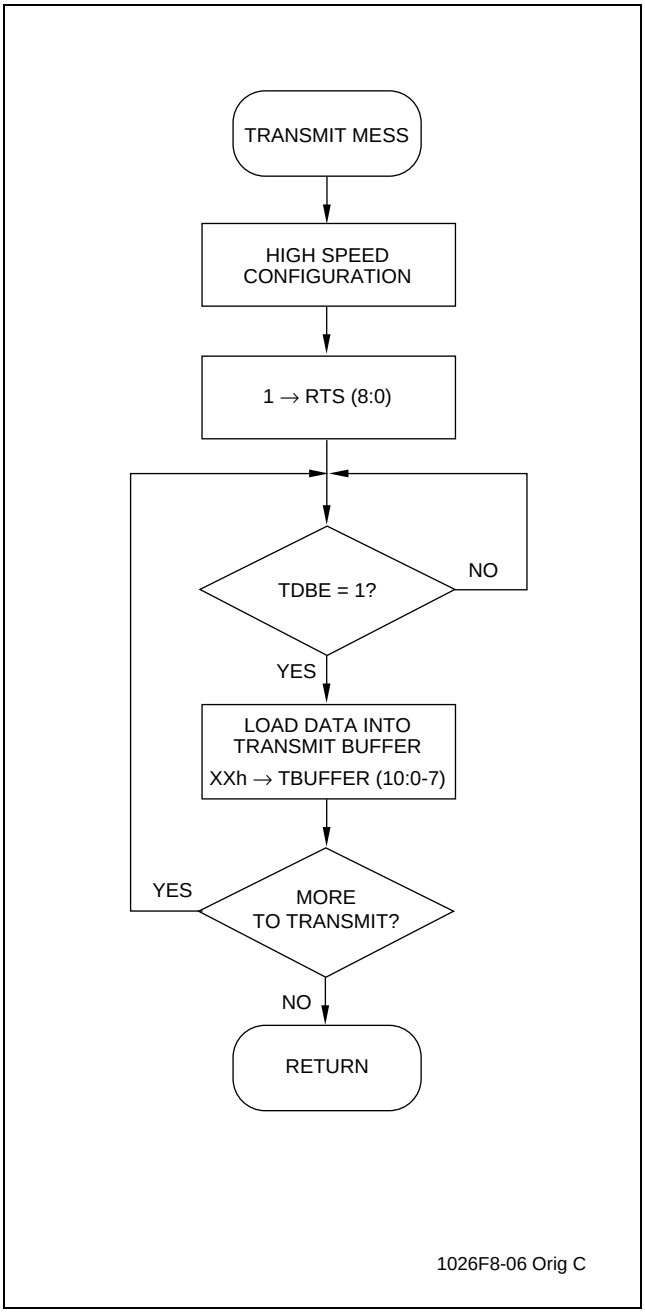


Figure 8-6. Originating a Fax Call - Phase C

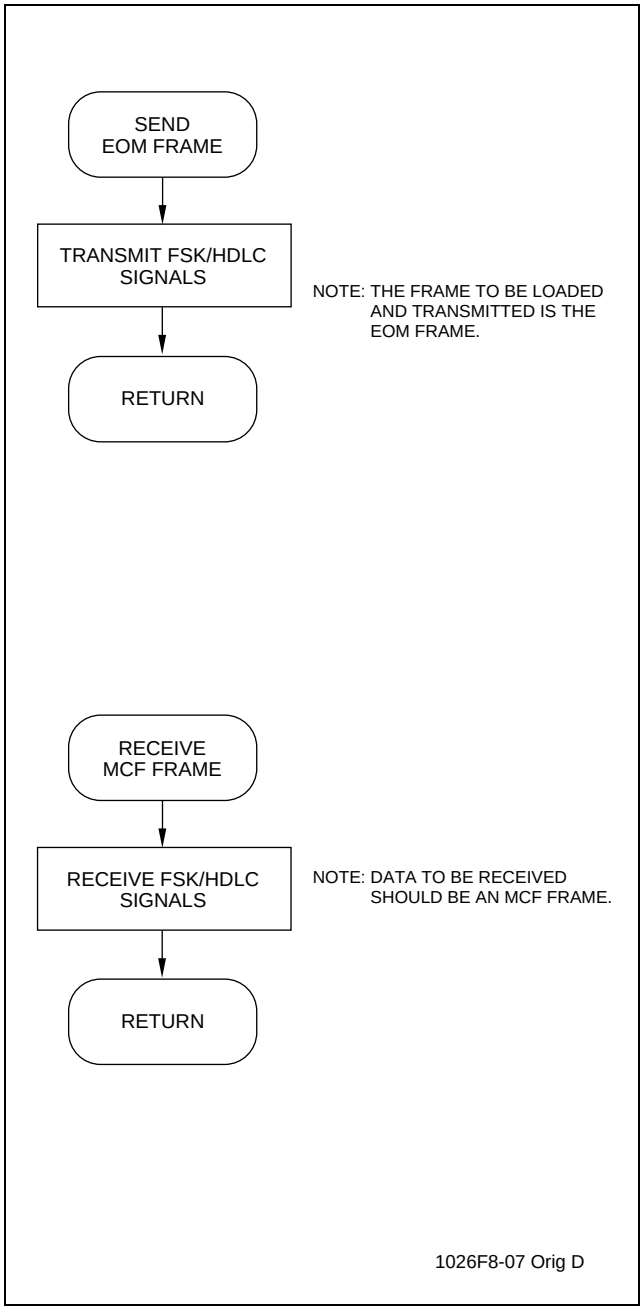


Figure 8-7. Originating a Fax Call - Phase D

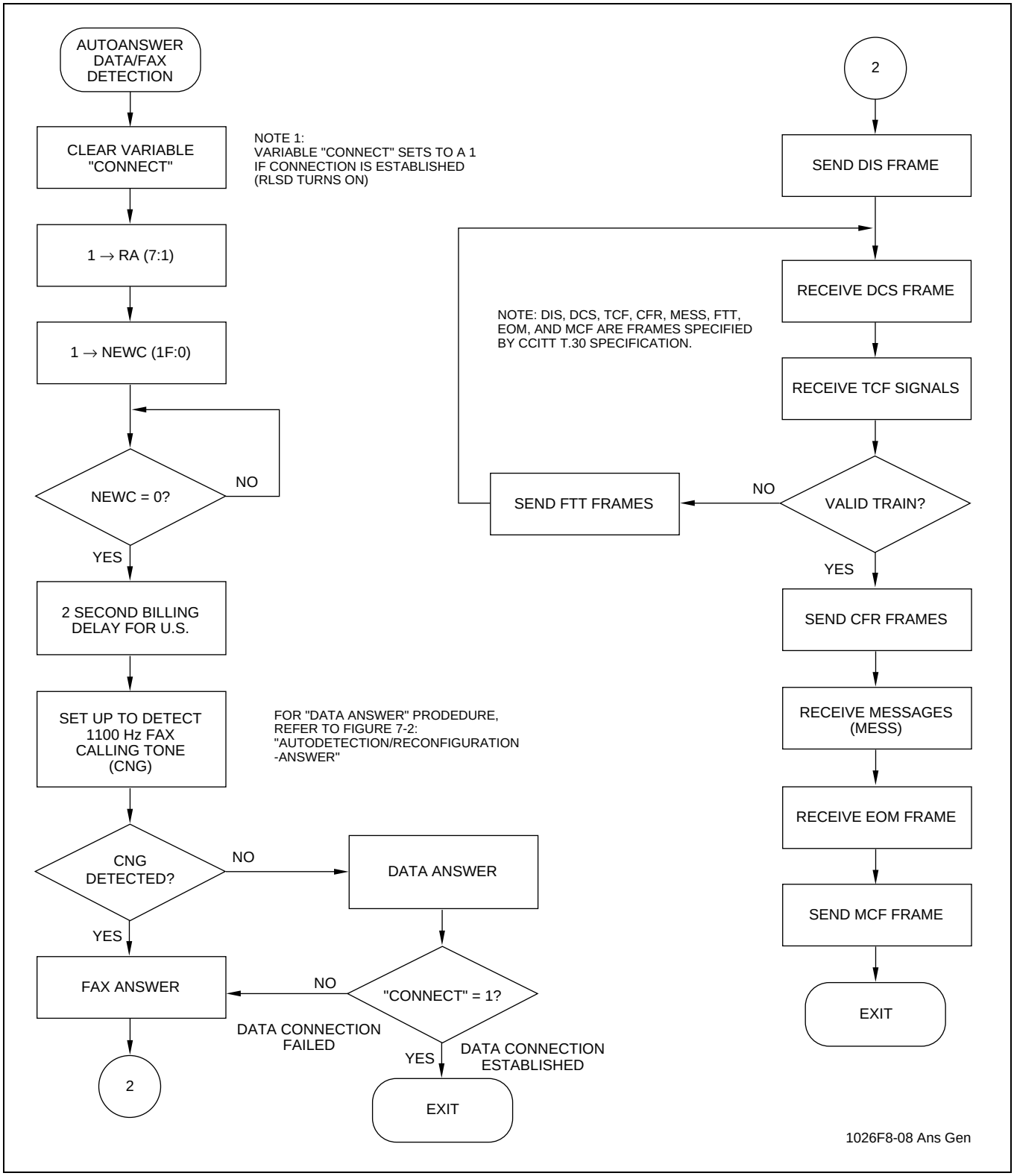


Figure 8-8. Answering a Fax Call - General

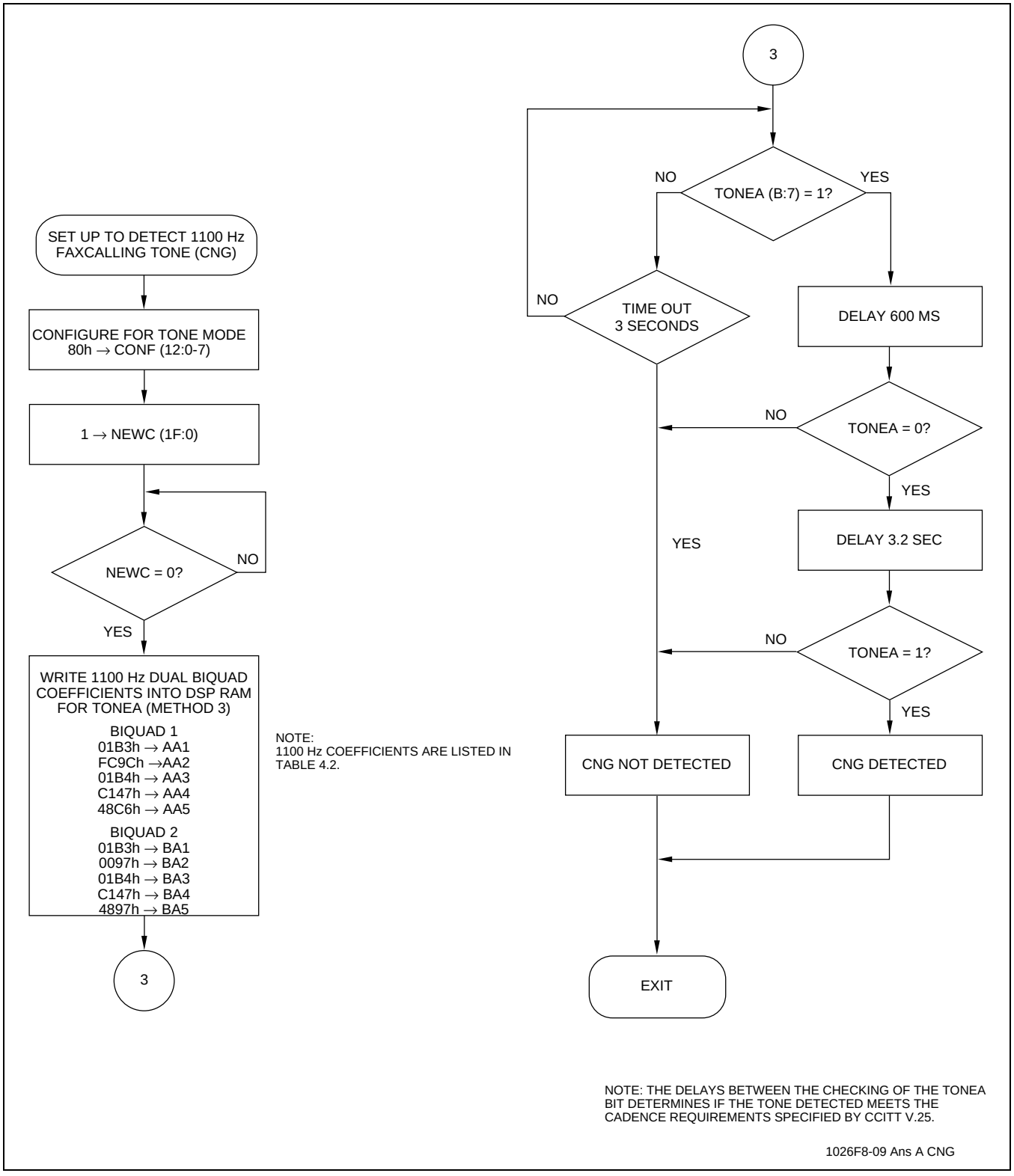


Figure 8-9. Answering a Fax Call - Phase A (CNG)

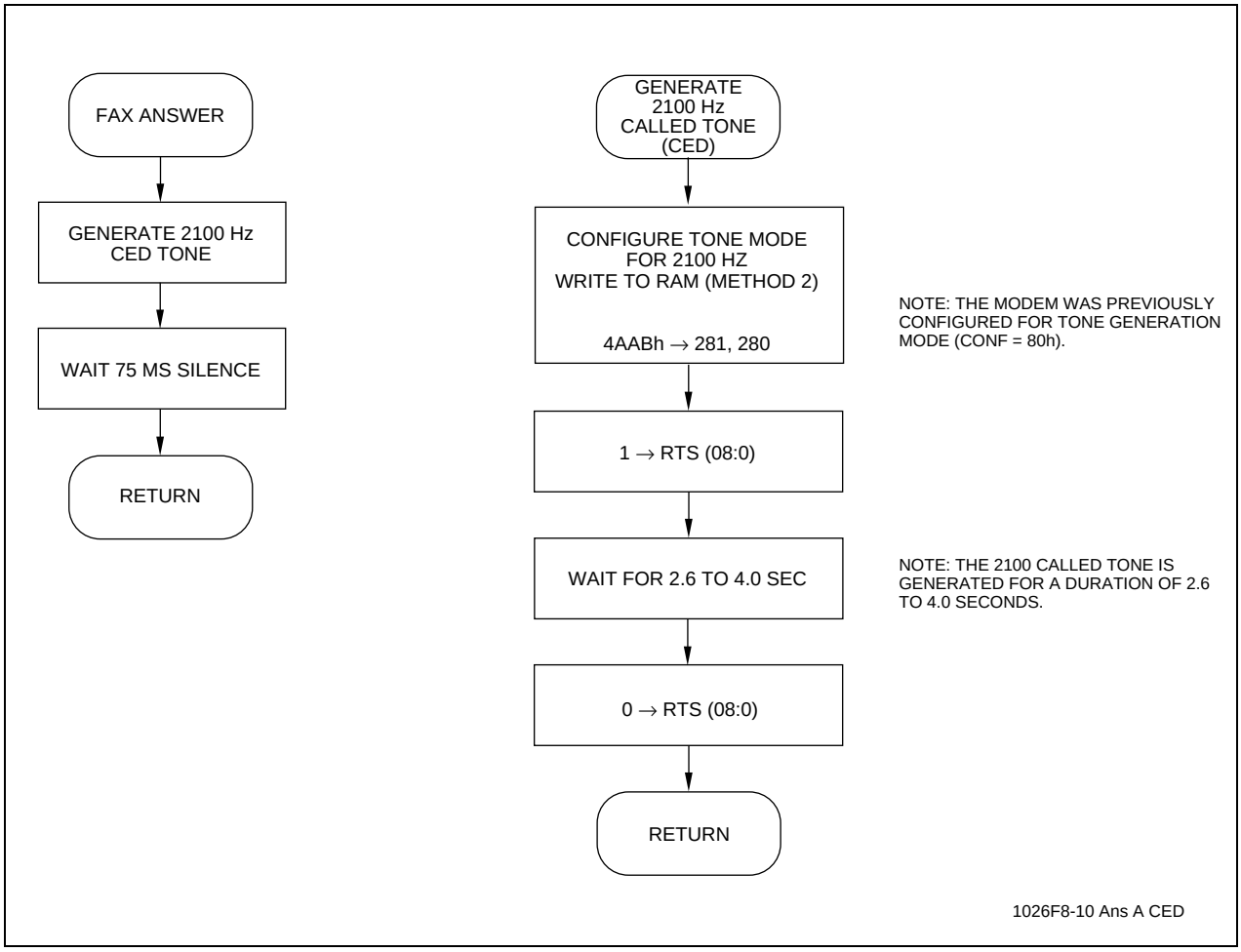


Figure 8-10. Answering a Fax Call - Phase A (CED)

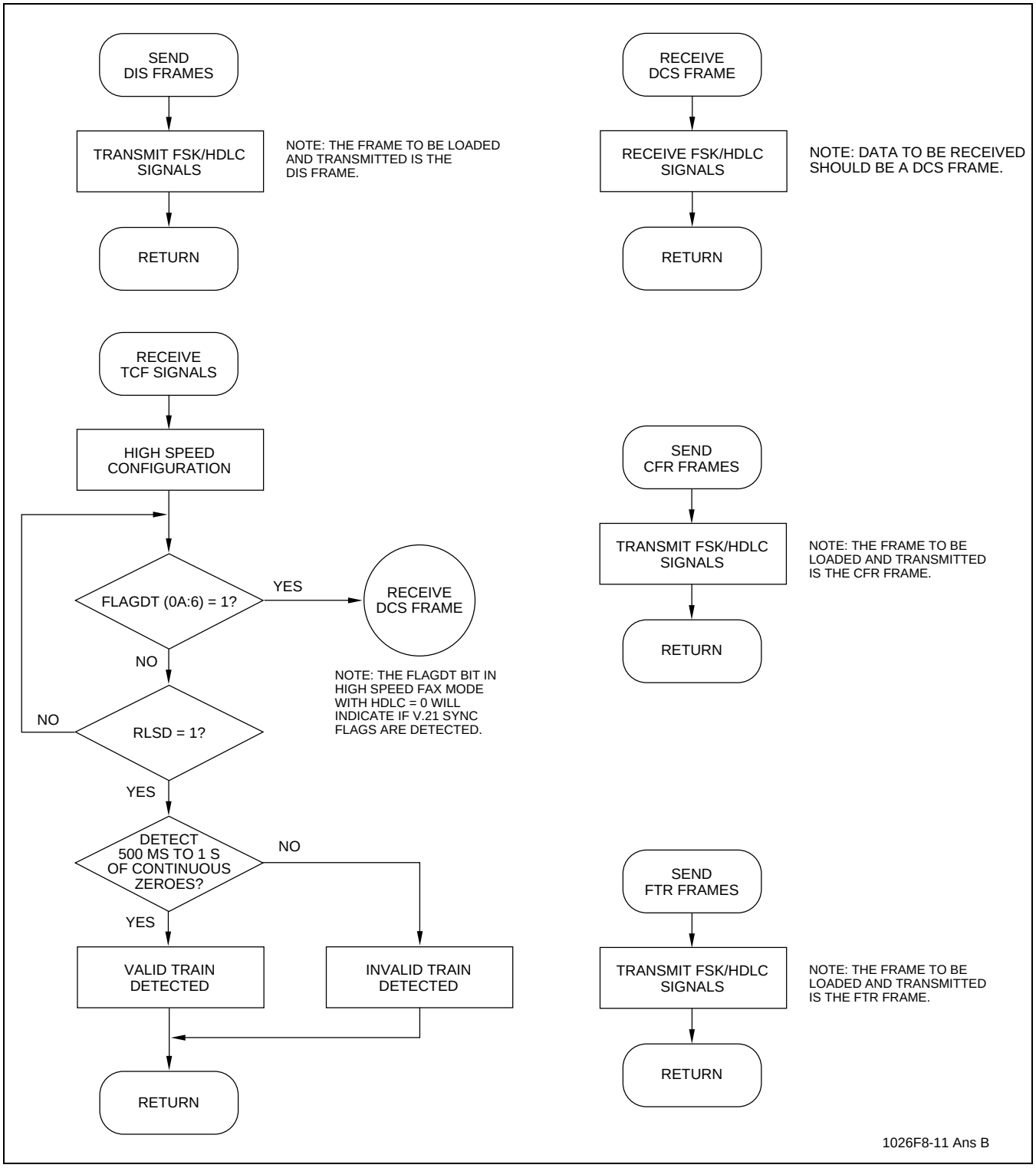


Figure 8-11. Answering a Fax Call - Phase B

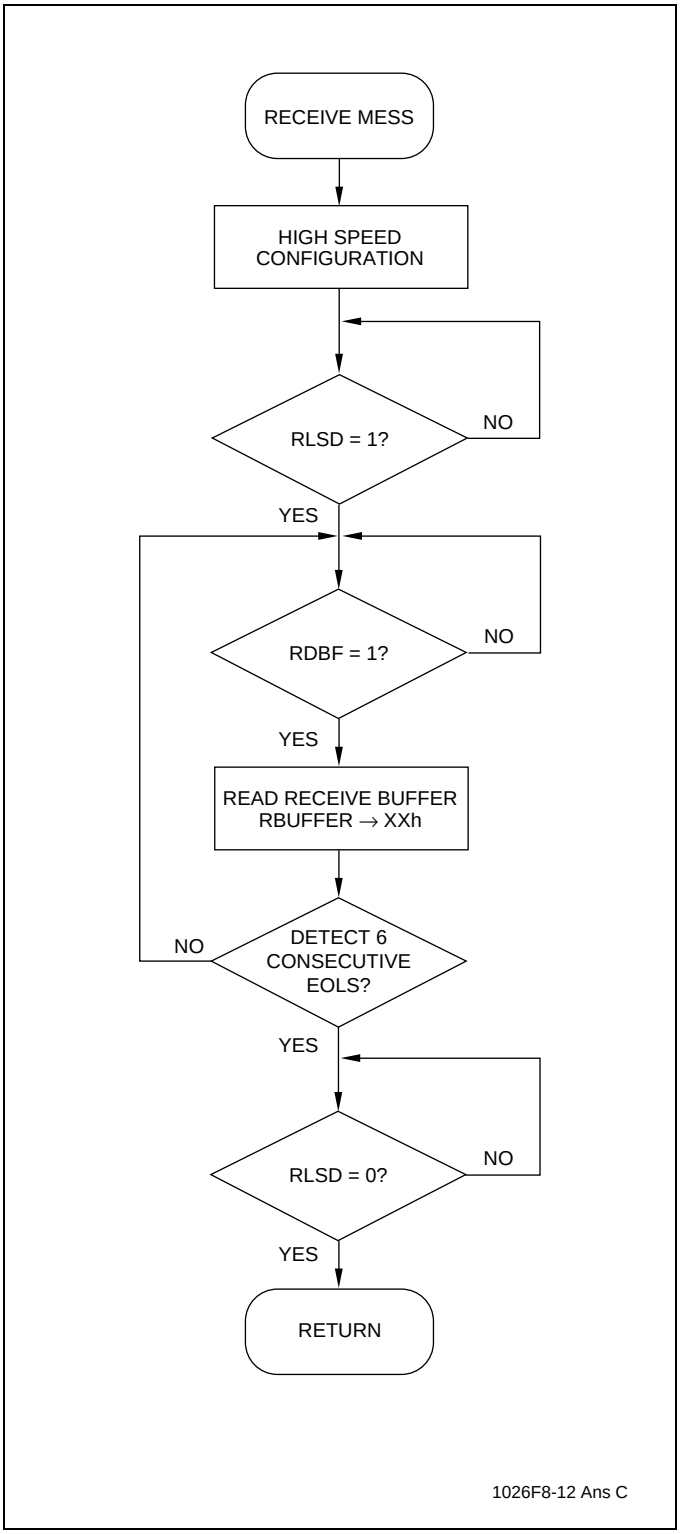


Figure 8-12. Answering a Fax Call - Phase C

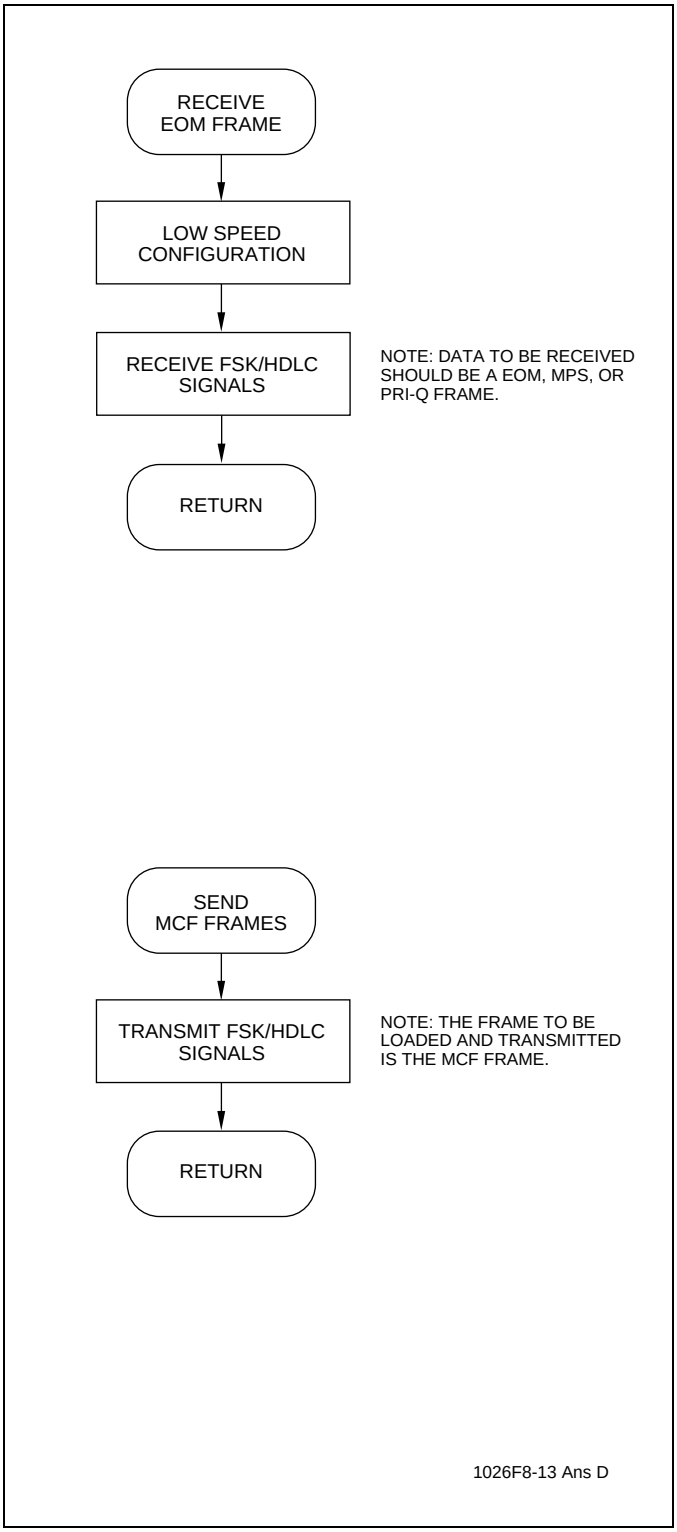


Figure 8-13. Answering a Fax Call - Phase D

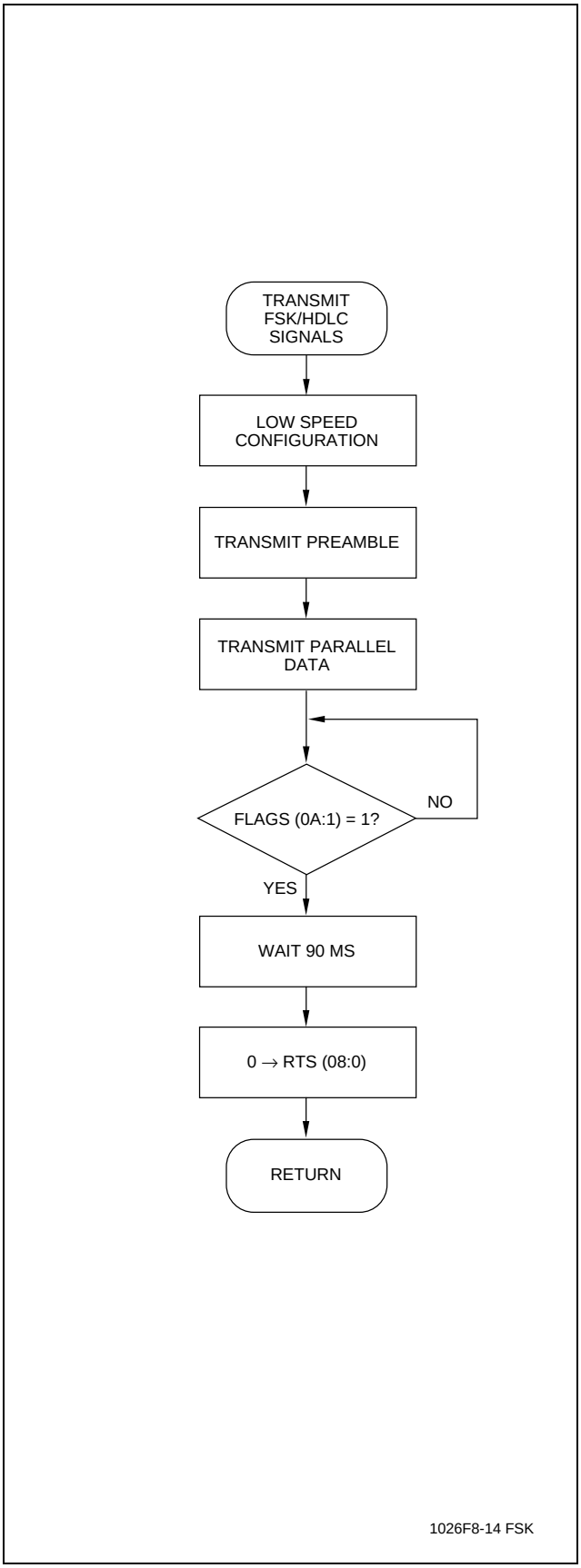


Figure 8-14. Transmitting FSK/HDLC Signals

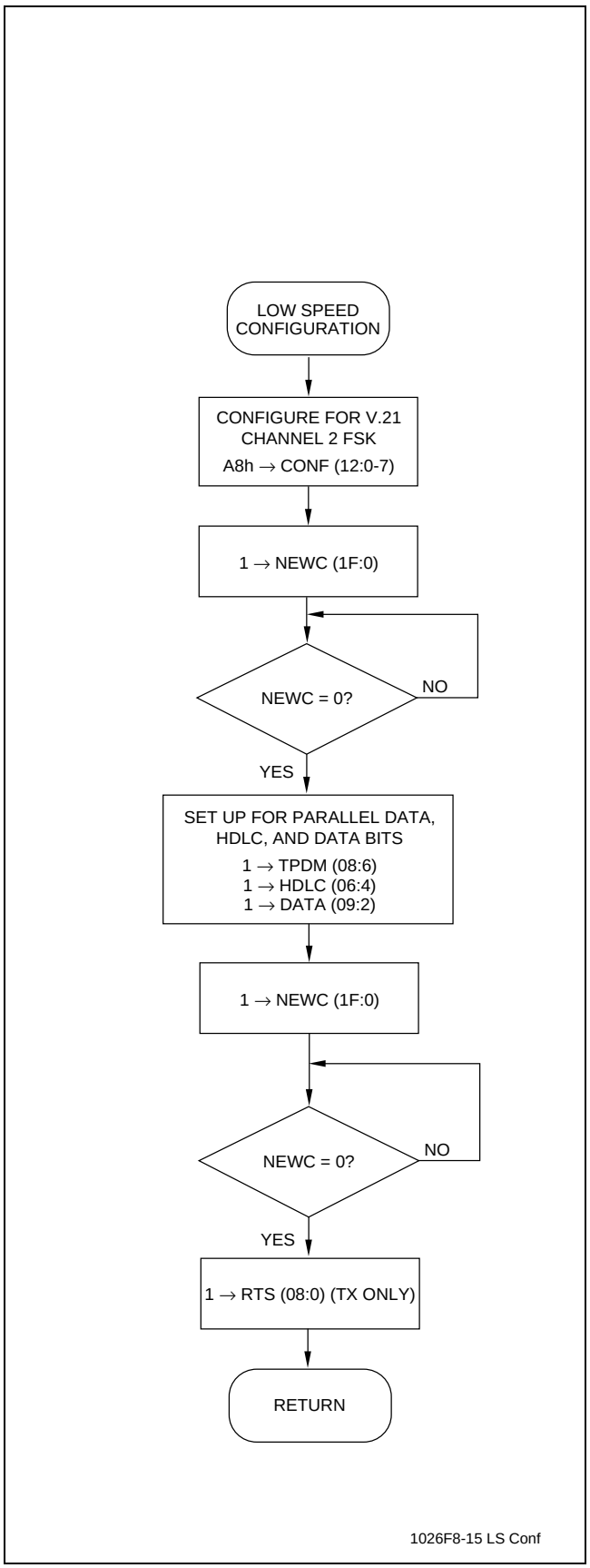


Figure 8-15. Low Speed Configuration Routine

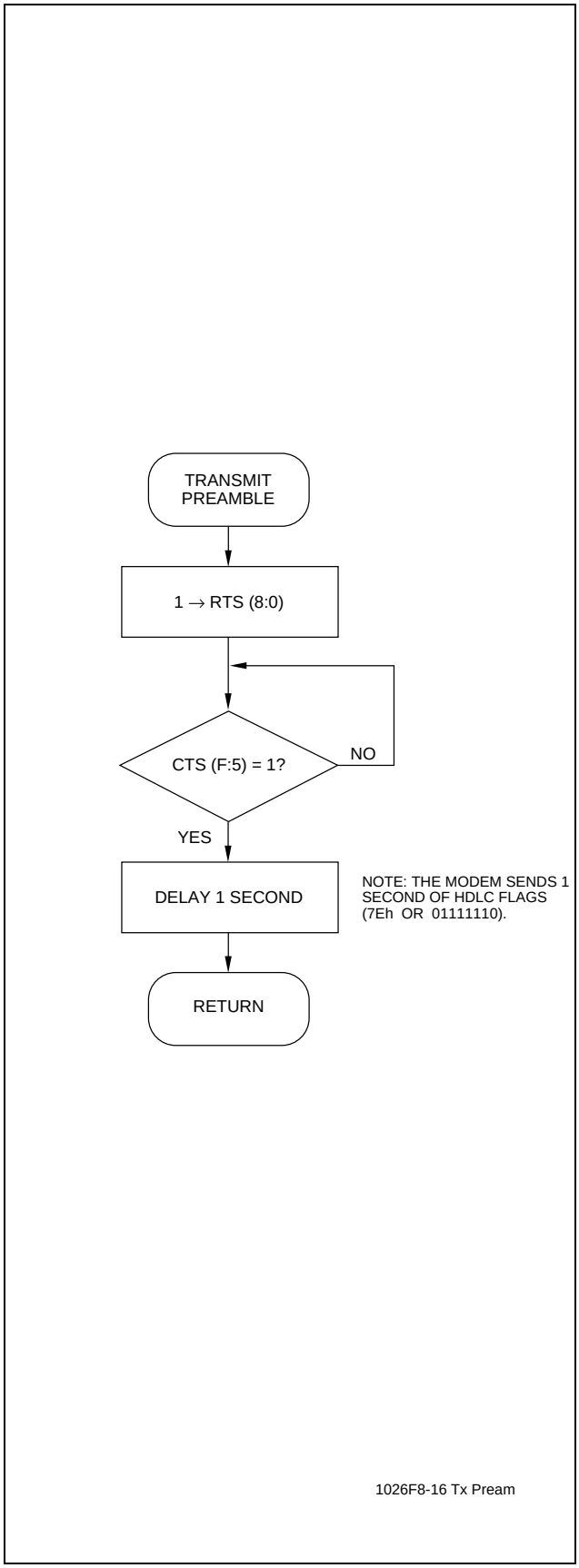


Figure 8-16. Transmit Preamble Routine

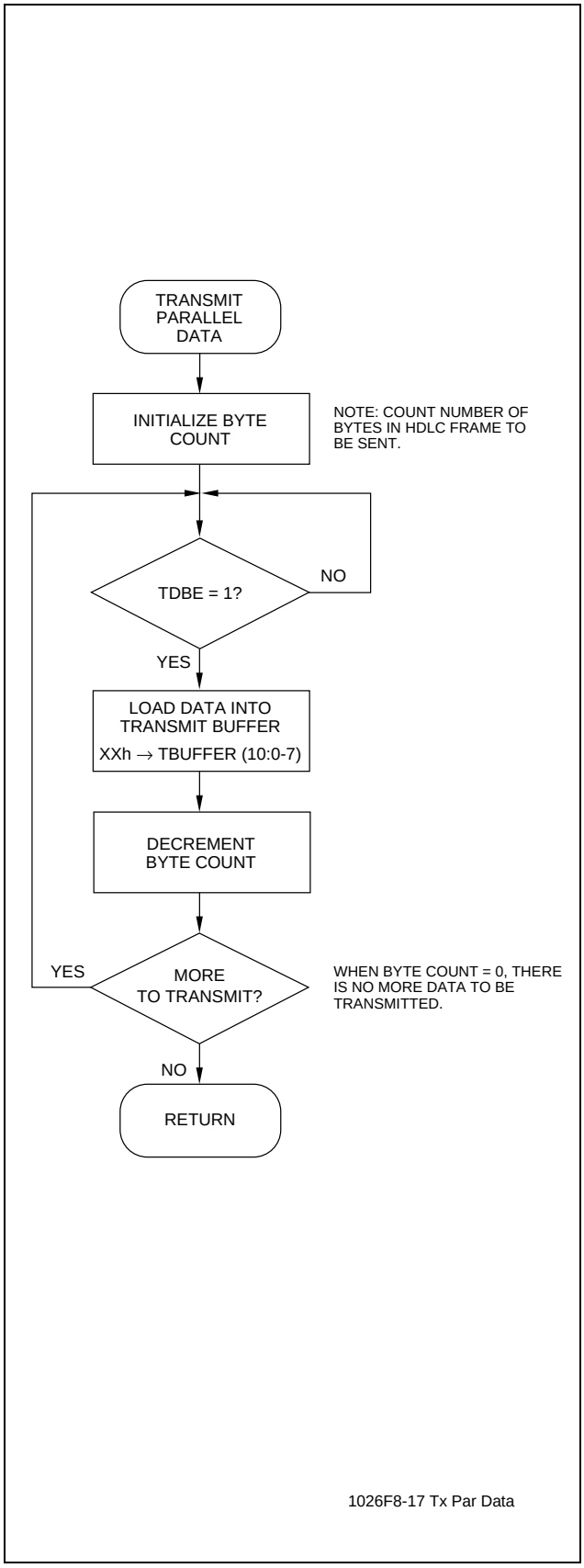


Figure 8-17. Transmit Parallel Data Routine

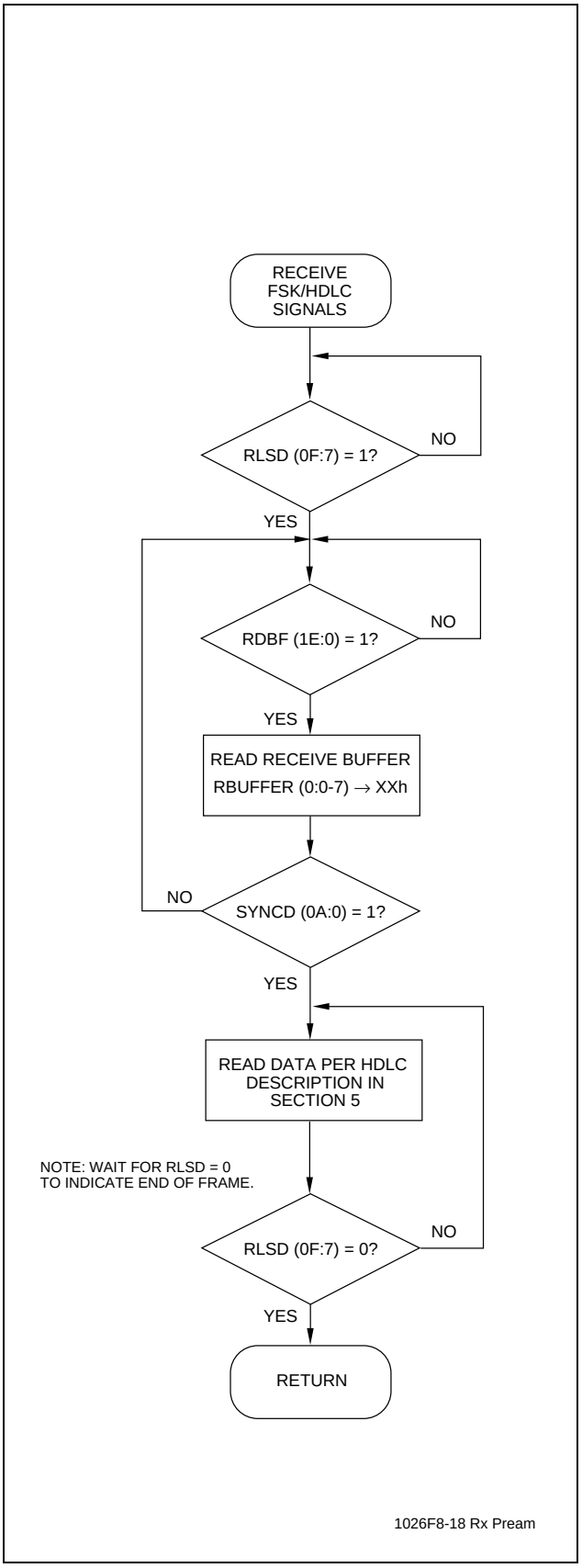


Figure 8-18. Receive FSK/HDLC Signals

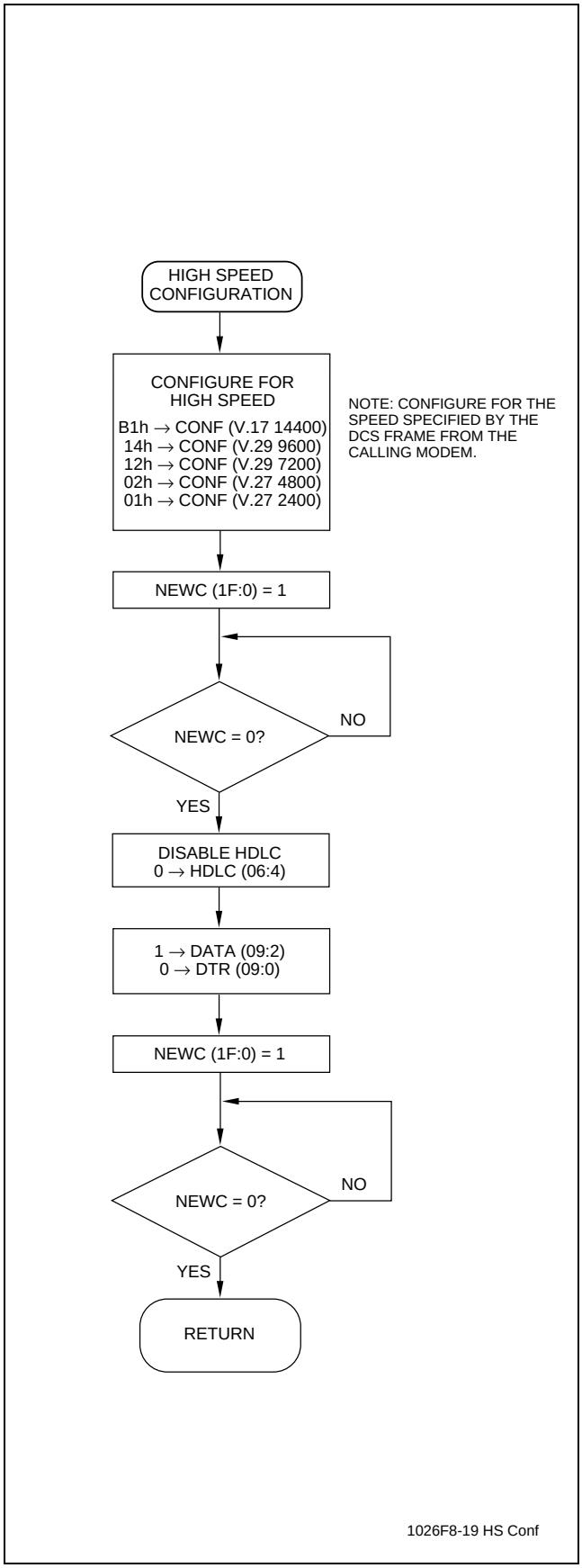


Figure 8-19. High Speed Configuration Routine

8.2.2 ECM Frame Structure

In Error Correction Mode, one frame of facsimile data consists of 256 or 64 octets of data. Each page may contain 1 to 256 frames. Also, 1 to 256 pages may be transmitted. The ECM frame structure is illustrated in Figure 8-22. Following the high speed training sequence, the flag, address field, and control field is transmitted. In ECM, Flag = 7E, Address = FF, and Control = B0. The Facsimile Control Field for the Facsimile Coded Data block (FCD) is 60. The frame number follows the FCF for FCD, followed by the facsimile data. Pad bits such as EOL, Tag, and Align bits follow the facsimile data. Finally, the FCS check and the ending flag is transmitted.

After 256 frames, a Return Control for Partial page (RCP) block is transmitted three times. The RCP block consists of the same Flag, Address Field, and Control field followed by the FCF for RCP. The FCS immediately follows with the ending flag. After the third RCP, a maximum of 50 ms of flags are transmitted.

An ECM message protocol example is shown in Figure 8-23. The bold arrows are high speed transmissions and the other arrows are FSK transmissions. The example is self-explanatory. If more information is needed, refer to the T.30 ECM specification.

In this paragraph, the Q refers to the NULL, EOP, MPS, or EOM Facsimile Control Field commands. The Partial Page Signals (PPS-Q) and Partial Page Request (PPR) frame structures are shown in Figure 8-24. The PPS-Q frame begins with the same Flag, Address field, and Control field. Two FCF commands follow. The first FCF transmitted is to indicate PPS. The second FCF is either NULL, EOP, MPS, or EOM. The page count followed by the block count, followed by the total number of frames in the block are transmitted next. The FCS and ending flag are finally transmitted.

The PPR frame structure also begins with the same Flag, Address, and Control field. The FCF for PPR is the next octet. The FIF consists of 256 or 64 bits depending on how many frames were transmitted. The contents of FIF is either a 0 or a 1. The bit number corresponds to the frame number and a 0 indicates the frames was received correctly and a 1 indicates an incorrect frame was received.

8.3 SIGNAL RECOGNITION ALGORITHM

A method of determining whether a high speed message or FSK handshaking is being received by the MDP is necessary when implementing the T.30 recommendation. When the calling unit transmitter and called unit receiver configure for V.29 or V.27 ter, sometimes the high speed message may not be received (typically due to a noisy line). In this case, the calling unit transmitter will try to send the message up to three times before re-negotiating in FSK signaling. The called unit receiver must, therefore, be able to distinguish between a high speed message and FSK handshaking.

The algorithm shown in Figure 8-25 can be used to perform the signal recognition. The use of the P2DET and PNDET status bits may also be incorporated for qualifying high speed PSK carrier.

High speed PSK reception in high noise environments can be optimized by setting the RTH bits so that the level of the noise is below the MDP's receiver threshold. This can be accomplished by measuring the received signal level via the AGC gain word RAM access while receiving the V.21 channel 2 carrier. Then, after configuring to a high speed configuration, RTH should be set to a value which will provide a threshold range centered around the expected receive level.

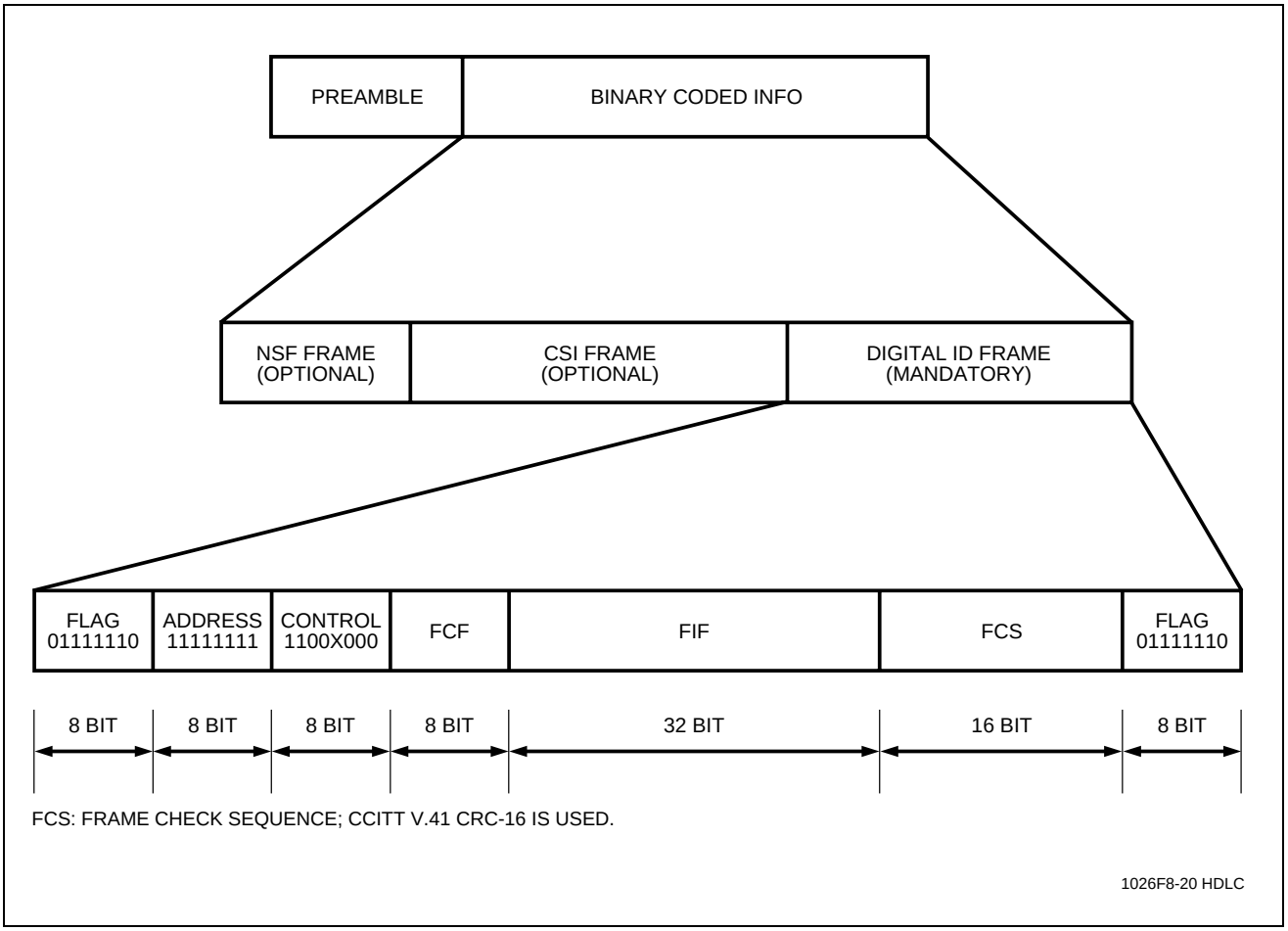


Figure 8-20. HDLC Frame Structure

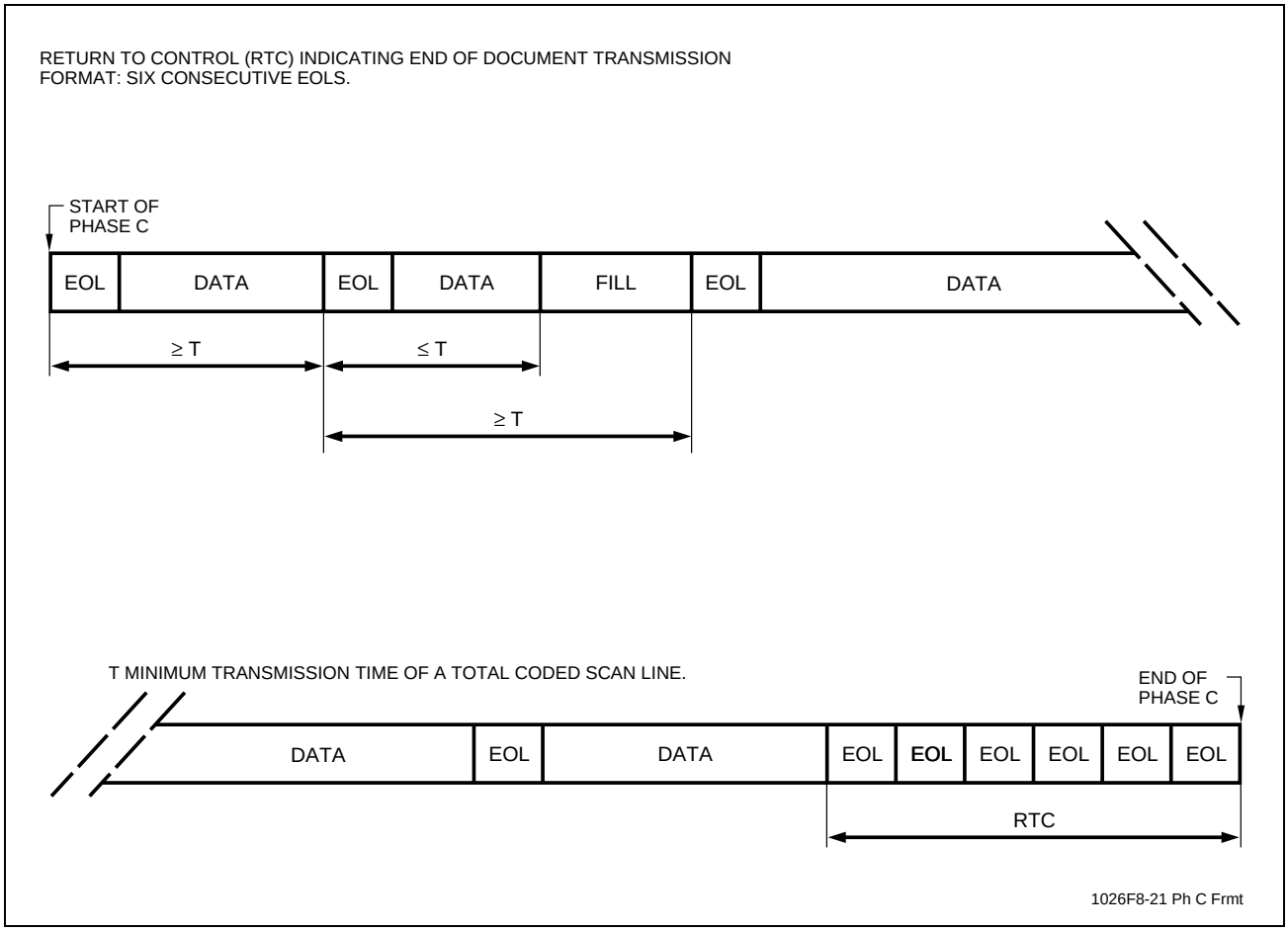


Figure 8-21. Phase C Format

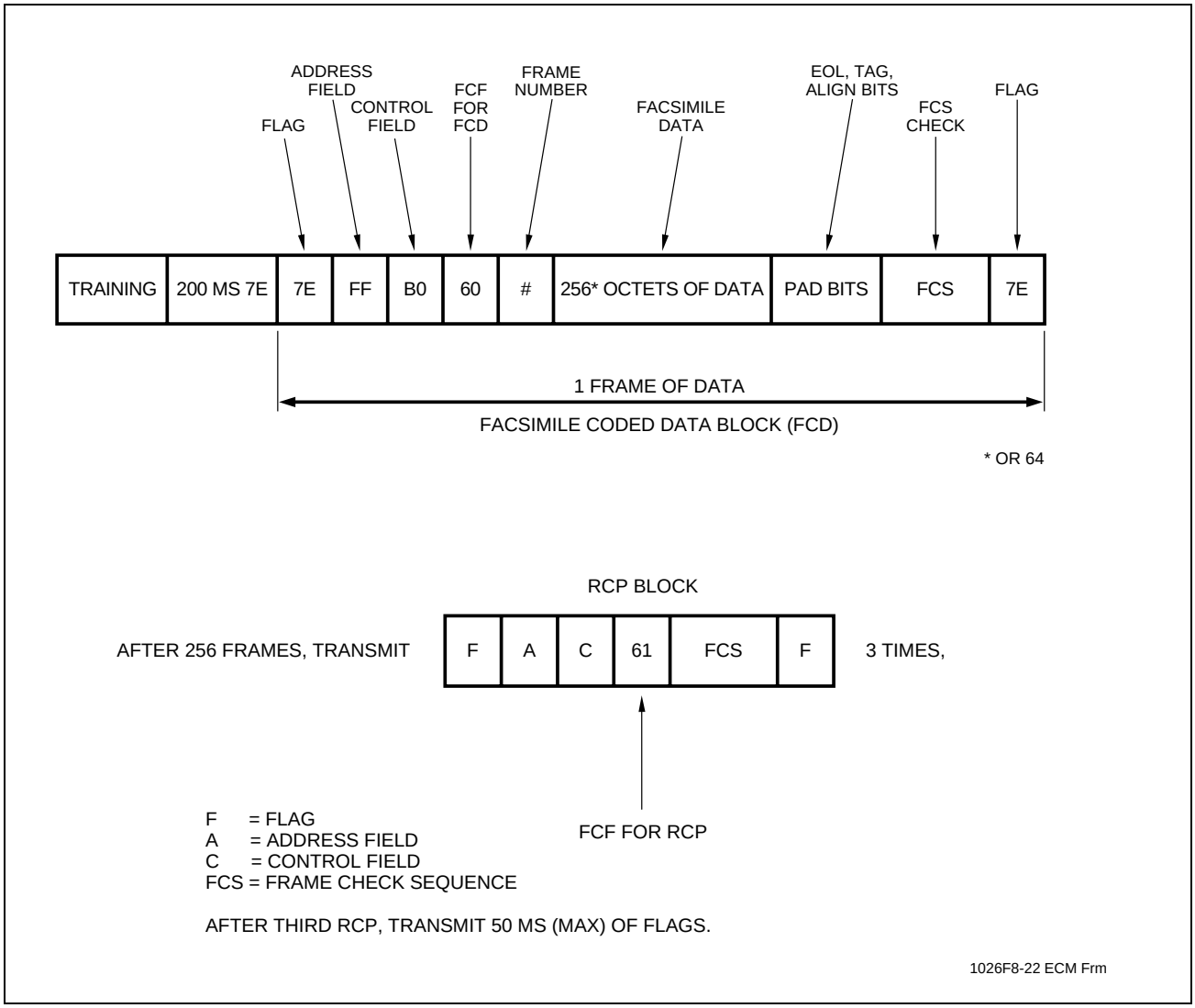


Figure 8-22. ECM Frame Structure

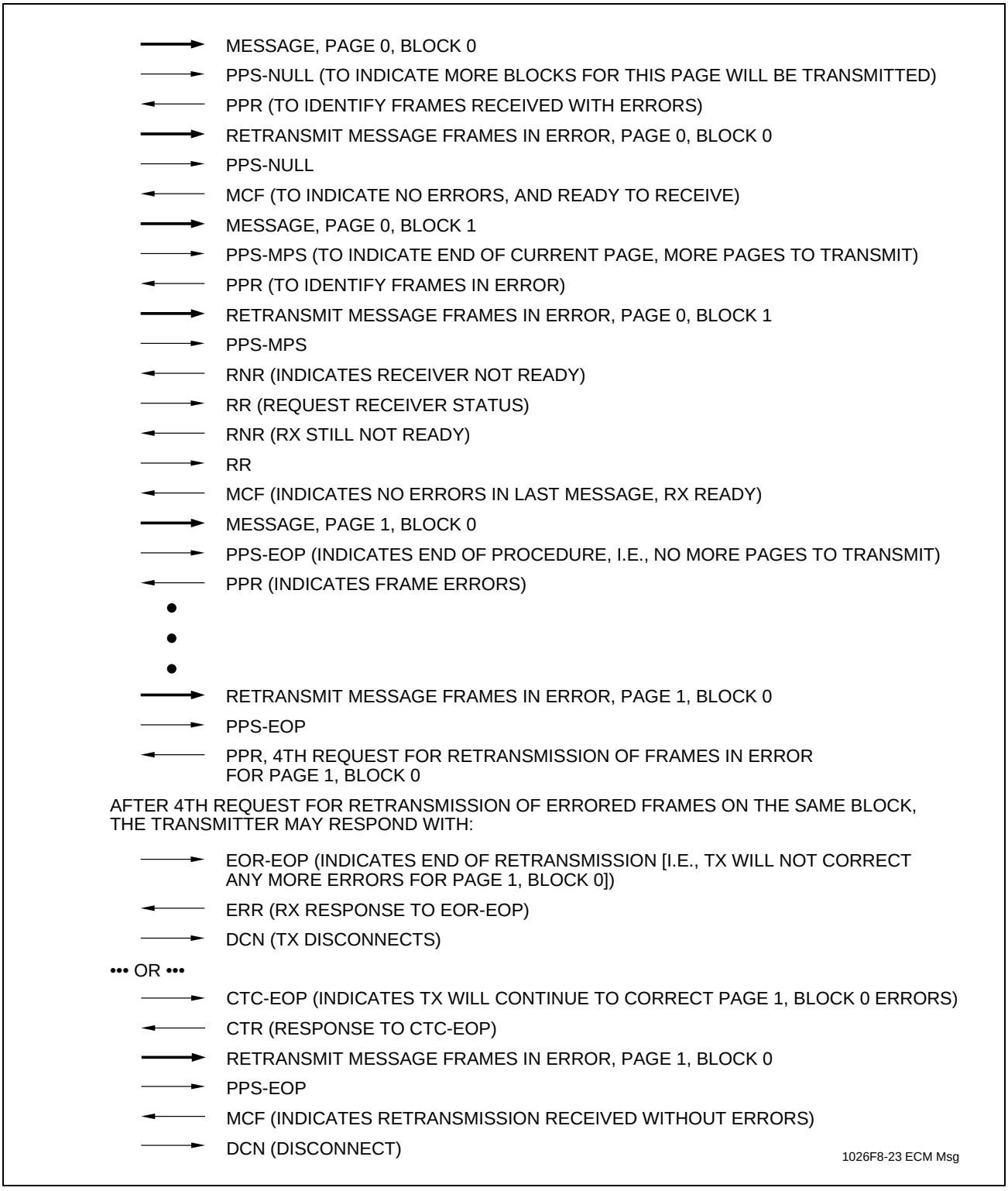


Figure 8-23. ECM Message Protocol Example

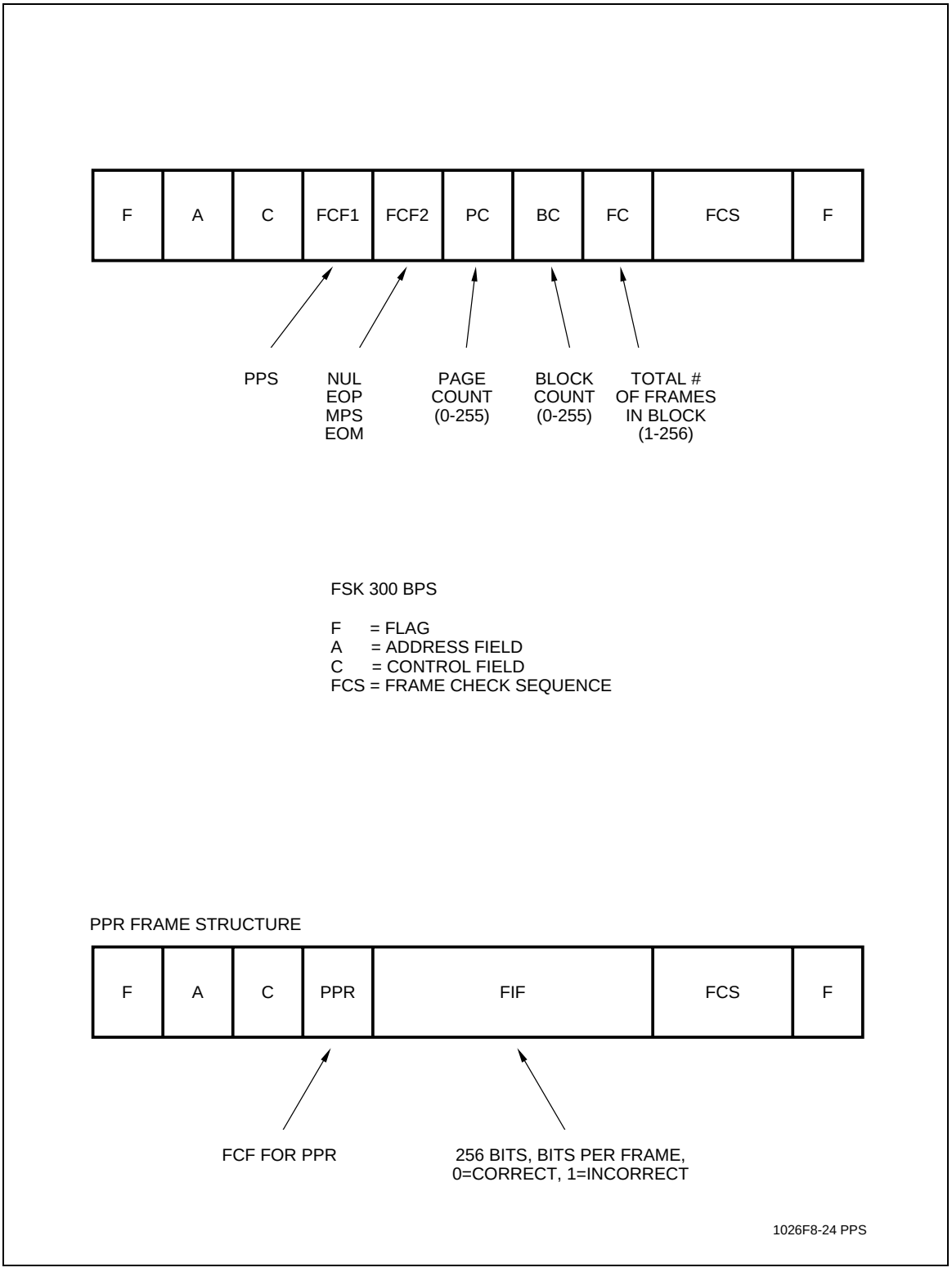


Figure 8-24. PPS and PPR Frame Structure

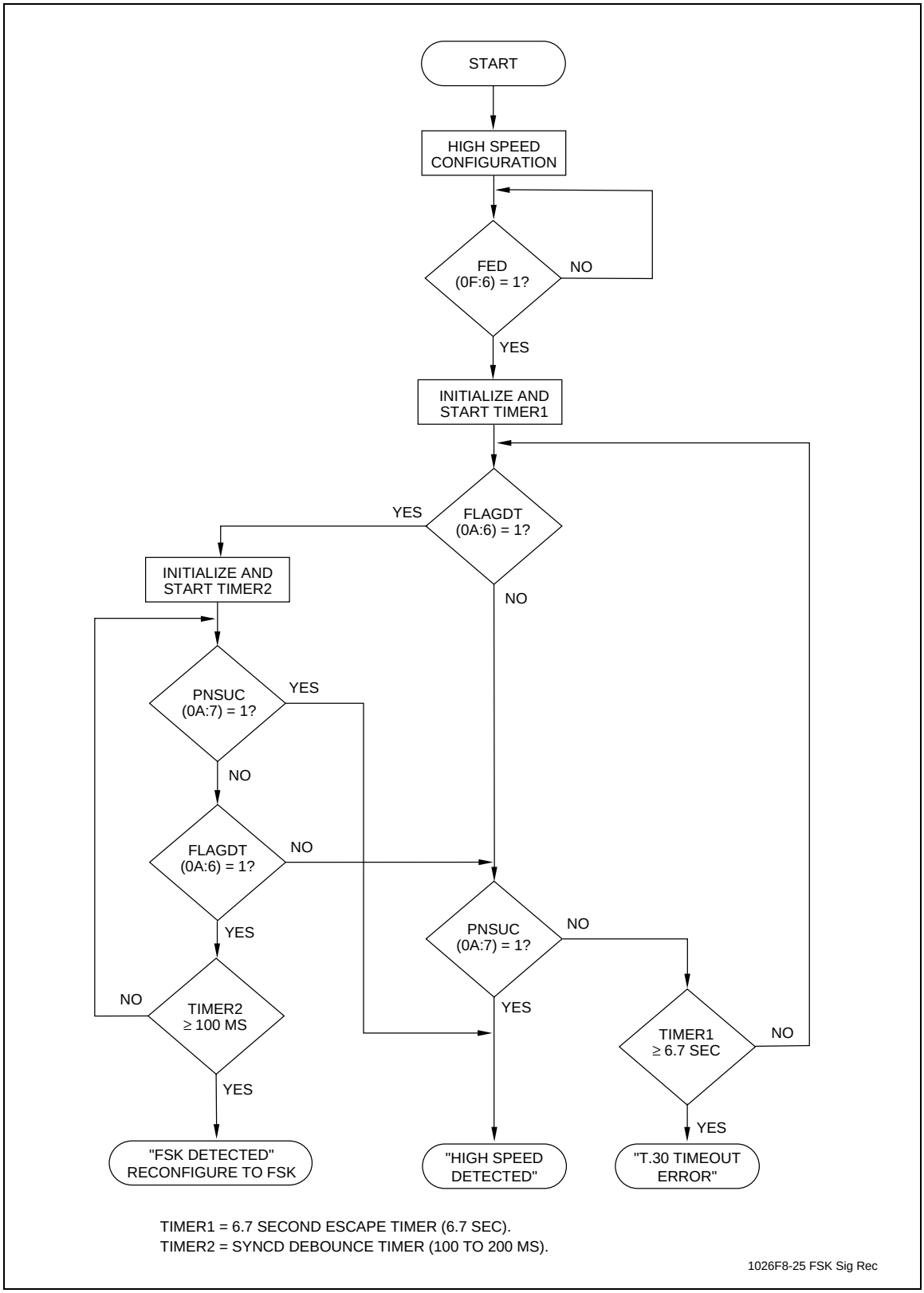


Figure 8-25. FSK Signal Recognition Algorithm

9. V.8 OPERATION CONSIDERATIONS

The host can access several registers in RAM to control and monitor V.8 operation (see Section 4). There are five control registers (Table 9-1) and three status registers (Table 9-2). The host also has access to 13 registers which contain the configuration (CONF) codes associated with the 13 modes of operation (Table 9-3).

To enter V.8 mode, load the interface memory CONF register (Table 3-1) with AA and then set the NEWC bit.

9.1 V.8 ORIGINATING MODEM OPERATING PROCEDURE

Once in the V.8 mode, set DTR to initiate the V.8 handshake.

In originate mode, the transmitter is set up to transmit Silence by default. (Optionally, CI may be sent if the host sets bit 304h:2.) The receiver is set up to detect ANS and ANSam. The data pump sets bit 301h:5 when ANS is detected and sets bit 302h:3 when ANSam is detected.

9.1.1 Originating Without CI Option (Default)

Once ANSam is detected, the transmitter waits a silence period before transmitting CM. The silence period is 500 ms if no phase reversals are detected in ANSam, otherwise the silence period is 1 second. The CM sequence consists of a Preamble, followed by a SYNC octet, a Data Call Function Category octet, at least one modulation mode octet, an optional protocol octet, and an optional GSTN octet (Table 9-4). The 16-byte transmit buffer, located at address 32Dh, is loaded with the CM sequence once ANSam is detected.

The number of modulation mode octets transmitted is a function of the bit settings in control addresses 306h to 308h (Table 9-1). For example, if no modulation bits are set in addresses 307h or 308h, then only one modulation octet is sent (modn0). On the other hand, if bits are set in address 307h, but not in address 308h, then modn0 and modn1 are sent. Only when address 308h contains non-zero modulation bits will all three modulation octets be sent.

The protocol octet is transmitted if bit 305h:0 is set. The 3-bit protocol field is located in bits 305h:7-5. The default protocol bits are set to indicate LAPM availability. The GSTN octet is sent if bit 304h:4 is set. The GSTN octet will be sent indicating cellular access if bit 305h:2 is set.

CM transmission continues until JM is detected. When JM is detected, the current CM octet is completed and then CJ gets appended to the transmitted data stream. A 75 ms silence period follows CJ transmission and the CONF register is updated to the "Modulation Mode" indexed by the highest common modulation mode in JM (Table 9-3).

If no modulation modes are common, the CONF register changes to AFh, the "V.8 Cleardown" mode.

9.1.2 Originating With CI Option

Once DTR transitions on, the transmitter is silent for 400 ms before the CI sequence (Table 9-5) is transmitted. CI is sent with a regular cadence of 1 second on and 1 second off. The on and off times are accessible via memory access (Section 4, Functions 89). In particular, the on time counter, MaxFrameByteCount, is located at 31Ch. This counter is a "byte" counter and defaults to 30 bytes for CI transmission. (Note that the MaxFrameByteCount should not be less than 9 { = 3 frames} if the minimum three frames of CI is desired.) If this location is negative (i.e., MSB = 1), then there is no cadence applied to the transmitted V.8 frame.

Note: MaxFrameByteCount = FFh when transmitting CM and JM.

The CI cadence will continue until ANSam is detected and the minimum three CI frames have been transmitted. Upon detection of ANSam, CM is sent in the manner described in Section 9.1.1.

9.2 V.8 ANSWERING MODEM OPERATING PROCEDURE

If configured as the V.8 answer modem, the transmitter will transmit ANSam. The receiver will detect V.8 frames CI, CM, and CJ. Bits 301h:3-1 hold the status of CM, CI, and CJ detection (Table 9-2).

When CM is detected, a JM frame is constructed using parameters from CM (Table 9-6).

The JM sequence starts with the 10 ONES preamble followed by the synchronization octet. Next comes the call function. If the received CM octet contains the same call function as the answer modem's "preferred" call function, then the same call function that was received in CM is also sent in JM.

If the CM octet contains a different call function that the "preferred" call function, then the CallFunctionAllowed register (address 32Ah) is consulted. (Table 9-7).The host can set up the CallFunctionAllowed register to indicate the call functions that it allows. It is a bit-mapped register where bit k is set if call function 2k is to be allowed. If the call function received in CM does not match any allowable call functions, then the preferred call function is returned with all modulation bits set to zero. On the other hand, if the call function is allowed, the answer modem will respond with the same call function as that received in CM.

JM will contain all the necessary modulation octets needed to reflect the jointly common modulation modes available at the answer modem and received in the CM sequence. However, if bit 305h:1 is set, then JM will contain the minimum number of modulation octets needed to convey the highest common mode. If no modulation modes are common, then the JM frame will send all modulation octets with none of the modulation bits set.

The protocol octet is sent only if the received CM contained a protocol octet AND control bit 305h:0 is set. The GSTN octet is sent if control bit 304h:4 is set OR if the received CM contained a GSTN octet. The GSTN octet will be sent indicating cellular access if control bit 305h:2 is set.

Table 9-1. V.8 Host Control Bits

Address (Hex)	7	6	5	4	3	2	1	0	Default Value (Hex)[1]
304	Call Function to be Transmitted			Send GSTN Octet		Transmit CI	No TX of ANSam until CI Detected		C0
305	Protocol Bits to be Transmitted				**No RLSD in V.8**	Cellular Access	Send Minimum JM Sequence	Send Protocol Octet	28
306	X	**V.34 FDX**	X	X	X	X	X	X	40
307	V.27	V.29	X	X	X	V.17	**V.22**	**V.32**	03
308	**V.21**	V.23 HDX	X	X	X	**V.23 FDX**			84

Notes:

1. Default values are written at POR.
2. Default bits turned on are indicated in bold.

Table 9-2. V.8 Status Bits

Address (Hex)	7	6	5	4	3	2	1	0	Default Value (Hex)*
301		FSK Byte Ready	ANS Detected	JM Detected	CJ Detected	CM Detected	CI Detected	Min CI Sent	00
302	Received Call Function			Protocol Octet Received	ANSam Detected			No Modes Common	00
303	Received Protocol Bits						Remote is using Cellular	Received GSTN Octet	00

* Cleared on NEWC with CONF = AAh.

Table 9-3. Modulation Modes

Address (Hex)	Configuration	Default Value (Hex)[1]
409	K56flex Receive	CE
309	V.34 full-duplex	CC
30B	V.32 bis	76
30C	V.22 bis	84
30D	V.17	B1
30E	V.29	14
30F	V.27	02
310	Reserved	08
311	Reserved	08
312	V.23 full-duplex (Note 2)	A4
313	V.23 half-duplex	A4
314	V.21	A0

Notes:

1. See CONF codes in Table 3-1.
2. Default value assumes V.23 answer mode; change to A1 for V.23 originate mode (see CONF bits in Table 3-1).

Table 9-4. CM Frame

Address (Hex)	Octet	Default Value (Hex)
	Preamble	FF
32D	SYNC CM	E0
32E	Data Call Function	C1
32F	modulation 0	40
330	modulation 1 *	13
331	modulation 2 *	94
332	Protocol (optional)	1A
333	GSTN (optional)	2D
334	Frame End	7E

* if necessary

Table 9-5. CI Frame

Address (Hex)	Octet	Default Value (Hex)
	Preamble	FF
32D	SYNC CI	00
32E	Data Call Function	C1
32F	EOF	7E

Table 9-6. JM Frame

Address (Hex)	Octet
	Preamble
32D	SYNC JM
32E	Call Function from CM
32F	Common modulation 0
330	Common modulation 1 *
331	Common modulation 2 *
332	Protocol (optional)
333	GSTN (optional)
334	Frame End
* if necessary	

Table 9-7. CallFunctionsAllowed

Address (Hex)	7	6	5	4	3	2	1	0	Default Value (Hex)
32A	CF 7 Allowed	CF 6 Allowed	CF 5 Allowed	CF 4 Allowed	CF 3 Allowed	CF 2 Allowed	CF 1 Allowed	CF 0 Allowed	40

9.3 V.8 AND AUTOMODE

The MDP offers an automode option for connecting to the large existing base of non-V.34 modems. By setting AUTO = 1 and DATA = 0 from the V.8 configuration (CONF = AA), the "V.32 bis automode" method of automoding will be performed as well as the V.8 method (Table 9-8).

Table 9-8. Automode Parameters

CONF	AUTO	DATA	Result
7Xh (V.32 bis/V.32 modes)	1	0	Automodes from V.32 bis/V.32 to V.22 bis, Bell 212A, V.21, V.23, and Bell 103.
7Xh (V.32 bis/V.32 modes)	0	1	V.32 bis only.
AAh (V.8 mode)*	1	0	Automodes from V.8 to K56flex or V.34, V.32 bis, Bell 212A, V.22 bis, V.21, V.23, and Bell 103.
AAh (V.8 mode)	0	1	V.8 (K56flex or V.34) or V.32 bis.
* Most common mode.			

9.4 HANDSHAKE MONITORING

9.4.1 V.8 Octet Monitoring

During the V.8 (Phase 1) procedure the received V.8 octets can be read from the interface memory RBUFFER register by clearing bit 305h:3 in the V.8 host control bits. The procedure is the same as accessing receive data during normal data mode.

Handshake Phase Monitoring

During the V.8/V.34 handshake, the secondary channel data buffers display the "state" of the receiver (SECRXB) and the transmitter (SECTXB). Bits 5, 6 and 7 of these buffers indicate the phase of the handshake (Table 9-9 and Table 9-10).

Using the New Status (NEWS) function, an interrupt can be generated whenever a change occurs to SECRXB and SECTXB. The NEWS masks for these locations are 370h and 371h, respectively. For a full description, refer to Section 4.

Table 9-9. Receiver Handshake Phase and States

Register (Hex)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
16 (SECRXB)	Receiver Handshake Phase			Receiver Handshake Phase State				

Bits 7-5: Receiver Handshake Phase.

Bit 7	Bit 6	Bit 5	Dec Value	Handshake Phase (ITU Specification)
0	0	0	0	Phase 1 (V.8)
0	0	1	1	Phase 2 (V.34)
0	1	0	2	Phase 3 (V.34)
0	1	1	3	Phase 4 (V.34)
1	0	0	4	Phase 4 Rate Renegotiation (V.34)

Bits 4-0: Receiver Handshake Phase States.

Phase 1

Receiver Handshake Phase 1 States

Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	State Number	Originate Mode Receiver State	Answer Mode Receiver State
0	0	0	0	0	00	Looking for ANSam	Looking for CI or CM
0	0	0	0	1	01	Found ANSam, looking for JM	Found CI, looking for CM
0	0	0	1	0	02	Found JM	Found CM, looking for CJ
0	0	0	1	1	03		CJ detected

Phase 2

See Figure 9-2.

Phase 3

See Figure.

Phase 4

See Figure 9-4.

Table 9-10. Transmitter Handshake Phase and States

Register (Hex)	7	6	5	4	3	2	1	0
17 (SECTXB)	Transmitter Handshake Phase			Transmitter Handshake Phase State				

Bits 7-5: Transmitter Handshake Phase

Bit 7	Bit 6	Bit 5	Dec Value	Handshake Phase (ITU Specification)
0	0	0	0	Phase 1 (V.8)
0	0	1	1	Phase 2 (V.34)
0	1	0	2	Phase 3 (V.34)
0	1	1	3	Phase 4 (V.34)
1	0	0	4	Phase 4 Rate Renegotiation (V.34)

Bits 4-0: Transmitter Handshake Phase State.

Phase 1

Transmitter Handshake Phase 1 States

Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	State Number	Originate Mode Transmitter State	Answer Mode Transmitter State
0	0	0	0	0	00	Pausing 400 ms (Transmitting silence)	Sending ANSam
0	0	0	0	1	01	Sending CI	Sending JM
0	0	0	1	0	02	Sending Silence (500 ms or 1000 ms)	Sending Silence (75 ms)
0	0	0	1	1	03	Sending CM	
0	0	1	0	0	04	Sending CJ	
0	0	1	0	1	05	Sending Silence (75 ms)	

Phase 2

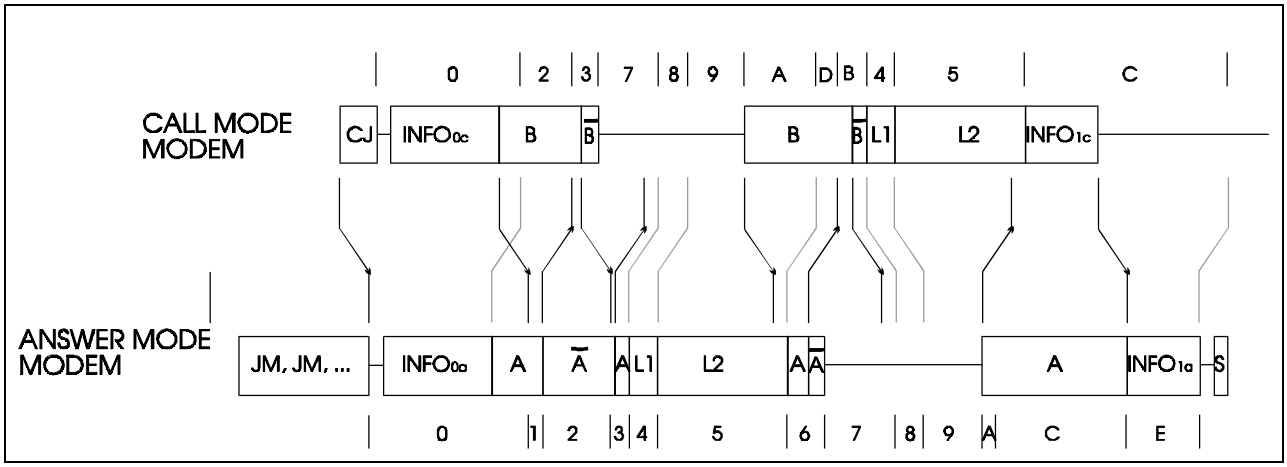
See Figure 9-2.

Phase 3

See Figure.

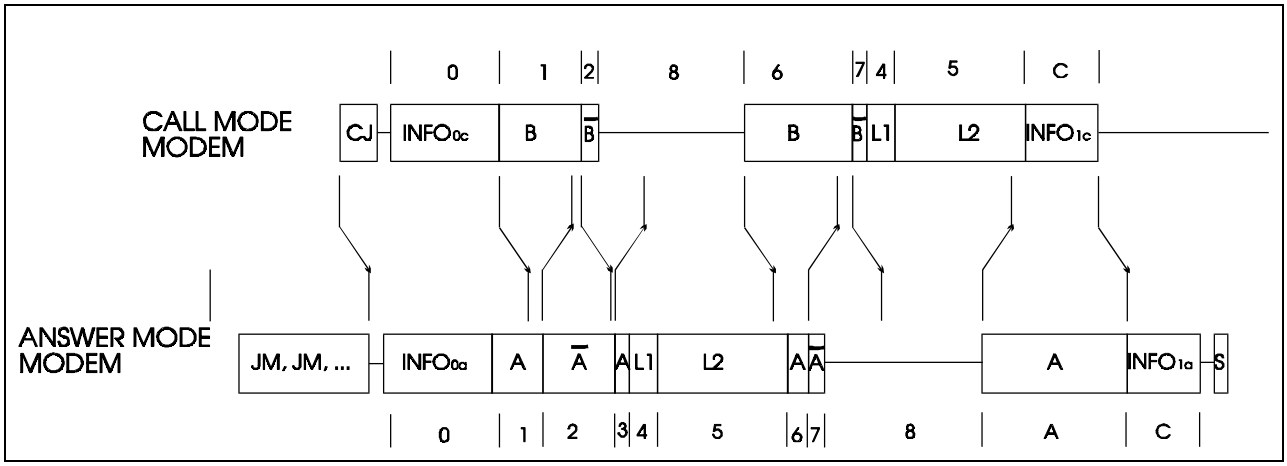
Phase 4

See Figure 9-4.



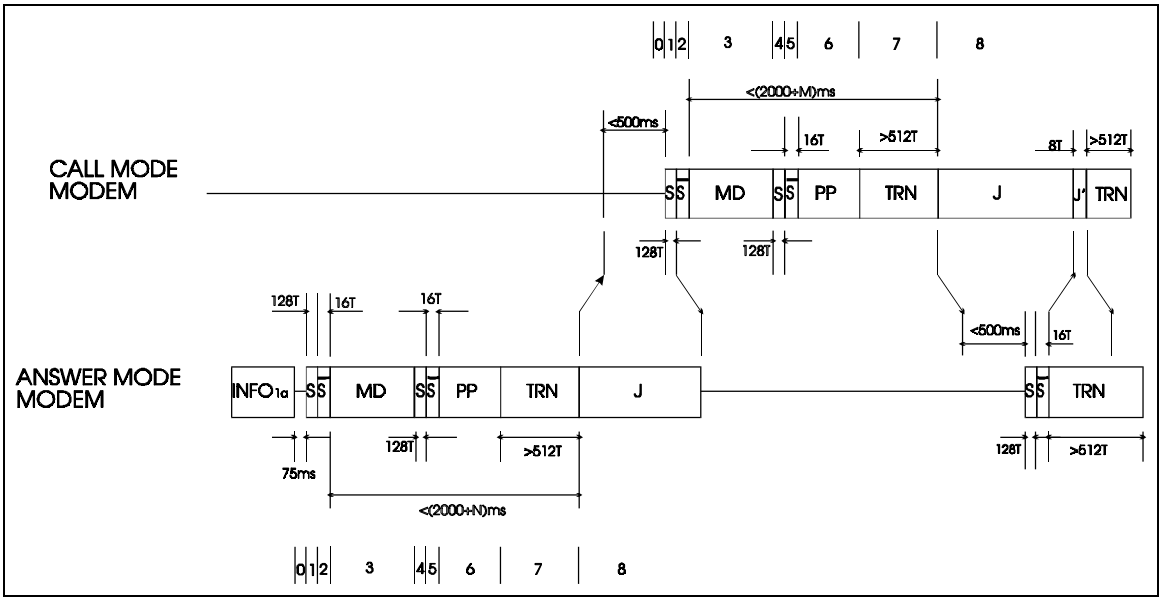
The phase state value is shown above or below the signal trace.

Figure 9-1. Phase 2 Receiver States



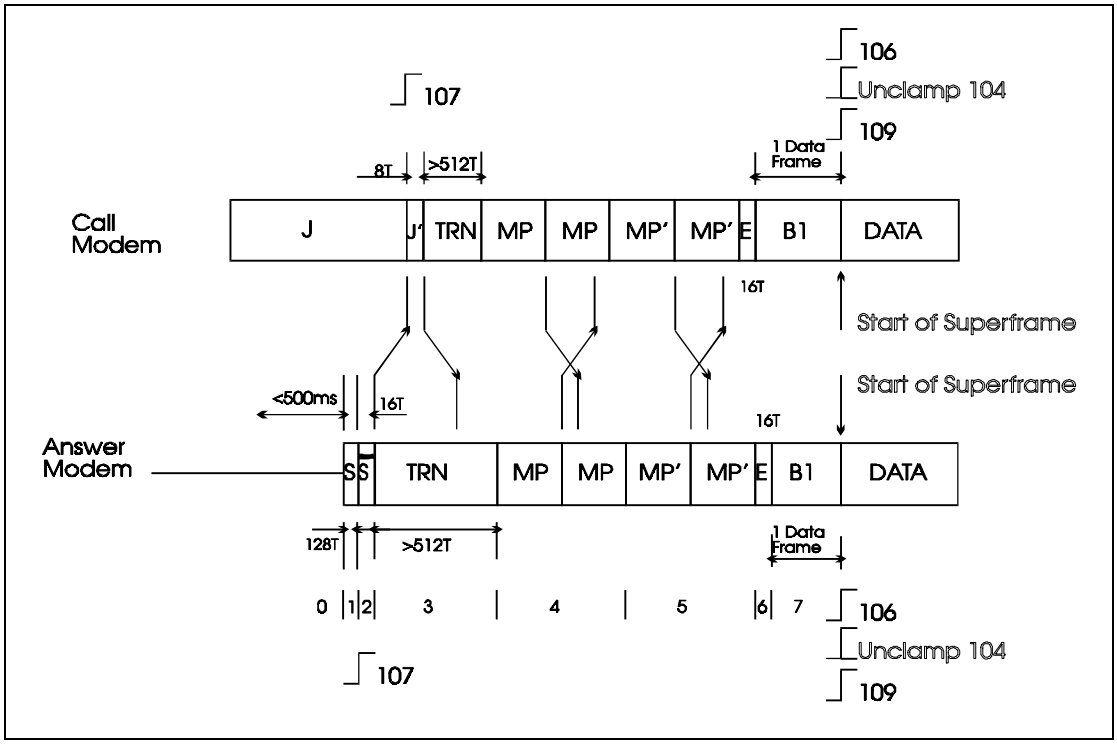
The phase state value is shown above or below the signal trace.

Figure 9-2. Phase 2 Transmitter States



The phase state value is shown above or below the signal trace.

Figure 9-3. Phase 3 States



The phase state value is shown above or below the signal trace.

Figure 9-4. Phase 4 States

10. V.8bis

10.1 V.8bis TRANSMITTER

V.8bis tones can be transmitted from tone mode (CONF = 8Xh), speakerphone mode (CONF = ACh), or V.21 mode (CONF = A0h with V21S = 1). CEQ should be 0. The V8bis tones are sent in the same manner as DTMF tones, i.e., write the codeword into TBUFFER when TDBE=1.

The codewords for V.8bis are described in Table 10-1.

Table 10-1. V.8 bis Codewords

V.8bis Codeword (Hex)	V.8bis Signal	Segment 1 Dual Tones (Hz)	Segment 1 Power level (dBm)	Segment 2 Single Tones (Hz)	Segment 2 Power level (dBm)
20	MR_e	1375 + 2002	-23.5	650	-23.5
21	MR_d	1375 + 2002	-10	1150	-10
22	CR_e	1375 + 2002	-23.5	400	-23.5
23	CR_d	1375 + 2002	-10	900	-10
24	ES_i	1375 + 2002	-10	980 *	-10
28	MR_e	1375 + 2002	-10	650	-10
2A	CR_e	1375 + 2002	-10	400	-10
30	**	1529 + 2225	-23.5	650	-23.5
31	MRd	1529 + 2225	-10	1150	-10
32	**	1529 + 2225	-23.5	400	-23.5
33	CRd	1529 + 2225	-10	1900	-10
34	ESr	1529 + 2225	-10	1650 *	-10
38	**	1529 + 2225	-10	650	-10
3A	**	1529 + 2225	-10	400	-10

Notes:

* The 1650 Hz and 980 Hz single tones are V.21 MARK frequencies for the high and low channels, respectively. Therefore, it would be generated by setting DTR immediately after writing 34h or 24h into TBUFFER. If in answer mode, set NV25 =1 to prevent answer tone from being sent instead of MARK.

** These signals are available, but are currently undefined by V.8bis.

10.2 V.8bis RECEIVER

The V.8bis detector is enabled by setting bit 439h:0 = 1 and setting NEWC from dial modes (CONF = 8xh), speakerphone mode (CONF = ACh), or V.21 mode (CONF = A0h with V21S = 1). (When in tone mode, the "talk-mode tone detectors" are unavailable when running the V.8bis receiver.)

When a valid V.8bis signal is received, the corresponding codeword appears in the V.8bis RX buffer (16h). Also, bit 7 of the V.8bis Rx buffer (16h:7) indicates that a dual tone has been detected. A value of E0h means that a valid Segment 1 (dual tone) has been received and a single tone is being detected.

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11. ADPCM VOICE COMPRESSION AND DECOMPRESSION

ADPCM compression (Rx-coding) of received, ADC digitized voice may be selected to minimize the memory required for message storage. Silence detection and deletion may also be selected to further reduce the memory storage requirements.

ADPCM decompression (Tx-decoding) of stored/recorded compressed voice may be selected in order to either playback or transmit messages. Silence interpolation may be enabled to interpolate any silence deleted during reception.

Data flow through the Rx-coder and Tx-decoder are shown in Figure 11-1 and Figure 11-2, respectively.

11.1 ADPCM RECEIVER (RX-CODER)

11.1.1 Mode Selection

ADPCM Rx-coding is selected when Coder Enable (CDEN) is set in Receive Voice Mode [i.e., Transmit Single Tone, Transmit Dual Tone, Dialing, or DTMF Receiver configuration (CONF = 80h, 83h, 81h, or 86h) and Receive Voice (RXV) is set]. (See Table 11-1.)

Squelching the transmitter output by setting the TXSQ bit will prevent the TXA1 and TXA2 noise floor from being coupled back into the RXA input when receiving voice samples in(either pass-through or ADPCM voice mode.

11.1.2 Operation

When Rx-coding is selected, received analog voice from the RXA input is sampled, converted to digital, digitally scaled, compressed (coded), then passed to the 16-bit Voice Receive Buffer (VBUFR) where the speech samples can be read by the host (Figure 11-1). Typical receive ADPCM voice mode operation is illustrated in Figure 11-3.

The host must select 2, 3, or 4 bits per sample compression with the Coder No. of Bits (CODBITS). With 2, 3, or 4 bits per sample at the 7.2k Hz default programmable sample rate, the 16-bit coder output words are provided at 14.4k, 21.6k, or 28.8k bps (900, 1350, or 1800 16-bit words per second), respectively. The specific application will dictate a higher bits/sample rate for best speech quality or a lower bits/sample rate for minimum storage requirements.

The Rx-coder writes 16-bit coded words to output register VBUFR then sets status bit RDBF. The IRQ output may be enabled using the RDBIE bit to interrupt the host whenever the RDBF bit sets to indicate that VBUFR is full.

Receive FIFO Operation

The receiver FIFO is always enabled, similar to data mode, to allow reading in bursts if desired. Always read from RBUFFER with the data coming in low-high order. The host must first read the status bits before reading the data. The low byte is ready to be read when PE is set and the high byte is ready to be read when FE is set. The first voice sample is ready when both SYNCD and PE are set.

11.2 ADPCM TRANSMITTER (TX-DECODER)

11.2.1 Mode Selection

ADPCM Tx-decoding is selected when Decoder Enable (DCDEN) is set in Transmit Voice Mode [i.e., Transmit Single Tone, Transmit Dual Tone, Dialing, or DTMF Receiver configuration (CONF = 80h, 83h, 81h, or 86h) and Transmit Voice (TXV) is set]. (See Table 11-1.)

11.2.2 Operation

When TX-decoding is selected, compressed digital voice samples (coded words) received from the host through the 16-bit Voice Transmit Buffer (VBUFT) are decompressed (decoded), digitally scaled, converted to analog, then routed to the TXA1 and TXA2 outputs (Figure 11-2). Typical transmit ADPCM voice mode operation is illustrated in Figure 11-4.

The host must select 2, 3, or 4 bits per sample decompression with the Decoder No. of Bits (DECBITS).

If enabled by the Silence Decoder Enable (SDCEN) bit, silence interpolation is performed to reconstruct deleted silence from stored voice samples and white noise is inserted (see Section 10.3.2). The programmable white noise level may be set to zero for absolute silence insertion.

The host supplies the decoder with the 16-bit coder output words by writing to VBUFT when TDBE is set.

Transmit FIFO Operation

Set FIFO = 1 to enable the transmit FIFO. Reset TEOF = 0. Write the low byte to TBUFFER. Set TEOF = 1 and then send the first high byte to TBUFFER. This will sync the host data stream and the data pump. Continue transmitting the 16-bit words in low-high order via TBUFFER while TXFNF = 1.

Table 11-1. ADPCM Voice Mode Selection

CONF	RXV	TXV	CDEN	DCDEN	Mode
*	0	1	0	0	Tx Pass-through Voice Mode
*	0	1	0	1	Tx ADPCM Voice Mode
*	1	0	0	0	Rx Pass-through Voice Mode
*	1	0	1	0	Rx ADPCM Voice Mode

NOTES:
* = ACh, 80h, 81h, 83h, or 86h.

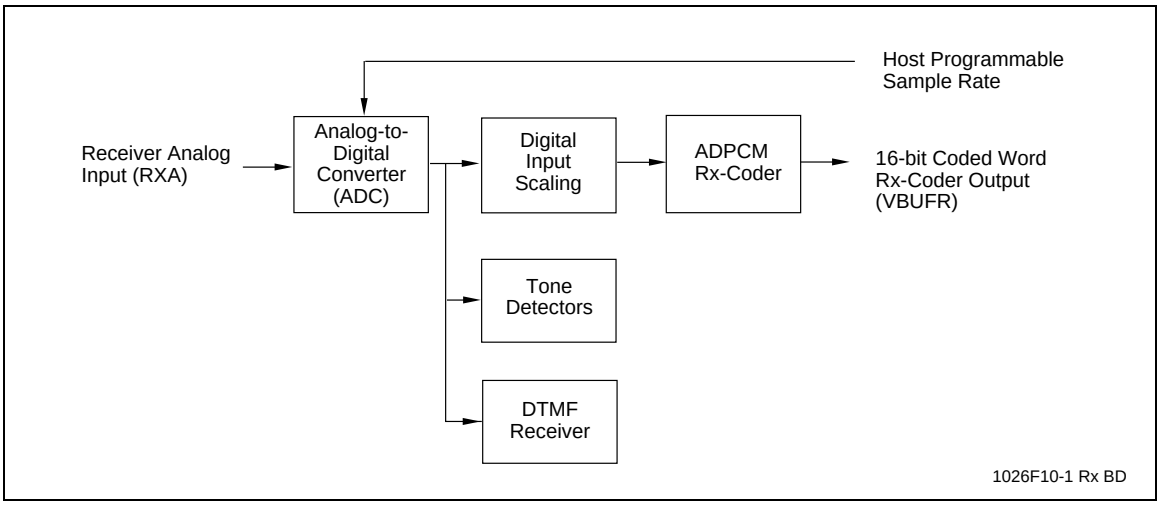

Figure 11-1. ADPCM Rx-Coder

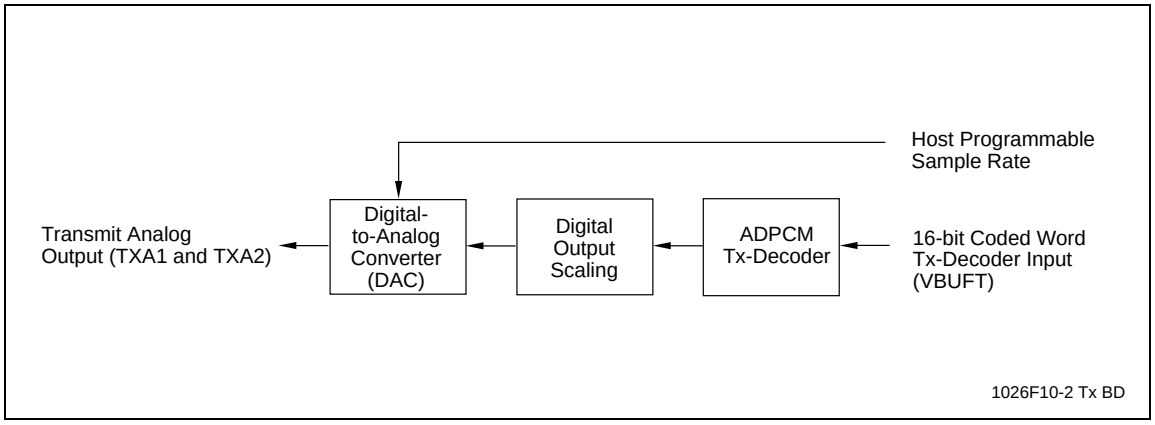

Figure 11-2. ADPCM Tx-Decoder

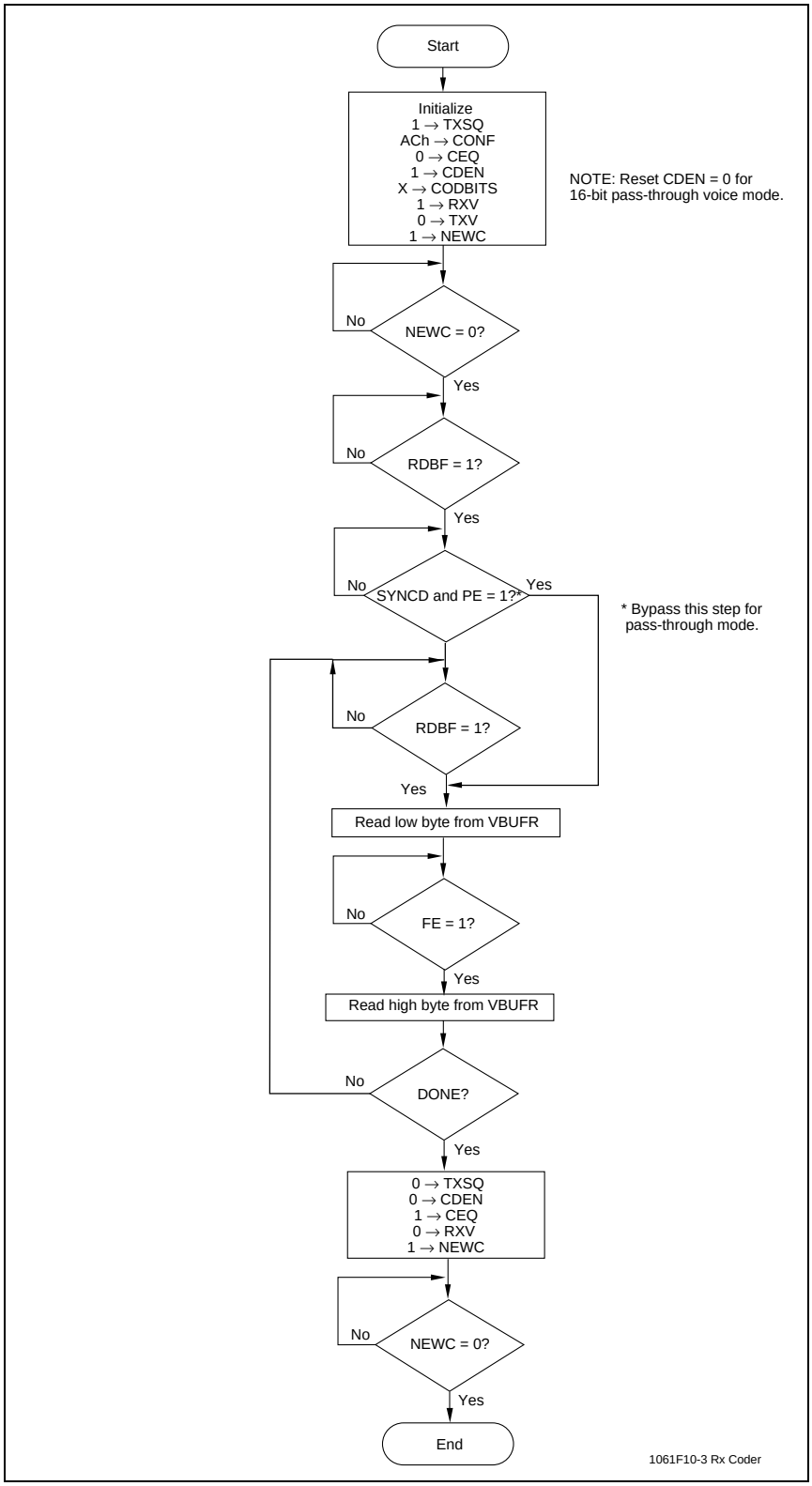

Figure 11-3. Rx-Coder Operation

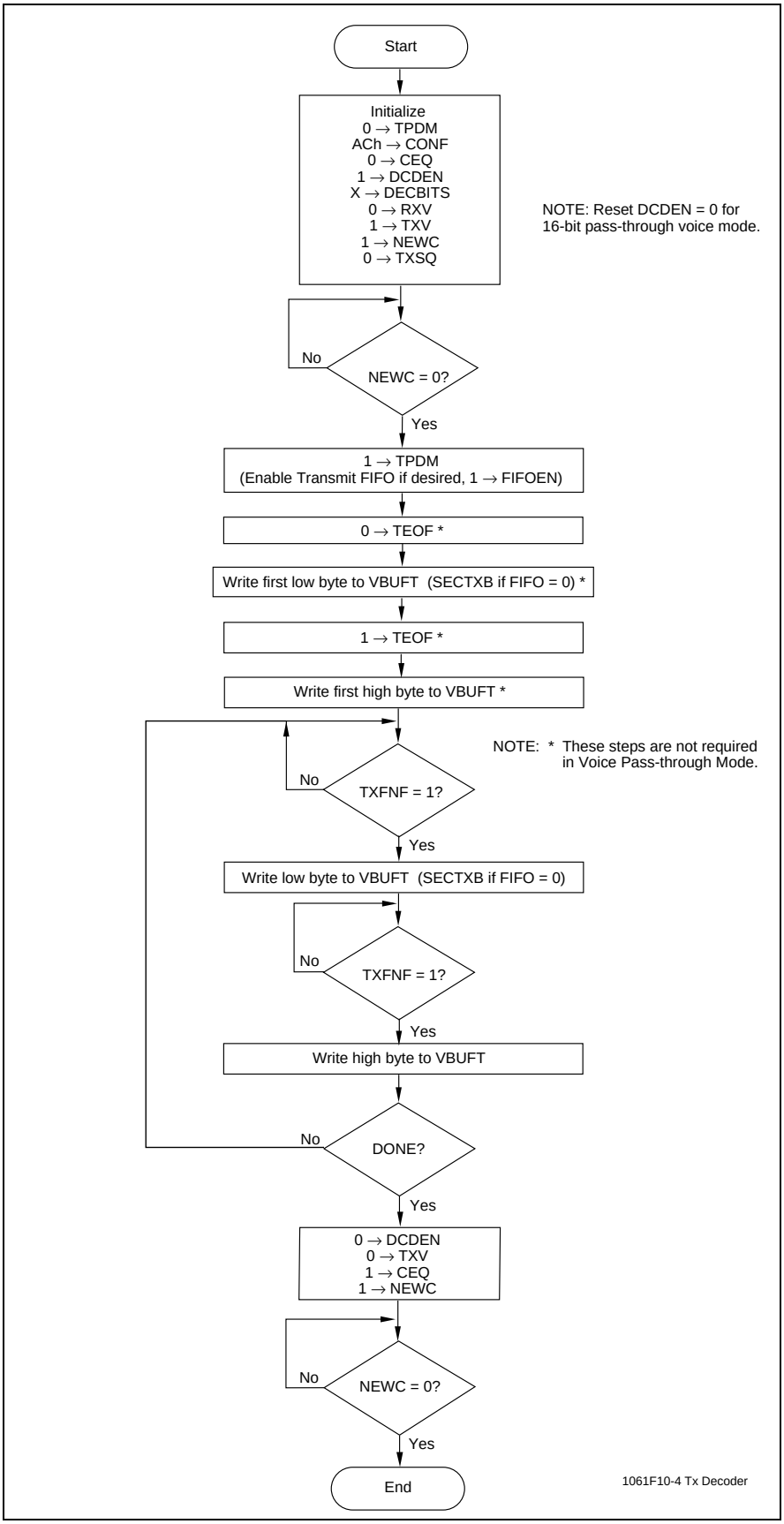

Figure 11-4. Tx-Decoder Operation

11.3 VOICE AGC

An optional AGC function in included in the voice receiver (compressed and uncompressed). Voice AGC is enabled or disabled by setting or resetting the VAGC bit [04h:2 (shared with NRZIE)].

The AGC is updated on a 28-sample "voice frame" basis. The average input sample (AverageENG) is compared to a voice threshold (VTHRESH) to determine if there is enough energy to perform the automatic gain control (AGC). When the average energy is below this threshold, the input samples are not AGC'ed. When the energy is above the threshold, the Gain is updated and the Gain is applied to the next voice frame. Gain is only updated when the energy is above VTHRESH and only once per voice frame. Furthermore, Gain is limited to the maximum voice gain (VMAXG).

11.3.1 Voice AGC Parameters

The voice AGC parameters are listed in Table 11-2.

Table 11-2. Voice AGC Parameters

Name	Description	Address (Hex)	Default* (Hex)
VMAXG	Maximum Gain	E63	4000
VAGCREF	AGC Reference Level	E62	0800
VTHRESH	AGC Energy Threshold	E65	0000
VSRATE0	Slew Rate 0	F62	4500, then 0300
Alpha	Low Pass Filter Gain	F61	0100
Pole	Low pass Filter Pole	D62	7EFF
VoiceSlewRateCtr	Counter Slew Rate Adjustment	3AE, 3AF	F10
* If bit 1 of register 04 (shared with TOD) is set, then the above voice AGC parameters are not initialized. This allows the host to write in values without having to worry about contentions with the data pump initialization.			

Voice AGC Reference (VAGCREF)

The AGC algorithm adjusts the Gain so that the squared output of the Voice LPF, $(LPFOutput)^2$, tends to VAGCREF. The default value of VAGCREF is 0100h corresponding to a recorded level of nearly -16 dBm. By lowering VAGCREF, the recorded volume is lowered.

Slew Rate (VSRATE)

The slew rate parameter controls the rate at which the gain tracks the input signal. The larger the slew rate multiplier, the faster the AGC Gain word tracks the input signal.

The VoiceSlewRateCtr is used to allow the AGC gain word to quickly adjust to the input level at the beginning of the recording and then slow down to a "steady-state" rate thereafter. The counter counts down at the 16-bit data rate and is disabled when the most significant byte is negative. The default VoiceSlewRateCtr value corresponds to two seconds for 4-bit ADPCM recording. So for the first two seconds, the AGC slew rate is 4500h and then it changes to 0300h for the remainder of the recording.

Maximum Gain (VMAXG)

The Gain value is limited to VMAXG. When VMAXG is small, the AGC process works to a lower level of input. Under default conditions, the 4000h value of VMAXG cuts off at -40 dBm. That is, the Gain remains constant (= VMAXG) for input levels below -40 dBm. By lowering VMAXG, lower level signals will receive gain.

Voice Energy Threshold (VTHRESH)

When the average frame value is above VTHRESH, the AGC process runs, otherwise the received samples are recorded without gain. This threshold comparison is intended to prevent the noise floor from being raised during silence periods. This "silence" feature can introduce choppiness if not tuned correctly. As a result, the default value for VTHRESH is zero which, effectively, disables this feature.

Low Pass Filter Output (LPFOutput)

The low pass filter output is a function of the input level and the LPF gain, Alpha. The default value of Alpha, together with the LPF pole value, give a LPF gain of 0 dB. By increasing Alpha, the recorded volume is lowered.

AGC Gain Equation: $Gain = Gain + [(LPFOutput)^2 - VAGCREF]\ VSRATE$

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12. SIMULTANEOUS AUDIO/VOICE AND DATA (AUDIOSPAN)

All RAM addresses mentioned in this section are 16-bit access if 12th bit of address field is set, or 8-bit access if 12th bit is reset, unless otherwise specified.

12.1 ML144/V.61 (V.32bis) AUDIOSPAN CONTROL

12.1.1 AudioSpan Control Registers

AudioSpan Control Register 1 (Address 439h)

Bits 7-2 Reserved

Bit 1 Host AudioSpan Enable/Disable (Host-SVDEn) (Do not set if V.8 is used.)

1 = Enable host AudioSpan.

0 = Disable host AudioSpan.

Bit 0 V.8bis Detector Enable/Disable (V8bDetEn)

1 = Enable V.8bis detector.

0 = Disable V.8bis detector.

AudioSpan Control Register 2 (Address 400h)

Bit 7 Half-Duplex Gain Control Enable/Disable (HDXgcEn)

1 = Enable half-duplex gain control. (Recommended for mic/spkr operation or when handset echo canceller is used.)

0 = Disable half-duplex gain control.

Bit 6 Mic AGC Enable/Disable (QmicAGCen)

1 = Enable AGC on mic. (Not recommended for headset or handset operation.)

0 = Disable AGC on mic.

Bit 5 Handset or Spkr/Mic Select

1 = Select Handset (TELIN/TELOUT lines selected).

0 = Select Spkr/mic (SPKRM/MICM lines selected).

Bits 4-3 Reserved

Bit 2 Voice Squelch (VoiceSq)

1 = Squelch voice. Set this bit to signal off-hook status to remote modem.

0 = Enable voice.

Bit 1 AudioSpan Symbol Rate Select

1 = 3000.

0 = 2800.

Bit 0 Reserved

Maximum Voice+Data Rate (Address 42Ah)

Bits 7:5 Reserved

Bit 4 Remote Tx Silence Detection Enable/Disable

1 = Enable remote Tx silence detection.

0 = Disable remote Tx silence detection.

Bit 3 Reserved

Bits 2-0 Maximum Voice+Data Rate

000 = 4800 bps.
001 = 4800 bps.
010 = 4800 bps (default).
011 = 7200 bps.
100 = 9600 bps.
101 = 12000 bps.
110 = 14400 bps.
111 = 14400 bps.

Bit 0 Reserved

12.1.2 ML144 Mode Selection

To enable ML144/V.61, perform the following:

1. Enable Host AudioSpan: Set bit 439h:1 to 1.
2. Select a V.32bis configuration: For example, set CONF to 76h.
3. Set NEWC to 1.

Alternatively,

1. Configure for V.8: Set CONF = AAh.
2. Set bit 350h:2. Do not set bit 439h:1 if V.8 is used.

12.1.3 Detecting Remote Off-Hook Status

Setting bit 400h:2 squelches the AudioSpan audio transmission and causes bit 419h:7 to be set on the remote modem. Bit 400h:2 should be set when the audio link is in an on-hook state.

When the handset is picked up or the mic is enabled, the host should reset bit 400h:2. This will cause bit 419h:7 to reset on the remote modem, indicating an audio link request.

12.1.4 Generating Ring and Ringback

A dual-tone generator is available during a ML144 AudioSpan connection. When enabled, the AudioSpan audio is suppressed and the tone(s) is routed to the speaker or handset, depending which is enabled. This can be used to generate a ring signal when detecting a remote off-hook status as described above. It may also be used to generate a local ringback signal while waiting for the remote user to answer.

Tone Generator Enable/Disable (Address AB0h)

Bits 7-0 Tone Generator Enable/Disable

Non-0 = Enable tone generator.

0 = Disable tone generator.

The tone generator is enabled my making address AB0 non-zero. This value is reset with NEWC, RTRN or RREN.

Tone 1 Frequency (Address BB0h) and Tone 2 Frequency (Address BB2h)

The frequency equation is:

$$N = F/0.13745$$

Where: N is the decimal equivalent of the hex number written to RAM and F is the frequency.

Tone 1 Amplitude (Address AB0) and Tone 2 Amplitude (Address AB2h)

The power equation is:

$$N = 2033(10^{Po/20})$$

Where: N is the decimal equivalent of the hex number written to RAM an Po is the power level in dBm.

The equation is based on VOLUME bits (01h:7-6) = 2.

Generating Ringback Example

1. Set ringback frequencies of 440/480 Hz: Write 0C81h and 0DA4h to addresses BB0h and BB2h, respectively.
2. Set a suggested power level of -20 dBm for each frequency: Write 00CBh to addresses AB2h and AB0h.
3. Enable the tone generator (start the tone transmission): Write a non-zero value to address AB0h. **Note:** AB0 should be that last address written to.
4. Control the cadence of the ringback: Write a zero and non-zero value to address AB0h as required.

12.1.5 ML144/V.61 AudioSpan Rate Sequence

The values in address 42Ah are used to generate the Tx Rate sequence words 2 and 3. The ARC bit must be set = 1 to allow the modems to negotiate the highest common voice+data rate to be used.

AudioSpan Rate Sequence Word 2 and Word 3 are stored in RAM and are set up from contents of address 42Ah after NEWC is set. They can be changed directly by the host, without using masking registers, after DTR is set. Tx Rate Sequence Word 1 and mask register are the same as V.32bis.

Tx Rate Sequence Word 2: Low Byte (Address 42Eh, Default = 11h); High Byte (Address 42Fh, Default = 0Dh)

Rx Rate Sequence Word 2: Low Byte (Address 432h); High Byte (Address 433h)

High Byte (Address 42Fh/433h) Definition

Bit 7 **0**

Bit 6 **0**

Bit 5 **0**

Bit 4 **0**

Bit 3 **1**

Bit 2 **1 = Voice+data rate at 4800 bps is enabled (default)**

Bit 1 **1 = Voice+data rate at 9600 bps is enabled**

Bit 0 **1**

Low Byte (Address 42Eh/433h) Definition

Bit 7 **0**

Bit 6 **1 = Voice+data rate at 7200 bps is enabled**

Bit 5 **1 = Voice+data rate at 12000 bps is enabled**

Bit 4 **1**

Bit 3 **1 = Voice+data rate at 14400 bps is enabled**

Bit 2 **0**

Bit 1 **0**

Bit 0 **1**

Tx Rate Sequence Word 3: Low Byte Address (430h, Default = 93h); High Byte Address (431h, Default = 01h)

Rx Rate Sequence Word 3: Low Byte Address (434h); High Byte Address (435h)

High Byte (Address 431h/435h) Definition

Bit 7 **0**

Bit 6 **0**

Bit 5 **0**

Bit 4 **0**

Bit 3 **0**

Bit 2 **0**

Bit 1 **0**

Bit 0 **1**

Low Byte (Address 430h/434h) Definition

Bit 7 **1**

Bit 6 **0**

Bit 5 **0**

Bit 4 **1**

Bit 3 **0**

Bit 2 **0**

Bit 1 **1 = Silence detection enabled at receiving transmitter (default)**

Bit 0 **1**

12.1.6 Selecting Voice+Data Rates

The value in address 42Ah can be used for the initial handshake, retrains and rate renegotiations. If a 0 is placed in address 42Ah, the user may modify the rate sequence directly through addresses 42Fh/42Eh. Rate changes may easily be accomplished by setting the desired speed in address 42Ah followed by setting RREN, however, using the rate sequence masks at address 42Fh/42Eh gives the user more flexibility. Changing CONF and setting RREN will change the data-only rate for when silence detection is being used. The voice+data rate will not be affected.

12.1.7 Maximum Voice+Data Rate

The voice+data rate is defined as the user data rate when audio information is being sent. Assuming minimal line disturbances, the maximum voice+data rate is 14.4k bps in ML144, however, a degradation in audio quality can be observed at this high rate. It is suggested that the voice+data rate be maintained at two speeds below the maximum possible data-only rate for the given line conditions (one speed is a difference of 2400 bps). For example, a line capable of supporting a 14.4k data-only connection would be able to support a 9.6k voice+data connection with good audio quality.

12.1.8 Data-only or Voice+Data Detection

If silence detection is used to allow the MDP to automatically shift between voice+data and data-only mode, bit A35h:E may be used to determine the state of the MDP. If set, bit A35h:E indicates the MDP is in data-only receive mode. When reset, the MDP is in voice+data receive mode.

12.1.9 Speaker Attenuation/Gain Control

Speaker Gain Control

The speaker gain may be controlled through the VOLUME bits (01h:7-6):

Speaker Attenuation (dB)	Value in 01h:7-6 (Bin)
Speaker off	00
0 dB (high volume)	01
6 dB (medium volume)	10
12 dB (low volume)	11

The speaker gain may also be altered through address 990h. This location is reset to default after a RREN and is adjustable only when the modems are connected. The speaker volume is relative to the microphone gain of the remote audio source. Values written to address 990h do not correspond to absolute output levels but rather to relative changes in output level. The following table illustrates the relative gain in 2 dB steps:

Speaker Relative Gain (dB)	Value in 990 (Hex)
+10	FC00 (maximum)
+8	FA00
+6	F800
+4	F400
+2	F200
0	F000 (default)
-2	EC00
-4	EA00
-6	E700
-8	E400
-10	E200

12.1.10 Microphone Gain Control

The microphone gain is controlled through bits 3D3h:2-1:

Microphone Gain (dB)	Value in 3D3h:2-1 (Bin)
0	00
10	01
15	10
20	11

The gain may also be altered through address B7Eh. This location is reset to default after a RREN and is adjustable only when the modems are connected. The total input gain should not bring the input signal level above -16 dBm to avoid input saturation. The following table illustrates the relative gain in 2 dB steps:

Microphone Relative Gain (dB)	Value in B7E (Hex)
+10	1500
+8	1200
+6	0F00
+4	0C00
+2	0A00
0	0800 (default value)
-2	0500
-4	0200
-6	FF00
-8	FD00
-10	FA00

The equation to calculate the relative gain change for both mic and speaker is as follows:

Gain change in dB = 20Log(M#2) - 20Log(M#1)

Where:

$M = 2^{(x + y/2048)}$

The 16-bit signed value is broken down as: xxxxxyyyyyyyyyyy (y = bits 0-A and x = bits B-F)

M#1 is calculated based on the current gain value.

M#2 is calculated based on the new gain value.

12.1.11 TELIN/TELOUT Gain Control

When using TELIN/TELOUT for handset operation, the gain control has to be through address B7Eh for TELIN and address 990h for TELOUT. The VOLUME bits and mic gain control at address 3D3h do not apply.

12.1.12 Handset Echo Canceller

When bit 400h:5 is set for handset operation, the handset echo canceller must be enabled to avoid echoes on the remote end. To enable the echo canceller, write 8004h to address A5Ch. If read back, a value of 0004 or 4004h will be present. 8004h should be written to A5C once the modems are connected and handset operation is desired.

The half-duplex gain control bit (400h:7) should also be set to further suppress the echo. When bit 400h:5 is reset for headset or mic/spkr operation, disable the echo canceller by writing 0000 to A5Ch.

12.2 HOST INTERFACE SELECTION AND SETUP

There are basically three audio interface possibilities:

1. Microphone/Speaker (Mic/SPKR): Where an external microphone and speaker is used. Ties into the MICV and SPKR-V pins.
2. Headset: Where a headset with built-in microphone or an external audio source and speaker is used. The external audio source can be in the form of a microphone, CD or DAT player. Ties into the MICV and SPKR-V pins.
3. Handset: Where a telephone handset is used. Ties into the TELIN and TELOUT pins.

The first two interfaces both use the same pins on the device but are in separate categories since some options such as volume and gain control may require different settings between the two modes.

Configuration for Interface Setups

To Select Mic/SPKR:

1. Turn off handset mode: Reset bit 400h:5 to 0.
2. Turn on the mic AGC if desired: Set bit 400h:6 to 1.
3. Enable the half-duplex gain control: Set bit 400h:7 to 1. *
4. If on, turn off the handset echo canceller: Write 0 to A5Ch. (Only matters if in connect mode.)
5. Adjust volume to the desired level: e.g., set VOLUME bits to 2.

To Select Headset:

1. Turn off handset mode. Reset bit 400h:5 to 0.
2. Turn off the mic AGC. Reset bit 400h:6 to 0.
3. Although not necessary, disable the half-duplex gain control: Reset bit 400h:7 to 0.
4. If on, turn off the handset echo canceller: Write 0 to A5Ch. (Only matters if in connect mode.)
5. Adjust volume to the desired level: e.g., set VOLUME bits to 2.

To Select Handset:

1. Turn on handset mode: Set bit 400h:5 to 1.
2. Turn off the AGC. Reset bit 400h:6 to 0.
3. Enable the half-duplex gain control: Set bit 400h:7 to 1. *
4. Turn on the handset echo canceller after connected: Writing 8004h to A5Ch.
5. Adjust volume as desired: Use speaker scale location 990h (default F000h). Note that this location may get reset after RRENs or RTRNs. **Note:** VOLUME bits do not apply in handset mode.

* Note that the half duplex gain control does not render the audio communication half duplex. It simply dynamically adjusts input and output gains to minimize acoustic echoes.

12.2.1 Typical Operation and Selection of User Interface

After a connection is accomplished, the audio channel should typically be off until an audio link is desired, therefore, the Voice squelch bit 400h:2 should be set. This is also referred to as the "User Command Data Mode bit". It signifies that the user wishes to remain in data mode with no audio.

When bit 400h:2 is set, the remote modem sets bit 419h:7, indicating that the other modem is "on-hook" (no audio link desired). It is suggested that the interface defaults to the Mic/SPKR configuration so that a simulated ring signal may be heard through the speaker. The ring signal can also be heard if headsets are used (assuming they are being worn). The application may want to flash some sort of indicator when an audio link request is detected if headsets are used. There is no currently no method of ringing the phone itself. A possible solution would be for the voice relay to be asserted only when a remote audio link request is detected and the voice relay line could then be used to cause external ring voltage circuitry to ring the phone.

Assuming one scenario at a time:

Scenario 1: User Picks Up the Handset

1. When the handset is picked up (LCS is detected), the user wants an audio link, therefore, the handset configuration should be initiated and bit 400h:2 (voice squelch) should be reset. This causes bit 419h:7 on the remote modem to turn off.
2. The remote modem may then signal a ring by using the dual tone generator and the local modem, where the handset was picked up, may generate a ringback tone (see the description on how to generate ring and ringback). The ringback tone should only be generated if bit 419h:7 is set, indicating that the remote modem is still "on-hook".
3. When the remote modem answers the audio link request by either picking up the handset or invoking Mic/SPKR or headset operation, it should turn off it's simulated ring and turn off bit 400h:2 which will cause the local modem to reset bit 419h:7. Upon detecting 419h:7 going off, the local modem should stop generating ringback. The audio link is now enabled.

Scenario 2: Using Headset or Mic/SPKR

1. When headsets or Mic/SPKR is used to initiate the audio link request, there is no line current sensing to know when an "off-hook" status is requested. The application must have a means of enabling this mode and instructing the MDP to reset bit 400h:2) for an audio link request. It is advisable that the application distinguish between headset and Mic/SPKR operation since the AGC is recommended for Mic/SPKR use but not for headset operation.

Scenario 3: Hanging Up (Terminating the Audio Link)

1. When either the local or remote modem goes back "on-hook", bit 400h:2 should be set again to squelch the audio link. This will cause the other modem (the one that has not hung up yet) to have bit 419h:7 set. By the same token, the modem that terminated the audio link will still see its bit 419h:7 reset until the other party "hangs up". This does not mean the modems should again generate ring or ringback tones!.
2. When the remote modem hangs up, the local modem should not generate ringback based on 419h:7 until it has gone "on-hook" and back "off-hook".
3. The local modem that "hung-up" should not generate ring until it has seen bit 419h:7 go from 0 to 1 and back to 0 again, indicating that the remote modem went "on-hook" and back "off-hook". In other words, ring and ringback tones should not be generated again until after both modems have been in a terminated audio link state.

Ring or No Ring?

Some applications may require the audio link always be enabled with no control from the modem, particularly in headset operation. In this case, bit 400h:2 should not be set and since 400h:2 is not set and therefore 419h:7 is not set on either modem, no ring or ringback tones should be generated.

If user audio link control and ring/ringback tones are to be used:

- The MDP will generate ring if bit 400h:2 is set and bit 419h:7 is reset. If 400h:2 is reset or if 419h:7 is set, ring tones will be off.
- The MDP will generate ringback if bit 400h:2 is reset and bit 419h:7 is set. If 400h:2 is set or if 419h:7 is reset, ringback tones will be off.

Note: Remember that ring and ringback tones should not be generated unless both modems have previously been in a terminated audio link state at a some time.

Muting the Outgoing Audio

Although the outgoing audio is squelched when bit 400h:2 is set, it should not be used for that purpose once the audio link is established. If used, it may terminate the audio link depending on how the received bit 419h:7 is interpreted. The input scale value at address B7Eh could be used but causes the remote eye to reduce down to single points.

A noise generator is available on the outgoing audio path. It is enabled by writing a non-zero value to address BB3h. A value of 0005h is suggested. The higher the value, the higher the noise. The value of 0005h is low enough to not be heard but will maintain a proper EQM value on the remote modem. If silence detection is enabled, the value of 0005h will cause the remote modem to shift to a data only mode rate which will automatically mute the received audio as well.

An example of when this should be used is while waiting for the remote modem to respond to an audio link request. When the local modem goes "off-hook", the outgoing audio path is enabled since bit 400h:2 is reset. This means that all input audio is getting across to the remote modem and can be heard over the speaker or headset. If the remote modem is generating a simulated ring, the audio which is coming from the local modem input can be heard between ring tone generation.

In order to prevent this, the local modem initiating the audio link request should mute its outgoing audio by writing 0005h (or desired value) to BB3. When the local modem detects the remote "off-hook" status (419h:7 = 0), the outgoing audio should be enabled again by writing 0000h to BB3.

13. SPEAKERPHONE CONFIGURATION

The Speakerphone Configuration Code (CONF) is ACh.

To configure for speakerphone operation:

1. Set CONF = ACh.
2. Set SP/HS = 1.
3. Reset MuteSp and MuteMic.
4. Adjust VMicLVL and VOLUME bit fields as desired.
5. Dial or answer.
6. If needed, adjust volume using VOLUP and VOLDWN.

13.1 INTERFACE MEMORY REGISTERS

The speakerphone registers are:

Register	7	6	5	4	3	2	1	0
14	SpDTMF	TonSpkE	TonLinE	—	—	SpRIEn	—	
13	—	VOLUP	VOLDWN	SP/HS	MuteSp	MuteMic	VMicLVL	

Note: The speakerphone registers are shared with other data-mode definitions.

SP/HS controls the speakerphone mode of operation. When SP/HS = 1, full-duplex operation is enabled. Conversely, when SP/HS = 0, the data pump functions in "handset" mode. In handset mode, the AGCs are frozen, the cross-correlator is disabled, and the acoustic echo canceller is "bypassed." The input from the voice IA is switched to come from TELIN and the output to the voice IA is sent to TELOUT.

13.1.1 DTMF and Dual Tone Modes

DTMF dialing can be sent to the line (DTMF = 1) and/or to the speaker (SpDTMF = 1) (see Table 13-1).

The dial digit is sent by writing to TBUFFER (similar to how it is done in mode 81h). To send a DTMF digit, write its number into TBUFFER. For example, to send the DTMF digit "4" to both the line and the speaker, set both SpDTMF and DTMF = 1 and then write a 04 into TBUFFER.

Table 13-1. DTMF Routing

DTMF	TonLinE	Dual Tone Mode	SpDTMF	TonSpkE	Dual Tone Mode
1	x	DTMF dialing to the line	1	x	DTMF dialing to the speaker
0	1	Dual Tone (using RTS)	0	1	Dual Tone (using DTR)
0	0	No tones	0	0	No tones

The dual tone parameters addresses are listed in Table 13-2.

Table 13-2. Dual Tone Frequency Parameters

Dual Tone Function	Address (Hex)
Line Dual Tone 1 Amplitude	868
Line Dual Tone 1 Frequency	968
Line Dual Tone 2 Amplitude	869
Line Dual Tone 2 Frequency	969
Number of Line Tones -1	B68
Speaker Dual Tone 1 Amplitude	86A
Speaker Dual Tone 1 Frequency	96A
Speaker Dual Tone 2 Amplitude	86B
Speaker Dual Tone 2 Frequency	9BF
Number of Speaker Tones -1	B6A
Note: Setting NEWC will reset these locations. All addresses are 16-bit access.	

In dual tone mode, RTS is used to control the line dual tone transmitter and DTR is used to control the speaker tone transmitter.

The equations for the frequency and power values are:

Frequency: $N = F/0.109863$

Power: $N = 9405\ (10^{Po/20})$

Where:

N is the decimal equivalent of the hex number written to RAM.

F is the frequency in Hz and Po is the power in dBm (based on a 600 ohm load).

The control parameter functions are:

- SpRIEn enables Ring detection. A tone pair is sent to the speaker when SpRIEn is enabled and incoming ring is detected.
- VOLUP and VOLDWN control the speaker volume in ± 2 dB increments in addition to the VOLUME bit field selection.
- MuteMic and MuteSp control the muting of the microphone and the speaker, respectively. To be more precise, the MuteSp bit mutes the "line input".
- MMicLVL and VMicLVL control the modem and voice microphone input levels, respectively.

13.2 VOICE PATHS

The following describes how to setup the voice mode paths. The Integrated Analog (IA) function has a dual interface: a Modem IA and a Voice IA. The voice transmit and receive paths can be switched through either IA. The speaker output can be from one of three different sources, RIN, mic (MICM or MICV) or MDP DSP (SR4OB or SR3OB). The input can be selected from RIN/TELIN or the Mic. Refer to the voice path figures at the end of this section. **Note**: The voice paths apply to CONF = Speakerphone mode (ACh), TXV = 1 and/or RXV = 1.

The voice block diagram is shown in Figure 13-1.

The transmit voice receiver path is illustrated in Figure 13-2 and the receiver voice path is illustrated in Figure 13-3.

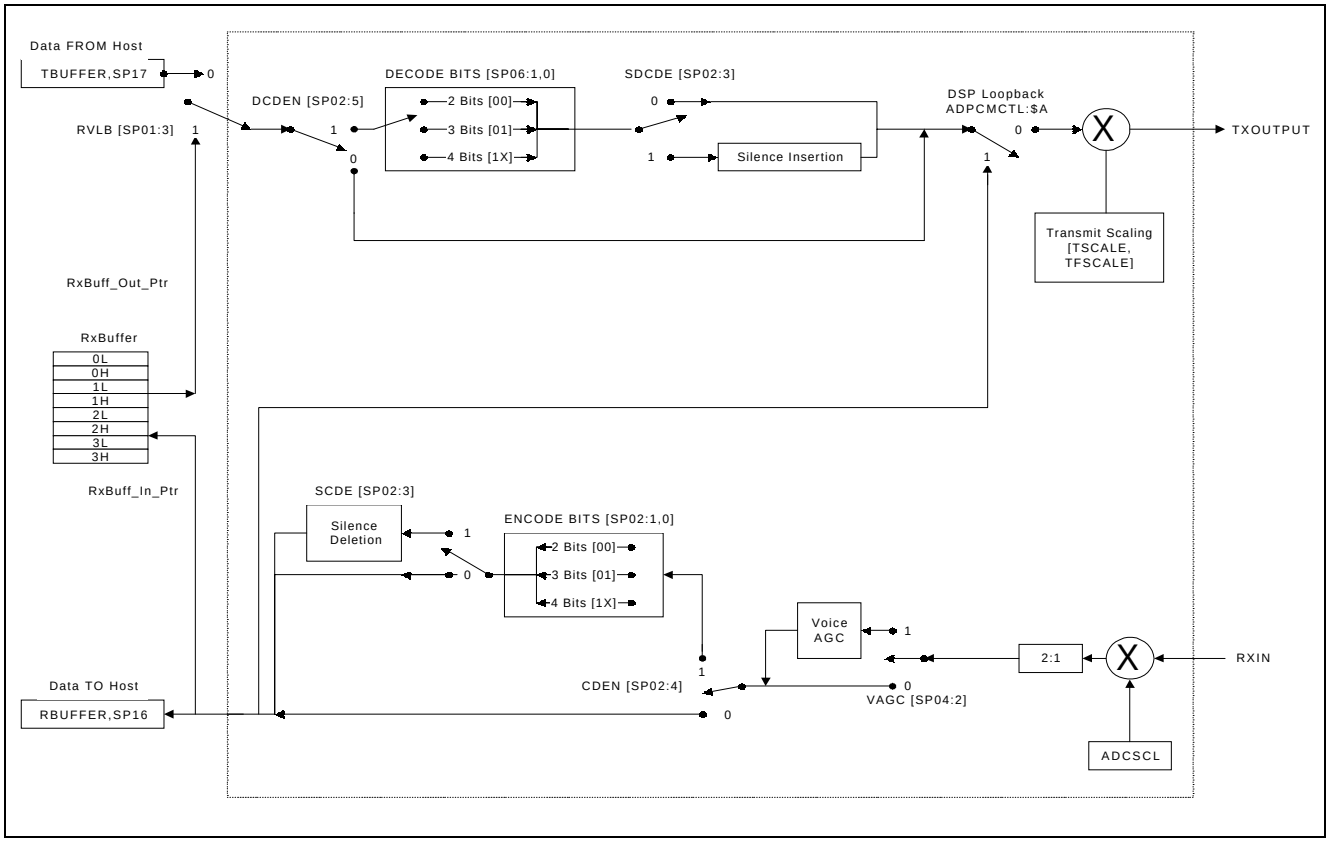

Figure 13-1. Voice Flow Block Diagram

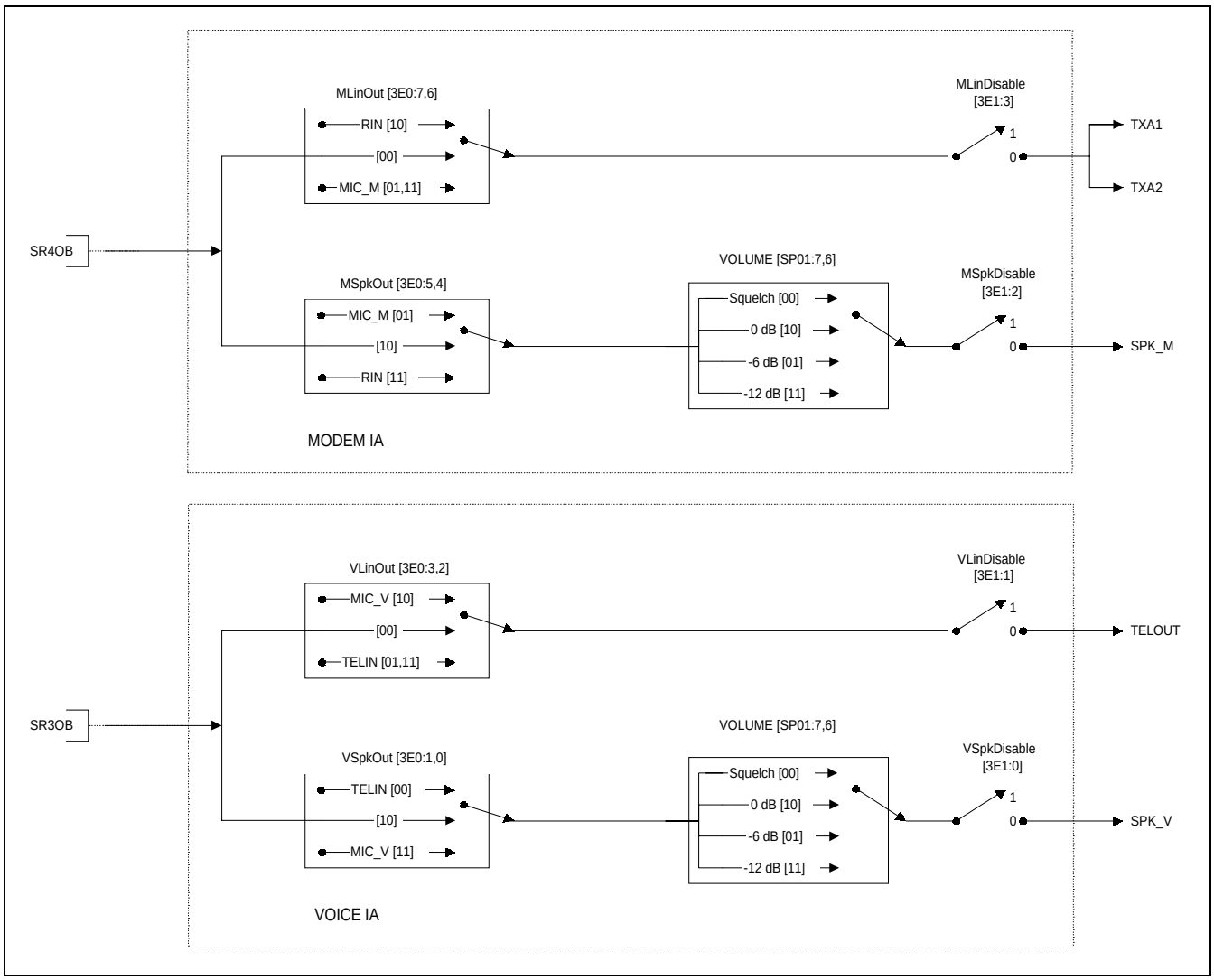

Figure 13-2. Transmit Voice Paths

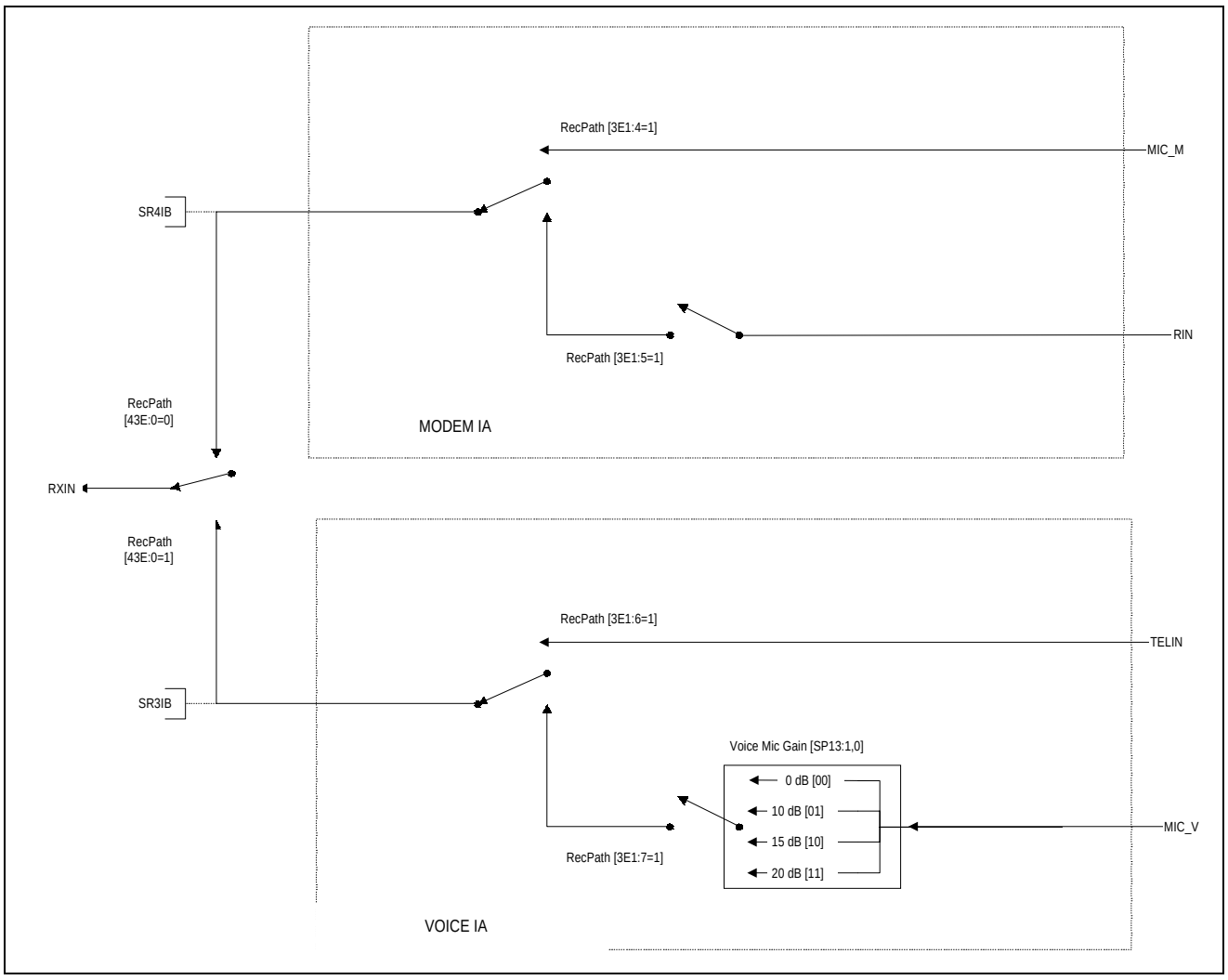

Figure 13-3. Receiver Voice Paths

Voice Output Path (Address 3E0h)

7-6	5-4	3-2	1-0
Modem IA Line Output	Modem IA Spkr Output	Voice IA Line Output	Voice IA Spkr Output

Bits 7-6 Modem IA Line Output

00 SR4OB to TXA1/TXA2
01 RIN to TXA1/TXA2
10 MICM to TXA1/TXA2
11 RIN to TXA1/TXA2

Bits 5-4 Modem IA Speaker Output

01 RIN to SPKM
10 SR4OB to SPKM
11 MICM to SPKM

Bits 3-2 Voice IA Line Output

00 SR3OB to TELOUT
01 TELIN to TELOUT
10 MICV to TELOUT
11 TELIN to TELOUT

Bits 1-0 Voice IA Speaker Output

00 TELIN to SPKV
10 SR3OB to SPKV
11 MICV to SPKV

Voice Control (Address 3E1h)

7	6	5	4	3	2	1	0
EnVMIC	EnTELIN	EnRIN	EnMMIC	MLinDis	MSpkDis	VLinDis	VSpkDis

Bit 7 **Enable the Voice Mic Input, MICV (EnVMIC)**

1 = Enable

0 = Disable

Bit 6 **Enable the Voice Line Input, TELIN (EnTELIN)**

1 = Enable TELIN input.

0 = Disable TELIN input.

Bit 5 **Enable the Modem Line Input, RIN (EnRIN)**

1 = Enable RIN input.

0 = Disable RIN input.

Bit 4 **Enable the Modem Mic Input, MICM (EnMMIC)**

1 = Enable MICM input.

0 = Disable MICM input.

Bit 3 **Disable the Modem Line Output, TXA2 (MLinDis)**

1 = Disable TXA2 output.

0 = Enable TXA2 output.

Bit 2 **Disable the Modem Speaker Output, SPKM (MSpkDis)**

1 = Disable SPKM output.

0 = Enable SPKM output.

Bit 1 **Disable the Voice Line Output, TELOUT (VLinDis)**

1 = Disable TELOUT output.

0 = Enable TELOUT output.

Bit 0 **Disable the Voice Speaker Output, SPKV (VSpkDis)**

1 = Disable SPKV output.

0 = Enable SPKV output.

13.2.2 Volume and Microphone Level Control

Volume Control (01h:7-6)

The VOLUME bits (01h:7-6) control the Voice and Modem speaker volume.

00	Squelch
01	6 dB attenuation
10	0 dB attenuation
11	12 dB attenuation

Voice Microphone Level Control (13h:1-0)

The VMicLVL bits (13h:1-0) control the Voice mic level.

00	00 dB gain
01	10 dB gain
10	15 dB gain
11	20 dB gain

13.2.3 Voice Loopback (Sidetone Feature)

A "voice loopback" feature takes samples from the selected receiver path and plays them back out the selected transmitter path(s). This is a "digital" loopback as opposed to the "analog" or "IA-loopback" features described above in the Line Output and Speaker Output sections. Sidetone can be used for a "music-on-hold" mode. For example, the receive voice samples can be taken from the MDP microphone input (MICM) and then played out over the MDP line out (TXA1/TXA2). The sidetone feature can be used in conjunction with recording. Addresses B6Bh and B69h control the amount of loopback leakage for the modem and voice IA, respectively. **Note:** TXV must be set to enable this feature.

13.2.4 Voice Record, Playback, and Tone Detector Control Register (Address 43E)

Bit 3 **Tone Detection Path Select**

0 = Detect tone from Modem IA

1 = Detect tone from Voice IA.

Bit 2 **Enable Voice Playback to the Modem IA (TXV must be 1)**

1 = Enable voice playback to the Modem IA.

0 = Disable voice playback to the Modem IA.

Bit 1 **Enable Voice Playback to the Voice IA (TXV must be 1)**

1 = Enable voice playback to the Voice IA.

0 = Disable voice playback to the Voice IA.

Bit 0 **Voice Record Path Select**

1 = Record from Voice IA.

0 = Record from Modem IA.

13.2.5 "Room Monitor" Mode

To operate in "room monitor" mode:

1. Set CONF = ACh.
2. Set RXV = 1.
3. Select the output to TXA1/TXA2 to come from SR4OB (3E0h).
4. Setup the voice IA mic level to 20 dB gain (14).
5. Disable the output to SPKV (VSpkDis), SPKM (MSpkDis), and TELOUT (VLinDis).
6. Set VAGC.
7. Select the "record" path to come from the Voice IA (43Eh).
8. Set NEWC.

In this mode, the tone detectors (including the DTMF receiver) are operational.

13.2.6 Voice Idle Mode

It is recommended that RXV be set when operating in voice idle mode from configuration ACh. This allows the transmitter to be used for tone generation (like dialing).

13.2.7 Business Audio (Sampling Frequency = 11025 Hz)

To enable business audio, set bit 43Eh:7. This bit takes effect at NEWC when CONF = ACh. (RXV and/or TXV must also be set.)

13.3 VOICE AGC

See Section 11.3.

13.4 SPEAKERPHONE CONVERSTATION RECORD

When in speakerphone mode, the conversation may be recorded by enabling variable gains on both the transmit and receive paths and reading samples from RBUFFER just as in voice pass through mode with the exception that RXV must be set to 0. The gain locations are AF0h for the transmitter (local speaker) and AF1h for the receiver (incoming voice). Both of these locations default to 0000h. The higher the value, the higher the gain.

Record Procedure

1. Connect in speakerphone mode.
2. Ensure RXV = 0.
3. Write the desired gain values in AF0h and AF1h; a value of 2000h is generally suitable.
4. Read in 16-bit samples through RBUFFER as per voice pass through record procedure. (See Section 11.)

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14. K56flex SETUP AND CODE CHANGES

This section describes the configuration procedure for K56flex downloadable data pump and provides a general description of the K56flex handshake. All RAM accesses are 8 bit (Method 1) unless otherwise noted.

NOTE: This section refers to "client" and "server" modems. For example, the RP56LD/SP MDP is used in a client modem application and the RL56DDP is used in a central site modem (CSM) server modem application.

14.1 K56flex SETUP

In a K56flex connection, the client modem (e.g., RP56LD/SP) will receive in K56flex PCM mode and will transmit a V.34 modulated signal. The server modem (e.g., RL56DDP) will do exactly the opposite. When a successful K56flex connection is established, the CONF register indicates the receiver configuration and speed (Table 14-1) and the SPEED bits indicate the transmitter configuration and speed (Table 14-2). The client modem's CONF value will change from AAh (V.8) to 9Xh if a K56flex handshake has been negotiated. The CONF value may change to a different 9Xh value when the connection is complete (RLSD = 1) depending on rate masks and ARA decisions. The server modem will contain a CXh value in CONF to indicate the V.34 receive speed.

In a K56flex connection, the state of the ORG bit simply determines which modem will send answer tone and which modem will detect it. After a V.8 procedure, similar to the standard V.8 used with V.34, the server modem will always be in an "answer" handshake mode, sending its half-duplex TRN first and the client modem will be in an "originate" handshake mode, sending its half-duplex TRN second. The same handshake sequence will occur regardless of who originated the call, i.e., the ORG bit does not influence the handshake sequence which takes place after V.8. The server modem will typically always answer calls while the client modem will usually originate them. In the event a server modem must use a call back feature, the ORG bit will have to be set on the server modem in order to detect answer tone. In this type of situation, the ORG bit will automatically change to 0 on the server modem and to 1 on the client modem after V.8.

14.1.1 Client Modem (Analog Modem) Configuration Procedure

1. Set CONF = AAh to select K56flex configuration.
2. Write the desired K56flex receive speed in address 409h by writing 9Xh, where X indicates the desired receive data rate. X is in increments of 2000 bps beginning with 32,000 when X = 1. If the ARA feature (EARC = 1) or the rate masks are used, the value in 409h may be left at default. See Table 14-1.
3. Set bit 406h:0 to enable the K56flex receiver.
4. Set ORG bit = 1 if originating, else reset ORG = 0.
5. Set bit 13Fh:6 to enable asymmetric data rates.
6. Set EARC and/or AUTO if desired.
7. Set NEWC.
8. Set DTR to initiate handshake.

14.1.2 Server Modem (Digital Modem) Configuration Procedure

1. Set CONF = AAh to select K56flex configuration.
2. Write the desired V.34 receive speed in RAM address 309h by writing CXh, where X indicates the desired receive data rate. X is in increments of 2400 bps. If the ARA feature (EARC = 1) or the rate masks are used, the value in 309h may be left at default. See Table 14-1.
3. Set bit 406h:0 to enable the K56flex transmitter.
4. Set ORG bit = 1 if originating, else reset ORG = 0.
5. Set bit 13Fh:6 to enable asymmetric data rates.
6. Set EARC and/or AUTO if desired.
7. Set NEWC.
8. Set DTR to initiate handshake.

Table 14-1. K56flex Data Rate Versus Configuration and Data Rate Mask Values

X	Data Rate for CONF = CX and Rate Mask 605h or 604h = 0Xh	Data Rate for CONF = 9X and Rate Mask 605h or 604h = 0Xh
1	2400	32000
2	4800	34000
3	7200	36000
4	9600	38000
5	12000	40000
6	14400	42000
7	16800	44000
8	19200	46000
9	21600	48000
A	24000	50000
B	26400	52000
C	28800	54000
D	31200	56000
E	33600	Reserved

Table 14-2. K56flex Data Rate Versus Speed Bit Values

SPEED (Hex)	Data Rate (bps)	SPEED (Hex)	Data Rate (bps)
0	0–300	10	33600
1	600	11	32000
2	1200	12	34000
3	2400	13	36000
4	4800	14	38000
5	9600	15	40000
6	12000	16	42000
7	14400	17	44000
8	7200	18	46000
9	16800	19	48000
A	19200	1A	50000
B	21600	1B	52000
C	24000	1C	54000
D	26400	1D	56000
E	28800	1E	Reserved
F	31200	1F	Reserved

14.1.3 K56flex Bit Definitions

39Bh:7 - A-law / μ-law Selection. When set, A-law is enabled; when reset, μ-law is enabled. If the modems are configured opposite of each other, they will automatically fallback to V.34. If communicating over an A-law system, the server modem must have this bit set for all modes of operation. The client modem must set this bit only for K56flex operation. Other client modes are not affected.

401h:5 - K56flex Detected. When set, this status bit indicates a remote K56flex modem has been detected. (This bit will set at the end of V.8.) Applicable only if 406h:0 = 1 and if V.8bis is not used as the K56flex phase 1 startup.

401h:4 - K56flex Detected. When set, this status bit indicates a remote answering K56Flex modem has been detected. Detects the K56 PN+ID signal. (This bit will set at the beginning of V.8.) Applicable only if 406h:0 = 1 and if V.8bis is not used as the K56flex phase 1 startup.

401h:0 - K56flex Handshake in Progress. When set, this status bit indicates the modems are proceeding with a K56flex handshake. (Valid after SECTXB>2Xh.)

406h:6 - Auto Robbed Bit Detection [Client Modem Only). If set, the modem will automatically detect robbed bit signaling and inform the server modem. The server modem will automatically adjust its transmitter for robbed bit signaling. This bit is set by default.

406h:2 - Old ROM Coded RBS Control Bit. Do not set this bit on downloadable devices.

406h:1 - K56flex Transmit Level (Server Modem Only). Used on server modem to control the K56flex transmit level (1 = -1dBm0, 0 = -12dBm0).

406h:0 - K56flex Enable. If set, K56flex is enabled; if reset, K56flex is disabled.

408h - Remote K56flex Code Version Number. This code version number is an ASCII number received during V.8 which may be used to identify the remote modem type (valid only if V.8bis is not used as the K56flex phase 1 startup). The code revision number is always odd for server modem and even for client modem.

409h - Desired K56flex Receive Speed. See Table 14-1.

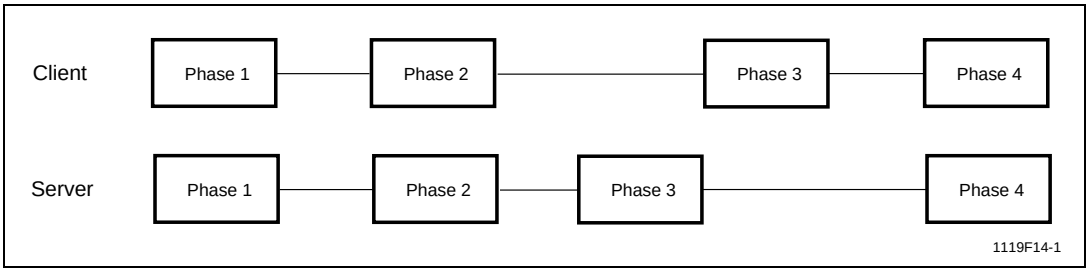
604h - Maximum Receive Rate Mask. See Table 14-1.

605h - Maximum Transmit Rate Mask. See Table 14-1.

The NEWC bit should be set after control bits have been setup as desired.

14.1.4 K56flex Handshake

The K56flex handshake is very similar to V.34. The modems first go through V.8bis then V.8, after which they exchange INFO0 parameters. Each modem then independently sends a probe signal followed by an exchange of INFO1 parameters. A half duplex TRN is then sent by each modem, starting with the server modem, followed by a full duplex TRN and an exchange of MP parameters. The handshake can be followed through the use of the SECTXB and SECRXB registers as in V.34 mode. After Phase 1 , the states are the same for both answer and originate mode. The handshake states are:



Handshake Sequence

Client and Server States During Phase 1 (after V.8bis)

Answer mode:

SECTXB = 0,1,2
SECRXB = 0

Originate mode:

SECTXB = 0,3,5
SECRXB = 1

Client States During Phase 2 (answer & originate mode)

SECTXB = 20,21,22,28,29,24,25,2C
SECRXB = 20,22,23,27,28,29,2A,2D,2B,24,25,2C,2D,2E,2F

Client States During Phase 3 (answer & originate mode)

SECTXB = 40,44,45,46,47,48
SECRXB = 30,31,32,33,48

Client States During Phase 4 (answer & originate mode)

SECTXB = 62,63,64,65,66,67
SECRXB = 61,62,63,65,68

Server States During Phase 2 (answer & originate mode)

SECTXB = 20,21,22,23,24,25,26,27,28,2A,2C
SECRXB = 20,21,22,23,24,25,26,27,28,29,2A,2C,2E

Server States During Phase 3 (answer & originate mode)

SECTXB = 40,41,42,43
SECRXB = 40,41,46,47,48

Server States During Phase 4 (answer & originate mode)

SECTXB = 60,61,62,63,64,65,66
SECRXB = 60,63,64,65,67

Retrains

Retrains follow the same flow of transmitter and receiver states excluding phase 1. Rate renegotiations are a repeat of phase 4 and provide the following states:

Client States During Rate Renegotiation

SECTXB = 80,81,82,83,84,85,86,87
SECRXB = 83,84,85,68

Server States During Rate Renegotiation

SECTXB = 80,81,82,83,84,85,86
SECRXB = 83,84,85,67

14.1.5 Detecting K56flex

When a client modem calls into a server modem it will search for V8bis CRe. If V.8bis is detected, the modems proceed under the K56flex V.8bis startup. The modems will then proceed to establish a K56flex connection. Bit 401h:5 will set, indicating a K56flex modem has been detected and bit 401h:0 will also set, indicating the handshake is proceeding in K56flex mode. Both bits will set at the end of V.8 when the CONF values changes to 9Xh (client modem) or CXh (server modem). If the client modem cannot reply as a K56flex modem, the modems will proceed in V.8 and attempt a V.34 connection or will fallback to a lower modulation mode as needed if the AUTO bit is set.

If a client modem calls another client modem setup to answer as a K56flex modem, the connection will automatically fallback to V.34. The same is true if the modems are not both setup for A-law or μ-law or if the line probe has determined that K56flex cannot be supported over the selected line. Bit 401h:0 will be cleared at the end of phase 2 if the modems fallback to V.34. The host should check this bit after SECTXB>30h to confirm if the handshake is proceeding in K56Flex or V.34 mode.

14.1.6 EQM Readings

The EQM readings and interpretation for the server receiver remain unchanged when compared to the RC336ACF or RC288DPX device in V.34 mode. The same is true for the client modem if connected in V.34 mode, however, the client modem, when receiving a K56flex PCM signal, will provide much smaller values for EQM. Values less than 0300h are typically good and above 0400h are bad. The EQM trip point for fallback or fall forward decisions may not be the same across all speeds. Each speed may require its own EQM limit. The same RAM address is used (20Ch) for reading EQM during the handshake and may be used while in data mode as well.

For the client modem only, a alternative location at 810h (16 bits), which provides larger and more stable values, may be read during data mode instead of the EQM at 20Ch while in K56flex mode. The EQM values at 810h are only valid in data mode and may not be used during the handshake. Although EQM values in 810h are updated during a V.34 or V.32bis connection and should reflect similar values as those seen in 20Ch, the preferred EQM address for these modes is still 20Ch. As a rule of thumb, fall forward and fallback decisions should be based on maintaining the EQM average reading at location 810h at value near 2000h-2500h for μ-law and A00h-1000h for A-law. The 810h EQM readings differ between μ-law and A-law, however, the 20Ch EQM readings do not.

14.1.7 Automatic Data Rate Selection

Automatic Data Rate Selection (ARA), when EARC = 1, also applies in K56flex mode, however, the ARA-in-RAM featured used in V.34 (server receiver in K56flex mode or V.34 mode) does not apply on the client modem when receiving a K56flex PCM signal. The K56flex mode uses predetermined EQM thresholds in order to select the proper data rate during the initial handshake or retrain when EARC = 1. The aggressiveness of the data rate selection may be influenced by changing the EQM scaling at A29h (16-bit access). The value at A29h may be changed in phase 3 (SECRXB = 4Xh). The default value is 0100h. A change of 0010h-0020h is enough to shift the data rate selection up or down by one speed. Increasing A29h will increase the EQM value, causing the ARA algorithm to select a less aggressive speed. Decreasing A29h will decrease the EQM value, causing the ARA algorithm to select a more aggressive speed. Upon connecting (RLSD = 1), the default value of 0100h may be written back to A29h. If not, the EQM value will remain higher or lower as scaled by the value in A29h.

For more flexibility, the user may prefer to take control over the data rate selection by monitoring EQM during phase 4 and manually selecting the data rate based on predetermined EQM thresholds. Such a method is used in V.34 mode with the RCV288DPx and RC336ACF/DPFL V.34 data pumps. The procedure for manual speed selection for both handshakes and retrains is as follows:

K56flex Mode (Client Receiver):

1. Turn off the EARC bit once the handshake is known to be progressing in K56flex mode.
2. Wait for SECTXB = 63h.
3. Wait for LSB of 04Dh = 02h; waiting for transmitted TRN counter to get near end.
4. Quickly read 50 samples (to get a good average) of EQM at 20Ch (16-bit reads) and obtain a total sum (allocate 3 bytes for sum).
5. Based on average EQM value read, select a receive data rate by writing the value 0Xh in 2E4h where X = the corresponding data rate as shown in Table 14-1. The following EQM table is used in the Rockwell ACi firmware. The low byte of the 3-byte EQM sum is thrown out.

K56EQMTable

HighByte,MidByte (Hex)	Receive Data Rate	By writing this hex value to 2E4h
01,30	;If EQM > than ##,##, choose 32 kbps	01
01,00	;If EQM > than ##,##, choose 34 kbps	02
00,F0	;If EQM > than ##,##, choose 36 kbps	03
00,E5	;If EQM > than ##,##, choose 38 kbps	04
00,E0	;If EQM > than ##,##, choose 40 kbps	05
00,D0	;If EQM > than ##,##, choose 42 kbps	06
00,C0	;If EQM > than ##,##, choose 44 kbps	07
00,B0	;If EQM > than ##,##, choose 46 kbps	08
00,A6	;If EQM > than ##,##, choose 48 kbps	09
00,95	;If EQM > than ##,##, choose 50 kbps	0A
00,90	;If EQM > than ##,##, choose 52 kbps	0B
00,50	;If EQM > than ##,##, choose 54 kbps	0C
00,05	;If EQM > than ##,##, choose 56 kbps	0D

V.34 Mode (Normal V.34 or Server K56flex Receive Mode):

1. Make sure EARC = 1 and ARA-in-RAM feature is enabled (3A5h:4 = 1).
2. Wait for SECRXB or SECTXB = 40h.
3. Read and save the symbol rate from 2E3h (will always be 3200 in K56flex mode). Based on the read symbol rate, write the suggested ARA-in-RAM values (see Table 14-3) to the specified locations (all are 8-bit writes)
4. Wait for SECTXB = 63h (handshake and RTRN).
5. Read and save value from 39Ah; this is the data rate the ARA has selected.
6. If the value is 04h or less (9.6k or less), or the rate mask has been set to speeds of 9.6k or less, or the symbol rate is less than 3000, end the procedure; otherwise continue.
7. Write 7800h to A29h (16-bit access), write 7F00h to B29h (16-bit access), and turn off the EARC bit; this scales the EQM value up and turns off ARA. (These locations will automatically be restored at connect time).
8. Wait for the LSB of 04Dh = 02h; waiting for transmitted TRN counter to get near end.
9. Quickly read 50 samples (to get a good average) of EQM at 20Ch (16 bit reads) and obtain a total sum (allocate 3 bytes for sum). The following EQM tables are used in the Rockwell ACi firmware. The low byte of the 3-byte EQM sum is thrown out.

   Note: The older method of basing the EQM tables on a "divide by total samples" average may still be used along with the previously defined EQM tables:

10a. If in answer or originate mode at 3429 symbol rate:

HighByte,MidByte (Hex)	EQM3429Table: Receive Data Rate	By writing this hex value to 2E4h
07,08	;If EQM > than ##,##, choose 12.0 kbps	05
04,7E	;If EQM > than ##,##, choose 14.4 kbps	06
02,DB	;If EQM > than ##,##, choose 16.8 kbps	07
01,F4	;If EQM > than ##,##, choose 19.2 kbps	08
01,25	;If EQM > than ##,##, choose 21.6 kbps	09
00,AF	;If EQM > than ##,##, choose 24.0 kbps	0A
00,6A	;If EQM > than ##,##, choose 26.4 kbps	0B
00,40	;If EQM > than ##,##, choose 28.8 kbps	0C
00,2A	;If EQM > than ##,##, choose 31.2 kbps	0D
00,00	;If EQM > than ##,##, choose 33.6 kbps	0E

10b. If in answer or originate mode at **3200 or 3000** symbol rate:

HighByte,MidByte (Hex)	EQM3200/3000Table: Receive Data Rate	By writing this hex value to 2E4h
07,3A	;If EQM > than ##,##, choose 12.0 kbps	05
04,B0	;If EQM > than ##,##, choose 14.4 kbps	06
02,EE	;If EQM > than ##,##, choose 16.8 kbps	07
01,C2	;If EQM > than ##,##, choose 19.2 kbps	08
01,09	;If EQM > than ##,##, choose 21.6 kbps	09
00,92	;If EQM > than ##,##, choose 24.0 kbps	0A
00,40	;If EQM > than ##,##, choose 26.4 kbps	0B
00,2E	;If EQM > than ##,##, choose 28.8 kbps	0C
00,00	;If EQM > than ##,##, choose 31.2 kbps	0D*

* Value 0Dh not valid if symbol rate = 3000.

Note: In steps 10a or 10b, 33.6 kbps (value of 0Eh) should only be selected if the symbol rate is 3429. If the average EQM is very good, yet the symbol rate is only 3200, then a maximum of 31.2 kbps should be selected (value of 0Dh). If the symbol rate is 3000, then a maximum of 28.8 kbps should be selected (value of 0Ch). If the user has limited the data rate through the rate mask to a value less than the one selected in steps 10a/b, the lower rate mask value will prevail.

Steps 10a/b select the desired receive rate and modify it just prior to the transmission of the MP sequence. The EQM windows listed may be altered as desired.

Table 14-3. ARA Values

Address (Hex)	2E3h Value (Corresponding Symbol Rate in Baud)				
	5 (3429)	4 (3200)	3 (3000)	2 (2800)	0 (2400)
3B0	20	20	20	20	20
3B1	18	18	16	10	0C
3B2	10	10	0D	07	07
3B3	0A	0A	08	04	03
3B4	08	08	03	02	02
3B5	05	05	02	01	01
3B6	03	03	01	00	00
3B7	02	02	00	A0	35
3B8	01	01	A0	40	05
3B9	00	00	50	10	01
3BA	4A	30	03	03	00
3BB	15	02	02	01	00
3BC	03	02	01	00	00
3BD	01	01	00	00	00
3BE	01	00	00	00	00
3BF	00	00	00	00	00

14.2 RETRAINS AND RENEGOTIATIONS

Retrains and rate renegotiations are handled in the same manner as in V.34 using the RTRN and RREN bits, respectively. For retrains, the EARC bit should be left on to allow the modem to select the highest rate possible under the current conditions. For rate renegotiations, the EARC bit should be turned off and the desired receive rate should be written to CONF (9Xh on client modem, CXh on server modem) followed by the setting of RREN. The rate masks may also be used. The CTS bit will turn off during the retrain or rate renegotiation process and will turn back on when completed.

The V.34 mask address at 383h/382h, which is used in V.34 mode, can still be used on the client modem when connected in K56flex but will only affect the transmit rate (the server modem's receive rate). When connecting in K56flex mode, it's preferable to use the new rate masks at 604h and 605h. These masks may also be used in V.34 and allow the user to manipulate the transmit and receive speeds independently as opposed to the 383h/382h mask which limits both the transmit and receive rate when used. Note, however, the new masks only limit the maximum data rate and do not allow the user to selectively disable data rates (see Table 14-1).

14.3 ROBBED BIT SIGNALING AND DIGITAL PAD DETECTION

The diagnostic status locations for robbed bit signaling (RBS) and digital pad detection algorithms are:

Client Modem

6E3h RBS pattern detected before pad (bits 0-5).
6E4h RBS pattern detected after pad (bits 0-5).
6E8h Number of robbed bits per frame of 6.
6E9h Receive data rate drop due to RBS.
6EAh RBS pattern detected (bits 0-5) (6E3h ORed with 6E4h).
6F3h Digital pad detection.

Server Modem

6ECh Number of robbed bits per frame of 6.
6EDh Receive data rate drop due to RBS.
6EEh RBS pattern detected (bits 0-5).

Definitions

Number of robbed bits per frame of 6 - Indicates the number of robbed bits detected for every 6 bytes of PCM data. Value is valid when RSLD = 1 or at completion of a retrain (CST = 1).

Receive data rate drop due to RBS - Depending on the number of bits robbed per every 6 bytes , the receive data rate will automatically be reduced. This data rate reduction value is reported as 02h, 04h, 06h or 08h for 2k, 4k, 6k or 8k bps. The robbed bit signaling does not affect the EQM readings used during phase 4 for the data rate selection. The host should

select the data rate based on EQM as always. Upon connecting, the true connect speed will be the host selected speed shown in 2E4h (or CONF value) minus the data rate drop due to RBS as shown in 6E9h (client) or 6EDh (server).

As an example: EQM measurements during phase 4 indicate a 50k bps data rate should be selected. The host therefore writes 0Ah in 2E4h. When RLSD = 1, the host checks either 2E4h or CONF to confirm the selected rate and then checks the data rate drop due to RBS in 6E9h (client) or 6EDh (server). If the data rate drop indicates 04h, then the receive data rate is actually 50k - 4k or 46k bps, which is what should be reported as the connect message.

The host should not write a 2E4h data rate value higher than indicated by EQM, no matter what the rate loss due to RBS is. Both the reduction due to RBS and the host data rate limit then need to be considered.

Other examples with the AT+MS command (host limited speeds):

Ex: +MS = 40000, 46000, EQM indicates 50k possible:

If loss due to RBS were 0k, write CONF=46k and print 46k
If loss due to RBS were 2k, write CONF=48k and print 46k
If loss due to RBS were 4k, write CONF=50k and print 46k
If loss due to RBS were 6k, write CONF=50k and print 44k

Same +MS but EQM indicates 44k possible:

If loss due to RBS were 0k, write CONF=44k and print 44k
If loss due to RBS were 2k, write CONF=44k and print 42k
If loss due to RBS were 4k, write CONF=44k and print 40k
If loss due to RBS were 6k, fallback to V.34 because actual data rate is less than indicated by EQM.

In other words the EQM speed - the RBS data rate loss = the max possible speed within the limits of the +MS setting. If the resulting true speed is less than the lowest +MS setting, fallback to V.34.

Any fall forward or fallback decisions during a K56flex connection should continue to be based on the EQM value at 810h and the requested data rate value in 2E4 should be increased or decreased from its current value. The purpose of the "data rate drop due to RBS" value is for reporting the actual speed in the connect message. It does not affect the data rate selection process. This value is valid when RSLD = 1 or at completion of a retrain (CST = 1).

RBS pattern detected - Robbed bit signaling systems may rob one least significant bit from one byte out of every 6 bytes of data. If the signal is routed through more than one robbed bit system, there can potentially be more than one bit robbed per every 6 bytes. The RAM Downloadable devices can handle up to 6 robbed bits per 6 bytes (typically, no more than 1-3 bits are robbed in total on a given call). The modem detects the number a robbed bit per 6 bytes and indicates the pattern in the 6 lower bits of the addresses shown above. A value of 05h (0000 0101) would indicate that 2 bits are being robbed out of every 6 bytes and that the first and third bytes were the bytes with the robbed bit. The pattern itself has no real significance other than for testing purposes. The number of bits set in the lower 6 bits of this value simply indicates the total number of robbed bits out of every 6 bytes. The total number of set bits should correspond to the "number of robbed bits" value in 6E8h (client) and 6ECh (server). The difference is that the RBS pattern value is available when SECTXB>40h.

Digital pad detection - Bit 7 = 1 indicates 6 dB pad, bit 6 = 1 indicates 3 dB pad, and bits 7 and 6 = 0 indicates no digital pad. This value is available when SECTXB>40h. This value is used for information only.

Bit 7 = 1 indicates 6 dB pad, bit 6 = 1 indicates 3 dB pad and bits 7 and 6 = 0 indicates no digital pad. This value is available when SECTXB>$40. This value is used for information only.

15. RAM MODULE DOWNLOADING

The MDP uses executable code modules (called RAM modules) downloaded from the Host during normal operation to configure the MDP and to add or modify MDP functions.

15.1 DOWNLOADING CAN BE INITIATED BY THE HOST OR THE MDP

15.1.1 Host Requested Download Scenario

Before setting NEWC to configure to a new mode, the Host may initiate a download to the MDP. For example, after POR, Hardware Reset, or Software Reset, the Host would download the RAM modules required for K56flex, before starting a K56flex connection.

15.1.2 MDP Requested Download Scenario

During a connection sequence, when the RAM modules in SRAM are not correct for the connection type, the MDP will request a download from the Host. For example, if the MDP SRAM is loaded with RAM modules for K56flex, but the connection type indicated in the V.8 sequence is V.FC, then the MDP will request the Host to download the RAM modules for V.FC before the connection sequence can continue.

15.2 DOWNLOAD ARCHITECTURE

RAM modules are downloaded into two SRAM sections:

- 12K x 8 section for Control Code, called the CTL SRAM.
- 12K x 8 (3K x 32) section for DSP Code, called the SPX SRAM.

Only the code necessary to run the selected mode is required to be in the SRAM, but code for other modes can also be in SRAM at the same time, as long as they do not overlap the same SRAM address space. The starting and ending address for each RAM module is included in the RAM files.

The RAM_Vector_Table must be downloaded last, i.e., after all other RAM modules are downloaded to the SRAM.

The MDP ROM contains code common to all modes, and code for the following specific modes: V.34, V.32, V.22, V.17, V.29, V.27, V.8 and all FSK modes.

Notes:

After POR, Hardware Reset, or Software Reset, but before K56flex RAM module and RAM_Vector_Table RAM module download, the MDP executes V.34 mode from MDP ROM since the RAM_Vector_Table are initialized to point to ROM.

The K56flex RAM module must be downloaded in order to operate in K56flex mode.

After downloading the K56flex RAM module and RAM_Vector_Table RAM module, the MDP executes K56flex and V.34 modes from MDP SRAM since the RAM_Vector_Table now points to SRAM.

15.2.1 Download Time

Assuming the Host Microprocessor is running faster than the MDP (i.e., the MDP is never waiting for the Host to download a data byte), the time to download 12K bytes into the CTL SRAM, is about 14.5 ms (plus some small handshake overhead), and the time to download 12K bytes into the SPX SRAM, is about 11.3 ms. Therefore, the worst case time to download all required RAM modules is less than 30 ms.

15.2.2 Download Protocol

The download protocol uses MDP Interface Memory Register ABCODE (14h:0-7) and a 2-byte RAM address register called RAM_adrcnt (MSB uses SECTXB 17h:0-7, and LSB uses SECRXB 16h:0-7) to control the downloading process.

The Host can request a download anytime by writing a download request code into ABCODE, and the MDP can also request a download by writing a download request code to ABCODE. The download control codes are defined in Table 15-1.

Table 15-1. ABCODE Download Control Codes and Definitions

Code (Hex)	Description
Written by MDP, checked by Host:	
40	MDP requests Host to download Rockwell K56flex RAM module.
42	MDP requests Host to download SPK RAM module.
Written by Host, checked by MDP:	
4E	Host requests download, then execute at 1400, 1401. This mode provides the flexibility for dynamic download-and-run on the fly.
4F	Host requests download to CTL SRAM, then return. This request is used before configuring NEWC to a new mode
5E	Host terminates current download process and requests another download.
5F	Host requests download to SPX SRAM.

15.3 DOWNLOAD FILE FORMAT

15.3.1 File Contents

RAM modules for the CTL SRAM section and for the SPX SRAM section are contained in two separate binary files:

Server Files are: SCTL###.RAM and SSPX###.RAM , where ### = Revision Number

Client Files are: CCTL###.RAM and CSPX###.RAM, where ### = Revision Number

Both RAM files have the same binary file format.

The following conventions are used:

byte	8-bits
word	16-bits, LSB first, MSB last
dword	32-bits, LSB first, MSB last
ASCII	sequence of bytes, terminated with a byte containing binary zero

The first byte of the RAM file is byte number 0 (zero).

The RAM file starts with an 8-byte header which has the format:

4 bytes	'DRAM'	indicates a RAM module download file (ASCII; e.g., 4452414D)
1 word	version	contains the version number of the RAM file type (always 0101)
1 word	nram	indicates the number of RAM descriptors following (binary; e. g., 0400 for 4 descriptiors)

Following the header are the RAM module descriptors, each of which have the following format:

1 word	mod	RAM module ID word (binary; e.g., 00EAh for RAM_Vector_Table_id)
1 word	id	RAM download ID word (binary; e.g., 00EAh for RAM_Vector_Table_id)
1 word	type	CTL SRAM download (0000h) or SPX SRAM download (8000h) (binary)
1 byte	crc	8-bit CRC code for the RAM module (binary; e.g., DCh)
1 byte		reserved (e.g., 00h)
1 dword	start	SRAM starting address for download (binary; 00001000h for RAM_Vector_Table)
1 dword	end	SRAM ending address for download (binary; 000013E1h for RAM_Vector_Table)
1 dword	len	number of bytes to download (binary; 000003E1h for RAM_Vector_Table) **[CTL file only]**
1 dword	len	number of dwords to download (binary; 000003E1h for RAM_Vector_Table) **[SPX file only]**
1 dword	len	length of data (number of bytes) to download (binary; 000003E1h for RAM_Vector_Table)
1 dword	pos	offset of first data byte (from start of the RAM file) (binary; e.g., 000000B5h for RAM_Vector_Table)
1 dword	next	offset to next descriptor (from start of the RAM file) (binary; e.g., 0000003Ah for RAM_Vector_Table)
asciiz	name	name of the section which contains the data (ASCII, e.g., 'RAM_Vector_Table')

The CRC is calculated as follows:

```
byte crc,*p;
dword l;
for(crc=0,p=file[pos],l=len;l--;p++)
crc=(crc<<1)+((crc&0x80)>>7)+*p;
```

15.3.2 Client RAM Files

CTL RAM File

The CTL RAM file contains the following modules:

Module Name	Module ID No.
RAM_Intercept_Vectors	$EA
General_RAM_code	$EB
Modes_RAM_code	$EC
K56_RAM_code	$40
SPK_RAM_code	$42

SPX RAM File

The SPX RAM file contains the following modules:

Module Name	Module ID No.
B0_RAM_CODE_VECTORS	$F0
PCMRX_RAMCODE	$F7
BAUD_RAMCODE	$F2
SPKPHONE_RAMCODE	$F9
PCMROM_RAM_SECTION	$F8
V61_RAMCODE	$FE
ENCODER_RAMCODE	$FD

15.4 RAM FILES USAGE INSTRUCTIONS

15.4.1 Client Modem

V.61 only operates between two clients. The SPX only allows download after RESET. If the user wants to download V.61 or speakerphone after V.8, a software reset must be done first before attempt to download RAM codes to the SPX. A software reset must also be done after using V.61 or speakerphone modes before downloading other modules.

15.4.2 To Run K56flex

To run K56flex, download the following CTL and SPX modules (RAM_Intercept_Vectors and B0_RAM_CODE_VECTORS must be the last modules downloaded within the CTL and SPX downloads, respectively):

CTL Modules	
Module Name	**Module ID No.**
Modes_RAM_code	$EC
General_RAM_code	$EB
K56_RAM_code	$40
RAM_Intercept_Vectors	$EA
SPX Modules	
Module Name	**Module ID No.**
BAUD_RAMCODE	$F2
ENCODER_RAMCODE	$FD
PCMRX_RAMCODE	$F7
PCMROM_RAM_SECTION	$F8
B0_RAM_CODE_VECTORS	$F0

15.4.3 To Run V.61 or Speakerphone

To run V.61 or Speakerphone, download the following CTL and SPX modules (RAM_Intercept_Vectors and B0_RAM_CODE_VECTORS must be the last modules downloaded within the CTL and SPX downloads, respectively):

CTL Modules	
Module Name	**Module ID No.**
Modes_RAM_code	$EC
General_RAM_code	$EB
SPK_RAM_code	$42
RAM_Intercept_Vectors	$EA

SPX Modules	
Module Name	**Module ID No.**
BAUD_RAMCODE	$F2
ENCODER_RAMCODE	$FD
SPKPHONE_RAMCODE	$F9
V61_RAMCODE	$FE
B0_RAM_CODE_VECTORS	$F0

15.4.4 Considerations

If a required RAM module is not present in RAM, the MDP will request the Host to download it before execution.

The Host must not download a set of modules that overlap in the SRAM address space. Also, the Host must update the RAM_Vector_Table to point to RAM modules currently loaded in SRAM.

Note: When the Host requests a download, the MDP will overwrite the SRAM specified by the Host, without checking Module IDs.

Interface Memory Register Definitions

ABCODE = 14h

RAM_adrcnt low byte = 16h

RAM_adrcnt high byte = 17h

RAM_CRC = 16h (only valid after ABCODE=00 or 5Eh)

15.5 DOWNLOAD PROCEDURES

15.5.1 Host Requested Download Procedure

The download process should only be requested by the Host while the MDP is IDLE (i.e., not "on-line" connected to another modem).

After POR, Hardware Reset, or Software Reset, the MDP automatically loads the default values into the RAM_Vector_Table, and clears SRAM addresses 1400h and 3000h.

To load RAM modules into the MDP, the Host requests a download as follows:

1. The Host writes ABCODE=4Fh (14h:0-7) for CTL SRAM download or 5Fh for SPX SRAM download. **Note:** Download order can be CTL SRAM before SPX SRAM, or SPX SRAM before CTL SRAM.
2. The Host waits for the MDP to acknowledge it is ready to accept new data, by reading Register 1Bh (the MDP copies the contents of ABCODE into Register 1Bh when it is ready to accept data).
3. The Host writes the 2-byte starting address, LSB **first**, from the RAM module descriptor in the RAM file, into RAM_adrcnt (MSB in SECTXB 17h:0-7 and LSB in SECRXB 16h:0-7). **Note:** If the MDP does not receive data from the Host within 30 seconds after writing the ABCODE to Register 1B, the MDP aborts the download by resetting ABCODE = 00h.
4. The Host reads each byte from the selected module in the RAM file and writes them to TBUFFER, while the TXFNF bit is 1 ($0Dh:1). During download, Register 1Bh is continuously updated with the DMA buffer status, but the Host should use the FIFO TXFNF bit because the DMA buffer is just an extension of the FIFO.

5. After the last byte for the selected module is written to TBUFFER, the Host writes ABCODE = 00h if this is the last module to download, or the Host writes ABCODE = 5Eh if there is another module to download.
6. The Host waits for Register 17h to be FFh, then reads the CRC byte from Register 16h. If the CRC value matches the CRC byte in the RAM file for the selected module, the module was correctly downloaded. If the CRC does not match, the module was incorrectly loaded; the Host should then issue a Reset (either Hardware or Software), and repeat the Download Procedure. After a module download, the MDP restores the contents of Register 1Bh, and resumes normal operation. Registers 16h and 17h are not restored.
7. If, at step 5, the Host had written ABCODE = 5Eh, indicating there is another module to download, then the Host repeats the Download Procedure, beginning at step 1, by writing ABCODE = 4Fh or 5Fh.
8. If all modules have been downloaded, the Host sets CONF as required and NEWC=1, to configure the MDP to a mode supported by the downloaded modules.

15.5.2 MDP Requested Download Procedure

After the Host sets NEWC = 1, or during a V.8 sequence, or during Automode, the MDP checks for the presence of the required RAM modules in SRAM before attempting the connection. If the mode specified in the CONF Register, or as a result of the V.8 or Automode sequences, is not supported by the required RAM modules present in SRAM, the MDP will request the Host to download the appropriate RAM modules as follows:

1. The MDP initializes RAM_adrcnt to FFFFh and writes the appropriate download request into ABCODE (see Table 15-1).
2. The Host reads the ABCODE value, and locates the requested RAM module in the appropriate RAM file.
3. The Host writes the 2-byte starting address, LSB byte **first**, for the requested module into RAM_adrcnt (MSB in SECTXB 17h:0-7, and LSB in SECRXB 16h:0-7). There is a 30-second timeout before the MDP aborts the download by resetting ABCODE = 00h.
4. The Host reads each byte from the selected module in the RAM file and writes them to TBUFFER, while the TXFNF bit is 1 (0Dh:1). During download, Register $1B is continuously updated with the DMA buffer status, but the Host should use the FIFO TXFNF bit because the DMA buffer is just an extension of the FIFO.
5. After the last byte for the selected module is written to TBUFFER, the Host writes ABCODE = 00 if this is the last module to download, or the Host writes ABCODE = 5Eh if there is another module to download.
6. The Host then waits for Register 17h to be FFh and reads the CRC byte from Register 16h. If the CRC value matches the CRC byte in the RAM file for the selected module, the module was correctly downloaded. If the CRC does not match, the Host should issue a Reset (either Hardware or Software), and repeat the Download Procedure. After a module download, the MDP restores the contents of Register $1B, and resumes normal operation. Registers 16h and 17h are not restored.
7. If, at step 6, the Host had written ABCODE = 5Eh, indicating there is another module to download, then the Host would use the Host Request Download Procedure, beginning at step 1, by writing ABCODE = 4Fh or 5Fh. There is a 30-second timeout for the Host to write to ABCODE before the modem aborts the download. The MDP will clear ABCODE if it decides to abort the download.
8. In the case where the Host requests a download-and-run (ABCODE = 4Eh), the download procedure is the same as described above, except when finished, the MDP will jump to the address contained in 1400h (LSB) and 1401h (MSB). This feature is currently not used.

15.6 DOWNLOAD ABORT

15.6.1 Host Abort of MDP Requested Download

The Host can abort a download request initiated by the MDP by writing ABCODE = 00h.

The MDP will then perform a soft reset and restart with CONF = 76h (V.32bis).

15.6.2 Host Abort of Host Requested Download

The Host can abort its own download request by either writing ABCODE=00h or setting NEWC = 1.

The MDP will reset ABCODE = 00 and will continue operation as if the download request was never issued.

The Registers 17h and 16h which contain the starting address will be FFh after the download abort. Only Register 1Bh is restored. In V.32 mode, Registers 17h and 16h are cleared after V.32 initialization.

Note: When the MDP is requesting a download, and NEWC is set to 1, the Host can not request another download (with ABCODE = 5Eh), because the NEWC bit will cause the MDP to abort the next download. The Host must finish the download request with an ABCODE = 00h before requesting another download using ABCODE = 4Fh or 5Fh.

15.6.3 Download Abort due to Timeout

If the Host does not enter a starting address for download within approximately 30 seconds from the download request, the modem will perform a soft reset and restart with CONF = 76h (V.32bis). To disable the 30-second timer (not recommended), the Host can set bit 87h:5 = 1, and the MDP will wait for Host download forever.

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INSIDE BACK COVER NOTES

Worldwide Headquarters
Rockwell Semiconductor Systems
4311 Jamboree Road,
P.O. Box C
Newport Beach, CA 92658-8902
Phone: (714) 221-4600
Fax: (714) 221-6375

For more information:
Call 1-800-854-8099
International information:
Call 1-714-221-6996

URL Address:
http://www.rss.rockwell.com
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literature@rss.rockwell.com

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Santa Clara, CA 95051
Phone: (408) 249-9696
Fax: (408) 249-7113

US Los Angeles
Rockwell Semiconductor Systems
1000 Business Center Circle
Suite 215
Thousand Oaks, CA 91320
Phone: (805) 376-0559
Fax: (805) 376-8180

US Southwest
Rockwell Semiconductor Systems
5000 Birch Street
Suite 400
Newport Beach, CA 92660
Phone: (714) 222-9119
Fax: (714) 222-0620

US North Central
Rockwell Semiconductor Systems
Two Pierce Place
Chancellory Park
Suite 810
Itasca, IL 60143
Phone: (630) 773-3454
Fax: (630) 773-3907

US South Central
Rockwell Semiconductor Systems
2001 North Collins Blvd
Suite 103
Richardson, TX 75080
Phone: (972) 479-9310
Fax: (972) 479-9317

US Northeast
Rockwell Semiconductor Systems
239 Littleton Road
Suite 4A
Westford, MA 01886
Phone: (508) 692-7660
Fax: (508) 692-8185

US Southeast
Rockwell Semiconductor Systems
3500 Parkway Lane, Suite 415
Norcross, GA 30092
Phone: (770) 246-8283
Fax: (770) 246-0018

US Florida/South America
Rockwell Semiconductor Systems
One Prestige Place
2600 McCormick Drive
Suite 350
Clearwater, FL 33759
Phone: (813) 799-8406
Fax: (813) 799-8306

US Mid-Atlantic
Rockwell Semiconductor Systems
Princeton Pike Corporate Center
993 Lenox Drive, Suite 200
Lawrenceville, NJ 08648
Phone: (609) 219-7462
Fax: (609) 895-2666

European Headquarters
Rockwell Semiconductor Systems
S.A.S.
Les Taissounieres B1
1680 Route des Dolines
BP 283
06905 Sophia Antipolis Cedex
France
Phone: (33) 4 93 00 33 35
Fax: (33) 4 93 00 33 03

Europe Central
Rockwell Int'l GmbH,
Rockwell Semiconductor Systems
Branch
Paul-Gerhardt-Allee 50 a
81245 München
Germany
Phone: (49-89) 829-1320
Fax: (49-89) 834-2734

Europe Mediterranean
Rockwell Semiconductor Systems
c/o Rockwell Automation S.r.l.
Via G. Di Vittorio, 1
20017 Mazzo Di Rho (MI)
Italy
Phone: (39 2) 93179911
Fax (39 2) 93179913

Europe North
Rockwell Semiconductor Systems, Ltd.
Berkshire Court
Western Road
Bracknell
Berkshire RG12 1RE
England
Phone: 44 (0) 1344 486444
Fax: 44 (0) 1344 486555

Europe North (Satellite)
Rockwell Semiconductor Systems
Israel, Ltd. (RSSI)
11 Galgaley Haplada Street
P.O. Box 12660
Herzlia 46733
Israel
Phone: (972) 9 9524000
Fax: (972) 9 9573732

Europe South
Rockwell Semiconductor Systems
S.A.S.
Tour GAN
Cedex 13
92082 Paris La Défense 2
France
Phone: (33) 1 49 06 39 80
Fax: (33) 1 49 06 39 90

APAC Headquarters
Rockwell Int'l Manufacturing Pte Ltd
1 Kim Seng Promenade
#09-01 East Tower
Great World City
Singapore 237994
Phone: (65) 737-7355
Fax: (65) 737-9077

Australia
Rockwell Australia Pty Limited
Suite 603, 51 Rawson Street
Epping, NSW 2121
Australia
Phone: (61-2) 9869 4088
Fax: (61-2) 9869 4077

China
Rockwell Semiconductor Systems
Worldwide, Inc.
Shanghai Representative Office
LT Square Building, Suite 3002
500 Chengdu North Road
Shanghai 200003 P.R.C.
Phone: 86-21-6361-2515
Fax: 86-21-6361-2516

Hong Kong
Rockwell Int'l (Asia Pacific) Ltd.
13th Floor, Suites 8-10,
Harbour Centre
25 Harbour Road
Wanchai,
Hong Kong
Phone: (852) 2 827-0181
Fax: (852) 2 827-6488

India
Rockwell Int'l Overseas Corporation
Regional Office - South Asia
Capital Trust House
47 Community Centre
Friends Colony
New Delhi - 110 065
India
Phone: (91-11) 692-4780
Fax: (91-11) 692-4712

Korea
Rockwell Collins Int'l, Inc.
Room No. 1508
Korea Textile Centre Building
944-31, Daechi-3dong
Kangnam P.O. Box 2037
Kangnam-ku
Seoul
Korea
Phone: (82-2) 565-2880
Fax: (82-2) 565-1440

Taiwan Headquarters
Rockwell Int'l Taiwan Company, Ltd.
Room 2808 International Trade Bldg.
333, Keelung Road, Section I
Taipei,
Taiwan
10548 ROC
Phone: (886-2) 720-0282
Fax: (886-2) 757-6760

Japan Headquarters
Rockwell Int'l Japan Co., Ltd.
Shimomoto Bldg
1-46-3 Hatsudai, Shibuya-ku
Tokyo, 151
Japan
Phone: (81-3) 5371 1520
Fax: (81-3) 5371 1501

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Semiconductor Systems