HITACHI SEMICONDUCTOR TECHNICAL UPDATE

DATE	9th April, 1999	No.	TN-SH7-143 A/E
THEME	Supported DMA Transfers		
CLASSIFICATION	☐ Spec. change ☐ Limitation on Use ☑ Supplement of Documents		
PRODUCT NAME	HD6417091BP200, HD6417091RBP200, HD6417750BP200, HD6417750F167, HD6417750VF128		
REFERENCE DOCUMENTS	SH7091 Hardware Manual, SH7091 Programming Manual, SH7750 Hardware Manual, SH7750 Programming Manual	Effective Date	eternity
		From	

1. Supported DMA Transfers

Some of the combinations of DMA Transfer with external request described in the SH-4 Hardware Manual are limited on use. Supported combinations depend on DMAC normal-mode and on-Demand Data Transfer mode.

1.1 In DMAC Normal-mode

In DMAC Normal-mode, Supported DMA Transfers with External request is as follows(Table 1.).

Table 1. Supported DMA Transfers with External Request (Normal-mode)

	Type of Transfer(Usable Memory Interface)		Address Mode	Usable Channels
	Transfer Source	Transfer Destination		
1	Synchronous DRAM	External device with DACK	Single	0, 1
2	External device with DACK	Synchronous DRAM	Single	0, 1
3	SRAM*1, DRAM	External device with DACK	Single	0, 1
4	External device with DACK	SRAM*1, DRAM	Single	0, 1
5	Synchronous DRAM	SRAM*1, MPX, PCMCIA *	Dual	0, 1
6	SRAM*1, MPX, PCMCIA *	Synchronous DRAM	Dual	0, 1
7	SRAM*1, DRAM, PCMCIA, MPX	SRAM*1, MPX, PCMCIA *	Dual	0, 1
8	SRAM*1, MPX, PCMCIA *	SRAM*1, DRAM, PCMCIA, MPX	Dual	0, 1

* : Setting DACK output in Dual Address Mode

SRAM*1: SRAM, Byte control SRAM, Burst-ROM

Usage notes:

(1) Usable Memory Interface with Single Address Mode Transfer is SRAM, Byte control SRAM, Burst-ROM, DRAM, Synchronous DRAM.

(2) In Dual Address Mode Transfer, it is possible to set DACK output for the following interface:
SRAM, Byte control SRAM, Burst-ROM, PCMCIA, MPX.

1.2 In on-Demand Data Transfer mode

In DDT-mode, Supported DMA Transfers with External Requests is as follows (Table 2.).

Table 2. Supported DMA Transfers with External Requests (DDT-mode)

	Type of Transfer(Usable Memory Interface)				Address Mode	Usable Channels
	Transfer Source		Transfer Destination			
1	Synchronous DRAM (64bit width)		External device with DACK		Single	0, 1, 2, 3
2	External device with DACK		Synchronous DRAM (64bit width)		Single	0, 1, 2, 3
3	Synchronous DRAM		SRAM*1, MPX, PCMCIA	*	Dual	1, 2, 3
4	SRAM*1, MPX, PCMCIA	*	Synchronous DRAM		Dual	1, 2, 3
5	SRAM*1, DRAM, PCMCIA, MPX		SRAM*1, MPX, PCMCIA	*	Dual	1, 2, 3
6	SRAM*1, MPX, PCMCIA	*	SRAM*1, DRAM, PCMCIA, MPX		Dual	1, 2, 3

* : Setting DACK output in Dual Address Mode

SRAM*1: SRAM, Byte control SRAM, Burst-ROM

Usage notes:

(1) Usable Memory Interface with Single Address Mode Transfer is Synchronous DRAM, and Supported Synchronous DRAM bus-width is 64bit.

(2) In Dual Address Mode Transfer, it is possible to set DACK output for the following interface:
SRAM, Byte control SRAM, Burst-ROM, PCMCIA, MPX.