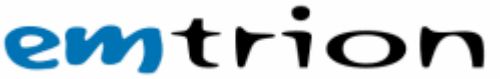
HiCO.SH7760

Processor Board with SH7760

HiCO.SH7760-DOC
Hardware Description



Revision No.	Changes	Date
1	First edition	2004-04-20 / Bue
2	Connector J105 changed, new connector J95, range and impedance of the analog output corrected, name of the device changed to HiCO.SH7760	2004-09-20 / Bue

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1. Introduction

The HiCO.SH7760 processor board is a CPU module based on the SH7760 processor from Renesas. Depending on the version ordered, the HiCO.SH7760 processor board comes with a 16 … 64 MB on-board-Flash and 64 MB of SDRAM. In addition to the processor and memory, it is equipped with a 10/100-Mbps Ethernet controller and a USB function controller.

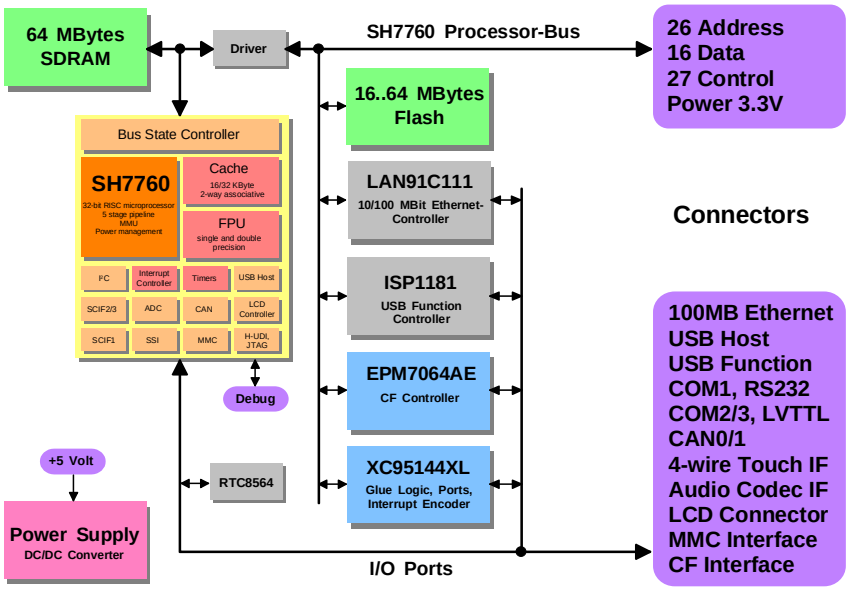
Most interfaces connect to both local connectors and to the connectors on the carrier module, the so-called BASE. The connectors to the BASE comply with the HiCO.nect standard from emtrion.

The local connectors are arranged so that HiCO.SH7760 may also be used as a reduced variant, i.e., as CORE module without having any connectors, the HiCO.nect plug connector excepted.

Furthermore, the HiCO.SH7760 processor board allows the installation of various standard operating systems such as Windows CE, Linux and QNX.

HiCO.SH7760 can be run standalone and only requires a +5V power supply to operate.

1.1. Block Diagram



2. Before Installing the Module

Please read the following notes prior to installing the HiCO.SH7760 processor module. They apply to all ESD (electrostatic discharge) components:

- Before installing the module it is recommended that you discharge yourself by touching a grounded object.
- Be sure all tools required for installation are electrostatic discharged as well.
- Before installing (or removing) a board, remove the power cable from your mains supply.
- Handle the board with care and try to avoid touching its components or tracks.

3. Functional Description

3.1. Processor

The HiCO.SH7760 processor board uses the SH7760 processor type from Renesas [1], a 32−bit RISC SH4 family processor.

In addition to the actual CPU core, this processor provides many practical features such as:

- Single and double precision FPU, IEEE754 compatible
- MMU with 4 GB of virtual address space
- 16-KB instruction cache and 32-KB operand cache, 2-way associative
- Interrupt controller with 15 levels
- Bus state controller with programmable timing
- Clock generator with power-down functions
- 8-channel DMA controller with two external inputs
- 3 32-bit auto-reload timers
- 3 UARTs
- 2 SSI and AC97 interfaces for Audio CODECs
- 2 I^2C bus channels
- MMC controller
- 2 CAN channels in accordance with CAN specification 2.0B
- SPI master/slave
- USB host according to USB 1.1
- LCD controller, max. 1024 * 1024 pixels, STN- and TFT displays
- 4-channel 10-bit AD converter
- H-UDI debug interface

The processor operates in the little endian mode, which allows you to make use of PC-compatible interfaces such as a CF card and operating systems like Windows CE.

The processor's input clock is 16 MHz. The internal PLLs are set to mode 3, according to the multiplicators 12-4-2. This means that the processor runs at 192 MHz, the bus interface at 64 MHz and the internal peripherals at 32 MHz.

3.2. Bus Interface

The SH7760 processor provides 7 areas with 64 MB address space each at data widths from 8 – 32 bits. The address usage is as follows:

Area	Function	Bus Width	Address Region
0	16 … 64 Mbyte Flash	32/8-bit ***	A0000000 – A3FFFFFF
1	On-board peripherals such as Ethernet, USB function, IO ports	16-bit	A4000000 – A7FFFFFF
2	External expansions	16-bit	A8000000 – ABFFFFFF
3	64 Mbyte SDRAM	32-bit	AC000000 – AFFFFFFF
4	External expansions	16-bit	B0000000 – B3FFFFFF
5	External expansions, e.g. ISA bus	8- / 16-bit	B4000000 – B7FFFFFF
6	PC card range	8-/ 16-bit	B8000000 – BBFFFFF

*** Enabling the BOOT8# signal allows you to boot from an external 8-bit PROM via HiCO.nect.

Areas 0, 1, 3 and 6 were programmed according to the requirements of the HiCO.SH7760 processor board. Areas 2, 4 and 5 were programmed with the slowest timing.

3.3. Interrupts

HiCO.SH7760 comes with an interrupt encoder that analyzes all interrupt sources, prioritizes them and outputs the interrupt with the highest priority to the processor as a 4-bit IRL code. For this, the processor's interrupt controller has to be programmed for level-encoded interrupt requests.

There are 7 local interrupt sources with these levels:

Source	Interrupt Level
Ethernet, LAN91C111	15
USB Function, ISP1181	12
CF Interface	9
Touch Pen Down/Up	6
MMC Card Detect Change	4
COM1, DCD Change	3
RTC	1

In addition, a 4-bit code can be applied by another external interrupt encoder via the J1 connector of the HiCO.nect plug connector. The codes are in accordance with the IRL coding of the processor's interrupt controller. The following values are possible:

External Interrupt Code	Interrupt Level
0x1	14
0x2	13
0x4	11
0x5	10
0x7	8
0x8	7
0xA	5
0xD	2
0xF	No interrupt

The 7 levels of the local interrupts cannot be provided via HiCO.nect, they will be ignored.

All interrupts can be disabled via two 8-bit mask registers. The two registers are located at the addresses 0xa4000000 (low byte) and 0xa4000002 (high byte), respectively. The following assignment applies:

Register	Data Bit	Meaning
0xa4000002	D[7..0] = IRQ[15..8]	1 = IRQ is disabled 0 = IRQ is enabled
0xa4000000	D[7..1] = IRQ[7..1] D0 = unused	1 = IRQ is disabled 0 = IRQ is enabled

All bits of both mask registers will be set to 1 upon reset. This means that all interrupts are disabled after a reset. The mask registers can be read back.

In addition to the normal interrupts, an NMI input is available. This input is not used on the HiCO.SH7760 processor board. It may be used for external functions via the J1 connector of HiCO.nect.

3.4. DMA

The DMA channels 0 and 1 are available to external devices.

DMA channel 0 is connected to the ISP1181 USB function controller. DMA channel 1 is connected to HiCO.nect's J1 connector and is thus available to external functions on the external BASE board.

3.5. RAM

A 64-MB SDRAM is provided as main memory. This RAM is located in the address range 0xAC000000 through 0xAFFFFFFF in area 3.

The memory consists of two 256-Mbps RAMs, type 4M*16*4, and are operated in parallel on a 32-bit wide data bus. They are clocked at 64 MHz and run with CAS latency 2.

3.6. Flash

A 16 … 64 MB flash memory may be used as program memory. The flash devices are located from 0xA0000000 ... 0xA3FFFFFF in area 0. Two StrataFlash memories in the BGA64 package are installed. Both flash memories are connected in parallel to a 32-wide data bus.

Signal BOOT8# on HiCO.nect's J1 connector serves to switch area 0 to an 8-bit wide data bus in order to boot from an external PROM. In this case, the on-board flash devices are disabled.

3.7. Serial Ports COM1 … COM3

The SH7760 processor has three serial ports with integrated FIFO, SCIF0, SCIF1 and SCIF2. All ports may be operated both asynchronously and synchronously. The ports SCIF1 and SCIF2 provide the handshake lines RTS and CTS.

The lines of port SCIF0 and SCIF1 are connected to J3 of the HiCO.nect plug connector and will need to be configured by external drivers. The connection is as follows:

Processor Port	HiCO.nect Port
SCIF0	COM3: RXD, TXD
SCIF1	COM2: RXD, TXD, RTS, CTS

SCIF2 has been implemented as a complete RS232 port COM1 on the processor board. Using additional logic, the handshake signals DCD and DTR can be provided for this port; there are no DSR and RI signals. All signals are routed to the 9-pin D-Sub connector J102 or to J3 of the HiCO.nect plug connector, respectively. Note that you may only use either the J3 or J102 connection at a time.

The DCD input signal serves to indicate when a cable has been plugged. The line's level can be read on data bit D0 at address 0xA4000080. At each level change, a flip-flop is set and a level 3 interrupt will be permanently issued. The state of the flip-flop can be read and written to data bit D0 at 0xA4000088. The flip-flop and thus the interrupt will be cleared by writing a 0. The flip-flop will be cleared after reset.

The DTR output signal is selected by writing data bit D0 on address 0xA8000090. The state of the DTR signal can be read back to bit 0 on the same address.

The following applies for the two handshake signals DCD and DTR:

Signal	Address	Direction	Data Bus
DCD	0xA4000080	read/write	Bit[7..1] = unused Bit 0 = DCD
Delta DCD	0xA4000088	read/write	Bit[7..1] = unused Bit 0 = Delta DCD
DTR	0xA4000090	read/write	Bit[7..1] = unused Bit 0 = DTR

3.8. I^2C Bus

The SH7760 processor provides two I^2C buses controllers according to Philips specification.

Bus 0 is used to select the real-time clock RTC8564 and the I^2C digital potentiometer AD5241 [3].

Bus 1 connects to J1 (5V-compatible) of the HiCO.nect plug connector via bidirectional buffers. The pull-up resistors of the 5V side of bus 1 connects to the +5V USB power supply.

3.9. SSI Ports

The SH7760 processor has two SSI channels and one AC97 interface (HAC) for the selection of external audio codecs.

Interface SSI0 is connected to HiCO.nect's J3 connector, which allows the selection of an external audio codec. Also, the input clock for the port must be externally supplied.

The SSI1 port is not used.

3.10. USB Host

The SH7760 processor has a USB host controller that complies with the USB 1.0 specification. Here, USB devices such as a keyboard, mouse, printer or a memory stick can be connected.

Both low-speed- and full-speed data transfers are possible. The lines are terminated with 15-KΩ resistors against GND. Power is supplied via the LM3525 single port USB power switch with over-current protection. The total power consumption of all connected USB devices should not exceed 0.5 A.

The data lines are connected to both J3 of HiCO.nect and to the USB connector J100.

3.11. USB Function

The ISP1181 USB interface device [4] is a USB 1.0 compliant full-speed Interface (12 Mbps) and used as USB function controller. The USB function port allows the transmission of data to an external host, e.g. between a host PC and Windows CE via Active Sync.

The USB device is selected via two 16-bit registers, an address- and a data register located in the address region 0xA4000200 through 0xA40002FF. The controller is able to issue a level 12 interrupt and to transfer data into the main memory via DMA channel 0.

3.12. CAN Interface

The SH7760 processor provides two full CAN controllers according to CAN 2.0B.

The data lines of both channels and the error input of channel 1 are connected to J3 of HiCO.nect. Note that an appropriate CAN transceiver has to be mounted on the BASE board.

CAN channel 0 is also connected to the J105 connector via an 82C251CAN transceiver. J105 allows the direct connection of a 9-pin D-Sub connector with flat cable connection.

3.13. MMC Port

The SH7760 processor also has an MMC controller capable of transferring data at a speed of up to 16 Mbaud. The MMC port's chip select-, clock- and data lines are connected to J2 of the HiCO.nect connector.

Additionally, a card detect input is available via which a level 4 interrupt can be issued when plugging or removing an MMC. Inserting or removing an MMC will set a flip-flop that permanently issues the interrupt.

The state of the flip–flop can be read and written to data bit D0 at address 0xA4000100. The flip-flop and thus the interrupt will be cleared by writing a 0. The flip-flop will be cleared after reset.

3.14. LCD Controller

The processor comes with a built-in LCD controller for using flat screens. The input clock for the controller can be selected between a 64-MHz bus clock, a 32-MHz peripheral clock and 25 MHz, which are supplied externally. The LCD controller's output signals are connected to both the connectors J2 and J3 of HiCO.nect and to the connectors J91 and J92.

The J91 connector allows the connection of TFT displays with 18-bit data bus by means of a suitable cable that is available from emtrion. Furthermore, the inputs for a 4-wire touch interface and 2 signals for controlling the supply voltage are routed to the J91 connector. If required, the pins 30 and 31 of a TFT VGA display may be connected (via software) to +3.3V or GND via two outputs of the I^2C AD5241 digital potentiometer [3]. These pins serve to switch the display mode in many display types. The supply voltage for the display can be set to +5V or +3.3 using the W90 jumper. The signal level is always 3.3V.

J92 may be used to directly connect the 5.7“ Colour STN ¼ VGA display SX14Q001 from Hitachi. This display allows the user to adjust the contrast on their monitor via software by means of the I^2C AD5241 [3] digital potentiometer. After power-on, the potentiometer is in its middle position and will have to be corrected via software. If you are using the SX14Q001-ZZA display, the touch screen may be connected to J91.

Make sure that your display is always connected to one connector only. Also, it is not possible to connect an analog CRT set.

Since the built-in LCD controller only has a 16-bit data bus, bit 0 is not selected with the colours red and blue in TFT displays. While this bit is always 0, all 6 bits are selected for green.

The upper 8 bits of the LCD controller on the HiCO.nect connector are connected to the pins GPIO[7 … 0] of J2. Thus all 16 data lines for the connection of a TFT display are also available on an expansion module. If the upper 8 data lines are not needed, e.g. when using an STN display, they may also be programmed and used as GPIO port D.

3.15. Touch Interface

Using the SH7760's 2 analog inputs AN0 and AN1 and the port pins Port B[3 … 1], a 4-wire touch interface is implemented. Port pin B4 is an input for reading the Pen Down signal; port pins B3, B2 and B1 are outputs used to control the touch interface.

Pen Down issues a level 6 interrupt. Pen Up must be identified by polling port B4.

The lines of the touch interface are connected to J2 of HiCO.nect and to the two connectors J90 and J91. J90 is suitable for the SX14Q001-ZZA display from Hitachi.

3.16. RTC

The processor does not come with a built-in real-time clock. This is why the RTC5864 device is used.

The RTC5864 device connects to the I^2C bus 0 and able to issue a level 1 interrupt.

The clock is buffered by a CR2016 button cell.

3.17. Analog Input

HiCO.nect's J3 connector provides an analog input ANI2. The analog input signal is connected to the analog input AN2 of the SH7760 processor via a voltage follower. The permissible input voltage range is 0 to 3.3 volts.

The analog inputs AN0 and AN2 are used for the touch interface, the analog input AN3 is not used.

3.18. Analog Output

J2 of the HiCO.nect plug connector also provides the analog output CONT. This output can be used to set the voltage (by software) from 0 V to 3.3 V by means of the AD5241 I^2C digital potentiometer [3].

After power-on, the potentiometer is always in its middle position; the output voltage is 1.65 V. The output impedance is 4.7 KΩ at 3.3 V and 104.7 KΩ at 0 V, respectively.

When connecting the SX14Q001 display type to the J92 connector, the CONT signal is used for the contrast setting.

3.19. Digital Outputs

HiCO.nect's J3 connector provides 8 digital I/O pins. The pins may either be programmed as output data D8 … D15 of the LCD controller or as GPIO port D.

The processor pins are directly connected to J3. If you wish to use these pins, we recommend that you connect suitable drivers with a 3.3V supply voltage to the lines.

Furthermore, there are 2 outputs OCO1# and OCO2#. They are selected via the AD5241 I^2C digital potentiometer [3]. The maximum current of the 2 outputs is -40 µA at 3.3V / +1.6 mA at 0.4V.

When connecting a TFT display to J91, the 2 outputs are used to select the display's pins 30 and 31.

3.20. CF Card Interface

The bus state controller of the SH7760 processor is able to control the processor bus in the areas 5 and 6 in compliance with PCMCIA cards. The processor does not have a complete PC card controller. This is why a PC card controller was implemented in a PLD.

The control signals of the PC card controller are routed to the J2 connector of HiCO.nect via a driver 74LVT244. This allows an easy implementation of a CF interface on an additional board.

The controller includes the 4 registers PCCISR, PCCGCR, PCCCSCR and PCCCSCIER. The following applies:

Register	Access	Value After Reset	Address	Register	Access
PCCISR	R	-	0xA4000160	8 Bits	16 Bits
PCCGCR	R/W	0x00	0xA4000162	8 Bits	16 Bits
PCCCSCR	R/W	0x00	0xA4000164	8 Bits	16 Bits
PCCCSIER	R/W	0x00	0xA4000166	8 Bits	16 Bits

The register addresses are decoded by means of the lower 11 address lines only. The registers are thus mirrored and several times available in area 1.

The data region of the PC card interface is located in area 6. The controller is able to issue level 9 interrupts.

A PCMCIA interface may only be implemented with restrictions. There is no control of address line A25, VSS and VPP, neither are the VS1 and VS2 signals analyzed. Also, the BVD1 and BVD2 signals are not analyzed. Therefore, the Battery Warning and Battery Dead states do not issue an interrupt. Although the associated enable bits have been implemented, they are of no effect here. Since neither the flash- nor I/O cards make use of the BVD signals, a CF interface may be implemented without any functional restrictions. Check for yourself if there are too many restrictions when using a PCMCIA interface. There should be no difficulties, however, in connection with Flash cards.

The controller is almost fully compatible with the PC card controller in the SH7727. For detailed information, please refer to section 30 of the SH7727 user manual.

3.21. LAN91C111 Ethernet Controller

The LAN91C111 chip from SMSC is used as Ethernet controller [2]. This controller comes with a Media Access Controller (MAC) and Physical Layer Interface (PHY) on a single chip. An on-chip SRAM serves to buffer transmit- and receive frames of 8K bytes. The chip is able to put itself to the operating modes 100 BASE-TX or 10BASE-T, both half- and full duplex.

The Ethernet controller is located in the address range 0xA4000300 through 0xA400030F. Both byte- and word accesses to the Ethernet controller are possible.

The MAC and configuration data of the Ethernet controller are stored in a 93C46 type EEPROM. The IOS lines of the controller are switched between 000 (On switch) and 111 (Off switch) using DIP switch S30 4. In this way, two different data sets may be selected in the EEPROM. By default, data set 0 is used. The DIP switch setting may be read at address 0xa40000a0 on bit 3.

The data lines as well as two status signals that serve to indicate the link status and 10/100 Mbps are connected to J3 of the HiCO.nect and to the RJ45 plug connector J104. The green LED indicates the LINK status and goes on as soon as a connection to another device has been established. The yellow LED indicates that a data transfer takes place. It is blinking on reception and transmission of a message.

When using the Ethernet signals on an external BASE board, an appropriate 1:1 transformer is required.

3.22. Status Port, Status LEDs

An 8-bit status port is located at address 0xA40000A0; it is used to read the status of the W30 jumper and S30 DIP switch.

LED D30 may be enabled or disabled by writing to the same address via data bit 0. The following applies for the port assignment:

Address	Direction	Function	Assignment
0xA40000A0	Read	Status port	Bit [7..5] x: unused Bit 4 = 0: W30 in position 1-2 1: W30 in position 2-3 Bit 3 = 0: S30-4 = On 1: S30-4 = Off Bit 2 = 0: S30-3 = On 1: S30-3 = Off Bit 1 = 0: S30-2 = On 1: S30-2 = Off Bit 0 = 0: S30-1 = On 1: S30-1 = Off
0xA40000A0	Write	Status LED	Bit[7..1] = unused Bit 0 = 0: LED = On 1: LED = Off

The second status LED D10 provides information on the current processor state by way of different brightness intensity levels. The LED cannot be controlled via software. The following applies for the light intensity of D10:

Light Intensity D10	Processor State
Off	Reset
Dark	Sleep– or Standby mode
Bright	Normal operation

3.23. Reset

There are several ways for issuing a reset signal:

- A voltage monitor checks the supply voltages +3.3 volts and +1.5 volts and issues a reset when the respective supply voltage falls below its required level. The +5V supply voltage is not monitored.
- The S100 momentary switch may be used to issue a manual reset.
- Via J1 of the HiCO.nect plug connector.
- Via the JTAG interface.
- Via any write access to address 0xA40000B0.

All resets are hardware resets of the processor board issuing a hardware reset of the processor. The processor may not be "manually" reset.

3.24. Supply Voltage

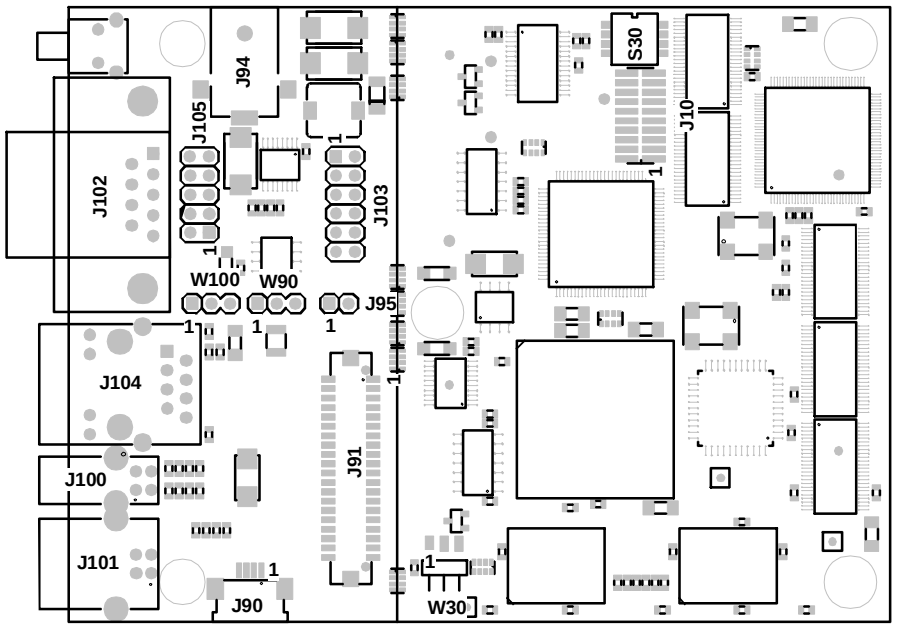
A voltage of +5 volts, +/- 5% must be fed via the J94 small voltage connector. The voltages +3.3 volts for most components and +1.5 volts for the processor kernel are locally generated by a DC/DC converter.

If the processor board is operated in its reduced variant, i.e., as CORE module, then +3.3 volts, +/-5% must be fed via the HiCO.nect plug connector.

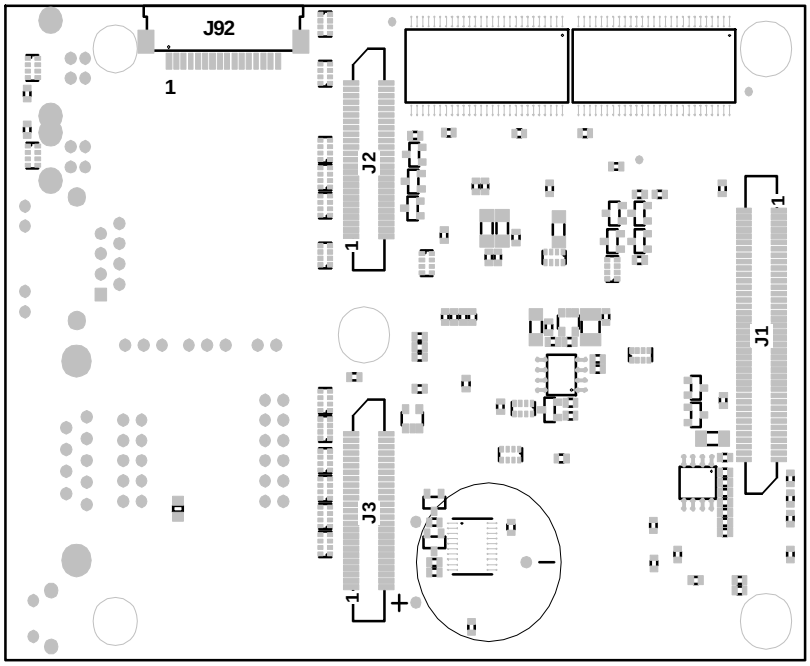
+5 volts are only required for the USB ports and a TFT display.

4. Location of the Connectors

Component side view:



Solder side view:



5. Pin Assignments

5.1. J1, HiCO.nect

Type Hirose FX6-80P, 80-pin

Pin	Signal	Pin	Signal
1	GND	2	+3.3V
3	ID0	4	ID1
5	ID2	6	n/c
7	A0	8	A1
9	A2	10	A3
11	A4	12	A5
13	A6	14	A7
15	A8	16	A9
17	A10	18	A11
19	A12	20	A13
21	A14	22	A15
23	A16	24	A17
25	A18	26	A19
27	A20	28	A21
29	A22	30	A23
31	A24	32	A25
33	GND	34	+3.3V
35	D0	36	D1
37	D2	38	D3
39	D4	40	D5

Pin	Signal	Pin	Signal
41	D6	42	D7
43	D8	44	D9
45	D10	46	D11
47	D12	48	D13
49	D14	50	D15
51	GND	52	+3.3V
53	DRQ1	54	CLK
55	DACK1#	56	BS#
57	IRQ0	58	RD#
59	IRQ1	60	WR#
61	IRQ2	62	WE0#
63	IRQ3	64	WE1#
65	NMI	66	WAIT#
67	RESO#	68	CS4#
69	RESI#	70	CS2#
71	CS0#	72	GND
73	BOOT8#	74	SDA5
75	n/c	76	SCL5
77	BAT	78	VCC5
79	GND	80	+3.3V

5.2. J2, HiCO.nect

Type Hirose FX6-50P, 50-pin

Pin	Signal	Pin	Signal
1	ENAVEE	**2**	GND
3	ENAVDD	**4**	REG#
5	DOFF#	**6**	VS1#
7	M	**8**	VS2#
9	FLM	**10**	RDY/BSY#
11	CL1	**12**	CE1#
13	CL2	**14**	CE2#
15	LCD0	**16**	RESET
17	LCD1	**18**	PDRV#
19	LCD2	**20**	BVD1
21	LCD3	**22**	BVD2
23	LCD4	**24**	CD1#
25	LCD5	**26**	CD2#
27	LCD6	**28**	PWAIT#
29	LCD7	**30**	GND
31	GND	**32**	I_CE1#
33	CONTRAST	**34**	I_CE2#
35	n/c	**36**	IOIS16#
37	GND	**38**	IORD#
39	MMC_IRQ	**40**	IOWR#
41	+3.3V	**42**	GND
43	MMC_CS#	**44**	TOUCH_X1
45	MMC_SCLK	**46**	TOUCH_X2
47	MMC_DI	**48**	TOUCH_Y1
49	MMC_DO	**50**	TOUCH_Y2

5.3. J3, HiCO.nect

Type Hirose FX6-50P, 50-pin

Pin	Signal	Pin	Signal
1	GPIO0/LCD8	**2**	OCO1#
3	GPIO1/LCD9	**4**	OCO2#
5	GPIO2/LCD10	**6**	CAN0_RX
7	GPIO3/LCD11	**8**	CAN0_TX
9	GPIO4/LCD12	**10**	CAN1_RX
11	GPIO5/LCD13	**12**	CAN1_TX
13	GPIO6/LCD14	**14**	CAN1_ERR
15	GPIO7/LCD15	**16**	TXD2
17	GND	**18**	RXD2
19	TXD1#	**20**	RTS2
21	RXD1#	**22**	CTS2
23	RTS1#	**24**	TXD3
25	CTS1#	**26**	RXD3
27	DTR1#	**28**	RTS3-CTS3
29	DCD1#	**30**	RTS3-CTS3
31	ETH_LED0#	**32**	AGND
33	ETH_TDP	**34**	ANI2
35	ETH_TDM	**36**	SS0_CK
37	GND	**38**	SS0_WS
39	ETH_RDP	**40**	SS0_DA
41	ETH_RDM	**42**	AC0_CLK
43	ETH_LED1#	**44**	n/c
45	USBH_5V	**46**	USBF_5V
47	USBH_DM	**48**	USBF_DM
49	USBH_DP	**50**	USBF_DP

5.4. J10, Debug Connector

Type 20-pin connector, 1.27 mm * 1.27 mm pitch

Pin	Signal	Pin	Signal
1	+3.3 V	**2**	+3.3 V
3	TCK	**4**	GND
5	TRST#	**6**	n/c
7	TDI	**8**	TDO
9	ASEBRK#	**10**	RESET#
11	TMS	**12**	HRESI#
13	PLD_TDI	**14**	PLD_TDO
15	PLD_TCK	**16**	GND
17	n/c	**18**	n/c
19	n/c	**20**	n/c

5.5. J90, Touch Connector for SX14Q001-ZZA

Type 4-pin FFC, 1.0 mm pitch

Pin	Signal
1	Touch TPX2
2	Touch TPY1
3	Touch TPX1
4	Touch TPY2

5.6. J91, TFT Connector

Type 40-pin connector, 1.25 mm * 1.25 mm pitch, Hirose DF13

Pin	Signal	Pin	Signal
1	ENAVEE	2	ENAVCC
3	M	4	n/c
5	TFT_DIP2	6	TFT_DIP1
7	TFT_VCC	8	TFT_VCC
9	DE	10	GND
11	BLUE5	12	BLUE4
13	BLUE3	14	BLUE2
15	BLUE1	16	GND
17	GND	18	GREEN5
19	GREEN4	20	GREEN3
21	GREEN2	22	GREEN1
23	GREEN0	24	GND
25	RED5	26	RED4
27	RED3	28	RED2
29	RED1	30	GND
31	GND	32	VSYNC
33	HSYNC	34	CLK
35	GND	36	VCC_TFT
37	Touch TPX1	38	Touch TPY1
39	Touch PTX2	40	Touch TPY2

5.7. J92, Display Connector for SX14Q001-ZZA

Type 26-pin FFC, 1.0 mm pitch

Pin	Signal
1	FLM
2	CL1
3	CL2
4	DISP OFF#
5	+3.3 V
6	GND
7	VCON
8	D0
9	D1
10	D2
11	D3
12	D4
13	D5
14	D6
15	D7
16	GND

5.8. J94, Power

Type Power supply jack, 2.0 mm pin

Pin	Signal
1	+5 Volt
2	GND
3	GND

5.9. J95, Power

Type 1*2 connector, 2.54 mm pitch

Pin	Signal
1	+5 Volt
2	GND

5.10. J100, USB Host

Type USB Type A

Pin	Signal
1	USBH_5V
2	USBH_DM
3	USBH_DP
4	GND

The housing of the J100 connector is connected to GND.

5.11. J101, USB Function

Type USB Type B

Pin	Signal
1	USBF_5V
2	USBF_DM
3	USBF_DP
4	GND

The housing of the J101 connector is connected to GND.

5.12. J102, COM1

Type D-Sub connector, 9-pin

Pin	Signal
1	DCD1#
2	RXD1#
3	TXD1#
4	DTR1#
5	GND1#
6	DSR1#
7	RTS1#
8	CTS1#
9	n/c

The housing of the J102 connector is connected to GND.

5.13. J103, Serial Ports COM2/COM3

Type 2*6 connector, 2.54 mm pitch

Pin	Signal
1	+3.3V
2	RTS3-CTS3
3	GND
4	RTS3-CTS3
5	TXD2
6	RXD3
7	RXD2
8	TXD3
9	RTS2
10	GND
11	CTS2
12	+3.3V

5.14. J104, Ethernet

Type RJ45 plug connector

Pin	Signal
1	TD
2	+3.3V
3	TD#
4	RD
5	-
6	RD#
7	-
8	GND

The housing of the J104 connector is connected to GND.

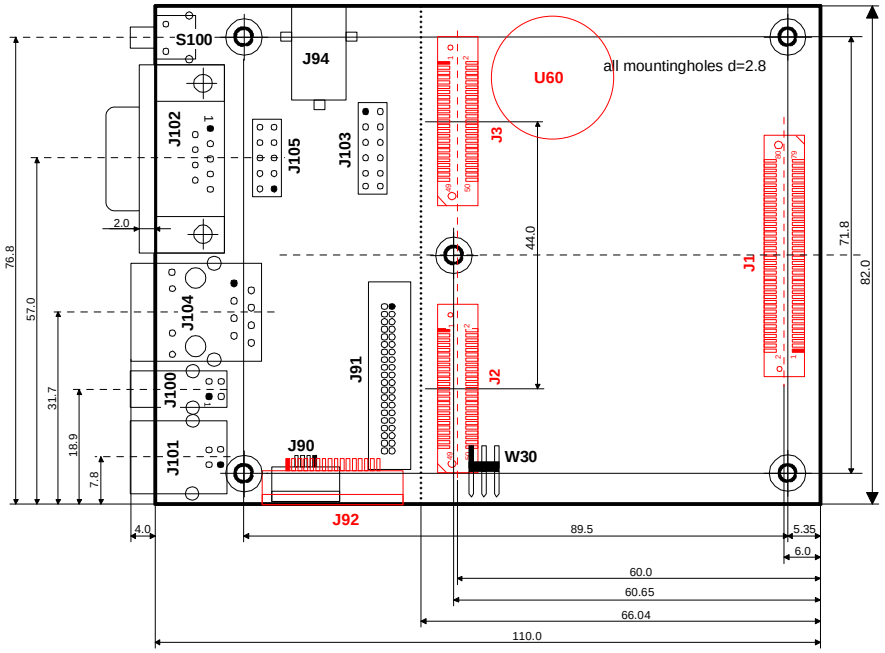
5.15. J105, CAN0

Type 2*5 connector, 2.54 mm pitch

Pin	Signal
1	n/c
2	n/c
3	CAN_L
4	CAN_H
5	GND
6	n/c
7	+5 Volt
8	n/c
9	GND
10	n/c

6. Dimensional Drawing

Component side view; the solder side connectors are marked red.



7. Technical Data

7.1. Mechanical Data

Weight	120 g
Board	Glasepoxi FR-4, UL-listed, 8 layers
Dimensions	110 mm x 82 mm x 20 mm

7.2. Electrical Data

Supply voltage	5V, +/-5%
Power consumption	0.4 A max.

7.3. Environmental Conditions

Operating temperature **Storage temperature**	0 ... +70°C, -40 ... +125°C
Relative humidity	0 ... 95 %, non-condensing

8. Reference

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[2] LAN91C111
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Datasheet
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SMSC

[3] I^2C compatible 256-Position Digital Potentiometers AD5241/5242
Datasheet
Revision B, 2002
Analog Devices Inc.

[4] ISP1181B Full-speed Universal Serial Bus interface device
Product Data
Rev. 01 — 03 July 2002
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