HITACHI MICROCOMPUTER TECHNICAL UPDATE

DATE	25 January 2001	No.	TN-SH7-272A/E
THEME	Bug of a serial data reception of the multiprocessor communication function at SCI		

CLASSIFICATION	☐ Spec change ☐ Supplement of Documents	■ Limitation on Use	
PRODUCT NAME	HD6417750 ,HD6417750S ,HD6417751	Lot	Lot #All

REFERENCE DOCUMENTS	SH7750 series Hardware Manual SH7751 Hardware Manual	Rev.	Effective Date
			Eternity

Notice

　　There is a restriction at using the multiprocessor communication function.

　　Please take care when using the multiprocessor communication function.

1. Bug

(1) SCSSR1.RDRF flag is set to 1 in the multiprocessor serial data reception after received a frame of data for another station even if SCSCR1.MPIE bit equals 1(the multiprocessor interrupt enabled).

(2) The value of SCSSR1.MPB bit is not correct.

(3) The flags, FER and ORER, can be set to 1 even if SCSCR1.MPIE bit equals 1.

2. Workaround

Use the following procedure for a serial data reception of the multiprocessor communication function.

(1) The procedure to distinguish the multiprocessor interrupt from the SCI interrupt

　　Please check the value of SCSCR1.MPIE bit in the interrupt handler, when a SCI interrupt request occurs on the multiprocessor serial data reception.

　　Case 1: SCSCR1.MPIE bit equals 1

　　　　　A received data should be ignored.

　　　　　Although the received data is for another station's (MPB=0), SCSSR1.RDRF flag is set to 1.

　　　　Please clear SCSSR1.RDRF flag to 0 in the RXI interrupt handler.

　　Case 2: SCSCR1.MPIE bit equals 0

　　　　　This case is the multiprocessor interrupt request or the RXI interrupt for a reception of this station's data.

(2) The procedure to distinguish the received data is "ID" or "data".

　　Don't use SCSSR1.MPB bit for the processing of software.

　　In the processing of software to distinguish a receive data between this station's ID (MPB=1) and a valid data (MPB=0), please create a user's defined flag on a memory which indicates information about starting a serial data reception.

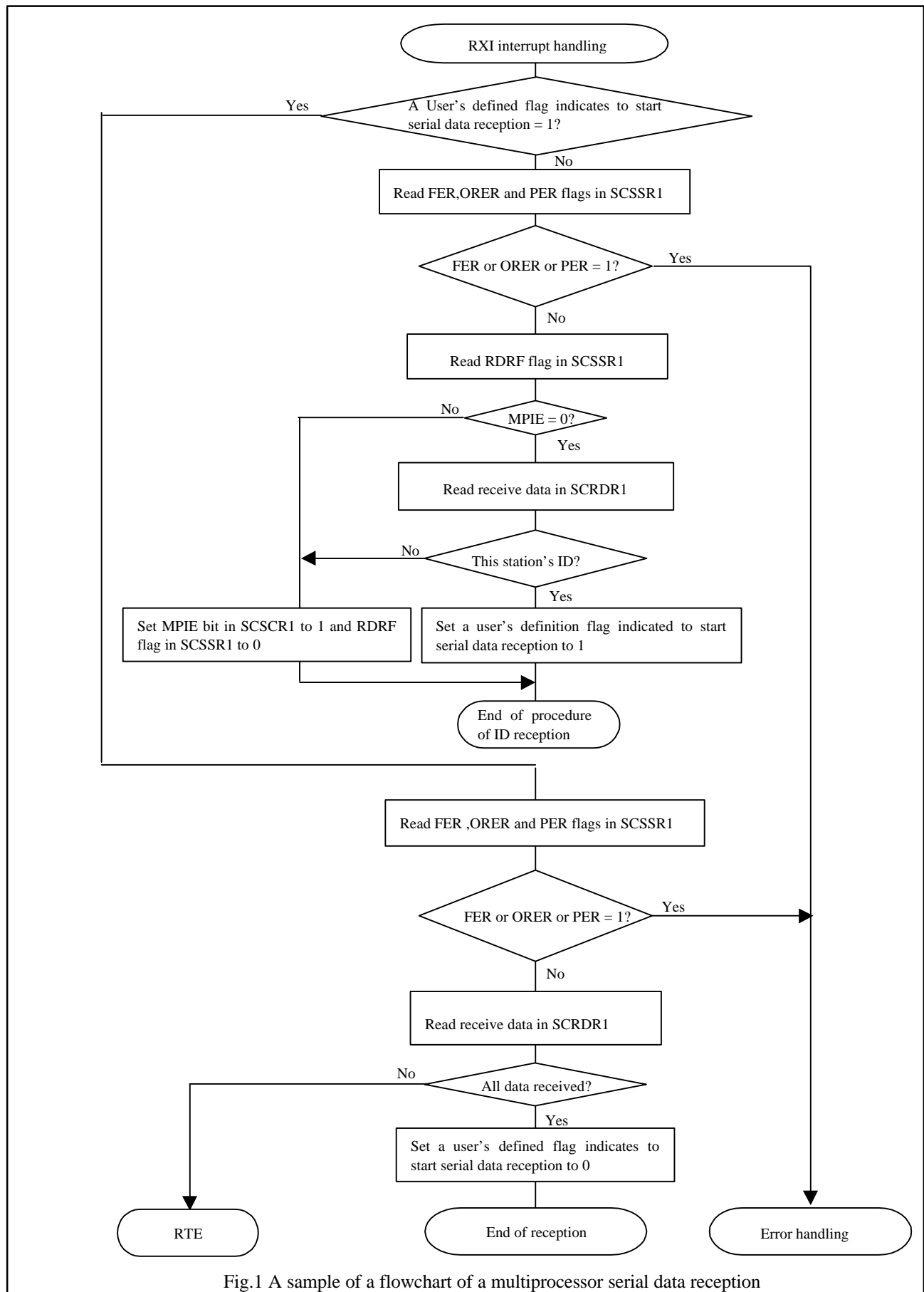　　A sample of a flowchart of a multiprocessor serial data reception is shown in the following.

Fig.1 A sample of a flowchart of a multiprocessor serial data reception