Date: Feb.04.2004

RENESAS TECHNICAL UPDATE

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
RenesasTechnology Corp.

Product Category	User Development Environment		Document No.	TN-CSX-063A/EA	Rev.	1.0
Title	SuperH RISC engine C/C++ compiler package Ver.8.0.01 Updates		Information Category	Specification Change		
Applicable Product	P0700CAS8-MWR P0700CAS8-SLR P0700CAS8-H7R	Lot No. All	Reference Document	SuperH RISC engine C/C++ Compiler Assembler Optimizing Linkage Editor User's Manual REJ10B0047-0100H Rev.1.0		

SuperH RISC engine C/C++ compiler package is updated in Ver.8.0.01.

See the notes below if you have the compiler package listed in the following table.

Part No.	Package version	Compiler version
P0700CAS8-MWR	8.0.00	8.0.00
P0700CAS8-SLR	8.0.00	8.0.00
P0700CAS8-H7R	8.0.00	8.0.00

If you have the compiler package of the Windows® version, download the update program from the following URL:

http://www.renesas.com/eng/products/mpumcu/tool/index.html

If you have the compiler package of the UNIX version, request the update program to an authorized product distributor.

The contents of updates in this package are shown below.

Descriptions of sections 1, 2, and 3.1 only apply to the Windows® version.

1. High-performance Embedded Workshop (Windows® version)

1.1 Reload of Files

The problem of not reloading the file when a file currently open in the editor window is edited, saved, and then updated by the external editor, has been corrected. (This problem only occurs with Ver. 3.0.02)

1.2 Problem with the Search Function of the Memory Menu

The problem of an empty [Memory] window with no description being displayed when carrying out a memory search selected from [Memory->Search...] in the menu, has been corrected.

1.3 Symbol Load Command

The problem with the Symbol Load command not operating has been corrected.

1.4 Adding and Modifying Regarding the Data Generated by the Project Generator

Project generation of the following CPUs has been newly added:

SH7641, SH7760

The I/O definition files (iodefine.h) of the following CPUs have been modified:

SH7047, SH7052F, SH7053F, SH7054F, SH7055F

The vector definition files (intprg.src, vecttbl.src, vect.inc) of the following CPUs have been modified:

SH7290, SH7294

2. SuperH RISC engine simulator/debugger (Windows® version)

2.1 Tool Trace Function of Debugging Extension for the SH4AL-DSP/SH-4A Simulator

The problem with the tool trace function of the debugging extension V1.0 not working properly when using it with the simulator for the SH4AL-DSP or SH-4A, has been corrected.

3. Compiler

3.1 Modification of option dialog (Windows® version)

The following four options which were under the [CPU] tab, are now located under the list of [Miscellaneous options :] of the [Other] category on the [C/C++] tab.

fixed_const [Miscellaneous options :][Floating-point constant is handled as a fixed-point constant]

fixed_max [Miscellaneous options :][treats 1.0 as maximum number of fixed type]

fixed_noround [Miscellaneous options :][delete type conversion after fixed multiple]

repeat [Miscellaneous options :][DSP repeat loop is used]

3.2 Illegal bitfield member comparison

Refer to RENESAS TECHNICAL UPDATE TN-CSX-061A/EA.

4. Optimizing Linkage Editor

4.1 Unnecessary error generated when sections are overlaid

The problem of an unnecessary error message (L2022) displayed when the following conditions were satisfied at the same time, has been corrected.

[Conditions]

(1) Uninitialized data sections were overlaid in the start option.

(2) The form=binary (or hexadecimal or stype) option was specified.

5. Standard Library Generator

5.1 Illegal fatal error

The problem of a fatal error generated when the fixed_const, fixed_max or fixed_noround option was specified, has been corrected.