# PowerVR PDP

The PowerVR PDP pixel display pipeline family has been developed to work with embedded graphics and video processor cores to enable video and graphical content from multiple sources to be displayed simultaneously with very high quality. The PowerVR PDP family is one of a range of PowerVR IP cores developed to meet the growing multimedia needs of the digital consumer market.

The PowerVR PDP family is fully customisable, enabling the feature set to be optimised for a number of low power, high-performance system-on-chip (SoC) applications such as portable communicators, PDAs, handheld gaming devices, car information systems (CIS), internet appliances, point of sale information systems, DVD players, and set-top boxes.

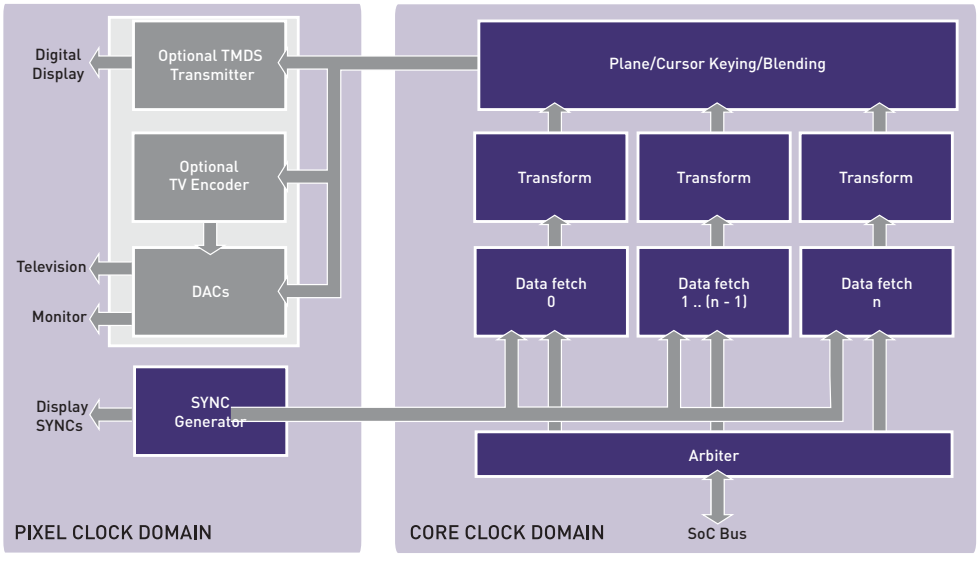
Benefits include:

- Optimised die size
- Easy SoC integration using customisable simple synchronous bus interfaces
- Synthesizable soft IP package
- Optional companion TVE TV encoder for driving worldwide standard televisions
- Advanced de-interlace engine available as an optional companion to the PDP Pro core
- Performance optimised for Unified Memory Architectures (UMA)
- Process portable design: 0.18µm, 0.13µm, 90nm and beyond

## PowerVR PDP family features

- Fully programmable CRTC timing generator for resolution and refresh optimisation
- Flexible resolution support up to 2048 x 2048 dependent on memory bandwidth
- 8-bit or 10-bit per component processing option (PDP Pro)
- Progressive and interlaced support
- Up to six planes displayed simultaneously
- Up to two independent hardware cursors (max 64 x 64 at 8bpp or 16bpp)
- Supports common 8, 16, 24, 32bpp packed graphics formats
- Supports common variants of packed and planar YCbCr video formats
- Picture-in-picture capability
- Global or pixel alpha blending between planes
- Configurable blend order
- Colour keying between any plane
- Up/down scaling of video plane (up to 8-tap horizontal, 4-tap vertical)
- Optional palette LUTs
- Independent gamma correction for video and graphics
- Background plane scrolling
- Split background plane
- Full scan design

**PowerVR PDP Base Architecture**



## Performance

PowerVR PDP's fully programmable pixel clock can operate up to a maximum frequency equal to the internal core clock frequency.

## Size and Power

The PDP IP core of choice can be optimised using a customisation tool that ensures the synthesised feature set matches the requirements of the target application. Power requirements have been optimised using sophisticated power management techniques such as module and register-level clock gating to ensure lowest active and standby power.

## Related System Solution IP

- PowerVR graphics cores: MBX Pro for high-end 3D graphics acceleration for consumer electronics devices including set-top boxes, consoles and home entertainment systems. MBX for best area/performance 3D graphics accelerator for handheld devices and mainstream set-top boxes. MBX Lite for entry level 3D graphics acceleration for mobile devices.
- PowerVR M2VX is a family of MPEG-2 video decoders for MP@ML, MP@HL and multiple stream decode.
- PowerVR MVDA2 is an efficient multi-standard video decode accelerator, designed to accelerate the decode of H.264, MPEG-4, MPEG-2, WMV8 and WMV9 video streams.
- PowerVR MVED1 is a multi-standard video codec accelerator, designed to accelerate the encode and decode of H.264, MPEG-4, MPEG-2, WMV8 and WMV9 video streams.
- PowerVR I2P-MC is an advanced motion compensation interlace-to-progressive scan converter enabling a premium quality de-interlacing solution.
- PowerVR I2P-MA is an advanced motion adaptive interlace-to-progressive scan converter enabling a high-quality de-interlacing solution.
- PowerVR TVE is a digital TV encoder which processes the PDP output stream to give Composite, S-Video (Y/C), or RGB (SCART) interlaced video for TVs. TVE includes programmable filters to optimise picture quality, a programmable subcarrier generator, and a versatile timing generator which supports world-wide TV systems. The TVE-M variant includes integrated video DACs and Macrovision™ copy protection.
- PowerVR IEP, Image Enhancement Processor, is a package of picture enhancement functions for high-quality picture output to modern displays.
- PowerVR DRE is a core which delivers enhanced response time for LCD panels.

## PDP Core design package

PDP is available as soft IP and ships with: synthesis scripts; extensive verification test suite to ensure correct implementation of the design in an SoC; behavioural simulator written in ANSI C; hardware implementation guide; programmer's reference manual; and feature-set configuration tool.

PowerVR
Imagination Technologies plc
Innovation Centre, Home Park Estate, Kings Langley, Herts, WD4 8LZ
licensing@powervr.com
**www.powervr.com**



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