Intel® 2700G Multimedia Accelerator

Design Guide

For the Intel® 2700G5 Multimedia Accelerator and the Intel® 2700G3 Multimedia Accelerator

April 2004

Document Number: 300949-001

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Revision History

Rev. No.	Description	Date
-001	Initial Release	April 2004

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1 Introduction

This design guide, along with the *Intel® 2700G Multimedia Accelerator Reference Platform Schematics*, contains the information required to complete a hardware design based on the 2700G Multimedia Accelerator component. This document contains Routing Guidelines, Power Delivery Requirements, Breakout and Routing Examples, PCB Manufacturing Recommendations, and Placement Examples and Recommendations.

This design guide provides Intel's design recommendations for systems based on a supported applications processor with Intel® XScale® technology and the 2700G Multimedia Accelerator.

Note: When a reference is made to the applications processor in this document, it is intended that this includes the Intel® PXA250, Intel® PXA255, Intel® PXA26x and Intel® PXA27x processor family of application processors. Where a reference is intended to refer to a specific processor, the specific processor will be listed separately. Note that the 2700G Multimedia Accelerator does not support all PXA26x processors; only those that make use of a 32-bit system bus.

This design guide covers the 2700G3 and 2700G5 Multimedia Accelerator components. The 2700G3/2700G5 Multimedia Accelerator components are in a package with 0.65 mm pitch.

Note: The descriptions contained in this document apply to both the 2700G3 Multimedia Accelerator and the 2700G5 Multimedia Accelerator, unless otherwise noted.

These design guidelines have been developed to ensure maximum flexibility for board designers while reducing the risk of board related issues. The design information provided in this document falls into one of the two following categories:

- *Design Recommendations* are items based on Intel's simulations and lab experience to date and are strongly recommended to meet the timing and signal quality specifications.
- *Design Considerations* are suggestions for platform design that provide one way to meet the design recommendations. They are based on the reference platforms designed by Intel. They should be used as an example, but may not be applicable to particular designs.

Platform schematics are available and are intended as a reference for board designers. While the schematics may cover a specific design, the core schematics will remain the same for most platforms. The schematic set provides a reference schematic for each platform component as well as common system board options. Additional flexibility is possible through other permutations of these options and components.

Note: For package information, refer to the Intel® 2700G Multimedia Accelerator Datasheet

The Intel® 2700G Multimedia Accelerator may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

1.1 Reference Documentation

Document Title	Location/Document Number
Intel® 2700G Multimedia Accelerator Datasheet	300948
Intel® 2700G Multimedia Accelerator Reference Platform Schematics	300953
Intel® 2700G Multimedia Accelerator Development Platform Schematics	300954
Intel® PXA27x Processor Family Developer's Manual	280000
Intel® PXA27x Processor Family Design Guide	280001

1.2 Component Overview

The Intel® XScale® technology application processor and 2700G multimedia accelerator delivers a feature-rich handheld platform solution.

1.2.1 Intel® 2700G Multimedia Accelerator

The 2700G Multimedia Accelerator works in conjunction with the application processor to provide handheld devices with enhanced multimedia capabilities. These components are interconnected via the general system bus; a 32-bit bus that can operate up to 100 MHz.

The 2700G Multimedia Accelerator provides an interface to the general system bus, local memory, two LCD display outputs, and one LCD input. Functionality includes:

- 32-bit 100 MHz or 133 MHz SDRAM interface for local memory
- High performance graphics acceleration via its 32-bit graphics engine that can operate at speeds up to 75 MHz
- Low-power states
- Accelerated dual display, including support for simultaneous displays with independent images and resolutions

1.2.1.1 Packaging/Power

- 14 mm x 14 mm 364 VF-BGA package with 0.65 mm ball pitch
- 1.2 V core with variable supplies (1.8 V, 2.5 V, 3.3 V) for I/O interfaces
  - 2.5 V and 3.3 V always required for PLL and Miscellaneous I/O

1.2.2 General System Bus

- Supports PXA27x processor as well as other application processors
- Supports 32-bit data bus width only
- Supports operation up to 100 MHz
- Operates at either 1.8 V or 2.5 V
- SRAM (write only) and Variable Latency I/O (VLIO) (read and write) protocols used to communicate with the 2700G Multimedia Accelerator

1.2.3 Local Memory Interface

- 32-bit wide SDRAM interface
- Supports speeds of 13 MHz to 133 MHz
  - Provides bandwidth up to 533 MB/s (133 MHz)
- Operates at either 1.8 V or 2.5 V
  - Maximum frequency of 100 MHz at 1.8 V
  - Maximum frequency of 133 MHz at 2.5 V
- Supports 64 Mb, 128 Mb, 256 Mb and 512 Mb SDRAM technologies
- Supports two x16-bit devices or one x32-bit device with four banks
- Self-refresh and deep power down support using CKE

1.2.4 Graphics capabilities

- 2D and 3D graphics acceleration
- High performance video acceleration
- 32-bit graphics engine with variable operating frequency (up to 75 MHz maximum)
- Dual display capabilities with independent images and resolutions
- Display resolutions up to 1280x1024 @ 60 Hz with 16bpp or 1024x768 @ 60 Hz with 24bpp from the 2700G Multimedia Accelerator

1.2.4.1 LCD Outputs

- Primary and auxiliary LCD outputs driven through the 2700G Multimedia Accelerator
- Flexible dual display allows either LCD interface to be driven by the 2700G Multimedia Accelerator's display engine
  - Other LCD interface driven by application processor's display engine through the 2700G Multimedia Accelerator
  - Auxiliary LCD output for systems supporting dual display
- Operate at either 1.8 V, 2.5 V, or 3.3 V
- Supports external encoders (VGA, TMDS, LVDS) to translate from LCD to a variety of display standards

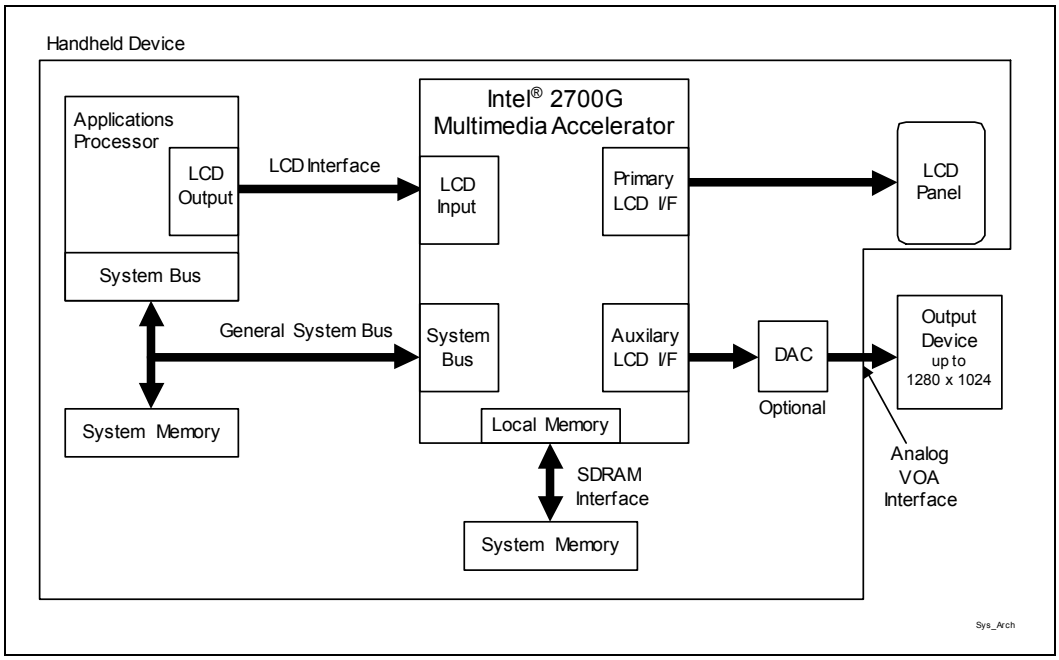
1.2.4.2 LCD Input

- Single LCD input interface to accept LCD output from the applications processor
  - 2700G Multimedia Accelerator's display switching capabilities redirects this display stream out the appropriate LCD output interface
- LCD input only used for systems that support dual display
- Operates at either 1.8 V or 2.5 V

1.3 System Configuration

Figure 1-1 illustrates a typical high level configuration using 2700G Multimedia Accelerator system.

Figure 1-1. Typical Intel® 2700G Multimedia Accelerator System Configuration



1.4 Interface Operating Summary

Table 1-1 summarizes the voltage and operating frequencies for each of the 2700G Multimedia Accelerator's interfaces.

Table 1-1. Interface Frequency and Voltage Summary

Interface	Signaling Voltage	Max Frequency
System Bus	1.8 V	100 MHz
	2.5 V	133 MHz
Local Memory	1.8 V	100 MHz
	2.5 V	133 MHz
Primary LCD Output	1.8 V, 2.5 V, and 3.3 V	108 MHz
Secondary LCD Output	1.8 V, 2.5 V, and 3.3 V	108 MHz
LCD Input	1.8 V and 2.5 V	46 MHz

1.5 General Design Considerations

If the guidelines listed in this document are not followed, it is recommended that thorough signal integrity and timing simulations are completed for each design. When the guidelines are followed, critical signals are recommended to be simulated to ensure proper signal integrity and flight time. Any deviation from the guidelines should be simulated.

Trace impedance is dependent on trace width, distance to reference plane, and dielectric constant. The trace impedance typically noted (i.e., 60 Ω ± 15%) is the nominal trace impedance for a 5-mil wide micro-strip trace that is 4.5 mils from its reference plane with a dielectric constant of 4.1. Different micro-strip and stripline configurations are possible, but changes in trace width, dielectric constants, and distances to reference plane(s) will impact the trace impedance. For example, if the distance from a signal to its reference plane is reduced (maintaining the same dielectric constant), a 5-mil trace will no longer result in a 60 Ω impedance. Due to these issues, special care should be taken when determining board stackup and routing techniques. Any significant deviations from the 60 Ω trace impedance target should be evaluated with post-layout simulations.

Additionally, the nominal impedance is the impedance of the trace when not subjected to the fields created by changing current in neighboring traces. When calculating flight times, it is important to consider the minimum and maximum impedance of a trace based on the switching of neighboring traces. Using wider spaces between the traces can minimize this trace-to-trace coupling. In addition, these wider spaces reduce settling time.

Coupling between two traces is a function of the coupled length, the distance separating the traces, the signal edge rate, and the degree of mutual capacitance and inductance. To minimize the effects of trace-to-trace coupling, the routing guidelines contained in this document should be followed.

To ensure a clean signal return path, maintaining a solid reference plane is recommended. Signals (especially critical signals) should avoid routing over plane splits or voids as much as possible. If a signal transitions reference planes, appropriate bypass capacitors or stitching vias are recommended between the reference planes (near the reference transition).

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2 Quadrant Layout and Component Placement

This chapter provides an example of a 2700G Multimedia Accelerator platform component placement for a reference design.

2.1 Component Quadrant Layout

Figure 2-1 provides the quadrant layout for the PXA27x processor and Figure 2-2 provides the quadrant layout for the 2700G3 and 2700G5 Multimedia Accelerator components. The quadrant layouts shown are approximations. The quadrant layout figures do not show the exact component ball count; only general quadrant information is presented and is intended for reference while using this document. Only the exact pin or ball assignment should be used to conduct routing analysis. Refer to the component datasheet for pin or ball assignment information.

Figure 2-1. Intel® PXA27x Processor HDCSP (VF-BGA) Quadrant Layout (Top View)

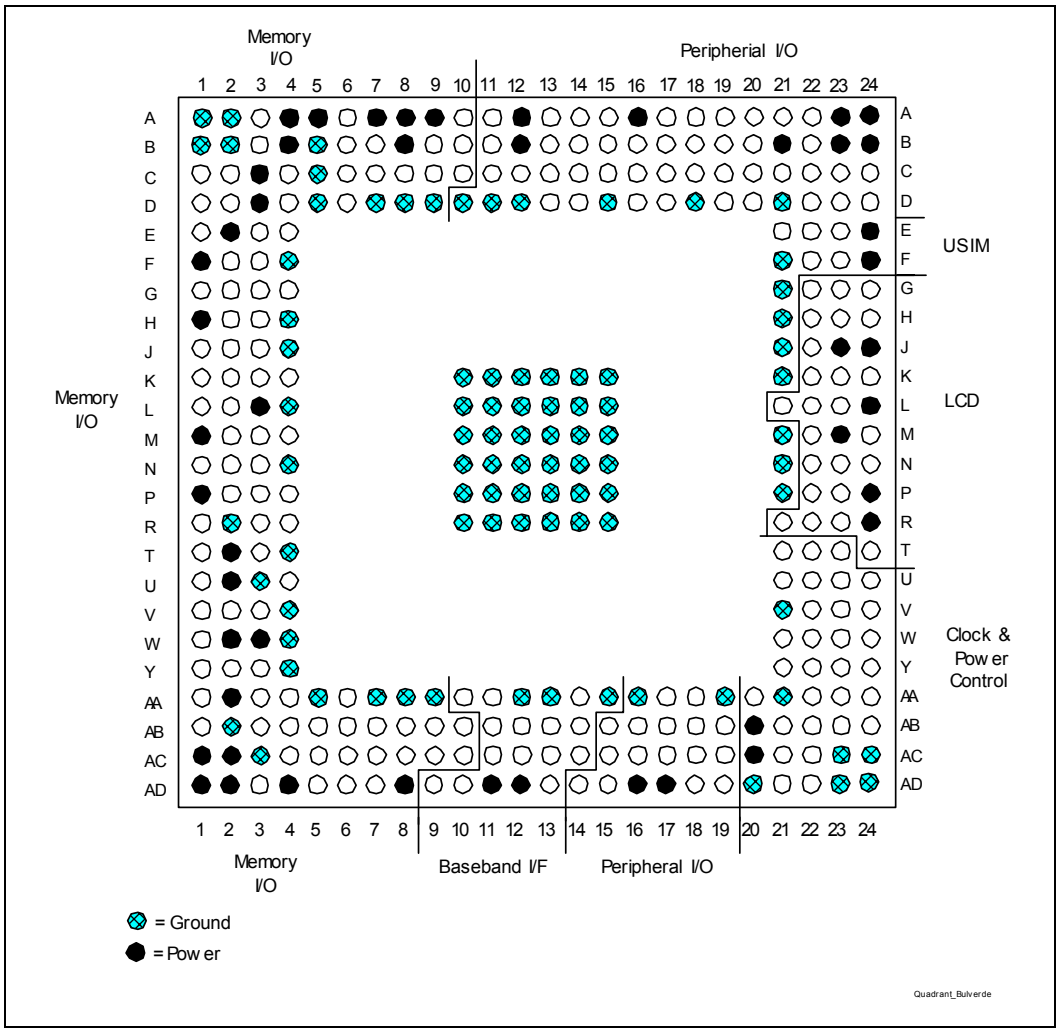
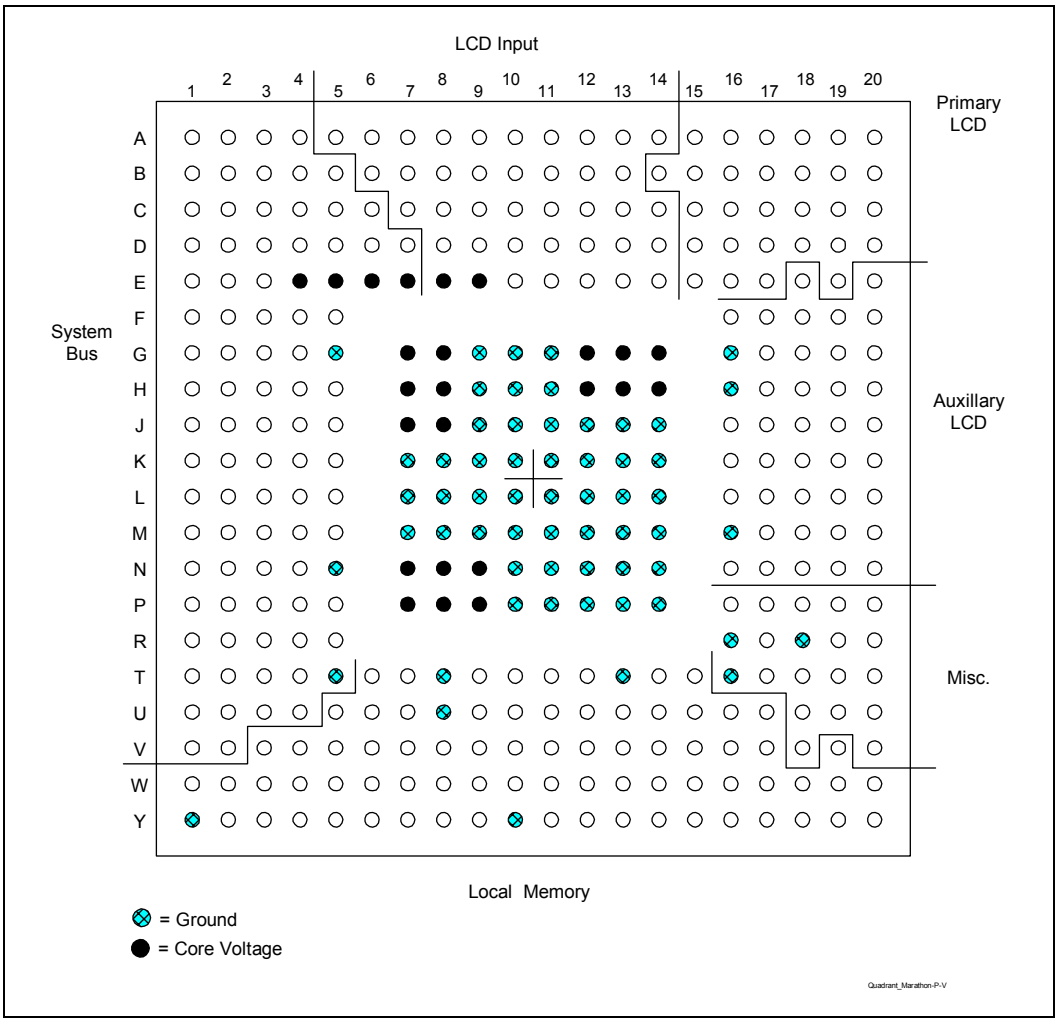


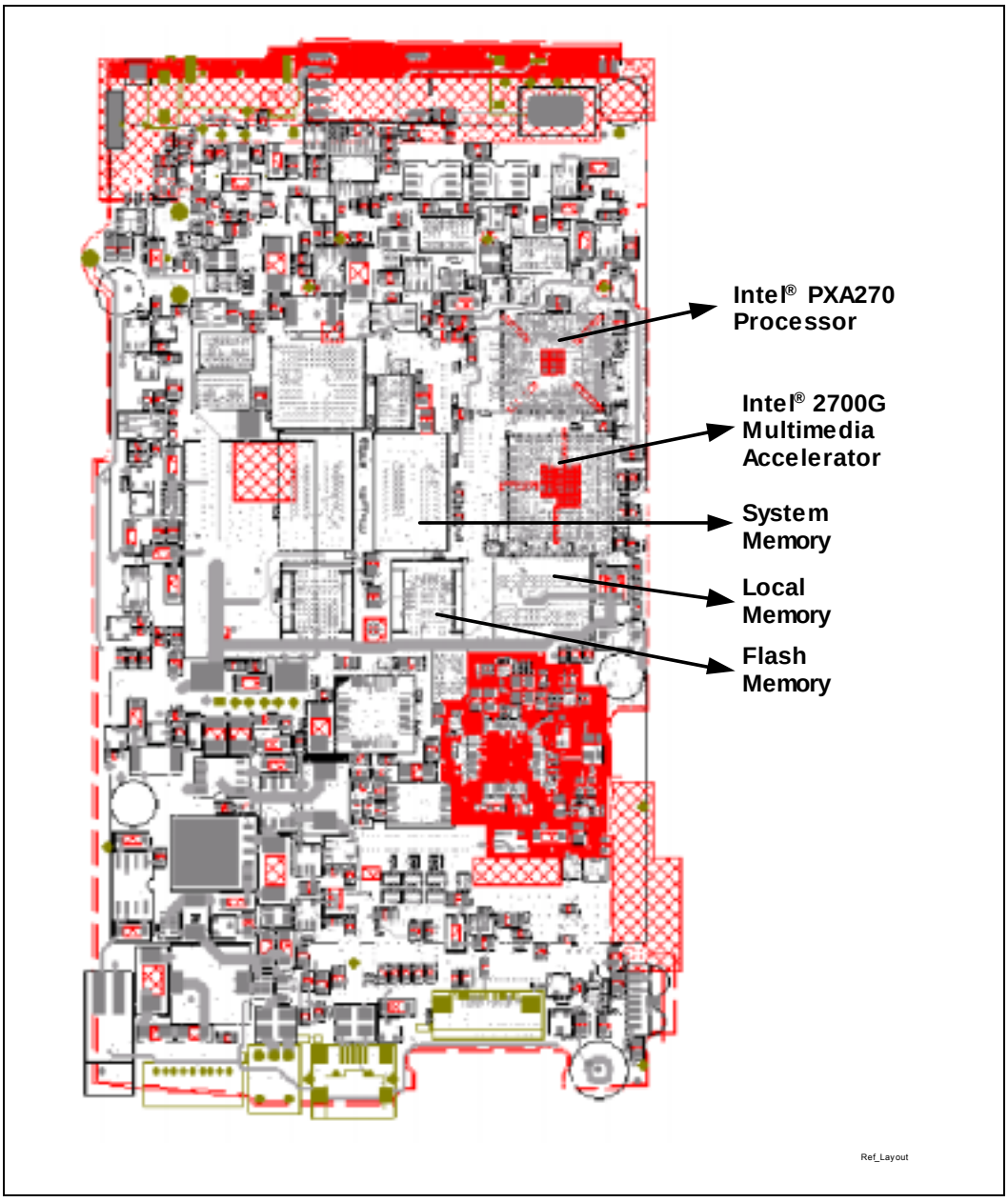
Figure 2-2. Intel® 2700G Multimedia Accelerator Quadrant Layout (Top View)



2.2 Platform Component Placement

The layout shown in Figure 2-3 represents a sample reference design for a 2700G Multimedia Accelerator platform, and is not intended to show what a production design would look like.

Figure 2-3. Reference Layout



3 Printed-Circuit Board (PCB) Technology

This chapter provides printed-circuit board (PCB) technologies recommended for use in 2700G Multimedia Accelerator systems. The 2700G3 and 2700G5 Multimedia Accelerator components use a 14 mm x 14 mm VF-BGA package with 0.65 mm ball pitch. The PXA27x processor uses a 13 mm x 13 mm VF-BGA package. The VF-BGA package's 0.65 mm ball pitch provides the high density required in portable digital assistant (PDA) and wireless handset applications, but also impacts the PCB technologies needed for proper breakout and routing.

3.1 General PCB Characteristics

The recommended PCB design characteristics for 2700G Multimedia Accelerator systems are shown in Table 3-1.

Table 3-1. Recommended PCB Design Guidelines

Feature	Dimensions (mm)	Dimensions (mils)
PCB Layers	6 to 8 layers (typical)	
PCB thickness	0.7874 to 1.5748 (typical)	31 to 62 (typical)
Land Pad Size	0.254	10
Solder Mask Opening	0.3560	14
Typical Trace Width	0.1016	4.0
Reduced Trace Width between Land Pads	0.0762	3.0
Typical Micro-via Size1	0.1016	4.0

3.2 PCB Layer Assignment (Board Stackup)

Layer assignment is generally flexible; two recommended PCB layer assignments are shown in Figure 3-1 and Figure 3-2. Both represent an eight layer PCB.

Figure 3-1. 8-layer PCB Stackup (Example 1)

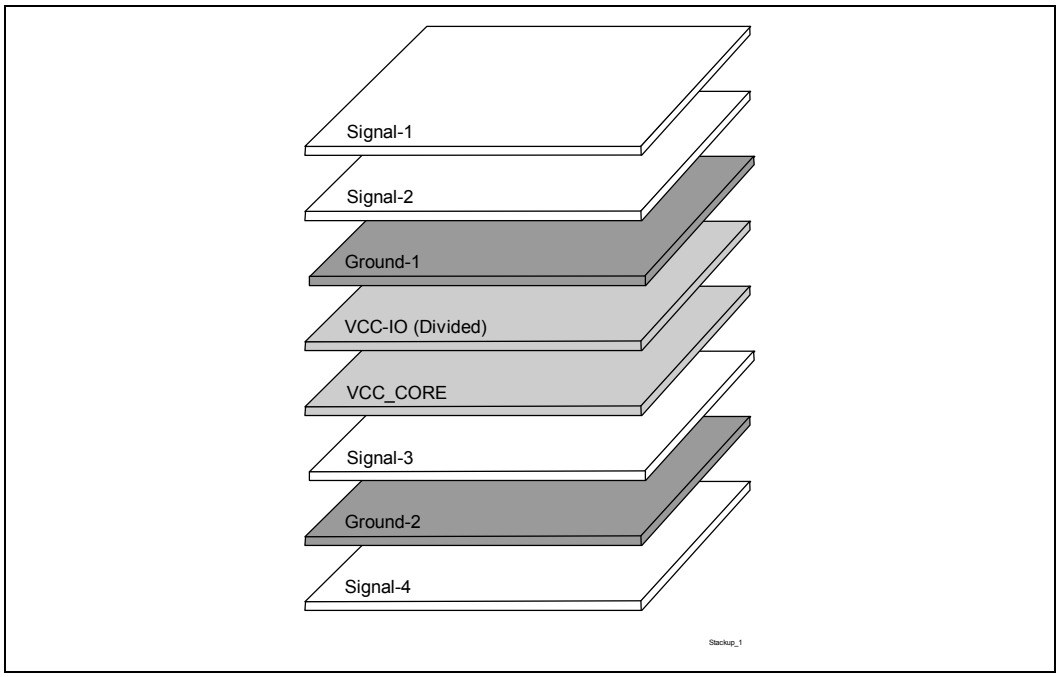
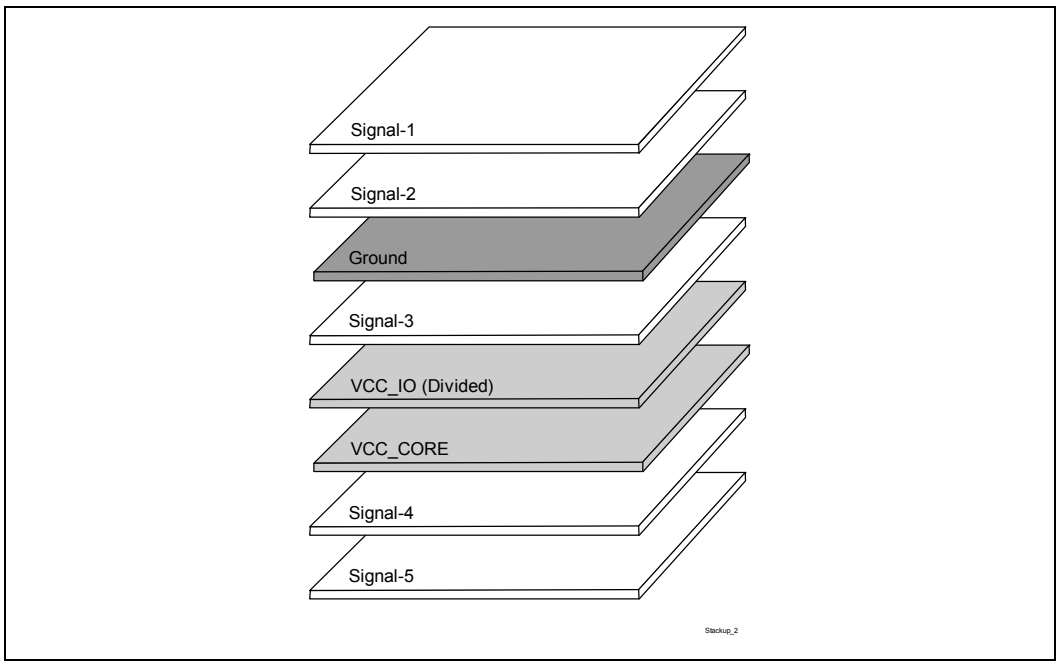


Figure 3-2. 8-layer PCB Stackup (Example 2)



4 Power Delivery and Power Savings

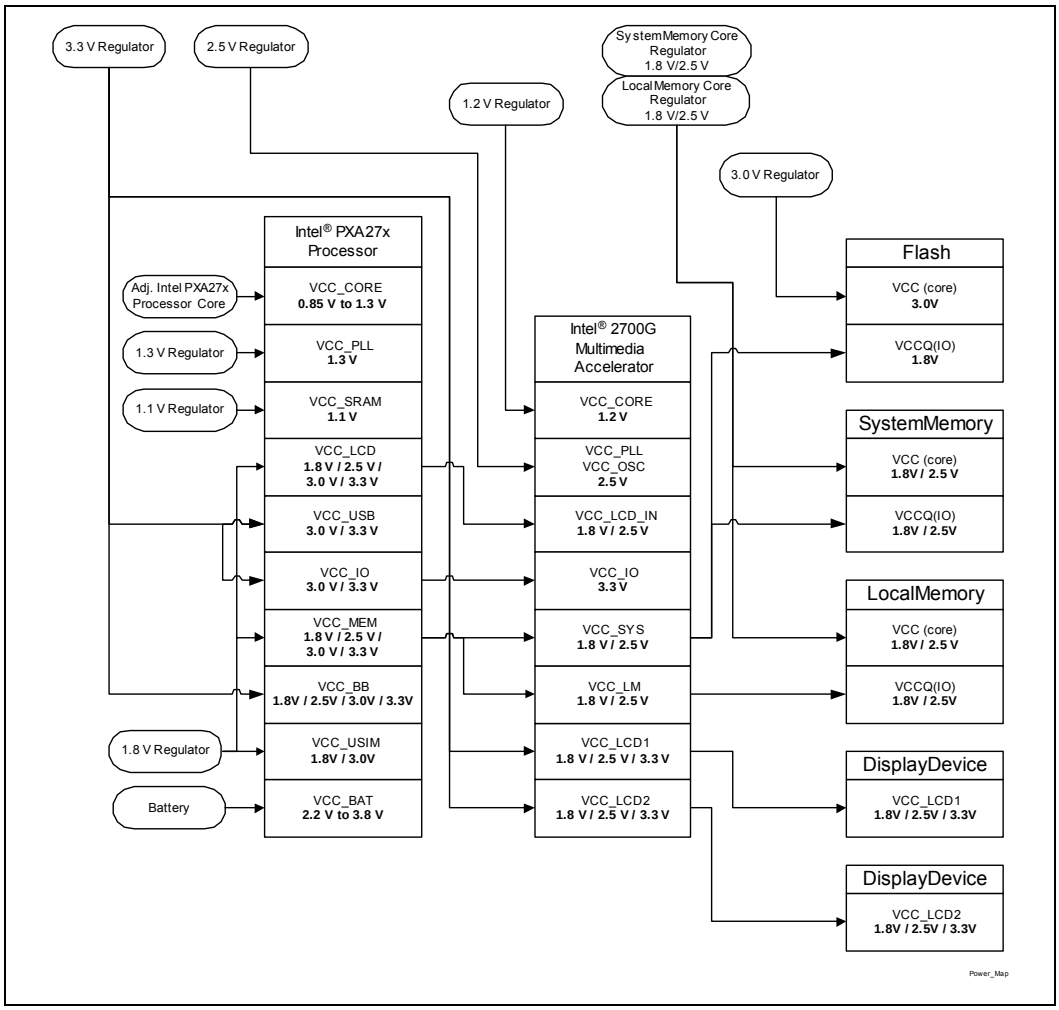
This chapter presents the power guidelines for a 2700G Multimedia Accelerator platform. Power delivery architecture, power supply decoupling, power sequencing, and power management are covered.

4.1 System Level Power Delivery

Figure 4-1 shows the power delivery architecture for an example 2700G Multimedia Accelerator platform.

Note: The solutions in this design guide are only examples. Many power distribution methods achieve the similar results. It is important to consider all system level implications to power delivery.

Figure 4-1. Intel® 2700G Multimedia Accelerator Platform Power Delivery Map



4.2 Intel® 2700G Multimedia Accelerator Power Delivery and Decoupling

4.2.1 Power Sequencing

The following 2700G Multimedia Accelerator-specific power sequencing requirements must be observed:

- Any I/O rail that is powered at 3.3 V (e.g., VCC_LCD1) must be tied to VCC_IO to ensure identical sequencing.
- Typical design practice has all power rails applied/removed as close in time as practical. If 2700G Multimedia Accelerator's rails can be brought up at roughly the same time, there are no specific sequencing requirements. However, if design limitations require significant delays between the application of power rails, then the 2700G Multimedia Accelerator's core power should be applied first.
- Additionally, the 3.3 V rail should be brought up no later than the other I/O rails.

4.2.2 Analog Power Delivery

There are two analog circuits that require filtered supplies on the 2700G Multimedia Accelerator: VCCA_CORE_PLL, VCCA_DISP_PLL and VAA_XTAL.

Figure 4-2. Example Analog Supply Filter for VCCA_CORE_PLL and VCCA_DISP_PLL

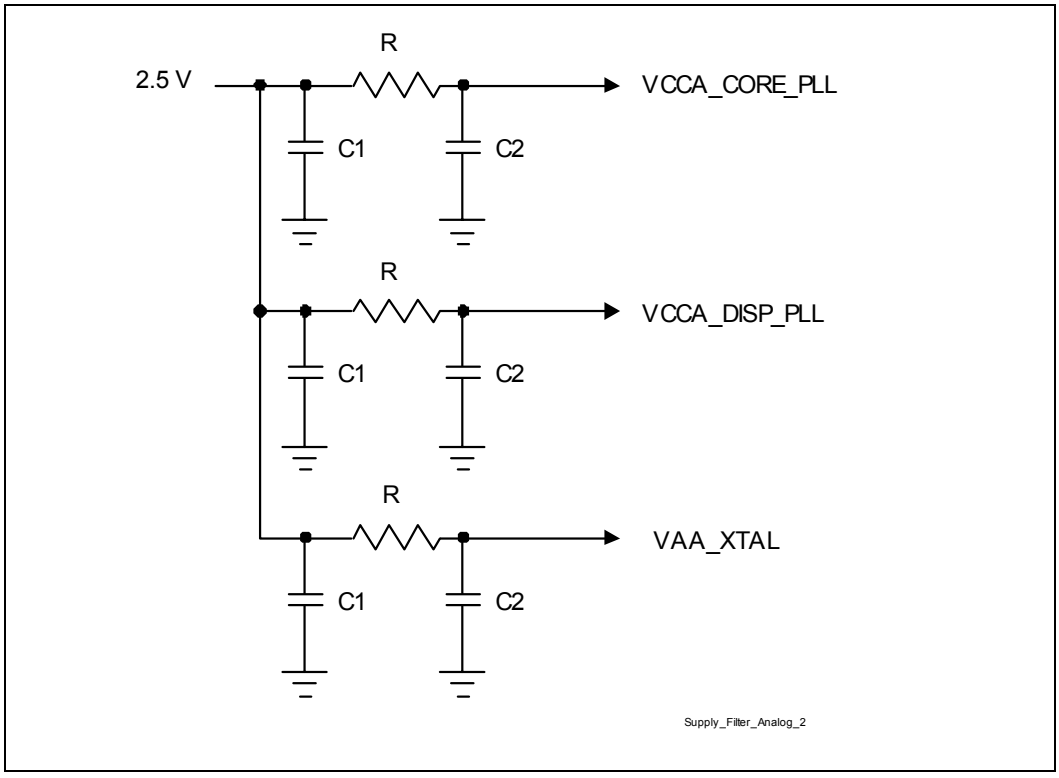


Table 4-1. Recommended Filter Components

Required Intel® 2700G Multimedia Accelerator Filters	R	C1	C2
VCCA_CORE_PLL	0 Ω	0.1 pF	0.1 pF
VCCA_DISP_PLL	0 Ω	0.1 pF	0.1 pF
VAA_XTAL	0 Ω	0.1 pF	0.1 pF

4.2.3 Power Delivery

Power may be delivered to the 2700G Multimedia Accelerator component primarily using two layers; although, floods on the top layer are also likely. Example power delivery scenarios are shown in the following figures.

Figure 4-3. Top Layer Power Delivery

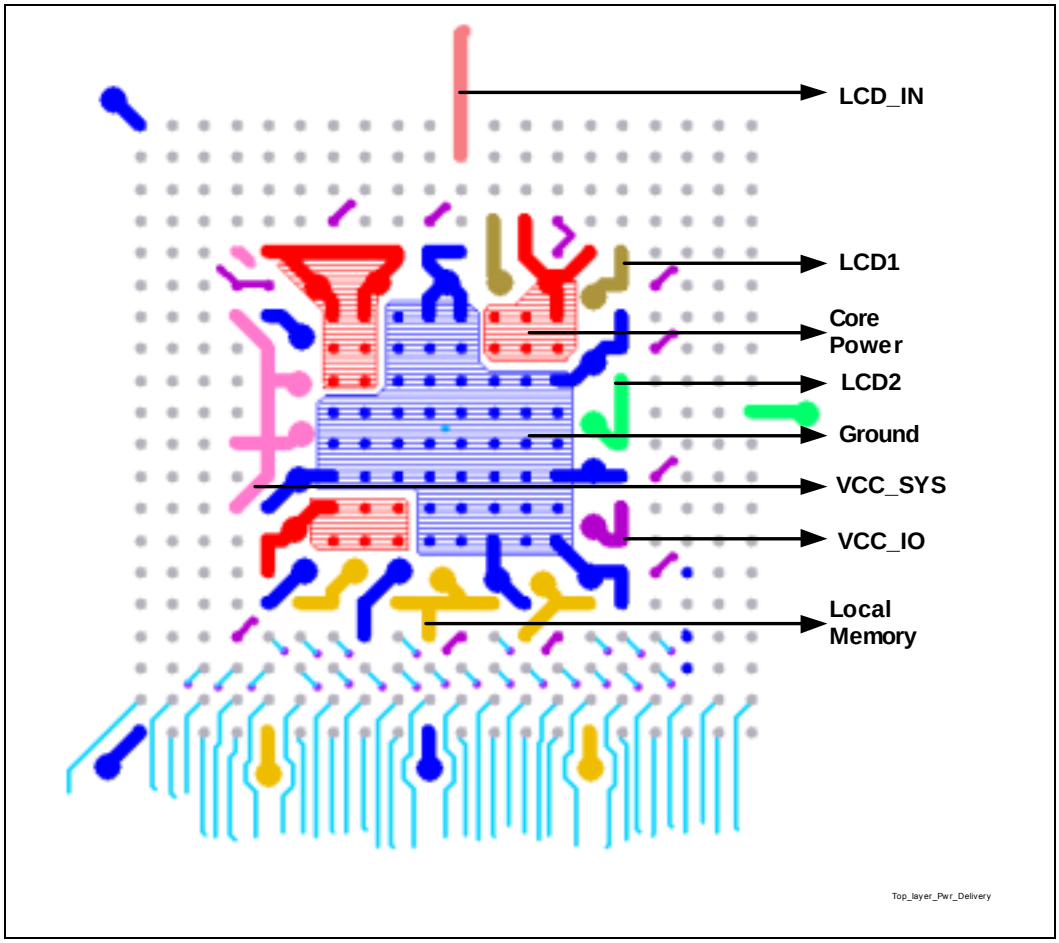


Figure 4-4. Power Delivery Layer A

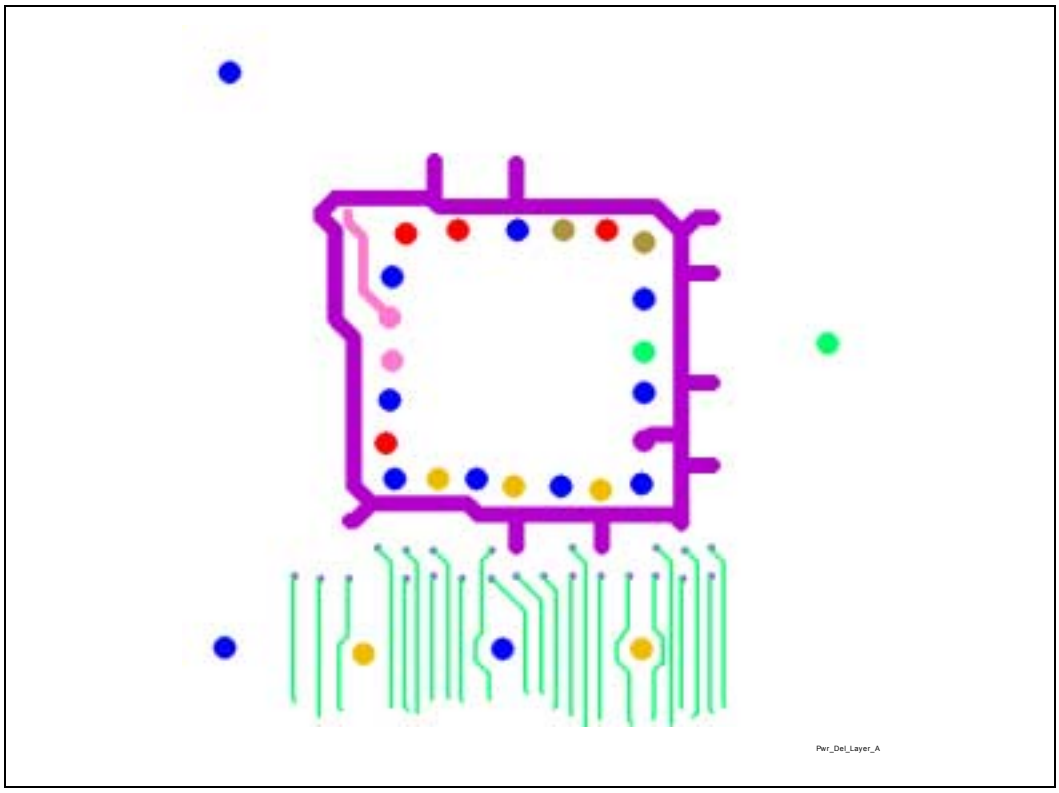
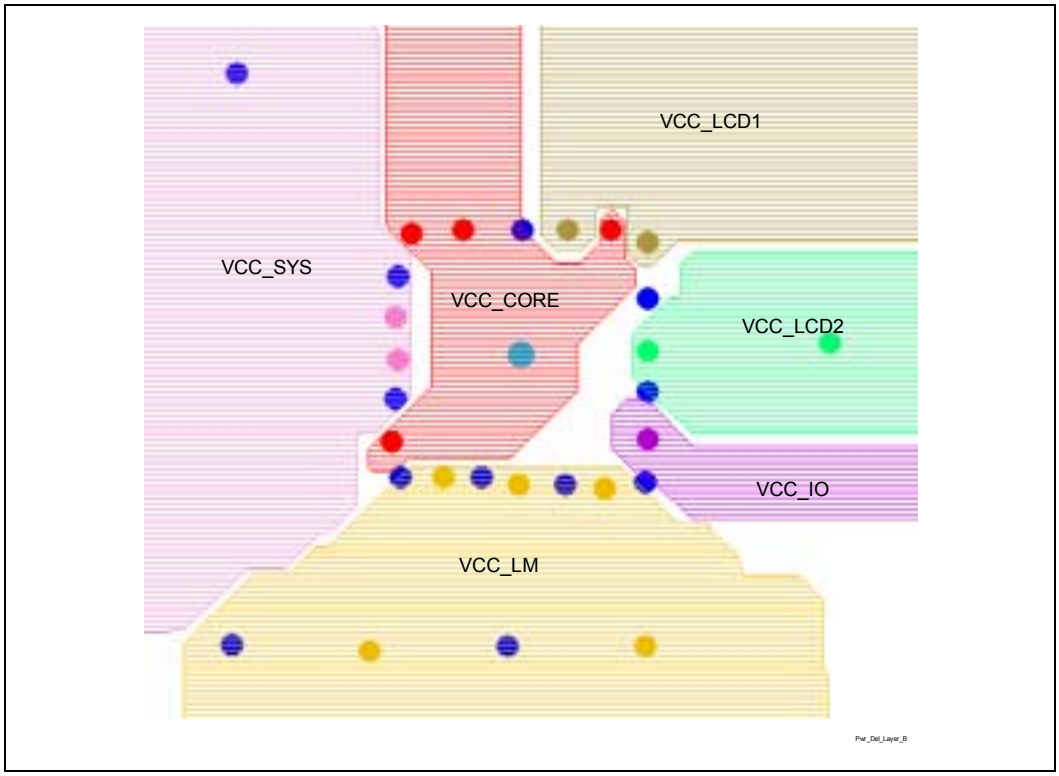


Figure 4-5. Power Delivery Layer B



4.2.4 Decoupling Capacitors

Table 4-2 and Table 4-3 shows examples of frequency and bulk capacitors for the 2700G Multimedia Accelerator.

Table 4-2. High Frequency Decoupling Recommendations

Pin	Decoupling Requirements
VCC_CORE	4 x 0.1 uF capacitor
VCC_SYS	3 x 0.1 uF capacitor
VCC_LM	3 x 0.1 uF capacitor
VCC_LCD_IN	1 x 0.1 uF capacitor
VCC_LCD1	2 x 0.1 uF capacitor
VCC_LCD2	2 x 0.1 uF capacitor
VCC_IO	1 x 0.1 uF capacitor

NOTE: Unless otherwise noted, capacitors should be placed less than 100 mils from the package.

Table 4-3. Bulk Decoupling Requirements

Pin	Decoupling Requirements
VCC_CORE	2 x 4.2 µF capacitor

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5 Design Guidelines

The main focus of the guidelines in this chapter is to minimize signal integrity problems on 2700G Multimedia Accelerator-based designs. The following guidelines are not intended to replace thorough system validation on 2700G Multimedia Accelerator-based products.

5.1 General System Bus

This section describes the design for the general system bus connection between the applications processor (specifically the PXA270 processor) and the 2700G Multimedia Accelerator. Note that this interface is used to communicate with a variety of system resources, including system memory and the Flash/ROM device. This section focuses only on the general system bus guidelines for connecting the 2700G Multimedia Accelerator to the processor's system bus. For complete design guidelines on the general system bus, refer to the application processor's design guide.

There are several protocols that run on the general system bus. The applications processor uses two of these protocols to communicate with the 2700G Multimedia Accelerator: *SRAM protocol* is only used for writes and *Variable Latency I/O* (VLIO) can be used for reads and writes. SRAM protocol is used for optimum write performance. This 32-bit bus operates at 1.8 V or 2.5 V and up to 133 MHz.

5.1.1 General System Bus Routing Guidelines

The following system bus signals need to be connected to the 2700G Multimedia Accelerator.

Table 5-1. Intel® 2700G Multimedia Accelerator-to-Intel® PXA270 Applications Processor General System Bus Connections

Intel® PXA 270 Applications Processor Signal Name	Intel® 2700G Multimedia Accelerator Signal Name
nCS[x], nCS[y] [1]	SYS_nCS[1:0]
MA[25:2]	SYS_MA[25:2]
MD[31:0]	SYS_MD[31:0]
nOE	SYS_nOE
RDnWR	SYS_RDnWR
nPWE	SYS_nPWE
nWE	SYS_nWE
nSDCAS	SYS_nCAS
DQM[3:0]	SYS_DQM[3:0]
RDY	SYS_RDY

NOTES:
1. The PXA270 processor has a total of 6 CS lines that can be used in a variety of configurations. When choosing which of the PXA270 processor's CS signals to connect to the 2700G Multimedia Accelerator, it is important to note that the 2700G Multimedia Accelerator's SYS_nCS0 is used for VLIO protocol transactions (read or write), and 2700G Multimedia Accelerator's SYS_nCS1 is used for SRAM protocol transactions. Refer to the application processor's design guide for additional details on the CS signals.

The following guidelines should be followed when routing the general system bus interface of the 2700G Multimedia Accelerator:

- General system bus signals should be routed using 60 Ω traces, with 10 mil (0.254 mm) spacing to neighboring signals.
- Trace widths and spacing can be less than 10 mils in the component (both 2700G Multimedia Accelerator and the applications processor) breakout regions, but should be spaced at 10 mils as much as possible. Within the breakout region, 3 mil (0.0762 mm) trace widths and 3 mils (0.0762 mm) spacing is permissible. The breakout region for each component should be less than 625 mils (15.75 mm).
- Where possible, try to keep data lines and their respective data mask signals routed on the same layer.
- Avoid routing over reference plane splits and voids.

Figure 5-1. General System Bus Topology 1

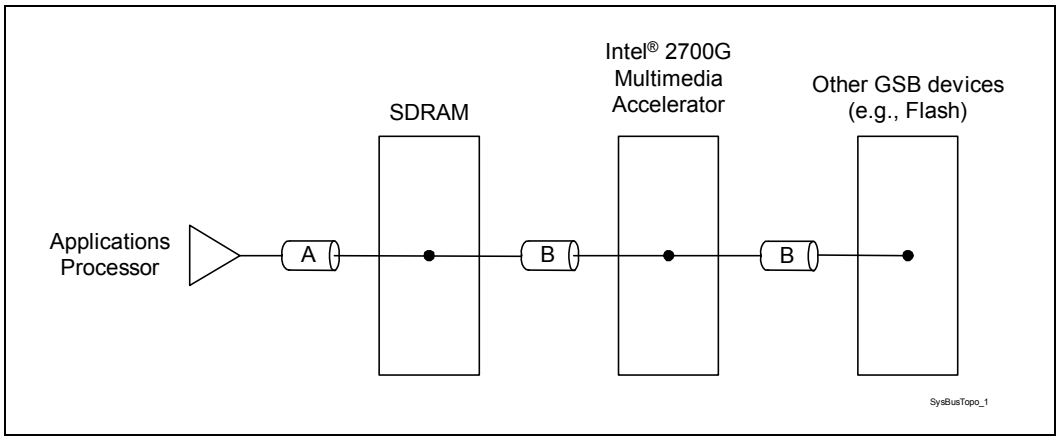


Table 5-2. General System Bus Routing Guidelines – Topology 1

Signal	Topo.	Trace		A		B	
		Z_O	Spacing	Min	Max	Min	Max
SYS_MA[25:2], SYS_MD[31:0], SYS_nWE, SYS_nCAS	1	60 Ω	10 mils; 0.254 mm	0.2 in; 5.08 mm	3.5 in; 77.47 mm	0.2 in; 5.08 mm	1.0 in; 25.4 mm

Figure 5-2. General System Bus – Topology 2

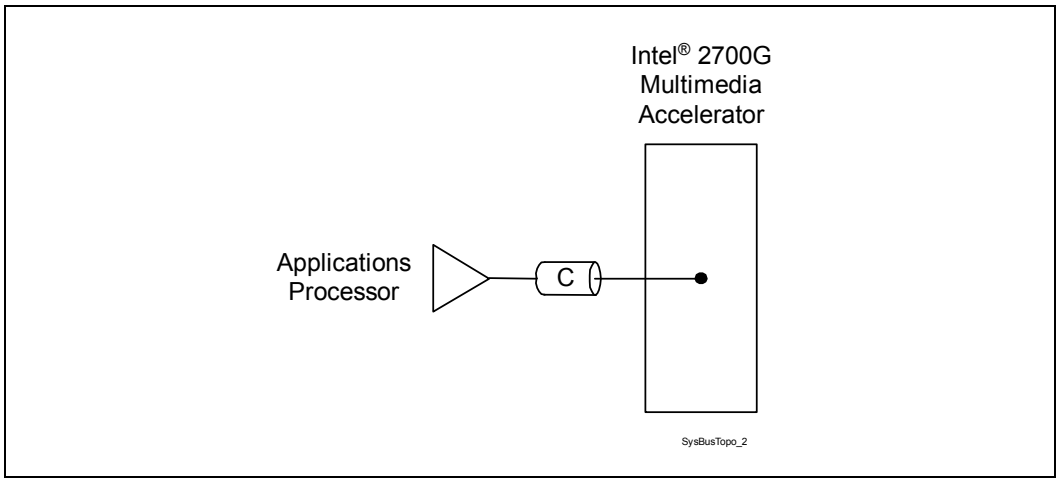


Table 5-3. General System Bus Routing Guidelines – Topology 2

Signal	Topo.	Trace		C	
		Z_O	Spacing	Min	Max
SYS_nCS[1:0]	2	60 Ω	10 mils; 0.254 mm	0.2 in; 5.08 mm	4.5 in; 114.3 mm

Figure 5-3. General System Bus – Topology 3

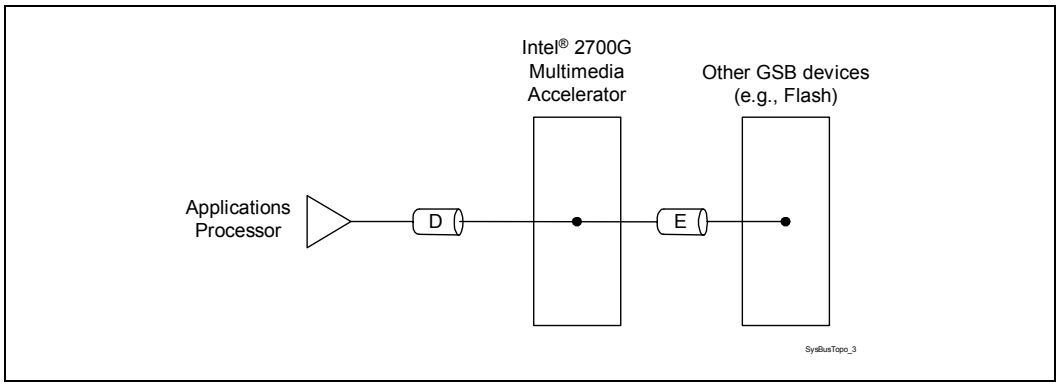


Table 5-4. General System Bus Routing Guidelines – Topology 3

Signal	Topo.	Trace		D		E	
		Z_O	Spacing	Min	Max	Min	Max
SYS_RDnWR, SYS_nPWE, SYS_nOE, SYS_RDY	3	60 Ω	10 mils; 0.254 mm	0.2 in; 5.08 mm	4.5 in; 114.3 mm	0.2 in; 5.08 mm	1.0 in; 25.4 mm

5.2 Local Memory Interface

This section describes the design for the local memory interface for the 2700G Multimedia Accelerator. The local memory interface can be connected to either a single x32 device, or two x16 devices. The local memory interface can support 1.8 V or 2.5 V signaling voltages. If operating at 1.8 V, the interface can run up to 100 MHz. If operating at 2.5 V, the interface can run up to 133 MHz.

5.2.1 Local Memory Routing Guidelines

5.2.1.1 Single x32-bit Device

Local memory Topologies 1 and 2 are used only when a single x32 bit SDRAM devices is used.

5.2.1.1.1 Local Memory Data, Address and Control (One x32 Device)

The following guidelines should be followed when routing the local memory interface of the 2700G Multimedia Accelerator:

- Local memory data, address and control should be using 60 Ω traces, with 7 mil (0.178 mm) spacing to neighboring signals. Spacing can be less than 7 mils in the component (both 2700G Multimedia Accelerator and the memory device) breakout regions, but should be spaced at 7 mils as much as possible. Within the breakout region, 3 mil (0.0762 mm) trace widths and 3 mils (0.0762 mm) spacing is permissible. The breakout region for each component should be less than 625 mils (15.75 mm).
- Care should be taken to match SDRAM interface signal lengths as closely as possible.
- Avoid routing over reference plane splits and voids.
- LM_CKE requires a 100 kΩ pull-down resistor to ground.

Figure 5-4. Local Memory – Topology 1

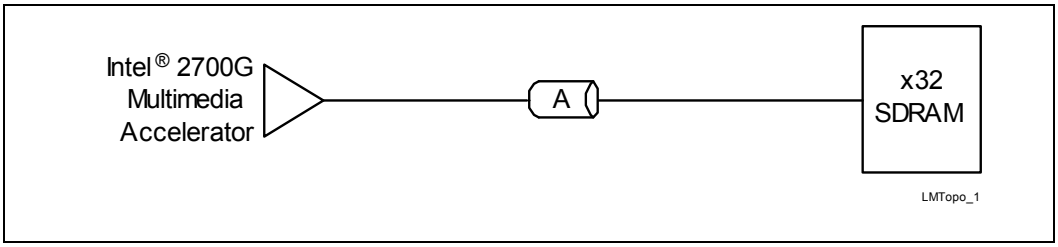


Table 5-5. Local Memory Data, Address and Control Routing Guidelines – Topology 1

Signal	Topo.	Trace		A	
		Z_O	Spacing	Min	Max
LM_D[31:0], LM_DQM[3:0], LM_A[12:0], LM_nWE, LM_nCS, LM_nRAS, LM_nCAS, LM_BA[1:0], LM_CKE	1	60 Ω	7 mils; 0.178 mm	0. 5 in; 12.7 mm	4.5 in; 114.3 mm

5.2.1.1.2 Local Memory Clock (One x32 Device)

The following guidelines should be followed when routing the 2700G Multimedia Accelerator's local memory clock:

- The local memory clock signal should be routed using 60 Ω traces, with 7 mil (0.178 mm) spacing to neighboring signals. Spacing can be less than 7 mils in component (both 2700G Multimedia Accelerator and the memory device) breakout regions, but should be 7 mils as much as reasonably possible.
- For maximum timing margins, the total LM_CLK length (B+C) should be tuned to slightly less than half the midpoint of data, address and control lengths. For example, if data, address and control signals are between 2 inches and 3 inches in total length, LM_CLK should be tuned to 2.4 inches.
- To decrease overshoot and ringback, a series resistor needs to be added between the LM_CLK and the x32 memory device. A 22 Ω resistor is recommended to be placed less than an inch from the 2700G Multimedia Accelerator.
- For normal operation, the LM_RCLK signal shall be connected to a pull-down resistor (100 kΩ).

Figure 5-5. Local Memory Clocks – Topology 2

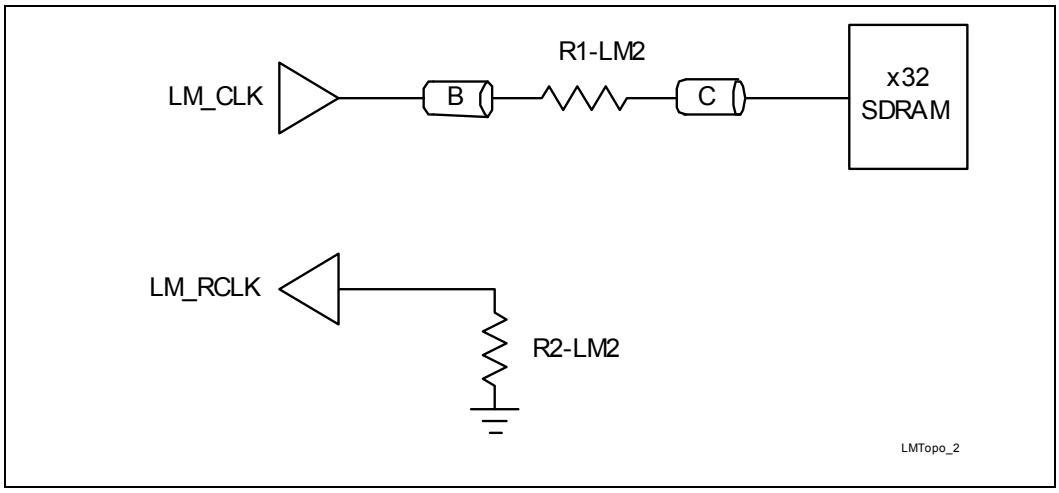


Table 5-6. Local Memory Clock Routing Guidelines – Topology 2

Signal	Topo.	Trace		B		C	
		Z_O	Spacing	Min	Max	Min	Max
LM_CLK	2	60 Ω	7 mils; 0.178 mm	0.0 in; 0.0 mm	1.0 in; 25.4 mm	0.25 in; 6.35 mm	3.5 in; 95.25 mm

NOTE: Actual LM_CLK lengths should be calculated based on the lengths of the data, address, and control signals.

Table 5-7. Local Memory Clock Routing Component Recommendations – Topology 2

Component	Value	Tolerance	Package Type
R1-LM2	22 Ω	± 5%	402 or 603
R2-LM2	100 kΩ	± 5%	402 or 603

5.2.1.2 Two x16-bit Devices

Local memory topologies 3, 4, and 5 are used only when two x16 bit SDRAM devices are used. Total local memory sizes of 16 MB, 32 MB, and 64 MB are supported in this configuration (dependent on SDRAM device configuration).

5.2.1.2.1 Local Memory Data (Two x16 Devices)

The following guidelines should be followed when routing the local memory interface of the 2700G Multimedia Accelerator:

- Local memory data signals should be routed using 60 Ω traces, with 7 mil (0.178 mm) spacing to neighboring signals. Spacing can be less than 7 mils in the component (both 2700G Multimedia Accelerator and the memory device) breakout regions, but should be spaced at 7 mils as much as possible. Within the breakout region, 3 mil (0.0762 mm) trace widths and 3 mils (0.0762 mm) spacing is permissible. The breakout region for each component should be less than 625 mils (15.75 mm).
- Care should be taken to match SDRAM interface signal lengths as closely as possible.
- Avoid routing over reference plane splits and voids.

Figure 5-6. Local Memory – Topology 3

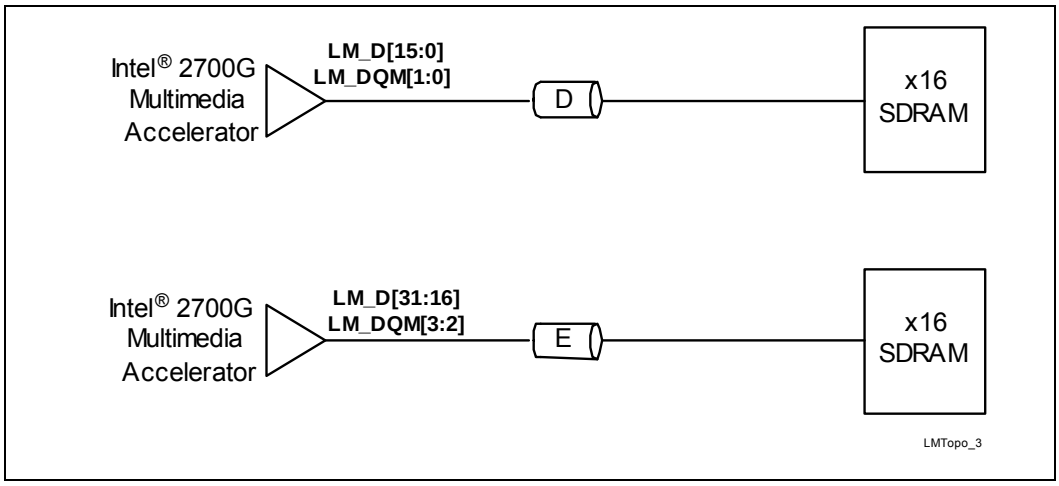


Table 5-8. Local Memory Data Routing Guidelines – Topology 3

Signal	Topo.	Trace		D, E	
		Z_O	Spacing	Min	Max
LM_D[31:0]	3	60 Ω	7 mils; 0.178 mm	0. 5 in; 12.7 mm	4.5 in; 114.3 mm

When routing this topology, make sure to keep DQMs aligned with the appropriate data byte. LM_DQM-to-LM_D mapping is shown in Table 5-9.

Table 5-9. Data Mask to Data Byte Mapping

Data Mask Signal	Corresponding Data Signals
LM_DQM0	LM_D[7:0]
LM_DQM1	LM_D[15:8]
LM_DQM2	LM_D[23:16]
LM_DQM3	LM_D[31:24]

5.2.1.2.2 Local Memory Address and Control (Two x16 Devices)

The following guidelines should be followed when routing the local memory interface of the 2700G Multimedia Accelerator:

- Local memory address and control signals should be routed using 60 Ω traces, with 7 mil (0.178 mm) spacing to neighboring signals. Spacing can be less than 7 mils in the component (both 2700G Multimedia Accelerator and the memory device) breakout regions, but should be spaced at 7 mils as much as possible. Within the breakout region, 3 mil (0.0762 mm) trace widths and 3 mils (0.0762 mm) spacing is permissible. The breakout region for each component should be less than 625 mils (15.75mm).
- Ensure that the stub lengths (segments G) to the SDRAM devices are equal.
- Care should be taken to match SDRAM interface signals as closely as possible.
- Avoid routing over reference plane splits and voids.
- LM_CKE requires a 100 kΩ pull-down resistor to ground.

Figure 5-7. Local Memory – Topology 4

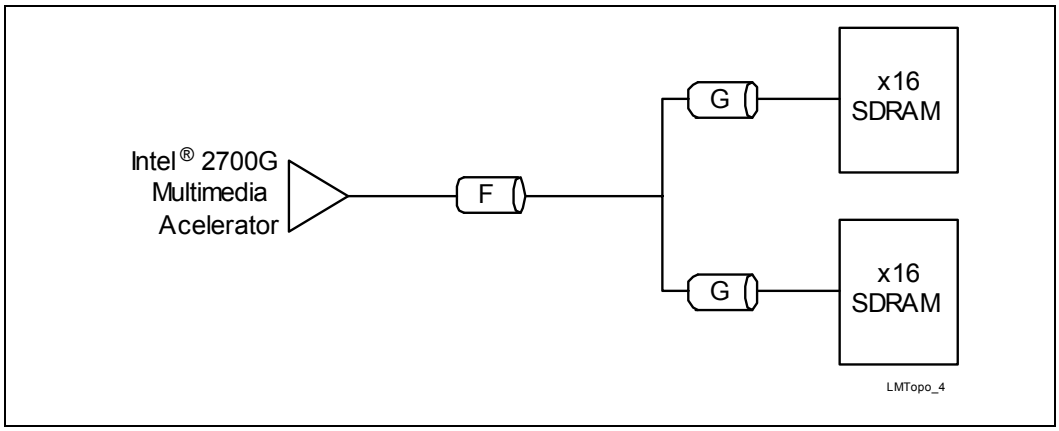


Table 5-10. Local Memory Address and Control Routing Guidelines – Topology 4

Signal	Topo.	Trace		F		G	
		Z_O	Spacing	Min	Max	Min	Max
LM_A[12:0], LM_nWE, LM_nCS, LM_nRAS, LM_nCAS, LM_BA[1:0], LM_CKE	4	60 Ω	7 mils; 0.178 mm	0.25 in; 6.35 mm	3.0 in; 76.2 mm	0.25 in; 6.35 mm	1.5 in; 38.1 mm

5.2.1.2.3 Local Memory Clock (Two x16 Devices)

The following guidelines should be followed when routing the local memory clock of the 2700G Multimedia Accelerator:

- The local memory clock signal should be routed using 60 Ω traces, with 7 mil (0.178 mm) spacing to neighboring signals. Spacing can be less than 7 mils in component (both 2700G Multimedia Accelerator and the memory device) breakout regions, but should be 7 mils as much as reasonably possible.
- To decrease overshoot and ringback, a series resistor needs to be added between the LM_CLK and the T-Section to the two x16 memory devices. A 22 Ω resistor is recommended to be placed within one inch from the 2700G Multimedia Accelerator.
- For maximum timing margins, the total LM_CLK length (H+J+K) should be tuned to slightly less than half the midpoint of data, address, and control lengths. For example, if data, address, and control signals are between 2 inches and 3 inches in total length, LM_CLK should be tuned to 2.4 inches.
- Ensure that the stub lengths (segments K) to the SDRAM devices are equal.
- For normal operation, LM_RCLK shall be connected to a pull-down resistor (100 kΩ).

Figure 5-8. Local Memory Clock – Topology 5

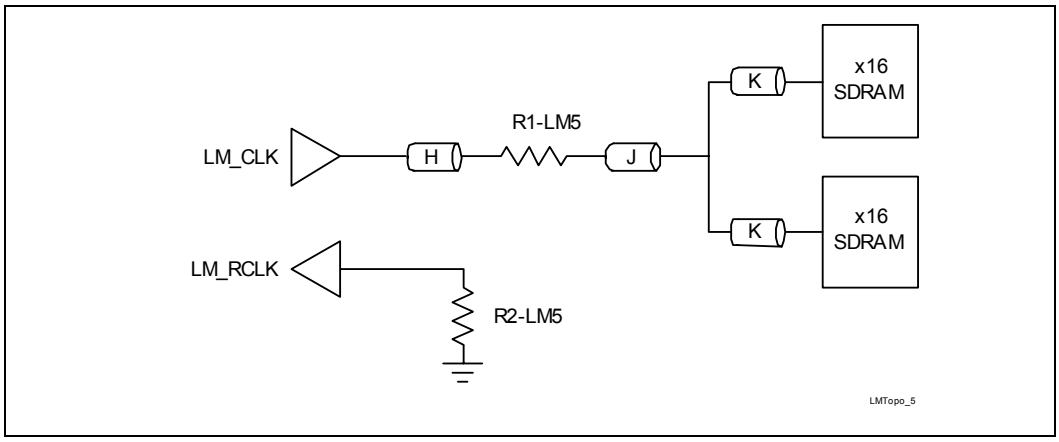


Table 5-11. Local Memory Clock Routing Guidelines – Topology 5

Signal	Topo.	Trace		H		J		K	
		Z_O	Spacing	Min	Max	Min	Max	Min	Max
LM_CLK	5	60 Ω	7 mils; 0.178 mm	0.25 in; 6.35 mm	1.0 in; 25.4 mm	0.5 in; 12.7 mm	2.5 in; 63.5 mm	0.25 in; 6.35 mm	1.0 in; 25.4 mm

Table 5-12. Local Memory Clock Routing Component Recommendations – Topology 6

Component	Value	Tolerance	Package Type
R1-LM5	22 Ω	± 5%	402 or 603
R2-LM5	100 kΩ	± 5%	402 or 603

5.2.2 Local Memory Decoupling Requirements

In addition to the minimum decoupling capacitors described in Section 4.2.4, the designer should place bypass capacitors at vias that transition the local memory signals from one reference signal plane to another. One 0.01-uF capacitor is recommended per 8 vias. The capacitor should be placed as close as possible to the center of the via field.

5.2.3 Leaving the Local Memory Interface Unconnected

If the system does not make use of the 2700G Multimedia Accelerator's local memory interface, the following guidelines should be followed:

- LM_RCLK shall have a 100 kΩ pull-down resistor to ground.
- LM_D[31:0] shall each have a 100 kΩ pull-down resistor to ground (Rpacks are acceptable).
- All other LM signals may be left as NCs (no-connects).
- VCC_LM must still be applied at either 1.8 V or 2.5 V.

5.3 Primary and Auxiliary LCD Output Interfaces

This section describes the design for the primary and auxiliary LCD output interfaces for the 2700G Multimedia Accelerator. Each of these interfaces will be electrically driven by the 2700G Multimedia Accelerator; however, the data being driven may originate with either the 2700G Multimedia Accelerator or the applications processor. If the data originates with the applications processor, it will be driven to the 2700G Multimedia Accelerator via its LCD input interface (discussed in Section 5.4). The 2700G Multimedia Accelerator will then redirect that display data stream to the appropriate LCD output interface.

Note: In this document, LCD1 refers to the Primary LCD, LCD2 refers to the Secondary LCD and LCDx refers to both the Primary and the Secondary LCD.

Note: The connectivity from the 2700G Multimedia Accelerator to the LCD panel (or intermediate device) should always follow the recommendations outlined here, regardless if the data being driven originates with the 2700G Multimedia Accelerator or the applications processor.

Each LCD output interface can drive either an active (TFT) display, or an intermediate device that translates the display stream from the LCD output format to another display format (e.g., TMDS for DVI connector, or analog RGB for 15-pin VGA connector). Each LCD output can run at a 1.8 V, 2.5 V, or 3.3 V signaling level. The 2700G Multimedia Accelerator supports 16-bpp, 18-bpp or 24-bpp color depth displays. The connections to active panel displays will vary depending on the color depth that the display supports. For example, a 16-bpp display will connect to the 2700G Multimedia Accelerator's LCD output differently than a 24-bpp display.

This section provides routing guidelines and example connectivity for 16-bpp, 18-bpp, 24-bpp active displays, as well as to intermediate (e.g., LCD-to-TMDS) devices. These guidelines apply to both the primary and auxiliary LCD outputs of the 2700G Multimedia Accelerator.

5.3.1 Strapping Options

The 2700G Multimedia Accelerator implements strapping options on the LCD signals. Refer to Section 5.5.2 for more details.

5.3.2 LCD Output Routing Guidelines

The following guidelines should be followed when routing the LCD output interfaces of the 2700G Multimedia Accelerator:

- LCD output pixel clocks (LCDx_PCLK) should be routed using 60 Ω traces, with 7 mil (0.178 mm) spacing to neighboring signals. Spacing can be less than 7 mils in the component (both the 2700G Multimedia Accelerator and the LCD connector or intermediate device) breakout regions, but should be spaced at 7 mils as much as reasonably possible. Within the breakout region, 3 mil (0.0762 mm) trace widths and 3 mil (0.0762 mm) spacing is permissible. The breakout region should be less than 625 mils (15.75 mm).
- LCD output data signals (LCDx_DD[23:0]), along with the control signals LCDx_LCLK, LCDx_FCLK, and LCDx_DEN should be routed 5 mils (0.127 mm) wide, with 7 mil (0.178 mm) spacing to neighboring signals. Spacing can be less than 7 mils in the component (both the 2700G Multimedia Accelerator and the LCD connector or intermediate device) breakout regions, but should be spaced at 7 mils as much as reasonably possible. Within the breakout region, 3 mil (0.0762 mm) trace widths and 3 mil (0.0762 mm) spacing is permissible. The breakout region for should be less than 625 mils (15.75 mm).
- These signals should be matched to the associated LCDx_PCLK to within ±500 mils (12.7 mm) of the associated LCDx_PCLK signal. Also, the primary LCD signal lengths do not impact the secondary LCD signal lengths.
- Avoid routing over reference plane splits and voids.

Figure 5-9. LCD Outputs – Topology 1

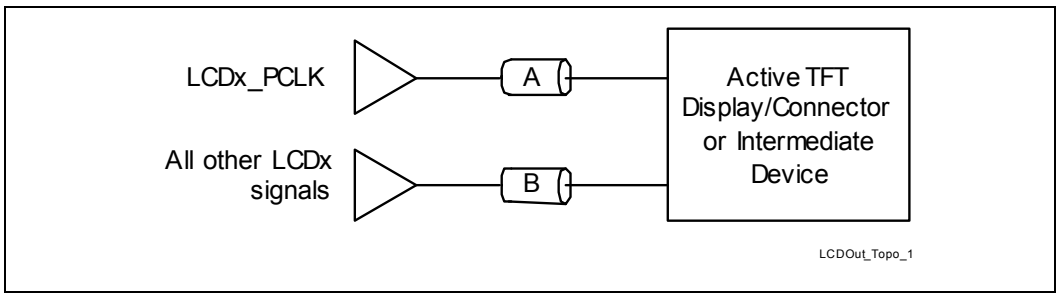


Table 5-13. LCD Output Routing Guidelines – Topology 1

Signal	Topo.	Trace		A (LCDx_PCLK)		B	
		Width	Spacing	Min	Max	Min	Max
LCDx_PCLK, LCDx_FCLK, LCDx_LCLK, LCDx_DEN, LCDx_DD[23:0]	1	5 mils; 0.127 mm	7 mils; 0.178 mm	0.2 in; 5.08 mm	7.5 in; 190.5 mm	0.2 in; 5.08 mm	7.5 in; 190.5 mm

NOTE: All B segments should match the A segment (LCDx_PCLK) within 500 mils (12.7 mm).

5.3.2.1 Intermediate Device (RGB DAC, TMDS or TV Encoder)

If a display format other than that used for active TFTs is desired (e.g., analog RGB or TMDS), it is possible to solder intermediate devices down on the system board (or attach via a daughter card or dongle). The 2700G Multimedia Accelerator's LCD output interfaces have variable signaling voltages. Since each interface can run at 1.8 V, 2.5 V, or 3.3 V, care should be taken to ensure that the intermediate device can operate at one of these signaling levels. Signaling voltage for the primary LCD output interface is independent of the signaling voltage for the auxiliary LCD output interface. The interface signaling voltages of both LCD outputs are also independent of the LCD input signaling voltage.

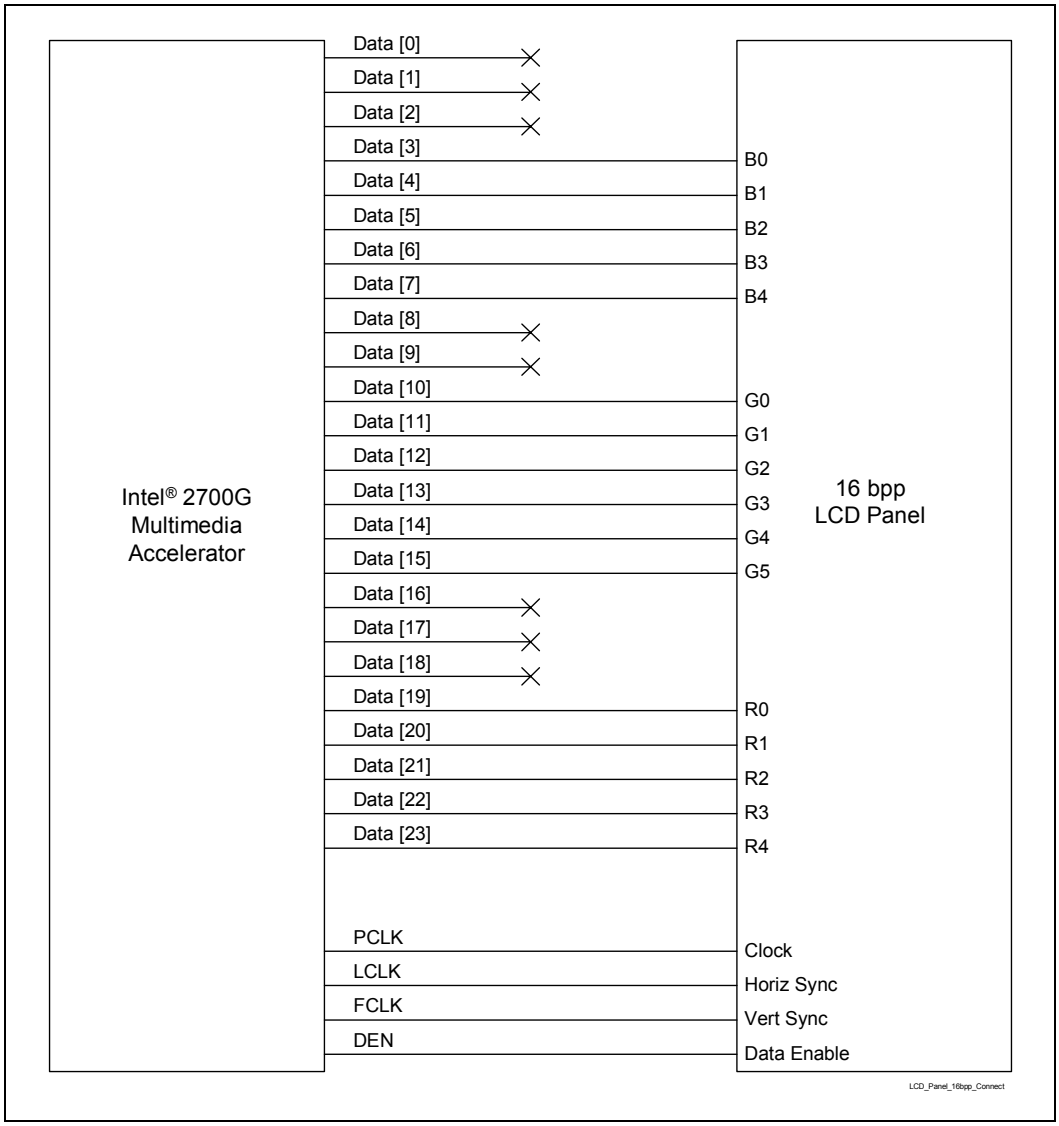
Each interface can support display resolutions up to 1280x1024 @ 60 Hz refresh at 16-bpp color depth (1024x768 @ 60 Hz for 24bpp). The 2700G Multimedia Accelerator LCD output ports are capable of interfacing with a wide variety of intermediate devices (e.g., discrete TMDS transmitter, LVDS transmitter, or analog RGB transmitter).

For device specific recommendations on power delivery and routing guidelines (from the device to the display), refer to the design documentation of the intermediate device.

5.3.2.2 16-bit Active LCD

The typical 16-bit LCD uses 5 bits for red, 6 bits for green, and 5 bits for blue pixel data; however, this can vary by display and is controlled by software. The format used by the panel determines which signals are connected from the 2700G Multimedia Accelerator. Consult the LCD panel manufacturer's documentation for panel specific details. This example assumes a 565 format.

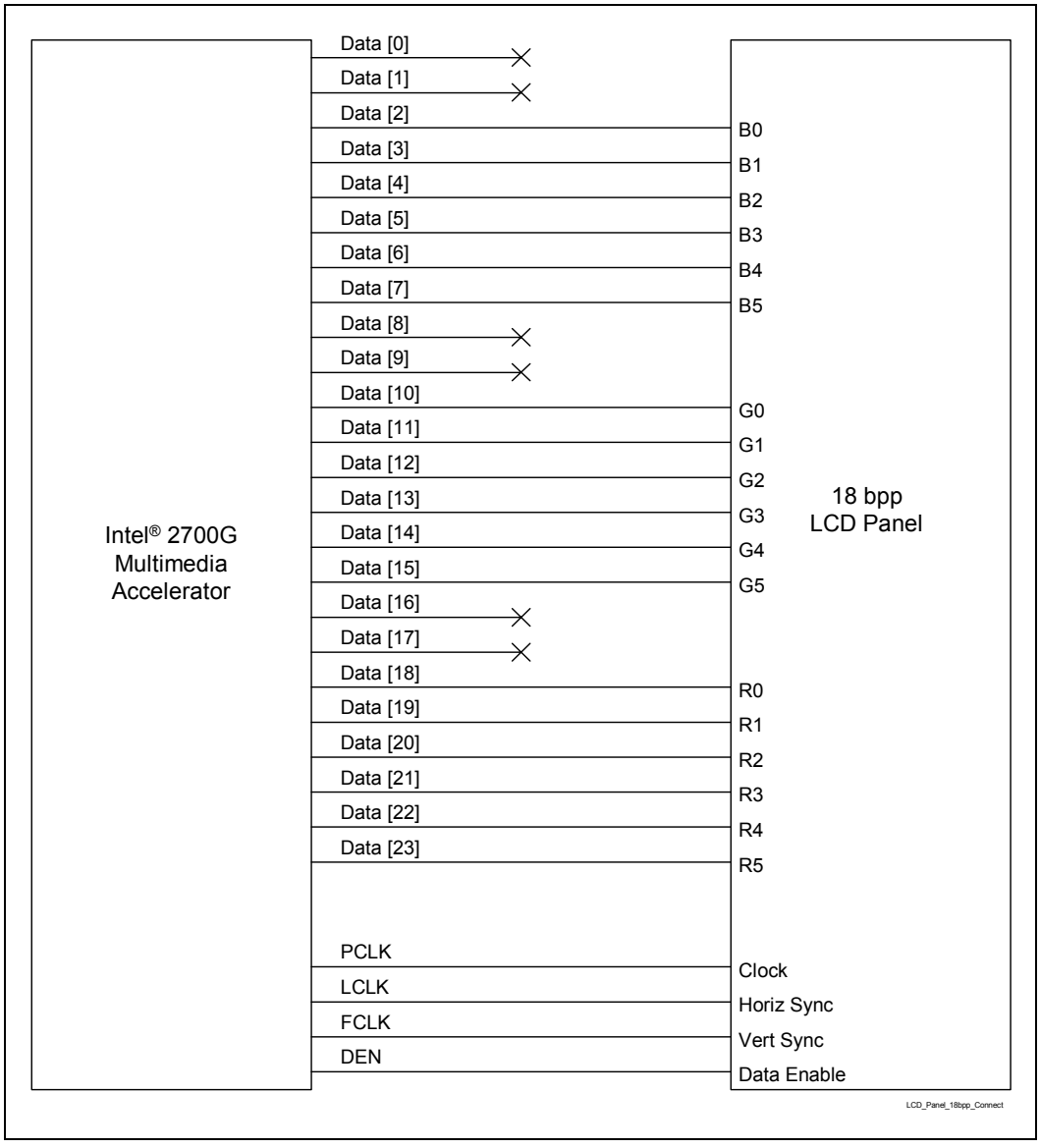
Figure 5-10. Intel® 2700G Multimedia Accelerator Connectivity to 16-bpp LCD Panel



5.3.2.3 18-bit Active LCD

A typical 18-bit LCD uses 6 bits for red, 6 bits for green, and 6 bits for blue pixel data. The format used by the panel determines which signals are connected from the 2700G Multimedia Accelerator. Consult the LCD panel manufacturer's documentation for panel specific details. This example assumes a 666 format.

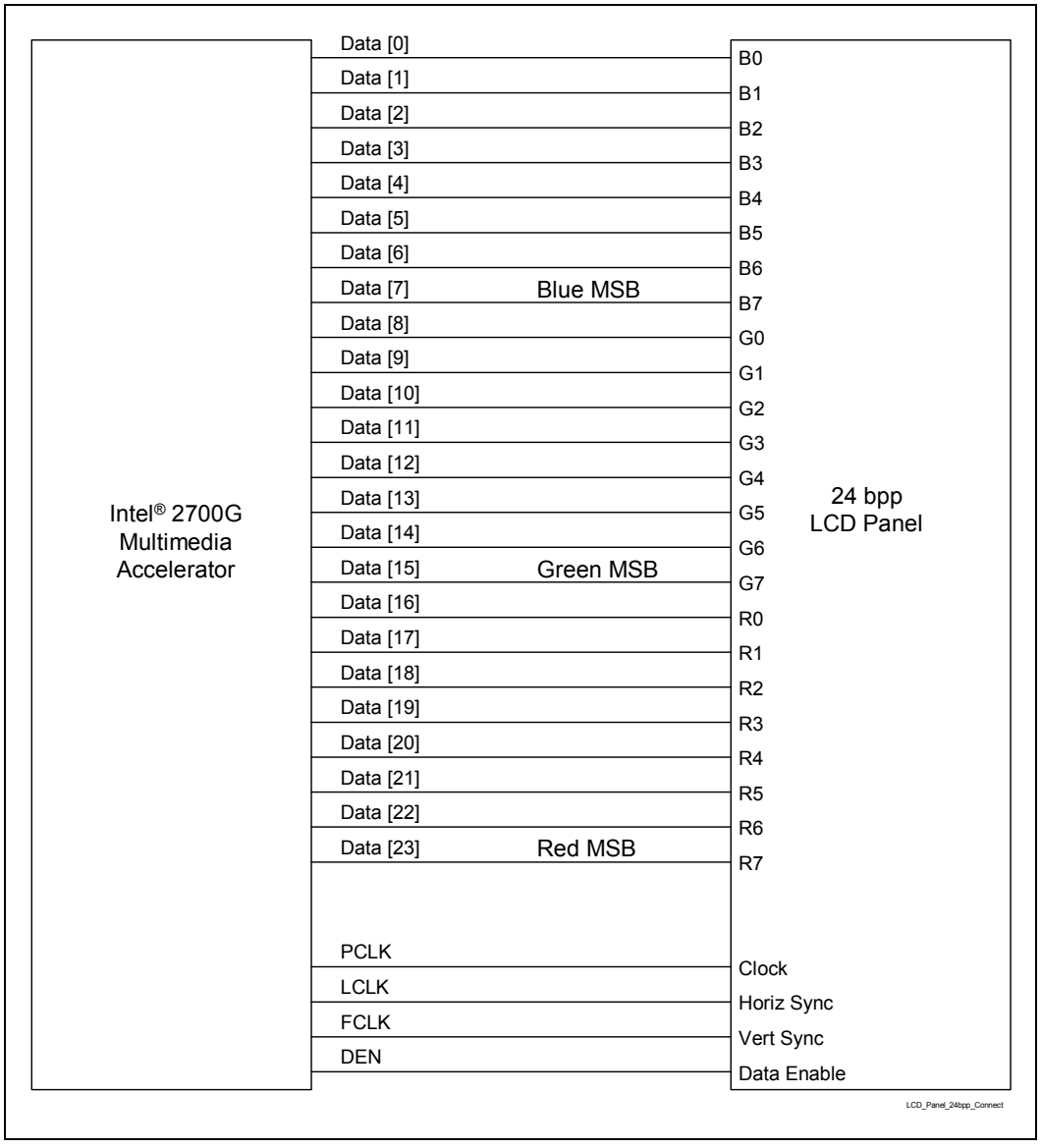
Figure 5-11. Intel® 2700G Multimedia Accelerator Connectivity to 18-bpp LCD Panel



5.3.2.4 24-bit Active LCD

The typical 24-bit LCD uses 8 bits for red, 8 bits for green, and 8 bits for blue pixel data; however, this can vary by display. The format used by the panel determines which signals are connected from the 2700G Multimedia Accelerator. Consult the LCD panel manufacturer's documentation for panel specific details. This example assumes an 888 format.

Figure 5-12. Intel® 2700G Multimedia Accelerator Connectivity to 24-bpp LCD Panel



5.3.3 Pulse Width Modulators

To allow control of the LCD backlight, independent of the state of the application processor, the 2700G Multimedia Accelerator provides two independently programmable pulse width modulators (PWMs). One PWM is intended for the primary LCD output and the second PWM is intended for the auxiliary LCD output. They are functionally and electrically interchangeable.

The pulse width modulator frequency is based on the 13 MHz external input clock. The frequency range supported (using a 50% duty cycle) is 198.3 Hz to 6.5 MHz. The specific registers used to program the PWMs are contained in the *Intel® 2700G Multimedia Accelerator Datasheet*.

The intent is for LCD1_PWM to be used with the primary LCD output (e.g., the LCD on a PDA) and for LCD2_PWM to be used with the auxiliary LCD output, and the drivers will support this configuration.

5.3.4 Leaving the LCD Output Unconnected

If the system does not make use of one of the 2700G Multimedia Accelerator's LCD output interfaces, the following guidelines should be followed:

- If LCD1 is left unconnected, individual strapping resistors, as discussed in Section 5.5.2, are still required on LCD1_DD[2:0].
- All other applicable LCDx signals may be left as NCs (no-connects).
- The applicable VCC_LCDx shall still be applied at 1.8 V, 2.5 V, or 3.3 V.

5.4 LCD Input

This section describes the design for the LCD input interface to the 2700G Multimedia Accelerator. This interface connects to the LCD output of the applications processor to allow a display stream driven by the applications processor to be redirected out one of the 2700G Multimedia Accelerator's output LCD interfaces (refer to Section 5.3).

The LCD input interface can run at a 1.8 V or 2.5 V signaling. The LCD input signaling voltage is independent of the LCD output signaling voltage (i.e., 2700G Multimedia Accelerator's LCD input signaling voltage is not impacted by the signaling voltage used by the 2700G Multimedia Accelerator to drive the intermediate device or LCD). The 2700G Multimedia Accelerator supports only active TFT displays at color depths of 16 bpp, 18 bpp, or 24 bpp on its LCD outputs. The LCD input will be remapped to the appropriate 2700G Multimedia Accelerator LCD output. Note that the 2700G Multimedia Accelerator cannot support the triple-pumped 24-bit format supported by some applications processors. If the display stream from the applications processor is re-routed by the 2700G Multimedia Accelerator to a 24-bit display, the applications processor will need to drive it as a 16-bit or 18-bit display. Regardless of display type being driven (16-bpp vs. 24-bpp vs. intermediate device), the LCD interface should follow the connectivity and routing guidelines detailed in this section.

5.4.1 LCD Input Routing Guidelines

The LCD input signals listed in Table 5-14 should be connected to the 2700G Multimedia Accelerator.

Table 5-14. Intel® 2700G Multimedia Accelerator-to-Applications Processor LCD Input Connections

Applications Processor Signal Name	Intel® 2700G Multimedia Accelerator Signal Name
L_PCLK_WR	LCD_IN_PCLK
L_FCLK_RD	LCD_IN_FCLK
L_LCLK_A0	LCD_IN_LCLK
L_BIAS	LCD_IN_DEN
LDD[17:0]	LCD_IN_DD[17:0]

The following guidelines should be followed when routing the LCD input interface from the applications processor to the 2700G Multimedia Accelerator:

- LCD input pixel clock (LCD_IN_PCLK) should be routed 60 Ω traces, with 7 mil (0.178 mm) spacing to neighboring signals. Spacing can be less than 7 mils in the component (both 2700G Multimedia Accelerator and the applications processor) breakout regions, but should be spaced at 7 mils as much as reasonably possible. Within the breakout region, 3 mil (0.0762 mm) trace widths and 3 mil (0.0762 mm) spacing is permissible. The breakout region for each component should be less than 625 mils (15.75 mm).
- LCD input data signals (LCD_IN_DD[17:0]), along with the control signals LCD_IN_LCLK, LCD_IN_FCLK, and LCD_IN_DEN should be routed 5 mils (0.127 mm) wide, with 7 mil (0.178 mm) spacing to neighboring signals. Spacing can be less than 7 mils in the component (both 2700G Multimedia Accelerator and the applications processor) breakout regions, but should be spaced at 7 mils as much as possible. Within the breakout region, 3 mil (0.0762 mm) trace widths and 3 mil (0.0762 mm) spacing is permissible. The breakout region for each component should be less than 625 mils (15.75mm).
- The maximum trace length for the LCD data and control signals is 7.5 inches. These signals should each be matched within ±500 mils (12.7 mm) of the LCD_IN_PCLK signal.
- Avoid routing over reference plane splits and voids.

Figure 5-13. LCD Input – Topology 1

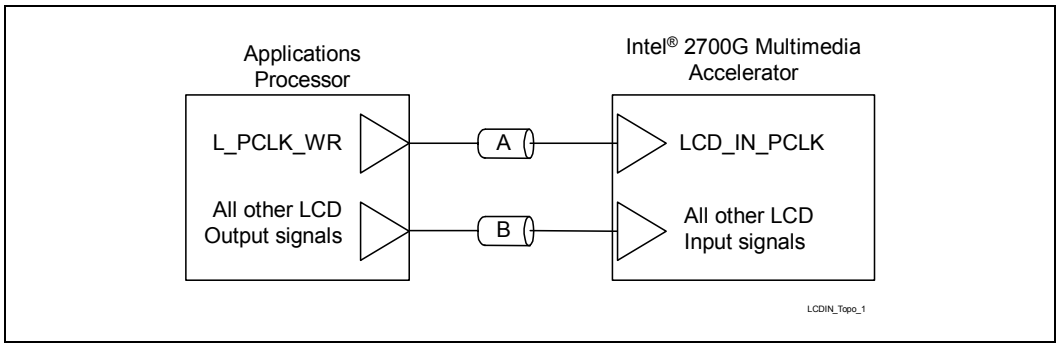


Table 5-15. LCD Input Routing Guidelines – Topology 1

Signal	Topo.	Trace		A		B	
		Width	Spacing	Min	Max	Min	Max
LCD_IN_PCLK, LCD_IN_FCLK, LCD_IN_LCLK, LCD_IN_DEN, LCD_IN_DD[17:0]	1	5 mils; 0.127 mm	7 mils; 0.178 mm	0.2 in; 5.08 mm	7.5 in; 190.5 mm	0.2 in; 5.08 mm	7.5 in; 190.5 mm

NOTE: All B segments should match the A segment (LCD_IN_PCLK) within 500 mils (12.7 mm).

5.4.2 Leaving the LCD Input Unconnected

If the system does not make use of the 2700G Multimedia Accelerator's LCD input interface, the following guidelines should be followed:

- If left unconnected, the 2700G Multimedia Accelerator's LCD input signals must be individually pulled down to ground via 100 kΩ resistors (RPacks are acceptable).
- To avoid the use of additional termination components, it is possible to use the applications processor's LCD output as "termination". Instead of using pull-down resistors, the 2700G Multimedia Accelerator's unused LCD input may be connected to the applications processor's LCD output. This scenario is only applicable if the application processor's LCD pins are not re-used as GPIOs.
- VCC_LCD_IN shall still be applied at either 1.8 V or 2.5 V.

5.5 Clocks, Reset, and Straps

This section describes the design for the 2700G Multimedia Accelerator's clock, reset, straps, and various other miscellaneous signals.

5.5.1 Clock Routing Guidelines

The 2700G Multimedia Accelerator generates its internal clocks from an external 13 MHz reference source. This reference may be derived from either an external crystal or a reference clock. If a crystal is used, XTAL_IN is the input from the crystal and XTAL_OUT provides the feedback to that external crystal. If a reference clock is used instead, it is provided through the 2700G Multimedia Accelerator's CLKIN pin.

If an external reference clock is used, that clock must be running whenever the 2700G Multimedia Accelerator is powered up. Using an external clock source may impact other components abilities to reduce their power consumption during certain system states (for example, display refresh only).

5.5.1.1 Crystal Reference Guidelines

The following guidelines should be followed when using an external crystal as the 2700G Multimedia Accelerator's reference source:

- XTAL_IN and XTAL_OUT should be kept as short and clean as possible. Trace lengths from the crystal's terminals to the XTAL_IN and XTAL_OUT balls should be less than 1 inch. Maximize spacing to all other signals as much as possible.
- XTAL_IN and XTAL_OUT should not be routed near high speed signals.
- Capacitors are required on both the XTAL_IN and XTAL_OUT connections. The equation for calculating the capacitance is:

  Equation 1: Capacitance = 2*C_L – 4 pF

  Where: C_L is the capacitive loading of the crystal that is used.

  For example, a crystal with 11 pF capacitance will require 18 pF capacitors on both XTAL_IN and XTAL_OUT.

Figure 5-14. Reference Crystal Topology

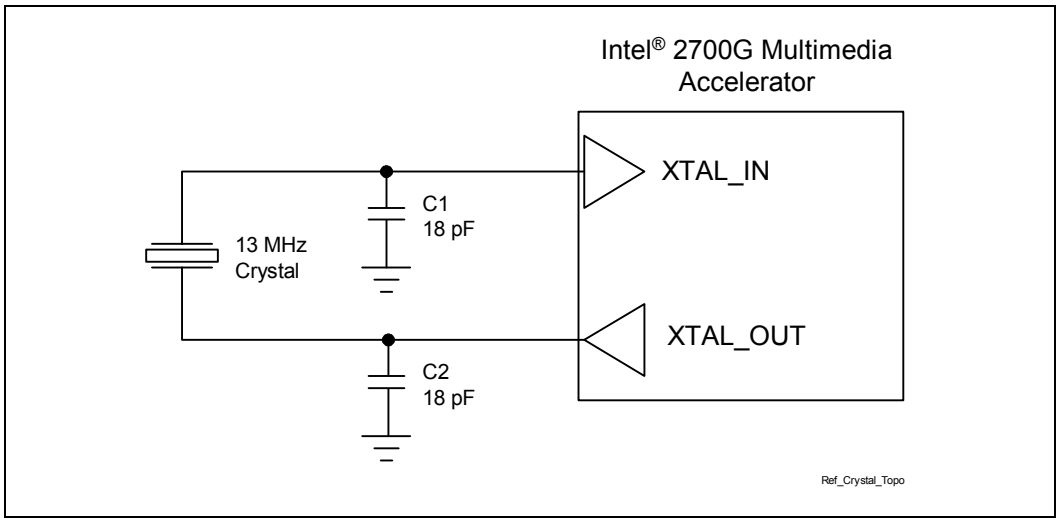


Table 5-16. Reference Crystal Component Recommendations

Component	Value	Package Type
C1, C2	Refer to Equation 1	402 or 603

5.5.1.1.1 Leaving the Crystal Unconnected

Since the 2700G Multimedia Accelerator's clock source may be derived from an external reference clock instead of a crystal, the following guidelines should be followed in that scenario:

- XTAL_IN must have a 100 kΩ pull-down resistor to ground.
- XTAL_OUT may be left as a NC (no connect).

5.5.1.2 Clock Reference Guidelines

The following guidelines should be followed when using an external clock as the 2700G Multimedia Accelerator's reference source:

- CLKIN should be kept as short and clean as possible. Trace lengths from the 2700G Multimedia Accelerator's CLKIN to the clock source should be less than 4 inches. Maximize spacing to all other signals as much as possible; spacing of 10 mils to neighboring traces is recommended.
- Series termination may be required if using CLKIN.

5.5.1.2.1 Leaving CLKIN Unconnected

Since the 2700G Multimedia Accelerator's clock source may be derived from an external crystal instead of through the CLKIN pin, the following guidelines should be followed in that scenario:

- CLKIN should have a 100 kΩ pull-down resistor to ground.

5.5.2 Straps

The 2700G Multimedia Accelerator implements 3 strapping options on the LCD1_DD[2:0] signals. Recommended pull-up/pull-down resistor value is 100 kΩ.

- LCD_DD0 identifies whether the 2700G Multimedia Accelerator's clock is being provided via a crystal (strapped high) or an external reference clock (strapped low).
- LCD_DD1 identifies the drive strength for the SYS_RDY signal on the 2700G Multimedia Accelerator's system bus interface. All other buffer drive strengths may be set via register writes once the 2700G Multimedia Accelerator is up and running (refer to the *Intel® 2700G Multimedia Accelerator Datasheet*). The system bus topology and loading determine the ideal drive strength for SYS_RDY (and all system bus buffers). Default recommendation for this strap is high. However, if a design has a lightly loaded system bus, a low buffer strength may be more optimal.
- LCD_DD2 identifies whether the 2700G Multimedia Accelerator's local memory read clock is being provided via an internal mechanism (strapped high) or through an external loopback via the LM_RCLK pin (strapped low). The external LM_RCLK option is not intended for production designs, so this strap should be pulled high.

Table 5-17. Straps

Signal	Strap Function	Strap High Option	Strap Low Option	Recommendation
LCD1_DD0	Clock Source	XTAL	CLKIN	• If using crystal: 100 kΩ pull-up to VCC_LCD1 • If using external reference clock: 100 kΩ pull-down to ground
LCD1_DD1	SYS_RDY Drive Strength	High buffer strength	Low buffer strength	• 100 kΩ pull-up to VCC_LCD1. Dependent on system bus loading.
LCD1_DD2	LM Return Clock Path	Internal	External loop to LMRCLK	• 100 kΩ pull-up to VCC_LCD1

5.5.3 Reset

The 2700G Multimedia Accelerator resets its internal logic when nRESET_IN is low. This pin should be connected to the nRESET_OUT pin of the applications processor.

The following guidelines should be followed when routing the 2700G Multimedia Accelerator's reset signal:

- nRESET_IN should be routed using 60 Ω traces and connect from the nRESET_OUT pin of the applications processor.

5.5.4 JTAG

The 2700G Multimedia Accelerator includes a JTAG port. However, this controller is used for boundary scan purposes and is not recommended for use in a production system. The 2700G Multimedia Accelerator has integrated internal pull-up resistors on the JTAG_nTRST, JTAG_TDI, and JTAG_TMS signals, per the IEEE 1149.1 standard. JTAG_TCK requires an external 10 kΩ pull-down resistor, whether the 2700G Multimedia Accelerator JTAG interface is being used or not.

If the JTAG port is being used, JTAG_nTRST must be driven from low-to-high either before or at the same time as nRESET_IN. If the JTAG port is not being used, JTAG_nTRST should be connected to nRESET_IN to cause a reset on JTAG_nTRST at power-up.

5.5.4.1 Leaving JTAG Unconnected

If the 2700G Multimedia Accelerator's JTAG interface is not used, the following guidelines should be followed:

- JTAG_TCK must have a 10 kΩ pull-down to ground.
- JTAG_nTRST must be connected to nRESET_IN.
- JTAG_TDO requires a 100 kΩ pull-down resistor to ground.

5.5.5 GPIOs

The 2700G Multimedia Accelerator has two software controllable GPIOs. Using a system register, these pins are programmable as either input-only (GPIs) or input/output (GPIOs). In GPIO mode, these signals can be programmed to drive high, drive low, or tri-state via a system register. In both GPI and GPIO modes, the state of the GPIO signals will be reflected in a 2700G Multimedia Accelerator register. The specific registers used to program the I/O mode, as well as drive the enabled outputs, are described in the *Intel® 2700G Multimedia Accelerator Datasheet.*

These pins require a pull-up or pull-down resistor, whether or not they are being used. Default recommendation is for a 100 kΩ pull-down resistor to ground. However, if the GPIOs are being used for a default high purpose (for example, DDC/I2C protocol requires external pull-up resistors), pull-up resistors to VCC_IO may be used instead.

5.5.5.1 Leaving GPIOs Unconnected

If one or both of the 2700G Multimedia Accelerator's GPIO pins is not used, the following guidelines should be followed:

- GPIOx should have a 100 kΩ pull-down resistor to ground.

5.5.6 Reserved Signal

The 2700G Multimedia Accelerator has a single Reserved signal labeled RSVD. This signal requires a 100 kΩ pull-down resistor to ground.

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6 Schematic Checklist

This checklist highlights schematics considerations that should be reviewed prior to manufacturing a motherboard that implements the Intel PXA270 processor and 2700G Multimedia Accelerator. The items contained in this checklist attempt to address important connections to these devices and any critical supporting circuitry. **This is not a complete list and does not guarantee that a design will function properly.**

6.1 General System Bus

Table 6-1 is a checklist of schematic recommendations for the General System Bus connection between the 2700G Multimedia Accelerator and the application processor.

Table 6-1. General System Bus Interface

Checklist Item	Recommendation	✓
SYS_nCAS	• Connect to system bus signal nSDCAS.	
SYS_MA[25:2]	• Connect to system bus address signals MA[25:2] pins. [1] • Ensure these are connected to proper system bus address pins 25:2 and NOT 23:0.	
SYS_MD[31:0]	• Connect to system bus data signals MD[31:0]. [1]	
SYS_nOE	• Connect to system bus signals nOE.[1]	
SYS_RDY	• Connect to system bus signal RDY (GPIO18) pin.	
SYS_nCS[0]	• Connect to one of the CS pins on the application processor. • Ensure that software comprehends which CS is chosen for 2700G Multimedia Accelerator VLIO.	
SYS_nCS1	• Connect to one of the CS pins on the application processor. • Ensure that software comprehends which CS is chosen for 2700G Multimedia Accelerator SRAM.	
SYS_nPWE	• Connect to system bus address signals nPWE (GPIO49). [1]	
SYS_RDnWR	• Connect to system bus address signals RDnWR. [1]	
SYS_DQM[3:0]	• Connect to system bus address signals DQM[3:0] pin. [1]	
SYS_nWE	• Connect to system bus address signals nWE. [1]	

NOTES:
1. These signals are connected to several system bus devices.

6.2 Local Memory Interface

The local memory interface for the 2700G Multimedia Accelerator can be a single x32 memory device or two x16 memory devices. Table 6-2 is a checklist of schematic recommendations to connect the 2700G Multimedia Accelerator to a single x32 memory device. Table 6-3 is a checklist of schematic recommendations to connect the 2700G Multimedia Accelerator to two x16 memory devices.

Table 6-2. Local Memory Interface (for a single x32 memory device)

Checklist Item	Recommendation	✓
LM_A[12:0]	• Connect to 2700G Multimedia Accelerator's local memory device's address pins.	
LM_D[31:0]	• Connect to 2700G Multimedia Accelerator's local memory device's data pins. The connections between the two devices are point-to-point.	
LM_DQM[3:0]	• Connect to 2700G Multimedia Accelerator's local memory device's DQM pins. The connections between the two devices are point-to-point.	
LM_BA[1:0]	• Connect to 2700G Multimedia Accelerator's local memory device's BA[1:0] pins.	
LM_RCLK	• This signal should have a 100 KΩ pull down.	
LM_nRAS	• Connect to 2700G Multimedia Accelerator's local memory device's nRAS pin.	
LM_nCAS	• Connect to 2700G Multimedia Accelerator's local memory device's nCAS pin.	
LM_nCS	• Connect to 2700G Multimedia Accelerator's local memory device's nCS0 pin.	
LM_CKE	• Connect to 2700G Multimedia Accelerator's local memory device's CKE pin. Requires a 100 kΩ pull down resistor to ground.	
LM_CLK	• Connect to the 2700G Multimedia Accelerator's local memory device's CLK pin. • To decrease overshoot and ringback, a 22 Ω series resistor needs to be added between the LM_CLK and the x32 memory device. Refer to Figure 5-5 for more details.	
LM_nWE	• Connect to the 2700G Multimedia Accelerator's local memory device's nWE pin.	

Table 6-3. Local Memory Interface (for two x16 memory device)

Checklist Item	Recommendation	✓
LM_A[12:0]	• Connect to 2700G Multimedia Accelerator's local memory device's address pins.	
LM_D[15:0]	• Connect to one of the x16 memory device's data pins.	
LM_D[31:16]	• Connect to the other x16 memory device's data pins.	
LM_DQM[3:0]	• Connect to 2700G Multimedia Accelerator's local memory device's DQM pins. • Make sure that DQM pins are aligned with the appropriate data lines. For example, the first 8 data lines can be assigned to the local memory device's first DQM pin and the next 8 data lines to the second DQM pin etc. as shown below: —LM_DQM0→LM_D[7:0] —LM_DQM1→LM_D[15:8] —LM_DQM2→LM_D[23:16] —LM_DQM3→LM_D[31:24]	
LM_BA[1:0]	• Connect to the 2700G Multimedia Accelerator's local memory device's BA[1:0] pins.	
LM_RCLK	• This signal should have a 100 KΩ pull-down.	
LM_nRAS	• Connect to 2700G Multimedia Accelerator's local memory device's nRAS pin.	
LM_nCAS	• Connect to 2700G Multimedia Accelerator's local memory device's nCAS pin.	
LM_nCS	• Connect to 2700G Multimedia Accelerator's local memory device's nCS0 pin.	
LM_CKE	• Connect to 2700G Multimedia Accelerator's local memory device's CKE pin. Requires a 100 kΩ pull down resistor to ground.	
LM_CLK	• Connect to the 2700G Multimedia Accelerator's local memory device's CLK pin. • To decrease overshoot and ringback, a series resistor needs to be added between the LM_CLK and the T-Section to the two x16 memory devices.	
LM_nWE	• Connect to the to 2700G Multimedia Accelerator's local memory device's nWE pin.	

6.3 Primary and Auxiliary LCD Output Interfaces

Table 6-4 is a checklist of schematic recommendations to connect the 2700G Multimedia Accelerator to the primary LCD output interface. Table 6-5 is a checklist of LCD strapping options for the primary LCD. Table 6-6 is a checklist of schematic recommendations to connect the 2700G Multimedia Accelerator to the auxiliary LCD output interface.

Table 6-4. Primary LCD Interface

Checklist Item	Recommendation	✓
LCD1_DD[23:0] For a 16-bit device	• The following recommendations are for a 16-bit display device: —Data pins LCD1_DD[2:0], LCD1_DD[9:8], LCD1_DD[18:16] are not connected. —Data pins LCD1_DD[7:3] are connected to LCD panel's pins B[4:0]. —Data pins LCD1_DD[15:10] are connected to LCD panel's pins G[5:0]. —Data pins LCD1_DD[23:19] are connected to LCD panel's pins R[4:0]. • LCD1_DD[2:0] have strapping options that must be implemented. Refer to Table 6-5 for more information.	
LCD1_DD[23:0] For a 18-bit device	• The following recommendations are for a 18-bit display device: —Data pins LCD1_DD[1:0], LCD1_DD[9:8], LCD1_DD[17:16] are not connected. —Data pins LCD1_DD[7:2] are connected to LCD panel's pins B[5:0]. —Data pins LCD1_DD[15:10] are connected to LCD panel's pins G[5:0]. —Data pins LCD1_DD[23:18] are connected to LCD panel's pins R[5:0]. • LCD1_DD[2:0] have strapping options that must be implemented. Refer to Table 6-5 for more information.	
LCD1_DD[23:0] For a 24-bit device	• The following recommendations are for a 24-bit display device: —Data pins LCD1_DD[7:0] are connected to LCD panel's pins B[7:0]. —Data pins LCD1_DD[15:8] are connected to LCD panel's pins G[7:0]. —Data pins LCD1_DD[23:16] are connected to LCD panel's pins R[7:0]. • LCD1_DD[2:0] have strapping options that must be implemented. Refer to Table 6-5 for more information.	
LCD1_PCLK	• Connect to the primary LCD display's pixel clock pin.	
LCD1_LCLK	• Connect to the primary LCD display's line clock pin.	
LCD1_FCLK	• Connect to the primary LCD display's frame clock pin.	
LCD1_DEN	• Connect to the primary LCD display's data valid pin.	
LCD1_PWM	• Used to control primary LCDs backlight.	

Note: If the system does not make use of the 2700G Multimedia Accelerator's LCD1 output interface, the following guidelines should be followed:

- LCD1 signals may be left as NCs (no-connects).
- The VCC_LCD1 shall still be applied at 1.8 V, 2.5 V, or 3.3 V.

Primary LCD Strapping Option

The 2700G Multimedia Accelerator implements 3 strapping options on the LCD1_DD[2:0] signals. Recommended pull-up/pull-down resistor value is 100 kΩ. All strapping options are to VCC_LCD1.

Table 6-5. Primary LCD Strapping Options

Signal	Strap Function	Strap High Option	Strap Low Option	Recommendation	✓
LCD1_DD0	Clock Source	XTAL	CLKIN	• If using crystal: 100 kΩ pull-up to VCC_LCD1 • If using external reference clock: 100 kΩ pull-down to ground	
LCD1_DD1	SYS_RDY Drive Strength	High buffer strength	Low buffer strength	• 100 kΩ pull-up to VCC_LCD1. Dependent on system bus loading.	
LCD1_DD2	LM Return Clock Path	Internal	External loop to LMRCLK	• 100 kΩ pull-up to VCC_LCD1	

Table 6-6. Auxiliary LCD Interface

Checklist Item	Recommendation	✓
LCD2_DD[23:0] For a 16-bit display	• The following recommendations are for a 16-bit display device: —Data pins LCD2_DD[2:0], LCD2_DD[9:8], LCD2_DD[18:16] are not connected. —Data pins LCD2_DD[7:3] are connected to LCD panel's pins B[4:0]. —Data pins LCD2_DD[15:10] are connected to LCD panel's pins G[5:0]. —Data pins LCD2_DD[23:19] are connected to LCD panel's pins R[4:0].	
LCD2_DD[23:0] For a 18-bit device	• The following recommendations are for a 18-bit display device: —Data pins LCD2_DD[1:0], LCD2_DD[9:8], LCD2_DD[17:16] are not connected. —Data pins LCD2_DD[7:2] are connected to LCD panel's pins B[5:0]. —Data pins LCD2_DD[15:10] are connected to LCD panel's pins G[5:0]. —Data pins LCD2_DD[23:18] are connected to LCD panel's pins R[5:0].	
LCD2_DD[23:0] For a 24-bit device	• The following recommendations are for a 18-bit display device: —Data pins LCD2_DD[7:0] are connected to LCD panel's pins B[7:0]. —Data pins LCD2_DD[15:8] are connected to LCD panel's pins G[7:0]. —Data pins LCD2_DD[23:16] are connected to LCD panel's pins R[7:0].	
LCD2_PCLK	• Connect to the auxiliary LCD display's pixel clock pin.	
LCD2_LCLK	• Connect to the auxiliary LCD display's line clock pin.	
LCD2_FCLK	• Connect to the auxiliary LCD display's frame clock pin.	
LCD2_DEN	• Connect to the auxiliary LCD display's data valid pin.	
LCD2_PWM	• Users to control auxiliary LCDs backlight.	

Note: If the system does not make use of the 2700G Multimedia Accelerator's LCD2 output interface, the following guidelines should be followed:

- LCD2 signals may be left as NCs (no-connects).
- The VCC_LCD2 shall still be applied at 1.8 V, 2.5 V, or 3.3 V.

6.4 LCD Input Interface

Table 6-7 is a checklist of schematic recommendations to connect the LCD input interface of the 2700G Multimedia Accelerator to the LCD output interface of the application processor.

This interface allows a display stream driven by the applications processor to be redirected out one of the 2700G Multimedia Accelerator's output LCD interfaces.

Table 6-7. LCD Input Interface (for Dual Display mode)

Checklist Item	Recommendation	✓
LCD_IN_DD[15:0]	• Connect to application processor's L_DD[15:0] (GPIO58 to GPIO73) pins.	
LCD_IN_DD[17:16]	• Connect to application processor's L_DD[17:16] (GPIO86 and GPIO87) pins.	
LCD_IN_PCLK	• Connect to application processor's L_PCLK_WR (GPIO76) pin.	
LCD_IN_LCLK	• Connect to application processor's L_LCLK_A0 (GPIO75) pin.	
LCD_IN_FCLK	• Connect to application processor's L_FCLK_RD (GPIO74) pin.	
LCD_IN_DEN	• Connect to application processor's L_BIAS (GPIO77) pin.	

Note: If the system does not make use of the 2700G Multimedia Accelerator's LCD input interface, the following guidelines should be followed:

- If left unconnected, the 2700G Multimedia Accelerator's LCD input signals must be individually pulled down to ground via 100 kΩ resistors (RPacks are acceptable).
- To avoid the use of additional termination components, it is possible to use the applications processor's LCD output as "termination". Instead of using pull-down resistors, the 2700G Multimedia Accelerator's unused LCD input may be connected to the applications processor's LCD output. This scenario is only applicable if the application processors' LCD pins are not re-used as GPIOs.
- VCC_LCD_IN should still be applied at 1.8 V or 2.5 V.

6.5 Clocks

The 2700G Multimedia Accelerator's internal clock can be derived from either an external crystal or a reference clock. Table 6-8 is a checklist of schematic recommendations for using a crystal (XTAL) or an external clock (CLKIN).

Table 6-8. Clocks

Checklist Item	Recommendation	✓
XTAL_IN	• If a crystal is, connect to a 13 MHz crystal and an 18 pF capacitor. • If a discreet crystal is NOT used to generate the 2700G Multimedia Accelerator's reference source, XTAL_IN should have a 100 kΩ pull-down resistor to ground.	
XTAL_OUT	• If a crystal is used, connect to a 13 MHz crystal and an 18 pF capacitor. • If a discreet crystal is NOT used to generate 2700G Multimedia Accelerator's reference source, XTAL_OUT should be a No-Connect.	
CLKIN	• CLKIN may be used as an alternate 13 MHz source for the 2700G Multimedia Accelerator's PLL reference clock. • If CLKIN is NOT used to generate 2700G Multimedia Accelerator's reference source, CLKIN should have a 100 kΩ pull down resistor to ground.	

6.6 JTAG and Reset

The 2700G Multimedia Accelerator includes a JTAG port and controller for boundary scan purposes. Table 6-9 is a checklist of schematic recommendations for leaving the JTAG port unused.

Table 6-9. JTAG and Reset

Checklist Item	Recommendation	✓
JTAG_TDI	• If not used, this signal must be pulled high with a 100 kΩ resistor to VCC_IO.	
JTAG_TDO	• If not used, this signal requires a 100 kΩ pull-down resistor to ground.	
JTAG_TMS	• If not used, this signal must be pulled high with a 100 kΩ resistor to VCC_IO.	
JTAG_TCK	• JTAG_TCK requires an external 10 kΩ pull-down resistor, whether the 2700G Multimedia Accelerator's JTAG interface is being used or not.	
JTAG_nTRST	• If not used, this signal should be connected to nRESET_IN.	
nRESET_IN	• Connect to application processor's nRESET_OUT pin.	

6.7 Miscellaneous

Table 6-10. Miscellaneous

Checklist Item	Recommendation	✓
RSVD	• This signal requires a 100 kΩ pull-down resistor to ground.	
POLL_FLAG	• Connect to application processor's polling flag (or a GPIO used as polling flag) pin.	
nINT	• This signal is an interrupt output used to interrupt the application processor. • Connect to one of the GPIO pins on the application processor. • Software needs to be aware of this interrupt signal to handle the interrupts from the 2700G Multimedia Accelerator properly.	
GPIO[1:0]	• The GPIO pins require a pull-up or pull-down resistor, whether or not they are being used. Default recommendation is for a 100 kΩ pull-down resistor to ground.	

6.8 Intel® 2700G Multimedia Accelerator Power Delivery

The 2700G Multimedia Accelerator offers power management through component selection, programmable power savings, and internal power management.

- **Core Voltage (VCC_CORE):** The 2700G Multimedia Accelerator's VCC_CORE is 1.2 V.
- **General System Bus (VCC_SYS):** The GSB operates at either 1.8 V or 2.5 V, which must be the same as the system memory (VCC_MEM) voltage of the application processor.
- **Local Memory (VCC_LM):** The local memory interface can support 1.8 V or 2.5 V signaling voltages. If operating at 1.8 V, the interface can run up to 100 MHz. If operating at 2.5 V, the interface can run up to 133 MHz.
- **Primary and Auxiliary LCD Output (VCC_LCDx):** Each LCD output can run at 1.8 V, 2.5 V, or 3.3 V. The voltage is dependent on the signaling requirements of the LCD or the display device that is used.
- **LCD Input (VCC_LCD_IN):** The LCD input interface can run at 1.8 V or 2.5 V. This voltage is the same as that of the application processor's VCC_LCD voltage. For example, if the VCC_LCD voltage of the PXA27x processor is 1.8 V, the 2700G Multimedia Accelerator's VCC_LCD_IN voltage must be 1.8 V.
- **Analog Power (VCCA_CORE_PLL, VCCA_DISP_PLL):** The two analog circuits operate at 2.5 V. The analog circuits require filtered supplies on the 2700G Multimedia Accelerator.

7 Layout Checklist

This checklist highlights design considerations that should be reviewed prior to manufacturing a motherboard that implements the Intel XScale® technology processor and the 2700G Multimedia Accelerator. The items contained within this checklist attempt to address important design considerations to these devices and any critical supporting circuitry. **This is not a complete list and does not guarantee that a design will function properly.**

7.1 General System Bus

Table 7-1 is a checklist of design recommendations for the General System Bus connection between the 2700G Multimedia Accelerator and the PXA270 application processor.

Table 7-1. General System Bus Design Checklist

Width/Spacing Recommendations	✓
General system bus signals should be routed using 60 Ω trace widths, with 10 mil (0.254 mm) spacing to neighboring signals.	
Trace widths and spacing can be less than 10 mils in the component (both 2700G Multimedia Accelerator and the applications processor) breakout regions, but should be spaced at 10 mils as much as possible.	
Within the breakout region, 3 mil (0.0762 mm) trace widths and 3 mils (0.0762 mm) spacing is permissible. The breakout region for each component should be less than 625 mils (15.75 mm).	
General Recommendations	✓
Where possible, try to keep data lines and their respective data mask signals routed on the same layer.	
Avoid routing over reference plane splits and voids.	

7.2 Local Memory

The local memory interface for the 2700G Multimedia Accelerator can be a single x32 memory device or two x16 memory devices. Refer to Section 5.2 for a detailed discussion of these topologies.

Table 7-2 is a checklist of design recommendations to connect the 2700G Multimedia Accelerator to a single x32 memory device. Table 7-3 is a checklist of design recommendations to connect the 2700G Multimedia Accelerator to two x16 memory devices.

Table 7-2. Local Memory Design Recommendations (Single x32 device)

Width/Spacing Recommendations	✓
When a x32 memory device is used, data connections (i.e., LM_D[31:0]) between 2700G Multimedia Accelerator and the memory device are point-to-point.	
Local memory data, address, control and the local memory clock should be routed using 60 Ω trace widths, with 7 mils (0.178 mm) spacing to neighboring signals.	
Spacing can be less than 7 mils in the component (both 2700G Multimedia Accelerator and the memory device) breakout regions, but should be spaced at 7 mils as much as possible.	
Within the breakout region, 3 mil (0.0762 mm) trace widths and 3 mils (0.0762 mm) spacing is permissible. The breakout region for each component should be less than 625 mils (15.75 mm).	
To decrease overshoot and ringback, a series resistor needs to be added between the LM_CLK and the x32 memory device. A 22 Ω resistor is recommended to be placed within one inch from the 2700G Multimedia Accelerator.	
For maximum timing margins, the total LM_CLK length (the total length between the 2700G Multimedia Accelerator and the memory device) should be tuned to slightly less than the midpoint of data, address, and control lengths. For example, if data, address, and control signals are between 2 inches and 3 inches in total length, LM_CLK should be tuned to approximately 2.4 inches.	
Matching Recommendations	✓
Care should be taken to match SDRAM interface signal lengths as closely as possible.	
Total lengths for data signals should be kept as similar as is reasonably possible. The tighter the range between minimum and maximum lengths, the greater the timing margin available on the interface.	
General Recommendations	✓
Avoid routing over reference plane splits and voids.	

Table 7-3. Local Memory Design Recommendations (two x16 devices)

Width/Spacing Recommendations	✓
When two x16 memory devices are used, connect LM_D[15:0] to one SDRAM device and LM_D[31:16] to the other SDRAM device.	
Local memory data, address, control signals and the local memory clock should be routed using 60 Ω trace widths, with 7 mil (0.178 mm) spacing to neighboring signals.	
Spacing can be less than 7 mils in the component (both 2700G Multimedia Accelerator and the memory device) breakout regions, but should be spaced at 7 mils as much as possible.	
Within the breakout region, 3 mil (0.0762 mm) trace widths and 3 mils (0.0762 mm) spacing is permissible. The breakout region for each component should be less than 625 mils (15.75 mm).	
For maximum timing margins, the total LM_CLK length (the total length between the 2700G Multimedia Accelerator and the memory device) should be tuned to slightly less than the midpoint of data, address and control lengths. For example, if data, address, and control signals are between 2 inches and 3 inches in total length, LM_CLK should be tuned to approximately 2.4 inches.	
To decrease overshoot and ringback, a series resistor needs to be added between the LM_CLK and the T-Section to the two x16 memory devices. A 22 Ω resistor is recommended to be placed 500 mils from the 2700G Multimedia Accelerator.	
It is critical to ensure that the stub lengths from the LM_CLK to the two x16 SDRAM devices are equal.	
Matching Recommendations	✓
Care should be taken to match SDRAM interface signal lengths as closely as possible.	
Total lengths for data, address, and control signals should be kept as similar as is reasonably possible. The tighter the range between minimum and maximum lengths, the greater the timing margin available on the interface.	
General Recommendations	✓
Avoid routing over reference plane splits and voids.	

7.3 Primary and Auxiliary LCD Output

Table 7-4 is a checklist of design recommendations to connect the 2700G Multimedia Accelerator to the primary or the auxiliary LCD devices.

Table 7-4. Primary and Auxiliary LCD Output Design Recommendations

Width/Spacing Recommendations	✓
LCD output pixel clocks (LCDx_PCLK) , along with the LCD output data signals (LCDx_DD[23:0]), and the control signals LCDx_LCLK, LCDx_FCLK, LCDx_DEN should be routed using 60 Ω trace widths, with 7 mil (0.178 mm) spacing to neighboring signals.	
Spacing can be less than 7 mils in the component (both 2700G Multimedia Accelerator and the LCD connector or intermediate device) breakout regions, but should be spaced at 7 mils as much as reasonably possible.	
Within the breakout region, 3 mil (0.0762 mm) trace widths and 3 mil (0.0762 mm) spacing is permissible. The breakout region should be less than 625 mils (15.75 mm).	
The maximum trace length for the LCD data and control signals is 7.5 inches. These signals should be matched to the associated LCDx_PCLK as close as reasonably possible. Length matching within ±500 mils (12.7 mm) of the associated LCDx_PCLK signal is recommended.	
General Recommendations	✓
Avoid routing over reference plane splits and voids.	

7.4 LCD Input Interface

Table 7-5 is a checklist of design recommendations to connect the 2700G Multimedia Accelerator's LCD input interface to the application processor's LCD output interface.

Table 7-5. LCD Input Interface Design Recommendations

Width/Spacing Recommendations	✓
LCD input pixel clock (LCD_IN_PCLK) should be routed using 60 Ω trace widths, with 7 mil (0.178 mm) spacing to neighboring signals.	
Spacing can be less than 7 mils in the component (both 2700G Multimedia Accelerator and the applications processor) breakout regions, but should be spaced at 7 mils as much as reasonably possible.	
Within the breakout region, 3 mil (0.0762 mm) trace widths and 3 mils (0.0762 mm) spacing is permissible. The breakout region for each component should be less than 625 mils (15.75 mm).	
LCD input data signals (LCD_IN_DD[17:0]), along with the control signals LCD_IN_LCLK, LCD_IN_FCLK, and LCD_IN_DEN should be routed 5 mils (0.127 mm) wide, with 7 mil (0.178 mm) spacing to neighboring signals.	
The maximum trace length for the LCD data and control signals is 7.5 inches. These signals should each be matched within ±500 mils (12.7 mm) of the LCD_IN_PCLK signal.	
General Recommendations	✓
Avoid routing over reference plane splits and voids.	

7.5 Clocks

The 2700G Multimedia Accelerator's internal clock can be derived from either an external crystal or a reference clock. Table 7-6 is a checklist of design recommendations for using a crystal (XTAL) or an external clock (CLKIN).

Table 7-6. Clocks

Crystal Reference Routing Guidelines	✓
XTAL_IN and XTAL_OUT should be kept as short and clean as possible. Trace lengths from the crystal's terminals to the XTAL_IN and XTAL_OUT balls should be less than 1 inch. Maximize spacing to all other signals as much as possible.	
Reference Clock Routing Guidelines	✓
CLKIN should be kept as short and clean as possible. Trace lengths from the 2700G Multimedia Accelerator's CLKIN to the clock source should be less than 4 inches. Maximize spacing to all other signals as much as possible; spacing of 10 mils to neighboring traces is recommended.	

7.6 Miscellaneous

Table 7-7. Miscellaneous

Reset Routing Guidelines	✓
nRESET_IN should be routed using 60 Ω trace widths and connect from the nRESET_OUT pin of the applications processor. This signal may be T'd to other devices that make use of this signal; however, no stubs are to be used on this net.	
GPIOs and RSVD	✓
The 2700G Multimedia Accelerator has one RSVD signal. This signal requires a 100 kΩ pull-down resistor to ground.	
The GPIO pins require a pull-up or pull-down resistor, whether or not they are being used. Default recommendation is for a 100 kΩ pull-down resistor to ground. However, if the GPIOs are being used for a default high purpose (for example, DDC/I2C protocol requires external pull-up resistors), pull-up resistors to VCC_IO may be used instead.	