Consider a 4 stage pipeline that consists of IF, ID, EX and WB stages. The time taken by these stages are 50 ns, (ons, 110 ns and 80 ns respectively. The pipeline registers are required! often every pipeline stage and each of these pipline registers consumes 10ns delay. What is the speedup of the pipeline under ideal conditions compare to the connesponding non-pipelined

implementation?

$$\frac{2\pi pipeline}{2\pi pipeline}$$

$$\frac{2\pi$$

or,
$$tp = max^{m}(5.0)(0), 110, 80) + 10$$

$$= 110 + 10 = 120 \text{ ns}$$

What is the difference between multiple processor, multi computer and multi cone sy stem? Hultiprocessor de la la mattionipation

- 1 A system with two or more CPUs that allows simultaneous proce-O Easier to process

an.

- 3) More difficult and costly to
- @ supprots parallel computing

- 1 A set of processors connected by the communication network that works jointly to solve a computation problem.
- @ Len easy to program
- @ Easion and cost effective to build.
- @ Supprorts distributed computing.

- () A single CPU or processor with two or more independent processing units called constant comes that one capable of reading and executing program instructions.
- @ Executes a single program faster.
- 3 Not as reliable as a multiprocessor
- 1) Have less troffic

- Multiprocess or
- 1) A system with two for more CPUs that allows simultaneous processing of programs.
- @ Executes multiple programs faster.
- 6) More reliable since failure in once CPU will not affect the other.
- 4 Have more traffic.

A 30% enhancement in speedup for a component of the processor has been proposed for a new anchitecture. If the enhancement is usable only for 50% of the time, what is fraction of the time must enhancement be used to achieve an overall speedup of

10 7

Say, the fraction of the time must entry enhancement is used to achieve an overall speedup = X

So,
$$\left(\frac{36}{56}\right) = 10$$

$$\alpha_{r}, \quad \chi = \frac{10 \times 5}{3}$$

$$\alpha_{r}, \quad \chi = \frac{50}{3}$$