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**NETAJI SUBHAS ENGINEERING COLLEGE**

**DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING**

**ANALOG & DIGITAL ELECTRONICS LABORATORY ECS- 391**

**EXPERIMENT NO- 01**

**TITLE: Realization of different logic gates using NAND Gate**

**OBJECT: Realization of truth table of different logic gates using NAND Gate.**

**EQUIPMENT & COMPONENT REQUIED**

**SL NO NAME SPECIFICATION**

**1. IC 7400 Quad 2 i/p NAND Gate**

**2. Bread Board -**

**3. Power Supply 5v/1A, DC Regulated, fixed**

**4. Connecting Wires Single strand wire**

**5.** quently performed in the design of digital systems are AND, OR, NOT, NAND, NOR, EX-OR, EX-NOR. The NAND & NOR are called universal gates as all the primary functions can be realized with them.

**NAND GATE: A NAND** gate has two or more inputs and only one output. The NAND operation is given Y**=A.B** and NAND operation is called “Universal Operation”

|  |  |  |
| --- | --- | --- |
| **I/P State** | **I/P State** | **O/P State** |
| **0** | **0** | **1** |
| **0** | **1** | **1** |
| **1** | **0** | **1** |
| **1** | **1** | **0** |

**SYMBOL:**

|  |  |  |
| --- | --- | --- |
| **I/P State** | **I/P State** | **O/P State** |
| **0** | **0** | **1** |
| **0** | **1** | **1** |
| **1** | **0** | **1** |
| **1** | **1** | **0** |

**SYMBOL:**

|  |  |  |
| --- | --- | --- |
| **I/P State** | **I/P State** | **O/P State** |
| **0** | **0** | **1** |
| **0** | **1** | **1** |
| **1** | **0** | **1** |
| **1** | **1** | **0** |

**SYMBOL:**

****

**Truth Table**

**Circuit Diagram:**

|  |  |  |
| --- | --- | --- |
| **I/P State (in V)** | **I/P State (in V)** | **O/P State (LED)** |
| **0** | **0** | **On** |
| **0** | **5** | **On** |
| **5** | **0** | **On** |
| **5** | **5** | **Off** |

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**Verification Table**