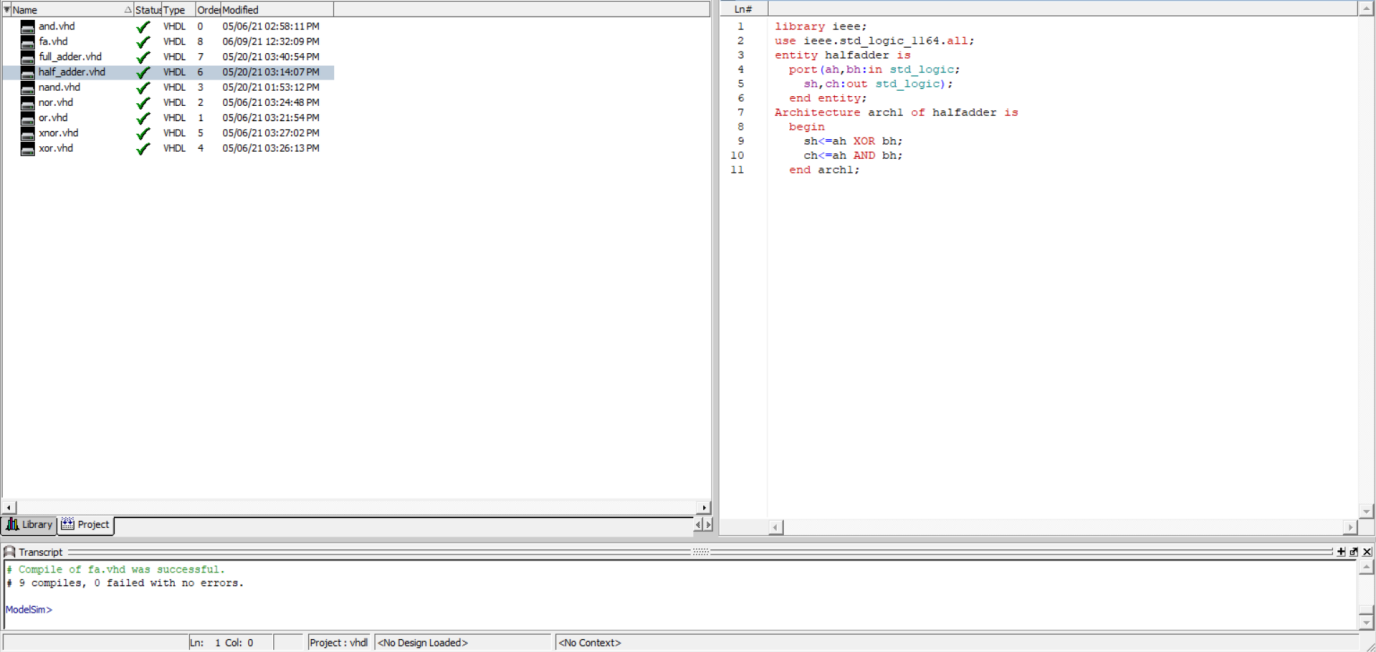
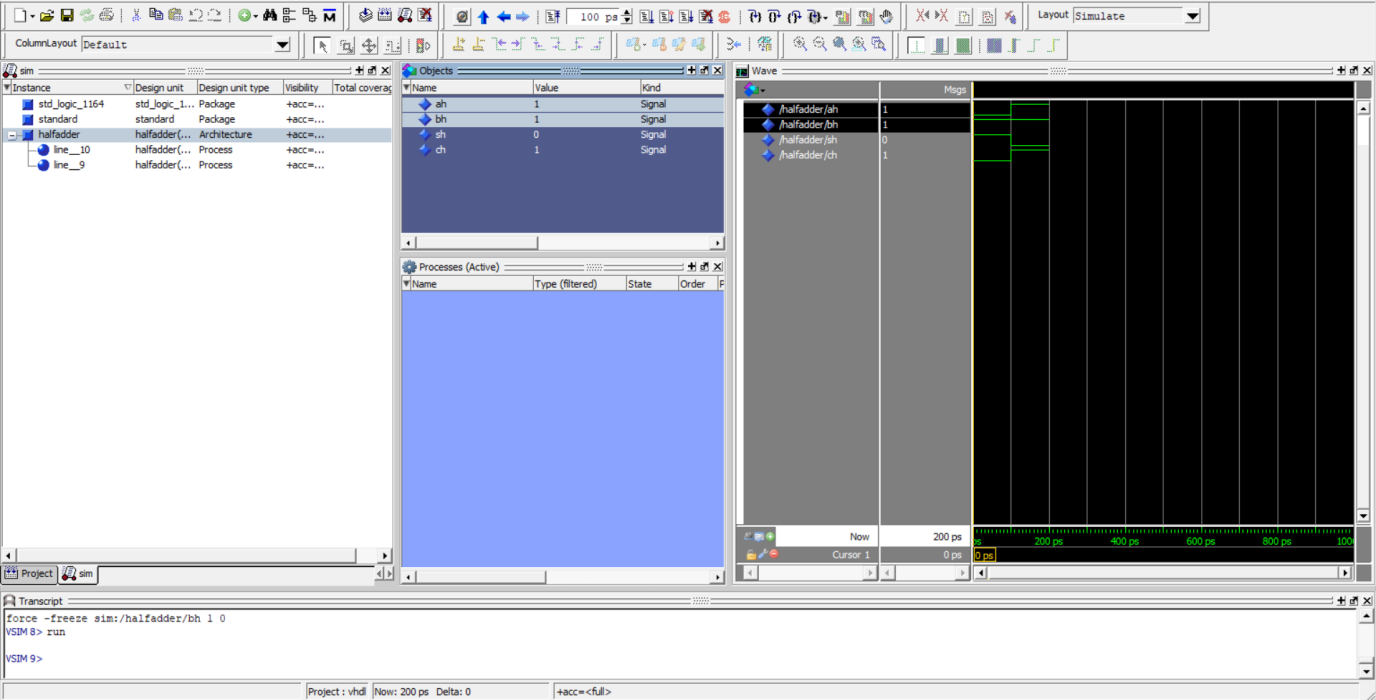
Q) Write a VHDL program to design the half adder and full adder using Dataflow design.

**HALF ADDER (DATAFLOW DESIGN)**





**FULL ADDER (DATAFLOW DESIGN)**

