Devrath Iyer

Email: deviyer@stanford.edu | 480-208-8616 | LinkedIn: devrathiyer | Github: devrathiyer

Education

Stanford University — Palo Alto, CA
Doctor of Philosophy, Electrical Engineering — *September 2024 - Present*

Stanford University — Palo Alto, CA
Master's of Science, Electrical Engineering (GPA: 3.93) — *June 2024*
Bachelor's of Science, Electrical Engineering and Computer Science (GPA: 3.91)

Relevant Coursework: VLSI Systems, Analog IC Design, Digital Design, Computer Architecture, MEMS Design, Circuits, PCB Design, Signal Processing, Operating Systems, Algorithms, Artificial Intelligence, SIMD Programming, Electromagnetics

Skills

- **Languages**: SystemVerilog/Verilog, C/C++, Python, Rust, Java, LaTeX, MIPS/ARM assembly, HTML/CSS/Javascript
- **Tools and Libraries**: Cadence JapserGold, Xilinx Vivado, Synopsys Verdi, Synopsys Protocompiler, Altium, EAGLE, Django, React, NodeJs, Numpy, TensorFlow, Autodesk Inventor/Fusion, Solidworks

Publications

- **Iyer, D.** & Achour, S. (2024). Efficient Optimization with Encoded Energy Functions. Manuscript submitted for publication.

Experience

Platform Engineering Group, Apple — Cupertino, CA
Silicon Prototyping Intern — *June 2023 - September 2023*

Automated configuration workflows for deploying media IPs (e.g. Neural Engine, ProRes) to an FPGA-based prototyping platform. Designed an architecture to store configuration data in FPGA memory, enabling SW to be fully coupled with RTL. Wrote scripts to both generate Verilog from configuration files and to read embedded data from running RTL.

ML Model Platform Team, Meta — Menlo Park, CA
Software Engineering Intern — *June 2022 - September 2022*

Designed and added features to ML infrastructure code related to model publishing workflows. Created utilities for researchers to run experiments on incrementally published models, including a tool to mix tensors from different training checkpoints and a tool to selectively update sparse tensors in an inference model.

Relevant Projects

Efficient Optimization with Encoded Energy Functions Research — April 2023 - Present
Research Intern, Novel Computing Systems Lab

Created compilation methods for probabilistic "p-bits". Used higher-order interactions to reduce the proportion of invalid state explored by p-bit systems. Created a programming language, made of types and gate operations, to express higher-order Ising models for NP-Complete combinatorial optimization problems. Demonstrated solution time and p-bit scaling superiority over conventional Ising models. Submitted paper to HPCA 2024.

Formal Verification of RISC-V Processor Core — January 2023 - June 2023
Course Grader, Electrical Engineering Department, Stanford University

Modified the open-source CVA6 RISC-V processor core to add formal verification through SymbioticEDA's RISC-V Formal specification. Used Cadence JasperGold to prove correctness of ALU, memory, and control flow instructions under an arbitrary pretrace of instructions. Packaged work into assignment for graduate computer architecture class at Stanford University.

3D NAND Flash Compute-in-Memory Research — March 2021 - June 2022
Research Intern, Brains in Silicon Lab

Created Python simulations for accuracy of analog matrix-vector multiplier using sub-threshold 3D NAND Flash strings. Designed temperature-robust analog-to-digital converter for quantizing results generated by Flash strings. Trained exponentially-quantized machine learning models to run on memory accelerator.

Additional Awards and Honors

Stanford Graduate Fellowship (2024): Full fellowship given to 100 doctoral students in science and engineering at Stanford
Apple Stanford EE Coterm Scholarship in Integrated Systems (2024): Awarded to 3 Coterminal Master's students in the EE department
National Merit Scholar (2020): Awarded to 7,600 students from an a group of 1.5 million by the National Merit Scholarship Corporation
Regeneron Science Talent Search Scholar (2020): Awarded to 300 students selected from almost 2,000 for original scientific research
Intel Andy Grove Scholar (2020): Competitive award for children of Intel employees pursuing higher education