## 參考文獻

- [1] Yu-Wei Lin, Hsuan-Yu Liu, and Chen-Yi Lee "A Dynamic Scaling FFT Processor for DVB-T Applications" IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 39, NO. 11, NOVEMBER 2004
- [2] Bevan M. Baas, *Student Member*, *IEEE* "A Low-Power, High-Performance, 1024-Point FFT Processor" IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 34, NO. 3, MARCH 1999
- [3] Sang-Chul Moon and In-Cheol Park "Area-Efficient Memory-Based Architecture for FFT Processing" Dept. of EECS, KAIST, Daejeon, Korea
- [4] Sang Yoon Park\*, Nam Ik Cho\*, Sang Uk Lee\*, Ki chul Ki m\*\*, Ji sung Oh\* "DESIGN OF 2W4WSK-POINT FFT PROCESSOR BASED ON CORDIC ALGORITHM IN OFDM RECEIVER" \*School of Electrical Engineering, Seoul National University, Seoul 15 1-742, Korea\*\*Dept. of Electrical Engineering, University of Seoul, Seoul 130-743, Korea\* \*DMS Lab, Samsung Electronics, Kyungkido, Korea
- [5] Shousheng He and Mats Torkelson Department of applied Electronics, Lund University" Designing Pipeline FFT Processor for OFDM (De)modulation" email:he@tde.1th.se;torkel@tde.1th.se
- [6] WLAN 64 ADSL 2x256 VDSL Zx256xZ",n=0:4 256x2",~0:3 DAB Jen-Chih Kuo, Ching-Hua Wen, and An-Yeu (Andy) Wu " IMPLEMENTATION OF A PROGRAMMABLE 64-2048-P01NT FFT/1FFT PROCESSORFOR OFDM-BASED COMMUNI CATION SYSTEMS" Graduate Institute of Electronics Engineering, and Department of Electrical Engineering, National Taiwan University, Taipei, 106, Taiwan, R.O.C.