

High-Speed FET-INPUT OPERATIONAL AMPLIFIERS

FEATURES

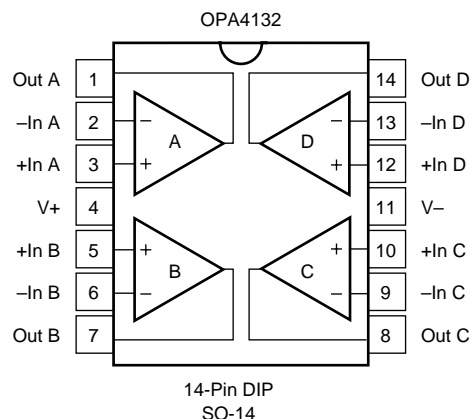
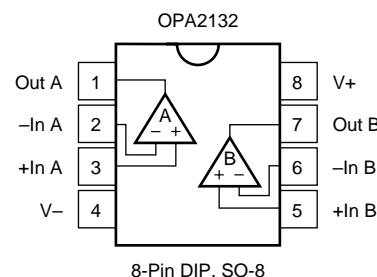
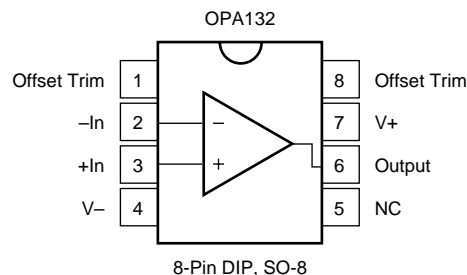
- **FET INPUT:** $I_B = 50\text{pA max}$
- **WIDE BANDWIDTH:** 8MHz
- **HIGH SLEW RATE:** $20\text{V}/\mu\text{s}$
- **LOW NOISE:** $8\text{nV}/\sqrt{\text{Hz}}$ (1kHz)
- **LOW DISTORTION:** 0.00008%
- **HIGH OPEN-LOOP GAIN:** 130dB (600Ω load)
- **WIDE SUPPLY RANGE:** ± 2.5 to $\pm 18\text{V}$
- **LOW OFFSET VOLTAGE:** $500\mu\text{V max}$
- **SINGLE, DUAL, AND QUAD VERSIONS**

DESCRIPTION

The OPA132 series of FET-input op amps provides high-speed and excellent dc performance. The combination of high slew rate and wide bandwidth provide fast settling time. Single, dual, and quad versions have identical specifications for maximum design flexibility. High performance grades are available in the single and dual versions. All are ideal for general-purpose, audio, data acquisition and communications applications, especially where high source impedance is encountered.

OPA132 op amps are easy to use and free from phase inversion and overload problems often found in common FET-input op amps. Input cascode circuitry provides excellent common-mode rejection and maintains low input bias current over its wide input voltage range. OPA132 series op amps are stable in unity gain and provide excellent dynamic behavior over a wide range of load conditions, including high load capacitance. Dual and quad versions feature completely independent circuitry for lowest crosstalk and freedom from interaction, even when overdriven or overloaded.

Single and dual versions are available in 8-pin DIP and SO-8 surface-mount packages. Quad is available in 14-pin DIP and SO-14 surface-mount packages. All are specified for -40°C to $+85^\circ\text{C}$ operation.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V+ to V-	36V
Input Voltage	(V-) -0.7V to (V+) +0.7V
Output Short-Circuit ⁽¹⁾	Continuous
Operating Temperature	-40°C to +125°C
Storage Temperature	-55°C to +125°C
Junction Temperature	150°C
Lead Temperature (soldering, 10s)	300°C

NOTE: (1) Short-circuit to ground, one amplifier per package.

PACKAGE/ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

SPECIFICATIONS

At $T_A = +25^{\circ}\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.

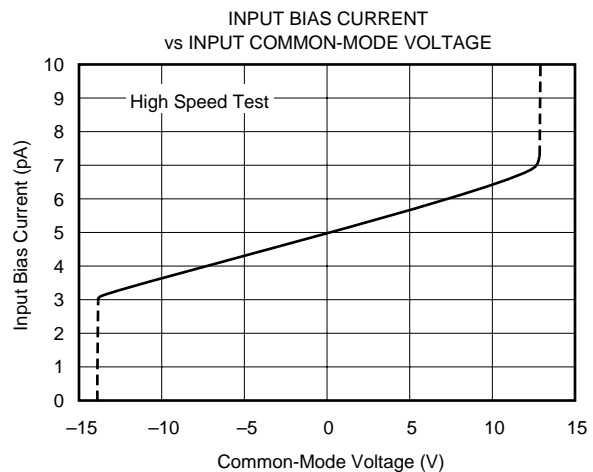
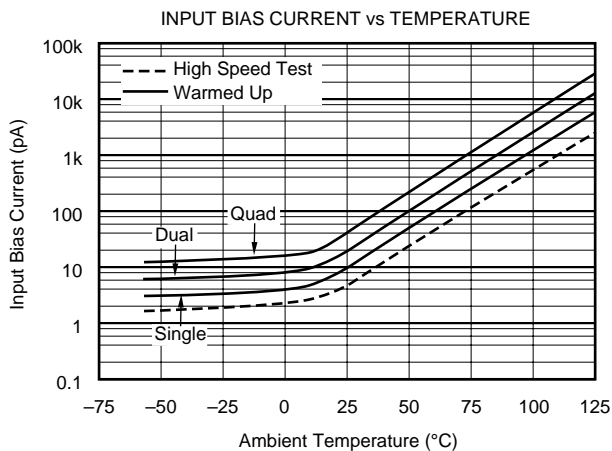
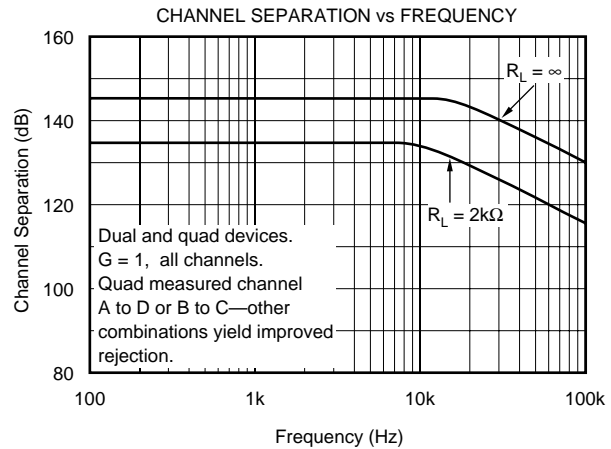
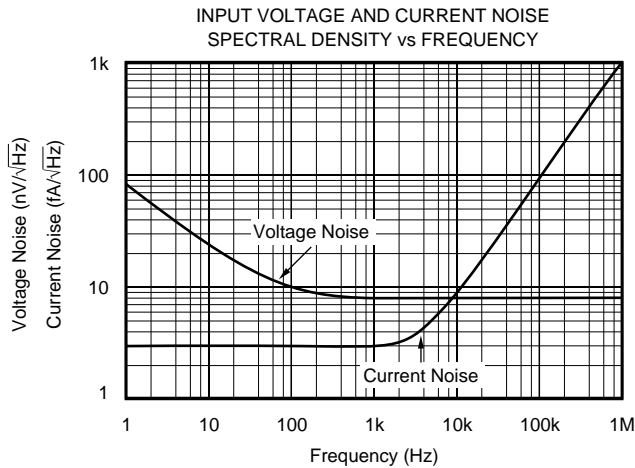
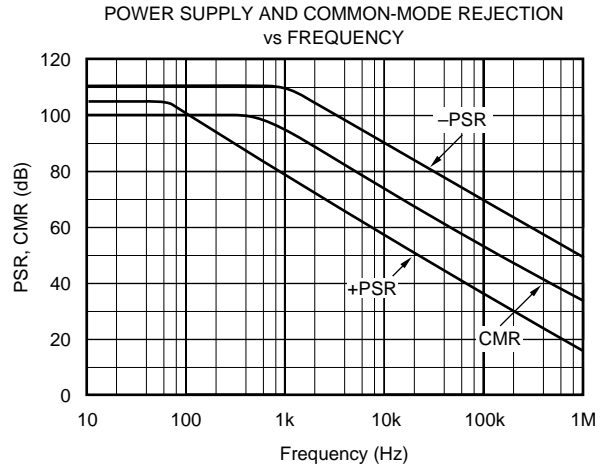
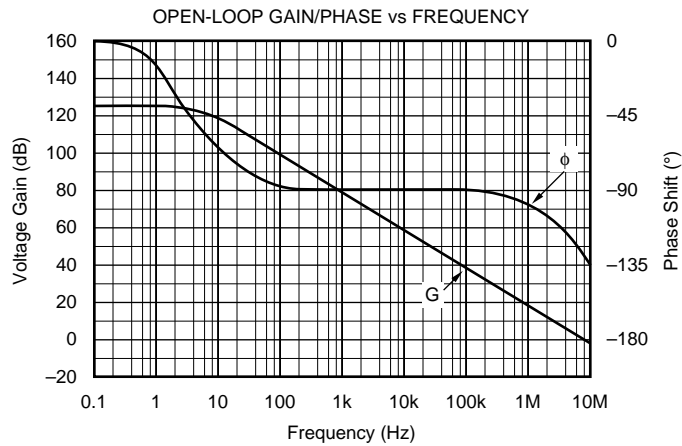
PARAMETER	CONDITION	OPA132P, U OPA2132P, U			OPA132PA, UA OPA2132PA, UA OPA4132PA, UA			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE Input Offset Voltage vs Temperature ⁽¹⁾ vs Power Supply Channel Separation (dual and quad)	Operating Temperature Range $V_S = \pm 2.5\text{V}$ to $\pm 18\text{V}$ $R_L = 2\text{k}\Omega$		± 0.25 ± 2 5 0.2	± 0.5 ± 10 15		± 0.5 * * *	± 2 * 30	mV $\mu\text{V}/^{\circ}\text{C}$ $\mu\text{V}/\text{V}$ $\mu\text{V}/\text{V}$
INPUT BIAS CURRENT Input Bias Current ⁽²⁾ vs Temperature Input Offset Current ⁽²⁾	$V_{CM} = 0\text{V}$ $V_{CM} = 0\text{V}$		+5 See Typical Curve ± 2	± 50 ± 50		* * *	* *	pA pA
NOISE Input Voltage Noise Noise Density, $f = 10\text{Hz}$ $f = 100\text{Hz}$ $f = 1\text{kHz}$ $f = 10\text{kHz}$ Current Noise Density, $f = 1\text{kHz}$			23 10 8 8 3			* * * * *		$\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{fA}/\sqrt{\text{Hz}}$
INPUT VOLTAGE RANGE Common-Mode Voltage Range Common-Mode Rejection	$V_{CM} = -12.5\text{V}$ to $+12.5\text{V}$	(V-) +2.5 96	± 13 100	(V+) -2.5	* 86	* 94	*	V dB
INPUT IMPEDANCE Differential Common-Mode	$V_{CM} = -12.5\text{V}$ to $+12.5\text{V}$		$10^{13} \parallel 2$ $10^{13} \parallel 6$			* *		$\Omega \parallel \text{pF}$ $\Omega \parallel \text{pF}$
OPEN-LOOP GAIN Open-Loop Voltage Gain	$R_L = 10\text{k}\Omega$, $V_O = -14.5\text{V}$ to $+13.8\text{V}$ $R_L = 2\text{k}\Omega$, $V_O = -13.8\text{V}$ to $+13.5\text{V}$ $R_L = 600\Omega$, $V_O = -12.8\text{V}$ to $+12.5\text{V}$	110 110 110	120 126 130		104 104 104	* 120 120		dB dB dB
FREQUENCY RESPONSE Gain-Bandwidth Product Slew Rate Settling Time: 0.1% 0.01% Overload Recovery Time Total Harmonic Distortion + Noise	$G = -1$, 10V Step, $C_L = 100\text{pF}$ $G = -1$, 10V Step, $C_L = 100\text{pF}$ $G = \pm 1$ 1kHz, $G = 1$, $V_O = 3.5\text{V}_{\text{rms}}$ $R_L = 2\text{k}\Omega$ $R_L = 600\Omega$		8 ± 20 0.7 1 0.5 0.00008 0.00009			* * * * * * *		MHz V/ μs μs μs μs % %
OUTPUT Voltage Output, Positive Negative Positive Negative Positive Negative Short-Circuit Current Capacitive Load Drive (Stable Operation)	$R_L = 10\text{k}\Omega$ $R_L = 2\text{k}\Omega$ $R_L = 600\Omega$	(V+) -1.2 (V-) +0.5 (V+) -1.5 (V-) +1.2 (V+) -2.5 (V-) +2.2	(V+) -0.9 (V-) +0.3 (V+) -1.2 (V-) +0.9 (V+) -2.0 (V-) +1.9 ± 40 See Typical Curve		* * * * * * * *	* * * * * * *		V V V V V V mA
POWER SUPPLY Specified Operating Voltage Operating Voltage Range Quiescent Current (per amplifier)	$I_O = 0$	± 2.5	± 15 ± 4	± 18 ± 4.8	* *	* *	* *	V V mA
TEMPERATURE RANGE Operating Range Storage Thermal Resistance, θ_{JA} 8-Pin DIP SO-8 Surface-Mount 14-Pin DIP SO-14 Surface-Mount		-40 -40		+85 +125	* *		* *	$^{\circ}\text{C}$ $^{\circ}\text{C}$ $^{\circ}\text{C}/\text{W}$ $^{\circ}\text{C}/\text{W}$ $^{\circ}\text{C}/\text{W}$ $^{\circ}\text{C}/\text{W}$

* Specifications same as OPA132P, OPA132U.

NOTES: (1) Guaranteed by wafer test. (2) High-speed test at $T_J = 25^{\circ}\text{C}$.

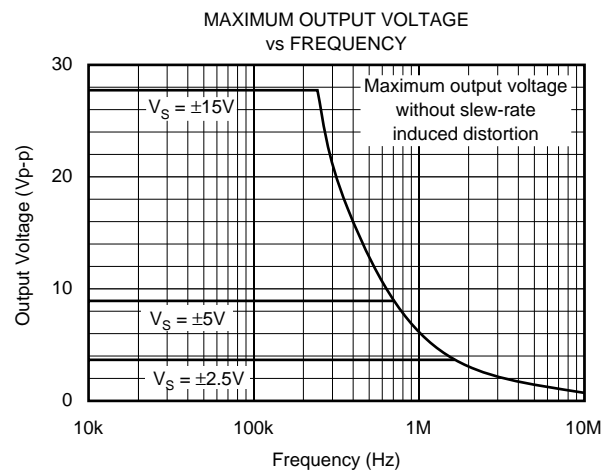
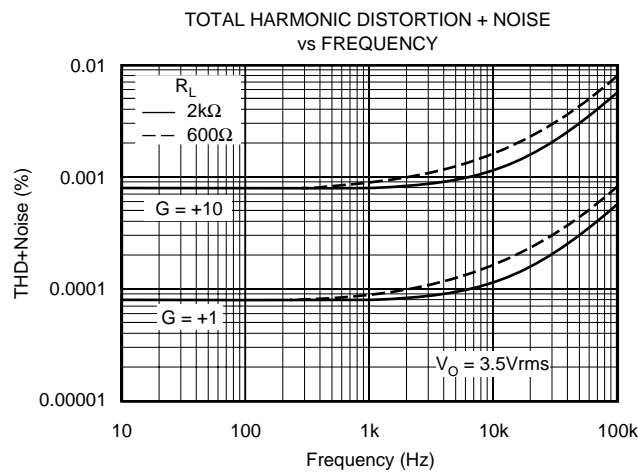
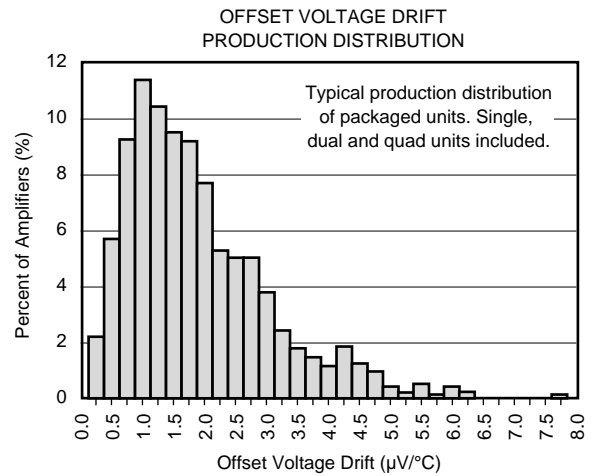
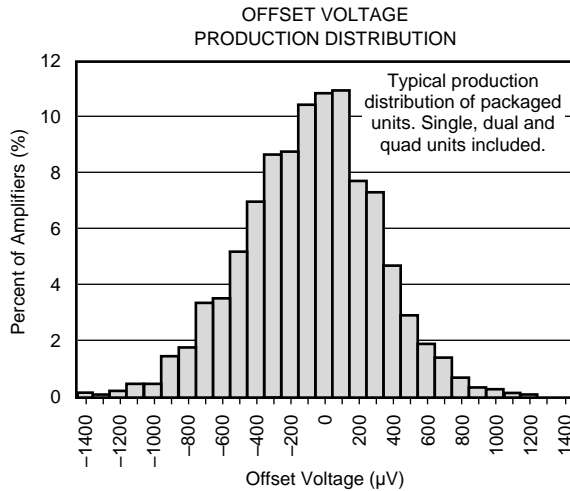
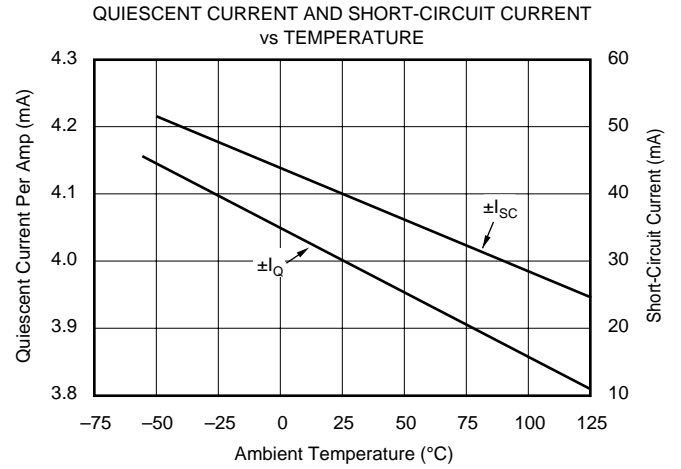
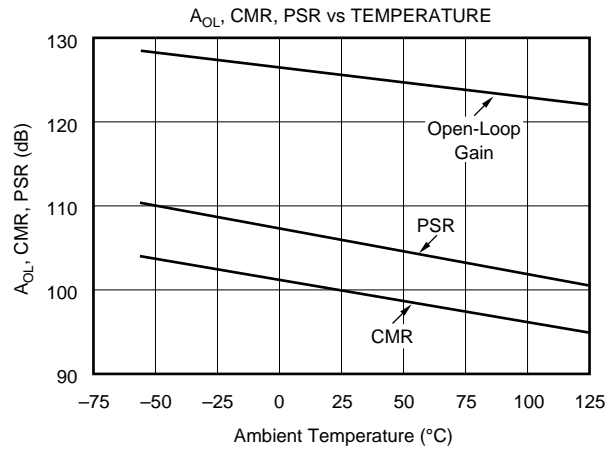
TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $R_L = 2\text{k}\Omega$, unless otherwise noted.



TYPICAL PERFORMANCE CURVES (Cont.)

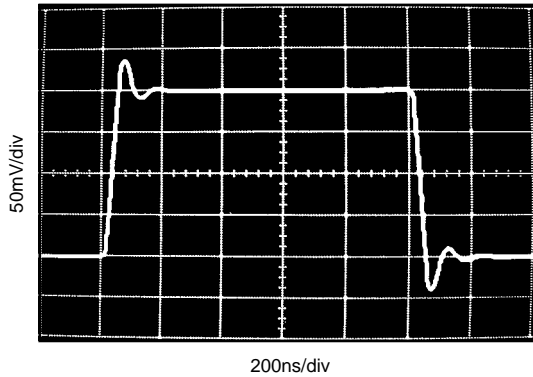
At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $R_L = 2\text{k}\Omega$, unless otherwise noted.



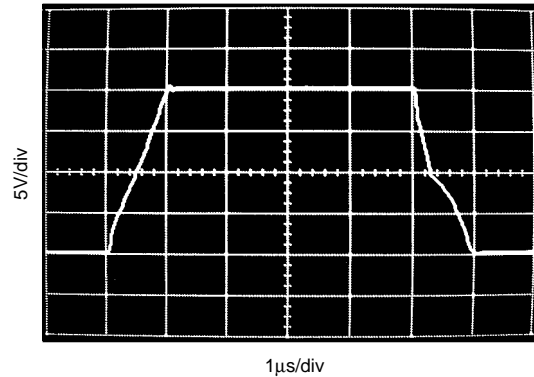
TYPICAL PERFORMANCE CURVES (Cont.)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $R_L = 2\text{k}\Omega$, unless otherwise noted.

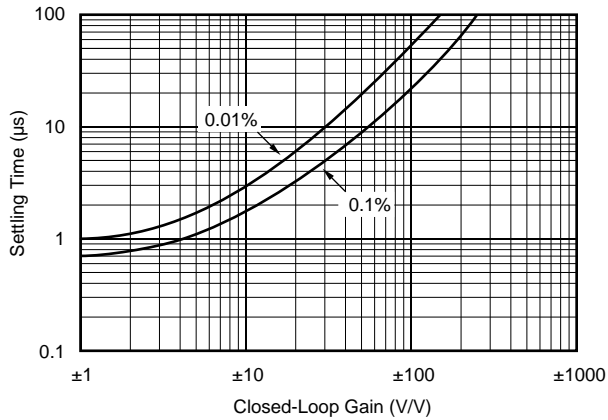
SMALL-SIGNAL STEP RESPONSE
 $G = 1$, $C_L = 100\text{pF}$



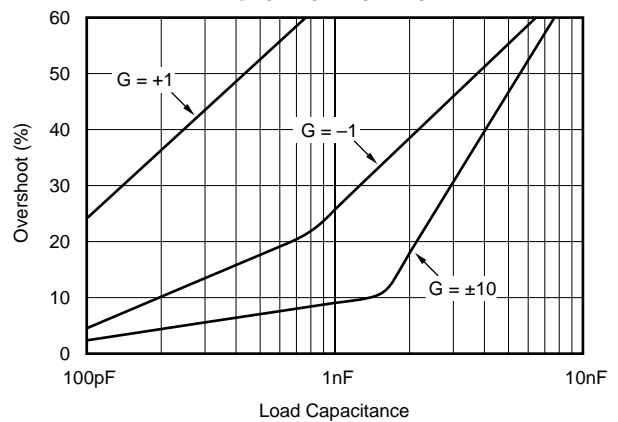
LARGE-SIGNAL STEP RESPONSE
 $G = 1$, $C_L = 100\text{pF}$



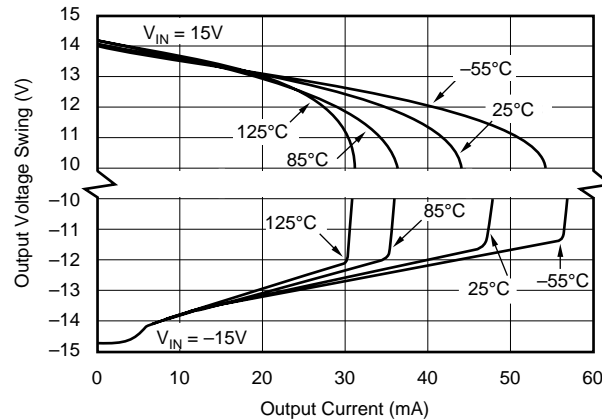
SETTLING TIME vs CLOSED-LOOP GAIN



SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE



OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



APPLICATIONS INFORMATION

OPA132 series op amps are unity-gain stable and suitable for a wide range of general-purpose applications. Power supply pins should be bypassed with 10nF ceramic capacitors or larger.

OPA132 op amps are free from unexpected output phase-reversal common with FET op amps. Many FET-input op amps exhibit phase-reversal of the output when the input common-mode voltage range is exceeded. This can occur in voltage-follower circuits, causing serious problems in control loop applications. OPA132 series op amps are free from this undesirable behavior. All circuitry is completely independent in dual and quad versions, assuring normal behavior when one amplifier in a package is overdriven or short-circuited.

OPERATING VOLTAGE

OPA132 series op amps operate with power supplies from $\pm 2.5\text{V}$ to $\pm 18\text{V}$ with excellent performance. Although specifications are production tested with $\pm 15\text{V}$ supplies, most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown in the typical performance curves.

OFFSET VOLTAGE TRIM

Offset voltage of OPA132 series amplifiers is laser trimmed and usually requires no user adjustment. The OPA132 (single op amp version) provides offset voltage trim connections on pins 1 and 8. Offset voltage can be adjusted by connecting a potentiometer as shown in Figure 1. This adjustment should be used only to null the offset of the op amp, not to adjust system offset or offset produced by the signal source. Nulling offset could degrade the offset voltage drift behavior of the op amp. While it is not possible to predict the exact change in drift, the effect is usually small.

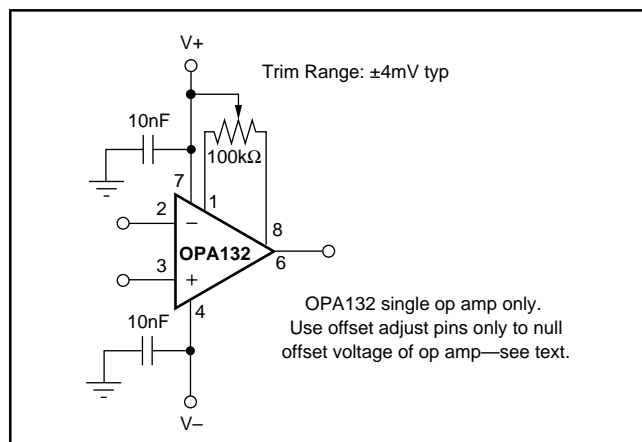


FIGURE 1. OPA132 Offset Voltage Trim Circuit.

INPUT BIAS CURRENT

The FET-inputs of the OPA132 series provide very low input bias current and cause negligible errors in most applications. For applications where low input bias current is crucial, junction temperature rise should be minimized. The input bias current of FET-input op amps increases with temperature as shown in the typical performance curve “Input Bias Current vs Temperature.”

The OPA132 series may be operated at reduced power supply voltage to minimize power dissipation and temperature rise. Using $\pm 3\text{V}$ supplies reduces power dissipation to one-fifth that at $\pm 15\text{V}$.

The dual and quad versions have higher total power dissipation than the single, leading to higher junction temperature. Thus, a warmed-up quad will have higher input bias current than a warmed-up single. Furthermore, an SOIC will generally have higher junction temperature than a DIP at the same ambient temperature because of a larger θ_{JA} . Refer to the specifications table.

Circuit board layout can also help minimize junction temperature rise. Temperature rise can be minimized by soldering the devices to the circuit board rather than using a socket. Wide copper traces will also help dissipate the heat by acting as an additional heat sink.

Input stage cascode circuitry assures that the input bias current remains virtually unchanged throughout the full input common-mode range of the OPA132 series. See the typical performance curve “Input Bias Current vs Common-Mode Voltage.”

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA132P	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI			
OPA132P1	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI			
OPA132PA	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI			
OPA132PA2	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI			
OPA132U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 132U	Samples
OPA132U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 132U	Samples
OPA132U/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 132U	Samples
OPA132U1	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI			
OPA132UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 132U A	Samples
OPA132UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 132U A	Samples
OPA132UA/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 132U A	Samples
OPA132UA/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 132U A	Samples
OPA132UA2	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI			
OPA132UAE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 132U A	Samples
OPA132UAG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 132U A	Samples
OPA132UG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 132U	Samples
OPA2132P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA2132P	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2132PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA2132P A	Samples
OPA2132PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA2132P A	Samples
OPA2132PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA2132P	Samples
OPA2132U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 2132U	Samples
OPA2132U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 2132U	Samples
OPA2132U/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 2132U	Samples
OPA2132U/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 2132U	Samples
OPA2132UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 2132U A	Samples
OPA2132UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 2132U A	Samples
OPA2132UA/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 2132U A	Samples
OPA2132UAE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 2132U A	Samples
OPA2132UAG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 2132U A	Samples
OPA2132UE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 2132U	Samples
OPA2132UG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 2132U	Samples
OPA4132PA	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI			
OPA4132UA	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA4132UA	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA4132UA/2K5	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA4132UA	Samples
OPA4132UA/2K5E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA4132UA	Samples
OPA4132UA/2K5G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA4132UA	Samples
OPA4132UAE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA4132UA	Samples
OPA4132UAG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA4132UA	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2132UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4132UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2132UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA4132UA/2K5	SOIC	D	14	2500	367.0	367.0	38.0

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com