NATIONAL SENIOR CERTIFICATE EXAMINATION
NOVEMBER 2020

ELECTRICAL TECHNOLOGY: DIGITAL

MARKING GUIDELINES

Time: 3 hours 200 marks

These marking guidelines are prepared for use by examiners and sub-examiners, all of whom are required to attend a standardisation meeting to ensure that the guidelines are consistently interpreted and applied in the marking of candidates' scripts.

The IEB will not enter into any discussions or correspondence about any marking guidelines. It is acknowledged that there may be different views about some matters of emphasis or detail in the guidelines. It is also recognised that, without the benefit of attendance at a standardisation meeting, there may be different interpretations of the application of the marking guidelines.

GENERAL

- All marking is done by the marker in red.
- The marker may not make any corrections on the candidate's answer book.
- The memorandum serves as a guideline only.
- Alternative answers must be considered.
- A tick must be placed at each correct answer for which a candidate receives a mark.
- A cross "x" must be placed at each answer that is wrong.
- Calculations are marked as follows, unless stated otherwise:
  - 1 mark is allocated for the formula.
  - 1 mark is allocated for the substitution.
  - 1 mark is allocated for the answer with the correct applicable unit shown.
  - If the unit is indicated incorrectly, the answer is marked as wrong.
  - If an incorrect answer has to be used in the subsequent calculation, it is taken as correct in that calculation and the answer of the relevant calculation must be recalculated by the marker and marked accordingly. An arrow must be inserted from the incorrect answer to the subsequent calculation where substitution has been done with the incorrect answer to show that the incorrect answer has been taken into consideration.
- Sketches are marked by allocating 1 mark for the drawing if it was drawn correctly and all the other marks are allocated for the correct labels.
- See also the marking notes at some answers.
- A line must be drawn through all work that is not applicable to the answer, for example rough work.
- A diagonal line must be drawn through the space for questions that the candidate left open.
- A diagonal line must be drawn through all pages of the answer book that were not used by the candidate.
- A horizontal line must be drawn by the marker at the end of each question to indicate the end of the question.
- The marks for each question are written in a circle on the left-hand side at the beginning of the relevant question.
- The mark allocations for answers are written on the right-hand side of the page below one another. No circles are made around these marks.
- This memorandum consists of 16 pages.

QUESTION 1 SAFETY

1.1 Operational equipment refers to fixtures, furnishings, implements, equipment, tools and devices, and anything that is used for any purpose in relation to carrying out duties in the workplace.

1.2 To provide for the health and safety of persons at work.
To provide for the health and safety of persons regarding the use of operational equipment and machinery.
The protection of persons other than persons at work against threats to health and safety resulting from or in relation to the activities of persons at work.
To establish an advisory board for occupational health and safety; and to provide for matters in relation thereto.

MARKING NOTE

Any two answers are correct.

1.3 (Section 85.7 & 8)
The employer must display a copy/summary of the safety legislation in a visible place where the workers report for duty.
The employer must ensure that the workplace is safe and keep it safe.
Machines, tools and equipment must be maintained by the employer to ensure that they are safe to use.
The employer must ensure that personal protective equipment is used to safely operate the machines, equipment and tools.
The employer must introduce safety rules and regulations to ensure that the work can be performed safely in the workplace.
The employer must provide the necessary personal protective equipment to employees to enable them to do their work safely.
The employer must train employees to enable them to do their work safely.
The employer must ensure that no worker has to do any work with any unsafe operational equipment.
The employer must appoint a supervisor for workers to ensure that they work correctly and safely according to the safety rules that the employer has introduced.

MARKING NOTE

Any two of the given answers are correct.

1.4 (Section 85.14)

The employee is responsible for his/her own health and safety.
The employee must work together with the employer to create a safe working environment.
The employee must correctly carry out the instructions of the employer or his/her representative regarding safety.
The employee must immediately report any unsafe condition to the employer or his/her representative.
Employees must report any event that threatens their health or any event where they injured themselves to the employer.

MARKING NOTE

Any two answers are correct.

1.5 (Section 85.18)

Check safety measures and regulations.
Identify unsafe actions and unsafe conditions in the workplace.
Investigate accidents together with the employer.
Investigate complaints from employees regarding their safety.
Inform the safety inspector of complaints and investigations in the workplace.
Inform the employer of unsafe conditions in the workplace.
Is familiar with the workplace and machines and equipment for the purpose of safety inspections.
Accompany the employer and the inspectors on inspections at the workplace.
Receive information from inspectors and the employer regarding safety in the workplace.
Serve as a member of the safety committee of the employer.

MARKING NOTE

The given answers serve as a guideline, the candidate must link his/her answers to the Electrical Technology centre.

QUESTION 2 SEMICONDUCTORS

2.1 2.1.1 Positive input voltage terminal
2.1.2 Inverting input terminal
2.1.3 Non-inverting input terminal

2.2 Inverting input: the output signal will be in phase and an amplified version of the input signal.
Non-inverting input: the output signal will be 180° out of phase and an amplified version of the input signal.

MARKING NOTE

The candidate should mention phase shift for the various inputs as applicable.

2.3 $$V_O = V_I\left(1+\frac{Rf}{R_I}\right)$$

$$8,5 = 10\times10^{-3}\left(1+\frac{Rf}{180}\right)$$

$$Rf = 152,82\ k\Omega$$

2.4 2.4.1 Reset input terminal
2.4.2 Trigger input terminal
2.4.3 Threshold voltage input terminal
2.4.4 Capacitor discharge input terminal

2.5 When the output terminal (terminal 3) is low, the discharge input terminal (terminal 7) will react as an open switch. (switch off)
When the output terminal is high, the discharge terminal will react as a closed switch. (switch on)

MARKING NOTE

The words in brackets may be used instead of open switch and closed switch.

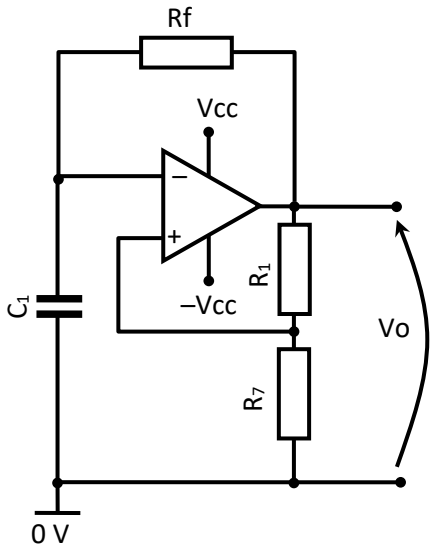
2.6 2.6.1 Switch bounce refers to the small mechanical oscillations or vibration of the switch plate during the switch function.

2.6.2 When these oscillations occur in the switch, digital circuits will interpret each oscillation pulse as a new input signal and react erroneously on the pulse. This action makes the circuit inaccurate and should therefore be prevented.

2.6.3 A switch-bounce prevention circuit uses a monostable multivibrator that ensures that only one single pulse is sent from the switch to the input of a logic circuit.

QUESTION 3 SWITCH AND CONTROL CIRCUITS

3.1



MARKING NOTE

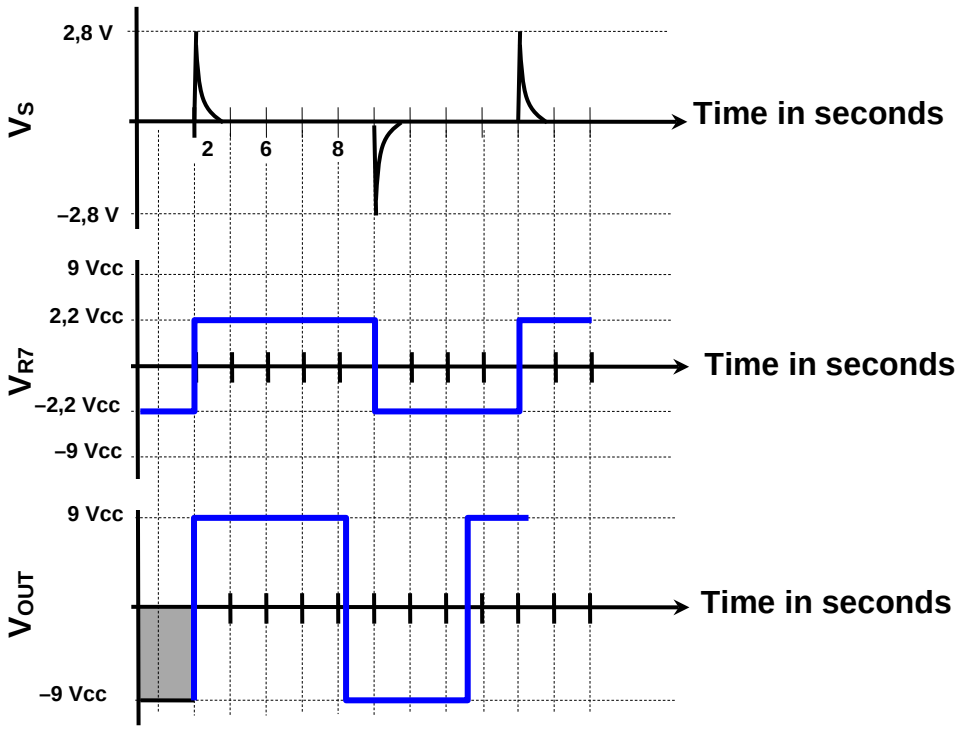
The mark is allocated for the correct positioning of the component with the correct labelling of the component.

3.2 3.2.1 $V_{R7} = V_{CC}\left(\frac{R_7}{R_7 + R_6}\right)$

$V_{R7} = 9 \times \left(\frac{330}{330 + 1000}\right)$

$V_{R7} = 2,233\ V$

3.2.2



3.3 $$V_{OUT} = -\left(V_{i1}\frac{Rf}{R_1} + V_{i2}\frac{Rf}{R_2} + V_{i3}\frac{Rf}{R_3}....\right)$$

$$V_{OUT} = -\left(\left[\left(100\times10^{-3}\right)\frac{18k}{1,8k}\right]+\left[\left(150\times10^{-3}\right)\frac{18k}{2,2k}\right]+\left[\left(-120\times10^{-3}\right)\frac{18k}{4,7k}\right]\right)$$

$$V_{OUT} = -\left(1+1,227+\left(-0,459\right)\right)$$

$$V_{OUT} = -1,767V$$

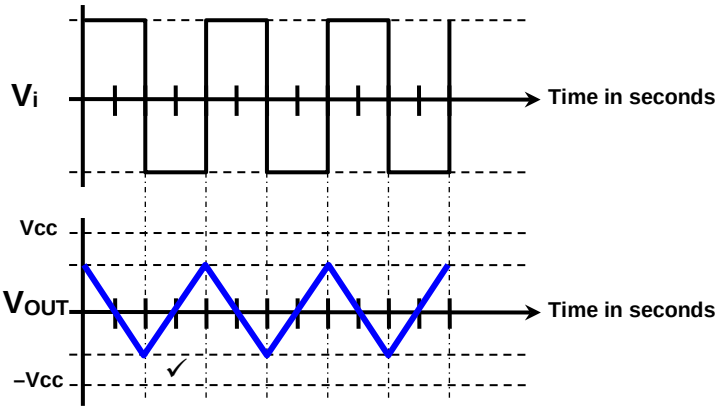
3.4 $$f = \frac{1}{2R_fC}$$

$$f = \frac{1}{2\times680000\times12\times10^{-9}}$$

$$f = 61,274Hz$$

3.5 3.5.1 Integrator

3.5.2



3.6 3.6.1 Monostable 555 timer circuit / 555 monostable multivibrator.

3.6.2 $$T = 1,1R_2C_1$$

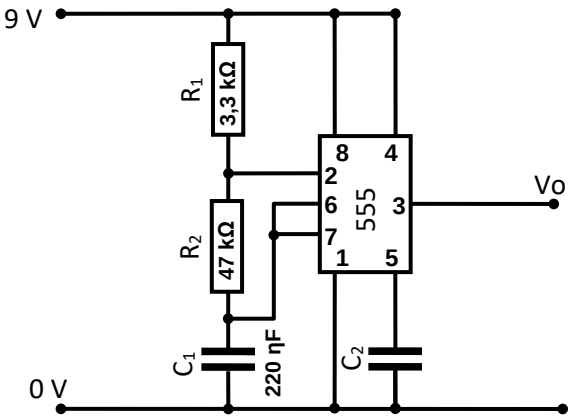
$$T = 1,1\times47k\times33\mu$$

$$T = 1,706s$$

3.6.3 The capacitor charges through resistor R_2 until the capacitor reaches the threshold voltage of ⅔Vcc.
The internal RS latch is activated at ⅔Vcc to reset.
Therefore the output of the 555-IC will tend to be low and the discharge terminal will be activated so that the capacitor can discharge through terminal 7.

3.6.4
- Serves as a pull-up resistor.
- The resistor keeps the voltage at the trigger terminal above ⅓ Vcc.
- When the pulse switch is activated, the voltage at the trigger terminal will be connected to the 0 V potential through the pulse switch.

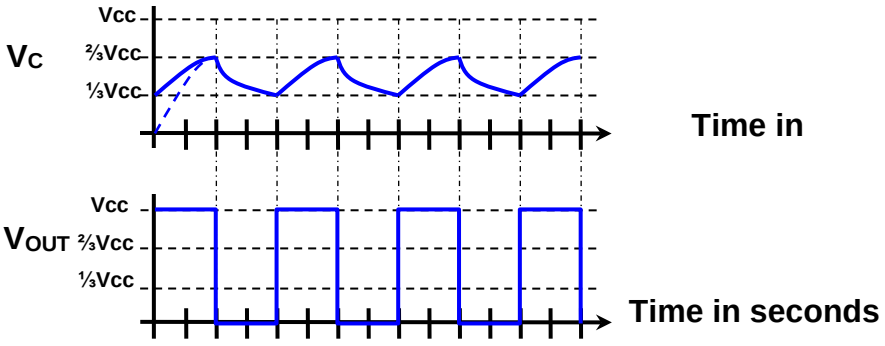
3.7 3.7.1



MARKING NOTE

A mark is allocated for each component that is connected correctly and for which the numbering and value are indicated correctly. (4 marks)
A mark is allocated for the correct connection of pin 6 and pin 7.
A mark is allocated for indicating the output.
A mark is allocated for the correct indication of the input voltage with a value.
A mark is allocated for the correct connection of pin 1 and pin 5; showing capacitor C_2 is optional – if the capacitor is not shown, there may be no connection to pin 5.

3.7.2



MARKING NOTE

The dotted line Vc shows an alternative for only the first waveform and may also be taken as correct.

3.7.3
- When the input voltage to the circuit is switched on, the voltage at the trigger terminal is less than ⅓Vcc.
- The internal RS latch is now set by pin 2.
- Therefore the output of the circuit will tend to be high.
- At this stage pin 7 is switched off and the capacitor now charges through resistors R_1 and R_2 until the voltage across the capacitor reaches ⅔ Vcc.
- The threshold voltage of the 555-IC is now reached and is put on pin 6 and pin 2 simultaneously.
- The internal RS latch is reset by the voltage at pin 6
- and the output of the 555-IC will now tend to be low.
- When the output of the 555-IC tends to be low, pin 7 is activated and the capacitor will now discharge through resistor R_2 to pin 7 to the 0 V potential of the circuit.

QUESTION 4 DIGITAL AND SEQUENTIAL DEVICES

4.1 Liquid crystal is placed between two transparent plates.
The transparent plates are polarised.
A reflecting metal surface is mounted behind the lower plate.
A transparent plastic plate is placed on top of the upper polarised plate.

4.2 Common anode package
or (Absorption display)
This unit has a common positive terminal and each LED segment is connected separately to the 0 V potential by a driver.

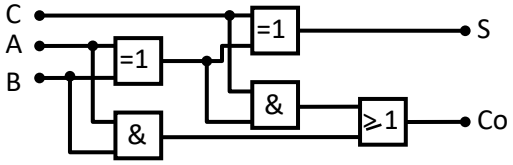
Common cathode package
or (Sourcing display)
This unit has a common negative terminal and each LED segment is connected separately to the positive potential by a driver.

4.3 Input voltage: 2 V
(2,1 to 2,5 may also be taken as correct)
Current flow: 20 mA
Reverse voltage: 6 V
Power: 600 mW
Soldering time: 5 s

MARKING NOTE

Any two of the given answers are correct.

4.4



MARKING NOTE

A mark is allocated to a logic function only if the relevant function's inputs and outputs are connected correctly and labelled correctly where applicable.

4.5 4.5.1

AND	S	R	Q
0	0	0	Qn
0	0	1	Qn
0	1	0	Qn
0	1	1	Qn
1	0	0	Qn
1	0	1	0
1	1	0	1
1	1	1	Prohibited

4.5.2
- AND logic function A does not react, while AND logic function B will react and place a high on its output.
- The inputs on NOR logic function D are now 1,0, respectively, and therefore NOR logic function D will react to its inputs to supply a low on its output, therefore output Not-Q is now low.
- This low on output Not-Q is fed back to NOR logic function C as a memory element.
- The inputs of NOR logic function C is now 0,0.
- NOR logic function C reacts to this change and places a high on its output to change output Q to high.
- This high of output Q is fed back to NOR logic function D as a memory element to keep output Not-Q a low.

4.6 When the clock pulse's wave leading edge tends to be high, the input NAND logic functions will react to their respective inputs.
The circuit is a wave leading edge trigger circuit, therefore the input clock is available only on the wave leading edge for the input logic gates to react and thereafter they will return to an output of high again.
The inputs to NAND logic function A are 1,1,1 and the inputs to NAND logic function C are 1,1,0.
NAND logic function A will react to its inputs to place a low on the input of NAND logic function B.
NAND logic function C does not react to its inputs and therefore its output will remain high unchanged.
NAND logic function B reacts to its input and changes its output to high.

This high is fed back to NAND logic function D and to NAND logic function C as a memory element and NAND gate D reacts to change its output to low.
This low is now fed back as a memory element to the input of NAND logic function B and to NAND logic function A.
NAND logic function A and NAND logic function C will not react to the feedback memory values and therefore their outputs will remain high unchanged.
NAND logic functions B and D use the memory values that were fed back to keep their outputs unchanged where Q = 1 and Q' = 0.

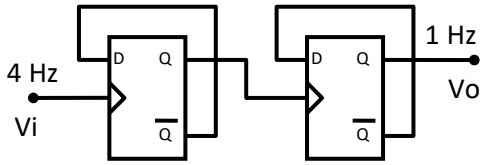
4.7 A synchronous counter uses a common clock pulse that tries to clock all the various JK flip-flops simultaneously.

An asynchronous counter has a clock pulse only on the first JK latch that serves as the LSB. The output of each JK latch is set as the clock pulse for the next JK latch.

4.8 4.8.1 The OR logic function turns the counter into a self-stop counter and the counting function will stop when the value 0110_2 is reached.

4.8.2
- The circuit will react to the wave leading edge.
- JK FFA is connected in the toggle function and will toggle from 1 to 0.
- JK FFB is also in the toggle function and changes the output from 0 to 1.
- JK FFC's inputs are 0, because AND logic function's one input is a 0 and therefore it places a 0 on FFC's inputs.
- Consequently FFC will not react to the clock pulse, because its inputs are in the unchanged state and its output will therefore remain 1 unchanged and the number 110_2 is now available on the counter.
- Because outputs QC and QB are connected to an AND-logic function C, the AND-logic function will place a high (1) on the output that serves as an input to the OR logic function.
- Therefore the OR logic function will keep the output high (1) and will not react any further to any incoming clock pulses.
- Consequently the counter will stop counting and will then stop by itself.

4.9



MARKING NOTE

1 mark is allocated for each D latch with feedback from Not-Q to input D shown and labelled correctly. (2 marks)
1 mark is allocated for the connection of Q to clock input of D latch 2.
1 mark is allocated for indicating the input on the clock input of D latch 1.
1 mark is allocated for indicating the output on Q of D latch 2.
A mark is allocated for indicating the input and output frequencies correctly.

QUESTION 5 MICROCONTROLLERS

5.1 Reduce the size of circuits because discrete components are replaced within a single IC package to perform the same function.
Circuits are cheaper because discrete components are placed in an IC format and therefore manufacturers have to stock and use fewer components.
Circuits are more reliable because fewer components are used to manufacture the IC than when discrete components are used.
Reduce production cost because manufacturers have to place fewer components on factory lines and stock fewer components.

MARKING NOTE

Any two correct answers are accepted.

5.2 Cannot supply high output currents to control other peripherals.
Cannot supply high output voltages to control peripherals with high voltages.
Have low output power and therefore cannot control high-power equipment directly.
Is sensitive to static electricity.

MARKING NOTE

Any of the given answers is correct.

5.3 5.3.1
- D: (RAM) Random-access memory where data is stored temporarily so that it can be read later for further calculations.
- E: (ROM) Read-only memory where the programs and instructions are stored and no data can be stored here.

5.3.2
- The circuit connects the various inputs and outputs to the communication bus of the PIC
- and also determines which terminal will be used as an input or output.

5.3.3
- The processor receives instructions (program) from the ROM and data from the inputs and then carry out the instructions in sequence (do calculations)
- to provide the required outputs on the output terminals.

5.3.4
- Communication bus
- Conductors that connect the various subcircuits of the PIC to one another so that data can be exchanged between these subcircuits.

5.4 Data bit
Control bit / Counter bit
Address bit
Clock-pulse bit

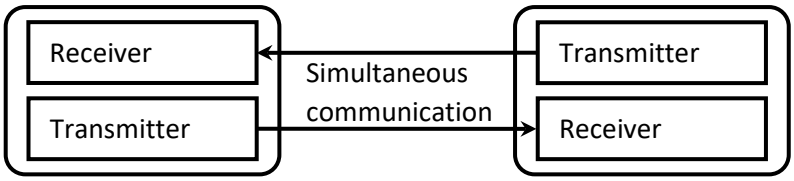
MARKING NOTE

Any three answers are correct.

5.5 Microcontroller consists of all the necessary subcircuits, consisting of memory circuits, CPU, input-output-circuits and clock generator, that are placed within a single IC package to function on its own.
A microprocessor is only the control unit that receives the operations of a program or instructions and inputs, processes them and provides a certain output. It cannot function on its own and depends on external equipment.

5.6 It is an electronic circuit that is used to convert an analogue input signal into a digital signal and then put it on the data bus for processing by the CPU.

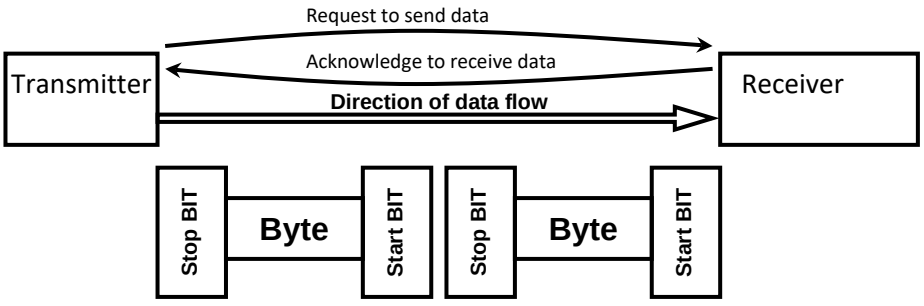
5.7



5.8 Synchronous communication uses a common clock pulse to synchronise the transmitter and the receiver.
Asynchronous system does not have a clock pulse to synchronise the system and uses a fixed data package.

5.9 A higher data transfer rate can be maintained.
Transmitter and receiver use the same clock pulse.

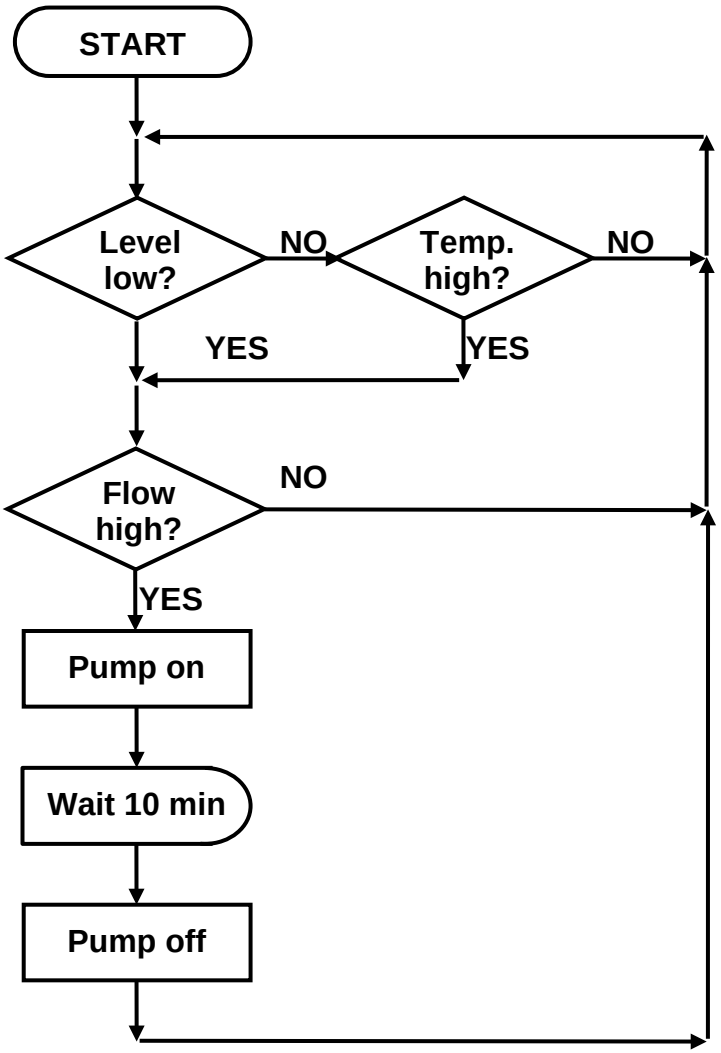
5.10



5.11 Universal Asynchronous Receiver Transmitter logic chip
that receives parallel data from the CPU
and converts it into series data
and then places the data on the output terminal.

5.12 The master pulls the SDA line low
while the SCL line is kept high.
The SCL line is now pulled low by the master as an indication that the data is going to start.
A clock pulse is created on the SCL line.
An address BIT is now sent to activate the relevant slave with the HSB first and a read or write bit at the end to indicate to the slave what must be done.
An ACKBIT / NACKBIT is placed after the read or write bit to indicate that a byte of data has been created.
The master now hands over to the slave and the slave must pull the SDA line low before the eighth clock pulse is created to indicate that the slave accepts the data.
When the slave has accepted the data, the master pulls the SCL line high as an indication that the data transmission process is completed.

5.13



MARKING NOTE

A mark is allocated to each block if the relevant block's description and output data lines are correct. (7 marks)
3 marks are allocated for data flow lines as shown if they are indicated correctly.
If function of temp. and level may be swapped and then still be taken as correct.

Total: 200 marks