NATIONAL SENIOR CERTIFICATE EXAMINATION
NOVEMBER 2020

ELECTRICAL TECHNOLOGY: ELECTRONICS

MARKING GUIDELINES

Time: 3 hours | 200 marks

These marking guidelines are prepared for use by examiners and sub-examiners, all of whom are required to attend a standardisation meeting to ensure that the guidelines are consistently interpreted and applied in the marking of candidates' scripts.

The IEB will not enter into any discussions or correspondence about any marking guidelines. It is acknowledged that there may be different views about some matters of emphasis or detail in the guidelines. It is also recognised that, without the benefit of attendance at a standardisation meeting, there may be different interpretations of the application of the marking guidelines.

QUESTION 1 OCCUPATIONAL HEALTH AND SAFETY

1.1
- Teamwork helps a team to meet its goals.
- Teamwork helps a team deliver quality work.
- Teamwork can win the respect of your co-workers.
- Working together as a team can improve discipline in the workshop.
- Teamwork will lead to improved productivity.

(Any TWO)

1.2 'Horseplay' is an unsafe act because it is inappropriate behaviour by learners in the workshop that compromises the safety of themselves and others.
It distracts others that could lead to accidents or incidents.

1.3 To review the effectiveness of health and safety measures.
To identify hazards and potential major incidents at the workplace.

1.4 An accident is an unplanned, uncontrolled event caused by unsafe acts and or unsafe conditions resulting in a personal injury, illness or the death of an employee.
An accident means an accident arising out of and in the course of an employee's employment and resulting in personal injury, illness or the death of the employee.

1.5
- Faulty tools or equipment
- Poor ventilation
- Poor quality of or missing guards on machines
- Excessive noise
- Lack of knowledge of emergency procedures

(Any ONE)

QUESTION 2 RLC CIRCUITS

2.1
- Q-factor for a parallel circuit concerns the relationship between the resistance and the reactance of the circuit.
- The Q-factor of the circuit is the ratio between the reactive power of either the inductor or the capacitor at resonance and the active power of the resistance.

2.2 Factors that affect the impedance of an RLC circuit:
- Frequency
- Inductance
- Capacitance

2.3 Any TWO of the following states can occur:
Z = R
$V_L = V_C$
$V_R = V_T$
$X_L = X_C$
Cos θ = 1
R = minimum
I = maximum
(Any TWO)

2.4 2.4.1

$$I_T = \sqrt{I_R{}^2 + (I_L - I_C)^2}$$
$$I_T = \sqrt{6^2 + (4-3)^2}$$
$$I_T = 6{,}083\ A$$

2.4.2

$$\cos\theta = \frac{I_R}{I_T}$$
$$\theta = \cos^{-1}\frac{I_R}{I_T}$$
$$\theta = \cos^{-1}\frac{6}{6{,}083}$$
$$\theta = 9{,}59^\circ$$

2.4.3 The phase angle is lagging because the inductive current is larger than the capacitive current.

NOTE: *If only the second part of the answer is given = 1 mark*

2.5 2.5.1

$$f_r = \frac{1}{2 \times \pi \times \sqrt{L \times C}}$$

$$f_r = \frac{1}{2 \times \pi \times \sqrt{80 \times 10^{-3} \times 33 \times 10^{-6}}}$$

$$f_r = 97{,}95\ Hz$$

2.5.2 $I = \frac{V_S}{Z}$ (R = Z during resonation)

$$I = \frac{120}{30}$$

$$I = 4\ A$$

2.5.3

$$V_L = I \times X_L$$

$$V_L = 4 \times 49{,}24$$

$$V_L = 196{,}94\ V$$

2.6 2.6.1 (a)

$$X_L = \frac{V_S}{I_L}$$

$$X_L = \frac{100}{2}$$

$$X_L = 50\ \Omega$$

(b)

$$X_C = \frac{V_S}{I_C}$$

$$X_C = \frac{100}{6}$$

$$X_C = 16{,}67\ \Omega$$

(c)

$$I_X = I_C - I_L$$

$$I_X = 6 - 2$$

$$I_X = 4\ A$$

NOTE: *If the learner shows a difference in reactive currents, he/she must get 3 marks.*

(d)

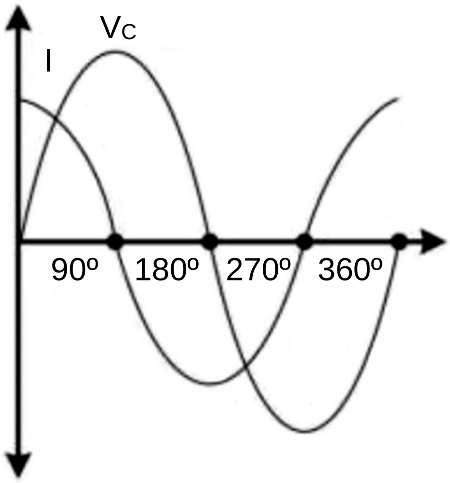
$$I_T = \sqrt{I_R{}^2 + (I_C - I_L)^2}$$

$$I_T = \sqrt{5^2 + (6-2)^2}$$

$$I_T = 6{,}4\ A$$

2.6.2 Phase angle is leading.

2.7 ***NOTE:*** *If the learner drew only one signal = 0 marks, it doesn't show relation.*



QUESTION 3 SEMICONDUCTOR DEVICES

3.1 The JFET is a voltage-controlled device.

3.2 3.2.1 Enhancement mode

3.2.2 ± 4 mA

3.2.3
- When a rising negative voltage ($-V_{GS}$) is applied to the gate, the drain-source current (I_{DS}) decreases.
- When a rising positive voltage ($+V_{GS}$) is applied to the gate the drain-source current (I_{DS}) increases. This confirms that the gate material is p-type which is forward biased by a positive voltage and reverse biased by a negative voltage.

3.3 3.3.1 P-channel Enhancement mode MOSFET

3.3.2
- The drain must be connected to positive.
- The source must be connected to negative.
- The gate voltage must be positive.

3.4 3.4.1 Saturation region

3.4.2 At point C the UJT triggers ON. As the UJT is triggered, its internal resistance and voltage will decrease while the current increases. This is contrary to Ohm's law and is called negative resistance.

3.5 3.5.1 Darlington pair

3.5.2
- Very high current gain.
- Improved input impedance.
- When used in common collector pair, it develops very low output impedance.

(Any TWO)

3.6 3.6.1

$$V_{uit} = V_{in} \times \left(-\frac{R_F}{R_{IN}} \right)$$

$$V_{uit} = 2 \times \left(-\frac{100 \times 10^3}{12 \times 10^3} \right)$$

$$V_{uit} = -16{,}67\ V$$

3.6.2 The amplifier is driven into saturation which causes the tops and bottoms of the peaks to be clipped. If the learner identified that the input is fed into the inverting input, there will be a 180 degree phase shift on the output = 2 marks.

3.6.3 +15 volt –15 volt

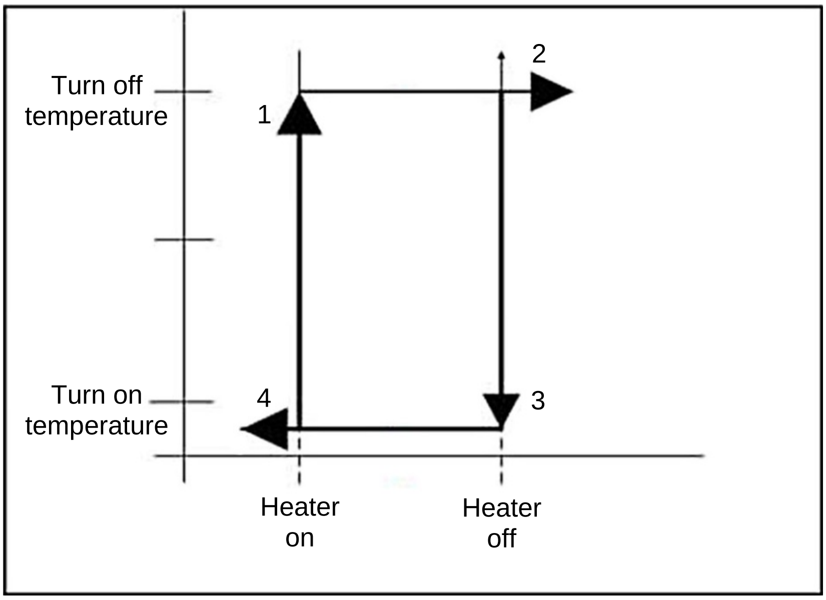
3.7
- Timing functions (turning a light on and off for a prescribed time)
- Creating a warning light
- Pulse, oscillation and signal generation
- Digital logic probes
- Controlling the positioning of a servo device

(Any TWO relevant answers)

3.8 In the construction of this IC there are three series-connected resistors of identical value, 5 kΩ. These resistors divide the voltages to 2/3 and 1/3 of the supply voltage.

QUESTION 4 SWITCHING CIRCUITS

4.1



4.2 4.2.1 Resistors R_1 and R_2 are pull-up resistors. R_1 and R_2 hold both trigger pin 2 and reset pin 4 high.

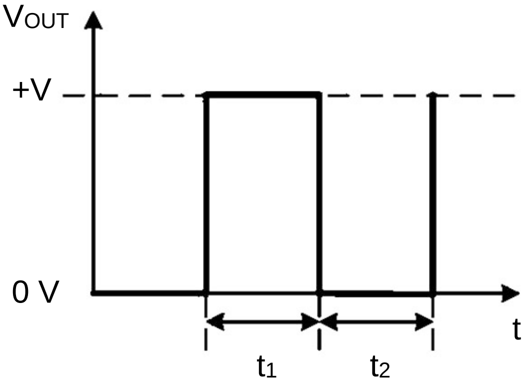
4.2.2 When set switch S_1 is pressed, trigger pin 2 will be pulled low and cause the IC output to 'flip' and rise high turning the LED on.

4.2.3 Threshold pin 6 is purposefully held at 0 V causing the IC not to reset, keeping the output high when S_1 is pressed.

4.3 4.3.1 Any ONE application of an astable multivibrator.

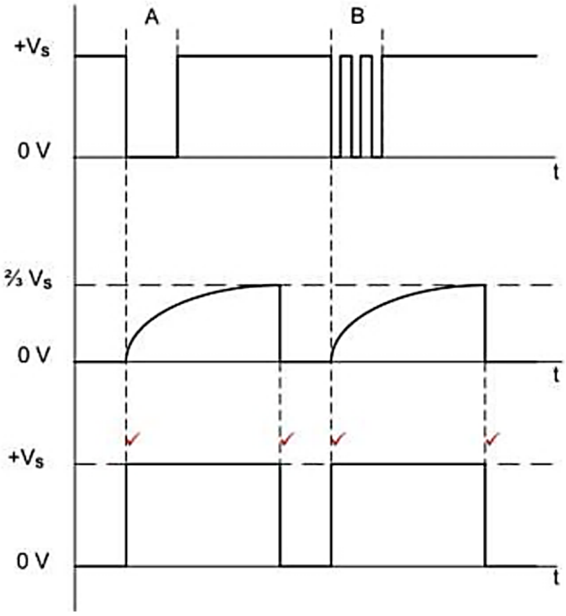
- Clock pulse generator
- Wave-forming circuits
- Device that requires square waves
- Schmitt-trigger circuits

4.3.2



4.3.3
- If the value of R_1 is increased, the RC time constant of the charging circuit (t_1) increases,
- keeping the output of the 555 IC high for longer.
- This means that the positive output pulse (high) will be longer than the negative output pulse (low).

4.4 4.4.1



NOTE: *If the amplitude of the output signal exceeds +Vs = –1 mark*
Inverted polarity: –2 marks

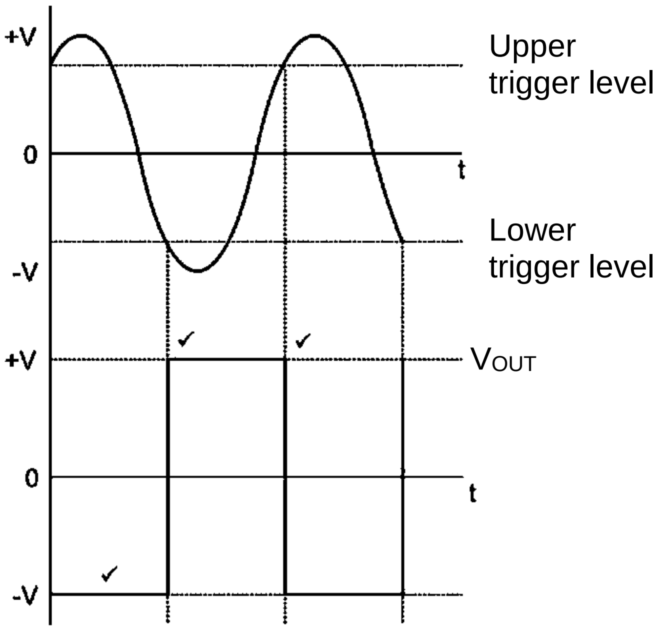
4.4.2 Trigger pulse B appears like a train of 'on' and 'off' pulses which is known as contact switch bounce.

NOTE: *Switch bounce only = 2 marks*

4.4.3
- When the first trigger pulse is applied, Pin 7 of the 555 will be pulled (set) high to allow the capacitor to start charging.
- The charging period of the capacitor will only end once it has reached 2/3 Vcc
- Any other pulses applied during this period will have no effect.

4.5 4.5.1
- Resistors R_F and R_1 create a voltage divider.
- They divide the output voltage which causes part of the output voltage to appear across R_1.
- The voltage across R_1 is fed on the Op-amp's non-inverting input.

4.5.2



NOTE: *1 mark = correct orientation*
2 marks = 1 mark for each correctly identified trigger point

4.5.3
- If the value of R_F increases, the voltage across R1 will decrease according to Kirchhoff's voltage law.
- Therefore, the voltage fed back to the non-inverting input will decrease.
- This will lead to a decrease in trigger voltage.

4.6
- First stage of many radio receivers to clean up noise.
- To eliminate switch bounce in digital circuits.
- Varying input waveforms, for instance sine wave, changed into square wave or rectangular wave.
- Signal recovery after experiencing severe distortion.
- Day-night switch/wave transformer

4.7 4.7.1 By adding another input resistor in shunt to the summing amplifier input.

4.7.2

$$V_{out} = -\left(V_1\frac{R_F}{R_1} + V_2\frac{R_F}{R_2} + V_3\frac{R_F}{R_3}\right)$$

$$V_{out} = -\left(50\times10^{-3}\frac{100\times10^3}{5\times10^3} + 150\times10^{-3}\frac{100\times10^3}{10\times10^3} + 300\times10^{-3}\frac{100\times10^3}{15\times10^3}\right)$$

$$V_{out} = -(1+1{,}5+2)$$

$$V_{out} = -4{,}5\ V$$

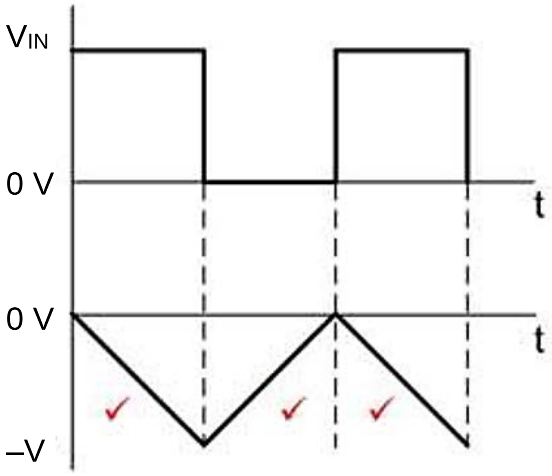
4.7.3 The answer in Question 4.7.2 is negative because the inputs are fed into the inverting input which will cause the output to be 180º out of phase.

4.8 4.8.1 Resistor R_2 determines the reference voltage of the comparator.

4.8.2
- Resistors R_1 and R_2 create a voltage divider that
- feeds a reference voltage into the non-inverting input
- while its inverting input is usually fed by a transducer.
- These two voltages are compared and as soon as the voltage on the inverting input goes higher than the non-inverting input, the amplifier's output will go into negative saturation.
- The moment the non-inverting voltage goes higher than the inverting voltage, the amplifier's output will go into positive saturation.

4.8.3 To adjust the reference voltage, resistor R_2 can be replaced by a variable resistor.

4.9 4.9.1



4.9.2
- If the RC time constant is short, the capacitor will charge rapidly
- reaching the maximum input voltage and remaining there until the input falls again.
- This results in the output having rounded leading and trailing edges
- with a flat top resembling a distorted square wave.

***NOTE:** The textbook only mentioned the passive integrator of which the following will be accepted. The following is the correct response for the Op-amp integrator.*

- If the RC time constant is short, the output will rise in a linear manner until reaching the maximum output voltage
- and remaining there until the input falls again.
- This results in the output having straight sloping leading and trailing edges with flat tops and bottoms.
- It will resemble a triangular wave with its top and bottom peaks cut off.

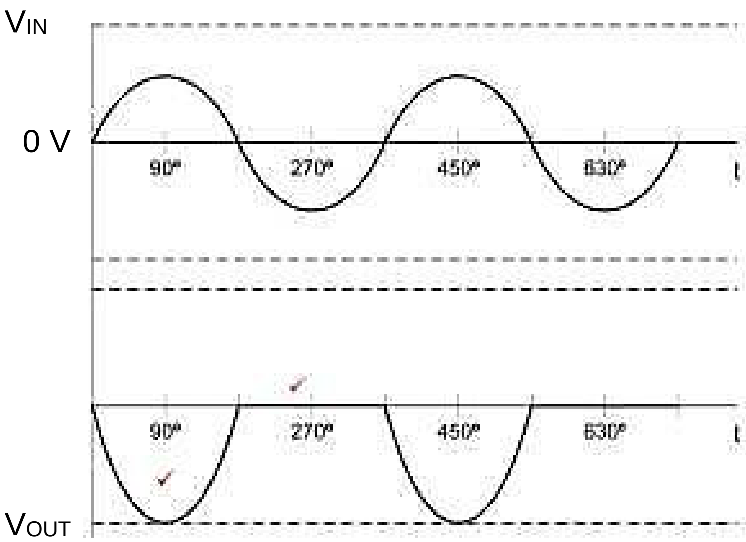
QUESTION 5 AMPLIFIERS

5.1 5.1.1 Q point Class A amplifier – the Q point is in the middle of the DC load line.
Class B amplifier – the Q point is on the cut-off of the DC load line.

NOTA: *If a learner draws the Q point instead of a narrative answer, mark on merit.*

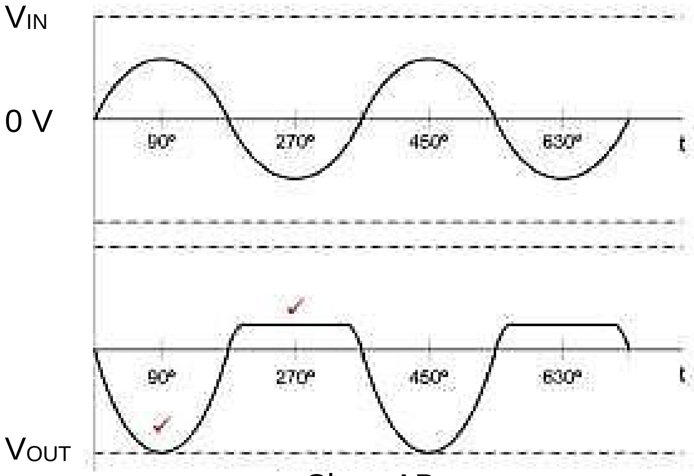
5.1.2
- Efficiency Class A amplifier – it has low efficiency, therefore, it has less output power.
- Class A amplifier – 25%.
- Class B amplifier – it has higher efficiency, therefore, produces more output power.
- Class B amplifier – 50%.

5.2 5.2.1 Class B amplifier



Class B 180º

5.2.2 Class AB amplifier



Class AB
< 180º < 360º

5.3 5.3.1
- C_2 serves as the AC coupling component between the two stages.
- C_2 also blocks or decouples the DC component of the signal.

5.3.2
- When an AC voltage is applied to the input of the first amplifier stage, an alternating current will flow in the collector circuit of transistor (Q_1).
- An alternating voltage will develop across the collector resistor (RC_1).
- The alternating voltage across the R_{C1} will be transferred through capacitor C_2 to the base of the transistor (Q_2) in the amplifier's second stage.
- The proses will be repeated and the amplified output can be measured between C_3 and 0 V.

5.3.3
- Impedance matching
- Correct frequency response
- DC isolation

5.4 5.4.1 Frequency response is the ability of the circuit to respond to a range of frequencies applied to the transistor's input.

5.4.2 Half-power points (–3 dB) is the point when the output is at half the input power.
OR
The half-power point is the point at which the output power has dropped to half of its peak value; that is, at a level of –3 dB.

5.4.3 At lower frequencies the reactances of the decoupling capacitors across the emitter resistors rise. These reactances combine with the resistance of their emitter resistors, causing the total impedance to rise limiting the stage gain.

5.5 5.5.1
- Poor frequency response
- Large and heavy
- Expensive components

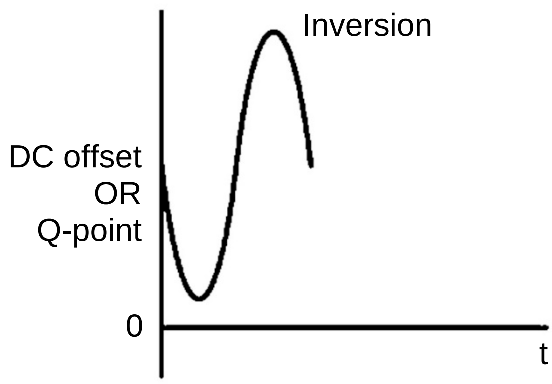
5.5.2 If the loudspeaker is changed to a low-impedance loudspeaker, a matching transformer must be chosen to drive the speaker to ensure maximum power transfer.

5.6 5.6.1 The emitter terminal is common to both the input and the output circuits.

5.6.2 Input signal will be connected between points B and C. The load can be connected between points E and F.

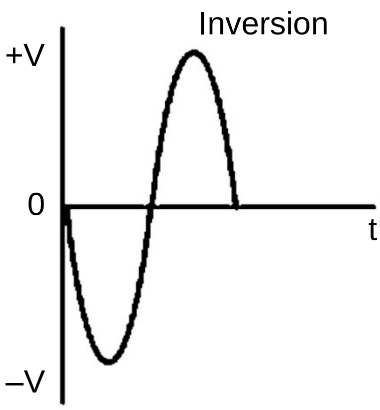
5.6.3 Emitter capacitor (C_3)
Emitter resistor (R_4)

5.6.4



NOTE:
1 mark = phase relationship
2 marks = 1 mark for each amplified half cycle

5.6.5

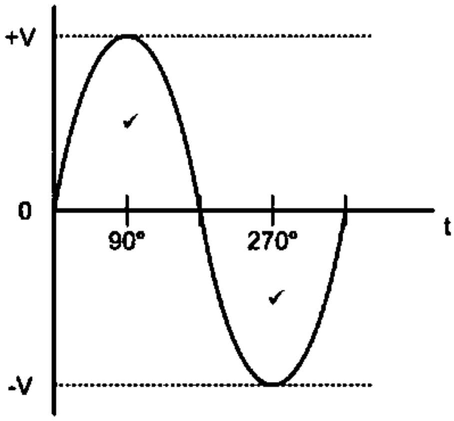


NOTE:
1 mark = phase relationship
2 marks = 1 mark for each amplified half cycle

5.7 5.7.1 Complimentary push-pull pair class AB amplifier

5.7.2 Cross-over distortion can be eliminated by biasing the two transistors Q_1 and Q_2 into class AB mode. This moves the Q-point to each transistor's linear amplification area. Adding a decoupling capacitor on the input will prevent the negative cycle on the input from draining the biasing to earth thus causing distortion. Since the transition response of each transistor overlaps with the others, distortion is eliminated.

5.7.3

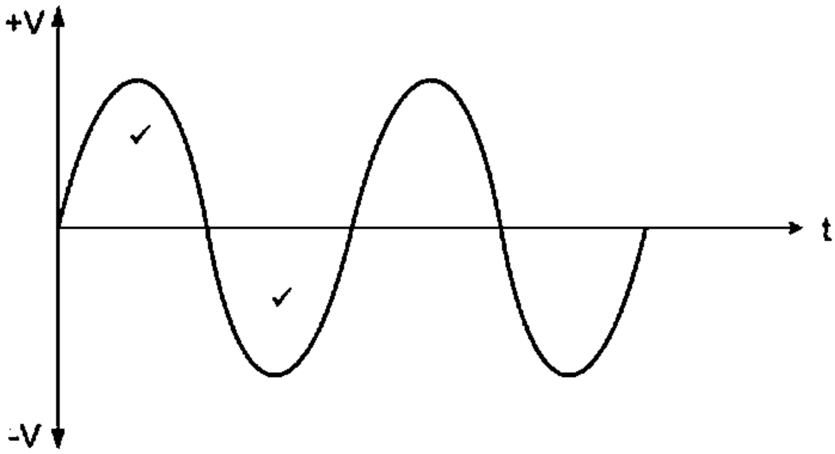


5.7.4 R_1 and R_2 form a voltage divider circuit used to forward bias transistor Q_1.

5.8 5.8.1 The RF coil offers resistance (reactance) against the change in the collector current and causes the collector voltage V_C to decrease.

5.8.2 The tank circuit receives energy from a DC source and converts that energy into a sinusoidal signal at a frequency determined by the inductor and capacitor.

5.8.3



5.8.4
- Hartley oscillator's tank circuit consists of two inductors and one capacitor.
- Colpitts oscillator's tank circuit consists of two capacitors and one inductor.

5.9
- Improving the amplifier's stability.
- Increasing the amplifier's bandwidth.
- Enhancing the amplifier's input and output impedances.
- Reducing or suppressing a noise produced in the amplifier.

Total: 200 marks