CADD LAB EXPERIMENTS LIST

3rd Semester CADD Lab

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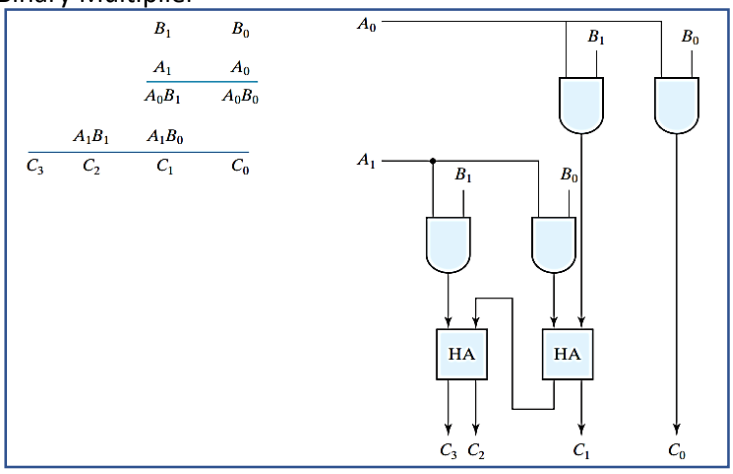
Write the SystemVerilog code for the following Combinational Circuits and implement them on the FPGA Board

1. Full Adder – Dataflow Style
2. Full Adder – Structural Style
3. Full Adder – Using Two Half Adders (Structural Style)
4. Logic Gates (All Gates)
5. 4:1 Mux – Dataflow Style
6. 4:1 Mux using 2:1 Mux (Structural Style)
7. 4:1 Mux Using two level logic (Structural Style)
8. 2 bits wide 4:1 Mux – Dataflow Style
9. Binary to Gray code converter
10. Gary to Binary code converter
11. Binary to Excess 3 code converter
12. 4-bit Ripple Carry Adder
13. 4 to 2 Priority Encoder
14. 8 to 3 Priority Encoder with a valid bit
15. 3 to 8 Decoder
16. 2 to 4 Decoder
17. Write an HDL module for a hexadecimal seven-segment display decoder. The decoder should handle the digits A, B, C, D, E, and F as well as 0–9.
18. Full Adder using 4:1 Mux
19. 2-bit Magnitude Comparator
20. Half Subtractor
21. Full Subtractor
22. Tristate Buffer
23. Binary Multiplier



24. Full Adder with 3 to 8 Decoder
25. BCD Adder
26. Four-bit adder–subtractor (with overflow detection)
27. Four-bit adder with carry lookahead
28. 2:1 Mux using Conditional Operator
29. 1:8 Demultiplexer
30. 4-bit Parallel Subtractor

Write the SystemVerilog code for the following Sequential Circuits and implement them on the FPGA Board

31. D latch, SR Latch – Dataflow Style, Structural Style
32. D FF, SR FF, JK FF, T FF – Dataflow Style, Structural Style, Behavioural Style
33. Tristate Buffer
34. Tristate Inverter
35. FFs with Synchronous reset
36. FFs with Asynchronous reset
37. Enabled FFs and Latches
38. FSM – Non-Overlapping Sequence Detectors – Moore Model
39. FSM – Non-Overlapping Sequence Detectors – Mealy Model
40. FSM – Overlapping Sequence Detectors – Moore Model
41. FSM – Overlapping Sequence Detectors – Mealy Model
42. Synchronous Up – Down Counter
43. Synchronous MOD Counter
44. Ring & Johnson Counter
45. Asynchronous Counter