CUSTOMIZED IC DESIGN USING CADENCE PRO

Description:

Cadence design tools are used in a variety of undergraduate and graduate classes to provide practical experience in the design of integrated circuits and systems. Additionally, they are used by several research groups in the design of chips integrating analog, digital, RF and MEMS circuitry. For the builders of tomorrow, creating the electronic systems that enable smart living will require advanced design technologies on multiple levels—semiconductor, chip packaging, system interconnect, hardware-software integration, system verification, and more. Past approaches to design that address these levels disjointedly are inadequate for the increasing complexity, low-power requirements, and shorter time-to-market challenges that designers face today. Successful companies will thrive by collaborating with ecosystem leaders in electronic design automation, intellectual property, chip fabrication, and other parts of the value chain to create a comprehensive environment for System Design Enablement (SDE). Cadence custom/analog/RF solutions are a key component of the SDE strategy.

DAY 1

- Semi-conductor IC design flow
- Verilog HDL coding for test bench design and RTL design
- Digital design using State machines
- Basic Linux commands
- Directory management
- Tool sourcing

- invocation

DAY 2

- Semi-custom IC design flow
- Digital CMOS circuit design
- Circuit implementation
    1. Schematic entry
    2. Layout
    3. DRC
    4. LVS
    5. RC extraction using Cadence tools

WORKSHOP HIGHLIGHTS

- **Cadence** offers a broad portfolio of tools to help you address an array of challenges and verify your chips, packages, boards, and entire systems.
- In this course, each student defines his/her own design project ranging from digital system integration to low-level circuit techniques. All the projects are implemented using Cadence design tools including Virtuoso, Diva or Calibre DRC/LVS/Extraction and SoC encounter (for Auto Place/Route).
- The designed projects may lead to Fabrication of test chips.