

# Report

Data collected from the simulation

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Direct Map Cache:

File Name	No.of Memory calls	Hit Count	Hit Rate
gcc.trace	515368	483504	0.93759926156
gzip.trace	481044	320883	0.66705540449
mcf.trace	727230	7505	0.01031998129
swim.trace	303193	280738	0.92593826374
twolf.trace	482824	476770	0.98746126953

Set Associative Cache:

File Name	No.of Memory calls	Hit Count	Hit Rate
gcc.trace	515368	483871	0.93831093908
gzip.trace	481044	320883	0.66705540449
mcf.trace	727230	7508	0.01032410654
swim.trace	303193	280825	0.92622520968
twolf.trace	482824	476844	0.98761453448

## Observations

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Even though in most of the cases we found that the hit rate was more than 0.9 in either caches, we can not give any surety on the hit rates. The hit rates varied from 0.01 (for the 'mcf.trace' file) to 0.98 (for the 'twolf.trace' file) for different memory access'. But on average, hit rates are high enough. Therefore the usage of the caches significantly reduces the time required for memory access.

Also, looking at the table, we can clearly find that using the 4-Way Set Associative Cache gives better hit rates by a slight amount in almost all the trace files when compared to a Direct Mapped Cache.

## Instructions to run the code

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Unzip the file and then use the commands

`“ javac IMT2019026_main.java ”`

and

`“ java IMT2019026_main ”`

in the shell/terminal.

## Calculation Part

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The index, tag, byte offset bits of each cache are calculated as follows before the simulation :

Direct Map Cache: Given 4 bytes for each block and a total size of 256KB. Hence there will be (256KB/4) number of lines or indices. I.e  $64 * 1024 = 65536 = 2^{16}$ .

Hence 16 index bits. Now since each block has 4 bytes, we will need 2 byte offset bits. Remaining  $(32 - 16 - 2)$  14 bits are for the tag.

4-way Set Associative Cache: Now divide the above DM cache into 4 parts, which gives us  $2^{16}/4 = 2^{14}$  number of indices for each set. That is 14 bits for index. 2 byte offsets bits. Remaining  $(32 - 14 - 2)$  16 bits are for the tag.

## Note

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All trace files were assigned with a single DM cache and SA cache but the values (tags, valid bits) were reset before the simulation of each trace file.