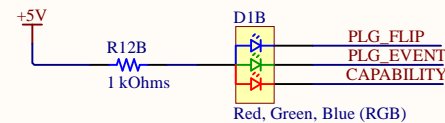
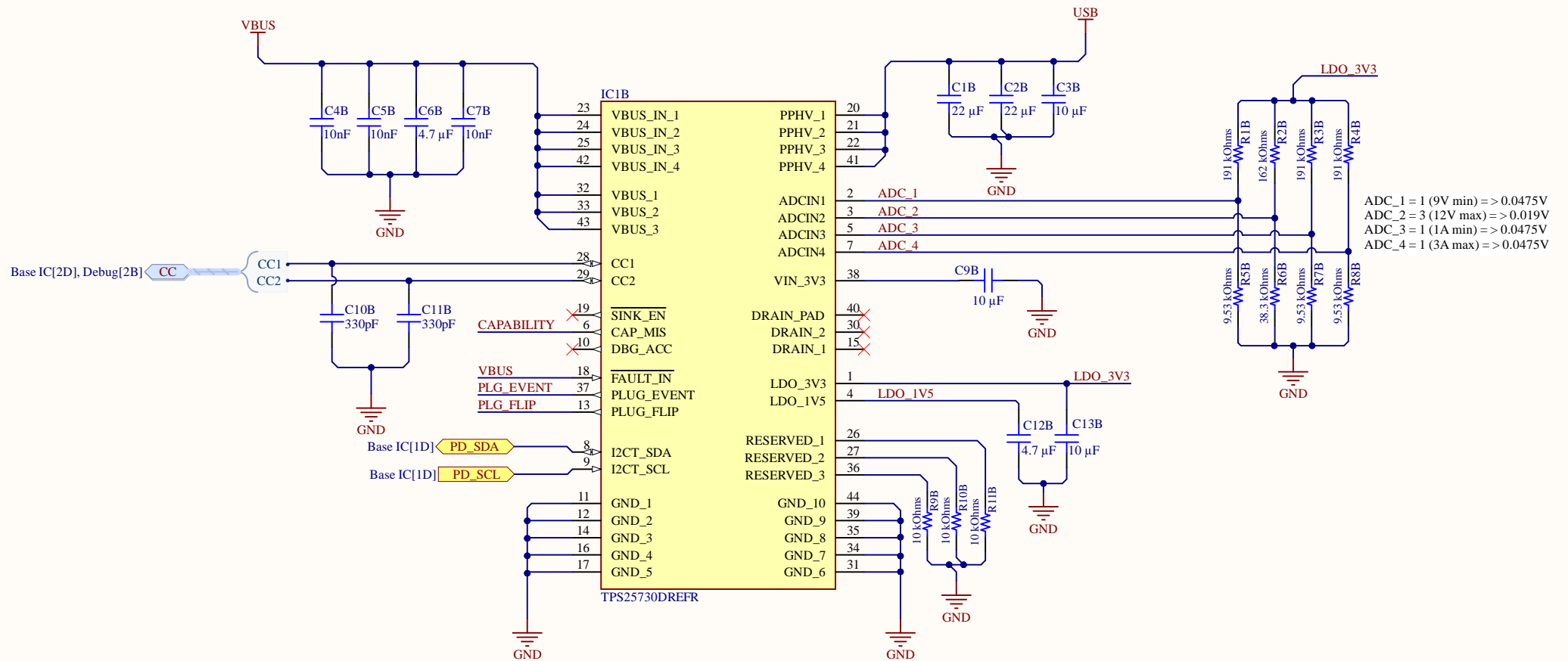



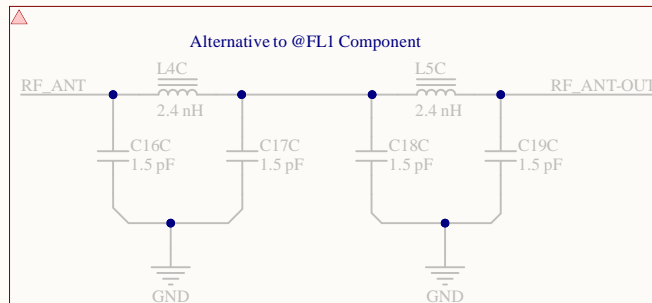
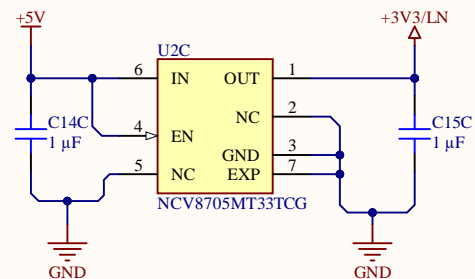
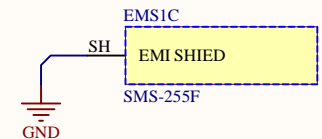
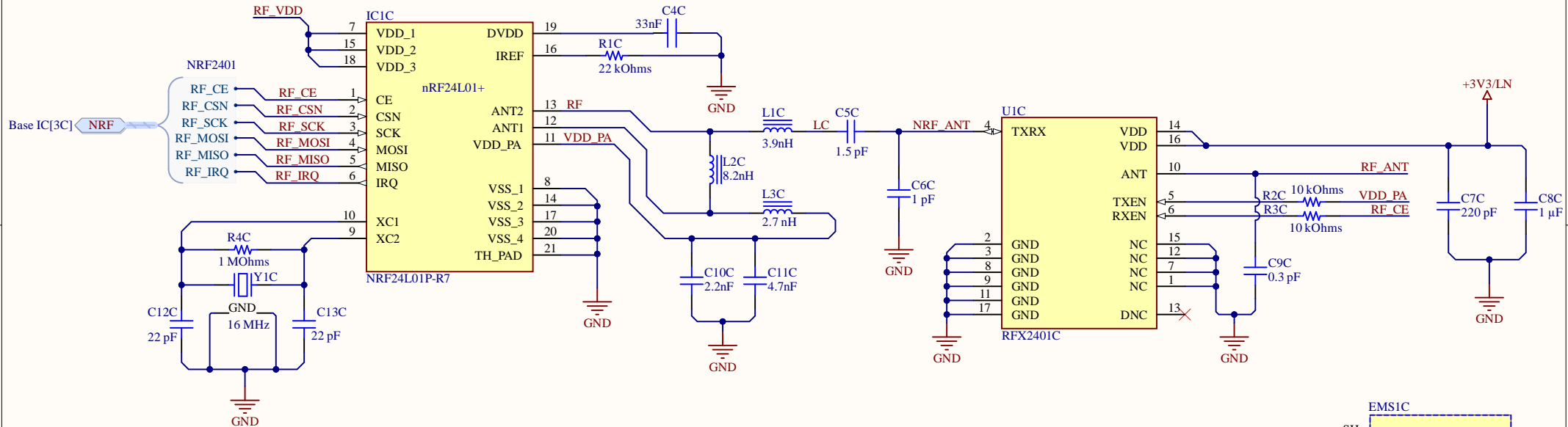
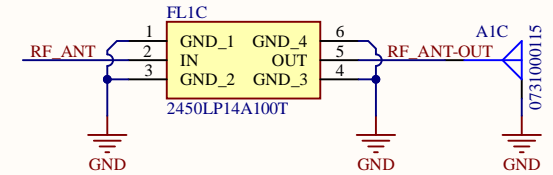
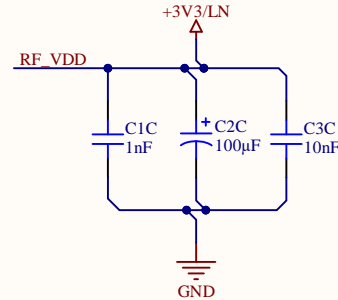
THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR
HEREWITH IS THE PROPERTY OF SPD Ind.



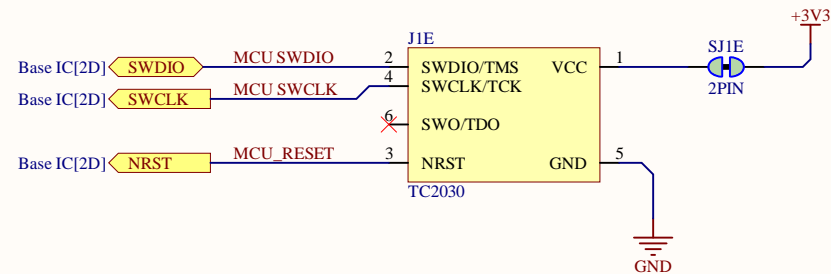
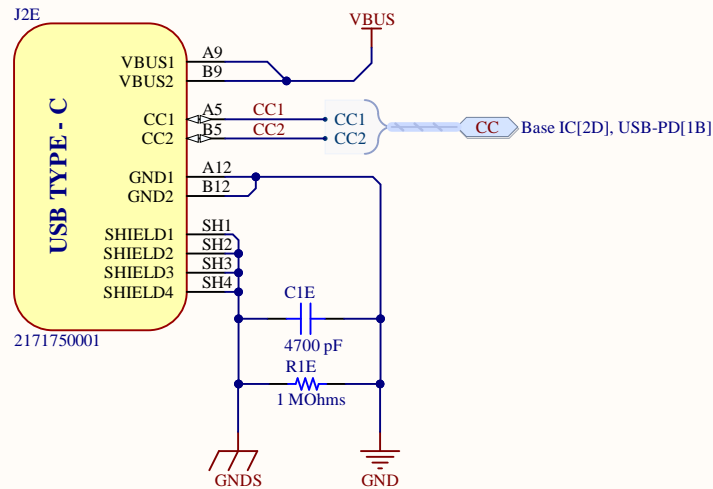
APPROVALS		DATE	PROJECT		 SPD	
ENG: DHARAGESWARAN S		10.03.2024	FluidGuard			
DSN: DHARAGESWARAN S		10.03.2024	PROJECT REVISION: V2.0		DOCUMENT REVISION: V1.3	
CHK: DHARAGESWARAN S		10.03.2024	Email: sdhamuvkl@gmail.com			
REFERENCE DOCUMENTS			TITLE			
			USB-PD CHARGER			
			BOM: #022024031040			
			ASSY DWG: #022024031030			
FAB DWG: #022024031020			SIZE	CAGE CODE	DWG NO.	REV
PCB DWG: #022024031010			A4	#	#022024031001	V2.1
SCALE:			FILE NAME USB-PD.SchDoc			SHEET 2 OF 5


@Y1 Given, $CL = 12 \text{ pF}$
 $CL = (C'1 * C'2) / (C'1 + C'2)$ Here, $C'1 = C1 + C_{pcb} + C_{i1}$ & $C'2 = C2 + C_{pcb} + C_{i2}$
Interisic Capacitance of nRF24L01 was $C_{i1} = C_{i2} = 1 \text{ pF}$
Parasitic Capacitance of FR-4 PCB $\approx 1.5 \text{ pF}$ Approx
And for $C1 = C2, \Rightarrow C^2 - 19C - 60 = 0$ by Quadratic Eq we get $C = 21.75 \mid -5.51$
So, $C \approx 22 \text{ pF}$

Parasitic Capacitance,
 $C' \approx (E_o * E_r * W) / H$ & $C_{pcb} = C' * L$
Here, W, H, L are width, height, length of the PCB trace.
 E_r is Dielectric Constant of FR-4 PCB ≈ 4.5



APPROVALS		DATE	PROJECT	
ENG: DHARAGESWARAN S		10.03.2024	FluidGuard	
DSN: DHARAGESWARAN S		10.03.2024	PROJECT REVISION: V2.0	
CHK: DHARAGESWARAN S		10.03.2024	DOCUMENT REVISION: V1.3	
			Email: sdhamuvkl@gmail.com	
REFERENCE DOCUMENTS			TITLE	
BOM: #022024031040			NRF24L01-TX	
ASSY DWG: #022024031030			SIZE	CAGE CODE
FAB DWG: #022024031020			A4	#
PCB DWG: #022024031010			SCALE:	FILE NAME
				NRF2401.SchDoc
			DWG NO.	REV
			#022024031002	V2.1
			SHEET	3 OF 5



APPROVALS		DATE	PROJECT		 SPD	
ENG: DHARAGESWARAN S		10.03.2024	FluidGuard			
DSN: DHARAGESWARAN S		10.03.2024	PROJECT REVISION: V2.0		DOCUMENT REVISION: V1.3	Email: sdhamuvkl@gmail.com
CHK: DHARAGESWARAN S		10.03.2024	TITLE			
REFERENCE DOCUMENTS			DEBUG PORT			
BOM: #022024031040						
ASSY DWG: #022024031030			SIZE	CAGE CODE	DWG NO.	REV
FAB DWG: #022024031020			A4	#	#022024031004	V2.1
PCB DWG: #022024031010			SCALE:		FILE NAME Debug.SchDoc	SHEET 5 OF 5