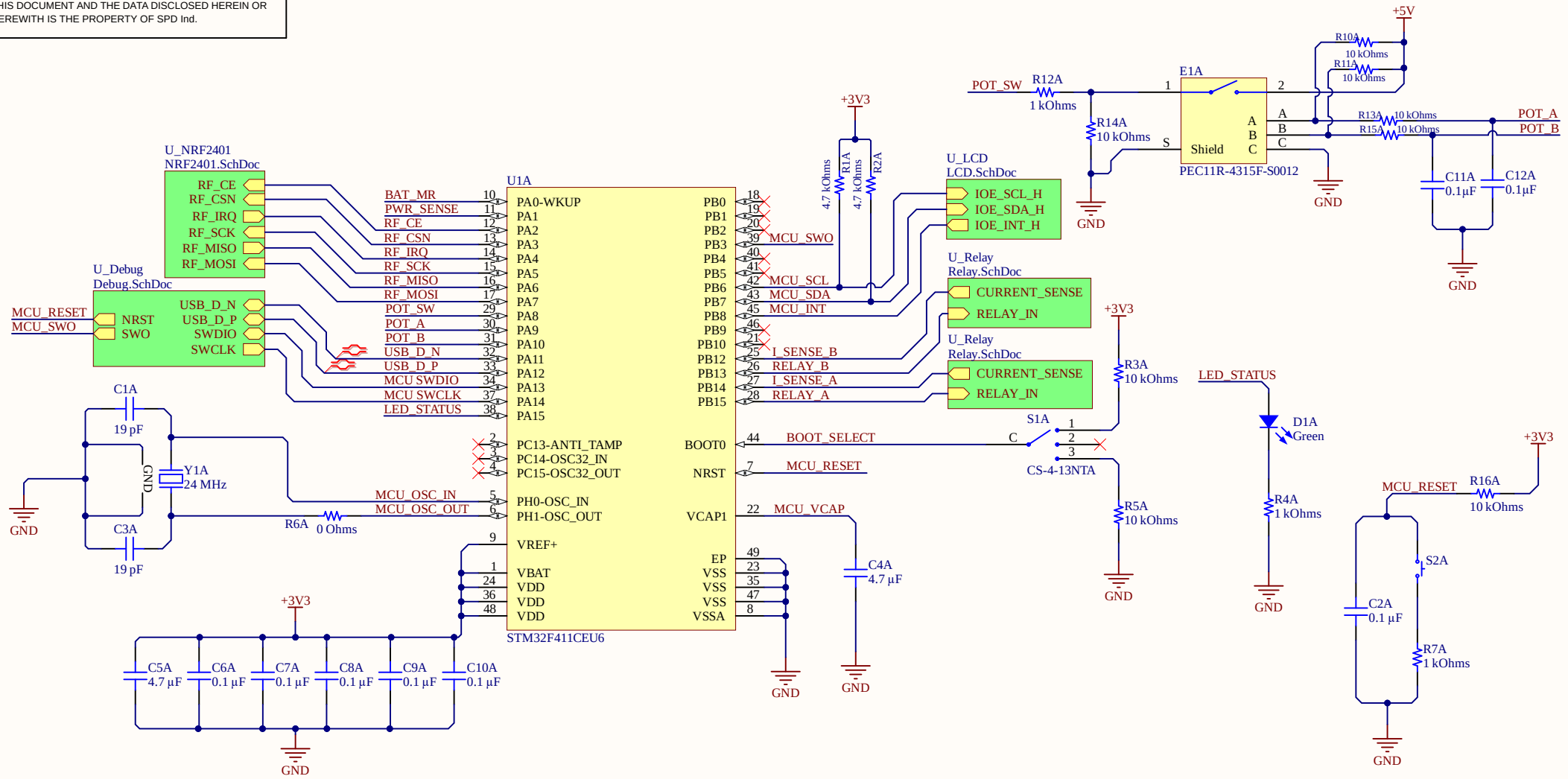


@Y1 Given, CL = 12 pF
CL = (Cl1 * Cl2) / (Cl1 + Cl2) + Cp
Parasitic Capcitance of FR-4 PCB ≈ 2.5pF Approx
And Cl1=Cl2, C ≈ 2*(CL-Cp)
So, C ≈ 19pF

Parasitic Capcitance,
C' ≈ (Eo * Er * W) / H & Cp = C' * L
Here, W, H, L are width, height, lenght of the PCB trace.
Er is Dielectric Constant of FR-4 PCB ≈ 4.5
So, C' ≈ 39.843 pF/m

APPROVALS		DATE
ENG:	DHARAGESWARAN S	15.03.2024
DSN:	DHARAGESWARAN S	15.03.2024
CHK:	DHARAGESWARAN S	15.03.2024

REFERENCE DOCUMENTS	
BOM:	#022024031540
ASSY DWG:	#022024031530
FAB DWG:	#022024031520
PCB DWG:	#022024031510

PROJECT: FluidGuard
PROJECT REVISION: V2.0
DOCUMENT REVISION: V1.2
Email: sdhamuvkl@gmail.com

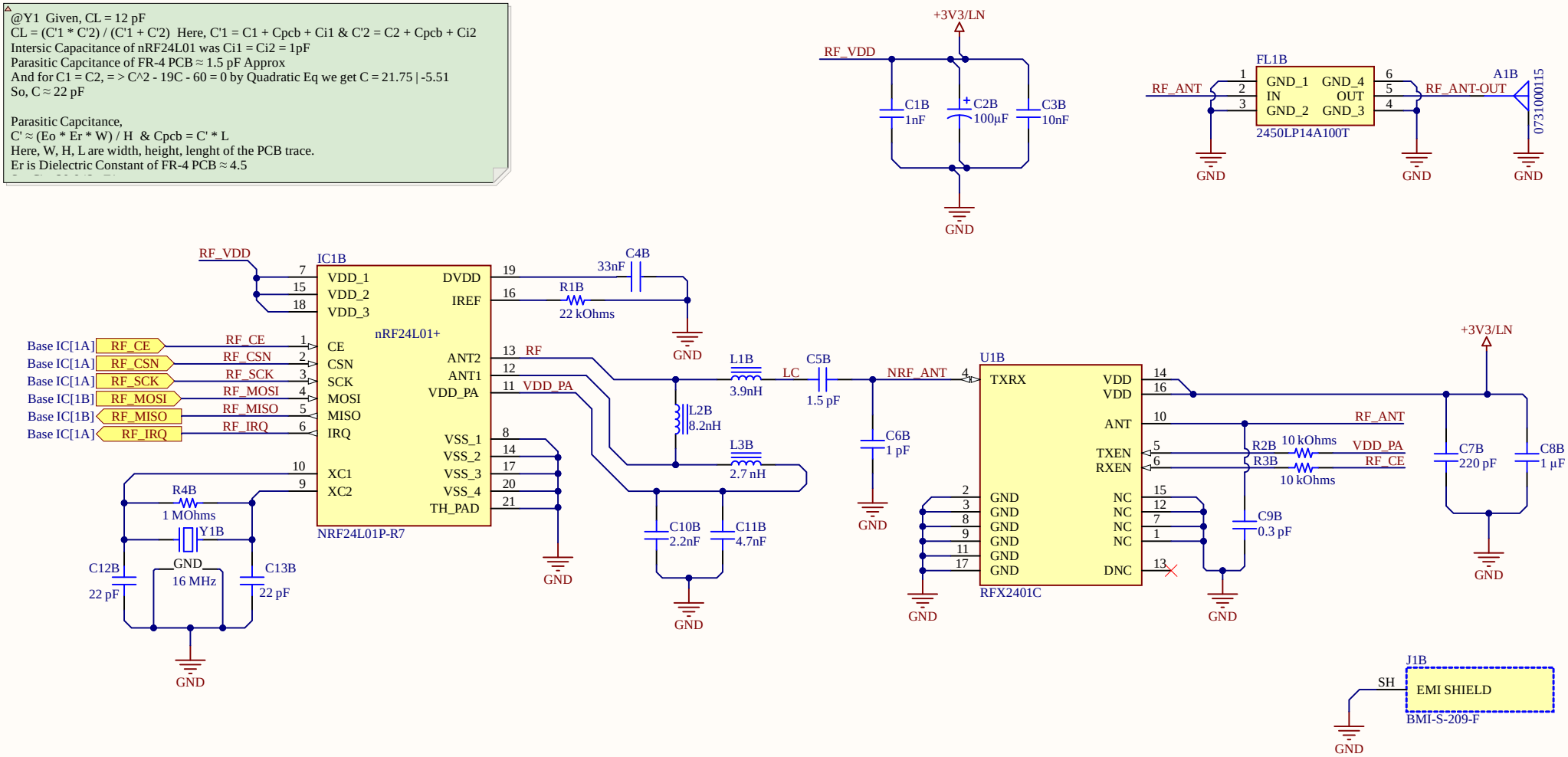
TITLE: FluidGuard(RX)-MCU BLOCK

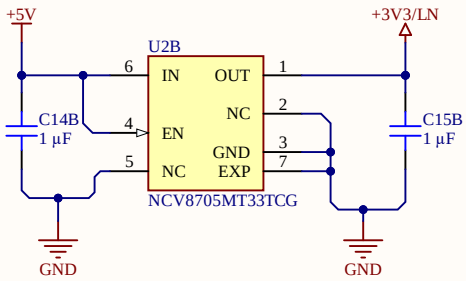
SIZE	CAGE CODE	DWG NO.	REV
A4	#	#022024031500	V2.1

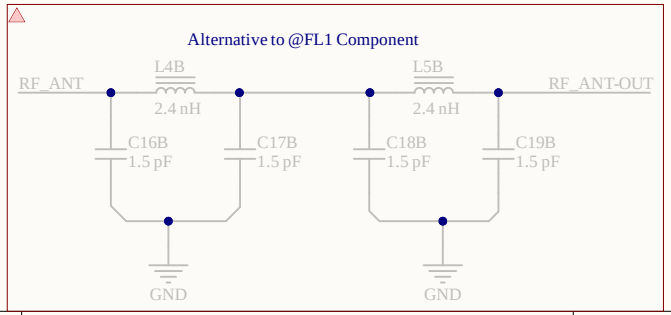
SCALE: | FILE NAME Base IC.SchDoc | SHEET 1 OF 7

@Y1 Given, CL = 12 pF
CL = (C'1 * C'2) / (C'1 + C'2) Here, C'1 = C1 + Cpcb + Ci1 & C'2 = C2 + Cpcb + Ci2
Intersic Capacitance of nRF24L01 was Ci1 = Ci2 = 1pF
Parasitic Capcitance of FR-4 PCB ≈ 1.5 pF Approx
And for C1 = C2, = > C^2 - 19C - 60 = 0 by Quadratic Eq we get C = 21.75 | -5.51
So, C ≈ 22 pF

Parasitic Capcitance,
C' ≈ (Eo * Er * W) / H & Cpcb = C' * L
Here, W, H, L are width, height, lenght of the PCB trace.
Er is Dielectric Constant of FR-4 PCB ≈ 4.5







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BOM:	#022024031540
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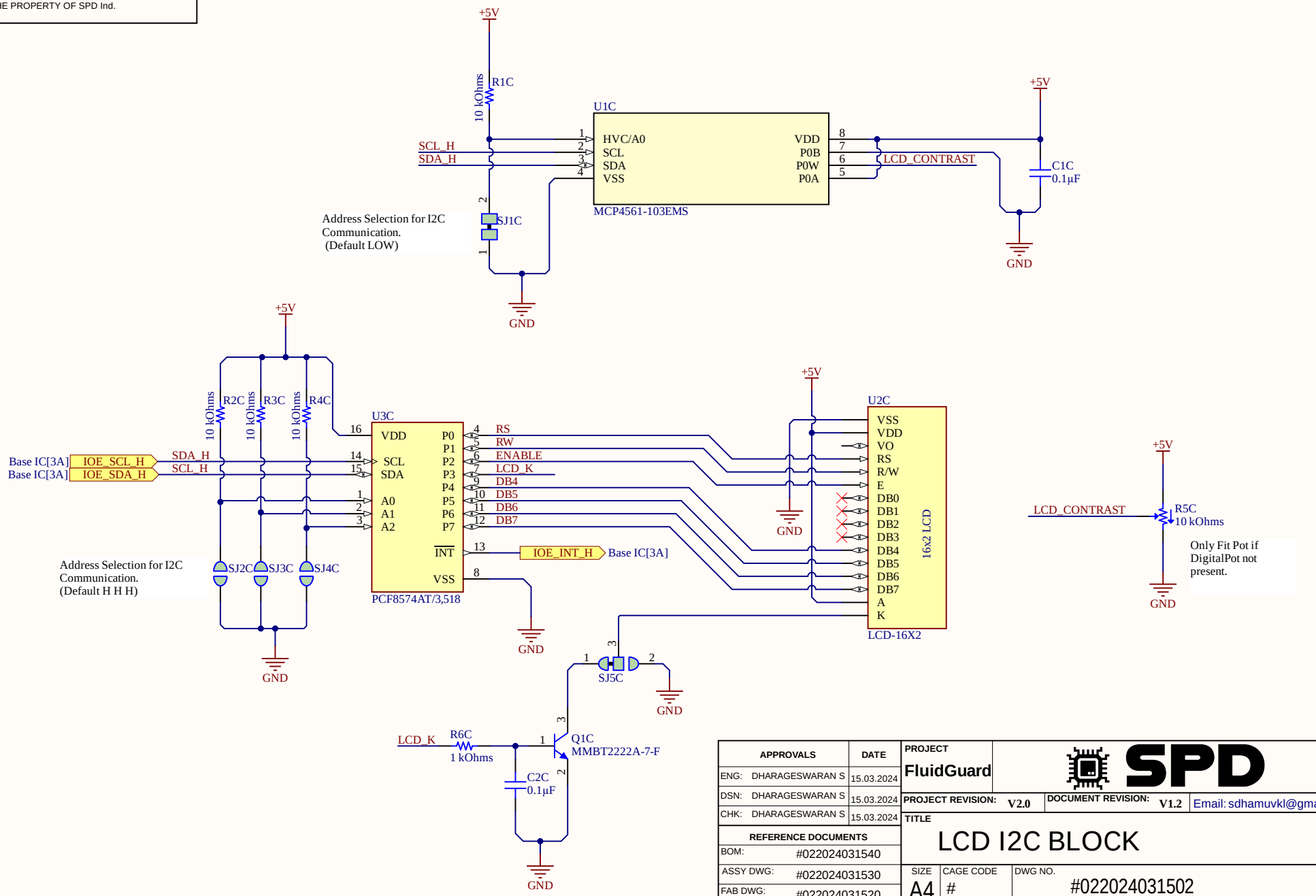
FAB DWG:	#022024031520
PCB DWG:	#022024031510

PROJECT: FluidGuard
PROJECT REVISION: V2.0
DOCUMENT REVISION: V1.2
Email: sdhamuvkl@gmail.com
TITLE: NRF24L01-RX
SIZE: A4
CAGE CODE: #
DWG NO.: #022024031501
REV: V2.1
SCALE:
FILE NAME: NRF2401.SchDoc
SHEET: 2 OF 7



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CHK:	DHARAGESWARAN S	15.03.2024

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FAB DWG:	#022024031520
PCB DWG:	#022024031510

PROJECT: FluidGuard

SPD

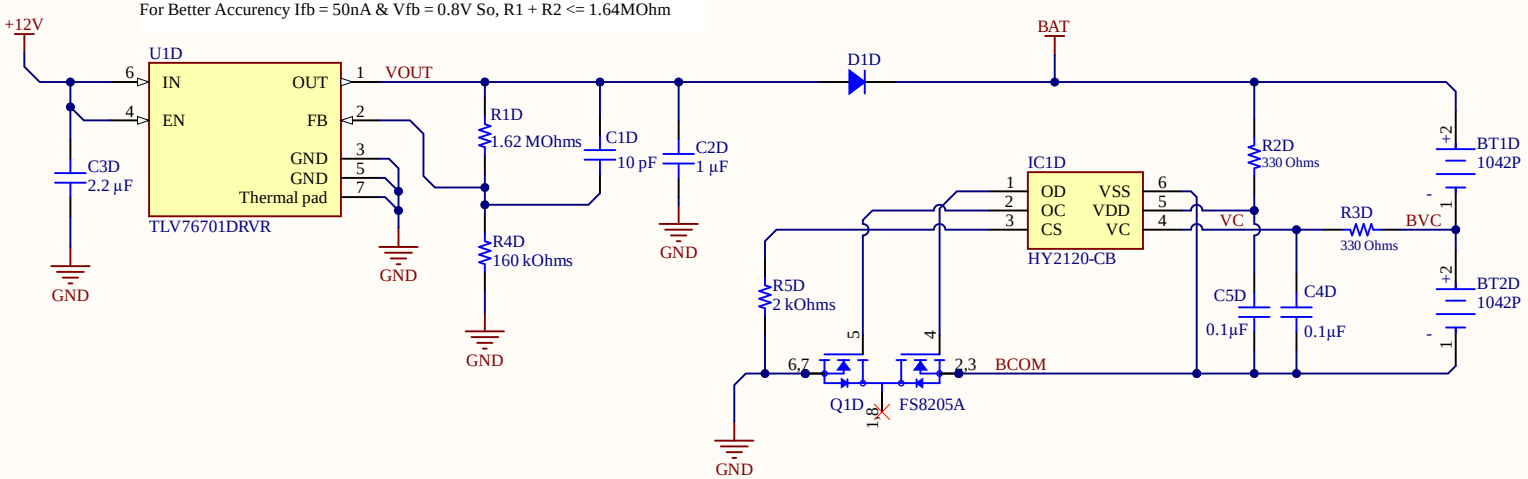
PROJECT REVISION: V2.0 | DOCUMENT REVISION: V1.2 | Email: sdhamuvkl@gmail.com

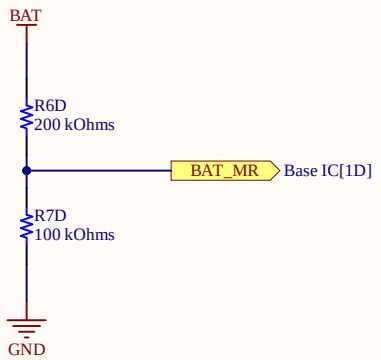
TITLE: LCD I2C BLOCK

SIZE	CAGE CODE	DWG NO.	REV
A4	#	#022024031502	V2.1

SCALE: | FILE NAME LCD.SchDoc | SHEET 3 OF 7

R1 + R2 <= Vout/(Ifb*100)
Vout = Vfb(1+R1/R2)
For Better Accurency Ifb = 50nA & Vfb = 0.8V So, R1 + R2 <= 1.64MOhm





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CHK:	DHARAGESWARAN S	15.03.2024

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FAB DWG:	#022024031520
PCB DWG:	#022024031510

PROJECT: FluidGuard

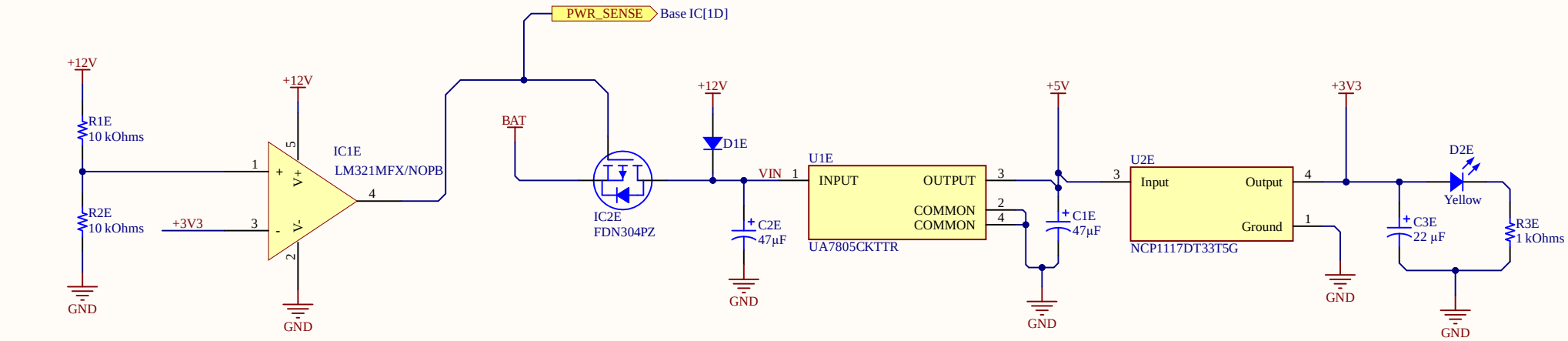
PROJECT REVISION: V2.0 | DOCUMENT REVISION: V1.2

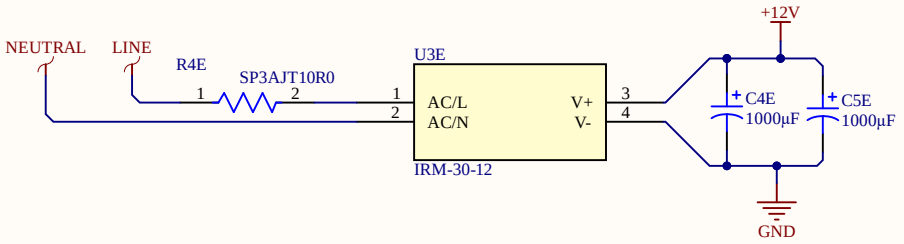
Email: sdhamuvkl@gmail.com

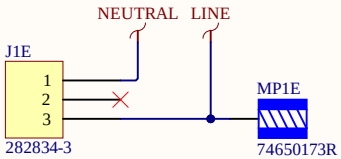
TITLE: BMS BLOCK

SIZE	CAGE CODE	DWG NO.	REV
A4	#	#022024031503	V2.1

SCALE: | FILE NAME: BMS.SchDoc | SHEET: 4 OF 7







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FAB DWG:	#022024031520
PCB DWG:	#022024031510

PROJECT: FluidGuard

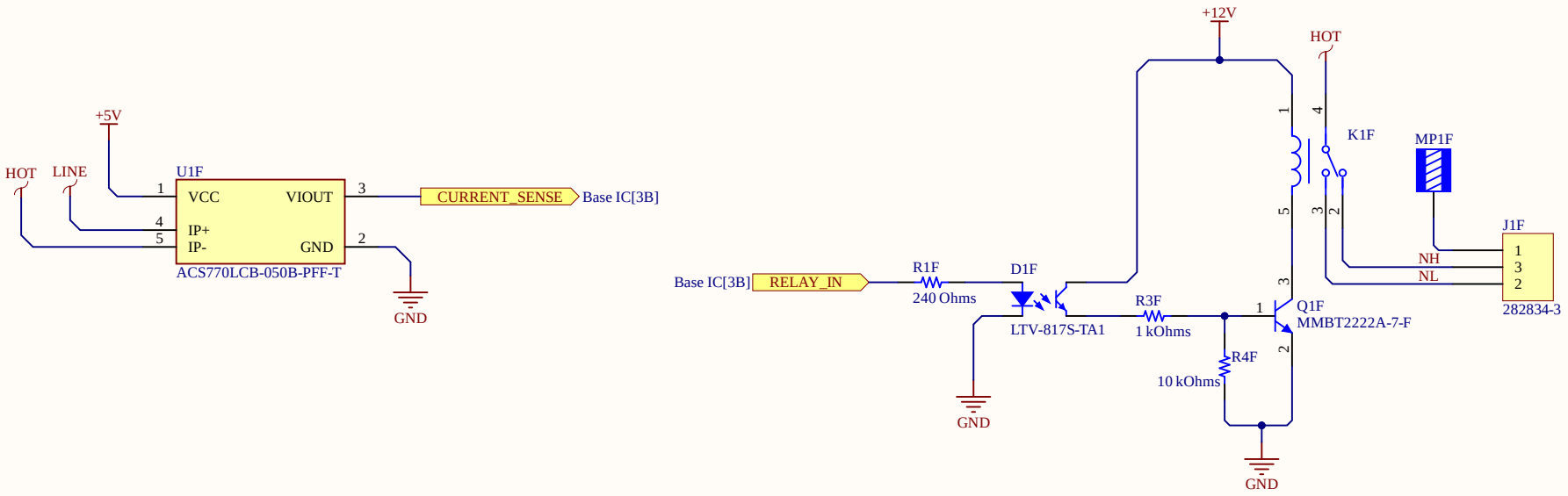
SPD

PROJECT REVISION: V2.0 | DOCUMENT REVISION: V1.2 | Email: sdhamuvkl@gmail.com

TITLE: POWER BLOCK

SIZE	CAGE CODE	DWG NO.	REV
A4	#	#022024031504	V2.1

SCALE: | FILE NAME PowerSwitch.SchDoc | SHEET 5 OF 7



APPROVALS		DATE
ENG:	DHARAGESWARAN S	15.03.2024
DSN:	DHARAGESWARAN S	15.03.2024
CHK:	DHARAGESWARAN S	15.03.2024

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BOM:	#022024031540
ASSY DWG:	#022024031530
FAB DWG:	#022024031520
PCB DWG:	#022024031510

PROJECT: FluidGuard

SPD

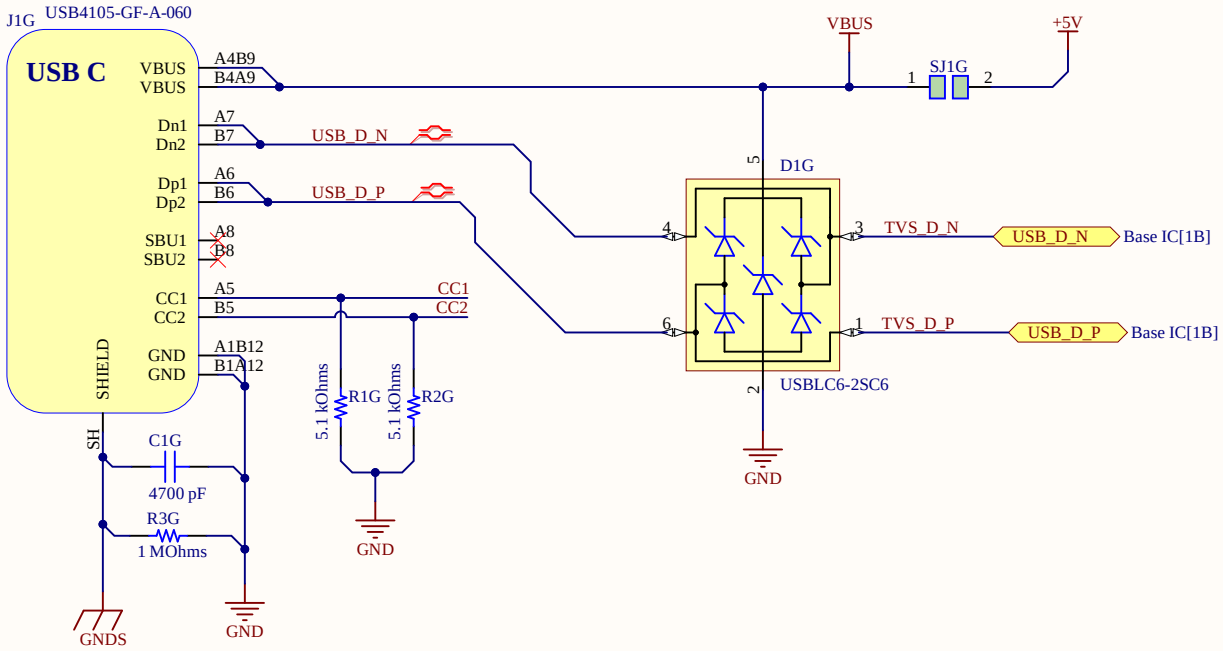
PROJECT REVISION: V2.0 | DOCUMENT REVISION: V1.2 | Email: sdhamuvkl@gmail.com

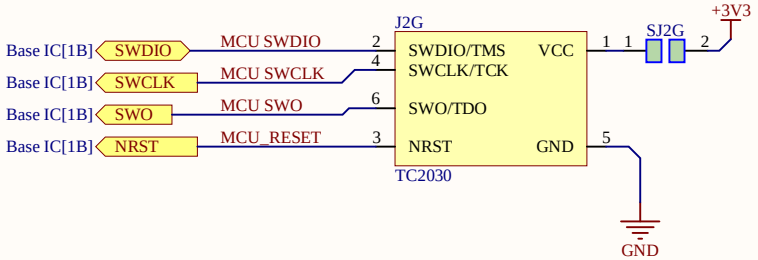
TITLE

LOAD SWITCH & SENSE

SIZE	CAGE CODE	DWG NO.	REV
A4	#	#022024031505	V2.1

SCALE: | FILE NAME Relay.SchDoc | SHEET 6 OF 7





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ENG:	DHARAGESWARAN S	15.03.2024
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CHK:	DHARAGESWARAN S	15.03.2024

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BOM:	#022024031540
ASSY DWG:	#022024031530
FAB DWG:	#022024031520
PCB DWG:	#022024031510

PROJECT: FluidGuard

PROJECT REVISION: V2.0

DOCUMENT REVISION: V1.2

Email: sdhamuvkl@gmail.com

TITLE: DEBUG PORTS

SIZE	CAGE CODE	DWG NO.	REV
A4	#	#022024031506	V2.1

SCALE:

FILE NAME: Debug.SchDoc

SHEET: 7 OF 7