# Assignment 7

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This  Assignment involves designing and implementing a serial asynchronous Receiver.

## Design

The input clock has 100Mhz and the baud rate is 9600, so make a new clock with a frequency of (100 / (9600*16 ) = 325.
The Receiver has four states Idle_State, Start_State, Serial_State, and Stop_State .initially, the Receiver will be in the Idle_State state.
In Idle_State when the receiver receives zero it will go to Start_State.
In Start_State, it will count 6 times and then read start bit and go in Serial_State.
In Serial_State, it will read 8bits, it will first count 16 times and then read a bit and after reading all 8 bits it will go in Stop_State.
In Stop_State, it will count 16 times and read stop bit and go to Idle_State.
One Button was also added to make output zero.

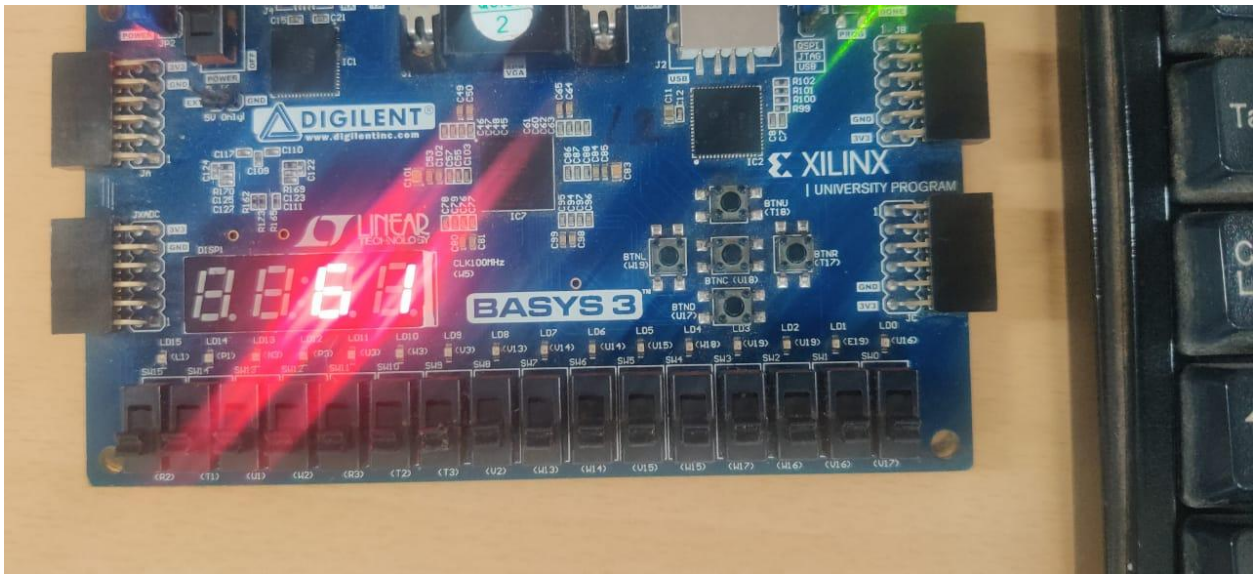
## CIRCUIT

This circuit has to connect to gtkterm and then when we write a character on gtkterm its Ascii value will be shown in seven segment display.
When the button will be pressed it will make 0 on seven segment display.

# Photo of Gtkterm


# Photo of FPGAS

For input for Ascii value of ‘a’



# 1. Slice Logic

| Site Type | Used | Fixed | Available | Util% |
|---|---|---|---|---|
| Slice LUTs* | 104 | 0 | 20800 | 0.50 |
| LUT as Logic | 104 | 0 | 20800 | 0.50 |
| LUT as Memory | 0 | 0 | 9600 | 0.00 |
| Slice Registers | 71 | 0 | 41600 | 0.17 |
| Register as Flip Flop | 71 | 0 | 41600 | 0.17 |
| Register as Latch | 0 | 0 | 41600 | 0.00 |
| F7 Muxes | 0 | 0 | 16300 | 0.00 |
| F8 Muxes | 0 | 0 | 8150 | 0.00 |

# 2. Memory

| Site Type | Used | Fixed | Available | Util% |
|---|---|---|---|---|
| Block RAM Tile | 0 | 0 | 50 | 0.00 |
| RAMB36/FIFO* | 0 | 0 | 50 | 0.00 |
| RAMB18 | 0 | 0 | 100 | 0.00 |

# 3. DSP

| Site Type | Used | Fixed | Available | Util% |
|---|---|---|---|---|
| DSPs | 0 | 0 | 90 | 0.00 |

## 4. IO and GT Specific

| Site Type | Used | Fixed | Available | Util% |
|---|---|---|---|---|
| Bonded IOB | 14 | 0 | 106 | 13.21 |
| Bonded IPADs | 0 | 0 | 10 | 0.00 |
| Bonded OPADs | 0 | 0 | 4 | 0.00 |
| PHY_CONTROL | 0 | 0 | 5 | 0.00 |
| PHASER_REF | 0 | 0 | 5 | 0.00 |
| OUT_FIFO | 0 | 0 | 20 | 0.00 |
| IN_FIFO | 0 | 0 | 20 | 0.00 |
| IDELAYCTRL | 0 | 0 | 5 | 0.00 |
| IBUFDS | 0 | 0 | 104 | 0.00 |
| GTPE2_CHANNEL | 0 | 0 | 2 | 0.00 |
| PHASER_OUT/PHASER_OUT_PHY | 0 | 0 | 20 | 0.00 |
| PHASER_IN/PHASER_IN_PHY | 0 | 0 | 20 | 0.00 |
| IDELAYE2/IDELAYE2_FINEDELAY | 0 | 0 | 250 | 0.00 |
| IBUFDS_GTE2 | 0 | 0 | 2 | 0.00 |
| ILOGIC | 0 | 0 | 106 | 0.00 |
| OLOGIC | 0 | 0 | 106 | 0.00 |

## 5. Clocking

| Site Type | Used | Fixed | Available | Util% |
|---|---|---|---|---|
| BUFGCTRL | 1 | 0 | 32 | 3.13 |
| BUFIO | 0 | 0 | 20 | 0.00 |
| MMCME2_ADV | 0 | 0 | 5 | 0.00 |
| PLLE2_ADV | 0 | 0 | 5 | 0.00 |
| BUFMRCE | 0 | 0 | 10 | 0.00 |
| BUFHCE | 0 | 0 | 72 | 0.00 |
| BUFR | 0 | 0 | 20 | 0.00 |

## 6. Specific Feature

| Site Type | Used | Fixed | Available | Util% |
|---|---|---|---|---|
| BSCANE2 | 0 | 0 | 4 | 0.00 |
| CAPTUREE2 | 0 | 0 | 1 | 0.00 |
| DNA_PORT | 0 | 0 | 1 | 0.00 |
| EFUSE_USR | 0 | 0 | 1 | 0.00 |
| FRAME_ECCE2 | 0 | 0 | 1 | 0.00 |
| ICAPE2 | 0 | 0 | 2 | 0.00 |
| PCIE_2_1 | 0 | 0 | 1 | 0.00 |
| STARTUPE2 | 0 | 0 | 1 | 0.00 |
| XADC | 0 | 0 | 1 | 0.00 |

## 7. Primitives

| Ref Name | Used | Functional Category |
|---|---|---|
| FDRE | 71 | Flop & Latch |
| LUT1 | 51 | LUT |
| LUT6 | 25 | LUT |
| LUT4 | 16 | LUT |
| CARRY4 | 13 | CarryLogic |
| OBUF | 11 | IO |
| LUT3 | 10 | LUT |
| LUT5 | 5 | LUT |
| LUT2 | 5 | LUT |
| IBUF | 3 | IO |
| BUFG | 1 | Clock |