Assignment 1

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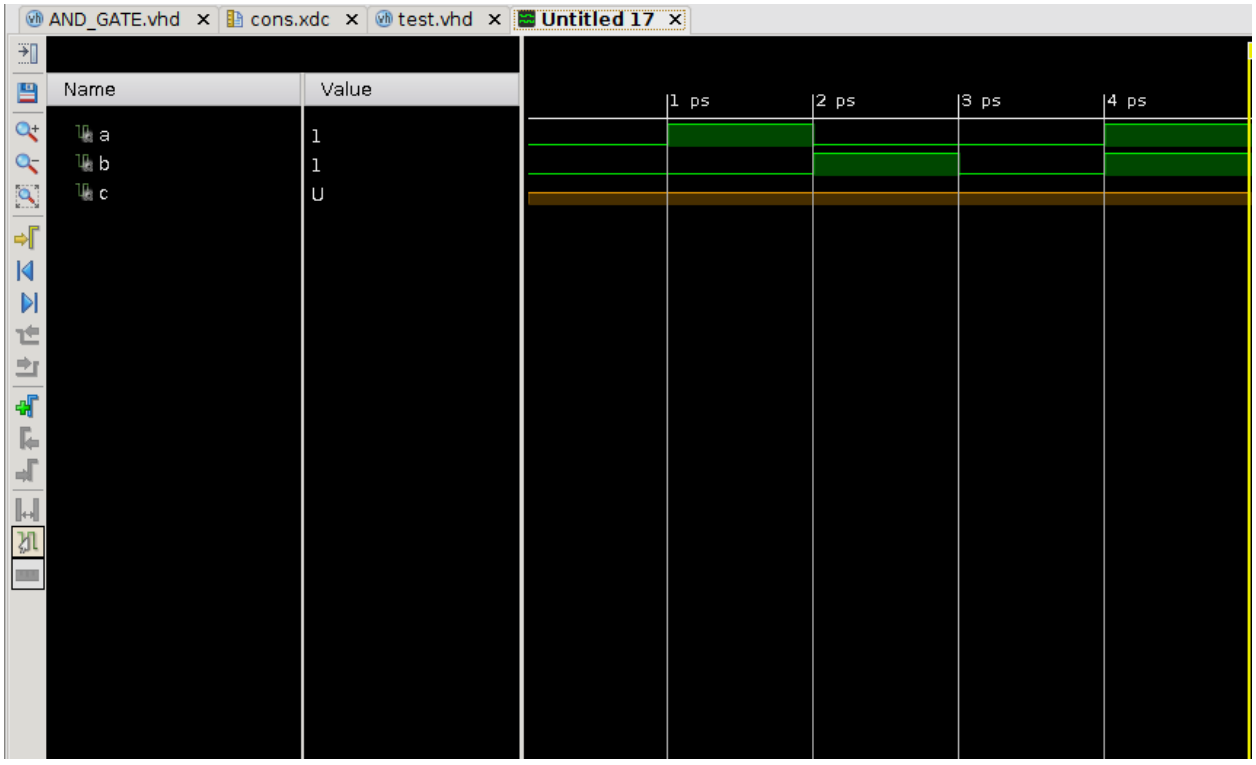
Steps of to make “And” Gate in Vivado are following:

1. Create a Vhdl file in “design Sources” and write vhdl of “And” gate.
2. Create a Xdc file in “Constraints” and write Constraint of “And” gate.
3. Create a Vhdl file in “Utility Sources” and write testbatch of of “And” gate.
4. Run Simulation and check if it is fine.

screenshots of our simulations



5. Run Synthesis and check if it is fine.
6. To get bit file press on genterate generate bitstream.
7. Press on Hardware Manager and click program Device and check in fpga that “And” Gate is working fine.

Resource	Count
Flipflops	0
LUTs	1
BRAMs	0
DSPs	0

Photo of FPGA: