Low Power Current-reused Voltage-Controlled Oscillator with Optimum Source Damping Resistors

Chien-Hsuan Liu, Chia-Yo Chan, Ruey-Lue Wang, and Yun-Kuin Su

Abstract **– In this paper, a low power current-reused voltage-controlled oscillator with source damping resistors is presented. It is designed by simulating optimum value of resistors. According to the simulation results, the output signals are symmetric and the $1/f^3$ region of the phase noise is reduced. The VCO_1 is designed at 2.26 GHz. The measured phase noise at 100-kHz and 1-MHz offset frequencies are -101.87 and -121.66 dBc/Hz. With 1.8V voltage supply, the power consumptions of the VCO is 1.62 mW. This circuit is fabricated by TSMC 0.18 um CMOS process.**

I. Introduction

In recent years, the great improvement of wireless communication technology has promoted a lot of studies on the design of ratio frequency circuits. The current trend of ratio frequency circuits is toward low power consumption and small chip area that could reduce the cost of chip.

With the decrease of gate channel length of the transistor, the $1/f$ noise of the transistor increases. Because the $1/f$ noise is the most significant part of the $1/f^3$ corner of the phase noise of VCO, the $1/f^3$ region of the phase noise also increases with the increase of the $1/f$ noise.

In order to achieve low power consumption, the current-reused VCO structure is chosen [1]. But in the current-reused configuration, the voltage swings in each output terminal are asymmetric. In this design, the phase difference of two voltage swings is simulated with varied source damping resistors. By finding available values of resistors, this technique will make differential voltage swing symmetric.

Besides the symmetry of output, the phase noise will also be influenced by the source damping resistors. The degeneration resistance can suppress the $1/f$ noise current. In order to lower the phase noise at $1/f^3$ region, the optimum value of the resistors must be used. Firstly, the range of resistances with symmetric differential voltage swing can be found by simulation. And then an optimum value for the lowest phase noise can be found in this range. This technique is so-called as source damping topology [2]. In this paper, we design a current-reused VCO by analyzing the influence of damping resistances on the phase error of differential outputs and phase noise.

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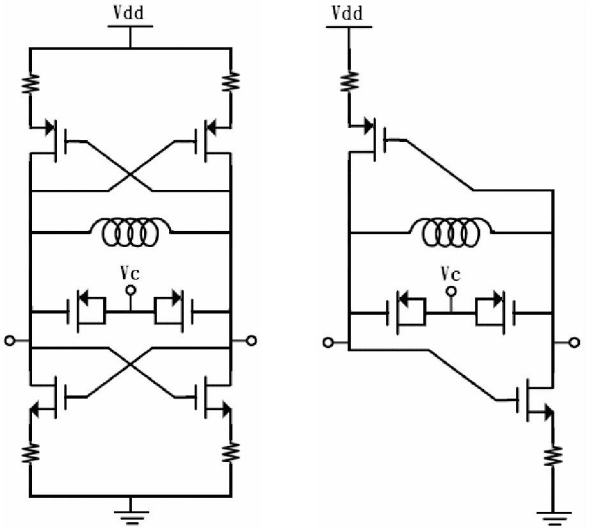


Fig. 1 (a) CMOS complementary VCO with source damping resistors and (b) current-reused VCO with source damping resistors

II. VCO Design

Fig.1 (a) shows a conventional CMOS complementary VCO with source damping resistors. Only the half circuit of the CMOS complementary VCO is used in this work, as shown in Fig. 1 (b). It is so-called as current-reused configuration. Because there is only one current flow in the current-reused VCO, the power consumption could be reduced sufficiently compared with conventional CMOS complementary VCO. Besides, the size of chip will also be reduced.

A. Symmetric Output Signals with Source Damping Resistors

If there are not source damping resistors in the current-reused VCO, the oscillation signals at two sides are

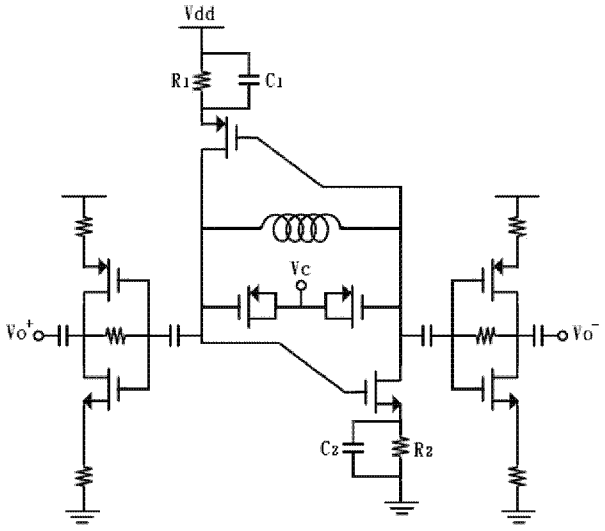


Fig. 2 Complete current-reused VCO

asymmetric because of two different switching transistors, P- and N-MOSFETs. For a transistor with channel width of W, length of L, and drain current of I_D, g_m can be given as

$$g_m = \sqrt{2\mu C_{ox}\frac{W}{L}I_D} \tag{1}$$

where μ is the carrier mobility of transistors. Because μ of PMOS is less than that of NMOS, PMOS has smaller transconductance. In the current-reused VCO, the P-MOSFET and N-MOSFET switch at the same time. The oscillator will operate in a voltage-limited region, so the voltage swing of differential outputs is different in amplitude and phase. These asymmetries are made by differences of g_m and parasitic capacitances of the P- and N-MOSFETs. Therefore the current-reused VCO without source damping resistors is not suitable to generate symmetric differential voltage swing.

Fig. 2 shows a complete current-reused VCO with source damping resistors and the inverters are used as buffers. These two source damping resistors R_1 and R_2 are used to control the DC current and let the VCO operate in a current-limited region [1]. In current-limited region, the voltage swing is controlled by DC current which is influenced by R_1 and R_2. Observing the simulation results, the differential outputs swing symmetrically at some certain ratios of R_1/R_2.

Fig. 3 shows the simulated plot of differential phase difference versus R_2. The optimum value of R_2 is 50Ω. Fig. 4 shows the simulated phase difference of two voltage swings versus R_1. Suitable values of R_1 can make phase difference approximate to 180°. The phase difference is smaller than 1.4° for the specified resistance values. It means the two voltage swings are reasonably symmetric.

From Fig. 3 and 4, the proper values of R_1 and R_2 which can make the differential voltage swing symmetric are from 630Ω to 800Ω and from 49Ω to 80Ω, respectively.

B. Reduced Phase Noise with Source Damping Resistors

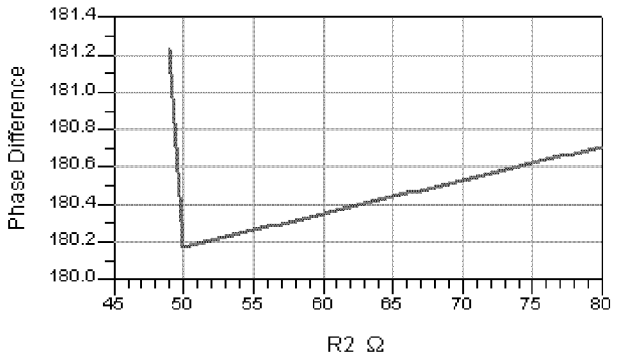


Fig. 3 Simulated phase difference of two voltage swings versus R_2

With the decrease of gate channel length of the transistor, the $1/f$ noise of the transistor is increasing. The $1/f$ noise is given by equation (2)

$$\overline{V_{n,1/f}^2} = \frac{K}{C_{ox}WL}\frac{1}{f} \tag{2}$$

From [3], the $1/f^3$ corner of the phase noise can be given

$$\omega_{1/f^3} \approx \omega_{1/f}\cdot\left(\frac{C_0}{C_1}\right)^2 = \frac{K}{C_{ox}WL}\cdot\frac{g_m^2}{\gamma\cdot g_{d0}}\cdot\frac{1}{4kT}\cdot\left(\frac{C_0}{C_1}\right)^2 \tag{3}$$

where $\omega_{1/f}$ is the corner of the transistor $1/f$ noise and C_0 and C_1 represent first and second Fourier series coefficient of the impulse sensitivity function (ISF). From equation (3), when gate channel length decreases, the corner of the transistor and the $1/f^3$ corner of the phase noise will increase. In order to decrease the $1/f^3$ corner of the phase noise spectrum, g_m should be reduced during the oscillation. The method of decreasing g_m used in this work is source damping topology [2]. Source damping resistor means a resistor in series with the source of the transistor and works as damping factor during oscillation. The overall transconductance of transistor, Gm versus gate voltage is given by

$$G_m = \frac{g_m}{1+g_m R_s} \tag{4}$$

where R_s is the resistance of source damping resistor. The G_m is equal to g_m of the transistor at little gate voltage. When the gate voltage becomes larger, G_m is close to $1/R_s$. By using the source damping resistors, the variation of G_m is reduced during the oscillation. Therefore the $1/f^3$ region of the phase noise is reduced.

In the part A, the useful range of values of R_1 and R_2 to make the differential outputs swing symmetrically are found. Using these values, the $1/f^3$ region and $1/f^2$ region of the phase noise are simulated. The phase noise at 100k-Hz offset frequency versus R_1 with the fixed R_2 of 50Ω is shown in Fig. 4. According to the simulated result, the optimum value of R_1 can be chosen in order to make the $1/f^3$ region of the phase noise lowest. The increase of $1/f^3$ region of the phase noise at larger R_1 is due to the

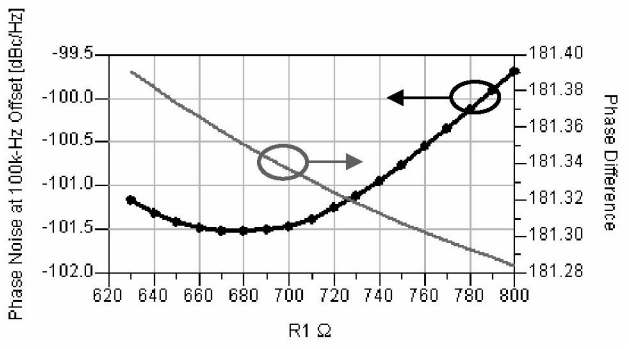


Fig. 4 Simulated phase noise at 100k-Hz offset and phase difference versus R_1

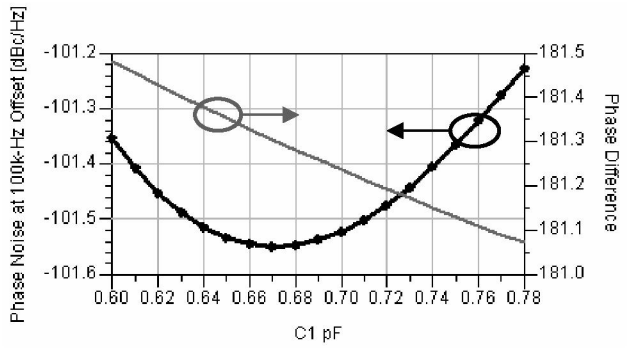


Fig. 5 Simulated phase noise at 100k-Hz offset and phase difference versus C_1

decrease of the voltage swing and the increase of the thermal noise in R_1.

C. Bypass Capacitors Paralleled with Resistors

In Fig. 2, C_1 and C_2 are bypass capacitors in parallel with the damping resistors in order to reduce the phase noise at high frequencies. The capacitance can not only compensate the parasitic but also bypass the thermal noise of the resistor which can improve the symmetry and reduce the noise. The equivalent resistances of C_1 and C_2 will also affect the control of DC current, so the values of C_1 and C_2 must be chosen. To find an optimum value of the bypass capacitor, the phase noise at 100k-Hz offset frequency and phase difference of voltage swings versus C_1 are simulated, as shown in Fig. 5.

III. Measurement Results

In this work, the current-reused VCO is designed at the operation frequencies, 2.26 GHz. the VCO is fabricated by TSMC 0.18μm CMOS process. It is designed using source damping topology with optimum values of resistors. The core DC current is 0.9mA with a 1.8V voltage supply. As shown in Fig. 6, the measured phase noise at 100-kHz and 1-MHz offset frequencies of VCO_1 are -101.87 and -121.66 dBc/Hz. The output power is -4.83 dBm.

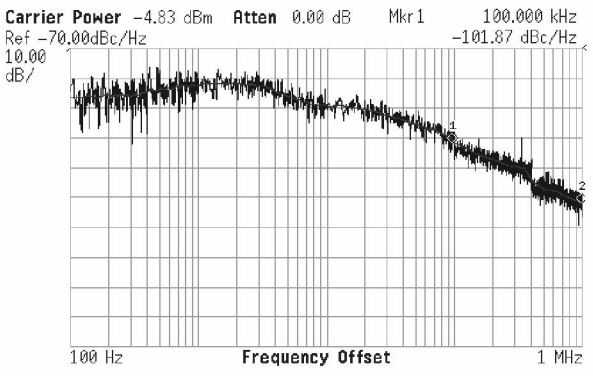
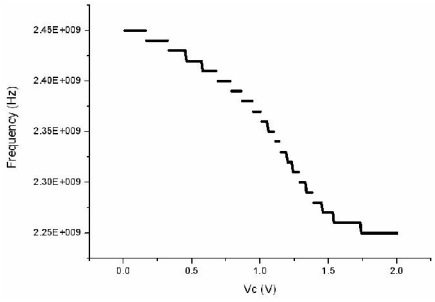


Fig. 6 Measured phase noise and output power.



(a)

Fig. 7 Measured tuning range.

Table I is the summary of the measured results. A figure-of-merit (FOM) has been defined in [1] to compare the performances of VCOs.

$$\mathrm{FOM} = \mathrm{L}\{f_m\} + 10\log\left[\left(\frac{f_m}{f_o}\right)^2 P_{DC}\right] \qquad (5)$$

where $\mathrm{L}\{f_m\}$ is the SSB phase noise measured at the offset frequency f_m from the oscillation frequency f_o. P_{DC} represents core DC power consumption in mW. The FOMs of the designed VCO is -187. The power consumption is 1.62mW.

Fig. 7 shows the measured tuning range. The measured tuning range is 2.25-2.45 GHz. The photograph of the VCO chip is shown in Fig. 8. The chip sizes is 1.01×0.86.

Table II shows the comparison of measured results of the presented VCO with those of recently published papers [1,2,4-7]. The phase noise performance is actually better than those in other recently presented papers [1,5,6,7]. Basically, power consumption is lower than that of the references [2,4] with the approximate phase noise due to optimum analysis on the damping impedances.

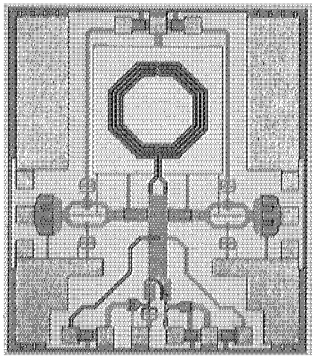


Fig. 8 Microphotograph of the designed VCO chip

TABLE I
Measurement results of VCO_1 and VCO_2

	VCO_1
Phase noise @100k-Hz	-101.87dBc/Hz
Phase noise @1M-Hz	-121.66dBc/Hz
Output power(dBm)	-4.83dBm
Core power consumption	1.62mW
Tuning range(GHz)	2.25-2.45 GHz
FOM	-187

TABLE II
Measurement results compared with other references

	Core Power (mW)	Freq. (GHz)	Phase Noise @100K	Phase Noise @1M	FOM
This work	1.62	2.26	-101.87	-121.66	-187
[1]	1	2	-103	NA	-189
[2]	NA	2.2	-103.5	-122.2	NA
[4]	2.175	2.01	-102	-124	-184.7
[5]	2.59	5	NA	-110	-180
[6]	1.8	2.1	NA	-110	-174
[7]	0.97	2.4	NA	-111	-178.7

IV. Conclusion

A low power current-reused voltage-controlled oscillator with source damping resistors is presented in this paper. It is designed by source damping topology with optimum resistors and bypass capacitors. By choosing the optimum values of source damping resistors and bypass capacitors, good symmetry of output voltage swings and lower phase noise can be done simultaneously. This VCO is operated at the frequency range from 2.25 GHz to 2.45 GH. The measured phase noises at 100 kHz and 1 MHz offset from 2.26 GHz are -101.87 dBc/Hz and -121.66 dBc/Hz, respectively. The power consumptions is 1.62mW. The current-reused VCO has lower power consumption and lower phase noise compared with other works.

Acknowledgement

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