A Fully-Differential Complementary Hartley VCO in 0.18 μm CMOS Technology

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***Abstract*—In this letter, a new complementary Hartley (C-Hartley) voltage controlled oscillator (VCO) with fully differential outputs is proposed, in which the self-biasing configuration is introduced to solve the biasing difficulty of a Hartley VCO by employing a five-port transformer. The proposed C-Hartley VCO with the center frequency of 5.6 GHz is implemented in a 1P6M 0.18 μm CMOS process. The measurement result shows that the phase noise is -123.6 dBc/Hz at 1 MHz offset frequency, while dissipating 6.5 mA from 1.6 V supply with the FOM of -188.5 dBc.**

***Index Terms*—CMOS, complementary, differential, hartley, self-biasing, transformer, voltage controlled oscillator (VCO).**

I. Introduction

THE voltage controlled oscillator (VCO) still remains an important component in the analog and RF system, since it affects the overall system performances. With the advance of submicron CMOS technology, the design of low phase noise VCO becomes more challenging. Several types of the VCO using a CMOS technology have been reported. Among them, the cross-coupled differential VCOs have been widely adapted in the CMOS transceivers due to the ease of design and moderate phase noise performances [1]. Recently, the Colpitts VCO has been paid great attention, after it is revealed that its cyclostationary noise nature improves the phase noise characteristics [2]. Originally, the Colpitts topology was developed for a single transistor oscillator, which basically uses a capacitor tapped feedback to generate the negative-*Gm*. Then it was extended to the differential or complementary topology [2]–[5]. The Hartley topology is also devised for a single transistor oscillator. However, it employs an inductor-tapped feedback. These tapped inductors cause many implementation difficulties. Contrary to the tapped capacitors, the tapped inductors provide both ac and dc path, and the separation of the ac and dc paths is not easy, making the realization of the dc-biasing networks difficult. And it entails many chip-size consuming inductors. In spite of these disadvantages, due to the circuit similarity to the Colpitts oscillator, it is expected to have low phase noise characteristics [6]. Thus, a novel biasing network and reduction of the number of inductors are the key design issues of the Hartley VCO.

In this letter, a differential CMOS C-Hartley VCO is reported, in which only one transformer is embedded. By introducing the differential and complementary topology with the self-biasing technique, the biasing difficulty of a Hartley VCO is eliminated. The designed VCO has low phase noise performances as well as low figure of merit (FOM).

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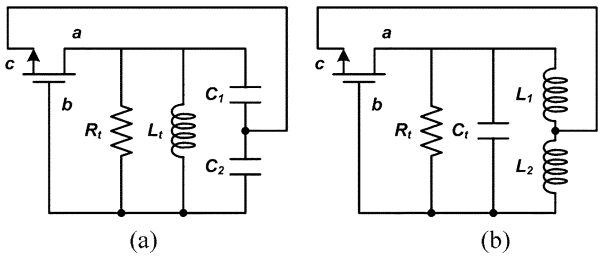

Fig. 1. One transistor oscillator topologies (a) Colpitts oscillator (b) Hartley oscillator.

II. Differential Hartley VCO

Fig. 1 shows the ac-equivalent circuits of the fundamental Colpitts and Hartley oscillators using a single transistor, where the details of the dc-biasing circuits are not shown. For both cases, one of the three terminals of the transistor (a, b, c) is supposed to be ac-grounded for the circuit realization. Depending on the ac-ground position, each oscillator can be realized in three different forms. It has to be noted that all three terminals of the transistor in the Hartley oscillator are connected through the inductors $(\mathrm{L}_1, \mathrm{L}_2)$, thereby it is not easy to set the dc voltages of each node, independently.

The Hartley oscillators using a NMOS or PMOS transistor with the source grounded are shown in Fig. 2. Since the voltages at the drain and gate nodes of the NMOS Hartley oscillator can be made equal to that of the PMOS oscillator, the two oscillators can be directly merged to a complementary form without hurting the oscillation condition. The resulting complementary configuration is similar to the C-Colpitts oscillator in [4]. The C-Colpitts oscillator becomes self-biased on its own due to the feedback inductor, which makes a dc-path between the drain and the gate nodes. But the C-Hartley oscillator has the dc-blocking capacitor, C_t', between the gate and the drain nodes. And to make matters worse, the C-Hartley oscillator needs dc-biases of the drain and gate nodes for the proper operation while maintaining the ac grounds at both nodes. Therefore, the C-Hartley oscillator in itself is of no use at all.

Fig. 3 shows how the self-biasing is obtained. The main idea is to use a differential configuration, in which two C-Hartley oscillators operating with anti-phases are combined into a single one. Since two C-Hartley oscillators have 180° phase difference, the center nodes of L_1' and L_2' become the virtual grounds. By connecting them, all gate and drain nodes can have the dc-path. Thus, the self-biasing is easily accomplished without inflicting the oscillation condition. The more detailed

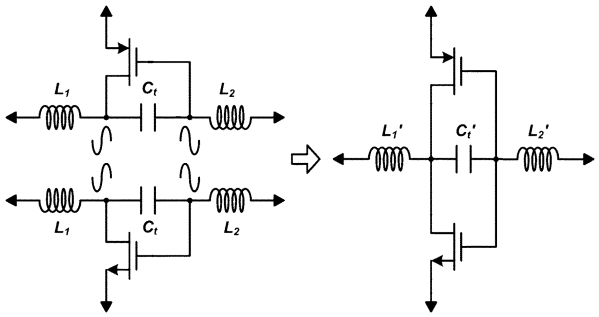

Fig. 2. The ac equivalent circuits of the Hartley oscillators using a PMOS or NMOS transistor, and its complementary form.

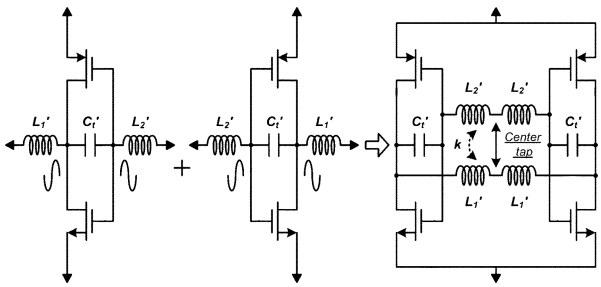

Fig. 3. Evolution from the complementary oscillators to the fully-differential C-Hartley oscillator.

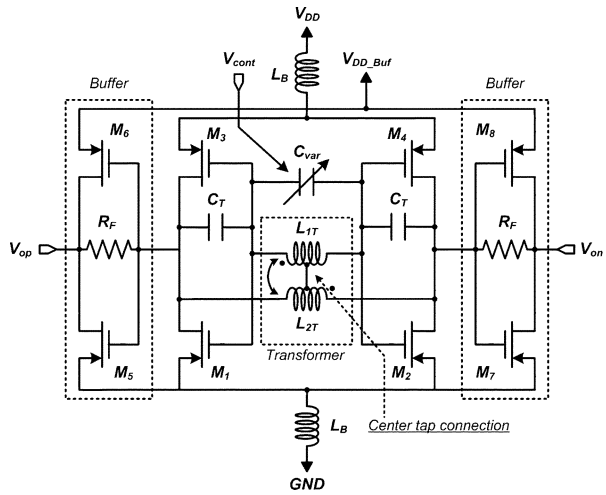

Fig. 4. Detailed schematic of the proposed differential C-Hartley VCO.

schematic of the proposed differential C-Hartley VCO is illustrated in Fig. 4. The 4-inductors $(\mathrm{L}_1', \mathrm{L}_2')$ are integrated into a single five-port transformer $(\mathrm{L_T})$ with a center tap. Consequently, the differential C-Hartley VCO is simply composed of two invertors with a NMOS and PMOS complementary pair, one transformer, and three capacitors that consist of two MIM capacitors and a varactor.

The transformer employed in the proposed VCO is simulated using 2.5 D EM simulator. The equivalent circuit of a five-port transformer is depicted in Fig. 5. It is designed to have asymmetric 2:1 turn ratio: two turns for the gate-side inductor and one turn for the drain-side. This asymmetric turn ratio is for the sake of optimization of the loaded Q factor of the LC resonator. When the transistors of the VCO core turn on, the impedances of

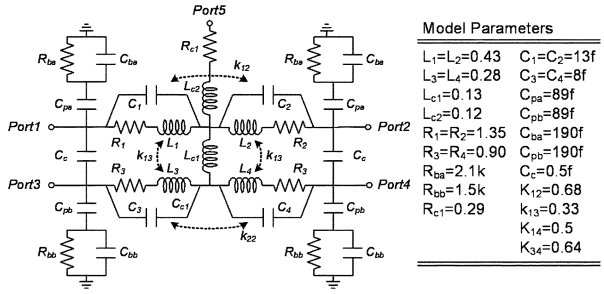

Fig. 5. Equivalent circuits of a five-port transformer with a center tap.

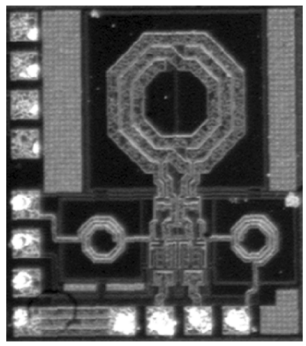

Fig. 6. Microphotograph of the proposed differential C-Hartley VCO (0.72×0.82 mm^2 including all pads).

the drains decrease to reduce the loaded Q factor of the LC resonator. On the other hand, the gate node impedances always remain high, irrespective of the transistor's turn-on or turn-off, so by making $\mathrm{L_{1T}}$ (two turn) higher than $\mathrm{L_{2T}}$ (one turn), the total effective loaded Q-factor can be increased. In the simulation, the differential C-Hartley VCO with an asymmetric 1:2 turn transformer shows about 3 dB lower phase noise performances than one with a symmetric 1:1 turn at the same frequency. The inductors, $\mathrm{L_B}$ also are helpful for the enhancement of the loaded Q factor [8].

The core NMOS sizes of $\mathrm{M_1}$ and $\mathrm{M_2}$ are 2.5 μm $\times$ 12 finger and the PMOS sizes are 2.5 times larger than that of the NMOSs. The size of feedback capacitor, $\mathrm{C_T}$ is determined to be around 200 fF. The accumulation NMOS varactor is used for the frequency tuning. The center frequency is set for 5.6 GHz with the tuning range about 150 MHz, which will be extended using the capacitor bank. The self biased output buffers are employed using high resistance feedback and its supply is separated with the core VCO circuit for the easy current measurement.

III. Experiment Results

The proposed differential C-Hartley VCO is implemented using a 1P6M 0.18 μm CMOS process with 2 μm-thick top metal as shown in Fig. 6. It has been tested on-wafer using 100 μm-pitch GSSG probe. The output spectrums and the phase noise performances are obtained by HP8764E signal analyzer. Fig. 7 shows the output frequencies as a function of the control voltage from 0 to 2 V, where the supply voltages are varied from 1.4 V to 2 V with 0.2 V step. The tuning range is about 160 MHz. The phase noise performances with the various supply voltages are shown in Fig. 8. The measured phase noises are -96.3 and -123.6 dBc/Hz at 100 kHz and 1 MHz offset, respectively from

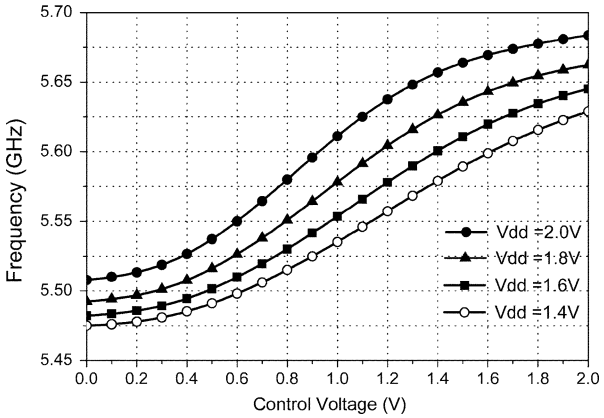

Fig. 7. Oscillation frequency as a function of the control voltage.

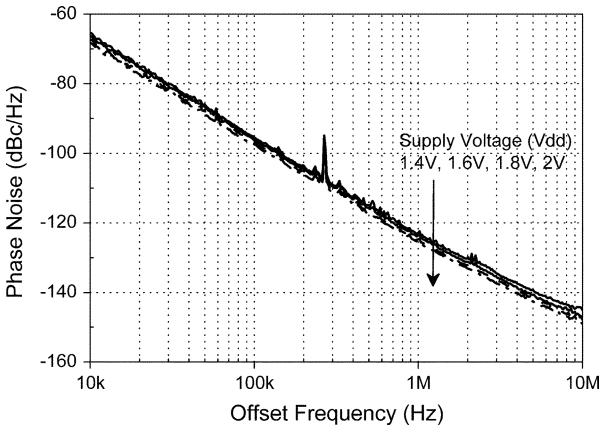

Fig. 8. Measured phase noises at the supply voltages of 1.4, 1.6, 1.8, and 2 V with the control voltages of 0.7, 0.8, 0.9, and 1 V as a function of offset frequencies.

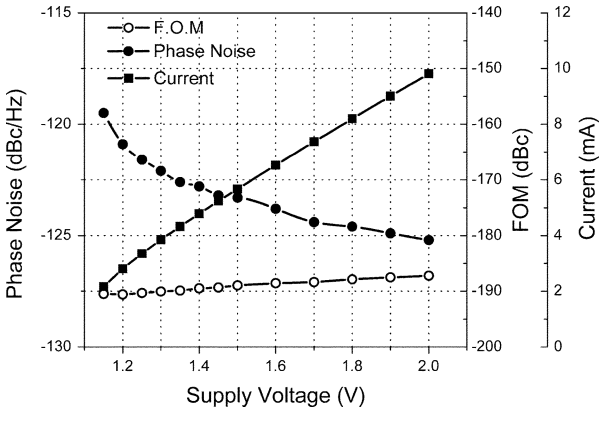

Fig. 9. Measured phase noises @ 1 MHz, figure of merits (FOM) and current consumptions of the VCO core as a function of the supply voltages.

a 1.6 V supply. The phase noise differences with the supply voltage change are less than 2 dB.

Fig. 9 shows the measured phase noises, the FOMs and the current consumptions as a function of the supply voltage. The phase noises are under -120 dBc/Hz and the FOMs are around -190 dBc, where the well-known FOM equation for a measure for the VCO comparison is used

TABLE I
COMPARISONS OF THE PROPOSED DIFFERENTIAL C-HARTLEY VCO AND THE PREVIOUSLY REPORTED RESULTS

Ref.	This	This	[3]	[4]	[5]	[6]	[7]	Unit
Freq.	5.6	5.6	5	6	5.6	4.5	5.62	GHz
PN@ 1MHz	-122.7	-123.6	-120.4	-118.1	-119	-122.5	-116.7	dBc/Hz
Current	4.6	6.5	2	4.6	2	4.5	3.9	mA
Supply	1.4	1.6	1.5	2.0	1.2	1.5	1.5	V
FOM	-189.6	-188.5	-189.6	-184.0	-190.3	-187.0	-184.0	dBc
Tech.	0.18	0.18	0.18	0.35	0.18	0.18	0.18	μm

$$\mathrm{F.O.M} = PN(\Delta f_{\mathrm{offset}}) + 10\log(P_{\mathrm{diss}}) - 20\log\left(\frac{f_{\mathrm{osc}}}{\Delta f_{\mathrm{offset}}}\right) \quad (2)$$

where f_{osc} is an oscillation frequency, $\Delta f_{\mathrm{offset}}$ is an offset frequency, *PN* is a measured phase noise and P_{diss} is a power consumption in milliwatt of the VCO core. The current consumption is linearly dependant on the supply voltage due to the self-biasing configuration. The phase noise performances of the proposed VCO as well as the FOM are better or comparable to the results reported in the literatures as summarized in Table I.

IV. CONCLUSION

We present a new fully differential C-Hartley VCO. By introducing the differential and complementary configuration as well as the self-biasing technique using a single transformer, the biasing difficulty of a Hartley VCO is removed. The proposed VCO has low phase noise performances at 5.6 GHz due to the topological advantages and also the asymmetric transformer. The measured phase noises are -96.3 and -123.6 dBc/Hz at 100 kHz and 1 MHz offset from 1.6 V supply, respectively. And it also shows low FOM of -188.5 dBc.

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