Design of Current Reuse CMOS LC-VCO

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***Abstract* — This paper describes the design of voltage controlled oscillator (VCO) with a low-power static frequency divider. The new LC-VCO replaces one of the NMOS of a conventional differential LC-VCO with a PMOS, which reduces power dissipation to the half and allows operation at reduced supply voltages. Based on a 0.13um UMC CMOS process, the VCO is simulated using 0.8V supply voltage. It is demonstrated that the proposed N-&P-MOS cross-coupled pair VCO operating at 806MHz can work with a power consumption of 0.24mW with as low as -133dBc/Hz of phase noise at 1-MHz offset. Finally, in order to generate the quadrature signals at 403MHz, a low-power static frequency divider is designed, which utilizes a parallel switching current topology.**

I. INTRODUCTION

In the last few years, the research and development of direct conversion radio transceivers have dramatically increased due to the need for low-power, low-cost, and highly integrated transceiver [1]. Many direct conversion architectures require quadrature local oscillator (LO) signals. Quadrature signal generation is required when the modulation scheme contains information in the phase. The importance of the accuracy of quadrature signal becomes critical when it is applied to zero-IF transceivers. Various quadrature signal generation techniques have been reported, such as the combination of voltage-controlled oscillator (VCO) and poly-phase filter [1], the quadrature voltage-controlled oscillator (QVCO), VCO at double frequency followed by master-slave flip-flops, and ring-type oscillator [2]. Each has their own advantage and disadvantage in terms of complexity, power consumption and critical wireless performance like phase noise degradation. When a VCO is used with a frequency divider to generate a quadrature signal, the VCO should be designed at 2x frequency and needs to be tuned large range to meet specifications and to compensate process variations. Due to their relatively good phase noise, ease of implementation, low power-consumption, and differential operation, cross-coupled LC oscillators play an important role in VCO circuit design. Fig. 1(a) shows a conventional LC-VCO, where a differential LC-VCO simply consists of a cross-coupled pair of transistors (M1 and M2) with an LC-tuning circuit. It is known, that the current source, shown in Fig.1 (a) may be the largest contributor to the phase noise in a VCO [2], especially to the $1/f^3$ shaped phase noise close to the oscillation frequency. A general LC-VCO can be symbolized as in Fig.1 (b) [3]. The oscillator consists of an inductor L and a capacitor C, building a parallel resonance tank, and an active element $-R$, compensating the losses of the inductor (R_L) and the losses in of the capacitor (R_C). As the capacitance C is proportional to a tuning input voltage, the circuit results in a VCO with angular center frequency $\omega_c = 1/\sqrt{LC}$. LC VCOs operating at UHF frequencies suffer from the low-Q spiral inductors at these frequencies. A typical value at 400MHz is (Q=3). The quality factor (Q) of spiral inductor improves significantly at 800MHz (Q of = 8-10, typical). Noise to signal ratio in an LC oscillator can be described by [4],

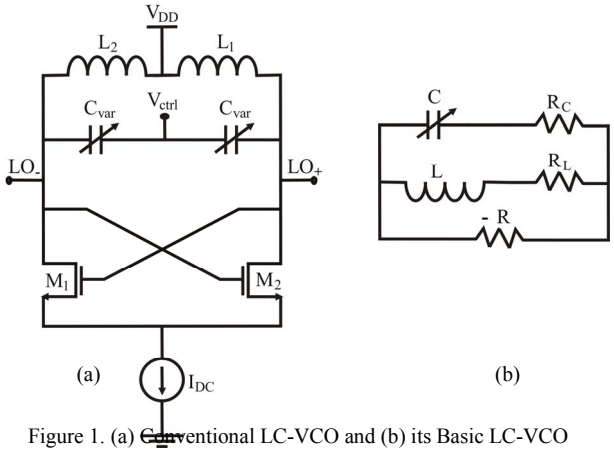

Figure 1. (a) Conventional LC-VCO and (b) its Basic LC-VCO

$$\frac{N}{S} = \frac{\omega . K . T}{Q . P_{diss}} \qquad (1)$$

This equation clearly shows the importance of high Q. Since Q of the capacitor is very high, LC tank Q is primarily determined by the Q of the spiral inductor.

In order to reduce the power dissipation to half that of conventional differential topologies, an 806MHz current-reuse differential LC-VCO is proposed in this paper. An analog master-slave divider employing parallel current switching topology is designed to divide the signal by two for MICS 402-405 MHz direct conversion transceivers.

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In section II, an innovative LC-VCO using current-reuse topology is introduced and the operational principles are described. In section III, the design of high-speed static frequency divider using parallel current switching topology is introduced. Simulation results and discussions are presented in section IV. Finally a conclusion is provided in section V of this paper.

II. LC-VCO DESIGN

A widely known oscillator is the conventional differential negative $-G_m$ oscillator that is shown in Fig. 1(a). The topology consists of two identical half circuits composed of switching transistors (M1 and M2), inductors (L1 and L2), and varactors (C_{var}). The negative conductance is provided by the cross-connected pairs of transistors M1 and M2, which acts as an active buffer. Fig.2 shows the proposed VCO by modifying the conventional VCO topologies for low-power applications.

The current reuse differential VCO topology is used by stacking switching transistors in series like a cascode. Where the LC-VCO replaces one of the NMOS of a conventional differential LC-VCO with a PMOS. The new VCO in Fig.2 uses both NMOS and PMOS transistors in the cross-connected pair as a negative conductance generator. A series connected N- and P-MOS transistors (M1 and M2) with LC-tanks constitutes the current-reused differential VCO. The series stacking of N- and P-MOS allows the supply current to be reduced by half compared to that of the conventional LC-VCO while providing the same negative conductance.

We explain the operation during each half period of the operation (when the voltage at node X is high and low): during the first half-period, the transistors M1 and M2 are on and the current flows from VDD to ground through the tuning inductor L. During the second-half period, the transistors are both off and the current flows in the opposite direction and lets the LC tank discharge. This results in the end save half of the power. Because the N- and P-MOS pair operates in triode region near the peak of the voltage swing, the voltage swing is only limited by the power supply. Therefore, this topology is likely suitable for MICS applications. Note that in the conventional differential VCO, the cross-connected transistors switch alternately, whereas in the proposed VCO, the N- and P-MOS switch at the same time.

In the conventional N- or P-MOS based differential VCO, where the transistors switch alternately, the phase noise can be degraded significantly by the noise near the second harmonic [5]. The proposed VCO does not have a common-source node because the transistors switch on and off at the same time. Therefore, the designed VCO is inherently immune to the phase noise degradation caused by second-harmonic terms at the common-source node. Utilizing of PMOS transistor in the cross-connected pair can additionally help to reduce the phase noise due to lower flicker noise and hot carrier effects [6].

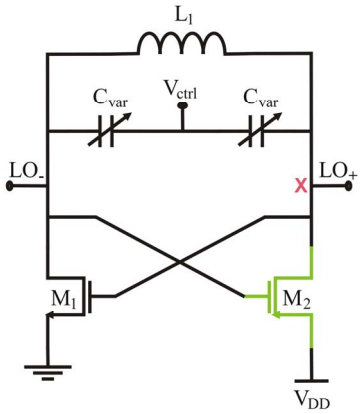

Figure 2. Proposed LC-VCO

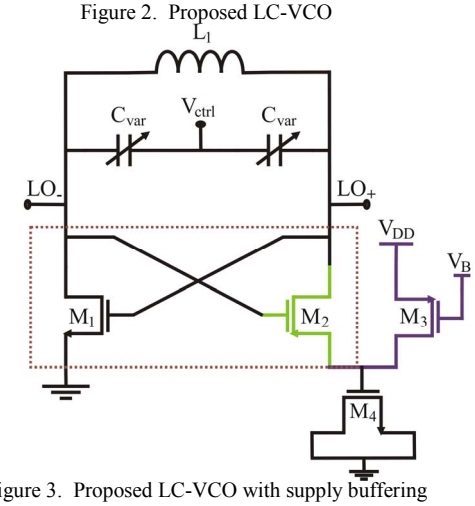

Figure 3. Proposed LC-VCO with supply buffering

To avoid the unsymmetrical in the circuit between the two branches because of using N- and P-MOS transistors and then maintaining the output waveform symmetric, the transistors aspect ratio should be well selected.

Sensitivity of a VCO to noise on the power supply is one of the most important parameters which contribute to jitter. The main problem in the circuit shown in Fig.2 is that the PMOS (M2) is directly connected to the supply source, which means that any change in VDD leads to direct change in V_{ds} of M2 and consequently its drain current will change which causes the frequency of the VCO to change. Therefore attempt should be made to increase the PSRR of the VCO and consequently minimize the effect of supply noise to the VCO frequency. In the structure shown in Fig.3, the transistor (M3) is added to isolate M2 from the VDD, therefore changes on the supply voltage VDD which causes changes on the voltage V_{ds} of M3, have a second order effect on the

current through M2 and high power supply rejection ratio is achieved. A small size M4 transistor implements capacitor used to cancel any noise oscillations that may occur at the supply source.

III. PARALLEL SWITCHING DIVIDER TOPOLOGY

Normally, the conventional static frequency dividers are built by master-slave DFF utilizing current mode logic (CML) structure. In such high-speed circuit, CML are often adopted instead of CMOS static logic due to its higher speed. Figure 4(a) shows the block diagram of the conventional 2:1 static frequency divider. It consists of two latches which connected in a master and slave configuration. Utilizing complimentary input clock signal, $clk+$ and $clk-$, trigger two latches to operate alternately between sense and latch modes.

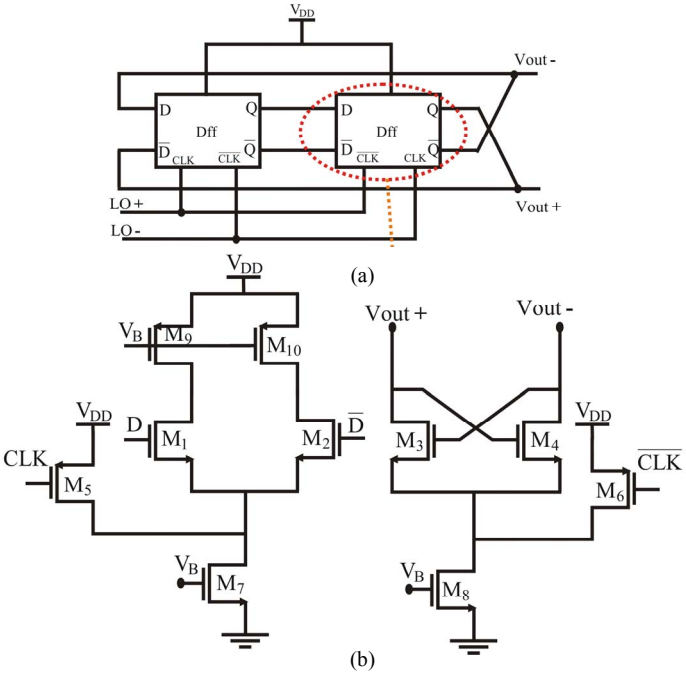

Figure 4. (a) Static divider, (b) Parallel current switching topology

In conventional static divider, if the process is variant or the input clock signal is affected by cross-talk, the DC level would be varied and yields a variable current [7]. In order to reduce the supply voltage, and keep the DC level constant without change, the concept of parallel current switching [7] is adopted in the design as shown in Fig. 4(b). Instead of stacking the NMOS differential pairs, PMOS transistors (M5-M6) are used as the clock input pair while transistors (M7 and M8) act as current sources. When the CLK is high, M5 turns off and M6 turns on. The current of M7 is steering in the reading pair while the current of M8 is taken away from the latching pair by M6. As a result, the latch operates in its sensing mode. On the contrary, as CLK goes low, the latching pair working in the latch mode. Due to the low supply voltage, transistors M7 and M8 operate in the linear region.

IV. SIMULATION RESULTS AND DISCUSSION

The quadrature signal generator utilizes the frequency driver, which is based on the topology of master-slave D flip-flop. Frequency divider drives a buffer circuit. The conventional and newly proposed VCOs, shown in Fig. 1,3 are designed and simulated in a UMC 0.13µm CMOS process under a typical-typical corner in Cadence. The two VCOs, working at 806 MHz are biased to draw 0.55 and 0.3mA from 0.8V supply, respectively. The current consumption is significantly reduced. The divider is biased to draw 0.2mA from 0.8V supply. The phase noise for both the conventional and the proposed one is shown in Fig. 5. The simulated values for the conventional and proposed VCO are -124 and -133dBc/Hz at 1MHz offset, respectively. Results clearly show that the conventional VCO degrades the phase noise more than the proposed one. The phase noise $L(\omega_m)$ can be expressed by Leeson's formula [8].

$$\mathrm{L}(\omega_m) \propto \frac{1}{\mathrm{V_o^2}} \cdot \frac{KT}{C_L} \cdot \frac{\omega_0}{Q} \cdot \frac{1}{\omega_m^2} \qquad (2)$$

where K is Boltzmann's constant, T is the absolute temperature, and ω_m is the offset frequency from the oscillation frequency ω_0, $\mathrm{V_0}$ is the output voltage amplitude, and C_L is the total output load capacitance. A high quality factor (Q) enhances the phase noise performance, as seen in (1). Also, reducing the biasing current injects less noise to the tank circuit, which also leads to better phase noise performance.

Figure 6 shows the simulated differential output voltage of the proposed VCO. The peak-to-peak voltage of the output waveform is as high as 800mV, but in the conventional VCO, the output waveform will be in a lower value, due to the stacked N- or P-MOS.

The figure of merit (FOM) is widely used to compare the VCO performance among different designs.

$$FOM = \mathrm{L}\{f_m\} + 10\log\left[\left(\frac{f_m}{f_0}\right)^2 P_{DC}\right] \qquad (3)$$

where, $\mathrm{L}\{f_m\}$ is SSB phase noise at the offset frequency of f_m from the oscillation frequency of f_0, and P_{DC} represents DC power dissipation in mWs. FOMs for the conventional and the newly one are -186 and-198dB, respectively. This good FOM for the proposed VCO compared to the conventional VCO is due to the low power consumption and good phase noise performance.

The simulated output power for the proposed VCO is 9dBm, which is enough to switch on and off the switching input ports of the mixer. The transistor aspect ratio of N-&P-MOS transistors should be chosen properly to make the circuits as symmetric as possible. The simulated PSRR from the V_{DD} supply voltage is shown in Fig.7. The simulated values for the proposed VCOs with and without the buffer are -76 and -14dB, respectively.

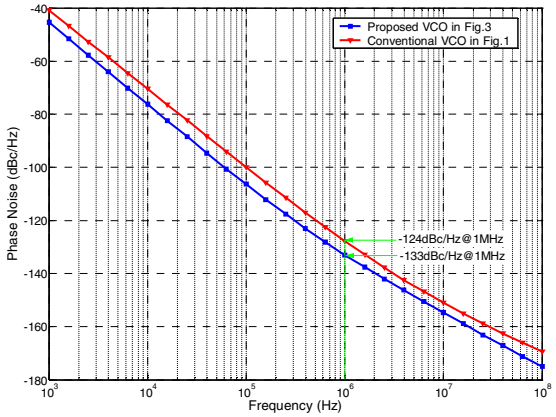

Figure 5. The phase noise of the conventional and proposed VCO

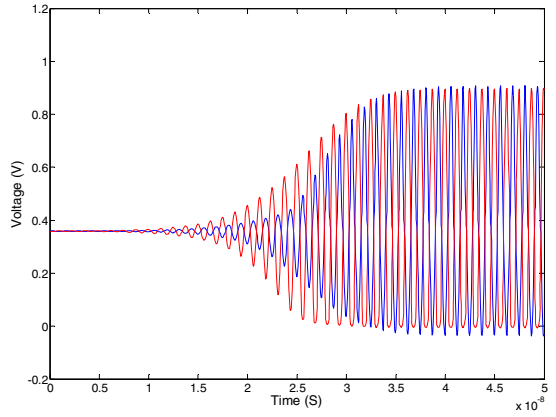

Figure 6. The output waveform of the proposed VCO at 806MHz

VII. Conclusion

The proposed N- and P-MOS cross-coupled pair LC-VCO topology offers low power, small size, and high performance (low phase noise) solutions for the integrated differential LC-VCO. A 403 MHz quadrature signal generator proposed in this work achieves a phase noise of -133dBc/Hz at 1MHz offset while consuming 0.3mA for the VCO and 0.2mA current for the divide-by-two. The proposed VCO reuse the dc current, so it consumes only half the amount of power and shows better phase noise performance compared to the conventional designs. By parallel connecting the clock input pair with the reading and latching pairs, the limitation on the supply voltage is alleviated, and the supply voltage is reduced by one transistor overdrive, so it provides a viable solution for ultra-low-voltage applications. Power supply noise is often a significant contributor of phase noise and cannot be ignored, so attempt was made to reduce the direct effect of the power supply on the circuit design, by isolating the power supply directly connected to the circuit, and adding a terminator MOS capacitor to cancel any power supply noise oscillations.

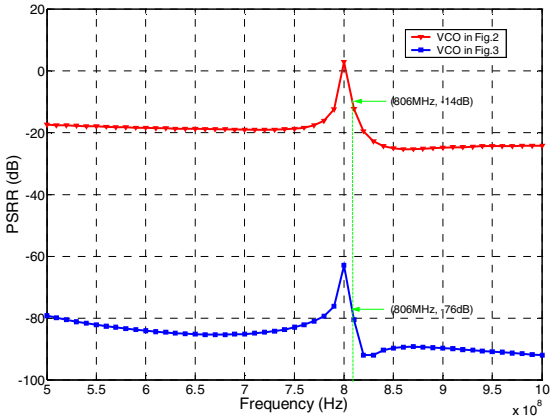

Figure 7. The PSRR of the proposed LC-VCO

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