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### Chapter 1

Introduction

# 1.1 5G Spectrum and bands

5G is the fifth generation of wireless cellular technology, offering higher upload and download speeds, more consistent connections, and improved capacity than previous networks.

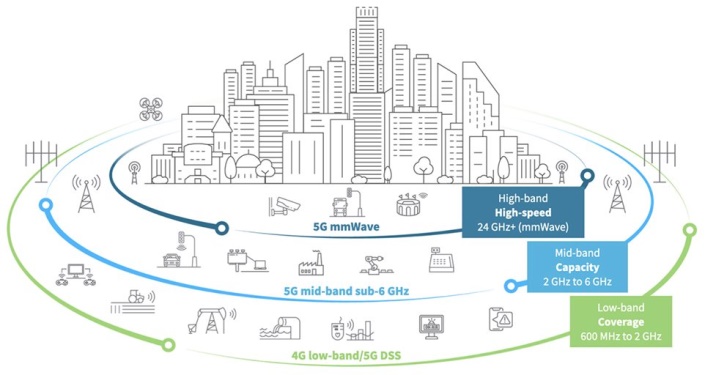
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Fig 1.1 5G spectrum bandwidth

The bands in 5g Spectrum are classified into:

**1. High Band (mmWave)**

* **Advantages**: Offers ultra-high data rates, enabling multi-gigabit-per-second speeds for high-bandwidth applications like 4K video streaming and virtual reality. Facilitates massive capacity due to large available spectrum.
* **Limitations**: Limited coverage area due to high propagation losses and susceptibility to blockages from obstacles like buildings and foliage. Requires dense deployment of small cells for adequate coverage.

**2. Mid Band (Sub-6 GHz)**

* **Advantages**: Balances between coverage and capacity, providing a good compromise between data rates and coverage area. Suitable for urban and suburban deployments, offering higher speeds than low band.
* **Limitations**: Limited available spectrum compared to low band, leading to potential congestion in densely populated areas. Offers lower data rates compared to high band mmWave.

**3. Low Band (Sub-1 GHz)**

* **Advantages**: Offers extensive coverage with superior signal penetration through buildings and obstacles, making it ideal for rural and remote areas. Provides reliable connectivity with wider coverage footprint.
* **Limitations**: Limited bandwidth leads to lower data rates compared to mid and high bands. Prone to congestion in urban areas due to the limited available spectrum, impacting overall network capacity.

# 1.2 Phase Locked Loop

A phase-locked loop (PLL) is a [control system](https://en.wikipedia.org/wiki/Control_system) that generates an output [signal](https://en.wikipedia.org/wiki/Signal_(electrical_engineering)) whose [phase](https://en.wikipedia.org/wiki/Phase_(waves)) is fixed relative to the phase of an input signal. It operate by producing an oscillator frequency to match the frequency of an input signal. It makes an output signal whose frequency is depends on the input phase difference. It maintains a well-defined phase relationship between two periodic signals - the input serves as a reference, while the output acts as a follower. Phase detector compares phase of input signal with the phase derived from its output oscillator adjusts the frequency of its oscillator to maintain the phase matches and by incorporating a [frequency divider](https://en.wikipedia.org/wiki/Frequency_divider) the PLL can generate a stable frequency that is a multiple of the input frequency. PLL used for clock synchronization, [demodulation](https://en.wikipedia.org/wiki/Demodulation), [frequency synthesis](https://en.wikipedia.org/wiki/Frequency_synthesis), [clock multipliers](https://en.wikipedia.org/wiki/Clock_multiplier), and signal recovery from a noisy communication channel. They are widely employed in [radio](https://en.wikipedia.org/wiki/Radio), [telecommunications](https://en.wikipedia.org/wiki/Telecommunications), [grid-tie inverters](https://en.wikipedia.org/wiki/Grid-tie_inverter), electronic power converters used to integrate [DC](https://en.wikipedia.org/wiki/Direct_current) renewable resources and storage elements such as [photovoltaics](https://en.wikipedia.org/wiki/Photovoltaics) and [batteries](https://en.wikipedia.org/wiki/Electric_battery) with the power grid, and other electronic applications.

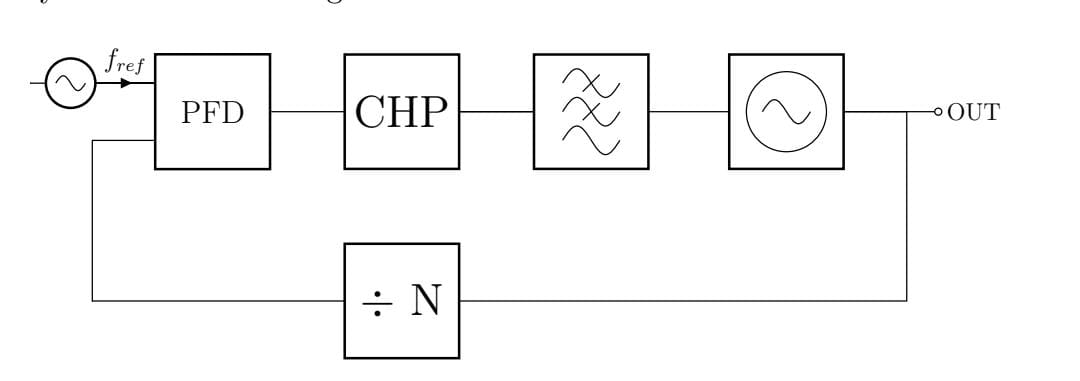


Fig 1.2 Phase locked loop

The modes of operation of Phase locked loop (PLL) are:

* **Free running**- the center frequency of the PLL, which is the frequency that the VCO runs at when not locked to the input frequency.
* **Capture**- in order for the VCO to lock to the input frequency initially, the frequency must be within the PLL’s capture range.
* **Phase lock (or tracking**) - once the VCO has locked to the input frequency, it will continue to track and adjust to the input frequency as long as it stays within the PLL’s lock range. The lock range is wider than the capture range.

# 1.3 Working of PLL

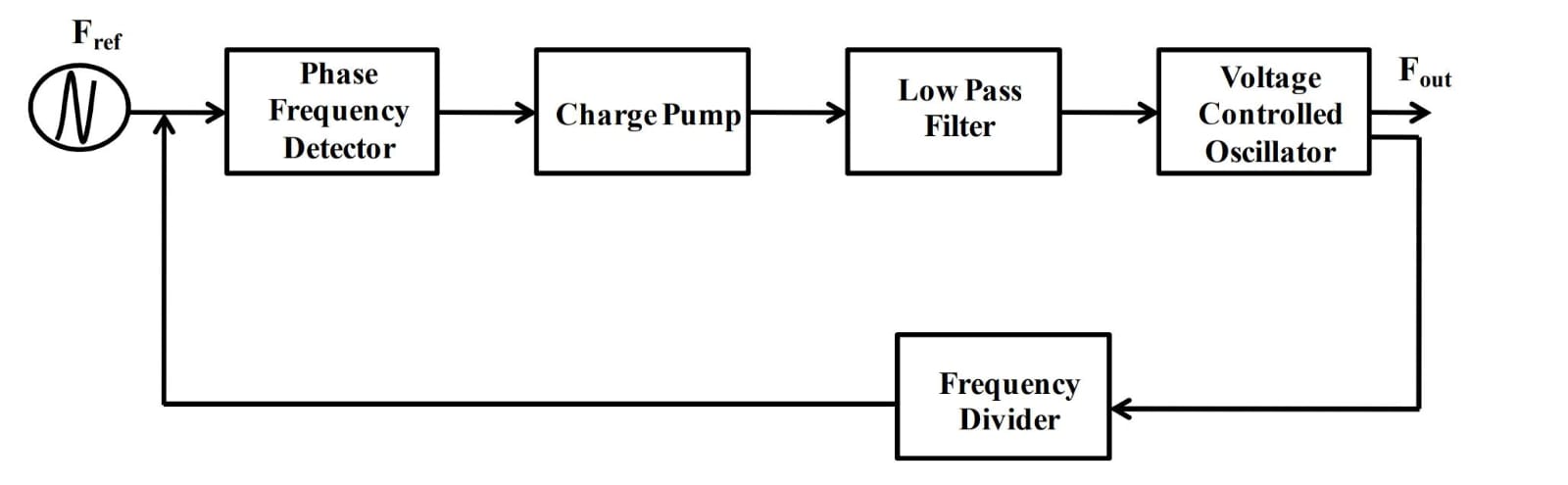


Fig.1.3 [Block diagram](https://en.wikipedia.org/wiki/Block_diagram) of a phase-locked loop

The block diagram shown in the figure shows an input signal, FI, which is used to generate an output, Fout. The input signal is often called the reference signal Fref.

At the input, a phase detector compares two input signals, producing an error signal which is proportional to their phase difference. The error signal is then low-pass filtered and used to drive a VCO which creates an output phase. The output is fed through an optional divider back to the input of the system, producing a [negative feedback loop](https://en.wikipedia.org/wiki/Negative_feedback_loop). If the output phase drifts, the error signal will increase, driving the VCO phase in the opposite direction so as to reduce the error. Thus the output phase is locked to the phase of the input. The analog PLL and digital PLL where Analog phase locked loops are generally built with an analog phase detector, low-pass filter and VCO placed in a [negative feedback](https://en.wikipedia.org/wiki/Negative_feedback) configuration. A digital phase locked loop uses a digital phase detector; it may also have a divider in the feedback path or in the reference path, or both, in order to make the PLL's output signal frequency a [rational](https://en.wikipedia.org/wiki/Rational_number) multiple of the reference frequency. A non-integer multiple of the reference frequency can also be created by replacing the simple divide-by-N counter in the feedback path with a programmable [pulse swallowing counter](https://en.wikipedia.org/wiki/Pulse_swallowing_counter). This technique is usually referred to as a [fractional-N synthesizer](https://en.wikipedia.org/wiki/Fractional-N_synthesizer) or fractional-N PLL.

The VCO generates a periodic output signal. Assume that initially the oscillator is at nearly the same frequency as the reference signal. If the phase from the oscillator falls behind that of the reference, the phase detector changes the control voltage of the oscillator so that it speeds up. If the phase creeps ahead of the reference, the phase detector changes the control voltage to slow down the oscillator. Since initially the oscillator may be far from the reference frequency, practical phase detectors may also respond to frequency differences, so as to increase the lock-in range of allowable inputs. Depending on the application, either the output of the controlled oscillator, or the control signal to the oscillator, provides the useful output of the PLL system

## 1.3.1 Phase Detector

The phase sensitive detector can be used in a number of circuits – anywhere that it is necessary to detect the phase between two signals. The phase detector enables phase differences to be detected and the resultant "error" voltage to be produced.

There are different types of phase detector. They can be categorised in a variety of ways, but one is given below:

* Phase only sensitive detectors
* Phase / frequency detectors

Phase only sensitive detectors that are only sensitive to phase are the most straightforward form of phase detector. As the name indicates their output is only dependent upon the phase difference between the two signals. When the phase difference between the two incoming signals is steady, they produce a constant voltage. When there is a frequency difference between the two signals, they produce a varying voltage at a frequency equal to the frequency difference.

The difference frequency product is the one used to give the phase difference. However it is quite possible that the difference frequency signal will fall outside the pass-band of the loop filter, and hence the overall phase locked loop. If this occurs then no error voltage pass through the PLL loop filter and on to the VCO to bring it into lock. This means that there only is a limited range over which the phase locked loop can be brought into lock. This range is called the capture range. Once in lock the loop can generally be pulled over a much wider frequency band.

Apart from using a phase frequency detector, there are several ways in which this problem can be overcome. The oscillator must be steered close to the reference oscillator frequency. This can be achieved in a number of ways. One is to reduce the tuning range of the oscillator so that the difference product will always fall within the pass-band of the loop filter. In other instances another tune voltage can be combined with the feedback from the loop to ensure that the oscillator is in the correct region. This is approach is often adopted in microprocessor systems where the correct voltage can be calculated for any given circumstance

* XOR phase detector:   The exclusive OR, XOR phase detector circuit can provide a very useful simple phase detector for some applications. It comprises of a logic exclusive OR circuit. Being digital in format it can often fit into a phase locked loop with ease as many of the circuits associated with the phase locked loop may already be in a digital format.
* Alternatively an exclusive OR can be made from discrete components to give a wider variety of levels and other options. Exclusive OR phase detector.
* The way in which an exclusive OR, XOR phase detector works can be seen by the diagram below:  
  XOR phase detector response waveforms. It can be seen that using these waveforms, the XOR logic gate can be used as a simple but effective phase detector. As might be expected for such a simple circuit, there are a few drawbacks to using an XOR phase detector:
* The phase detector is sensitive to the clock duty cycle. This means that a steady duty cycle, i.e. 1:1 should be used. It will lock with a phase error if the input duty cycles are not 50%.
* The output characteristic of the XOR phase detector show repetitions and gain changes. This means that if there is a frequency difference between the input reference and PLL feedback signals the phase detector can jump between regions of different gain.

The characteristic of the phase detector is as shown below

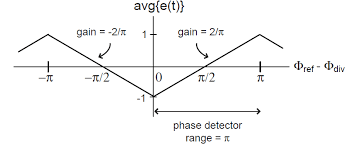


Fig.1.4 XOR phase detector response curve

* The nominal lock point with an XOR phase detector is also at the 90° static phase shift point.
* Unlike an analog mixer phase detector, the XOR version is independent of input amplitude and constant over a π phase range.

## 1.3.2 Voltage Controlled Oscillator VCO Design for PLLs

The performance of the voltage controlled oscillator in any phase locked loop is a key circuit block, determining many aspects of the overall performance. Within a phase locked loop, PLL, or frequency synthesizer, the performance of the voltage controlled oscillator is key.

The voltage controlled oscillator performance governs many aspects of the performance of the whole phase locked loop or frequency synthesizer.

The design of a high performance voltage controlled oscillator is not a trivial task. Consideration of the circuit components used and the layout plays role in determining the performance. This requires sound theoretical design, followed by careful choice of all the components and then a good PCB layout. Even with circuit simulation, it may take a couple of iterations of the VCO layout .

## 1.3.3 Impact of loop filter on PLL performance

* The loop filter characteristics affect a number of areas of the phase locked loop performance.
* Filter comparison frequency:   One of the major functions of the loop filter is to remove unwanted components of the phase detection or phase comparison frequencies. If they appear at the input to the VCO, then sidebands will appear offset from the carrier by a frequency equal to the phase comparison frequency.
* Loop stability:   The break points and roll off of the loop filter are of particular importance. The filter should be designed to give the required fall in loop gain at the unity gain point for the loop, otherwise the loop can become unstable.
* Transient response / tracking:   In some applications it may be necessary for the phase locked loop to track another signal or change frequency. The loop filter acts to slow the response down. The narrower the loop bandwidth, i.e. the lower the cut-off frequency of the filter, the slower the response of the loop to responding to changes. Conversely if the loop requires a fast response to changes in frequency, then it will need a wide loop bandwidth.

## 1.3.4 Divider

The divider is used to scale down the VCO output frequency in order to compare it with the reference frequency. There are both analog and digital divider structures, both frequently used in PLL design. In digital dividers, the speed of their logic gates limits their working frequency (in GHz). Hence, they are not suited for higher frequency applications. For very high frequencies analog dividers are commonly used.

## 1.3.5 Charge pump

Charge pump is used to sink or source current to or from the loop filter based on the output from the phase detector. When the phase detector sends an UP pulse the charge pump converts it to a current that charges the loop filter, i.e, charge current. Correspondingly the loop filter gets discharged by the DOWN pulse. When both switches are off the voltage is held constant since there is no current if low. The up and down charges will respectively charge and discharge the loop f ilter output, and as a result the VCO output frequency will increase and decrease accordingly. The switches in the model are usually implemented by NMOS and PMOS transistors. Charge pumps tend to suffer from non-idealities such as charge sharing, current mismatch, charge injection, noise and power dissipation. Various charge pump topologies exist that help reducing these non-idealities.

Generally charge pumps can be categorized into four different topologies: conventional tri-state, current steering, differential input single-ended output and fully differential.

# 1.4 Phase locked loop operation

The basic concept of the operation of the PLL is relatively simple, although the mathematical analysis and many elements of its operation are quite complicated. The diagram for a basic phase locked loop shows the three main element of the PLL: phase detector, voltage controlled oscillator and the loop filter.

In the basic PLL, reference signal and the signal from the voltage controlled oscillator are connected to the two input ports of the phase detector. The output from the phase detector is passed to the loop filter and then filtered signal is applied to the voltage controlled oscillator.

The Voltage Controlled Oscillator, VCO, within the PLL produces a signal which enters the phase detector. Here the phase of the signals from the VCO and the incoming reference signal are compared and a resulting difference or error voltage is produced. The error signal from the phase detector passes through a low pass filter which governs many of the properties of the loop and removes any high frequency elements on the signal. Once through the filter the error signal is applied to the control terminal of the VCO as its tuning voltage. The sense of any change in this voltage is such that it tries to reduce the phase difference and hence the frequency between the two signals. Initially the loop will be out of lock, and the error voltage will pull the frequency of the VCO towards that of the reference, until it cannot reduce the error any further and the loop is locked.

When the PLL, phase locked loop, is in lock a steady state error voltage is produced. By using an amplifier between the phase detector and the VCO, the actual error between the signals can be reduced to very small levels. However some voltage must always be present at the control terminal of the VCO as this is what puts onto the correct frequency.

The fact that a steady error voltage is present means that the phase difference between the reference signal and the VCO is not changing. As the phase between these two signals is not changing means that the two signals are on exactly the same frequency. PLL is a very useful building block, particularly for radio frequency applications. It forms the basis of a number of RF systems including the indirect frequency synthesizer, a form of FM demodulator and it enables the recovery of a stable continuous carrier from a pulse waveform. In this way PLL is an essential RF building tool.

# 1.5 Performance parameter

* Type and order.
* [Frequency ranges](https://en.wikipedia.org/wiki/Pll_ranges): hold-in range (tracking range), pull-in range (capture range, acquisition range), lock-in range.
* Loop bandwidth: Defining the speed of the control loop.
* Transient response: Like overshoot and settling time to a certain accuracy (like 50 ppm).
* Steady-state errors: Like remaining phase or timing error.
* Output spectrum purity: Like sidebands generated from a certain VCO tuning voltage ripple.
* Phase-noise: Defined by noise energy in a certain frequency band. Highly dependent on VCO phase-noise, PLL bandwidth, etc.
* General parameters: Such as power consumption, supply voltage range, output amplitude.

**Effect of Phase on signal**

**Synchronization Issues:** In digital systems, phase differences between clock signals can cause synchronization issues, leading to data transfer errors and reduced system performance**.**

**Latency:**

Phase misalignment in synchronized systems can introduce latency, affecting the timing and coordination of processes.

**Signal Distortion:**

In analog circuits such as mixers and amplifiers, phase differences between input signals can cause signal distortion, affecting the quality of the output signal.

**Symbol Errors:**

In digital communication systems, a phase difference can cause symbol errors, leading to an increased bit error rate (BER).

**Phase Noise:**

In oscillators and synthesizers, phase noise refers to the short-term random fluctuations in the phase of the signal. High phase noise can degrade the signal quality and increase the error rate in communication systems.

**Phase angle of points on a sine wave**

The key to the operation of a phase locked loop is the phase difference between two signals, and the ability to detect it. The information about the error in phase or the phase difference between the two signals is then used to control the frequency of the loop.

This phase difference can also be represented on a circle because the two waveforms will be at different points on the cycle as a result of their phase difference. The linear plot can also be represented in the form of a circle. The beginning of the cycle can be represented as a particular point on the circle and as a time progresses the point on the waveform moves around the circle. Thus a complete cycle is equivalent to 360° or 2π radians. The instantaneous position on the circle represents the phase at that given moment relative to the beginning of the cycle.

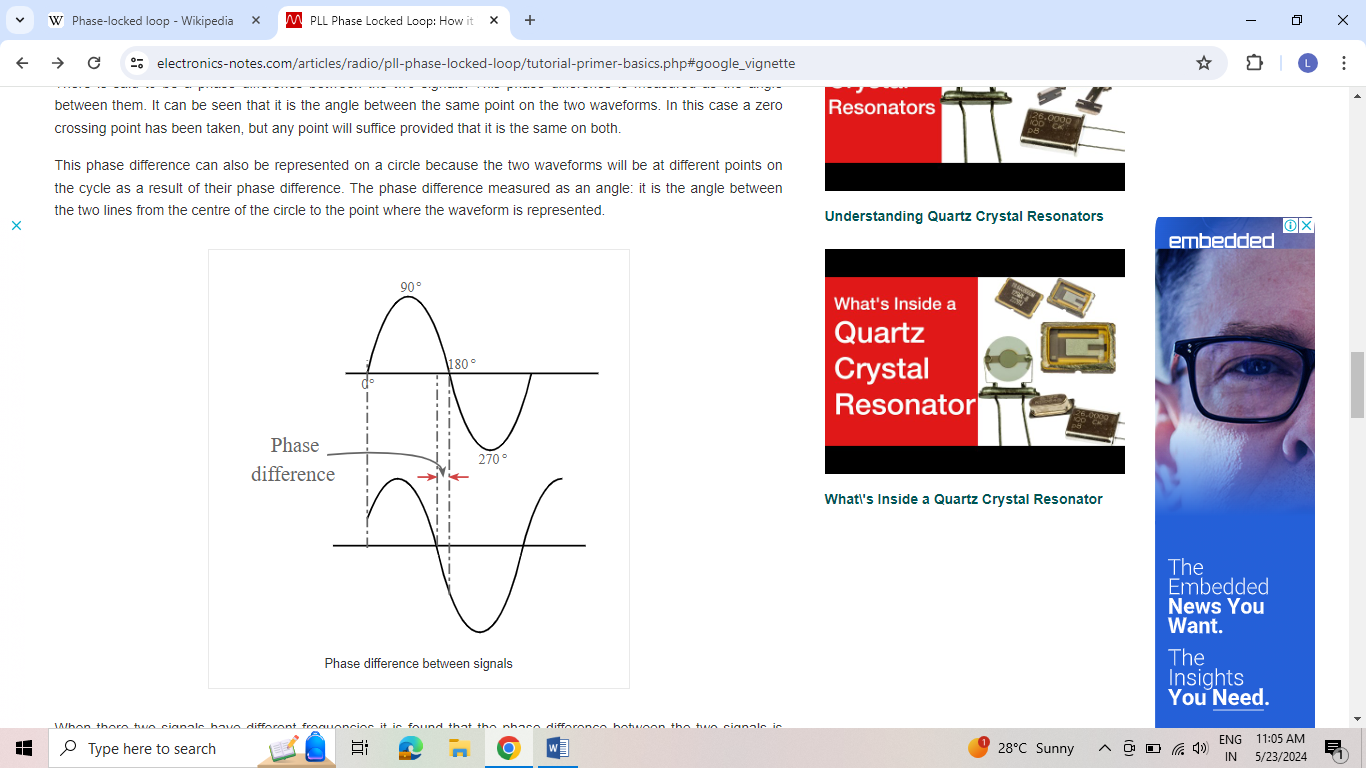


Fig.1.5 Phase difference between signals

When there two signals have different frequencies it is found that the phase difference between the two signals is always varying. The reason for this is that the time for each cycle is different and accordingly they are moving around the circle at different rates.

It can be inferred from this that the definition of two signals having exactly the same frequency is that the phase difference between them is constant. There may be a phase difference between the two signals. This only means that they do not reach the same point on the waveform at the same time. If the phase difference is fixed it means that one is lagging behind or leading the other signal by the same amount, i.e. they are on the same frequency.

# 1.6 Voltage Controlled Oscillator

A voltage-controlled oscillator (VCO) is an [electronic oscillator](https://en.wikipedia.org/wiki/Electronic_oscillator) whose [oscillation](https://en.wikipedia.org/wiki/Oscillation) [frequency](https://en.wikipedia.org/wiki/Frequency) is controlled by a [voltage](https://en.wikipedia.org/wiki/Voltage) input. The applied input voltage determines the instantaneous oscillation frequency. VCO is also an integral part of a [phase-locked loop](https://en.wikipedia.org/wiki/Phase-locked_loop). VCOs are used in [synthesizers](https://en.wikipedia.org/wiki/Synthesizer) to generate a [waveform](https://en.wikipedia.org/wiki/Waveform) whose [pitch](https://en.wikipedia.org/wiki/Pitch_(music)) can be adjusted by a voltage determined by a [musical keyboard](https://en.wikipedia.org/wiki/Musical_keyboard) or other input.

## 1.6.1 Voltage Controlled Oscillator in 5G

* **LC-VCO (Inductor-Capacitor VCO):** This is a fundamental VCO design that utilizes an inductor (L) and capacitor © to create a resonant tank circuit. The control voltage tunes the resonance frequency of the tank, affecting the VCO’s output frequency. LC-VCOs offer good phase noise performance and are relatively simple to design. However, the quality factor (Q) of the inductor is crucial for achieving high performance at millimeter-wave frequencies used in 5G.
* **N-push VCO:** This topology builds upon the LC-VCO by adding a varactor diode in parallel with the capacitor. The varactor diode’s capacitance changes with the applied control voltage, enabling finer control over the oscillation frequency. N-push VCOs offer wider tuning ranges compared to basic LC-VCOs and are suitable for applications requiring flexibility in the output frequency.
* **Ring VCO:** This design utilizes a chain of inverting gain stages (like transistors) connected in a ring oscillator fashion. The output frequency is determined by the propagation delay through the chain. By adjusting the control voltage to individual stages or the overall bias current, the propagation delay and hence the output frequency can be controlled. Ring VCOs are known for their compact layout and low power consumption, making them attractive for integration in 5G devices. However, their phase noise performance can be inferior to LC-VCOs.

## ****1.6.2 Key Performance parameters of VCOs****

The designing of voltage controlled oscillator have several parameters that must be considered before the design starts. These defines the key performance parameters needed for the VCO.

* VCO tuning range: It is obvious that the voltage controlled oscillator must be able to tune over the range that the loop is expected to operate over. This requirement is not always easy to meet and may require the VCO or resonant circuit to be switched in some extreme circumstances.
* VCO tuning gain: The gain of the voltage controlled is measured in terms of volts per Hz (or V/MHz, etc). As implied by the units it is the tuning shift for a given change in voltage. The voltage controlled oscillator gain affects some of the overall loop design considerations and calculations.

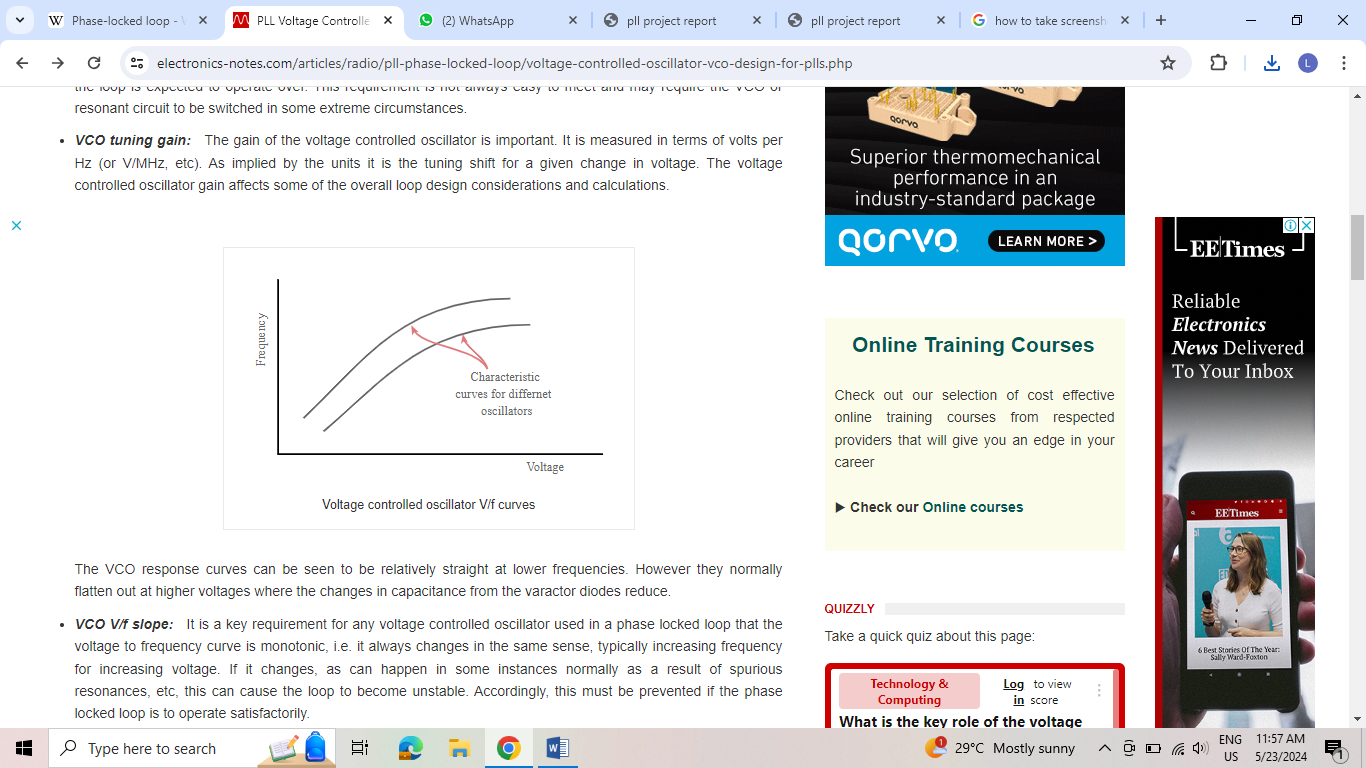


Fig.1.6 VCO Voltage versus frequency curves

* The VCO response curves can be seen to be relatively straight at lower frequencies. However they normally flatten out at higher voltages where the changes in capacitance from the varactor diodes reduce.
* VCOs Voltage versus frequency slope:   It is a key requirement for any voltage controlled oscillator used in a phase locked loop that the voltage to frequency curve is monotonic, i.e. it always changes in the same sense, typically increasing frequency for increasing voltage. If it changes, as can happen in some instances normally as a result of spurious resonances, etc, this can cause the loop to become unstable. Accordingly, this must be prevented if the phase locked loop is to operate satisfactorily.

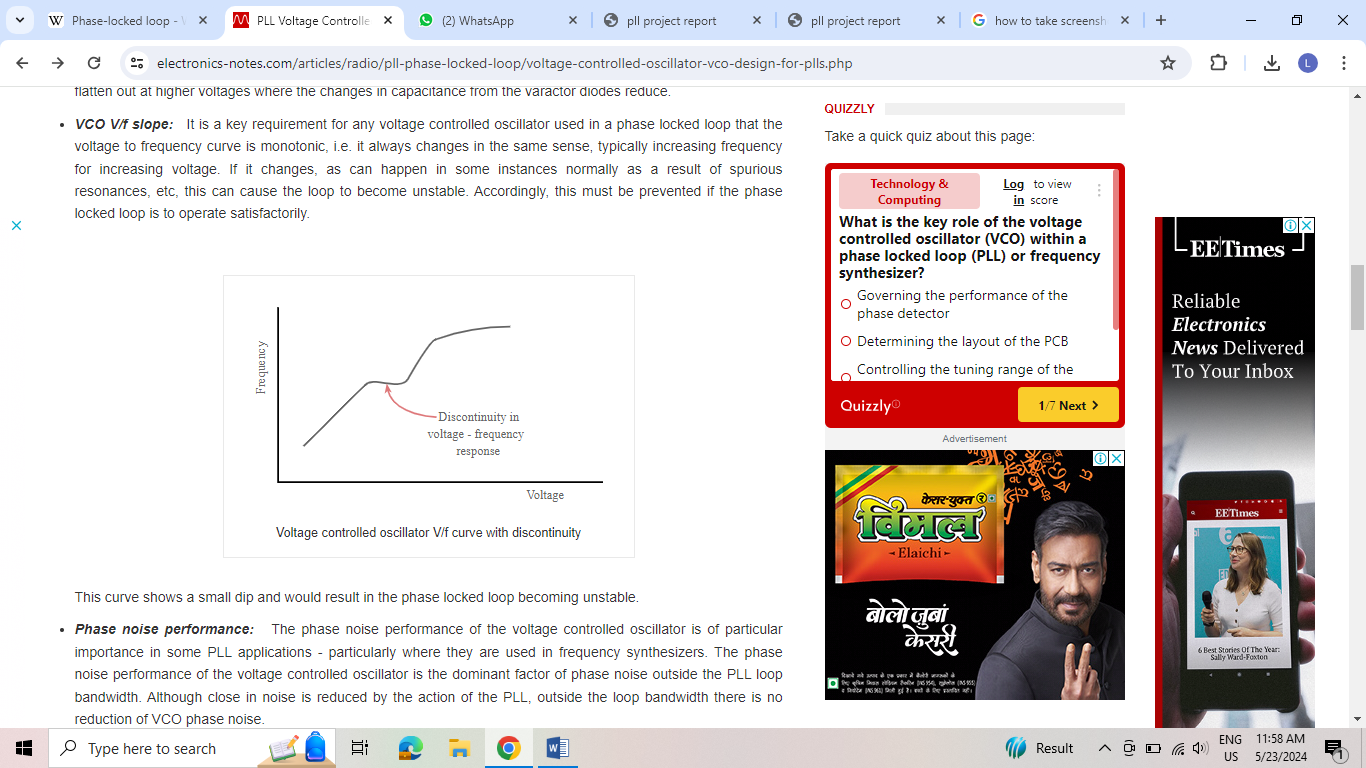


Fig.1.7 VCO voltage versus frequency curve with discontinuity

* This curve shows a small dip and would result in the phase locked loop becoming unstable.
* Phase noise performance:   The phase noise performance of the voltage controlled oscillator is of particular importance in some PLL applications – particularly where they are used in frequency synthesizers. The phase noise performance of the voltage controlled oscillator is the dominant factor of phase noise outside the PLL loop bandwidth. Although close in noise is reduced by the action of the PLL, outside the loop bandwidth there is no reduction of VCO phase noise.
* These are some of the main requirements that need to be known from the outset of the design of the VCO. Careful optimisation of the Q of the tuned circuit, especially using varactor diodes with as high a Q as possible, choice of active device, optimisation of the feedback within the oscillator.

## 1.6.3 VCO feedback

A VCO may be considered as an amplifier and a feedback loop. The gain of the amplifier may be denoted as A and the feedback as B. For the circuit to oscillate the total phase shift around the loop must be 360° and the gain must be unity. In this way signals are fed back round the loop so that they are additive and as a result, any small disturbance in the loop is fed back and builds up. In view of the fact that the feedback network is frequency dependent, the build-up of signal will occur on one frequency, the resonant frequency of the feedback network, and a single frequency signal is produced.

Many oscillators and hence VCOs use a common emitter circuit. This in itself produces a phase shift of 180°, leaving the feedback network to provide a further 180°.Other oscillator or VCO circuits may use a common base circuit where there is no phase shift between the emitter and collector signals (assuming a bipolar transistor is used) and the phase shift network must provide either 0° or 360°. For the oscillator to oscillate on a given frequency, the system includes a resonant circuit to ensure that the oscillation occurs on a given frequency. The resonant circuit can be one of a number of configurations from an LC resonant circuit in either series or parallel resonance dependent upon the circuit, or a quartz crystal, etc.

## 1.6.4 Choice of VCO active device

Bipolar devices and FETs both can be used within a VCO, using the same basic circuit topologies. The bipolar transistor has a low input impedance and is current driven, while the FET has a high input impedance and is voltage driven. The high input impedance of the FET is able to better maintain the Q of the tuned circuit and this should give a better level of performance in terms of the phase noise performance where the maintenance of the Q of the tuned circuit is a key factor in the reduction of phase noise.

Another major factor is the flicker noise generated by the devices. Oscillators are highly non-linear circuits and as a result the flicker noise is modulated onto VCO as sidebands and this manifests itself as phase noise. In general, bipolar transistors offer a lower level of flicker noise and as a result VCOs based around them offer a superior phase noise performance.

# 1.7 Current Reuse Oscillator

## 1.7.1 Designing of Current Reuse Oscillator

In NMOS or PMOS only topology, cross–connected pairs provide the negative conductance, which compensates loss in the LC-tanks. The current-reuse topology both PMOS and NMOS in the cross-connected configuration generates negative conductance. The series connection of PMOS and NMOS transistors helps in reducing the supply current to be half compared to that of the conventional NMOS or PMOS only topology while providing the same negative conductance. Additionally, this topology maintains balanced DC conditions neglecting the additional resistor Rs. Assuming the resistance Rs= 0, the current flows from supply voltage to ground through the tank inductor L when both the transistors M1, M2 are in on state. The transistors are in on state during one-half of the oscillation time. During the second half time, the transistors are off and the current flows in the opposite direction through the drain node capacitances of the transistors. The main difference between the conventional cross pair NMOS only and current reuse topology is that in the former the switching of transistors takes place alternatively while in the latter case switching of transistors occur at the same time. To reduce the swing of the transistor in the voltage-limited regime, a series resistor Rs is added to the topology to reduce the swing greater than the supply limits during the second half time when transistors are in off state. The voltage swing during on state of the transistors is minimum and a large amount of dynamic current flow through the transistors. On the other hand, the voltage swing is maximum when transistors are off due to the voltage limited regime operation.

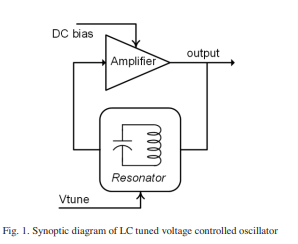


Fig.1.8 Synoptic diagram of LC tuned VCO

The voltage dependence of the capacitance can be expressed as

……………………………………………………………………………………(i)

where C0 is the zero-bias value, VR the reverse-bias voltage, ϕB the built in potential of the junction, m is the grading. Coefficient depends on the technology. Thus the varactor allows us to tune the capacitance form Cmin to Cmax.

# 1.8 Key characteristics

**Power Efficiency**: By reusing current across multiple transistors, CROs significantly reduce power consumption.

**Phase Noise Reduction**: Enhanced design techniques, such as adaptive control of transistor operation, improve phase noise performance.

**Wide Tuning Range**: Incorporating both coarse and fine tuning mechanisms allows for a broad frequency range, suitable for applications like 5G.

**Compact Design**: The efficient use of current and integrated components enables a more compact circuit layout.

**Enhanced Performance**: Improved start-up conditions and stability are achieved through advanced control techniques.

These features make CROs ideal for high-frequency and power-sensitive applications, particularly in modern communication systems.

Current reuse oscillators offer several advantages:

**Enhanced Power Efficiency**: By reusing current across multiple stages, CROs consume less power compared to traditional oscillators.

**Improved Phase Noise**: Advanced design techniques reduce phase noise, leading to better signal stability and clarity.

**Wider Tuning Range**: CROs can achieve a broad frequency tuning range, making them versatile for various applications.

**Compact Design**: Efficient current use and integrated components result in smaller, more compact circuit designs.

**Cost-Effective**: Lower power consumption and smaller size contribute to overall cost savings in both production and operation.

Here are the working steps of a current reuse oscillator:

**Initialization**: Apply the supply voltage to the oscillator circuit.

**Current Flow**: The current from the power supply flows through both the PMOS and NMOS transistors in the circuit.

**Oscillation Initiation**: The complementary arrangement of PMOS and NMOS transistors facilitates the start of oscillation by creating a regenerative feedback loop.

**Current Reuse**: The same current is reused in both transistors, reducing overall power consumption.

**Tuning**: Coarse and fine tuning mechanisms adjust the frequency of oscillation.

**Adaptive Control**: Adjust the transconductance and biasing of transistors to optimize performance under different conditions.

**Output Generation**: The oscillator produces a stable output signal with reduced phase noise and a wide tuning range.

# 1.9 Optimization parameters of VCO

**Power**

P = Vdd Idd..………………………………………………………………….…………………………………………..(ii)

Where:

P is the power consumption in watts (W).

Vdd is the supply voltage in volts (V).

Idd is the supply current in amperes (A).

This formula provides the power consumed by the VCO when it is operating at a given supply voltage and current. Optimizing the VCO involves minimizing Idd while maintaining adequate performance to reduce overall power consumption.

**FOM (Figure of Merit)**

FOM stands for Figure of Merit, which is a metric used to evaluate the performance of oscillators, particularly Voltage-Controlled Oscillators (VCOs). The Figure of Merit is a useful measure because it combines multiple key performance parameters into a single value, allowing for quick comparisons between different oscillator designs.

Figure of Merit is typically defined as the ratio of the oscillation frequency to a specified noise metric. The most commonly used noise metric for VCOs is phase noise, which quantifies the spectral purity of the oscillator’s output signal.

It is a valuable tool for oscillator designers because it allows them to quickly assess the trade-offs between frequency and noise performance in different VCO designs. By optimizing the circuit parameters to maximize the Figure of Merit, designers can achieve oscillators with improved spectral purity and frequency stability, which is crucial for applications such as communication systems, radar systems, and frequency synthesizers.

The figure of merit (FOM) for a voltage-controlled oscillator (VCO) is a key performance metric that combines phase noise, power consumption, and oscillation frequency. It is calculated using the following formula:

………………………………..…..…………(iii)

Where:

* + - Freq is the oscillation frequency.
    - Power is the power consumption.
    - PN is the phase noise.

This formula evaluates the oscillator’s efficiency, balancing phase noise reduction against power consumption and frequency.

**Area**

If you’re looking for a simplified formula to estimate the area of a Voltage-Controlled Oscillator (VCO) circuit on an integrated circuit (IC), it’s important to note that there isn’t a single universal formula due to the complexity and variability of VCO designs. However, I can outline some factors that contribute to the overall area of a VCO circuit:

**Transistor Count**: The number of transistors used in the VCO circuit, along with their sizes, plays a significant role in determing the area.

**Capacitors and Inductors**: The area occupied by capacitors and inductors used in the VCO circuit also contributes to its overall size.

**Interconnects**: The routing of signals between different components in the VCO circuit requires metal layers, vias, and routing space, which adds to the area.

**Technology Node**: The fabrication process and technology node used to manufacture the IC affect the minimum feature sizes and interconnect densities, which in turn influence the overall area.

**Layout Efficiency**: How efficiently the components are laid out on the chip can impact the final area. Careful placement and routing can reduce wasted space and minimize parasitic effects.

Given these factors, a simple formula to estimate the area of a VCO circuit could be:

Area= k x (Ntransistors x Atransistors + Ncapacitors x Acapacitors + Ninductors x Ainductors) + Interconnected area

Where,

* + k is a scaling factor for layout efficiency and technology specific considerations.
  + Ntransistors, Ncapacitors, and Ninductors are the number of transistors, capacitors, and inductors respectively in the circuit.
  + Atransistors , Acapacitors and Ainductors are the average area occupied by the transistors, capacitors, and inductors respectively.

Noise in a Voltage-Controlled Oscillator (VCO) can be quantified in various ways, and there are several formulas and expressions used to characterize different types of noise. Here, I’ll provide formulas for two common types of noise in VCOs: phase noise and flicker noise.

* **Phase Noise**:

Phase noise is often expressed in terms of its spectral density, typically measured in dBc/Hz (decibels relative to the carrier per Hz of bandwidth) at a given offset frequency from the carrier. The phase noise spectral density \( L(f) \) at a frequency offset \( f \) from the carrier can be approximated by the Leeson’s formula:

L(f) = Losc +10log10 (f / fosc) + . (f / fosc )2 **……………………………………………………………..(iv)**

Where:

Losc is the offset indeendent phase noise at a given offset.

fosc  is the oscillation frequency of the VCO.

is the noise corner parameter, representing the slope of the phase noise spectrum.

* **Flicker Noise (1/f Noise):**

Flicker noise, also known as 1/f noise, is often expressed in terms of its spectral density( S(f) ), typically measured in dBc/Hz. Flicker noise spectral density can be modeled by a power-law dependence on frequency:

……………………………………………………………………..(v)

Where:

K is a constant that depends on the specific technology and opearting conditions.

is a noise exponent which ranges between 1 and 2 flicker noise.

### 

### 

### Chapter 2

Literature Review

1. Current Reuse Oscillator Design for 5G Mobile Application using 90nm CMOS, K.A. Karthigeyan and S. Radha [IEEE 2022].

This paper presents a current reuse oscillator designed for 5G millimeter band frequencies. The designed was VCO simulated with low-Q inductor on-chip CMOS integration. The oscillator generates a signal of 440mV amplitude running at 27. 7S GHz with the phase noise of -102.5dBc and 550 mV amplitude running at 40 GHz with the phase noise of-103.6 dBc at lMHz carrier offset. The oscillator circuit designed from a 1V supply drawing bias currents of 1.5 mA and 1 mA DC current for the lowest and highest frequency band operation.

[2]. Design of Millimeter Wave LC Oscillators for 5G Applications, Shravan Ramesh, Nithin M and Harish M Kittur [IEEE 2019].

This paper deals with the design of various LC oscillators around 25 GHz which can be used for millimeter wave CMOS radios. Cross coupling is a standard technique used in oscillators and the losses in an LC tank is replenished by the negative resistance of the cross coupled circuit. This paper utilizes cross coupling technique to design oscillators centred around 25 GHz. Four topologies of oscillators are designed in 90nm CMOS technology with a peak to peak output swing of 800mV from a 1.2V supply. The design uses a non ideal inductor modeled with parasitic elements. The simulated phase noise results with the non ideal inductor is around - 97 dBc / Hz at an offset of 1 MHz and the total power consumption is around 60 μW.

[3]. Current reuse RF LC-VCO design for autonomous connected objects, ENIS, University of Sfax, Sfax, Tunisia [IEEE 2018].

In this paper, a fully integrated sub-mW current-reuse LC voltage controlled oscillator (VCO) is presented. It is designed by following a design methodology to find the optimal parameters lowering the power consumption. The implemented LC-VCO is successfully demonstrated through its silicon prototype in 130nm CMOS technology. It consumes only 262μ W from 1V supply voltage making it suitable for autonomous connected objects and IoT applications.

[4]. Low Power Current-reused Voltage-Controlled Oscillator with Optimum Source Damping Resistors, Chien-Hsuan Liu, Chia-Yo Chan, Ruey-Lue Wang, and Yun-Kuin Su [IEEE 2007].

In this paper, a low power current-reused voltage-controlled oscillator with source damping resistors is presented. It is designed by simulating optimum value of resistors. According to the simulation results, the output signals are symmetric and the 1/f 3 region of the phase noise is reduced. The VCO 1 is designed at 2.26 GHz. The measured phase noise at 100-kHz and 1-MHz offset frequencies are -101.87 and -121.66 dBc/Hz. With 1.8 V voltage supply, the power consumptions of the VCO is 1.62 mW. This circuit is fabricated by TSMC 0.18 um CMOS process.

[5]. Design and Study the Performance of a CMOS-Based Ring Oscillator Architecture for 5G Mobile Communication ,Abdul Rahman ,Siddharth Kishore, A. R. Abdul Rajak 1.

The paper presents a novel Complementary Metal Oxide Silicon (CMOS) ring oscillator that serves as a Voltage Controlled Oscillator. The suggested architecture utilizes the advantages of both a current-starved ring oscillator and a negative-skewed delay by combining their constituent parts. The proposed architecture has a control voltage of 1.15 V and a supply voltage of 2 V, generating a 9.35 GHz dominant frequency with a 13.82% harmonic distortion between the inputs and outputs. The proposed architecture can implement 5G-based applications that require high frequency and low power by carefully selecting the passive components within the design.

[6]. Design of low phase noise and low power modified current-reused VCOsfor 10 GHz applications, Meng-Ting Hsu a,b,n, Wei-Jhih Li b, Chien-Ta Chiu b.

The traditional current-reused circuit with a wide tuning range of 17.2% is presented in the first chip. It has a phase noise-118 dBc/Hz at 1 MHz offset and 5 mW core power dissipation with a voltage supply under 1.5 V. The performance of FOM is as high as −191.8 dBc/Hz. Extra NMOS cross-coupled pairs inside the traditional current-reused circuit in the second chip is proposed to speed up the oscillation and stability. The phase noise is −106.19 dBc/Hz and the core power dissipation is 3 mW with a voltage supply under 1.5 V. For the third chip, two dc level shifters are adopted to improve the symmetry of the output signal and to decrease noise interference. The phase noise and core power are -106.9 dBc/Hz and 2.88 mW, respectively. It also has a high performance of FOM with −182.4 dBc/Hz.

[7]. Low-power low-phase noise VCO for 24 GHz applications. pP anelAbrar Siddique, Tahesin Samira Delwar, Murod Kurbanov, Jee-Youl Ryu 2020.

The VCO has been implemented using 65 ​nm CMOS technology. The proposed VCO baised with 0.9 ​V and it showed the lowest power consumption of 1.35 ​mW and the lowest phase noise of −117 ​dBc/Hz at the 1 ​MHz offset frequency as compared to conventional results. This circuit also showed wide tuning range of 26.4%, low FOMT of −194.3 ​dBc/Hz, and small area in core die of 0.35 ​mm ​× ​0.35 ​mm. In addition, we have analyzed the mesaured output power spectrum of the proposed VCO using spectrum analyser (Anritsu, MS2760A) whereas the measured output power of the designed VCO is −7.9 dBm at the frequency of 24.5 ​GHz.

[8]. Design and Analysis of 15.8 GHz LC-VCO Using PMOS Cross Coupled, D. -X. Mai, S. Bui and T. -K. Nguyen, 2019 31st International Conference on Microelectronics (ICM).

This paper presents a design of low phase noise LC-VCO. A circuit using LC tank oscillator with PMOS cross coupled along with varactor in PMOS type is proposed. The VCO uses 5 bits for coarse and fine-tuning frequency. The post-layout simulation shows the frequency tuning range from 14.2 to 15.8 GHz has phase noise of -95 dBc/Hz, -114.5 dBc/Hz at 100 kHz and 1 MHz offset, respectively. The circuit is designed based on 28nm process under supply voltage of 0.9 V and current consumption of 10 rnA.

[9]. Design of 6.7 GHz ˜ 7. 518 GHz Cross Coupled LC-VCO in 180nm CMOS technology, S. S. S and S. S. Yellampalli,2021 5th International Conference on Computing Methodologies and Communication (ICCMC).

This paper discusses the analysis and design of LC VCO in 180nm CMOS technology with 7 GHz resonating frequency using Cadence Virtuoso environment. The designed circuit works at 1.8 V supply voltage. VCOs are the main component of PLL that is used in the generation of IR pulses in UWB systems. The designed LC - VCO with a bandwidth of 6.711 GHz - 7.518 GHz is to be used in the IR-UWB system that generates short pulses using indirect IR-UWB method. The gain K of LC VCO designed was 484 Mhz/V. The output power P (mw) was 2.25mw. The observed Phase noise at 1MHz is -103.2dbc/Hz and at 10 MHz is -131.5dbc/Hz. The resonating frequency was verified using PSS analysis, which gives a resonating frequency of 7 GHz. The FOM of the designed VCO is - 136.98 8 dbc/Hz.

[10]. An advanced low power low noise 2.45 ghz current Reuse -gm cmos cross coupled vco for wsn . Arnov Mukherjee1, Pankaj Rangaree2 ,Dr.G.M.Asutkar3.

The VCO proposed in the paper consists of a single on chip inductor with four MOS transistors that simplify the schematic, shrink the chip area remarkably and low down the power consumption to a great extent as well. This paper presents an advanced low power low noise 2.45 GHz current reuse -Gm CMOS cross coupled VCO for WSN applications. The proposed current reuse VCO is designed with 0.13µm CMOS process. At supply of 1 V DC, the proposed VCO draws only 350 µA current resulted into the VCO to operate at an ultra low power of only 0.35 mW. Over the tuning range of 2.45GHz the proposed VCO have phase noise of -126.89 dBc/Hz at 1.1 MHz offset frequency. The tuning voltage (Vtune) is set to be 1V for 2.45 GHz ISM frequency band applications. The proposed VCO shows excellent performance optimization for low power and low phase noise of compact transceiver system for WSN.

### Chapter 3

Methodology

### Two Types of Voltage Controlled Oscillators

* **Harmonic Oscillators**: The output is a signal with a sinusoidal waveform.

Examples are crystal oscillators and tank oscillators.

* **Relaxation Oscillators**: The output is a signal with a sawtooth or triangular waveform and provides a wide range of operational frequencies. The output frequency depends on the time of charging and discharging of the capacitor.

# 3.1 Ring Oscillator

Ring oscillator is an odd number of inverters are connected in a series form with positive feedback & output oscillates between two voltage levels either 1 or zero to measure the speed of the process. In place of inverters, we can define it with NOT gates also. These oscillators have an ‘n’ odd number of inverters. For instance,  if this oscillator has 3 [inverters](https://www.elprocus.com/what-is-an-inverter-types-circuit-diagram-applications/) then it is called a three-stage ring oscillator. If the inverter count is seven then it is seven stage ring oscillator. The number of inverter stages in this oscillator mainly depends on the frequency which we want to generate from this oscillator.

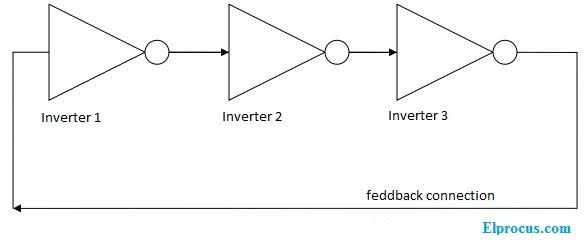


Fig.3.1 Ring-oscillator block diagram

The designing of the ring oscillator can be done using three inverters. If the oscillator is employed with a single-stage, then the oscillations & gain are not sufficient. If the oscillator has two inverters, then the oscillation and gain of the system are a little bit more than the single-stage ring oscillator. So this three-stage oscillator has three inverters that are connected in the form of series with a positive feedback system. So the oscillations & the gain of the system are sufficient. This is the reason to choose the three-stage oscillator.

The inverter gives a delay to the input signal and if the numbers of inverters are increases then oscillator frequency will be decreased. So the desired oscillator frequency depends on the number of inverter stages of the oscillator.

The s frequency of oscillation formula for this oscillator is

………………………………………………………………………………… (vi)

T = time delay for single inverter

n = number of inverters in the oscillator

### Ring Oscillator using Transistor

The ring oscillator is a combination of inverters connected in a series form with a feedback connection. And the output of the final stage is again connected to the initial stage of the oscillator. This can be done through the transistor implementation also. The below figure shows the ring oscillator implantation with a [CMOS transistor](https://www.elprocus.com/the-fabrication-process-of-cmos-transistor/).

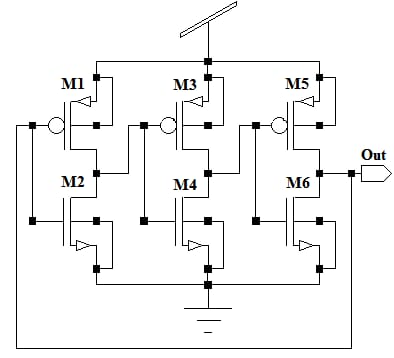


Fig.3.2 Ring Oscillator design

### Applications

### A few****applications of this oscillator**** will be discussed here. They are

* These are used to measure the effect of voltage and temperature on an[integrated chip](https://www.elprocus.com/application-specific-integrated-circuits/).
* During wafer testing, these oscillators are preferred.
* In frequency synthesizers these oscillators are applicable.
* For data recovery purposes in serial data communications, these oscillators are useful.
* In [phase-locked loop (PLL)](https://www.elprocus.com/phase-locked-loop-operating-principle-and-applications/) the VCO’s can be designed by using this oscillator.

A [ring oscillator](https://en.wikipedia.org/wiki/Ring_oscillator) has been designed to generate the desired frequency in any condition. The frequency of oscillation is dependent on the number of stages and delay time of each inverter stage. And the effect of temperature and voltage of this oscillator can be tested in five conditions. In all the different test conditions if the temperature increases the time period of the output can be decreased compared with the least temperature value. We need to analyze the phase noise and jitter value if the temperature varies.

# 3.2 Current starved oscillator

Ring oscillators can be realized by a number of ways. As frequency of oscillations depends on delay introduced by each inverter stage so delay should be voltage controlled. One way to control the dealy is to control the amount of current available to charge or discharge the capacitive load of each stage. This type of circuit is called a current starved ring VCO. In this VCO basically the control voltage (Vctrl ) modulates the turn-on resistances of the pull-down transistor and pull-up transistors through a current mirror. These variable resistances control the current available to charge or discharge the load capacitances. Large value of Vctrl allows a large current to flow, producing a small resistance resulting into small delay. Current starved ring VCO uses variable bias currents to control its oscillation frequency.

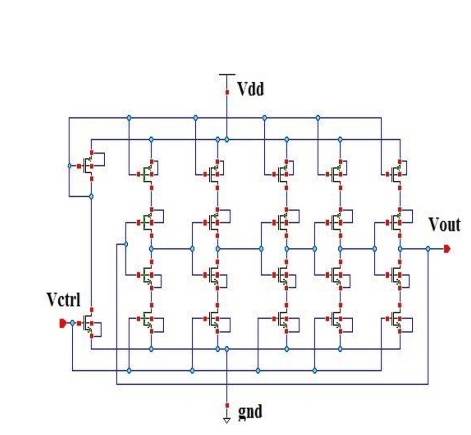


Fig.3.3 Current stared Oscillator design

The transistors M1 and M 2 operate as inverters while M 3 and M 4 operate as current sink and current source respectively. The current sources limit the current available to inverters. The drain currents of transistors M 5 and M 6 are same and set by the input control voltage (Vctrl ). The current in transistors M 4 and M 5 are mirrored from bias stage to each inverting stage. The bias circuit is used to provide correct polarization for transistor M3 and M 4 [6]. The benefit of this configuration is that the oscillation frequency can be tuned for a wide range by changing the value of control voltage. Fig. 3 shows the small signal equivalent model of a delay cell of starved ring VCO.

From the small signal equivalent model the incremental gain of current starved ring VCO can be given as

……………………………………………………………………………………....(vii)

The variation of control voltage (Vctrl) determines the frequency range and linearity of VCO. The major drawback of this stage is longer rise/fall time when bias current is quite small because the voltage swing of the VCO becomes slower. In addition to this, if bias current is increased then the voltage headroom of the current source MOS transistors becomes narrow. The oscillation frequency ( osc f ) is derived as follows. The total capacitance on the drains of M 3 and M 4 is given as.

………………………………………………………………………….(viii)

The oscillation frequency is determined by the bias current ( d I ), number of stages ( N ), total capacitance (Ctotal ) and control voltage (Vctrl ) as

………………………………………………………………………………(ix)

# 3.3 Cross coupled oscillator

A cross-coupled oscillator is a type of electronic oscillator circuit commonly used to generate high-frequency signals. It is often implemented using either bipolar junction transistors (BJTs) or metal-oxide-semiconductor field-effect transistors (MOSFETs). The basic principle of operation involves two amplifying devices (transistors) that are connected in such a way that they provide positive feedback to each other, sustaining oscillations. Here’s a detailed explanation of its working and design:

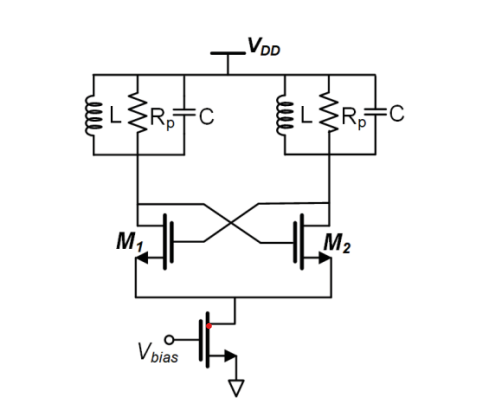


Fig.3.4 Cross Coupled Oscillator design

**Working Principle**

**Feedback Mechanism**: In a cross-coupled oscillator, two transistors are used, with the output of each transistor fed back to the input of the other. This positive feedback loop is crucial for sustaining oscillations.

**Start of Oscillations**: When power is initially applied, noise or a small signal in the circuit is amplified by the first transistor. This amplified signal is then fed back to the second transistor, which further amplifies it and feeds it back to the first transistor.

**Sustaining Oscillations**: The feedback loop ensures that the signal continues to build up until it reaches a steady-state amplitude. The frequency of oscillation is primarily determined by the reactive components (inductors and capacitors) in the circuit.

**Frequency Determination**: The resonant frequency of the LC tank circuit typically determines the frequency of oscillation. This can be given by the formula:

………………………………………………………………………………….……(x)

where L is the inductance and I is the capacitance.

**Design of Cross-Coupled Oscillator**

**Components**

A pair of identical transistors (MOSFETs) is used.

LC Tank Circuit: Consists of inductors and capacitors to set the oscillation frequency.

Biasing Resistors: To properly bias the transistors.

Coupling Capacitors: To allow AC signals to pass while blocking DC components.

Power Supply: To provide the necessary operating voltage for the transistors.

**Design Steps**

Choosing Transistors: Select transistors with sufficient gain and frequency response for the desired oscillation frequency.

LC Tank Circuit Design: Determine the desired frequency of oscillation and calculate the values of L and C using the resonant frequency formula. Choose components that can operate efficiently at the desired frequency.

Biasing Network: Design the biasing network to set the operating point of the transistors. This typically involves selecting appropriate resistor values to ensure that each transistor operates in its active region.

Coupling Mechanism: Connect the output of each transistor to the input of the other using capacitors. These capacitors should be chosen to have low reactance at the operating frequency to ensure effective coupling.

Power Supply: Ensure the power supply provides a stable voltage within the transistors’ operating range.

**Practical Considerations**

* **Component Tolerances**: Ensure components have tight tolerances for stable frequency.
* **Temperature Stability**: Consider temperature coefficients of components, especially inductors and capacitors, to maintain frequency stability.
* **Power Supply Noise**: Use a well-filtered power supply to minimize noise in the oscillator circuit.
* By following these principles and design steps, you can effectively design and understand the working of a cross-coupled oscillator suitable for your application.

# 3.4 Current reuse oscillator

A current reuse oscillator (CRO) is a type of electronic oscillator that aims to enhance power efficiency by reusing the same current in multiple active components. This technique is often employed in voltage-controlled oscillators (VCOs) to reduce power consumption while maintaining or improving performance metrics like phase noise and tuning range.

Recent advancements in CROs include designs for low-power, low-phase-noise applications suitable for 5G and IoT devices. For example, a CMOS VCO using a current-reuse structure has demonstrated significant improvements in power efficiency and phase noise, making it ideal for high-frequency applications in wireless communication systems. These designs often incorporate complementary PMOS and NMOS transistors to maximize current efficiency and employ adaptive control techniques to enhance performance under varying conditions.

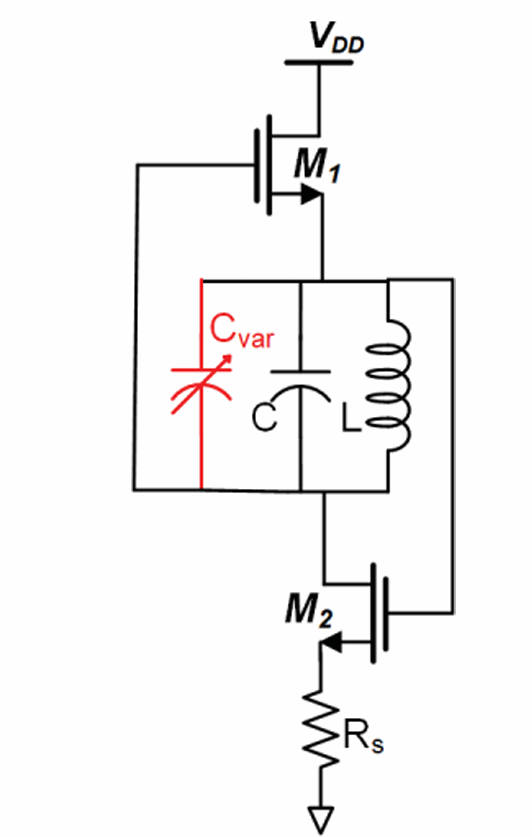


Fig 3.5 Current Reuse Oscillator

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### Chapter 4

Motivation

# 4.1 Reducing the Phase noise

Reducing phase noise in the design of Voltage-Controlled Oscillators (VCOs) for current reuse oscillator topologies in the 28 GHz range for 5G applications is crucial for several reasons:

1. **Signal Integrity**: Lower phase noise ensures higher signal integrity, which is essential for maintaining the quality of the transmitted and received signals in high-frequency 5G communications.
2. **Channel Interference**: 5G networks operate in densely packed frequency bands. Reduced phase noise minimizes interference between adjacent channels, which is critical for maintaining high-quality communication and reducing errors.
3. **Data Throughput and Reliability**: High phase noise can lead to increased bit error rates, degrading the modulation quality. Reducing phase noise improves data throughput and the reliability of high-speed data transmission in 5G networks
4. **Purity**: To comply with regulatory standards and to avoid interference with other systems, 5G transmitters must maintain high spectral purity. Lower phase noise contributes to a cleaner signal spectrum, meeting these stringent requirements.
5. **Noise Figure (NF)**: In current reuse topologies, the VCO’s phase noise performance significantly impacts the overall noise figure of the transceiver. Lower phase noise translates to a better noise figure, enhancing the receiver's sensitivity and dynamic range.
6. **System Performance**: Overall system performance, including the efficiency of signal processing and the robustness of communication links, is heavily influenced by the VCO’s phase noise characteristics. Reducing phase noise leads to more efficient and reliable system performance.
7. **Power Efficiency**: Current reuse topologies aim to maximize power efficiency by reusing the same current across multiple stages. Achieving low phase noise while maintaining power efficiency is challenging but crucial for the effective performance of 5G transceivers.
8. **Link Budget**: Lower phase noise improves the link budget by enhancing the signal-to-noise ratio (SNR), allowing for longer communication distances and better overall link quality.

# 4.2 Figure of Merit

Reducing the Figure of Merit (FoM) is generally preferred for the following reasons:

1. **Performance Enhancement**: Lower FoM indicates superior oscillator performance, balancing phase noise, power consumption, and operating frequency effectively.
2. **Energy Efficiency**: Decreasing FoM implies higher energy efficiency, crucial for battery-powered devices, reducing power consumption without sacrificing performance.
3. **Signal Quality**: A reduced FoM signifies lower phase noise, leading to higher signal quality and reliability, essential for applications like 5G communication.
4. **System Integration**: Optimal FoM facilitates smoother integration into complex systems, ensuring overall system performance and stability.
5. **Competitive Advantage**: Achieving a lower FoM gives a competitive edge by offering better-performing products with improved energy efficiency and signal integrity.

### Chapter 5

Software Requirements

# 5.1 Cadence



* Cadence Design Systems provides software and engineering services for electronic design automation (EDA), primarily used in the semiconductor and electronics industries.
* Founded in 1988, Cadence's tools are critical in designing integrated circuits (ICs), printed circuit boards (PCBs), and systems on chips (SoCs).
* Key software offerings include Virtuoso for analog design, Encounter (now Innovus) for digital design, and Allegro for PCB design. These tools help engineers design, simulate, and verify their electronic products, ensuring functionality and manufacturability.
* Cadence evolved from focusing on standalone EDA tools to offering a comprehensive suite that supports end-to-end design processes. Over the years, it has integrated advanced technologies such as machine learning and cloud computing into its solutions to enhance design efficiency and accuracy.
* The company also expanded into system-level design and verification with products like Palladium for hardware emulation and Protium for prototyping.
* These advancements reflect Cadence's commitment to addressing the complexities of modern electronics and facilitating the development of innovative, high-performance devices.

# 5.2 Ltspice

* LTspice, initially released by Linear Technology in 1999 as SwitcherCAD, focused on simulating power supply circuits.
* It was rebranded to LTspice in the early 2000s, expanding to general analog circuit simulation. The 2008 release of LTspice IV brought performance improvements and expanded libraries. Following Analog Devices' acquisition of Linear Technology in 2016, LTspice gained more component libraries and enhanced support. LTspice XVII, released in 2017, introduced multi-core support and a better user interface.
* LTspice is used for analog circuit simulation, power supply design, transient and AC analysis, noise analysis, and Monte Carlo simulations.
* It excels in designing DC-DC converters and linear regulators, ensuring circuits meet performance criteria. Its capability to simulate across various temperatures and analyze noise makes it essential for robust analog and power electronics design
* LTSpice is capable of performing types of analysis which are generally viewed as special cases of the three main types.  We outline them below. DC Sweep allows a series of DC operating points to be calculated while sweeping or incrementally changing the value of an independent current or voltage source. This analysis is used largely to determine the DC large-signal transfer characteristic. The Transfer Function analysis is related. It computes the small-signal DC gain from a specified input to a specified output, and the corresponding input and output resistance.
* In manner similar to DC Sweep, Temperature Analysis allows a series of analyses to be performed while varying the temperature of the circuit. Because the characteristics of many devices depend on temperature, this facility provides a useful tool for investigating the effect of temperature variation on circuit operation. Any of the above main analysis types can be performed in conjunction with Temperature Analysis, thus providing insight into temperature dependencies.
* Sensitivity Analysis indicates which components affect circuit performance most critically. There are several ways in which to investigate the impact of component tolerances on a specific circuit behaviour. One way is to perform a parameter sweep of a component value and observe the range of corresponding circuit behaviour. Another is to assign a set of random numbers to different circuit components having either a Gaussian or uniform distribution and observe the overall statistical behaviour of the circuit subject to various stimuli. The latter analysis is known as a Monte Carlo Analysis. Finally, Noise and Fourier Analysis procedures calculate the dynamic range of a circuit.
* Noise analysis calculates the noise contribution of each element, injects its effect back into the circuit and calculates its total effect on the output node in a mean-square sense. The Fourier analysis computes the Fourier series coefficients of the circuit's voltages or currents with respect to the period of the input excitation.

### Chapter 6

Implementation

# 6.1 Ring Oscillator design

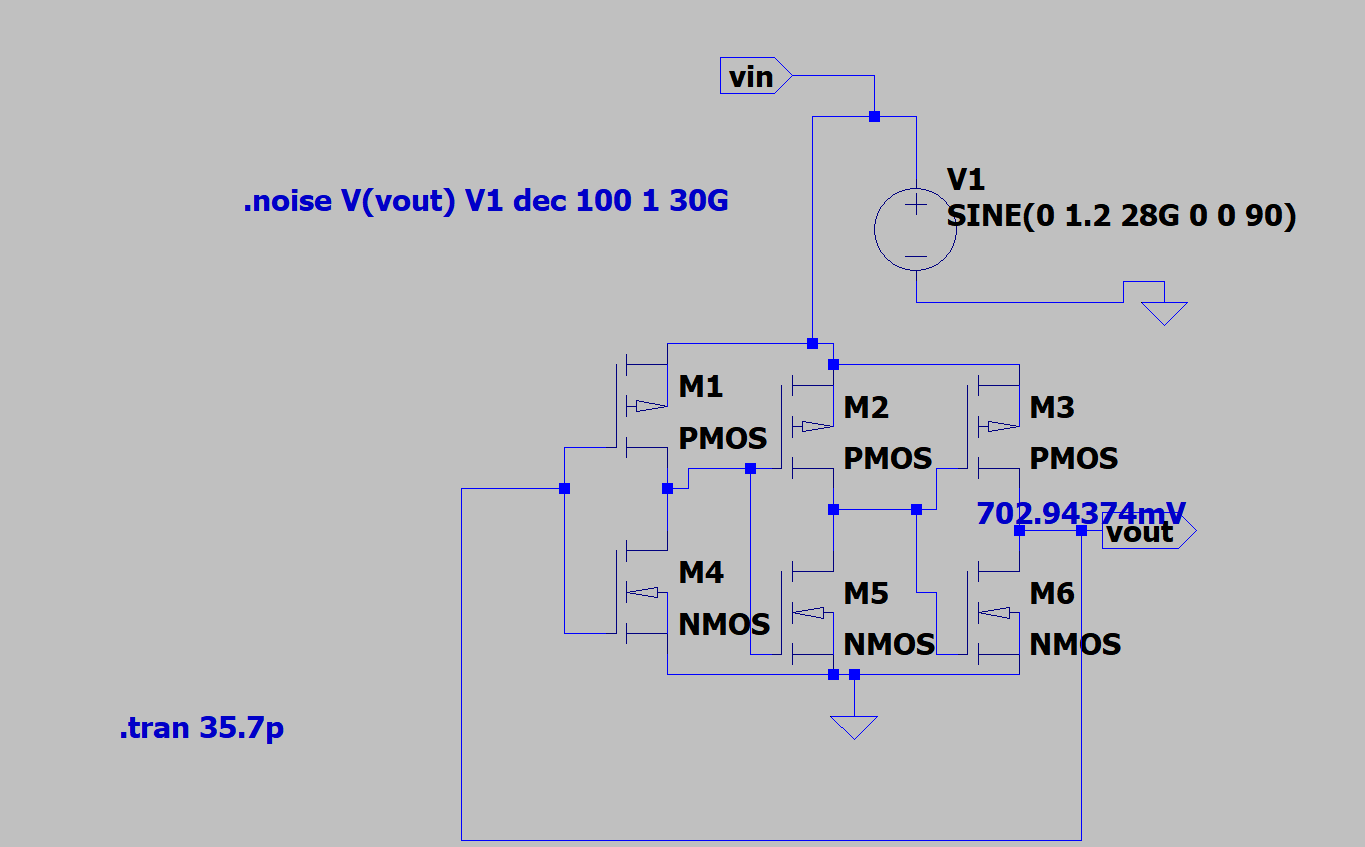


Fig 6.1 Ring Oscillator design

* Ring oscillator is a **Simple Design c**omposed of an odd number of inverters in a loop, ring oscillators are easy to design and implement, requiring minimal components.

# 6.2 Current starved Oscillator design

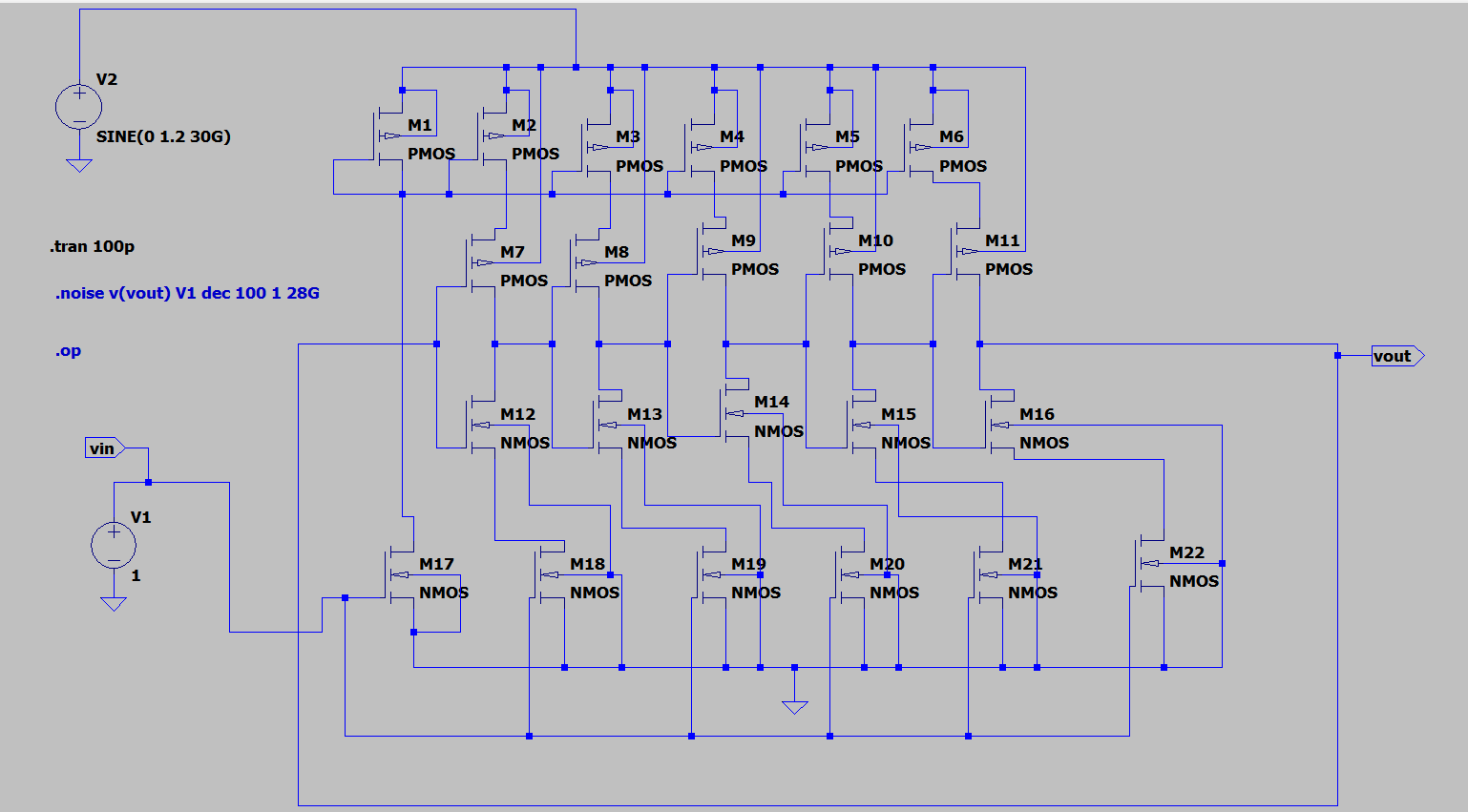


Fig 6.2 Current starved Oscillator design

* Current starved Oscillator provides **Precise Control** Utilizes current mirrors to control the charging and discharging currents, allowing for fine-tuning of the oscillation frequency.

# Cross coupled Oscillator design

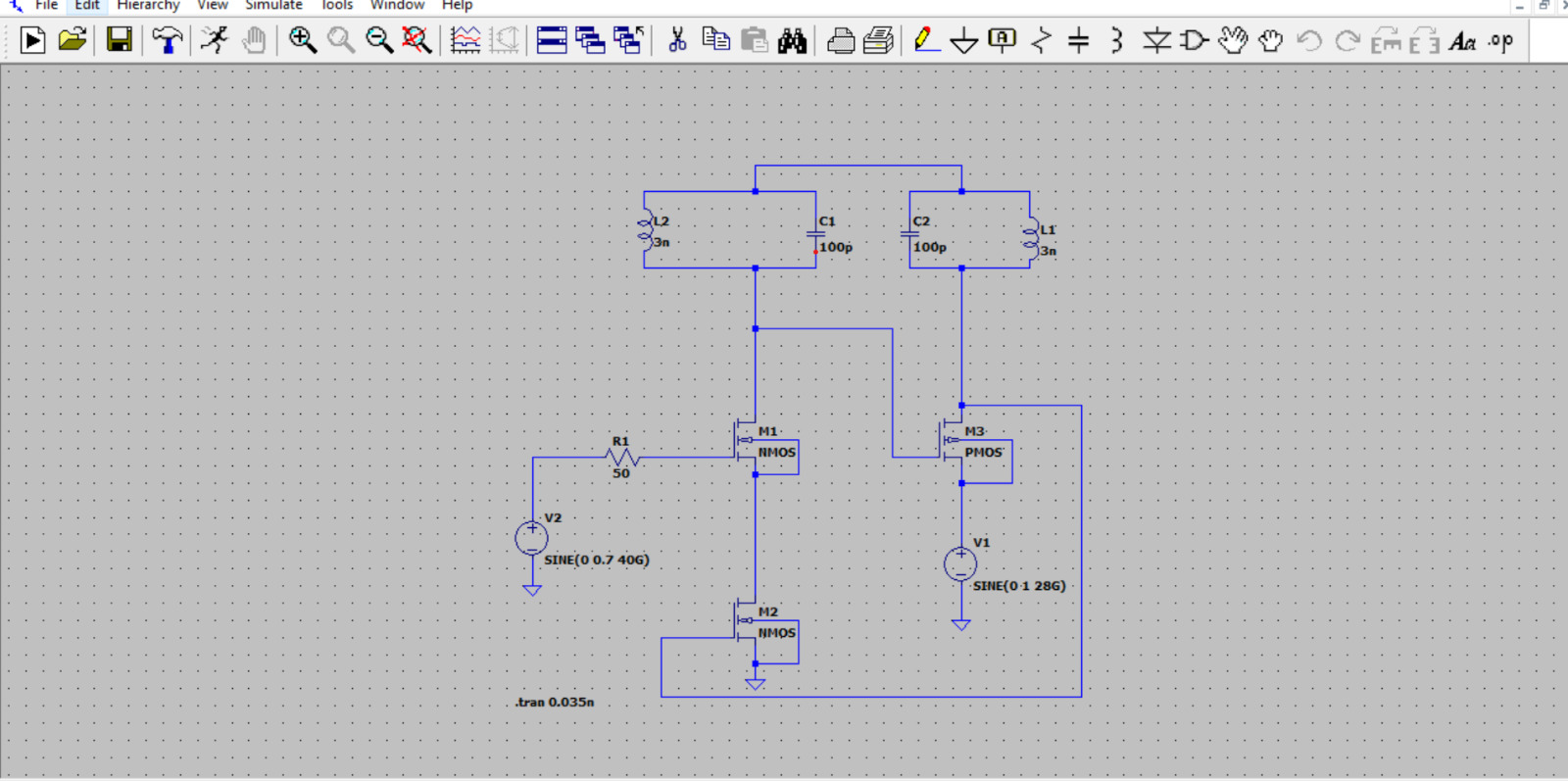


Fig 6.3 Cross Coupled Oscillator design

The cross-coupled oscillator topology is characterized by several design elements:

* **Tank Circuit**: It typically includes an LC tank circuit, which consists of an inductor (L) and a capacitor (C) that determine the oscillation frequency.
* **CMOS Technology**: Often implemented using CMOS technology, which offers low power consumption and is suitable for integration into modern integrated circuits.
* **Cross-Coupled Transistors**: The core of the oscillator consists of a pair of cross-coupled transistors (usually NMOS or PMOS), which provide the necessary feedback to sustain oscillations.
* **Differential Pair**: It features a differential pair configuration, producing two outputs that are 180 degrees out of phase, improving noise rejection and signal integrity.
* **Biasing Network**: Includes a biasing network to set the operating point of the transistors, ensuring stable operation across varying conditions.

# Current reuse Oscillator

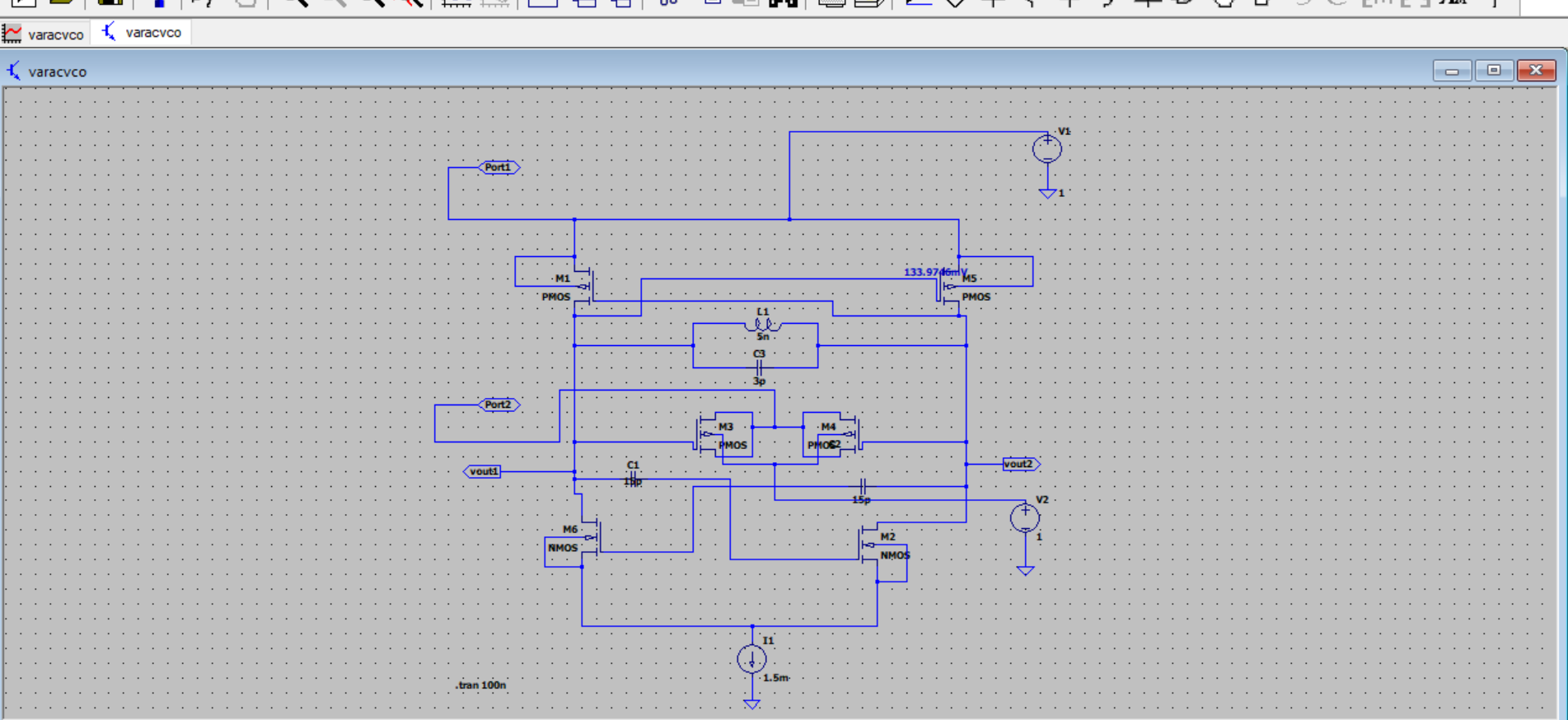


Fig.6.4 Current reuse design

The current reuse oscillator topology has several design characteristics:

* **Tank Circuit**: Like the cross-coupled oscillator, it employs an LC tank circuit (inductor L and capacitor C) to set the oscillation frequency.
* **CMOS Technology**: Often realized in CMOS technology to leverage its low power consumption and ease of integration into modern integrated circuits.
* **Current Reuse**: The core feature is the reuse of bias current through a stacked transistor configuration (typically one NMOS and one PMOS transistor). This stacking allows the same current to flow through both transistors, improving power efficiency.
* **Differential Operation**: It often uses a differential pair to provide balanced outputs that are 180 degrees out of phase, enhancing noise rejection and signal integrity.
* **Shared Biasing Network**: A shared biasing network is used to set the operating points of the transistors, maintaining stable operation while reusing current, which is crucial for reducing power consumption.

### Chapter 7

Result Analysis

# 7.1 Simulation

## 7.1.1 Ring Oscillator

**Simulation of Ring Oscillator design:**

Fig 7.1 Ring Oscillator transient response

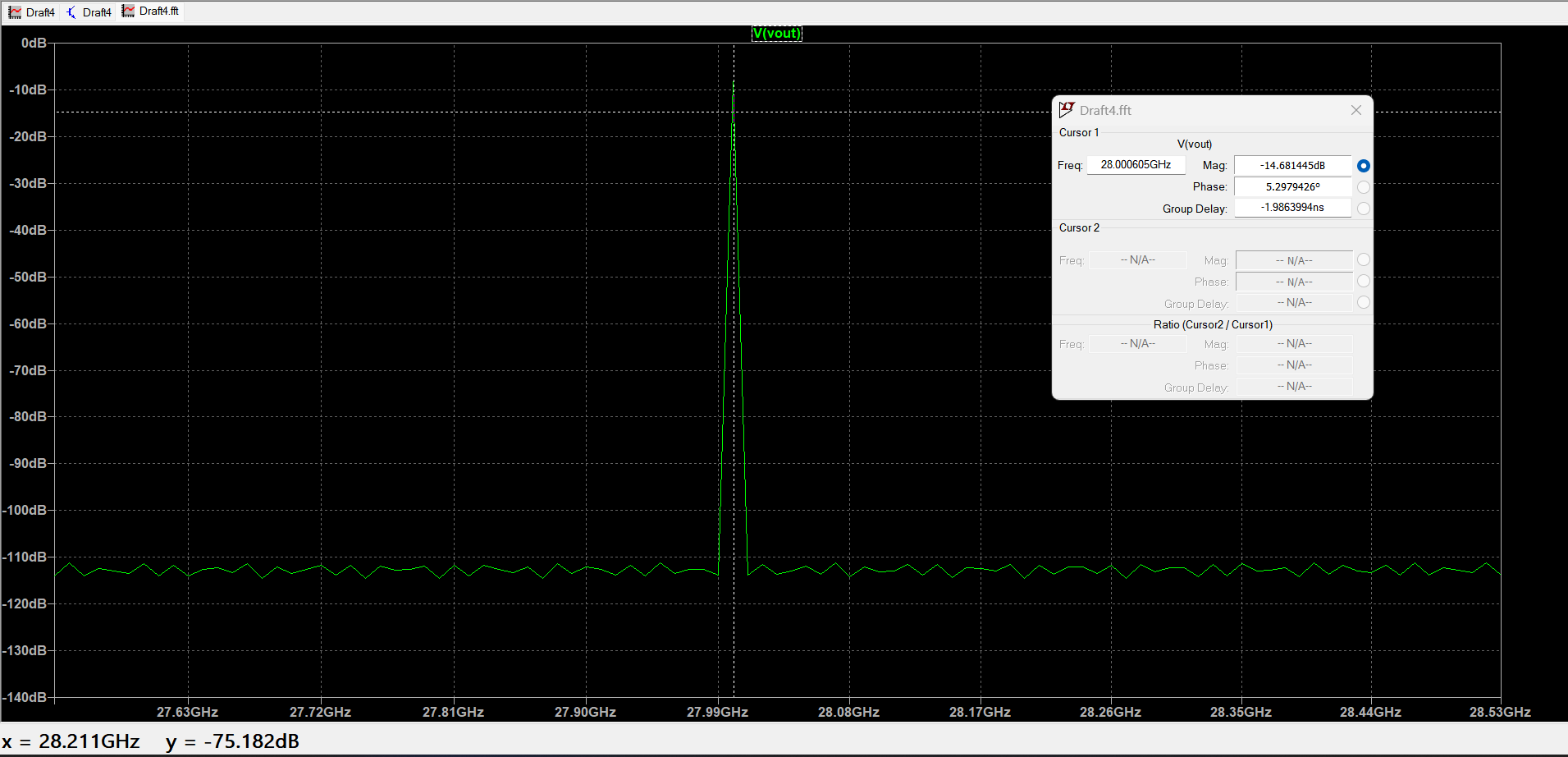


Fig 7.2 Ring Oscillator frequency fft response

* **It has High Frequency Tuning Range it** offers a wide tuning range of frequencies by adjusting the supply voltage or load capacitance, making it versatile for various applications.
* Provides the oscillation for 28G frequency with the phase noise of -124.2dB at 1M Hz with FoM of -206.8dBc/Hz

## 7.1.2 Current starved Oscillator

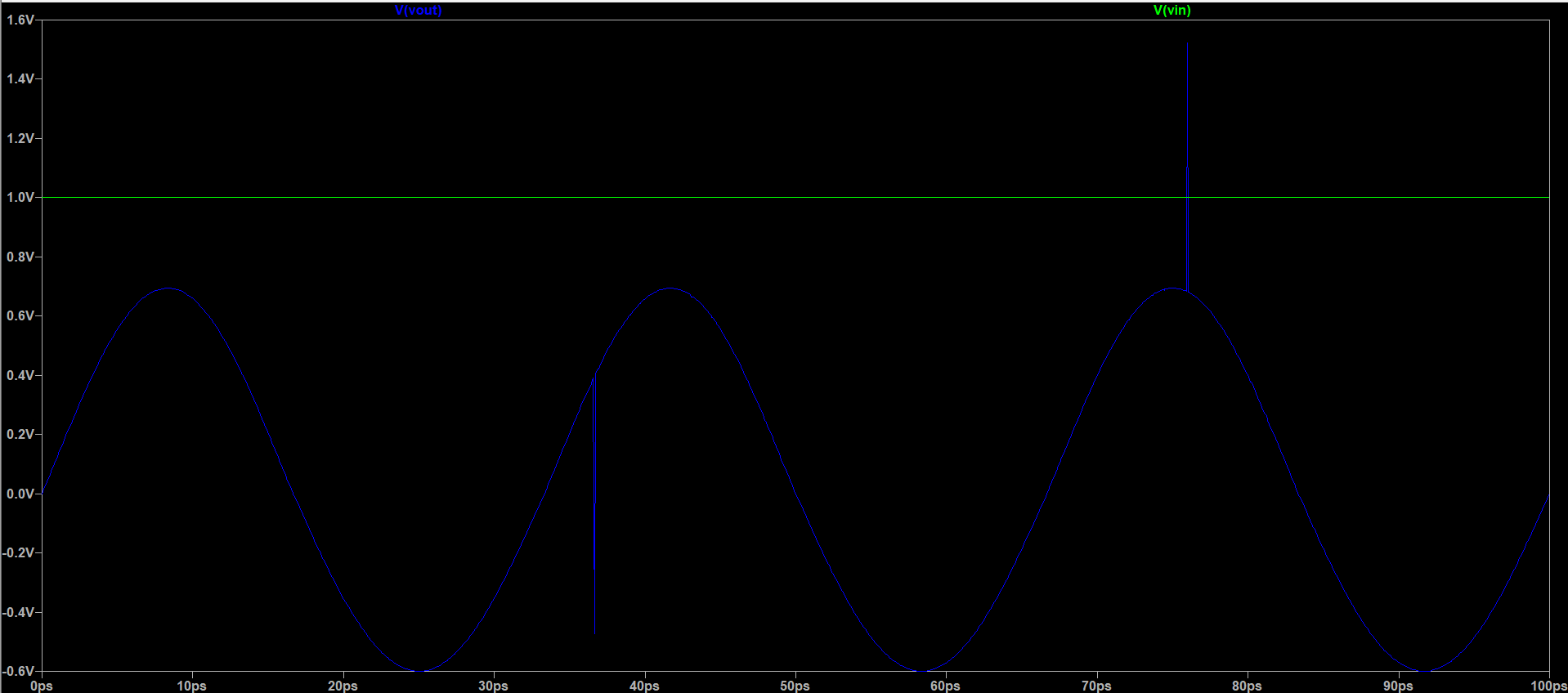
**Simulation of current starved oscillator**

Fig 7.3 Current starved Oscillator transient response

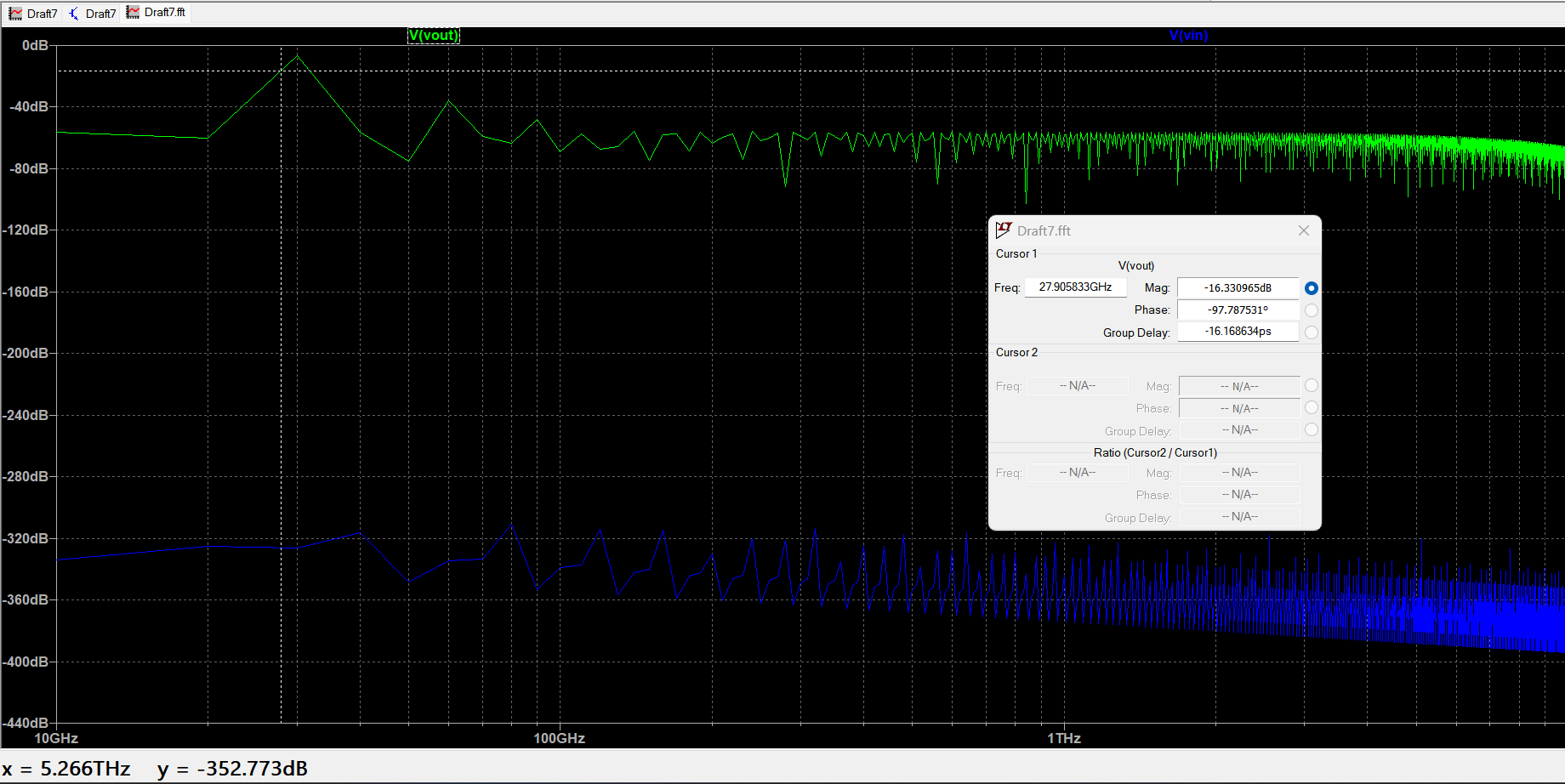


Fig 7.4 Current starved Oscillator fft response

* **Low Power Consumption**: By limiting the current flow through the inverters, it achieves lower power consumption, which is ideal for battery-operated devices.
* Provides the oscillation for 28G frequency with the phase noise of -87.3dB at 1M Hz with FoM of -253.8dBc/Hz

## 7.1.3 Cross coupled Oscillator

**Simulations of cross coupled oscillator**

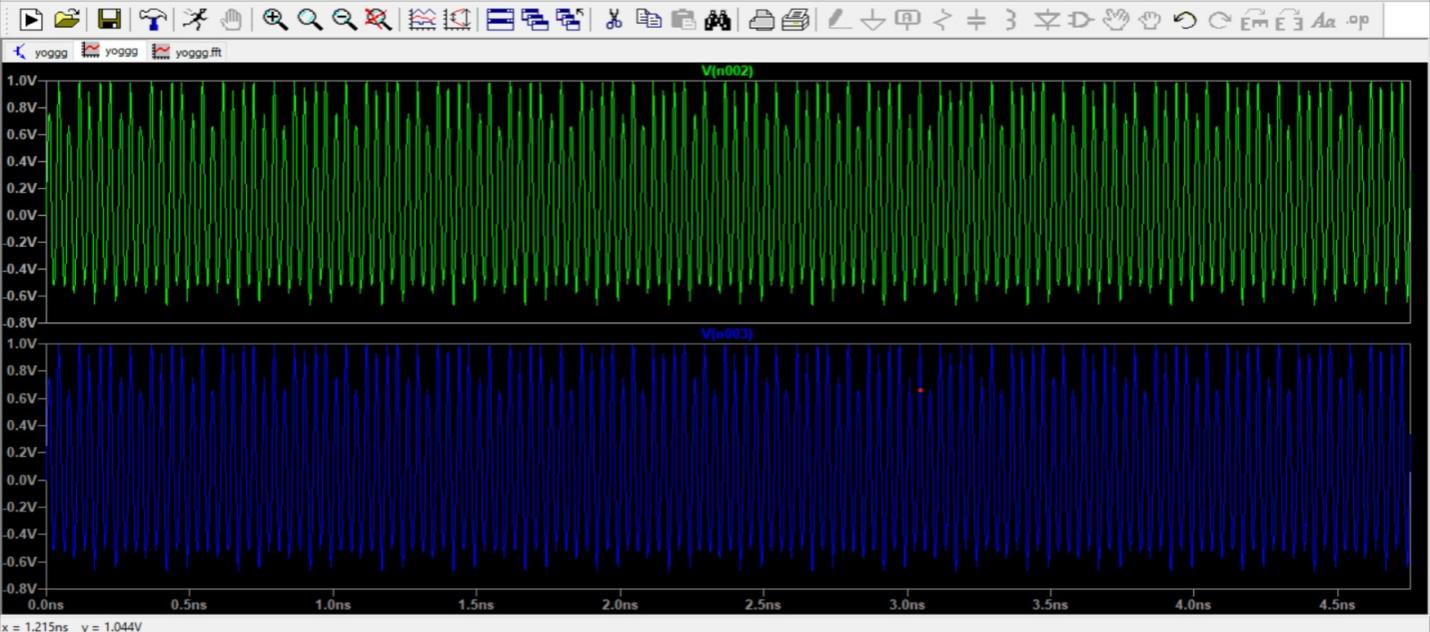


Fig 7.5 Cross Coupled Oscillator transient response

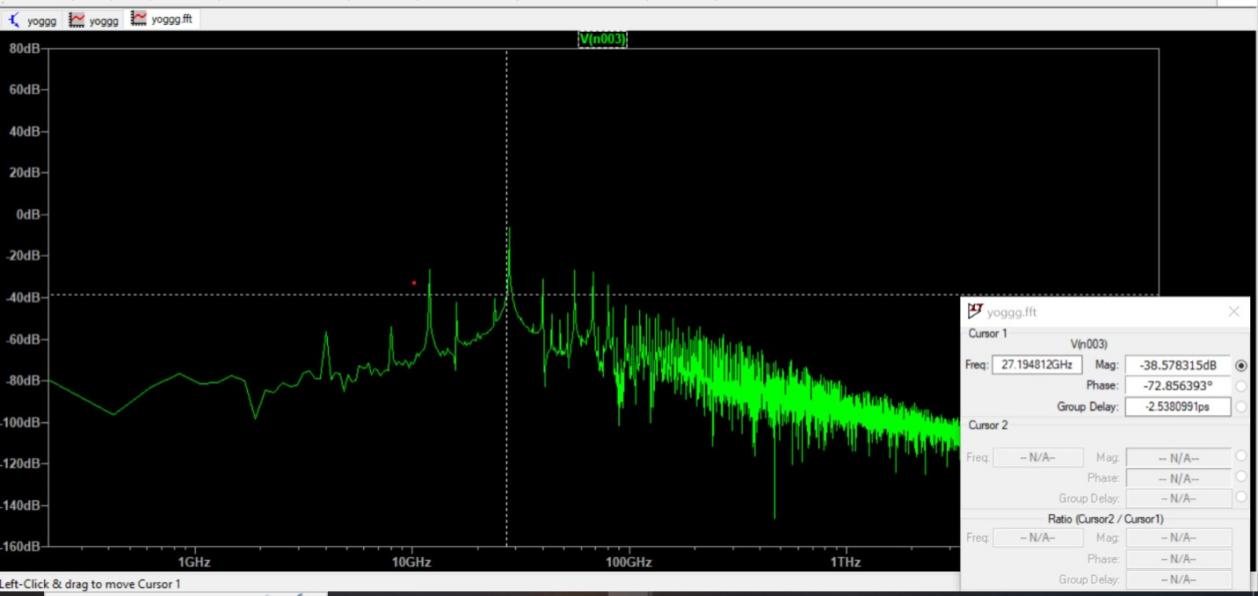


Fig 7.6 Cross Coupled Oscillator fft response

* Cross Coupled Oscillator provides h**igh Phase Noise Performance**: The cross-coupled design provides strong negative resistance, enhancing phase noise performance, crucial for high-frequency communication systems.
* **Differential Outputs**: Offers balanced differential output signals, reducing common-mode noise and improving signal integrity in communication circuits.
* Provides the oscillation for 28G frequency with the phase noise of -132.26dB at 1M Hz with FoM of -198.1dBc/Hz

## 7.1.4 Current reuse Oscillator

**Simulations of current reuse oscillator**

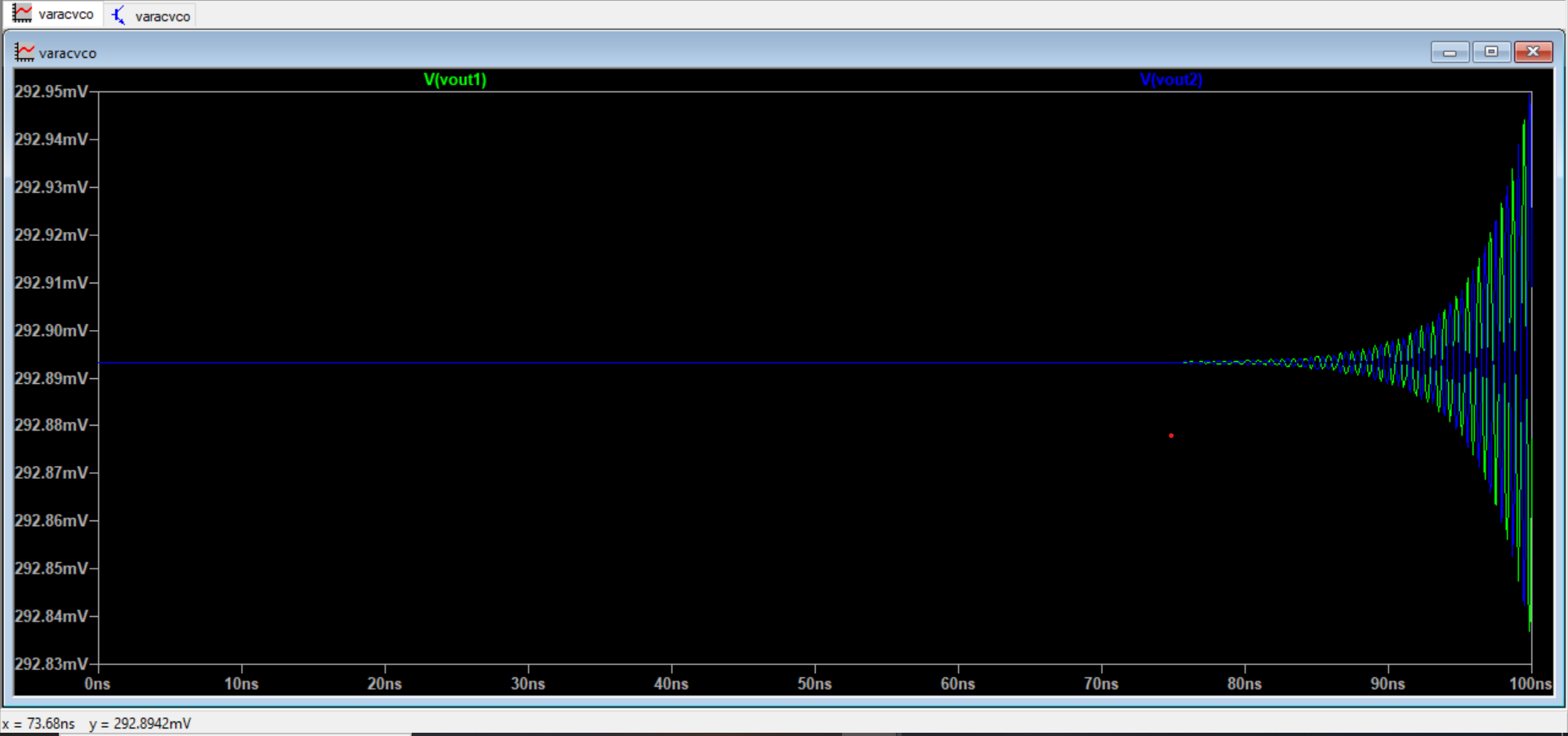


Fig 7.6 Current reuse transient response

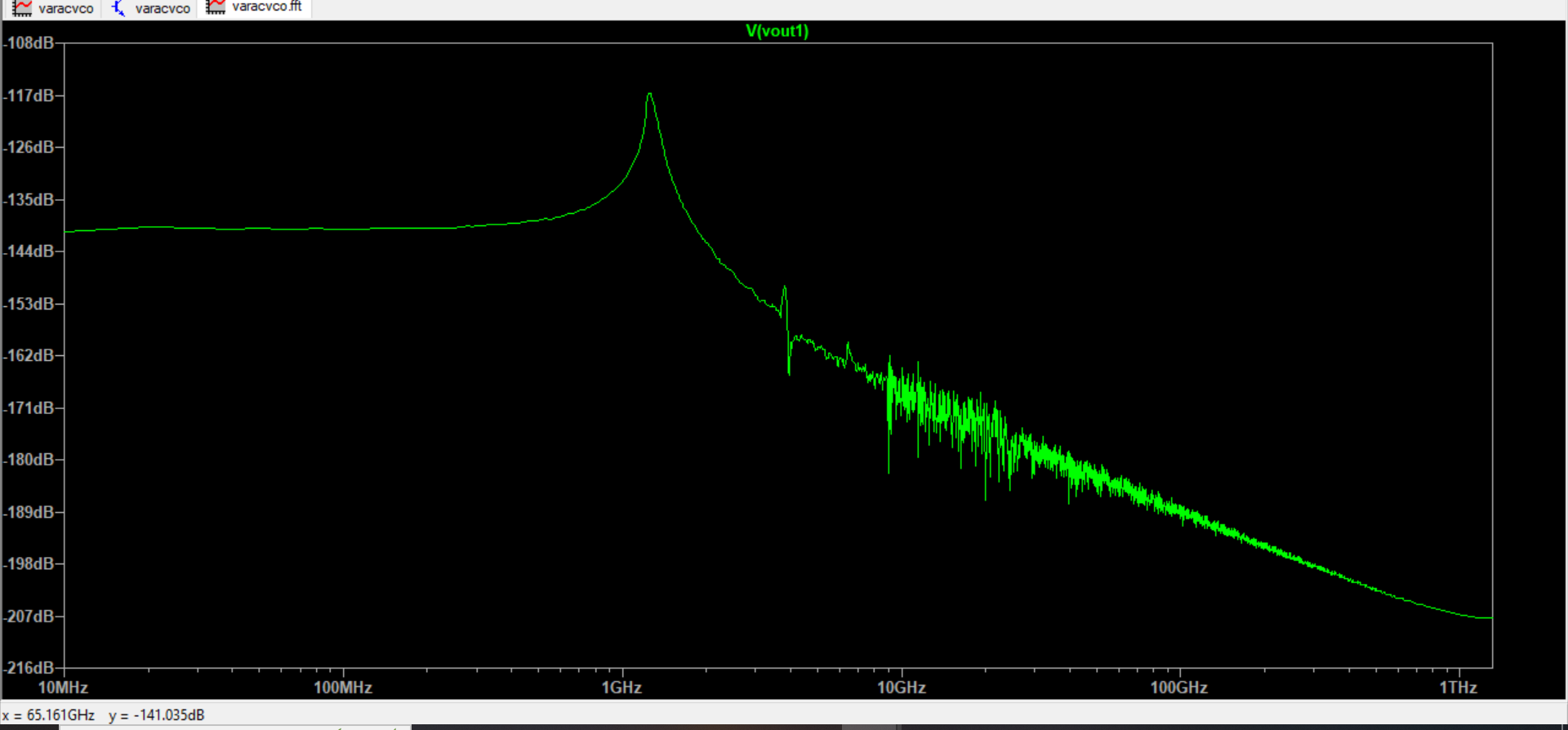


Fig 7.7 Current reuse fft response

* **Current reuse is a power efficiency** Reuses the current within the oscillator stages, significantly reducing overall power consumption, which is beneficial for energy-efficient 5G mobile applications.
* **Compact integration f**acilitates the integration of multiple oscillation functions within a single circuit, saving space and reducing the size of the oscillator module in compact devices.
* Provides the oscillation for 28G frequency with the phase noise of -133.dB at 1M Hz with FoM of -206.08dBc/Hz

# 7.2 Performance Analysis

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Oscillator Topology | Ring oscillator | Current starved | Cross coupled | Current reuse |
| Mid band Frequency  (1G-10G Hz) | 6.24G | 1.2G | 4.02G | 5.204G |
| Phase noise@1MHz  (dBc/Hz) | -124.2 | -87.3 | -132.16 | -133 |
| Figure of Merit  (dB/Hz) | -206.8 | -153.4 | -198.10 | -206.02 |
| Power consumption(mW) | 0.903m | 0.657m | 4.11m | 1.35m |

The Comparative analysis of Cross Coupled and current reuse topologies

|  |  |  |
| --- | --- | --- |
| Oscillator Topology | Cross coupled | Current reuse |
| High band Frequency  (27G-50G Hz) | 27 | 27 |
| Phase noise@1MHz  (dBc/Hz) | -41.1 | -127 |
| Figure of Merit  (dB/Hz) | -102.877 | -215.33 |
| Power consumption(mW) | 1.6m | 3.0m |

# 7.3 Applications

Current reuse oscillator design offers significant advantages for 5G mobile applications:

1. Power Efficiency: Reduces power consumption, extending battery life.

2. Compact Design: Allows smaller, integrated circuits, fitting within space-constrained devices.

3. Enhanced Linearity: Maintains signal quality, reducing distortion.

4. Cost-Effective Production: Simpler designs lower manufacturing costs.

5. Thermal Management: Less heat generation improves reliability.

6. High Frequency Performance: Suited for the high frequencies required in 5G.

7. Improved SNR: Better signal-to-noise ratio for clear communication.

8. Increased Battery Life: Optimized power usage prolongs battery life.

9. Reduced Interference: Minimizes electromagnetic interference.

10. Scalability: Easily adaptable to various 5G applications.

### Chapter 8

Conclusion

Complementary Metal Oxide Semiconductor (CMOS) design of VCO on different topologies provides unique characteristic advantages for specific applications. Here for the 5G mobile application needs features of power consumption, minimum noise, compact and others.

The mid band frequency current reuse oscillator provides the phase noise -133dB and FoM of -206dBc/Hz

The 28Ghz ranged current reuse oscillator provides the low phase noise and reduced FoM which provides the compact circuit that includes tank circuit CMOS with the result of -127dB phase noise and FoM of -215.33dBc/Hz with low power.

A series connected PMOS-NMOS configuration LC resonant tank configuration VCO is designed for 5G band frequencies using 90nm CMOS process.

References

1. Current Reuse Oscillator Design for 5G Mobile Application using 90nm CMOS, K.A. Karthigeyan and S. Radha [IEEE 2022].
2. Design of Millimeter Wave LC Oscillators for 5G Applications, Shravan Ramesh, Nithin M and Harish M Kittur [IEEE 2019].
3. Current reuse RF LC-VCO design for autonomous connected objects, ENIS, University of Sfax, Sfax, Tunisia [IEEE 2018].
4. Low Power Current-reused Voltage-Controlled Oscillator with Optimum Source Damping Resistors, Chien-Hsuan Liu, Chia-Yo Chan, Ruey-Lue Wang, and Yun-Kuin Su [IEEE 2007].
5. Design and Study the Performance of a CMOS-Based Ring Oscillator Architecture for 5G Mobile Communication ,Abdul Rahman ,Siddharth Kishore, A. R. Abdul Rajak 1.
6. Design of low phase noise and low power modified current-reused VCOsfor 10 GHz applications, Meng-Ting Hsu a,b,n, Wei-Jhih Li b, Chien-Ta Chiu b.
7. Low-power low-phase noise VCO for 24 ​GHz applications. pP anelAbrar Siddique, Tahesin Samira Delwar, Murod Kurbanov, Jee-Youl Ryu 2020.
8. "Design and Analysis of 15.8 GHz LC-VCO Using PMOS Cross Coupled," D. -X. Mai, S. Bui and T. -K. Nguyen, 2019 31st International Conference on Microelectronics (ICM).
9. "Design of 6.7 GHz ˜ 7. 518 GHz Cross Coupled LC-VCO in 180nm CMOS technology," S. S. S and S. S. Yellampalli,2021 5th International Conference on Computing Methodologies and Communication (ICCMC).
10. “An advanced low power low noise 2.45 ghz current reuse -gm cmos cross coupled vco for wsn” Arnov Mukherjee1, Pankaj Rangaree2 ,Dr.G.M.Asutkar3.